
**Plasma Treatment Method for Ohmic Contacts on Zinc Oxide Thin Film Transistors**

THESIS

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# PLASMA TREATMENT METHOD FOR OHMIC CONTACTS ON ZINC OXIDE THIN FILM TRANSISTORS

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# Abstract

This research utilizes plasma treatments as a method to decrease the contact resistance on zinc oxide (ZnO) thin film transistors (TFT). In recent years, researchers have achieved gigahertz RF switch cutoff frequency with ZnO TFTs. To further increase the cutoff frequency, the total resistance of this device must be minimized. Modern ZnO TFTs are fabricated with submicron channel lengths, which contains minimal resistance due to the TFT channel, making contact resistance significant to the total resistance of the device. This research developed a method to integrate plasma treatments into the fabrication of ZnO TFT to decrease the contact resistance, thus increasing the cutoff frequency of the device. Three plasma treatment methods were used, including Ar plasma generated in an inductively coupled reactive-ion etch (ICP-RIE) chamber, Ar plasma applied in-situ in a metal-sputter chamber before sputtering tungsten (W) contacts, and by remotely generated hydrogen plasma. The plasma treatments were implemented after the deposition of ZnO and prior to the deposition of sputtered tungsten (W) contacts. The plasma treatments increased the conductivity of the ZnO, which allowed for the formation of ohmic contacts on the ZnO TFT. The contact resistance of the untreated ZnO TFT sample was 1.9 ohm-mm, while the ICP-RIE Ar plasma treatment, in-situ Ar plasma treatment, and H plasma treatment demonstrated minimum contact resistances of 1.2, 1.0, and 1.5 ohm-mm respectively. The in-situ Ar plasma treatment demonstrated the best results, with a decrease in contact resistance of 47%.

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*This work is dedicated to my lovely wife and three daughters. They are my greatest supporters and source of motivation. I could not have completed this work without my wife's constant devotion to our family.*

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Blaine Z. Underwood

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PLASMA TREATMENT METHOD FOR OHMIC CONTACTS ON ZINC OXIDE THIN FILM TRANSISTORS

# I. Introduction

## 1.1 Background

Zinc oxide (ZnO) has dramatically grown in interest to the semiconductor industry due to its desirable characteristics as a thin film transistor (TFT) active layer. Specifically, ZnO maintains high-performance electrical properties while in the amorphous and nanocrystalline form, which allows it to be deposited on a wide range of substrates instead of being limited to the typical silicon wafer substrate [7]. The freedom to choose specific substrates allows for improved integrated circuit functionality, such as heat dissipation and insulation. ZnO also has a large bandgap, making it transparent to the visible light spectrum and useful in high-power applications. Previous studies have even shown ZnO to maintain its semiconductor properties on flexible substrates, opening up the applications for flexible electronics. The listed characteristics make ZnO a versatile material for use in a wide range of electronics including flat-panel displays, wearable electronics, monolithic integration of high-performance devices and even electronics integrated directly onto the windshield of vehicles.

## 1.2 Problem Statement

This research focuses on using ZnO TFTs for RF switching devices. Researchers have created a nanocrystalline ZnO TFT that is capable of achieving an RF switch

cutoff frequency of 25 GHz, which is the highest reported for a metal-oxide semiconductor [2]. With optimization, this device is expected to achieve a cutoff frequency greater than 500 GHz [8]. This research optimizes the ZnO TFT further by decreasing the contact resistance between the tungsten (W) contacts and the ZnO surface. This was accomplished through the use of post-deposition plasma treatments. The cut-off frequency of a TFT is inversely proportional to the contact resistance; therefore, the cutoff frequency is increased by decreasing the contact resistance in the TFT.

### 1.3 Limitations

There are many factors demonstrated in research that affect contact resistivity, including the type of metal used for contacts, annealing metal contacts, ZnO surface treatments, ZnO thickness, and ZnO deposition conditions. Previous research at AFRL has demonstrated ZnO TFTs with the highest charge mobility reported for ZnO[9]; therefore, the same settings were used in this research for the deposition of the ZnO. Post-deposition plasma treatments were utilized in this research for decreasing contact resistance. This research also used W contact metal because it has been shown in previous research to create an ohmic contact that can also be selectively etched on ZnO [2]. The methods of plasma surface treatments are limited by the available equipment in the AFRL and AFIT cleanrooms. The machines used to generate the plasma for this research are the inductively-coupled reactive-ion etch (ICP-RIE) system, an atomic layer deposition (ALD) system, and a metal-sputtering system.

## 1.4 Approach

### 1.4.1 Plasma Surface Treatment.

This work concentrates on decreasing contact resistivity of ZnO TFTs through a post-deposition treatment with hydrogen and argon plasma. Treating metal-oxide semiconductors with these plasmas have demonstrated a reduction in surface resistivity in other studies, but the implementation of these treatments in a microwave device has not been shown. The listed plasmas can be used to bombard the surface of the metal oxide with ions and increase the free electron concentration of the material. This increase in negative charge carriers brings the Fermi energy level of the ZnO closer to the conduction band energy level. The increase in conductivity of the surface of the ZnO allows for an ohmic contact to form between the ZnO and the contact metal, thus significantly decreasing the voltage drop across the junction and minimizes the overall resistance of the ZnO TFT. After the minimization of contact resistance by plasma treatment, the cutoff frequency of the ZnO will be increased.

### 1.4.2 Channel Recovery.

After the use of surface treatments to create a conductive layer of ZnO, the channel region of the ZnO TFT will no longer be a semiconductor and will act as a conductor. This research would like to keep the conductive surface in the contact regions, but retain the as-deposited semiconductor properties in the channel region. Since the entire ZnO surface will be treated, the channel region of the TFT will also be more conductive, which is not ideal for the performance of the TFT; therefore, a channel recovery experiment will be performed after the surface treatment experiment. The channel recovery experiment will utilize plasma treatments and annealing to undo the effects of the surface treatments. The source and drain

contacts will be used to mask and encapsulate the contact regions of the TFT to maintain the low contact resistivity in those areas.

## 1.5 Summary

To demonstrate the need for further research in this area, Chapter II will detail the advancements made in metal-oxide TFTs and the limitations of the current technology. Furthermore, it will cover the relevant history of research on ZnO as a semiconductor material, which includes similar experiments that this work utilizes for guidance on treatments that have demonstrated desirable results with ZnO. Chapter III will frame the method for the next steps to take based on the literature and determine the test structures that should be fabricated. The results of the fabricated test structures will be discussed and analyzed in chapter IV. Chapter V will summarize the results of this work, draw conclusions based on those results and provide guidance on the next steps that can be taken to further the advancements in this area of study.

# II. Literature Review

## 2.1 History of TFTs

Due to its abundant supply in nature, ZnO was one of the first semiconductor materials researched when semiconductor devices were first being developed in the 1940s [1]. ZnO naturally occurs as an n-type semiconductor, and researchers quickly lost interest in it because of the difficulty in creating p-type ZnO. The cause of the as-grown n-type conductivity is highly debated in the literature, but in recent years, research has pointed to hydrogen contamination as the most likely cause [10]. The lack of p-type conductivity restricted ZnO to use as the active material in thin film transistor devices, which were limited to low-performance applications as compared to single-crystal Si transistors. The invention of active-matrix-liquid crystal displays in the 1960s erupted a huge demand for thin-film transistors, especially for the flat panel display industry [5]. The most common TFT semiconductor material in this industry is hydrogenated amorphous Si (a-Si:H) TFTs. The low charge mobility and low breakdown voltage of a-Si:H is inadequate for high-speed, and high power electronics, but is still useful in low-frequency applications like flat panel displays which are used in televisions and smartphones screens today. In the early 2000s, thin-films were considered for high-performance applications when researchers discovered the much more superior properties of metal-oxide semiconductors as compared to a-Si:H.

## 2.2 Metal Oxide TFTs

TFTs are most commonly used in large flat panel displays such as television screens, and phone screens. Flat panel displays are usually built on glass instead of Si wafers, so traditional bulk silicon transistors cannot be used, while TFT active

layers, such as ZnO, can be deposited directly onto glass substrates. The most common active layer material used in visual display TFTs is a-Si. Researchers are looking to replace the a-Si:H, which has a very low charge mobility of 1 $cm^2$/V-s. Metal oxide semiconductors, ZnO specifically, have displayed a mobility of up to 110 $cm^2$/V-s [7]. The conduction band in metal oxides is composed of overlapping ns-orbitals. The ionic bonds in metal oxides cause the ns-orbitals to have an isotropic shape, which allows metal oxides to maintain orbital overlap and high charge mobility even in amorphous form. Figure 1 demonstrates the overlap of the spherical ns-orbitals for crystalline and amorphous metal oxides[11].

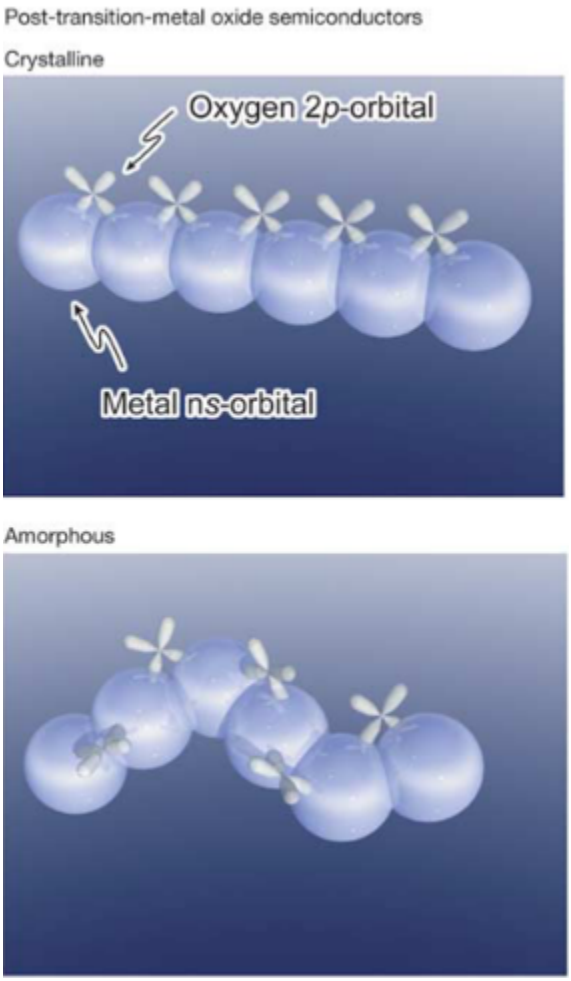



**Figure 1. The top figure is a model for crystalline metal-oxide orbitals while the bottom figure is for amorphous metal-oxide orbitals. The large spheres are metal ns-orbitals which maintain an overlap for conduction even in amorphous form. [11].**

Conduction in a-Si is dependent on the $sp^3$ orbitals, in which the orbital overlap is highly dependent on directivity due to the covalent bonds of Si [11]; hence, in amorphous form, the orbital overlap is decreased greatly, which results in a low charge mobility for the semiconductor. Figure 2 demonstrates the overlap of the $sp^3$orbitals for crystalline and amorphous Si [11].

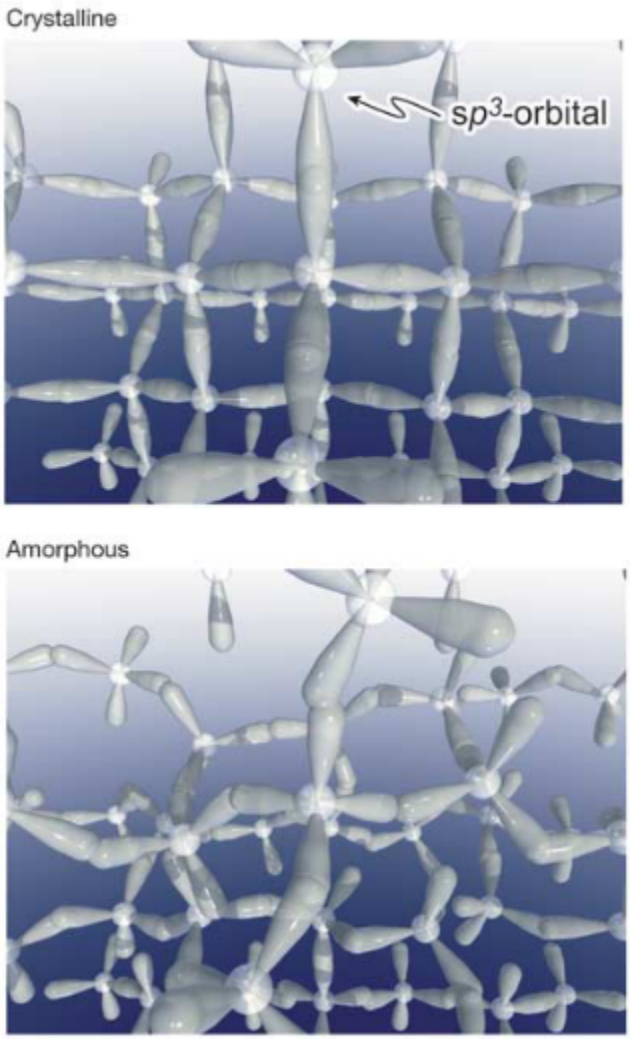



**Figure 2. The top figure is a model for crystalline silicon orbitals while the bottom figure is for amorphous silicon orbitals. There is a much smaller overlap of the $sp^3$-orbitals in the amorphous form [11].**

## 2.3 ZnO Semiconductor Properties

ZnO is a semiconductor material that has been researched extensively since the creation of semiconductor devices. It is an abundant material from nature and can be grown as large single-crystals. In the early days of semiconductor development, researchers initially lost interest in ZnO due to the difficulty in achieving p-type conductivity. Researchers would like to control the conductivity of ZnO, whether that be making it display more or less n-type conductivity. To be able to adjust the electrical conductivity of ZnO, one must first understand the mechanism which causes n-type conductivity in the ZnO crystal lattice structure.

### 2.3.1 n-Type Conductivity.

ZnO exhibits an inherent n-type conductivity when grown. The cause of this conductivity is due to the introduction of impurities and defects during the growth process. Van de Walle argues that hydrogen impurities are the most likely cause of the n-type conductivity because hydrogen is difficult to eliminate from the growth process [10]. Hydrogen has a strong affinity for oxygen and acts as a shallow donor when bonded to oxygen [1]. Hydrogen also acts as a donor by filling oxygen vacancies in ZnO [1]. Other researchers argue that native defects such as zinc interstitials are the cause of the n-type conductivity [12].

## 2.4 ZnO Native Defects

ZnO always occurs as an n-type semiconductor, but the cause of this conductivity is highly debated in the literature. Researchers seek to control the conductivity of ZnO and therefore must understand what causes the n-type conductivity. The native defects identified as possible n-type donors are oxygen vacancies and Zn interstitials, which are covered in the following sections.

### 2.4.1 Oxygen Vacancy.

Oxygen vacancies are an intrinsic defect in the as-grown ZnO crystal structure. It is the most frequently mentioned native defect for ZnO in literature. Many publications state that the oxygen vacancy acts as a donor and is a contributor to the n-type conductivity of ZnO, but recently this has been proven not to be the case [13]. The oxygen vacancy is a deep donor in ZnO with an approximate transition level 1.0 eV below the conduction band and therefore should not contribute to conductivity [13]. The concentration of oxygen vacancies can be manipulated by controlling the oxygen levels in the ZnO crystal growth process. In oxygen-rich environments, the formation energy of oxygen vacancies increases, which decreases the likelihood of the defect occurring during crystal growth [1, 14].

### 2.4.2 Zn Interstitials.

Zn interstitials ($Zn_i$) are another native defect of ZnO that is often debated in the literature about its role in contributing to the n-type conductivity of ZnO. The $Zn_i$ occupies either the tetrahedral, or octahedral site in the ZnO wurtzite crystal structure [15]. In this site, the $Zn_i$ donates two electrons to the conduction band, becoming a shallow donor [15]. $Zn_i$ are not stable in this configuration due to small migration barriers as low as 0.57 eV, which allows the $Zn_i$ to diffuse easily out of the ZnO sample [16]. The instability of $Zn_i$ has led many researchers to conclude that the $Zn_i$ is not the cause of the intrinsic n-type conductivity demonstrated in ZnO. Look *et al.* determined that $Zn_i$ becomes a stable donor by bonding to N, which commonly substitutes for O in ZnO [12]. Once bonded to $N_O$, the $Zn_i$ contributes one electron to the conduction band, becoming a shallow donor [12]. It is unlikely that this bond would occur in significant concentrations due to the relatively large formation energy of the $Zn_i$; therefore, the $Zn_i$-$N_o$ complex is probably not the cause

of n-type conductivity in ZnO [16].

## 2.5 ZnO Growth Process

ZnO crystallizes in the wurtzite crystal structure shown in Figure 3. ZnO is commonly available as a bulk crystal, and can also be grown in amorphous and polycrystalline forms [1]. The ZnO used in this research is a nanocrystalline thin-film. Nanocrystalline is a type of polycrystalline material in which the crystallites measure on the nano-scale. A benefit to using nanocrystalline ZnO, instead of crystalline, is that it is substrate agnostic, which opens up its potential applications with the freedom to choose substrates with desirable properties for the finished product. As mentioned previously, ZnO still maintains its electrical properties in amorphous form due to the large ns-orbitals. These properties enable researchers to use ZnO grown by many different methods, including bulk crystal growth, pulsed laser deposition (PLD), atomic layer deposition (ALD), and oxidation. This research will utilize the PLD method for depositing ZnO.

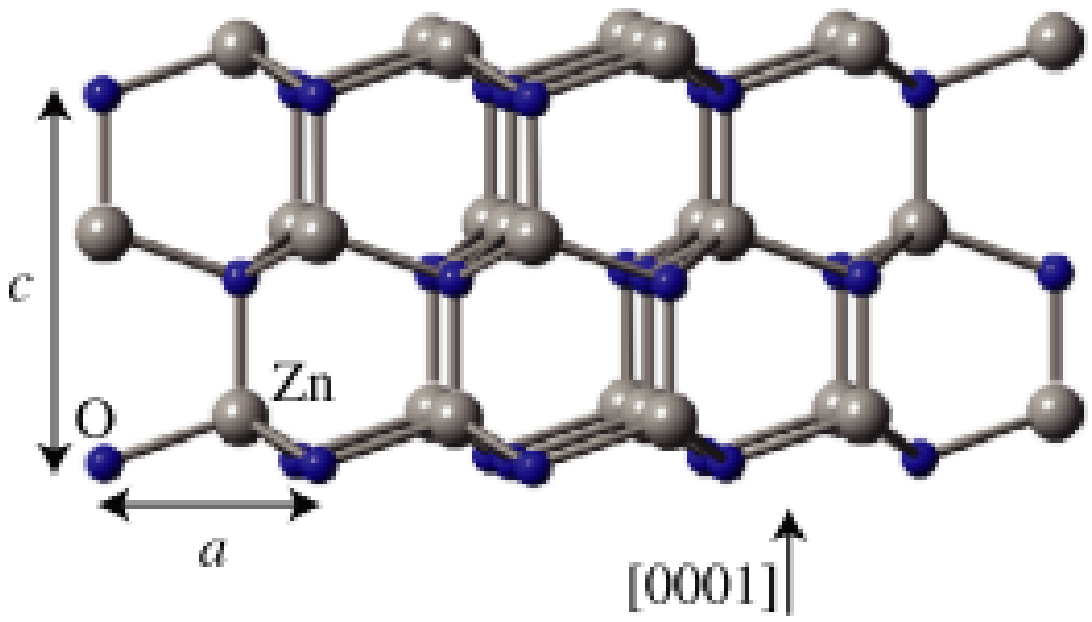



**Figure 3. Wurtzite crystal structure of ZnO [1].**

### 2.5.1 Pulsed Laser Deposition of ZnO.

Pulsed laser deposition is a method used in the semiconductor industry to deposit thin-films of material on a substrate. This method involves emitting a high-power laser aimed at a target. The laser scans across the target as the target revolves, to ensure uniform deposition of material. The laser pulses at a set frequency and evaporates the target material into a plume, which then condensates onto the substrate. The material slowly builds up thickness on the substrate until the desired thickness is achieved, usually on the nanometer scale. The PLD method commonly used for ZnO deposition in research because it has achieved high-quality ZnO films at relatively low temperatures and is not substrate dependent. An example of the high-quality properties of PLD ZnO is the ZnO TFT devices created by AFRL, in which a drain–current ON/OFF ratio of $10^{12}$ and field-effect mobility of 110 $cm^2$/V-s were achieved [7].

## 2.6 ZnO TFTs

ZnO TFTs have many practical advantages over its single crystal counterparts because the disordered structure allows it to be substrate agnostic and also flexible while maintaining its semiconductor properties [11]. ZnO has gained interest in recent years to replace a-Si:H as the primary TFT active layer used in visual displays due to its superior semiconductor properties. As mentioned previously, a-Si:H TFTs demonstrate a low charge mobility up to 1 $cm^2$/V-s, while ZnO TFTs have achieved a charge mobility up to 110 $cm^2$/V-s [1]. ZnO is also a wide bandgap semiconductor, with an energy gap of 3.37 eV, making it transparent to visible light and useful in high-power applications [11]. Using this PLD ZnO, AFRL created a transistor with a channel length of 0.75μm and a measured cutoff frequency of 25 GHz [8]. It is estimated that with further optimization, the ZnO TFT could achieve a cutoff frequency of over 500 GHz [8]. These electrical characteristics of ZnO TFTs not only make it useful for visual displays but could allow for its use in place of high-performance single-crystal semiconductors while allowing for transparent and flexible applications.

## 2.7 ZnO Ohmic Contacts

High-performance TFTs must have ohmic contacts with negligible contact resistances. An ohmic contact demonstrates a linear IV characteristic as governed by Ohm's Law. This means that the contact resistance is constant for forward and reverse biasing. For an ohmic contact to be created, a metal with a work function less than, or relatively close to the electron affinity of the semiconductor must be used. ZnO has an electron affinity of approximately 4.35 eV; therefore, metals such as Al and Ti are commonly used to create ohmic contacts because their work function is less than 4.35 eV[17]. The potential barrier height is equal to the

difference between the semiconductor conduction band energy level, $E_c$, and the Fermi energy level, $E_f$. Figure 4 displays the band diagram of a titanium contact on ZnO.

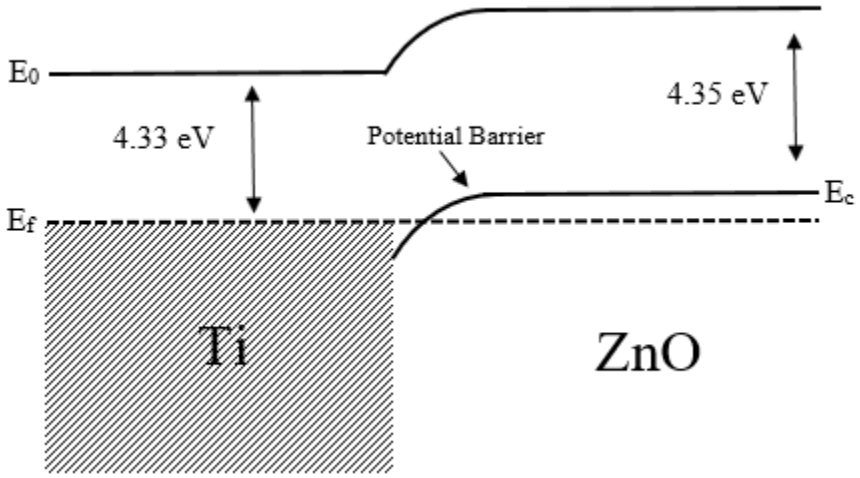



**Figure 4. Energy band diagram for a Ti contact on ZnO.**

Metals with slightly larger work functions than the semiconductor electron affinity can also be used to create ohmic contacts. In the case of ZnO, tungsten (W) is used because its work function, 4.5 eV, is slightly larger than the ZnO electron affinity. The potential barrier height for this type of contact is equal to the difference between the metal work function and the semiconductor electron affinity. Figure 5 displays the energy band diagram for a tungsten contact on ZnO.

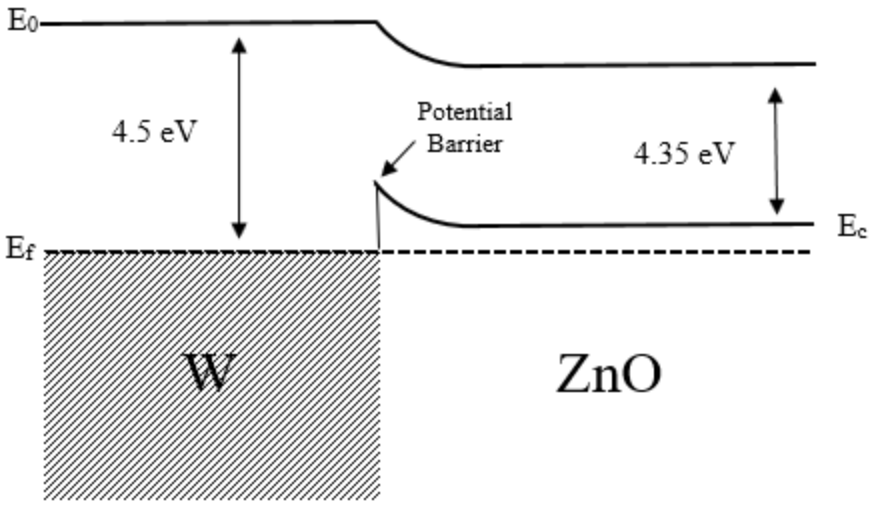



**Figure 5. Energy band diagram for a W contact on ZnO.**

The contact resistance of these contacts can be reduced by increasing the doping concentration at the semiconductor surface. Increasing the doping concentration would decrease the barrier height for the Ti contact on ZnO, which allows for a greater amount of thermionic emission of electrons over the potential barrier. In the case of the W contact on ZnO, an increased doping concentration would decrease the barrier width and allow for more electrons to tunnel through the barrier due to field emission. For traditional semiconductor materials, such as silicon, increased doping concentrations are accomplished by using the n-type dopant, phosphorous, and diffusing it into the silicon in a diffusion furnace. This traditional process is not compatible with metal-oxide semiconductors because the phosphorous atoms do not bond readily to the metal oxide atomic structure and, therefore, do not contribute to conduction, not to mention that high-temperature annealing can negatively alter the composition of the ZnO material. New techniques must be developed to create a highly doped surface layer on ZnO.

## 2.8 Selective Etch Contact Method

ZnO TFTs are typically limited to relatively long channel lengths of >1 µm. The large channels are due to difficulties in selectively etching metal contacts, so a liftoff process is typically used to form the contacts instead. In 2014, a student at the Air Force Institute of Technology (AFIT) developed a method to selectively etch tungsten from the surface of the ZnO TFT to form source and drain contacts [2]. This process used e-beam lithography for sub-micron patterning of the channel. A plasma-assisted etch (PAE) was used to selectively remove the tungsten from the TFT channel region. A channel length of 200 nm was achieved using this method [2]. A scanning electron microscopy (SEM) image of the cross-section of a selectively etched W contact on ZnO after PAE is shown in Figure 6.

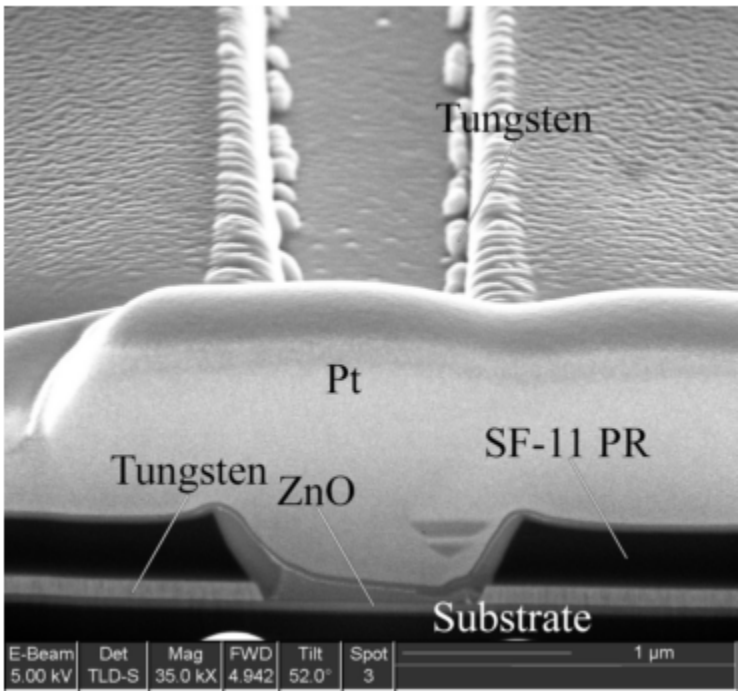



**Figure 6. SEM image of the cross-section of a W contact on ZnO after PAE [2].**

## 2.9 Plasma Treatment Solution

A proven method of increasing the carrier concentration of ZnO is the use of plasma treatments [18, 19, 20, 21]. Plasma treatment of ZnO occurs after the deposition of the ZnO onto a substrate. The ions in the plasma interact with the ZnO and affect the carrier concentration near the surface. Commonly used plasmas for plasma treatments are hydrogen, argon, and oxygen [18, 19, 20, 21]. The listed plasmas interact with ZnO in very different ways, described in the following sections.

### 2.9.1 Hydrogen Plasma Treatment.

Hydrogen plasma increases carrier concentration in two ways. Hydrogen ions can become donors by filling oxygen vacancies in the ZnO crystal structure and also by implanting in the crystal as an interstitial atom[1]. One must account for the temperature dependence of interstitial hydrogen. At temperatures above $150^{o}$C, interstitial hydrogen diffuses out of the ZnO, lowering the carrier concentration [22]. This presents a problem because, for electronic applications, the donors in ZnO must be stable at higher temperatures. Conversely, substitutional hydrogen in ZnO remains stable at temperatures up to $500^{o}$C [22]. Besides increasing the carrier concentration of ZnO, studies have shown hydrogen also increases the charge mobility in ZnO, contrary to the effects of doping other semiconductor materials [23, 24]. The increase in mobility is due to the large 1s orbital from the H atoms, which increases the number of overlapping orbitals in the ZnO[23]. Figure 7 shows a model of $H_O$ in ZnO with the large 1s orbital [1]. The ball and stick diagram, shown in Figure 8, demonstrates the three different ways hydrogen bonds ZnO, including at the bond-center site, at the antibonding site, and at the substitutional oxygen site[1].

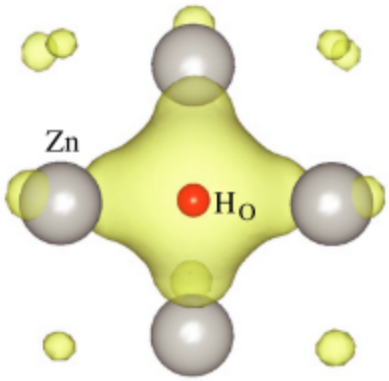



**Figure 7. Model depicts the fully symmetric bonding state of substitutional hydrogen in ZnO [1].**

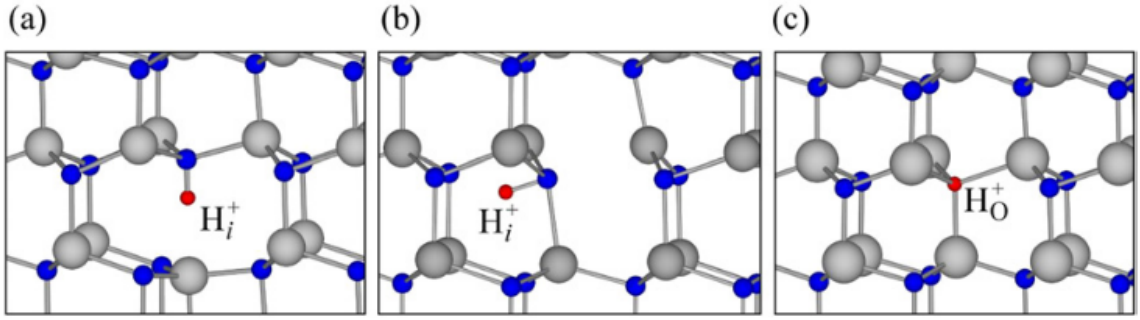



**Figure 8. Ball and stick model of hydrogen dopant bonding locations in ZnO: (a) at the bond-center site; (b) at the antibonding site; (c) at the substitutional oxygen site [1].**

### 2.9.2 Argon Plasma Treatment.

Argon plasma treatment has been shown in recent research to decrease the resistivity at the surface of ZnO by orders of magnitude [19, 21, 25]. The cause of this increased conductivity has not been definitively proven in literature. It is commonly reported that the argon plasma treatment increases carrier concentration by selectively dislodging oxygen from the ZnO [21, 26, 17], but this seems unlikely because more recent research suggests that oxygen vacancies are not directly responsible for the increased carrier concentration near the surface because they act as deep donors and should not contribute to conduction [13]. It is theorized that the

oxygen vacancies could allow for hydrogen to bond as a donor in the vacancy location, which is why there is often a correlation between oxygen vacancies and increased conductivity [1].

## 2.10 Treatments to Decrease Conductivity

In this research, the previous plasma treatments mentioned will be applied to the entire ZnO surface, making it conductive in the contact and channel regions of the device. For this device to operate as a transistor, its channel region must be restored to the original semiconductor state. The ZnO as a semiconductor should be highly resistive at 0 V applied gate bias. A method must be developed to undo the effects of the previous plasma treatments and decrease the conductivity back to a semiconductor state by increasing the resistivity at 0 V gate bias. In literature, two methods that have been reported to increase the resistivity of ZnO are oxygen plasma treatment and oxygen annealing.

### 2.10.1 Oxygen Plasma Treatment.

Oxygen plasma treatments of ZnO have been shown to decrease the threshold voltage by decreasing the number of charge carriers in the conduction band, as shown in Figure 9 [3]. The decrease in carrier concentration also leads to an increase in resistivity, as shown in Figure 10 [3]. The listed properties of oxygen plasma treatments show their potential for use in undoing the effects of the H and Ar plasma treatments. This research will use oxygen plasma treatments for the channel recovery experiment.

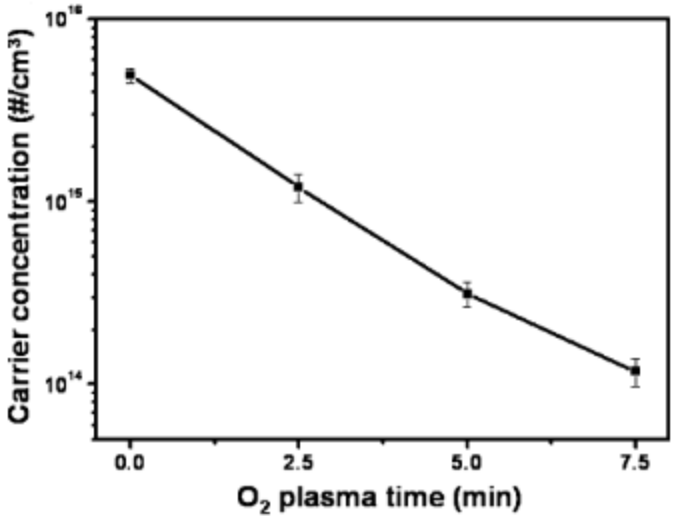



**Figure 9. Carrier concentration of ZnO vs. $O_2$ plasma treatment time [3].**

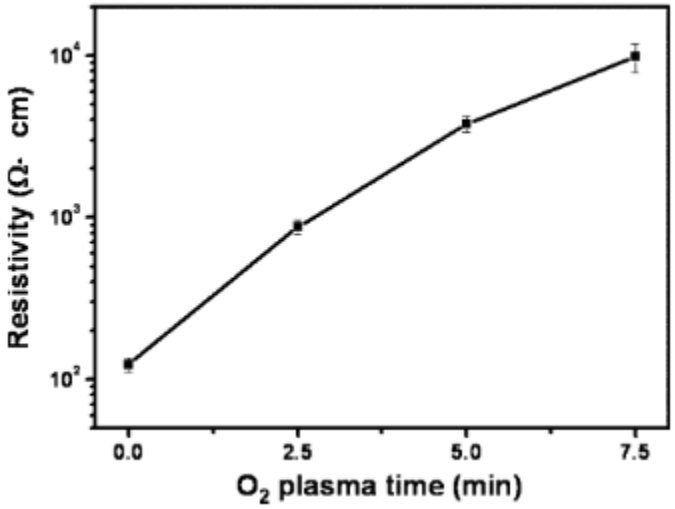



**Figure 10. Resistivity of ZnO vs. $O_2$ plasma treatment time [3].**

### 2.10.2 Oxygen Anneal.

Researchers have demonstrated the creation of ZnO thin-films through the use of oxygen annealing [27, 28]. For some oxygen anneal methods, a thin film of highly conductive Zn is deposited and then annealed in $O_2$ gas. The Zn oxidizes to create a semiconductive ZnO thin film. For this research, $O_2$ annealing will not be utilized to create ZnO, but to make highly conductive ZnO less conductive. Kwang Hwan Ji *et*

*al.* did an experiment using oxygen annealing in which the $O_2$ pressure demonstrated a 2 V increase in the threshold voltage of an InGaZnO TFT. This suggests that the density of charge carriers is decreased by increasing the oxygen pressure during the annealing [29]. In a study by Bouhssira *et al.*, the conductivity of ZnO thin-films was reduced by multiple orders of magnitude utilizing oxygen annealing post-treatment at various temperature levels. In addition to the lower conductivity, an increase in electrical activation energy was reported. Since activation energy is equal to the conduction band energy level minus the Fermi energy level, these results suggest that the oxygen annealing decreased the number of charge carriers in the conduction band. These results are shown in Figure 11 [4].

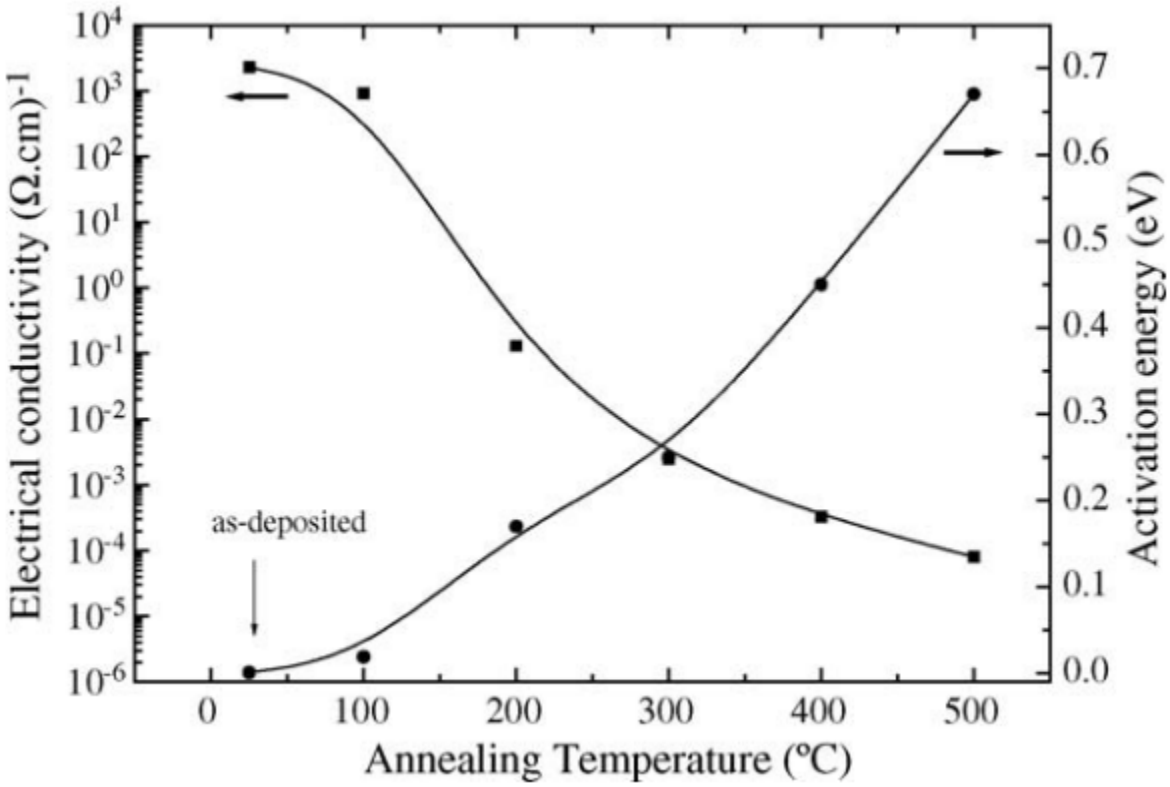



**Figure 11. Electrical conductivity of ZnO thin films and electrical activation energy vs. annealing temperature [4].**

## 2.11 Contact Resistance Measurements

Accurate resistance measurements must be taken to test the effectiveness of the plasma treatments on decreasing the mean contact resistance. For devices as small as the TFTs in this experiment, specialized techniques must be used to accomplish this task. Two common methods used in research are Transfer Length Method (TLM) and Cross-Bridge Kelvin Resistor (CBKR).

### 2.11.1 Transfer Length Method .

TLM is a technique to measure resistance in a device such as a TFT accurately. This method effectively characterizes the ohmic contact and provides the contact resistance and sheet resistance of the active layer of the TFT. To make a TLM measurement, one must first fabricate a TLM structure on the material being characterized. The structure consists of ohmic contacts on the active layer of the TFT spaced at varying intervals shown by L1 and L2 in Figure 12. The resistance between contacts is measured by supplying a constant current through the device and then measuring the resultant voltage drop across the device with a high resistance voltmeter. With a constant current being supplied, a high impedance voltmeter measures the voltage drop between two adjacent contacts in the TLM structure. Using a high impedance voltmeter ensures that no current flows through the voltmeter and all of the voltage drop is across the actual TLM structure. If voltage is forced and current is measured instead, then one must account for the resistance due to the voltage source and probe contacts. The total resistance ($R_T$) of the TLM structure can accurately be calculated by dividing the measured voltage (V) by the supplied current (I) as shown in Equation 1 [30]. A model of a TLM test structure is shown in Figure 12.

$$R_T = V/I. \tag{1}$$

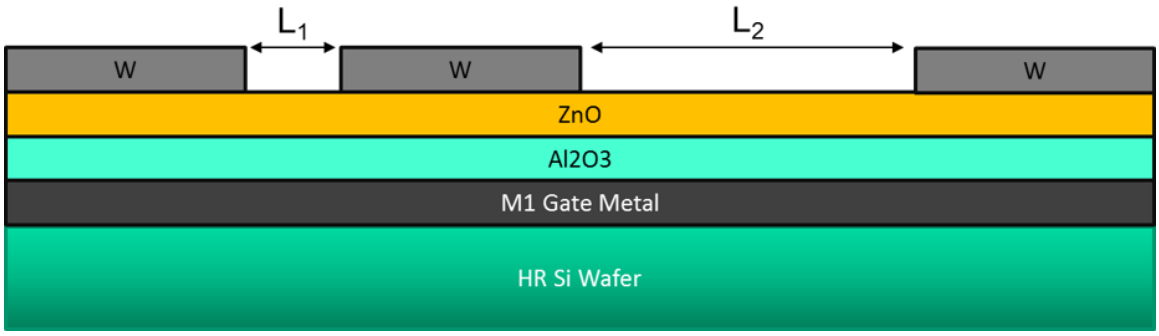



**Figure 12. Cross-sectional model of a TLM Test Structure.**

To isolate the contact resistance from the total resistance, the values of the total resistance, $R_T$, versus transmission length, L, must be plotted, as shown in Figure 13. The y-intercept of the plot is equal to two times the contact resistance, 2 $R_c$. The slope of the trend line is equal to the sheet resistance, $R_{sh}$, multiplied by length and divided by the width of the contact area, W [30]. The x-intercept of the plot is equal to negative-two multiplied by the transfer length, $L_T$[30]. Transfer length is the distance charges travel under a source or drain contact before moving through it, as depicted in Figure 13. The specific contact resistivity, $\rho_c$, can also be calculated using $R_c$, W, and $L_T$, as shown in equation 2.

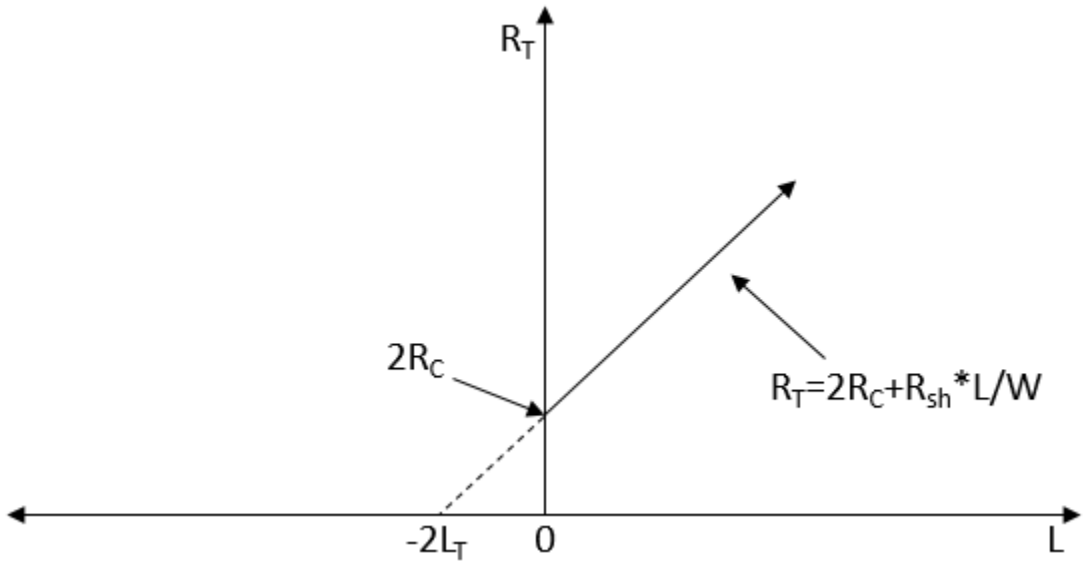



**Figure 13. TLM plot for finding contact resistance, RC, and transfer length, LT.**

$$\rho_c = R_C L_T W \tag{2}$$

The above TLM model does not take into account contact resistance as a function of gate voltage. As gate voltage increases, the contact resistance decreases. Kagan uses a TLM model that plots RT of the TLM device as a function of channel L, at various gate voltages, $V_{GS}$, and finds the common cross-point [5]. The y-intercept for each line is equal to the resistance from the source and drain contacts, $2R_c$, also represented by $R_S+R_D$. As gate voltage increases, the y-intercept decreases slightly, which means $2R_c$ also decreases. The resistance determined by the cross-point, $2R_0$, represents the limit of $2R_c$ for a high gate voltage [5]. This method is demonstrated by the TLM plot in Figure 14 [5].

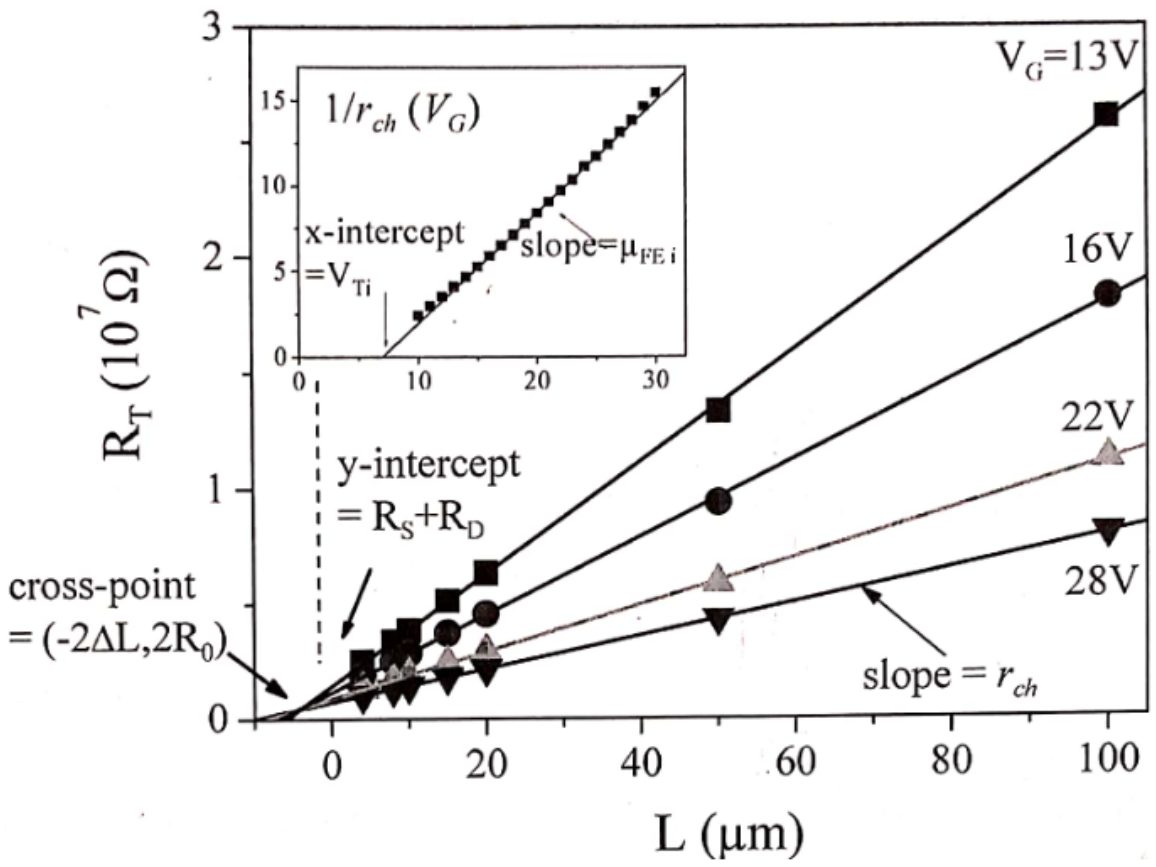



**Figure 14. TLM plot depicting the cross-point of the $R_T$ lines plotted at various gate voltages[5]. $R_S$+$R_D$ equals $2R_c$ for a given $V_G$, and $2R_O$ is equal to the limit of $2R_c$ at a very high gate voltage.**

This method of utilizing a cross-point in the TLM model was designed for hydrogenated-amorphous Si TFTs with a highly-doped ohmic layer under the contacts, shown in Figure 15 [5]. Metal-oxide semiconductors, such as a-IGZO, have been reported not to exhibit this cross-point because they do not have a highly-doped ohmic layer to form contacts on [31], although this finding is still debated among researchers.

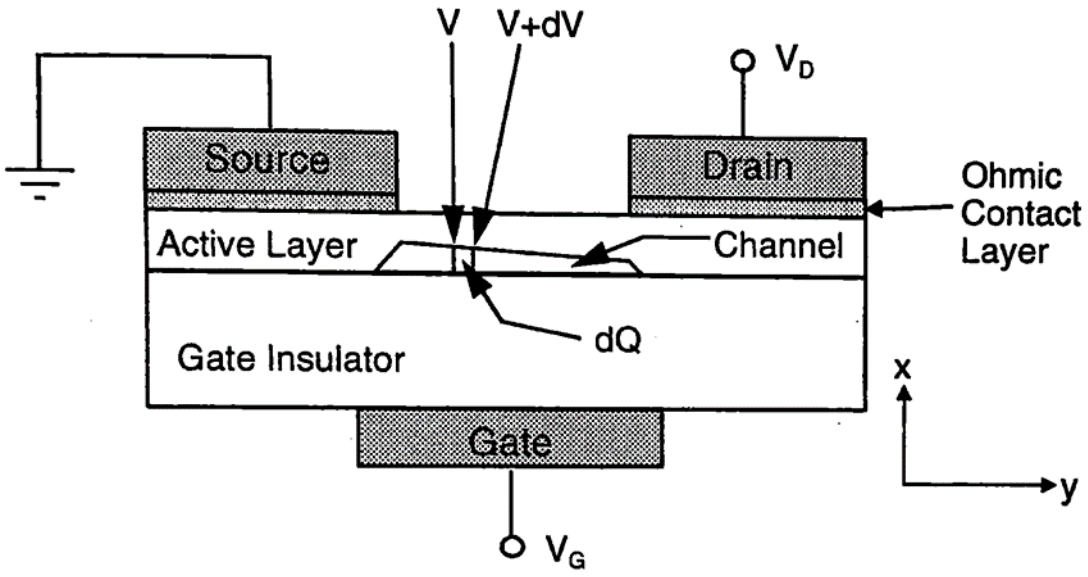



**Figure 15. Cross-sectional model of an a-Si:H TFT with an ohmic contact layer [5].**

For the purpose of this research, the intersection of the two highest gate voltage lines measured will be used to approximate $2R_c$ for each sample. The same two gate voltage lines will be used for each sample so that they can be compared to determine the best method for reducing $R_c$.

### 2.11.2 Cross-Bridge Kelvin Resistor.

Cross-bridge kelvin resistors (CBKR) are commonly used test structures for determining the contact resistivity of semiconductor devices [6]. Standard CBKR test structures consist of four terminals as shown in Figure 16. The measurement is made by forcing a constant current between pads one and two and measuring the resultant voltage drop across pads three and four.

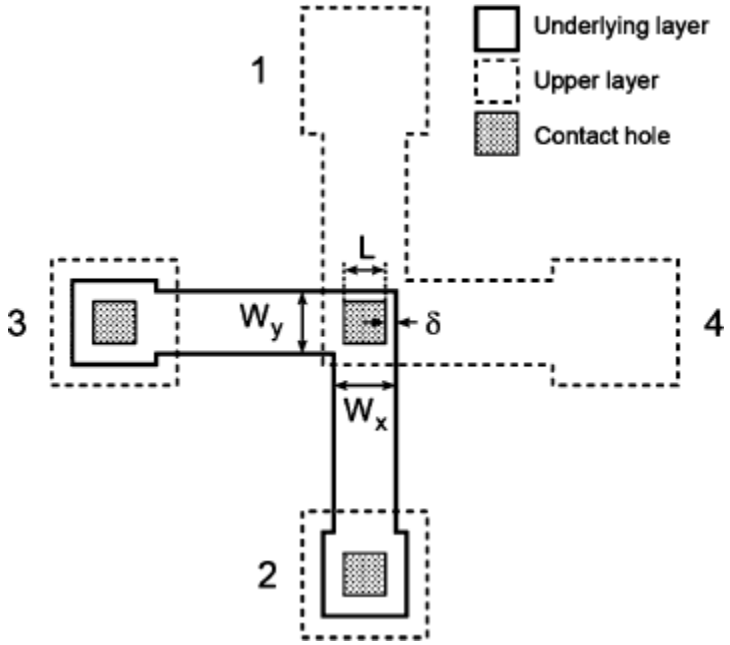



**Figure 16. Four-terminal CBKR structure [6].**

The measured Kelvin resistance is determined by dividing the forced current magnitude divided by the measured voltage drop, just like Equation 1 for the TLM structures. The CBKR method is different from TLM in that the calculated resistance value is equal to the contact resistance. For a one-dimensional model, the contact resistivity can be directly determined from the contact area, A, where A is equal to $L^2$, and the Kelvin resistance, as shown in equation 3.

$$\rho_c = R_k A \tag{3}$$

# III. Methodology

## 3.1 Introduction

The goal of this research is to increase the RF switch cutoff frequency, $f_c$, of a ZnO TFT. An RF switch represents a short in the on-state and high impedance in the off-state. The cutoff frequency is inversely related to both the on-resistance ($R_{on}$) and the off-capacitance ($C_{off}$) of the TFT, as shown in Equation 4

$$f_c = (2\pi R_{on} C_{off})^{(-1)}. \tag{4}$$

Therefore, when the on-resistance of the device is decreased, the cut-off frequency will be proportionally increased, thus improving the performance of the RF switch. The on-resistance of the TFT is the sum of the contact resistance of both contacts on the ZnO, the bulk ZnO resistance and the channel resistance as shown in Equation 5

$$R_{ON} = R_{sh} L_C + 2R_c \tag{5}$$

where $R_{sh}$ is the sheet resistance, $L_C$ is the channel length, and $R_c$ is the contact resistance.

To further increase the cutoff frequency, the off capacitance must be decreased in addition to the on-resistance. The off capacitance is proportional to the gate overlap with the source and drain contacts shown as $L_{OL}$ in Figure 17.

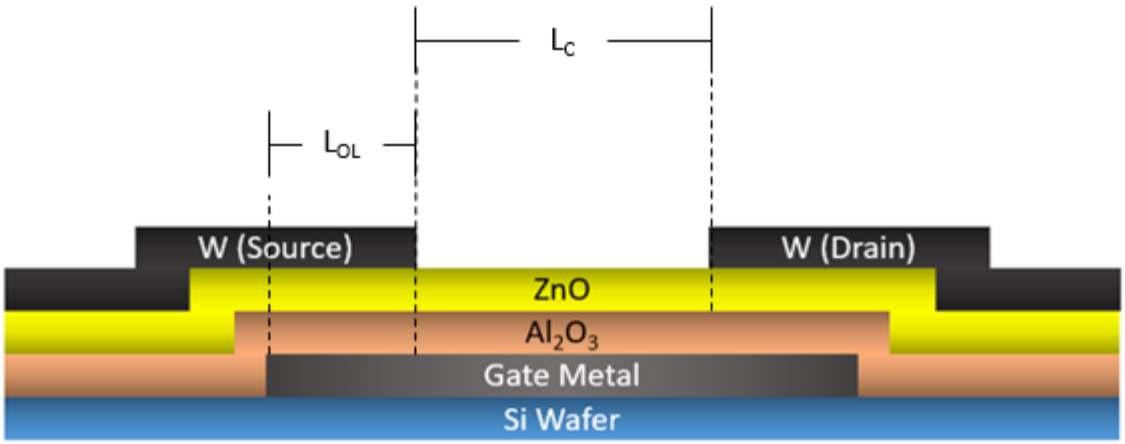



**Figure 17. Cross-sectional model of a ZnO TFT depicting the gate overlap, $L_{OL}$, and the channel length, $L_C$.**

The off-capacitance of the device can be modeled as the equivalent circuit shown in Figure 18.

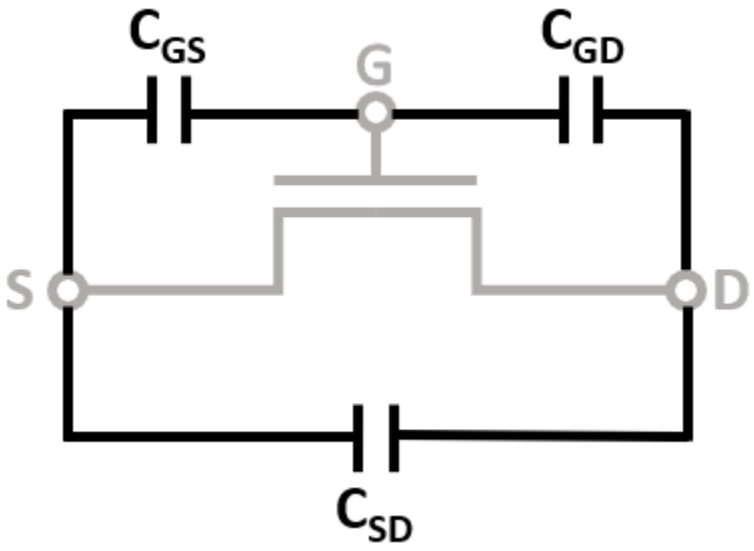



**Figure 18. Equivalent circuit capacitance of a TFT.**

From the equivalent circuit, the equation for $C_{off}$ is derived as shown in Equation 6

$$C_{off} = C_{DS} + C_{GS}C_{GD}/(C_{GS} + C_{GD}). \tag{6}$$

$C_{GS}$ is equal to $C_{GD}$, which can both be approximated as shown in Equation 7

$$C_{GS} = C_{GD} = \varepsilon_r \varepsilon_o L_{OL} W_C / d. \tag{7}$$

Finally, $C_{off}$ is approximated by Equation 8, where d is the distance between the gate and the source/drain contacts.

$$C_{off} = C_{DS} + \varepsilon_r \varepsilon_o L_{OL} W_C / (2d). \tag{8}$$

ZnO is a normally-off semiconductor which requires a positive gate bias to turn on. To be able to conduct charge from one the source contact to the drain contact there must be a gate overlap with the contacts. For optimal electrical characteristics, the gate overlap must be equal to or greater than the transfer length of the current flow in the ZnO into the source and drain contacts. The transfer length is the distance under the source and drain contact that the current passes through. Figure 19 shows a model depiction of transfer length on the cross-section of a TFT contact.

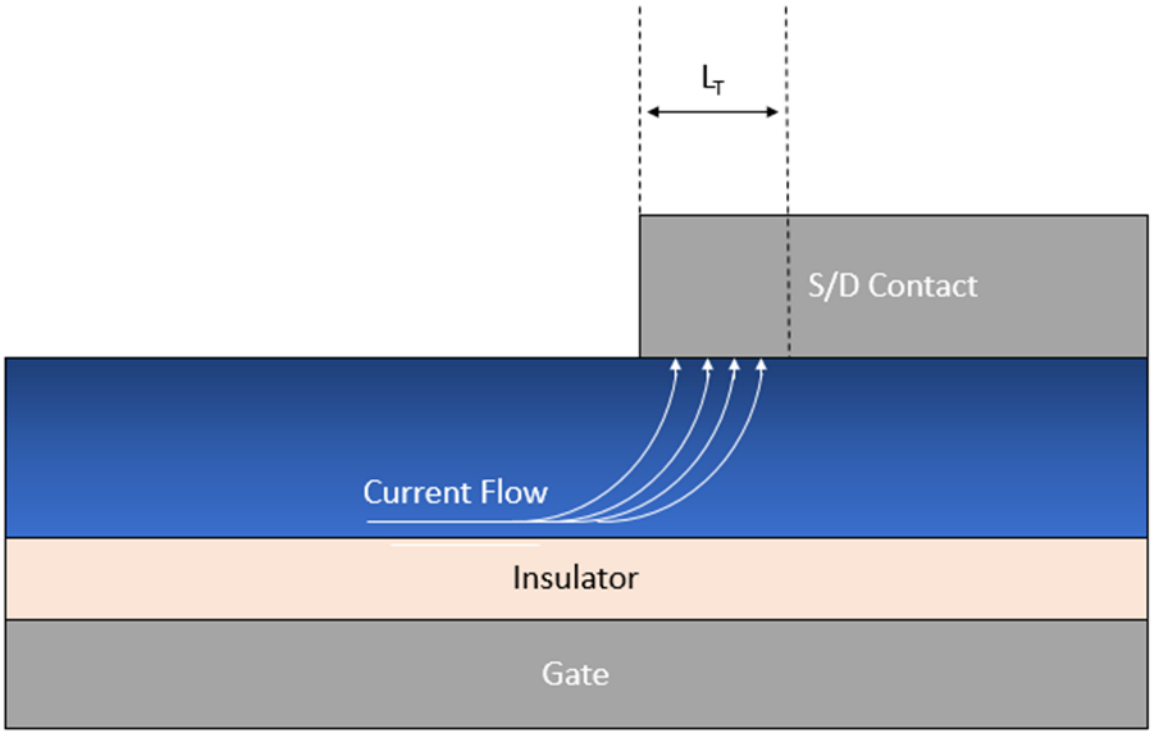



**Figure 19. Cross-sectional model of a transistor contact which depicts transfer length, $L_T$.**

If the gate overlap is less than the charge transfer length, resistance will increase due to the limited area for charges to move through. The gate overlap must be equal to or greater than the transfer length to minimize resistance in the TFT. The transfer length can be estimated as shown in Equation 9

$$L_T = (\rho_c / R_{sh})^{(1/2)}. \tag{9}$$

By increasing the conductivity of the ZnO surface, the specific contact resistivity, $\rho_c$, is reduced. As a result, $L_T$ is decreased which allows the $C_{off}$ to be decreased as well. $\rho_c$ is directly proportional to $R_c$, as shown previously in Equation 2, and both values should be decreased by the use of Ar and H plasma treatments. The resulting decrease in $C_{off}$ further increases the cutoff frequency. $C_{off}$ can be approximated by Equation 10

$$C_{off} = C_{DS} + (\rho_c/R_{sh})^{(1/2)}[\varepsilon_r \varepsilon_o W_C/(2d)]. \quad (10)$$

This research centers on decreasing the contact resistivity of a ZnO TFT. To accomplish this task, the surface of the ZnO active layer, in the contact regions, must be made as conductive as possible through post-deposition treatment. The conductive layer of ZnO shrinks the width of the tunneling barrier between W and ZnO, allowing for charge carriers to flow more easily through the barrier, which decreases the contact resistance. A model of the band diagram for a W contact on an n+ZnO ohmic layer is shown in Figure 20.

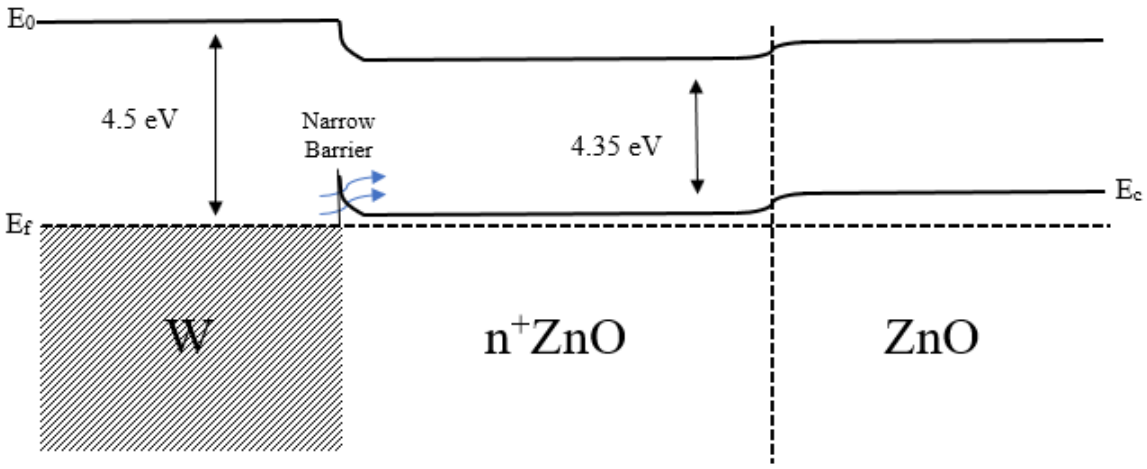



**Figure 20. The energy band diagram of a W contact on an ohmic layer of n$^+$ZnO, demonstrating the decreased barrier width.**

This research utilizes post-deposition plasma treatments to decrease the contact resistance on the ZnO surface. To develop a process in which the plasma treatments can be incorporated into the ZnO TFT fabrication, a series of experiments must take place to determine the most effective methods and settings for applying the plasma treatment. Once a process is developed to minimize contact resistivity, then an oxygen plasma treatment experiment will be conducted on the low resistivity devices to recover the channel properties. Based on the equipment available for

these experiments, the plasma treatment methods used were Ar plasma in an ICP-RIE chamber, in-situ Ar plasma in a sputtering chamber, and H plasma in an ALD chamber. The plasma treatments were incorporated into an existing ZnO TFT fabrication process at AFRL, as described in the following section.

## 3.2 Implementation of Plasma Surface Treatments

The plasma treatments in this research are used to create a conductive surface on ZnO. These plasma treatments must be implemented in a way that is compatible with the fabrication process of the ZnO TFT. This research will use a set of masks from AFRL that was designed, prior to this research, for ZnO TFT fabrication and includes TLM structures. The structure of the ZnO TFT is a reverse staggered gate TFT. To fabricate this ZnO TFT, first, gate metal contacts were deposited on a high-resistivity Si wafer. A 25-nm thick layer of Al2O3 was then deposited by ALD for gate insulation. Next, a 50-nm thick ZnO active-layer was deposited by pulsed-laser deposition (PLD). The wafer was then diced into quarters, using a diamond scribe, to allow for multiple plasma treatments on devices from the same wafer. Each quarter-wafer contains approximately twenty-five dies on them. Each die includes TLM test structures, CBKR test structures, and multiple TFT devices. After the quartering of the wafers, plasma post-deposition treatment of the ZnO thin-film samples was then performed to create a conductive surface layer on the ZnO. Witness samples were included during the plasma treatment process for the etch-depth experiment. Once the plasma treatment was accomplished, W was sputtered onto the ZnO active layer, which is used for the source and drain contact metal. A model of the plasma treatment process followed by the W depositions is shown in Figure 21.

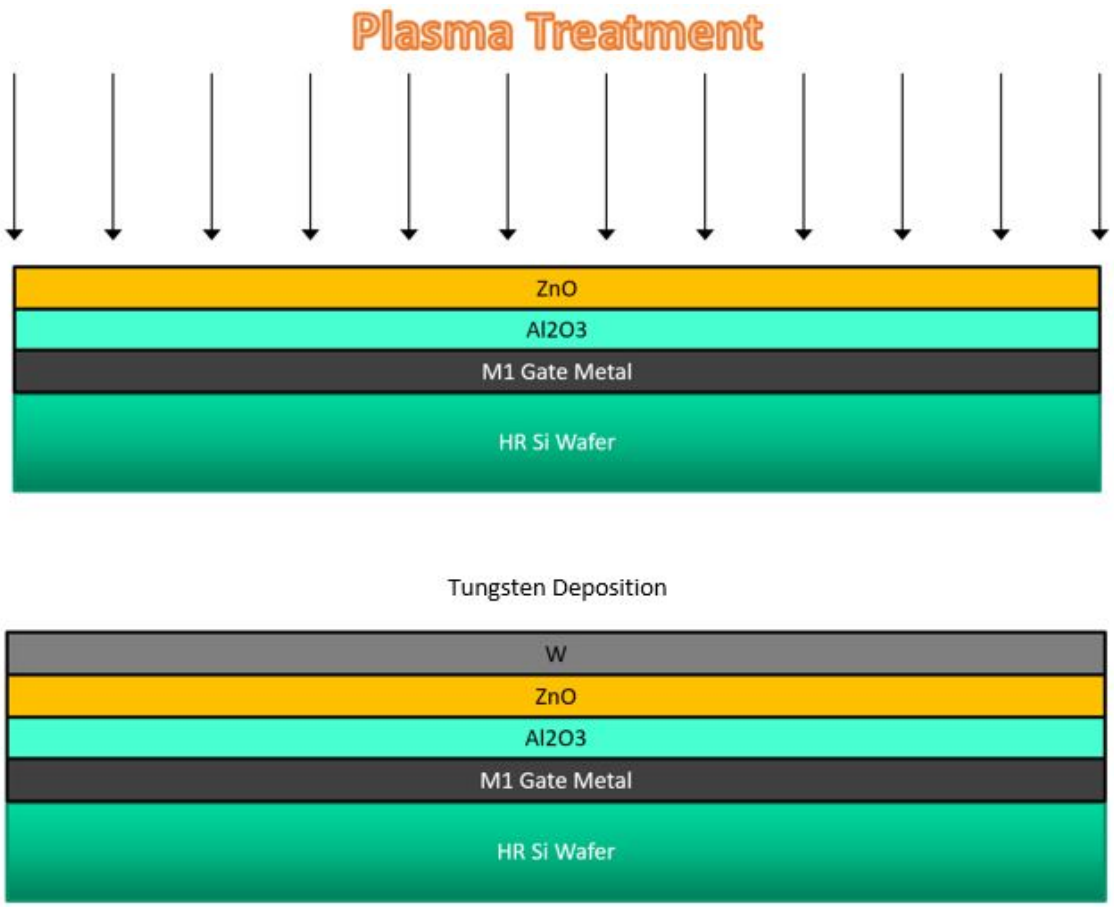



**Figure 21. The process for implementing plasma treatments followed by W deposition.**

## 3.3 Factor Selection for Experiments

To determine the relevant factors for the mentioned plasma treatment experiments, one must first understand how the machines used in this experiment function. The following sections cover the basic operation of the machines used in this research for plasma surface treatments.

### 3.3.1 Plasma-Enhanced Atomic Layer Deposition Tool.

In a plasma enhanced atomic layer deposition (PEALD) tool, remote plasma is used as an energy source to aid in the chemical reaction process to deposit an atomic layer of material on a sample. The plasma is generated by flowing a gas into

the ALD chamber at a set flow rate and applying RF power to it. High energy ions from the plasma provide the kinetic energy necessary for a chemical reaction to occur with the surface of the sample. In this research, instead of using plasma for the deposition of material, the plasma is used to incorporate hydrogen ions into ZnO to create a high concentration of donors at the ZnO surface.

### 3.3.2 ICP-RIE Tool.

An ICP-RIE tool is used to create an anisotropic etch on a sample using an ionized reactive gas. A coil is used to inductively couple RF power with the reactive gas to create the plasma. A separate RF bias is independently applied to the chuck that the sample rests on. The RF power on the chuck causes a difference in voltage to occur between the plasma and the chuck across a region known as the plasma sheath. The voltage difference accelerates positive ions from the plasma to the sample, which creates an anisotropic etch. In this experiment, a reactive gas is not used, but instead, Ar gas flows into the chamber at a set flow rate and will be inductively coupled with RF power to create Ar plasma. The Ar ions are used to bombard the surface of the ZnO with controlled energy supplied by the set ICP RF power.

### 3.3.3 RF Sputtering Tool.

An RF Sputtering tool is used to deposit a thin film of material onto a substrate. In this research, the sputter chamber will be used to deposit W onto ZnO. The mechanism in which the sputter chamber deposits material is to first evacuate gas from the chamber and then to fill the chamber with an inert gas, usually argon. Next, the inert gas is ionized with RF power between an anode and a cathode, which creates a plasma. The target material to be deposited is located on the cathode.

The positive ions in the plasma bombard the target, dislodging material, which collects on the substrate to form a thin film. The sputter chamber used for this research also contains an in-situ sputter-etch mechanism, which is typically used to etch the surface of a substrate to prepare it for deposition by removing a thin layer of the surface. The sputter-etch is accomplished in the same way as the sputter deposition except instead of the target material being located on the cathode, the substrate is now located on the cathode and is bombarded by the ions. This sputter-etch is the method used for the in-situ plasma treatments for this research.

### 3.3.4 Factor Selection Conclusion.

For the experimental design of the plasma surface treatments, the factors in the plasma treatment methods mentioned that will be examined in this experiment are power, time and flow rate. These factors will be analyzed at high and low levels through the use of a factorial design experiment.

## 3.4 Plasma Treatment Experimental Design

A total of three experiments were conducted to increase conductivity at the ZnO surface, and each examined the effects of the three factors, mentioned in the previous section, on the mean resistivity. The three different treatment methods including Ar plasma in an ICP-RIE chamber, Ar plasma generated in-situ in a W sputtering chamber, and remote hydrogen plasma in an ALD chamber. For these experiments, three factors were investigated at two settings each. This experimental design contains a total of four runs for each of the ICP Ar plasma experiment and the hydrogen plasma experiment. The in-situ Ar experiment had a total of eight runs due to the easier implementation of the plasma treatment in the W sputtering chamber. The experimental design used in these experiments is the most efficient

method to investigate the effects of the three factors and all possible combinations of the two levels for each in the limited amount of runs allowed in this research [32]. This experimental design helps determine the factors that significantly affect the mean of the contact resistivity for the samples.

### 3.4.1 Hydrogen Plasma Treatment.

The high and low factor levels for the hydrogen plasma experiment were determined based on similar research from the literature as well as recommendations from senior engineers and the technicians who run the machines. With hydrogen plasma treatments there is a concern for high etch rates that some research has demonstrated. To reduce the risk of etching away the ZnO active layer, relatively low settings for power and time are used. The settings for each of the four runs in this experiment is shown in Table 1.

**Table 1. The experiment design for the hydrogen plasma treatment.**

| Run | Power (W) | Time (s) | sccm |
|---|---|---|---|
| 1 | 40 | 20 | 5 |
| 2 | 40 | 40 | 10 |
| 3 | 30 | 20 | 10 |
| 4 | 30 | 40 | 5 |

### 3.4.2 ICP-RIE Chamber Argon Plasma Treatment.

The high and low factor levels for the ICP-RIE Ar plasma experiment were determined by talking with subject matter experts at AFRL, who have experience with the machine and with plasma treatment on ZnO. Ar etches ZnO, so to minimize the amount of etching that will occur, conservatively low power levels and times are used. Plasma is not stable at flow rates below 10 sccm. Therefore the low

level in this experiment is 30 sccm. The settings for each of the four runs in this experiment is shown in Table 2.

**Table 2. The experiment design for the ICP-RIE argon plasma treatment.**

| Run | Power (W) | Time (s) | sccm |
|---|---|---|---|
| 1 | 400 | 40 | 60 |
| 2 | 200 | 20 | 60 |
| 3 | 200 | 40 | 30 |
| 4 | 400 | 20 | 30 |

### 3.4.3 In-situ Argon Plasma Treatment.

The high and low factor levels for the sputtering chamber in-situ Ar plasma experiment were chosen by consulting with experts at AFRL who are familiar with plasma treatments in the sputtering tool. The sputtering chamber is more limited than the ICP-RIE on what settings can be used to maintain a stable plasma. The AFRL technicians tested various settings and provided a range that could be used for the Ar plasma treatment experiments. The settings for each of the eight runs in this experiment are shown in Table 3.

**Table 3. The experiment design for the In-situ argon plasma treatment.**

| Run | Power (W) | Time (min) | sccm |
|---|---|---|---|
| 1 | 30 | 3 | 34 |
| 2 | 10 | 3 | 49 |
| 3 | 30 | 6 | 49 |
| 4 | 30 | 6 | 34 |
| 5 | 10 | 6 | 34 |
| 6 | 10 | 6 | 49 |
| 7 | 30 | 3 | 49 |
| 8 | 10 | 3 | 34 |

### 3.5 Plasma Etching Experiment

Some etching of the ZnO layer was expected to occur as a side effect of the plasma treatments. Witness samples of PLD ZnO wafers were used to monitor the amount of etching that occurred at the ZnO surface. These samples were run simultaneously with the plasma treated samples in the experiments listed previously. The witness samples help determine the maximum power and time settings that can be used for the treatments without etching away the active layer of the devices. The witness samples consisted of a Si wafer with 50 nm of PLD ZnO deposited on it and a thick layer of patterned s1818 (used to mask the ZnO from the plasma treatment). The wafer was diced into pieces, so it could be used with multiple treatment settings. After the plasma treatments, the photoresist was removed, and the step height was determined by Atomic Force Microscopy (AFM). A model of the witness sample is shown in Figure 22. A model of the step height measurement method is shown in Figure 23.

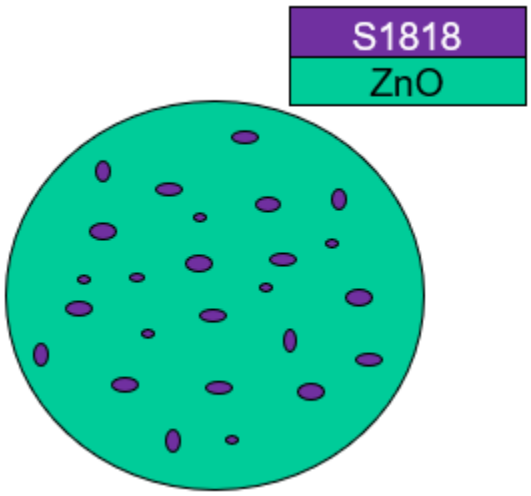



**Figure 22. A model of the witness sample.**

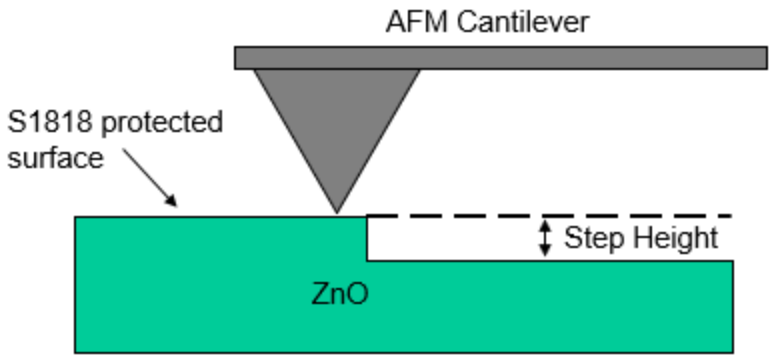



**Figure 23. A model of the AFM step height measurement method.**

### 3.6 Contact Resistance Measurements

TLM structures were used to determine the contact resistance of the plasma-treated devices. The TLM design used in this research was created by AFRL, and consists of metal contacts to ZnO spaced at 2, 4, 6, 8, 10, and 12 μm intervals. To better visualize the fabrication of the device, a cross-sectional model of the TLM structure at one of the spacings is shown in the following sections at critical steps in the fabrication process. The location of the cross-section on the TLM model is shown in Figure 24.

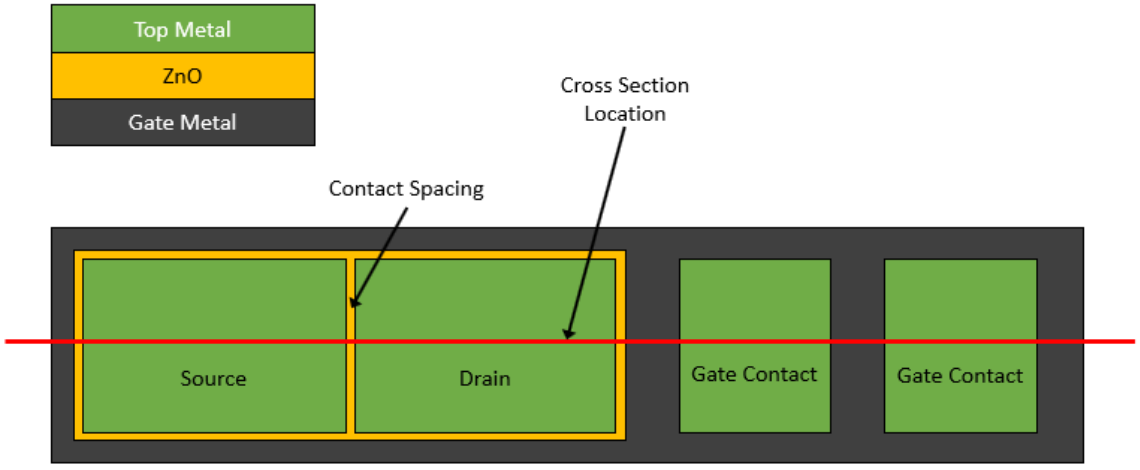



**Figure 24. Top-view model of one spacing in the TLM structures. The red line is the location of TLM cross-section shown in subsequent figures.**

The TLM structures were fabricated on a high-resistivity Si substrate. These devices are a bottom gate design. The first step of the fabrication is to deposit gate metal contacts using a liftoff method. This stack of metal is a standard gate metal design used at AFRL for ZnO TFTs because of its quality adhesion and electrical properties. Next, a 25-nm thick layer of $Al_2O_3$ was deposited by ALD for gate insulation. Following the insulating layer, a thin film of 50-nm thick ZnO was deposited by PLD, which is the active layer of the TLM. Specifics of the PLD process can be found in ref [9]. Plasma post-deposition treatments of the ZnO thin film samples were performed by three different methods. The first method used an ICP-RIE chamber to apply an Argon plasma treatment. The second method uses an ALD to create hydrogen plasma remotely to treat the ZnO surface. The third method utilized the sputter chamber, but prior to sputtering W, the in-situ process used argon plasma to treat the ZnO surface. In all three experiments, the samples were exposed to air after the plasma treatment and before putting down sputtered W contacts. A model of the plasma treatment is shown in Figure 25.

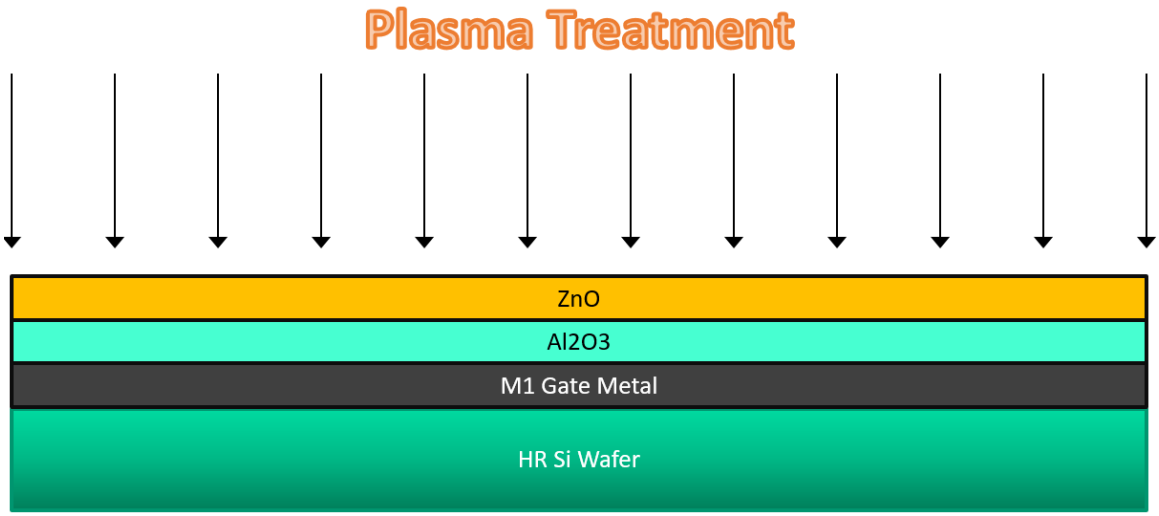



**Figure 25. Cross-sectional model of the plasma treatment of the ZnO surface.**

Immediately following the plasma treatment, 100 nm of tungsten was sputtered

onto the ZnO. The tungsten was then patterned with photoresist and etched in an RIE. Next, the exposed ZnO and Al2O3 was etched away together in an ICP-RIE. The photoresist was then removed. The cross-section of the TLM structure at this point in the fabrication is shown in Figure 26.

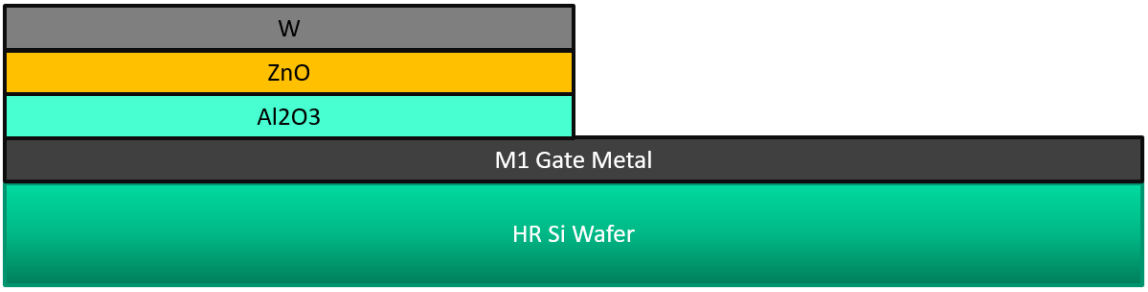



**Figure 26. Cross-sectional model of the TLM cross-section after W etch and ZnO/Al2O3 etch.**

Metal contacts for probing were created using a liftoff process. This stack of metal protects the device from physical damage during probing, and also has desirable adhesion and electrical properties for contact W on the ZnO TFT. The top layer of the metal stack is composed of nickel, and was used as an etch mask to pattern the W contacts. The W contacts were patterned using RIE, exposing the ZnO channel, as shown in the model of the cross-section in Figure 27.

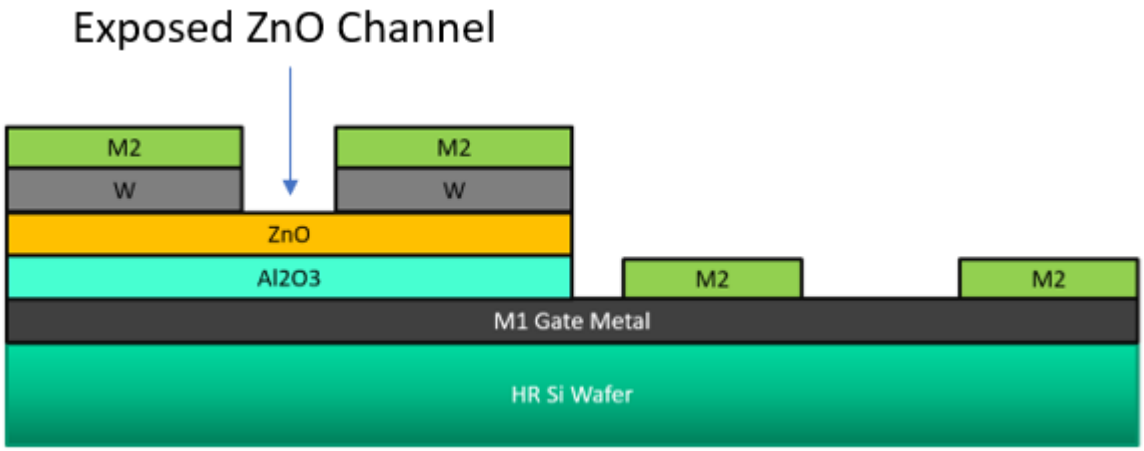



**Figure 27. Cross-sectional model depicts the exposed ZnO channel region after clearing the tungsten on the TLM structure.**

## 3.7 Channel Recovery Experiment

For the channel recovery experiment, the goal is to recover the channel properties while maintaining the low contact resistance created by the previous plasma treatments. This experiment was planned to be accomplished by first fabricating devices based on the optimum factor levels determined in the prior plasma treatments. The entire surface of the ZnO active layer would be exposed during the plasma treatments, and therefore the resulting device containing this ZnO will have a highly conductive channel. After fabrication of the plasma-treated ZnO TFTs, the channel region would still be exposed, whereas the source and drain contact regions are covered by metal contacts. Post treatments could then be implemented at this point in the fabrication to make the channel region more resistive, converting it back to the as-deposited state. The result that would be measured in this experiment is the sheet resistance of the "recovered" ZnO. Sheet resistance would be determined using TLM test structures as mentioned before in the TLM section of this chapter.

### 3.7.1 Oxygen Plasma Channel Recovery Experiment.

A factorial experiment was planned to determine what factor levels should be used in the plasma treatment to achieve a sheet resistance like the untreated ZnO TFT devices. The oxygen plasma treatment would have taken place after the deposition of the contact metal with the channel exposed, as shown in Figure 28.

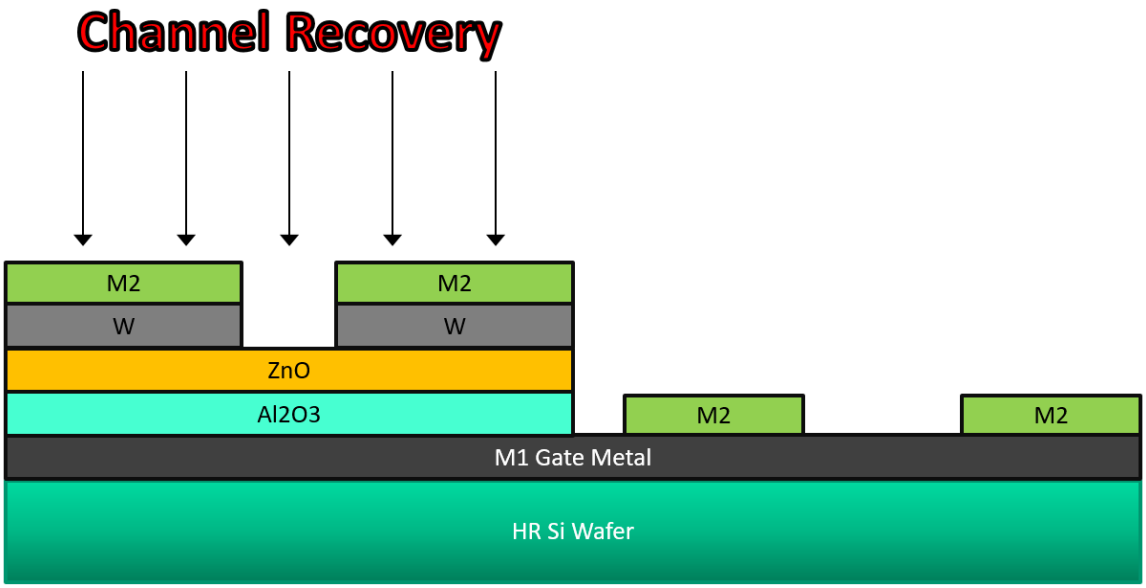



**Figure 28. Cross-sectional model of the oxygen plasma treatment method for channel recovery.**

The high and low factor levels for the ICP-RIE $O_2$ plasma experiment were determined by reviewing similar $O_2$ plasma treatments on ZnO in the literature [20, 26, 3]and by talking with the technician who runs the ICP-RIE to determine typical settings for the specific machine. The settings for each of the four runs in this experiment are shown in Table 4.

**Table 4. Experiment design for the oxygen plasma treatment.**

| Run | Power (W) | Time (s) | sccm |
|---|---|---|---|
| 1 | 400 | 40 | 60 |
| 2 | 200 | 20 | 60 |
| 3 | 200 | 40 | 30 |
| 4 | 400 | 20 | 30 |

### 3.7.2 Oxygen Anneal Channel Recovery Experiment.

In this experiment, a PLD chamber would be used to accomplish $O_2$ annealing treatments. This was planned to be a half-factorial design experiment. The factors that would be varied in the experiment are $O_2$ pressure, temperature and time. The

settings for these factors are based on settings from similar experiments in the literature [29, 4], as well as the limitations of the PLD chamber. The settings for each of the four runs in this experiment are shown in Table 5.

**Table 5. Experiment design for the oxygen annealing .**

| Run Order | Temperature (°C) | Time (min) | Pressure (atm) |
|---|---|---|---|
| 1 | 200 | 60 | 0.1 |
| 2 | 400 | 10 | 0.1 |
| 3 | 400 | 60 | 0.9 |
| 4 | 200 | 10 | 0.9 |

# IV. Results and Analysis

## 4.1 Chapter Overview

In this chapter, the device fabrication is explained in detail and the results from the experiments, designed in the previous chapter, are presented and analyzed. These results include TLM Plots, contact resistance measurements and etch depth measurements from each plasma-treated device. The results of each experiment will be compared, and a plasma treatment technique will be identified as the best method for decreasing contact resistance of the ZnO TFT.

## 4.2 Surface Etching Experiment

During the plasma surface treatments of ZnO, ions from the plasma bombard the surface of the ZnO possibly dislodging a significant amount of material, also known as etching. Since this experiment is dealing with thin-films of only 50 nm, the etching amount needs to be very minimal. Otherwise, there will be severe performance issues for the fabricated device, or the entire active layer could be etched away. To measure the amount of etching that each plasma treatment results in, witness samples of ZnO (masked with photoresist) were run alongside the plasma-treated device samples. The photoresist was then stripped from the witness samples, and the resulting step height from the resist covered regions to the exposed regions was measured using an AFM. The step height indicates the etch depth in ZnO due to each plasma setting. The AFM results for each plasma treatment are shown in Tables 6-8, along with the factor plots in Figures 29-31 showing the mean etch depth for each factor level. The factor plots used in this research are meant to visually demonstrate the significance of a factor on affecting the contact etch depth but do not necessarily show the actual trend for contact resistance in response to a

given factor.

**Table 6. Etch depth of the ICP-RIE Ar plasma treated ZnO Surface**

| Run | Power (W) | Time (s) | sccm | etch depth (nm) |
|---|---|---|---|---|
| 1 | 400 | 40 | 60 | 2.0 |
| 2 | 200 | 20 | 60 | 1.0 |
| 3 | 200 | 40 | 30 | 1.4 |
| 4 | 400 | 20 | 30 | 0.9 |

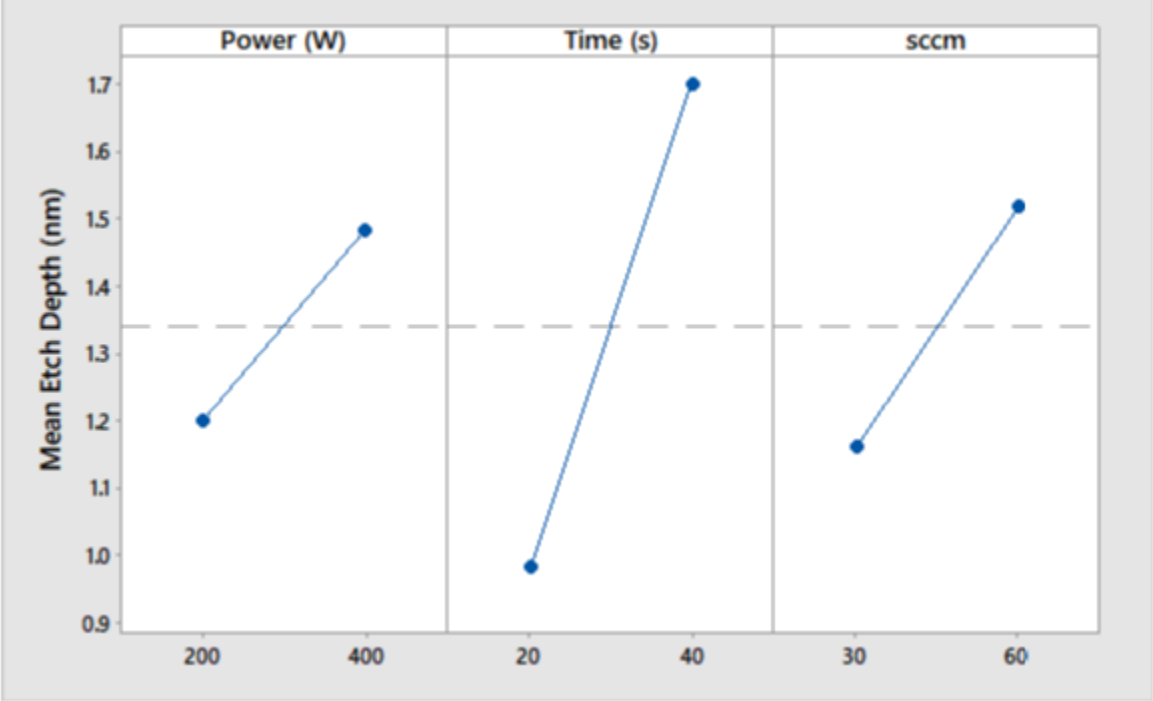



**Figure 29. Mean etch depth for each factor setting in the ICP Ar plasma treatment.**

**Table 7. Etch depth of the In-situ Ar Plasma Treated ZnO Surface**

| Run | Power (W) | Time (s) | sccm | etch depth (nm) |
|---|---|---|---|---|
| 1 | 30 | 3 | 34 | 4.4 |
| 2 | 10 | 3 | 49 | 1.7 |
| 3 | 30 | 6 | 49 | 10.4 |
| 4 | 30 | 6 | 34 | 9.1 |
| 5 | 10 | 6 | 34 | 2.7 |
| 6 | 10 | 6 | 49 | 2.3 |
| 7 | 30 | 3 | 49 | 4.8 |
| 8 | 10 | 3 | 34 | 1.9 |

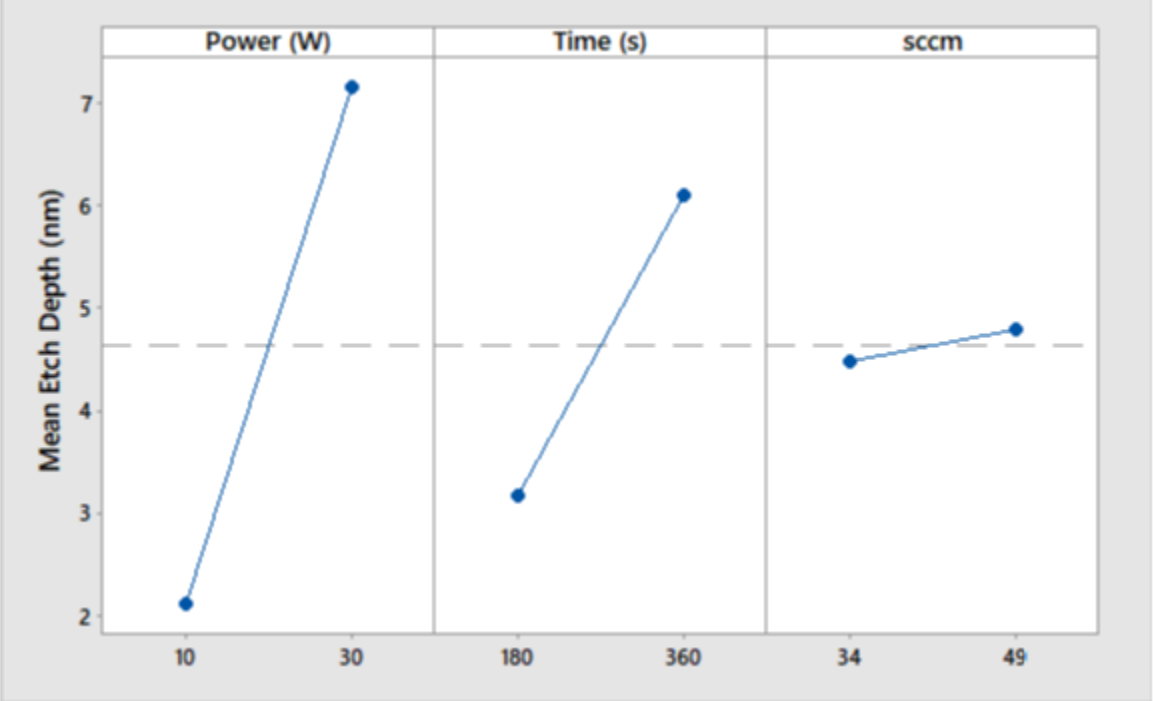



**Figure 30. Mean etch depth for each factor setting in the In-situ Ar plasma treatment.**

**Table 8. Etch depth of the H Plasma Treated ZnO Surface**

| Run | Power (W) | Time (s) | sccm | etch depth (nm) |
|---|---|---|---|---|
| 1 | 40 | 20 | 5 | 0.3 |
| 2 | 40 | 40 | 10 | 2.3 |
| 3 | 30 | 20 | 10 | 0.1 |
| 4 | 30 | 40 | 5 | * |

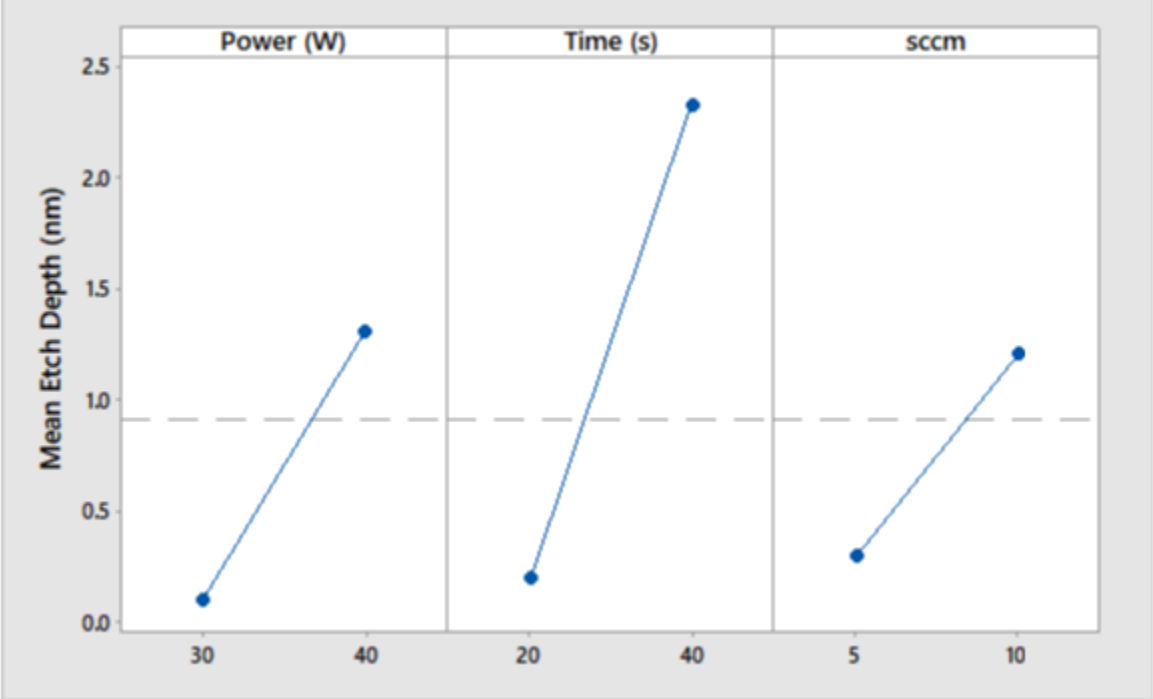



**Figure 31. Mean etch depth for each factor setting in the H plasma treatment.**

### 4.2.1 Surface Etching Experiment Summary.

The purpose of the plasma etching experiment was to test if the plasma surface treatments could be implemented without causing an unacceptable amount of etching the ZnO surface. The results from this experiment show minor amounts of etching in almost every case except for the in-situ treatments for the plasma treatment times that were six minutes long. In this case, etching of over 10 nm was observed, or more than 20% of the ZnO films thickness. In follow-on experiments, this result will have to be taken into account if longer treatment times or higher power levels are used. A possible solution to mitigate the amount of etching is to deposit a thicker film of ZnO, thick enough to negate the amount of etching. It is unclear why the remote hydrogen plasma caused etching to occur on the ZnO surface since there was no bias to supply kinetic energy to the ions. One possible explanation for the etching due to the hydrogen plasma is that the hydrogen

radicals from the remote plasma reacted with the oxygen at the ZnO surface causing the removal of oxygen and zinc.

### 4.3 Contact Resistance Results

The goal of the plasma treatment experiments is to use the plasma treatments to create a highly conductive layer on the surface. The ZnO should ideally go from a semiconductor to a conductor in this experiment. To test the resultant decrease in contact resistance from the plasma treatments, TLM structures were used to determine the contact resistance between the W contacts and the ZnO active layer.

Each sample in these experiments contains twenty-five identical die in terms of layout design. TLM structure is located on each die and was individually tested. The TLM structure contain six spacing ranging from 2-12 μm by increments of 2 μm. During the test of each TLM spacing, the drain-to-source voltage, $V_{ds}$, was set to 0.2 V, because previous testing of the samples showed that 0.2 V was in the linear region of the devices. The drain current, $I_d$, was recorded for each gate voltage, which was varied from 0-10 V by increments of 2 V. The resistance from the voltage source and probe contacts were assumed to be negligible. $R_{on}$, in terms of ohm-mm, was calculated for each gate voltage using Equation 11, where w is the width of the TLM structure (141μm).

$$R_{on} = w * V_{ds}/I_d \tag{11}$$

A TLM Plot was made for multiple dies on each of the samples in these experiments. The $R_c$was extracted from each of the plots by finding the intersection of the 8 and 10 $V_{gs}$ lines on the TLM plots. One detail to note is due to liftoff-resist exposure error in the fabrication process, some of the spacings were up to a micron smaller than the intended design. All spacings on an individual die were decreased

equally, which means the slope of the TLM plot is not affected. This defect was mitigated by using the cross-point since the $R_{on}$ at this cross-point would not change with slightly smaller spacings. This defect is apparent by the negative y-intercept seen in the TLM plots. The y-intercept should be positive and depict $2R_c$ for the given gate voltage, but the lines are shifted to the right due to the exposure error. This shift is demonstrated in the TLM plot in Figure 32. The $R_c$ for each TLM plot was calculated and recorded in Tables 9-12.

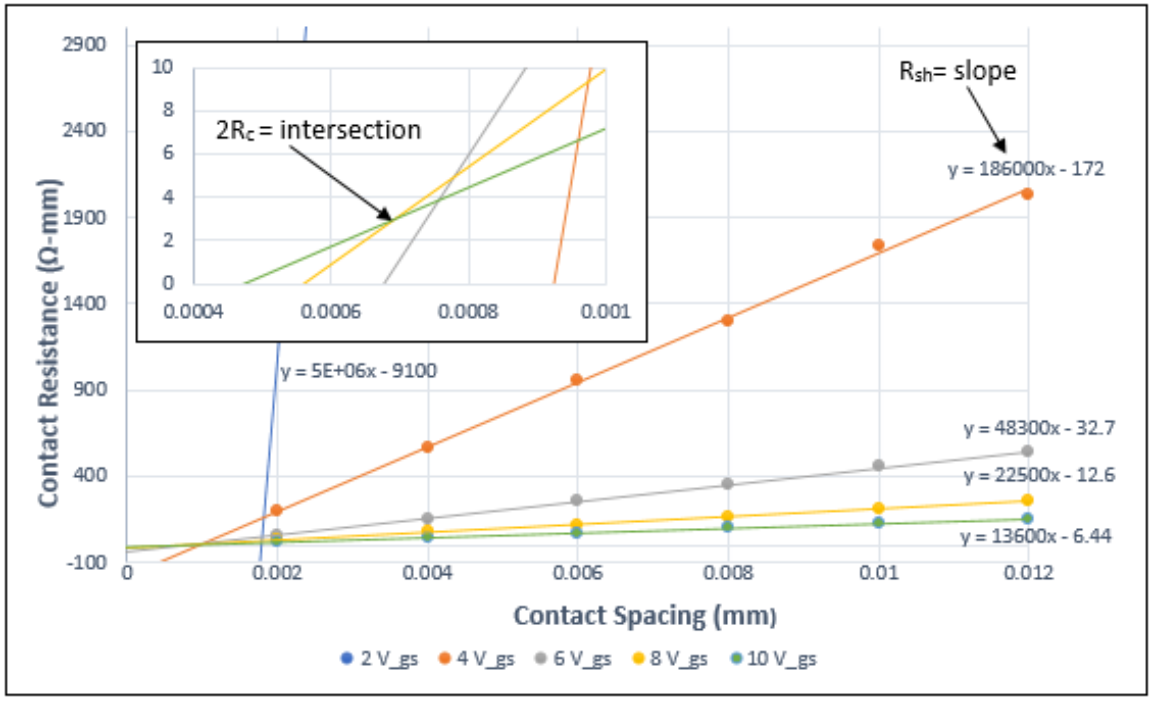



**Figure 32. TLM plot for the In-Situ-8 samples. Inset: A zoomed in TLM plot depicting the $2R_c$ intersection point.**

**Table 9. Contact resistance for the as-deposited ZnO**

| Reference # | Rc (ohm-mm) |
|---|---|
| 1 | 2.0 |
| 2 | 1.8 |
| avgerage | 1.9 |

**Table 10. Contact resistance for the ICP-RIE Ar plasma treated ZnO**

| Run | Power | Time | sccm | Rc (ohm-mm) |
|---|---|---|---|---|
| 1 | 400 | 40 | 60 | 1.9 |
| 2 | 200 | 20 | 60 | 1.7 |
| 3 | 200 | 40 | 30 | * |
| 4 | 400 | 20 | 30 | 1.2 |

**Table 11. Contact resistance for the in-situ Ar plasma treated ZnO**

| Run | Power | Time | sccm | Rc (ohm-mm) |
|---|---|---|---|---|
| 1 | 30 | 3 | 34 | 1.1 |
| 2 | 10 | 3 | 49 | 1.3 |
| 3 | 30 | 6 | 49 | * |
| 4 | 30 | 6 | 34 | 1.0 |
| 5 | 10 | 6 | 34 | 1.1 |
| 6 | 10 | 6 | 49 | 1.4 |
| 7 | 30 | 3 | 49 | 1.1 |
| 8 | 10 | 3 | 34 | 1.5 |

**Table 12. Contact resistance for the H plasma treated ZnO**

| Run | Power | Time | sccm | Rc (ohm-mm) |
|---|---|---|---|---|
| 1 | 40 | 20 | 5 | 1.8 |
| 2 | 40 | 40 | 10 | 1.8 |
| 3 | 30 | 20 | 10 | 1.2 |
| 4 | 30 | 40 | 5 | * |

The mean $R_c$ for each factor in each experiment was plotted to aid in determining the impact of each factor. From these plots, one can see relatively how much effect each factor had on the $R_c$. The mean factor plots are shown in Figures 33-35.

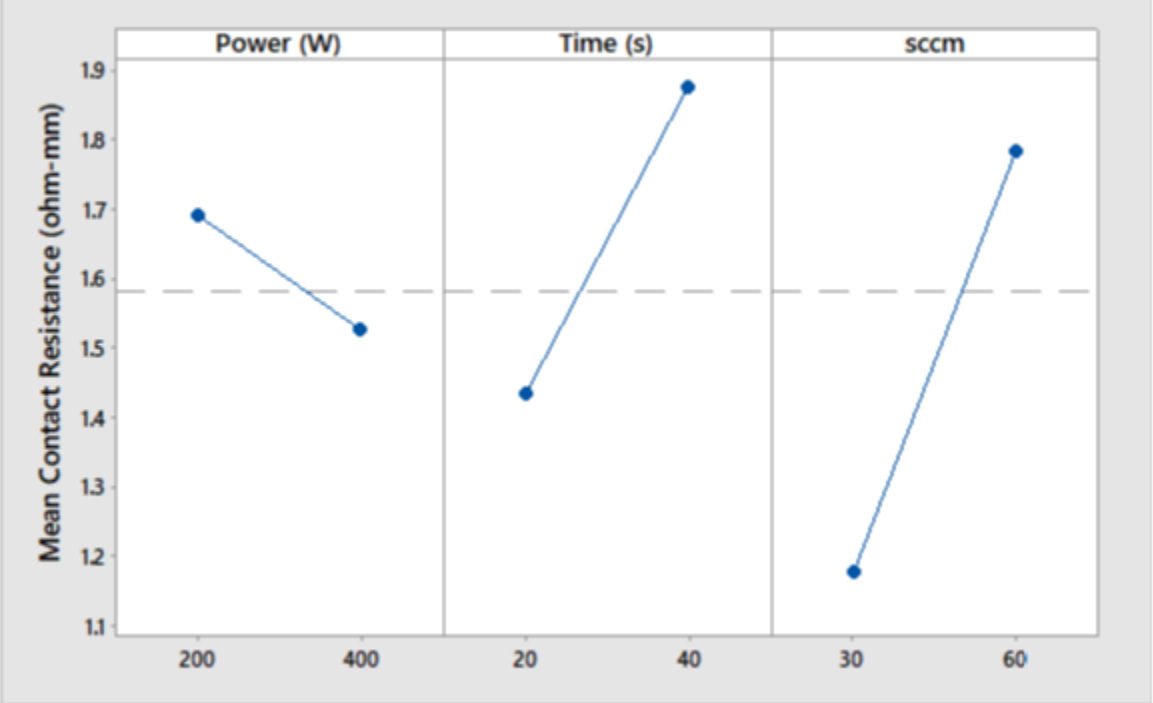



**Figure 33. Mean contact resistance for each factor setting in the ICP-RIE Ar plasma treatment experiment.**

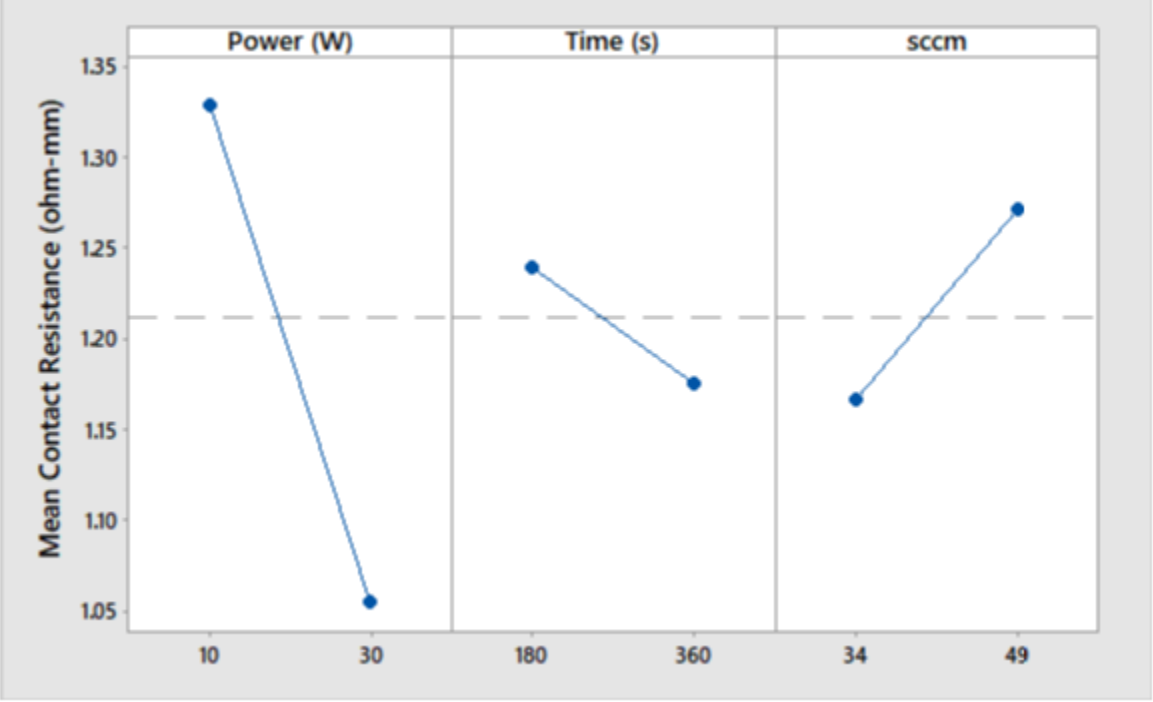



**Figure 34. Mean contact resistance for each factor setting in the In-situ Ar plasma treatment experiment.**

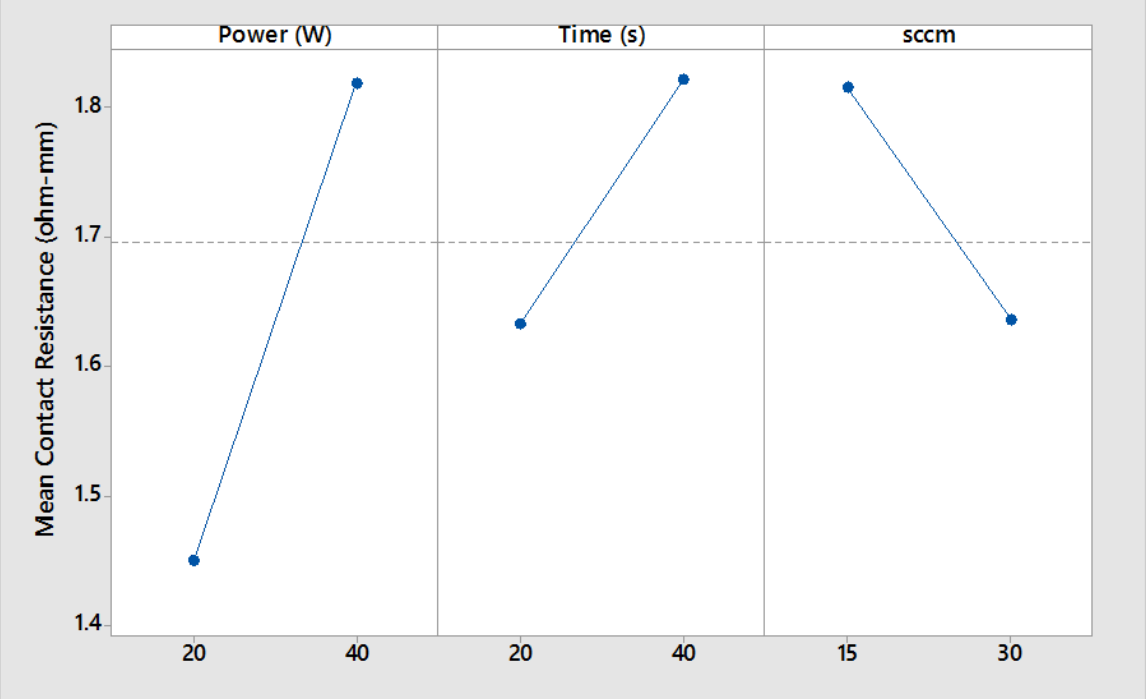



**Figure 35. Mean contact resistance for each factor setting in the H plasma treatment experiment.**

### 4.3.1 Contact Resistance Summary.

The experimental data was able to demonstrate that each of the plasma treatments decreased contact resistance when compared to the reference sample contact resistance, measured at 1.9 ohm-mm. The lowest contact resistance achieved by the ICP-RIE Ar plasma treatment, in-situ Ar plasma treatment, and the H plasma treatment were 1.2, 1.0, and 1.5 ohm-mm respectively. The in-situ treatment showed the best results and was the easiest to implement because it was accomplished with the sputter chamber before putting down W contacts. With only three runs in the ALD and ICP-RIE experiments, more runs will have to be accomplished to definitively determine which of the three methods has the most significant effect on decreasing contact resistance. For the in-situ treatment, an optimum treatment setting would include a larger power level and longer treatment

times since the factor plot shows a trend of decreased contact resistance as those two factors increase.

### 4.4 Contact Resistance vs. Etch Depth

A small amount of etching on the witness samples was observed from the plasma treatment experiment. The measured etch depth may also be a significant factor in the contact resistance of the ZnO TFT. To test if the etch depth correlates with contact resistance, a plot of contact resistance in response to etch depth was created for each of the three plasma treatment experiments, as shown in Figures 36-38.

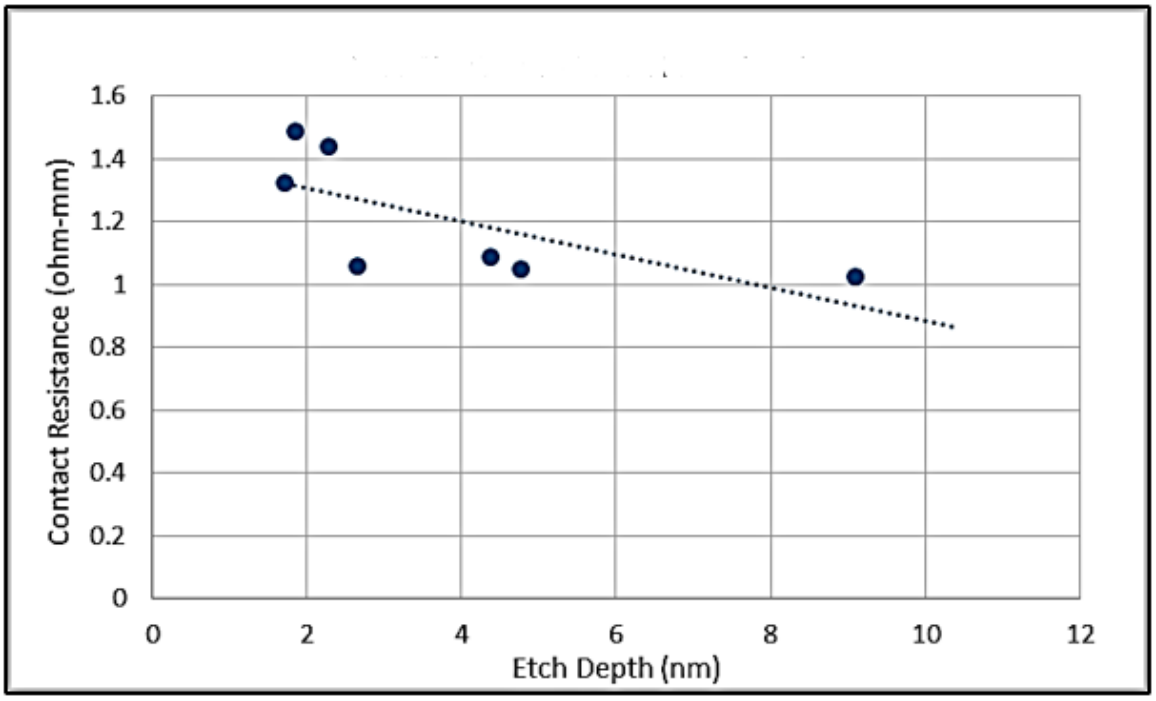



**Figure 36. Contact resistance in response to etch depth for the in-situ Ar plasma treatment.**

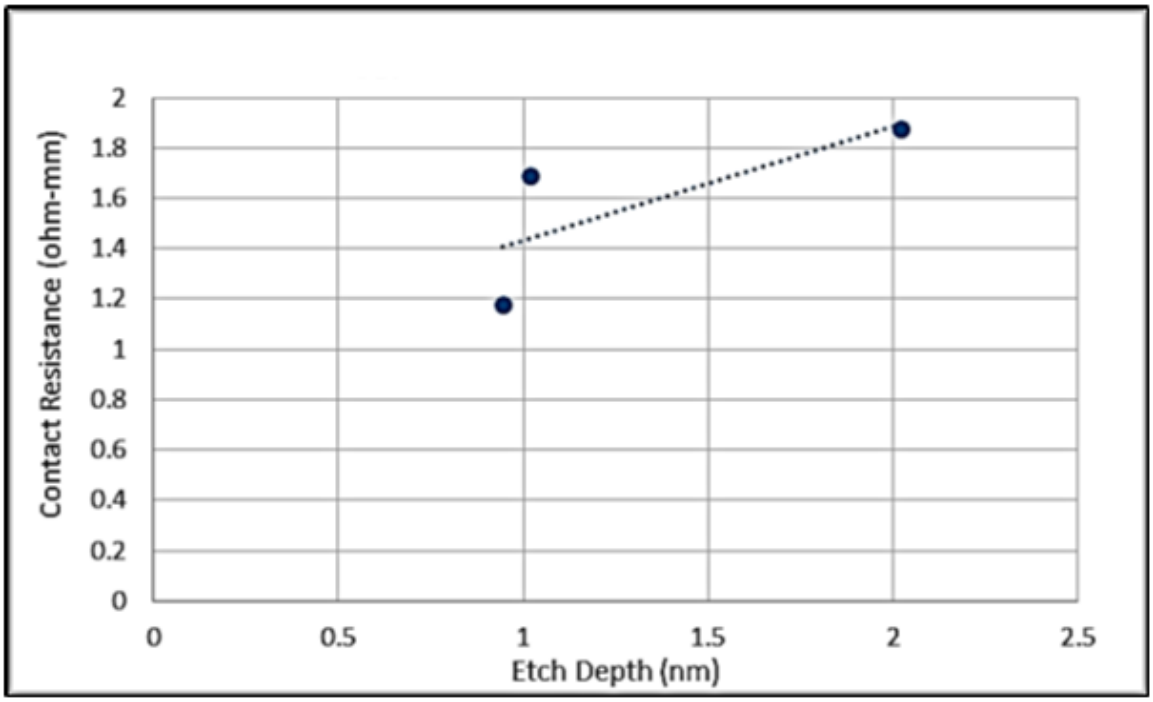



**Figure 37. Contact resistance in response to etch depth for the ICP-RIE Ar plasma treatment.**

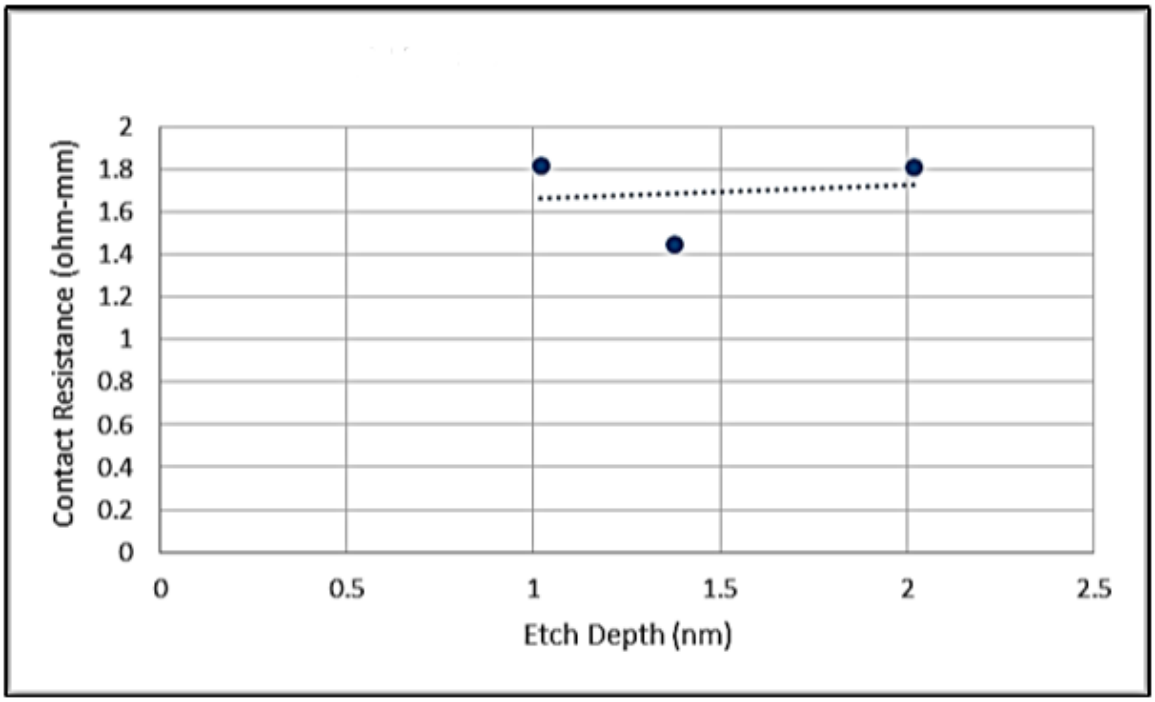


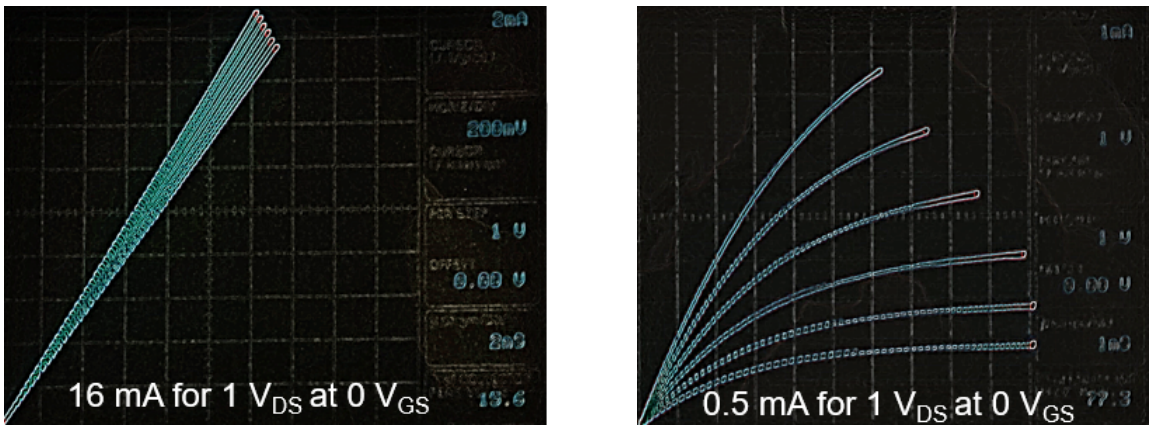

**Figure 38. Contact resistance in response to etch depth for the hydrogen plasma treatment.**

### 4.4.1 Contact Resistance vs. Etch Depth Analysis.

The result of the contact resistance as a result of the etch depth plot, for the in-situ experiment, shows a clear trend of a decrease in contact resistance as etch depth increases. This indicates that if the ZnO surface is etched even further, a lower contact resistance could be accomplished. This finding is possibly due to the incorporation of $Zn_i$ dopants in the ZnO crystal structure. The Zn is dislodged from the surface of the ZnO by the Ar plasma and some of the dislodged Zn can penetrate into the ZnO lattice structure to form the $Zn_i$. The larger etch depths create increased amounts of dislodged Zn, which possibly leads to increased numbers of $Zn_i$ in the ZnO crystal lattice. This trend is not apparent in the hydrogen plasma experiment, or the ICP argon plasma experiment.

## 4.5 Channel Recovery

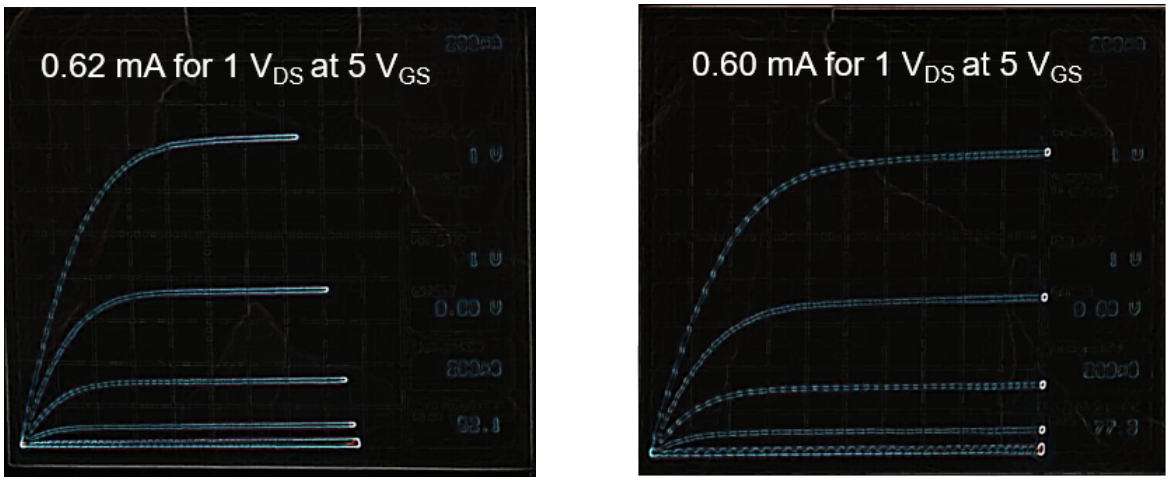
The channel recovery experiment was supposed to utilize oxygen plasma treatments or oxygen annealing to undo the increased conductivity in the channel region of the ZnO TFTs. These experiments were determined to be unnecessary because the Ar plasma treated ZnO TFTs lost their increased conductivity after a 250 $^\circ$ C hot plate bake. To demonstrate the observed channel recovery, Figure 39 shows the IV characteristics of the highly conductive Ar plasma treated sample from run one of the in-situ experiment and the IV curve for an as-deposited ZnO TFT sample. These curves were measured after the clearing of the tungsten metal from the TFT channel region and before the hot plate bake.




(a) (b)

**Figure 39. (a) IV curve from an Ar plasma treated sample, from run one of the in-situ experiment, before the 250 ° C bake. The forced voltage is 0.2 V per division and the measured current is 2 mA per division. The applied gate voltages are 0-5 V at 1 V increments. (b) IV curve from the reference sample before the 250 ° C bake. The forced voltage is 1 V per division and the measured current is 1 mA per division. The applied gate voltages are 0-5 V at 1 V increments.**

At this stage in the fabrication the ZnO surface in the channel region of the TFT is exposed to air. The samples were then baked at 250 ° C for ten minutes on a hot plate. Following this bake, the samples were then probed again on a curve tracer to show the IV characteristics. The IV curve for the in-situ Ar treated device and the IV curve for the as-deposited reference sample is shown in Figure 40.




(a) (b)

**Figure 40. For both of the IV curves displayed, the forced voltage is applied at 1 V per division and the measured current is 0.2 mA per division. The applied gate voltages are 0-5 V at 1 V increments. (a) IV curve from an Ar plasma treated sample, from run one of the in-situ experiment, after the 250 ° C bake. (b) IV curve is from the reference sample after the 250 ° C bake.**

### 4.5.1 Channel Recovery Analysis.

Before the 250 ° C bake the in-situ plasma treated sample was much more conductive than the as-deposited sample, conducting 16 mA at 1 $V_{ds}$ and 0 $V_{gs}$, while the as-deposited sample only conducted 0.5 mA at the same settings. After the 250 ° C bake on a hot plate, the IV curves of the two samples became almost identical, which indicates that the observed increased conductivity in the Ar plasma treated sample was undone by the 250 ° C bake. Similar results were observed for all of the Ar plasma treated samples, although images of the IV curves were not obtained. Although the channel Ar plasma treated ZnO TFT devices were recovered to their as-deposited conductivity, the devices still showed a decreased contact resistance. These results suggest that the Ar plasma treatments introduce n-type dopants into the ZnO which easily diffuse out of the crystal lattice, which suggests $Zn_i$ as the likely dopant due to its known low migration barriers. The devices still demonstrated decreased contact resistances after the 250 ° C bake,

which is evidence of charge encapsulation by the W source and drain contacts. The encapsulated charge created a conductive surface layer between the ZnO and the W contacts which resulted in the decreased contact resistance.

# V. Conclusion

## 5.1 Conclusions of Research

The goal of this thesis ultimately was achieved. This goal included determining settings for plasma treatments to decrease contact resistivity on ZnO and to integrate this treatment into the fabrication process for a ZnO TFT. This goal meant that not only did the plasma treatments need to reduce contact resistivity on the ZnO, but the effects of the treatments needed to be undone in the channel region of the device from the recovery experiments. Interestingly enough, the Ar plasma treated device channels were easily recovered with a $250^{o}$ C dehydration bake. The increased conductivity in ZnO due to the Ar plasma treatment is theorized to be caused by the formation of $Zn_i$, which act as a shallow donor in ZnO. The plasma-treated devices maintained a lower contact resistance in the contact regions, even after the $250^{o}$ C bake. The lowest contact resistances achieved by the ICP-RIE Ar plasma, in-situ Ar plasma, and H plasma were 1.2, 1.0, and 1.5 ohm-mm respectively. It was also demonstrated that the plasma treatments caused minimal surface etching (10.4 nm was the largest etch depth), proving compatibility for use in thin-film applications. Based on these results, it is recommended that the in-situ treatment be used as the method to include in the ZnO TFT fabrication process to decrease contact resistance. This plasma treatment for ohmic contacts is capable of increasing the RF switch cutoff frequency to the highest frequency reported in research for ZnO TFTs.

## 5.2 Recommendations for Future Research

This research was not able to use the CBKR structures due to a layout error. The error created a short between the gate pad and pad four. A new layout and

stepper mask must be created to fix this error. It would be useful to have CBKR structures to verify the results seen in the TLM analysis. An advantage to having CBKR structures over TLM structures is that it does not require plots to extrapolate the contact resistivity. The resistivity is calculated directly from the measured voltage.

Due to time limitations, follow up experiments using different combinations of factor levels were not accomplished. More test runs must be accomplished to determine an optimum setting for reducing contact resistance. This would include completing all combinations of the different factor levels for the ICP-RIE Ar plasma treatment, and the H plasma treatment experiments. More runs can also be used to test for curvature in the results, by testing midpoints for the factor settings.

The ALD used for the hydrogen treatments malfunctioned at the beginning of experimentation due to a microcontroller issue. The ALD was not able to be fixed in time to accomplish all of the experiments I initially sought out. Future experiments should accomplish the experimental design of the H plasma treatment. In addition to the H plasma treatment, researchers should look into accomplishing a combination of Ar plasma and H plasma treatments, and analyze the effect on contact resistivity. This Ar and H plasma combination was another experiment initially planned for, but not accomplished due to the ALD microcontroller issue.

The Ar treated samples did not need a channel recovery experiment due to the low-temperature recovery from the dehydration bake, but the H plasma treated samples do need to be recovered. Due to the issues mentioned previously with the ALD, a recovery experiment did not take place in this research. The experiment would have required the use of the ALD to treat the surface of ZnO with H plasma and the run the oxygen recovery treatments at the last step of the process follower.

### 5.2.1 Ga-doped ZnO Ohmic Layer.

An ohmic contact method that deserves serious consideration, but this research did not have enough time to investigate, is using a Ga-doped ZnO (ZnO:Ga) ohmic layer instead of applying plasma treatments. Previous research has shown that ZnO:Ga grown by PLD in pure Ar demonstrates high conductivity [33]. Essentially, this was the goal of the plasma treatment in this thesis, but instead of treating the contact regions with plasma, ZnO:Ga is deposited. To fabricate this ZnO:Ga ohmic contact, the same TFT fabrication process should be used as in this thesis, but instead of the plasma treatments, ZnO:Ga should be deposited immediately after deposition of the ZnO active layer as shown in Figure 41.

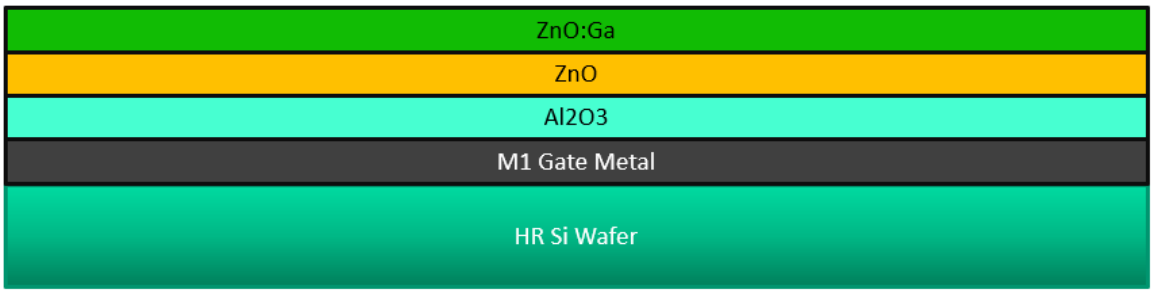



**Figure 41. Cross-sectional representation of the Ga-doped ohmic layer deposited directly after the ZnO layer.**

After the ZnO:Ga is deposited, the fabrication process is identical to the process in this thesis until after the W is cleared in the channel region of the TFT, shown in Figure 42.

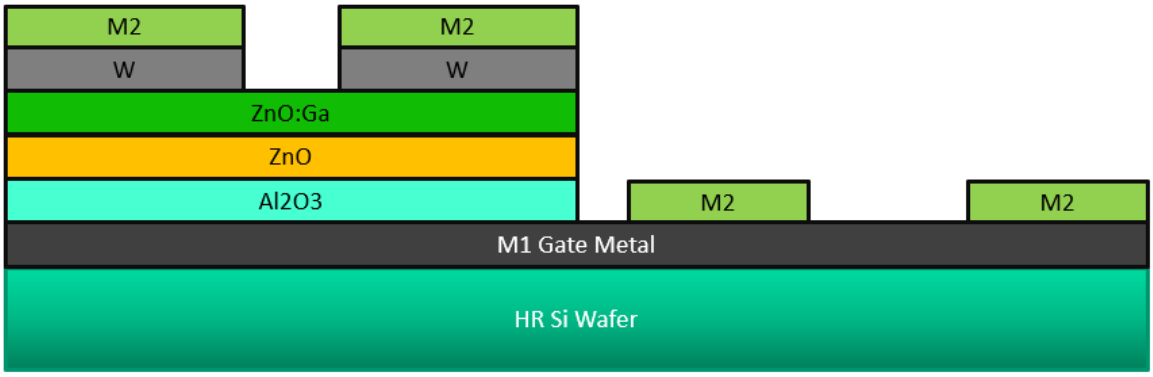



**Figure 42. Cross-sectional representation of the Ga-doped ohmic layer ZnO TFT just after the W is cleared from the channel region.**

Finally, with the ZnO:Ga expose in the channel region, a ZnO:Ga etch should be accomplished. The ZnO:Ga must be cleared to prevent shorting between the source and drain contacts. Therefore an over-etch must be accomplished. The over-etch will etch partially into the ZnO active layer, so in order to avoid hurting the performance TFT, a thicker ZnO active layer should be deposited. The ZnO TFT with the ZnO:Ga cleared out of the channel region is shown in Figure 43.

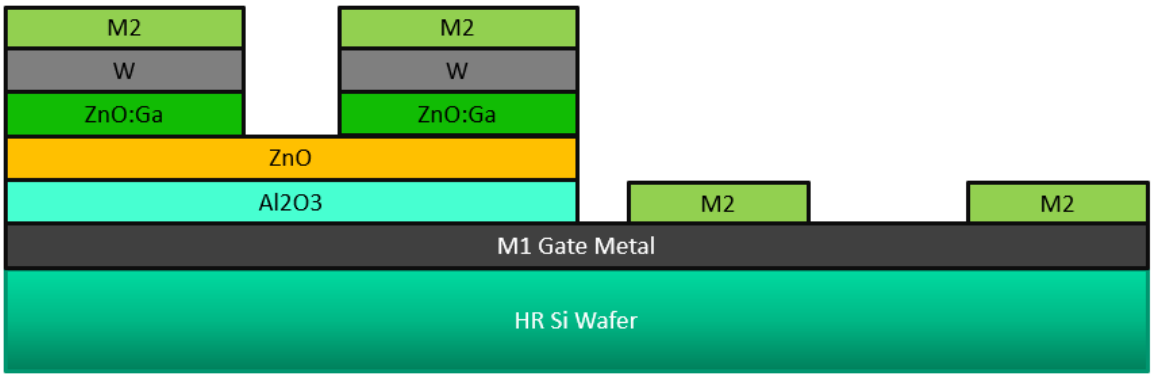



**Figure 43. Cross-sectional representation of the Ga-doped Ohmic layer deposited directly after the ZnO layer.**

The ZnO:Ga is cleared from the channel region of the ZnO TFT, but remains under the W contacts. The highly-conductive ZnO:Ga ohmic layer allows for negligible contact resistance with the W contacts. More experimentation will be needed to determine how thick to make the ZnO:Ga ohmic layer; the etch method

and etch rate for clearing the ZnO:Ga in the channel region; and finally, how thick to make the ZnO active layer to account for the ZnO:Ga over-etch.

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**14. ABSTRACT**

This research utilizes plasma treatments as a method to decrease the contact resistance on zinc oxide (ZnO) thin film transistor (TFT). In recent years, researchers have achieved gigahertz RF switch cutoff frequency with ZnO TFTs. To further increase the cutoff frequency, the total resistance of this device must be minimized. This research developed a method to integrate plasma treatments into the fabrication of ZnO TFT to decrease the contact resistance, thus increasing the cutoff frequency of the device. Three plasma treatment methods were used, including Ar plasma generated in an inductively coupled reactive-ion etch (ICP-RIE) chamber, Ar plasma applied in-situ in a metal-sputter chamber before sputtering tungsten (W) contacts, and by remotely generated hydrogen plasma. The plasma treatments were implemented after the deposition of ZnO and prior to the deposition of sputtered tungsten (W) contacts. The plasma treatments increased the conductivity of the ZnO, which allowed for the formation of ohmic contacts on the ZnO TFT. The contact resistance of the untreated ZnO TFT sample was 1.86 ohm-mm, while the ICP-RIE Ar plasma treatment, in-situ Ar plasma treatment, and H plasma treatment demonstrated minimum contact resistances of 1.18, 1.03, and

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