

# Interoperability and Cold-Spare Support for VLSI ICs Using a System-in-Package I/O Kit

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**Abstract**— VLSI ICs using sub-100 nm CMOS technology provide high speed and low power relative to larger geometry technology. However, at voltages above the breakdown voltage of individual I/O transistors, cold-spares support and interoperability with heritage I/O standards are problematic. A System-in-Package (SiP) methodology leveraging BAE Systems' family of radiation-hardened by design (RHBD) I/O chiplets simplifies VLSI IC design while supporting 3.3 V I/O and cold-spares operation. The SiP methodology and chiplets described support multiple technology nodes from 90 nm to at least 7 nm. Tristate I/O, Flash memory interface and ANSI/Vita 78 SpaceVPX applications illustrate use of the I/O chiplets.

**Keywords**—VLSI, System-in-Package, SiP, cold-spares, radiation-hardened by design, RHBD, chiplet, I/O, SpaceVPX, interoperability.

## I. INTRODUCTION

Improvements in semiconductor processing techniques have led to very large scale integration (VLSI) integrated circuit (IC) technology nodes advancing from 90 nm through multiple nodes to 7 nm and below [1]. The lower power consumption and increased gate density achieved with each new processing node makes such advances very attractive. Lower power supply voltages (1.5 V to 0.7 V) and transistor scaling partly enable these improvements but also reduce transistor breakdown voltage. Typically, dual or triple gate oxide I/O transistors and/or transistor stacking are used to support higher voltage (e.g. 3.3 V) I/O.

In applications such as high reliability space systems, integrated circuits are often in standby redundant configurations with no power applied and thus require cold-spares interfaces to other powered and active components. Many of these interfaces operate above the voltage that process nodes of 90 nm and below typically support without power applied to the I/O circuits. A System-in-Package (SiP) methodology using I/O chiplets to interface between low voltage VLSI IC I/O and system I/O provides cold-spares interfaces at the package level while reducing the number of I/O types that need to be supported in the VLSI IC.

## II. CONVENTIONAL PRACTICE

### A. VLSI High Voltage I/O

In addition to thin oxide devices used to optimize density, power and performance of core logic and memory, VLSI processes may provide thick oxide transistors supporting higher breakdown voltages. Extra processing steps required to provide these typically dual or triple oxide transistors increase wafer processing time and wafer cost. Without custom process steps or layout techniques, the thick oxide I/O devices often limit total dose hardness of the ICs. The larger geometries required for such devices also increase the area required on the VLSI die for I/O circuits. As core transistor oxide thickness shrinks due to scaling or newer geometries are adopted (e.g. FinFET, gate-all-around, etc.), providing I/O transistors to support high voltages becomes more complex and expensive. Furthermore, as core transistors scale to <1 V even triple oxide I/O transistors may not support the required I/O voltages, particularly when practical levels of overshoot and undershoot are considered.

Alternately, high voltage I/O circuits use a stack of lower breakdown voltage transistors. The transistor stack divides the high voltage strain over multiple transistors but requires multiple bias voltages. Fig. 1 shows a tristate driver implementation using four transistors.  $V_h$  switches between the I/O supply voltage,  $V_{supply}$ , and  $V_p$ .  $V_l$  switches between ground and  $V_n$ .  $V_{inout}$  switches between  $V_{supply}$  and ground. Bias voltages  $V_p$  and  $V_n$  are selected to keep all four transistors in a safe operating range. All voltages ( $V_{gs}$ ,  $V_{ds}$ , etc.) are limited by design to meet long term reliability requirements. In applications such as high reliability space systems, many ICs are in standby with no power applied so bias voltages  $V_p$  and  $V_n$  are not available making the I/O subject to damage.

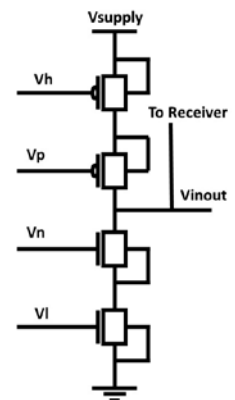


Fig. 1. Stacked transistor I/O uses bias voltages to split voltage stress across multiple transistors.

A so-called warm-spare approach uses a low current, auxiliary power source applied to just the I/O to maintain the bias voltages while the VLSI IC core is not powered. This requires on-die isolation between the I/O and VLSI core, reduces reliability of the standby VLSI device and may require an auxiliary power converter at the unit or chassis level if, for example, the unit must interface to another powered system while not powered. Thus, the warm-spare approach is also problematic.

### B. External Cold-Spare Buffering

VLSI I/O buffering through separate, larger geometry technology node (e.g. 180 nm) discrete devices or FPGAs commonly provides cold-spare interfaces when the VLSI technology does not natively support cold-spare at the required voltage. These extra packages significantly increase printed wiring board area, increase power consumption and often limit performance of the I/O interface. Signals such as enables and direction control for operating separate buffers or transceivers increase the VLSI package I/O count and further limit performance due to extra signal line length and capacitance on the printed wiring board.

## III. SYSTEM-IN-PACKAGE I/O INTERFACES

### A. Overview

Our System-in-Package (SiP) methodology uses I/O chiplets packaged with one or more VLSI ICs to interface between standard VLSI IC I/O and system I/O<sup>1</sup>. Fig. 2 illustrates the method with a top view of a package substrate layout with one VLSI IC and several I/O chiplets. SiP packaging of I/O chiplets provides several advantages over alternative methods. First, I/O chiplets developed in a technology such as 180 nm CMOS support both cold-spare I/O at high voltage (e.g. 3.3 V) and adequate performance at lower voltage (e.g. 1.8 V) to interface with VLSI ICs. Use of radiation-hardened by design (RHBD) techniques ensures high total dose tolerance for space applications. Second, the VLSI IC only needs to support a few I/O types such as 1.8 V LVCMOS, LVDS and perhaps SerDes. Chiplets provide the unique I/O support for other voltages and requirements such as open drain (e.g. I<sup>2</sup>C) or 3.3 V PCI. Third, terminating enable and direction control signals at the chiplets within the SiP,

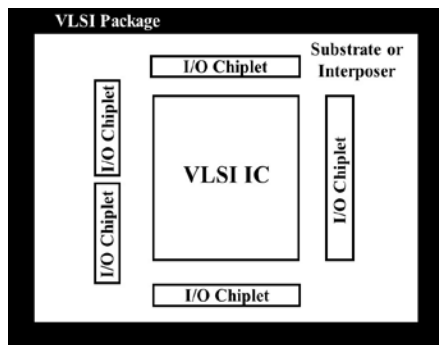


Fig. 2. Top view of package substrate with VLSI IC and I/O chiplets.

<sup>1</sup> Patent pending.

reduces package I/O and improves performance. Fourth, a family of I/O chiplets using a few standard chiplet footprints (die size, I/O, power and ground locations) provides flexibility in interfacing the same VLSI IC to different system I/O required across multiple applications. A final key advantage is that one family of I/O chiplets supports many VLSI technology nodes. The 1.8 V VLSI interface chiplets described herein support at least eight technology nodes from 90 nm to 7 nm [2]. With proper choice of chiplet technology and I/O design style, voltages above 3.3 V for external interfaces and below 1.8 V for VLSI IC interfaces are also achieved.

### B. Chiplet Family

There are many +3.3 V LVCMOS unidirectional and bidirectional functional signals such as individual control lines and interrupts in heritage space designs. There are also a number of I/O protocols operating at 3.3 V including I<sup>2</sup>C, SPI, PCI and legacy memory (FLASH, PROM, SRAM and SDRAM). Our initial family of 180 nm RHBD I/O chiplets supports all of these I/O interfaces plus LVDS for protocols such as SpaceWire. The family includes 21 chiplet types using three standard and one custom footprint. The smallest footprint (2.475 mm x 2.1 mm) supports nine chiplet types including up to 16 LVCMOS transceivers, 16 bi-directional transmission gates, 16 bi-directional open drain interfaces or 8 LVDS buffers per chiplet. The intermediate footprint (2.475 mm x 2.85 mm) supports eight chiplet types including 16 LVCMOS transceivers with direction control per pair, 16 LVDS buffers, SpaceVPX control interface and FLASH interface buffer. The largest standard footprint (2.475 mm x 5.35 mm) supports three chiplet types including 64 bi-directional transmission gates, triple modular redundant (TMR) FLASH interface, and 8-port SpaceWire buffer. A custom footprint (2.475 mm x 8.35 mm) supports a full 32-bit PCI interface. Standardized chiplet width and common footprints facilitate a reticle layout containing a process monitor die and all 21 chiplet types, many with multiple copies. The small size of each chiplet and use of conservative design rules provides high yield to minimize cost.

Radiation-hardened by design (RHBD) techniques enable the chiplets to operate in harsh radiation environments. A combination of edgeless transistor design and full guard-ring layout techniques mitigates Total Ionizing Dose (TID) radiation effects. Furthermore, the guard-ring structures prevent Single Event Latchup (SEL) from occurring. Single Event Effects (SEE), particularly Single Event Transients (SET), are mitigated using hardware proven circuit design techniques. Similarly, other included design techniques enhance operation in high dose rate environments.

## IV. EXAMPLE APPLICATIONS

### A. Tristate Low Voltage CMOS I/O Interface

Chiplets typically support eight or more tristate interfaces. Fig. 3 shows one tristate I/O and illustrates how a chiplet converts 1.8 V tristate I/O on a VLSI IC to 3.3 V cold-spare tristate I/O. The VLSI IC uses any technology that supports 1.8 V CMOS I/O. That includes at least eight nodes from 90 nm down to 7 nm [2]. Cold-spare is not required for the VLSI

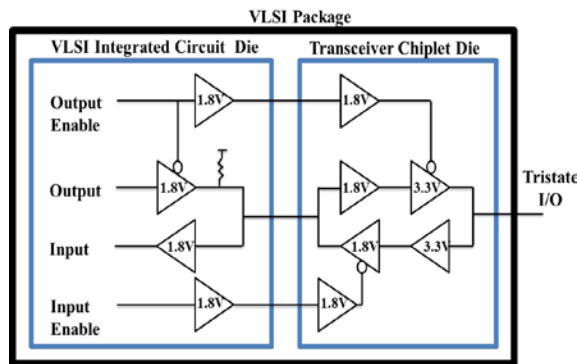


Fig. 3. VLSI IC to chiplet interface for tristate I/O keeps input and output enables within the VLSI package.

I/O since the chiplet does not drive the VLSI IC when powered down and protects the VLSI IC from the potentially active external interface. The VLSI IC provides input and output enables to the transceiver chiplet. These outputs are required since the VLSI IC does not support the required 3.3 V and cold-spares operation. The conventional solution using an external transceiver requires these additional outputs from both the VLSI IC and the package. In addition, the VLSI IC would require higher power output drivers and external transceivers typically limit performance.

### B. Triple Modular Redundant Flash

Space systems often achieve high reliability for non-volatile memory using triple modular redundant (TMR) Flash. Switching Flash memory devices off when they are not in use improves reliability [3]. Since the VLSI IC providing the Flash controller typically performs other functions and remains powered, a cold-spares interface is required between the VLSI IC and Flash devices.

The Flash devices do not provide a cold-spares interface. While power is off, Flash device inputs must be at a low voltage. The VLSI IC cannot simply drive those inputs to a low level before removing Flash power since some of the control signals are active low. Another issue is that the VLSI IC NAND controller inputs must be at known, valid logic levels during Flash power-off state and cannot float to an intermediate voltage.

Fig. 4 illustrates two methods for using chiplets to provide a reliable interface. Method a) uses a transfer gate chiplet between the VLSI IC and Flash control and status signals. When Flash devices do not have power, the transfer gates open and resistors set voltage levels at safe values. Cold-spares LVC MOS chiplets protect the data I/O since their outputs are driven low before removing power. Method b) uses chiplet(s) with internal cold-spares interface to isolate and protect the I/O. The portion of the chiplet(s) interfacing with the VLSI I/O remains powered whereas the portion interfacing with the Flash devices does not receive power. Method b) requires switched power to the VLSI package that is not required for method a).

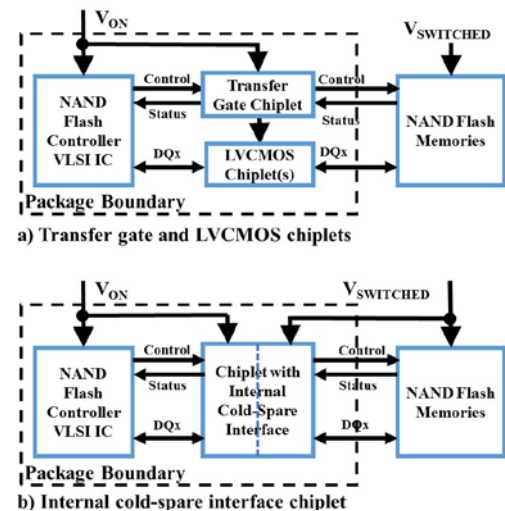


Fig. 4. Switching Flash memory power off while using either cold-spares method a) or method b) improves Flash reliability.

### C. SpaceVPX Interfaces

SpaceVPX [4] is a recent form factor standard [5] developed to meet the needs of current and future space electronics digital modules. When applied to spacecraft payloads SpaceVPX offers a high degree of fault tolerance, interoperability, scalability and flexibility. References [6] and [7] describe several SpaceVPX modules implemented across the industry.

Fig. 5 shows a typical SpaceVPX system. The system includes dual-redundant power supplies, system controller modules, and data-plane switch modules; six payload modules in an n of m redundant configuration; and two internally redundant Space Utility Management (SpaceUM) modules. The data, control, utility and expansion signal planes shown in the bottom of Fig. 5 interconnect the modules in a redundant manner such that there are no single points of failure in the system. The SpaceUM modules control power to each module individually with redundant modules typically powered off. These modules, operating as cold-spares, reduce power consumption, reduce thermal load on the spacecraft and improve system reliability. The signal planes interconnect powered and cold-spares modules thus requiring cold-spares I/O.

Fig. 5 illustrates the SpaceVPX modules interconnected via the four types of signal planes and a typical set of chiplets. Various VLSI ICs (not shown), supported by the I/O chiplets, perform the main functions of the modules. Five different types of I/O chiplets provide all required signals for the control, utility and expansion signal planes. The RapidIO data plane uses AC coupled SerDes signals that are typically cold-spares capable provided that powered transmitters do not babble into SerDes receivers that are not powered. For an unavoidable babbling SerDes transmitter, a cold-spares SerDes chiplet before the SerDes receiver (not shown) provides a reliable interface. I/O chiplets enable SpaceVPX systems with redundant power-switched modules to provide maximum fault tolerance and reliability.

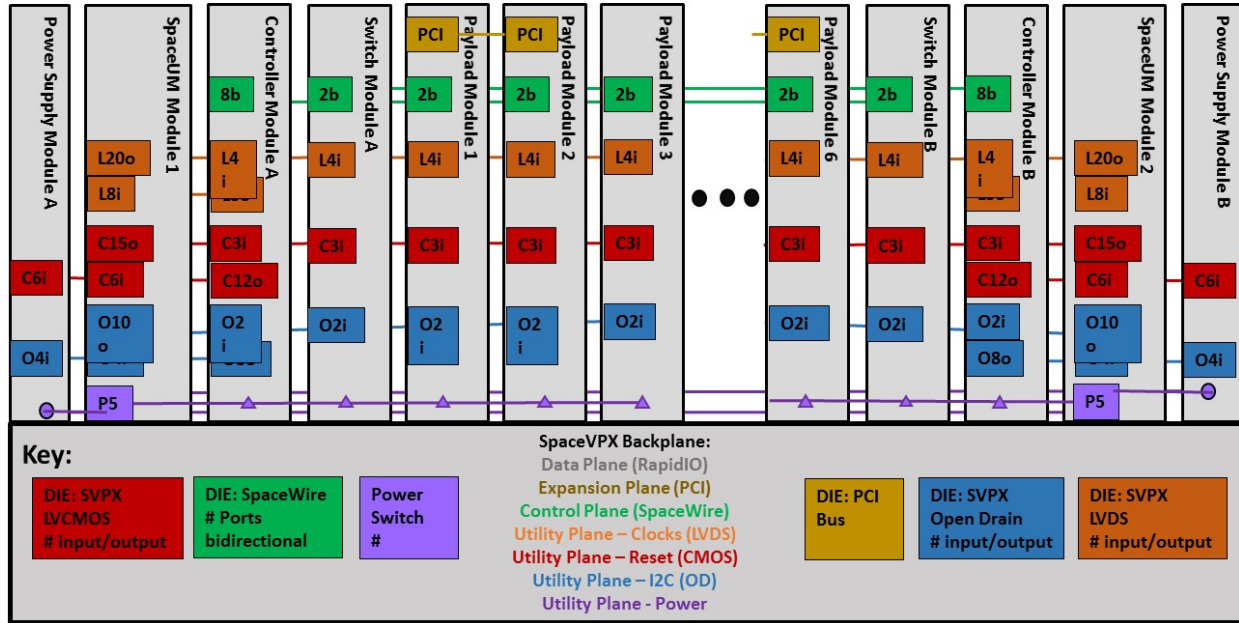


Fig. 5. Five types of I/O chiplets provide cold-spares interfaces for control, utility and expansion plane signals in a SpaceVPX system.

## V. SUMMARY

A family of I/O chiplets solves a wide variety of interface challenges that arise using deep submicron integrated circuits. Directly supporting only a few types of I/O and interfacing with chiplets that support additional I/O types, I/O voltages and cold-spares operation simplifies VLSI ICs. Common footprints and die sizes for various types of chiplets permits changing I/O types at the package level by simply changing the chiplets packaged with the VLSI IC. This commonality also reduces manufacturing cost through standard wafer probes, similar test patterns and simplified wafer layout.

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