RHBD Techniques for a Sub-Sampling Phase-Locked Loop in 32nm PD-SOI

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***Abstract*—This work details radiation-hardened by design (RHBD) techniques applied to a 15GHz sub-sampling quadrature phase-locked loop (PLL) in the 32nm partially-depleted silicon-on-insulator (PD-SOI) technology node. Radiation vulnerabilities are identified and both component and system level techniques are utilized to mitigate them. This work will provide RF circuit RHBD insight at 32nm PD-SOI and contribute to existing RHBD infrastructure.**

Keywords—Phase-locked Loop (PLL); Radiation hardened by design (RHBD); Single-event Transients (SETs); Single-event Upsets (SEUs).

I. Introduction

Phase-locked loops (PLLs) are versatile circuits most often utilized in clock and communication systems for generation, distribution, synchronization, and recovery of clock signals. Previous research has shown PLLs to be vulnerable to radiation induced perturbation and degradation [1]. Mitigation of radiation effects in PLLs is particularly important due to the reliance of downstream circuits on the PLL output. This work presents a radiation hardened by design (RHBD) 15GHz charge-pump PLL in 32nm partially-depleted silicon-on-insulator technology, which leverages both component and system level hardening techniques.

II. Background

A. Phase-locked Loops

A PLL is a circuit that utilizes negative feedback to generate a periodic signal with a phase corresponding to the phase of an input reference signal. Core components of charge-pump PLL (CP-PLL) circuits include the phase frequency detector (PFD), charge-pump (CP), low-pass loop filter (LPF), voltage-controlled oscillator (VCO), and frequency divider. The PFD measures the phase error between a reference signal and the PLL output signal then sends a corresponding UP or DOWN control signal to the charge pump. The charge-pump sinks or sources charge from the LPF capacitor based on these control signals. The LPF sets the loop characteristics and aids in stabilizing the loop by filtering out high frequency noise and feedback. The VCO generates a periodic output signal with a frequency proportional to the analog voltage seen at the output of the LPF. The frequency divider is used to divide the frequency of the PLL output signal by an integer multiple before passing it to the PFD, allowing for an output frequency higher than that of the reference signal.

A linear model was used to approximate the behavior of the CP-PLL and is shown in Fig. 1 [2]. In the model the input and output are the phase of the reference and VCO waveforms, respectively. The PFD-CP is modeled as the difference between the reference and feedback phase multiplied by the charge pump gain (K_{PD}). The LPF is modeled as its s-domain transfer function and the VCO is modeled as an integrator with a gain (K_{VCO}). Lastly, the feedback divider is modeled as a division of the output phase by the divide ratio N. PLLs can be implemented with dual feedback loops in which one maintains frequency and other phase lock. This will be discussed in more detail in the design overview.

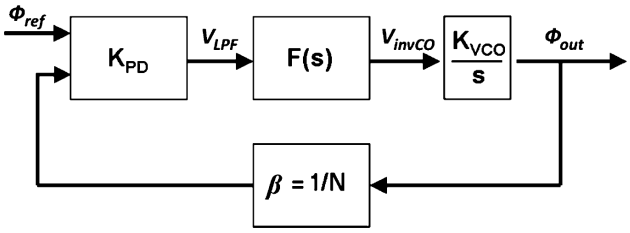

Fig. 1. Charge pump phase-locked loop linear phase domain model [2].

B. PLL Radiation Vulnerabilities

Research has shown PLLs are vulnerable to SEEs (single event effects). A SEE can result in significant performance perturbations, which can have serious consequences depending on the sensitivity of downstream systems. Types of SEEs include single event upsets (SEUs) and single event transients (SETs)[3][4]. A SEU occurs when an ion strike results in a stored digital value changing its state. Vulnerable PLL components include those with digital circuitry that store a state such as the PFD and frequency divider. An SEU can introduce error in the negative feedback loop by triggering an incorrect PFD or frequency divider output resulting in phase error due to the charge-pump setting an incorrect VCO control voltage. A SET occurs when a voltage is temporarily perturbed by an ion strike. Additional vulnerable PLL components include those with analog signals such as the charge-pump and VCO. A SET can introduce error through a perturbation on the VCO control voltage node by a strike to the charge-pump or alter the VCO phase directly by a strike to the VCO [1]. Additionally, a SET can result in an upset in some instances

such as in the PFD. Regardless of the strike location the resulting loop behavior can be characterized in terms of a voltage perturbation on the VCO control voltage, a loop recovery time, and an output phase error [2].

In addition to SEEs, RF circuits in PD-SOI technologies have been shown to be moderately vulnerable to total-ionizing dose (TID) and temperature-combined effects [5][6]. While the 20.4GHz LC tank VCO in 32nm PD-SOI of [5] exhibited acceptable TID performance degradation at room temperature, it exhibited notably higher performance degradation when the irradiation was combined with high temperature (100°C). Due to the wide operating temperature range target for this PLL consideration of combined temperature effect is important. Resulting degradation effects included increased phase noise, shifted the tuning range and decreased output power. Phase noise degradation is anticipated and designed for with a wide phase loop bandwidth and a tuning range to allow for maximum VCO phase noise suppression. Potential shifts in tuning range are compensated for with switched capacitor banks allowing external correction. Device level design decisions may also increase robustness to TID. One paper [7] found that body-contacted devices have superior TID tolerance and should be used in lieu of floating body devices where applicable. Additionally, increased device finger widths may be used to improve TID tolerance.

III. PLL DESIGN

A. Performance Specifications and PLL Architecture

One objective of this work is to achieve a rad-hard PLL design with performance specifications comparable to modern-day un-hardened PLL counterparts. Four important performance specifications are output frequency, tuning range, phase noise and lock time. The nominal output frequency of this design is 15GHz with a target tuning range of +/-10%. The phase noise specification is -110dBc/Hz at 1MHz offset and the maximum lock time target is 2µs. Supply voltage, temperature, and radiation tolerance specifications must be met. Design performance must remain in specification for a supply voltage variation of +/-5% and operational over the full temperature range of -55°C to 125°C. Lastly, the design must be tolerant to TID up to 300 krad(SiO_2) and employ circuit and system level SEE mitigation measures to minimize the perturbations that propagate to and are observed at the output.

This design utilizes a sub-sampling architecture introduced in [8] due to its advantages in noise performance. Fig. 2 displays the system level block diagram for this architecture in which dual feedback loops replace the traditional single loop. The first loop controls frequency lock and is designed as a typical CP-PLL feedback loop except that it contains an intentional dead zone in its response to phase error. This blocks the PFD output for any absolute phase error under 180˚, allowing the second feedback loop to take control. A schematic representation implementing a PFD with a dead zone in its response is shown in Fig. 9. This loop controls the phase lock once the frequency loop has reduced the phase error under 180˚. The phase loop is not designed as a typical CP-PLL feedback loop. Instead this loop leverages direct sampling of the VCO output using a sub-sampling phase detector (SSPD). This results in a reduction of phase noise by increasing the CP feedback gain $ß_{CP,}$ which is defined to be the CP gain divided by the divide ratio N. The CP feedback gain is much higher in a sub-sampling architecture and this suppresses in-band loop noise. More detail can be found in [8]. An important characteristic of the phase loop is that it is frequency agnostic and may lock on a harmonic of the lock frequency. Therefore a frequency loop is needed. This loop responds to any frequency error that accumulates at least 180° of absolute phase error. Once it reduces the frequency error the phase loop is able to take control and reduce the phase error to its steady state value. Simulations showed a maximum pull-in range for the phase loop of about 40MHz for the nominal output frequency of 15GHz.

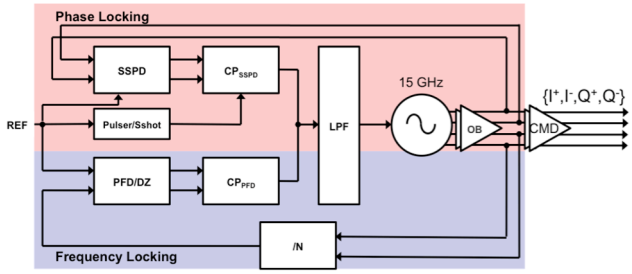

Fig. 2. System level block diagram of a quadrature PLL implementing phase (top) and frequency (bottom) feedback loops in a sub-sampling architecture.

B. Component and Loop Design

The quadrature VCO topology utilizes two coupled LC tanks resulting in four outputs spaced 90° apart. An LC tank VCO is used due to its superior noise performance and stability at the target frequency range. The LC tank utilized a complementary cross-coupled pair topology due to its increased voltage output swing and higher inductance relative to an NMOS or PMOS-only topology. A complementary topology splits the inductance across each half of the tank, allowing a larger inductance to be used relative to what a NMOS or PMOS-only topology would allow. Fig. 3 displays the 575µm by 350µm layout of the VCO.

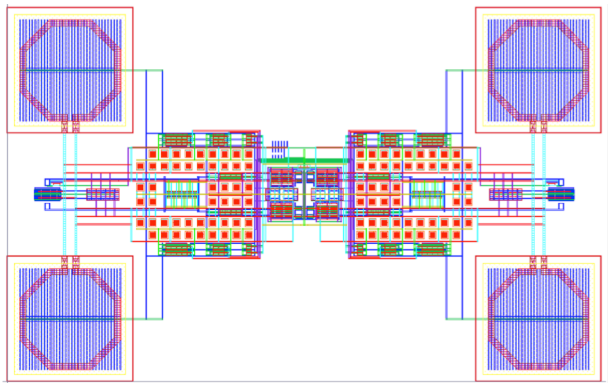

Fig. 3. VCO layout with dual coupled LC tanks (left and right side) producing quadrature outputs. Each LC tank incorporates two inductors in parallel.

The VCO buffers were designed with source followers followed by NMOS current mode logic (CML) differential pairs. CML is used due to its compatibility with high frequency operation. CML latches were used for the initial stages of the frequency divider while DICE flip-flops were used for the later stages. The PFD charge pump was designed using a current steering topology referred to as an active amplifier single-ended charge pump in [9]. The sub-sampling detector and charge pump used the topology provided in [8].

A 3rd order loop filter is used to set the loop characteristics, designed to maximize the bandwidth tuning range of the phase loop while maintaining sufficient phase margin. The calculated phase loop bandwidth tuning range is 15 to 35MHz with a phase margin of approximately 30°. Behavioral models for each PLL component were used in the tuning the loop filter and characterization of the radiation response. These models were substituted one by one into the full closed-loop circuit and simulated.

C. Design Results

Fig. 4 displays the lock-in behavior of the PLL for an initial control voltage of 200mV. The response demonstrates the transient behavior of the dual feedback loop topology. The frequency loop activates every time the absolute phase error exceeds 180˚. The phase loop completes the locking process and maintains lock at steady state operation.

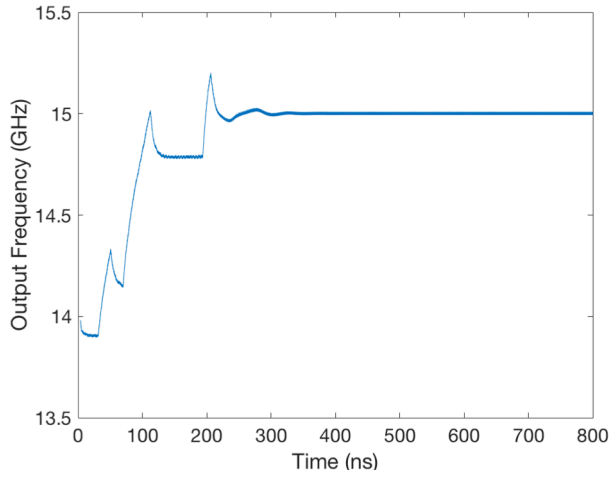

Fig. 4. PLL output frequency during lock acquisition. The frequency loop activiated three times before acquistion process was completed by the phase loop at approximately 300ns.

The simulated output frequency range of the VCO is 15GHz +/-15% for a control voltage of 100-800mV. Parameter degradation is likely to occur at the edges of this voltage range. The charge pump current mirror performance begins to degrade for output voltages under 250mV. The simulated phase noise is within the target specification by 10dBc at 1MHz offset based on the calculated loop bandwidth. These phase noise results do not include parasitic elements extracted from the layout, which may lower the Q factor of the LC tank in the VCO, resulting in increased phase noise.

Design components were simulated across temperature, supply voltage and corner variation. Some parameter degradation occurred but each design component remained operational across all variation simulations. The VCO frequency shifted under +/-1.25% for a +/-5% change in supply voltage and under +/-1.5% over the operating temperature range. The variation in PFD-CP output current was under +/-4% for a +/-5% change in supply voltage using external biasing.

IV. RHBD Techniques and Results

A. Loop Level Radiation Response Characterization

To characterize the radiation vulnerability of a PLL design a metric is needed to quantify the degree to which a SEE disturbs the output. Introduced in [1], Equation 1 is the instantaneous normalized phase displacement ($Ø_{DISP}$) between the output signal at lock and the output signal during a disturbance. T_{lock} is the period of the output signal during steady state operation and T_e is the instantaneous period of the output.

$$\phi_{disp} = 2\pi * \frac{|T_e - T_{lock}|}{T_{lock}} \quad (1)$$

With the identification of a performance metric, the worst-case $Ø_{DISP}$ and the conditions for its occurrence can be determined. This work leverages the generalized linear model for SET propagation in PLLs presented by Loveless in [2] to gain insight into the hardness of the design based its loop characteristics. The model encompasses transient perturbations generated within each PLL component and models them as a transient on the VCO control voltage. Loveless also derives the worst-case output $Ø_{DISP}$, shown in Equation 2, due to a SET based on loop characteristics including the natural frequency (ω_n), the ideal recovery time (t_{rec}), the lock frequency (f_{lock}), and the divide ratio (ß). The natural frequency is the oscillation frequency of the 2nd order closed loop system response. The ideal recovery time is the minimum time required for the loop to recover excluding non-ideal behavior of system components. The lock frequency (f_{lock}) is simply the steady state output frequency of the VCO. For positive frequency modulations the terms in the denominator are added while for negative frequency modulations they are subtracted.

$$\phi_{disp} = \frac{2\pi\omega_n^2 t_{rec}}{\beta f_{lock} \pm \omega_n^2 t_{rec}} \quad (2)$$

When Equation 2 is plotted for a negative frequency modulation with t_{rec} as the independent variable, there is a value of t_{rec} for which $Ø_{DISP}$ increases dramatically (or becomes non-linear). This occurs because as the instantaneous output frequency decreases, T_e and therefore $Ø_{DISP}$ eventually approach infinity. Termed the critical time constant τ_{crit}, this value represents the minimum recovery time for the initial perturbation needed to maximally disturb the PLL. $Ø_{DISP}$ may

also be plotted vs. the deposited (or sunk) charge Q_{SET} calculated by multiplying the ideal recovery time by the charge pump current and setting SET duration t_{SET} to zero. Fig. 5 displays $Ø_{DISP}$ of the phase loop vs. the charge Q_{SET} removed by an SET. The blue curve represents the $Ø_{DISP}$ for a PLL with a wideband VCO. The critical time constant τ_{crit} is represented by the vertical black dotted line. The maximum $Ø_{DISP}$ for the narrowband VCO of this design is shown as the red horizontal dotted line. The green line approximating the new $Ø_{DISP}$ vs. Q_{set} relationship demonstrates how it saturates due to the bandwidth limitations of the narrowband VCO and results in the immunity of this design to the τ_{crit} vulnerability. Design recommendations and procedures on how to increase τ_{crit} to improve hardness in applications utilizing wideband VCOs can be found in [2].

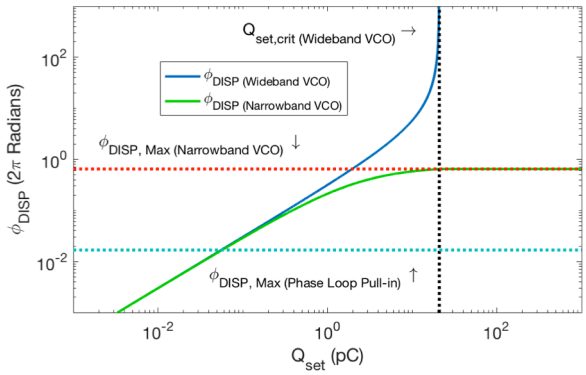

Fig. 5. Calculated worst-case $Ø_{DISP}$ vs. control voltage node sunk charge for an ideal phase loop with an ideal wideband (dark blue) VCO and this design's narrowband (green) VCO. $Ø_{DISP}$ corresponding to max pull-in frequency of phase loop (cyan).

B. *Frequency Loop Recovery Characterization*

Every loop recovery from a SET perturbation will be one of two types. Either the loop will recover with only the phase loop or both the phase and the frequency loop are activated. Shown in light blue on Fig. 5 is the $Ø_{DISP}$ corresponding to the maximum pull-in frequency of the phase loop. This shows that any SET induced perturbations that can be recovered from by only the phase loop have limited impact on the PLLs operation and cannot increase the $Ø_{DISP}$ above 16.8mRadians. Since the maximum $Ø_{DISP}$ only occurs due to perturbations that result in the frequency loop being activated, a top priority is minimizing the probability of frequency loop activation as well as its recovery time.

The $Ø_{DISP}$ model results in Fig. 5 use the phase loop parameters and does not consider the frequency loop. This model cannot be applied to the frequency loop in the same way due to the non-linearity introduced by the dead zone in the response and the limited pull-in range of the SSPD in the phase loop. If the frequency loop reduces the frequency error to just above that of the pull-in threshold needed by the phase loop, then the loop can stay out of lock for hundreds of nanoseconds while the phase error accumulates to the 180° needed to activate the frequency loop again. An example of this is displayed in Fig. 6 and the topic is discussed in [11].

Fig. 7 displays $Ø_{DISP}$ for the full PLL circuit due to a SET strike at 1.2µs resulting in a PFD state change. The cause and outcomes of a state change will be discussed later in more detail. The lock frequency is 15GHz, CP current is 90µA and the divide radio is 32. The red horizontal line represents the maximum possible $Ø_{DISP}$ for which the phase loop could recover without the frequency loop. For nominal CP current a SET that activates the PFD charge pump may result in a $Ø_{DISP}$ an order of magnitude above that of a SET recoverable with only the phase loop.

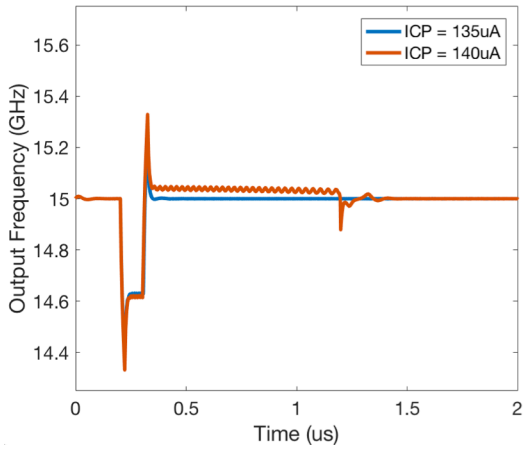

Fig. 6. PLL output frequency during a frequency loop perturbation for two nearly identical charge pump currents. This demonstrates the non-linearity introduced by the dead zone behavior and limited pull-in range of the SSPD.

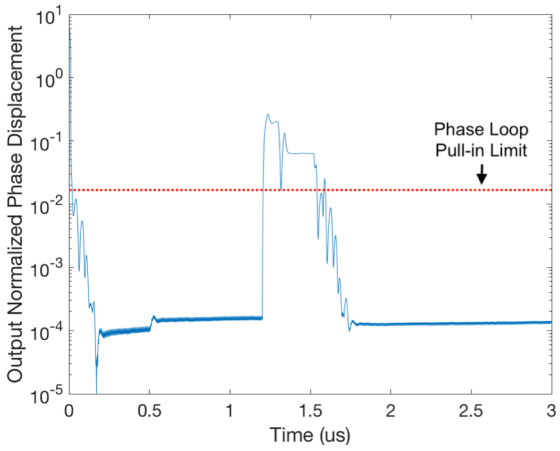

Fig. 7. Output phase displacement ($Ø_{DISP}$) during lock aquitistion and a SET perturbation resulting in activation of the frequency loop. The max $Ø_{DISP}$ corresponding to the phase loop pull-in range is also shown.

Since the highest $Ø_{DISP}$ occurs due to SEEs that result in the frequency loop CP being activated it is beneficial to look at the relationship between CP current, loop recovery time and $Ø_{DISP}$. Fig. 8 displays the relationship between these using a behavioral model of the loop. Graph (A) in Fig. 8 displays the maximum $Ø_{DISP}$ over current while graph (B) displays the recovery time. The recovery time is found by taking the moving average of $Ø_{DISP}$ and finding the time at which it drops

below 200µRadians. While the max $Ø_{DISP}$ has a clear increasing trend over charge pump current, recovery time does not. This is because of the non-linearity introduced by the dead zone. These results show that as long as lock-in time specifications are met, low current values in the range of 40µA to 75µA result in the lowest maximum $Ø_{DISP}$ and highest regularity of the recovery time.

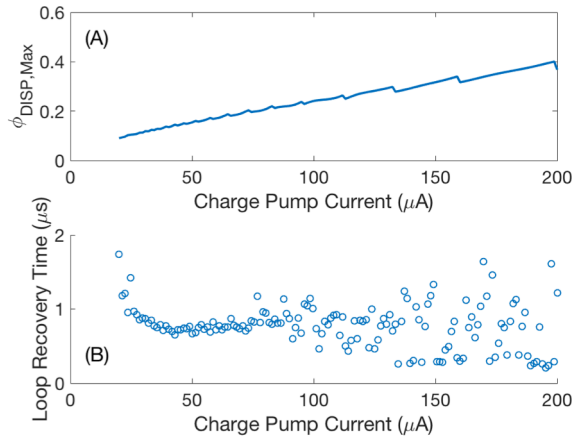

Fig. 8. (a) Maximum $Ø_{DISP}$ in radians for PLL behavioral model vs. charge pump current, (b) Loop recovery time in µS of PLL behavioral model vs. charge pump current. Non-linearity due to PFD dead zone and limited SSPD pull-in range.

C. *Phase Frequency Detector State Change Vulnerability*

Fig. 9 displays a behavioral schematic of the PFD and dead zone circuit. The PFD detects rising edges of input signals and is vulnerable to SETs. Due to this vulnerability a SET can result in a PFD state change that persists multiple reference cycles. Fig 8 displays the reference (REF), feedback (FB) and DOWN current control signals with each PFD state annotated on the rising edge that sets it.

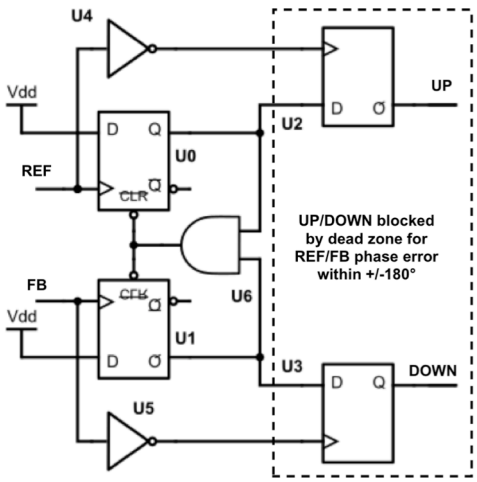

Fig. 9. PFD with dead zone behavioral schematic. Output flip flops only pass high UP or DOWN signal from PFD if it remains high for over 180˚.

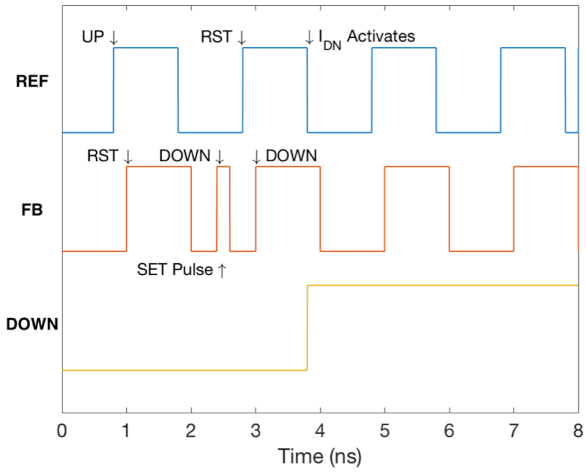

Fig. 10. Reference, feedback and CP down control signal during SET that results in a PFD state change.

For the state change to occur, the SET must set an UP state if the FB is leading and a DOWN state if the REF is leading. This results in the charge pump being activated on the next falling edge of the lagging signal. Since the PFD state has been reset, the CP will remain enabled until the FB rising edge shifts to within 180° of the adjacent REF rising edge. The SET is causing the PFD to change which rising edges it is attempting to align. SET pulses causing this may originate in the output stages of the frequency divider, the input buffer inverters in the PFD, or in the PFD logic itself. This is the worst-case vulnerability identified in this design as it results in the activation of the PFD charge pump and a frequency loop feedback signal shift up to 180°.

D. *Component Radiation Response Characterization*

The VCO and loop characteristics limit the worst-case perturbations due to SEEs and hardening of individual components can be used to further harden the design. Conventional circuit radiation hardening techniques were applied to PLL components such as the frequency divider and PFD. DICE flip-flops were used in the frequency divider and dead zone generation circuit in place of conventional flip-flops. Bias currents in both charge pumps were made to be externally tunable and capacitors were added to some biasing circuit nodes for increased immunity. Also the dummy node and buffer utilized in the charge pump's current steering topology improves CP SET mitigation by reducing the voltage across the output switching transistors. This is utilized in both charge pumps. The component RHBD techniques reduce but do not eliminate the potential for SET and SEU induced perturbations. This section identifies potential remaining vulnerabilities at steady state operation and possible future work to mitigate them. Validated bias-dependent single event models for 32nm were utilized to characterize the radiation response [10] with an LET of 100MeV-cm^2/mg.

The quadrature LC Tank VCO exhibited inherent robustness to SETs due to its high quiescent current and its coupled architecture. SEE strikes on the PMOS and NMOS

cross-coupled pair as well as the tail source were simulated. Simulations showed that while a single strike may disrupt one or two periods of the VCO output, its effect on the control loop or VCO control voltage was inconsequential. The phase loop quickly corrected any minor phase shift and the frequency loop did not activate.

The VCO output buffers and first three stages of the frequency divider utilize current mode logic (CML) due to the high output frequency. SET strikes to the CML buffers were found to cause up to four cycles in the output signal to be dropped at the nominal frequency of 15GHz. This results in an approximately 250ps pause in the output of the buffer. As with a strike to the VCO, the frequency loop did not activate and the maximum $Ø_{DISP}$ was inconsequential.

SET strikes to the PFD charge pump output switches were simulated. The CP active amplifier single-ended charge pump topology [9] minimizes the voltage across the output switches while inactive, thus reducing the charge collected when the switching transistors are struck. The frequency loop did not activate and the PLL recovered with only the phase loop. SET strikes to the CP control signals only activated the CP for the length of the SET and did not result in the activation of the frequency loop.

E. Discussion and Future Work

These techniques are being incorporated into a comprehensive quadrature PLL for fabrication in 32nm. Future work includes developing a mitigation technique for the PFD state change vulnerability. The PFD state change is the only identified vulnerability that requires frequency loop activation to recover and thus results in the highest $Ø_{DISP}$. Mitigation of this vulnerability would decrease the max $Ø_{DISP}$ of any identified vulnerability by an order of magnitude. One possible solution is a lock detection and indication circuit that resets the PFD immediately after the first activation pulse while the loop is in lock. This would prevent a CP activation time of longer than the reference period, which could be easily corrected by the phase loop alone. In addition, more research into the impact on radiation vulnerability of the non-linearity introduced by the PFD dead zone is needed.

V. CONCLUSION

This work detailed RHBD techniques applied to a 15GHz sub-sampling quadrature PLL in 32nm PD-SOI. Previous research and data from the 32nm PD-SOI technology generation was used in the form of data-calibrated bias-dependent SE models to identify vulnerabilities. Both component and system level techniques were utilized to mitigate vulnerabilities and harden the design. This work contributes insight and results on the application of RHBD techniques to a high performance sub-sampling PLL at the 32nm PD-SOI node.

ACKNOWLEDGMENT

This work was supported in part by the Defense Threat Reduction Agency under grant HDTRA1-17-1-0003. The authors would like to thank the Cadence Design Systems and Mentor Graphics University programs for providing access to design, verification, and simulation tools.

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