Fast, Full Chip Image Stitching of Nanoscale Integrated Circuits

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***Abstract*— The rapid progression of semiconductor technology has significantly impacted the ability to examine and analyze complex integrated circuits (ICs). Small device feature sizes, combined with large die sizes, add a heavy processing burden that severely limits our timely ability to perform defect validation and anti-tampering analysis at full scale.**

In this paper, we describe the algorithmic steps taken in the processing pipeline to quickly create a global image database of an entire advanced IC. We focused specifically on the image alignment and stitching algorithms necessary to support a combined field-of-view of a given layer of a die. We describe key algorithmic challenges such as contextual semantics that limits the robustness of the alignment algorithm. We also describe the use of database indexing to manage and traverse the enormous amounts of data.

Keywords— SEM, chip delayering, image stitching, nanoscale, IC failure analysis, anti-tampering, reverse engineering.

I. Introduction

Large area de-processing [1] and nanometer scale imaging tools [2] are now available. For example, a plasma source FIB-SEM approach can delayer large chip area by removing IC materials [3]. However, defect validation in failure analysis cases and anti-tampering verification of state-of-art ICs can only be performed in isolation with limited scope and speed in analysis. Full scale analyses of the whole IC die are problematic because, as minimum device feature size shrink and the number of devices multiply, the complexity of the image processing and the size of the global IC image data base poses an ever-challenging workload. Full scale IC analysis is important because state-of-art IC are particularly vulnerable to insertion of sparse modification that are difficult to identify and can compromise critical functionality and reliability.

For large chip dies, the challenges in chip delayering is the consistency and robustness. That is, the surface quality needs to be good and uniform so that image quality does not degrade. Furthermore, the surface plane should be planar such that imaging can be consistent on a single IC layer. For example, a bevel delayering output would cut across multiple IC layers including metal and via layers. Furthermore, with non-planar transistors in small geometry transistors, ultra-planar delayering may be important to properly extract transistor circuitry from captured images.

This paper is structured as follows: Section II provides background information on our teardown system and workflow. Section III provides details on the algorithmic steps to align and stitch SEM images and quickly create a global image database of the IC. Section IV includes results and analysis of algorithms. We conclude this paper in Section V.

II. Background

A. Image Processing System

We have developed an image processing system and associated software stack SEM imagery. The image processing system hardware consists of heterogeneous processors (multicore CPU and GPUs) connected to high density memory storage system. We use an Infiniband network switch to provide high bandwidth access between the processors and memory storage. As shown in Figure 1, the system is housed in a server cabinet as the high performance computing companion to the Zeiss MultiSEM (mSEM). We structured the hardware in a streaming fashion such that we can process images as they are captured by the mSEM.

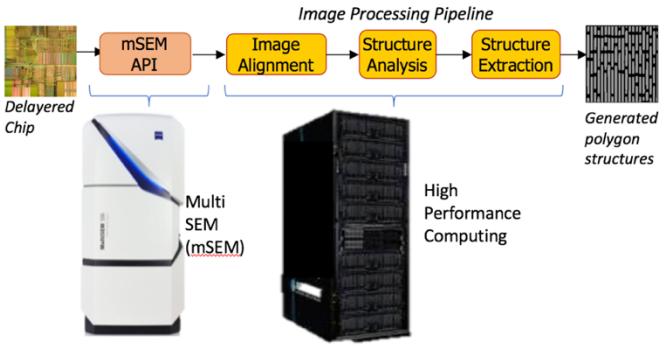

Fig. 1. Image processing pipeline of de-processed chip

The system runs a software application developed to interface with the mSEM, process the captured images, and store the imagery into the storage system. The dataflow diagram in Figure 1 illustrates the image processing steps, including image alignment, structure analysis and structure extraction. Figure 2 presents the resulting data from image processing steps. The system also analyzes and generates metadata related to the imagery, including alignment, structure, and other parameters. We have developed an interactive visualization tool that allows the operator to visually see the images, its associated quality, and the metadata in a manner that supports an efficient delayering workflow.

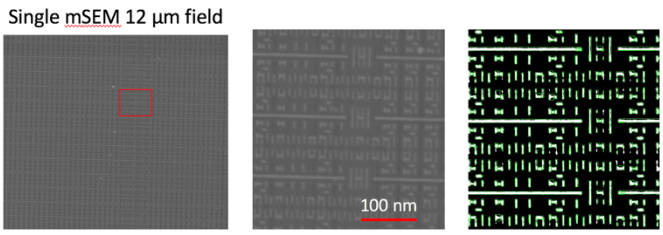

Fig. 2. Example processed output from data capture (left), alignment (middle), and structure generation (right)

B. *Image Processing Software*

In this paper, we focus on the image alignment processing stage that enables robust stitching results across imaging and common delayering issues. Proper alignment is critical to the performance of preceding image processing steps, and as such, requires strong scrutiny and effort for robustness sake. Traditionally, stitching algorithms are designed for natural scenes, and natural images are visually more forgiving. In comparison, circuit images have edge-based content, and less texture/color content. Circuit images have more repetitive patterns, which makes traditional stitching algorithms fail to match corresponding points in overlap regions. For example, images where single directional interconnect wires dominate, picket-fence artifacts may make the image registration difficult, and in turn, produces poor quality stitches.

III. Image Stitching and Analysis

Our approach includes several processing steps to stitch together high-resolution circuit images to form a composite mosaic. First, we enhance the contrast and brightness in the overlap regions. These local enhancements bring out the delayering noise as features in the non-circuit areas to improve image registration. For example, polishing marks from mechanical polish may be useful for alignment purposes. As shown in Figure 3, the original circuit image may be visually dark. A simple histogram equalization may not be able to enhance all of the edge information in the image. Instead, using a contrast normalization step [4,5], we can enhance all high frequency content in the image so as to provide strong feature points for stitching.

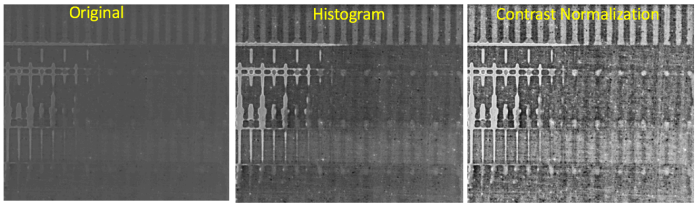

Fig. 4. Image enhancement to improve the signal-to-noise (SNR) for image alignment

Second, we extract features points from the overlap regions and finding corresponding features in the common image regions. A key novelty here is the use of sampled feature points that are distributed across the overlap regions. As shown in Figure 4, feature points are sampled across distributed tiles because (1) Repeated patterns in circuit images can fool matching points, and (2) noisy patches on key dominant can throw off ranking of features.

Specifically, in a traditional algorithm, the strongest feature points are used by first sorting the entire set of feature points in the overlap regions. However, if there are repetitive circuit structures, then it is difficult to disambiguate among the feature points. Also, if there are noisy patches (dust or artifacts introduced by chip delayering artifacts, electron discharge, then the list of feature points is skewed when considering the list as a whole.

By sampling the feature points across tiles, the algorithm enforces the need to selectively sample across the overlap regions such that there is sufficient distribution of unique feature points for comparison. The number of feature points per tile region can be set as a threshold based on noise level of the imagery or when the tile has few textures. That is, more points may be needed when the tiles have few features or are noisy. This approach is similar to stitching aerial imagery where there are occlusions and many environmental effects.

Figure 5 illustrates an example block diagram of the algorithm using the "Tile Norm ROI" approach (Figure 4). For every image overlap region, we perform the following processing steps:

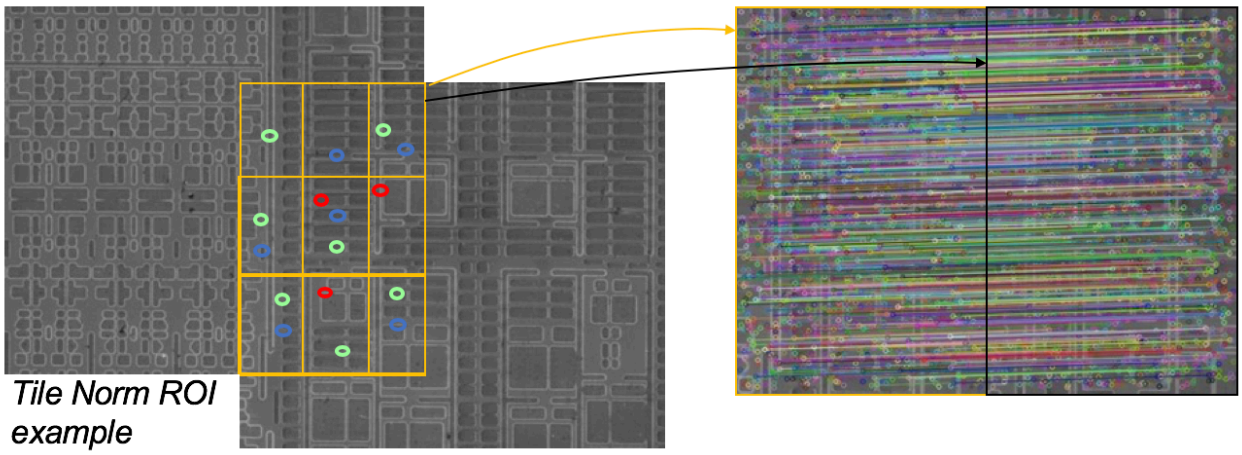

Fig. 3. Image stitching of high resolution of Multi-beam SEM images. Left side is the feature extraction per tile in the overlapped region, and right side is the matched points connected by a color line.

- Use enhanced image data to increase feature point detections.
- Detect feature points evenly across overlap using tile-normalization.
- Compute Feature Descriptors for each feature point.
- Match feature pairs. Apply symmetric match to reduce false matches.
- Apply motion and distance constraints to remove outliers
- Inlier points are used for motion estimation between SEM images.

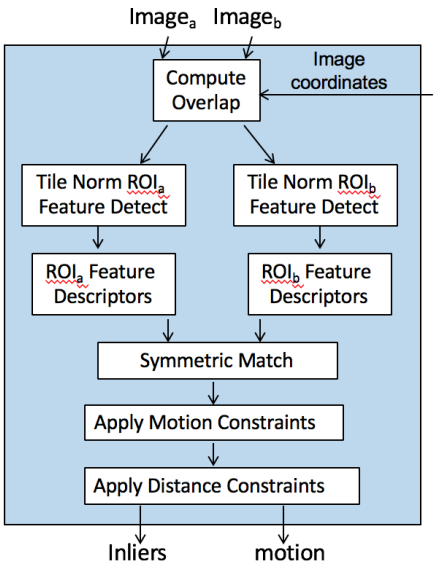

Fig. 5. Example algorithm pipeline for image stitching for chip images using tiled feature points

Note: "motion" refers to the displacement between two overlaps in translation, scale, and rotation. To address large number of seams in the composite mosaic image, we further disclose a bundle adjustment stage.

In the third stage, we finely tune the registration parameters across multiple images as a bundle to refine the final registration result. Because most of the images have more than one neighbor, and not all image registrations are correct, we use bundle adjustment (BA) to optimize the image stitching. BA can be defined as simultaneously refining the alignment results for each image. The alignment coordinate refers to the 3D vector that provides the best alignment for the overlap region. the net result of BA is the best fit adjustment based on minimizing the net error among the images. The output of BA is the new global coordinates of all images. In order to determine the global coordinates of each image, we solve the following optimization problem:

$$\underset{\vec{x}}{argmin}\left[\sum_{a,b\in overlap} w_{ab}\left(R_{ab}\vec{x}_a - \vec{x}_b - \vec{t}_{ab}\right)^2 + \beta\sum_i(\vec{x}_i - \vec{s}_i)^2\right]$$

where $\vec{x}_i$ is the coordinate of image i, and R_{ab} and $\vec{t}_{ab}$ are rotation matrix and translation vector from image a to image b. $\vec{s}_i$ is the reference coordinate (or fiducial point) for image i. These fiducial points are predetermined points as a reference to the circuits. β is the regularization parameter, which controls how much influence $\vec{s}_i$ has. w_{ab} is the weight for the motion estimate between image a and b. We use the number of matches as the weight to cast the vote in BA. The transformation with the most matches 'wins' and the change of the coordinates will be greatly influenced by that. Figure 6 is an example of mSEM bundle adjustment. Different color of circles represents the stage coordinates of images before and after BA. The reference point is the fiducial point that the mSEM image coordinates stay unchanged.

This bundle adjustment step consists of an iterative refinement of the relative motion parameters for a group of images. The first BA is the refinement of the relative motions among subfield images per mSEM. Secondly, BA is applied to a region which includes hundreds and thousands of mSEM

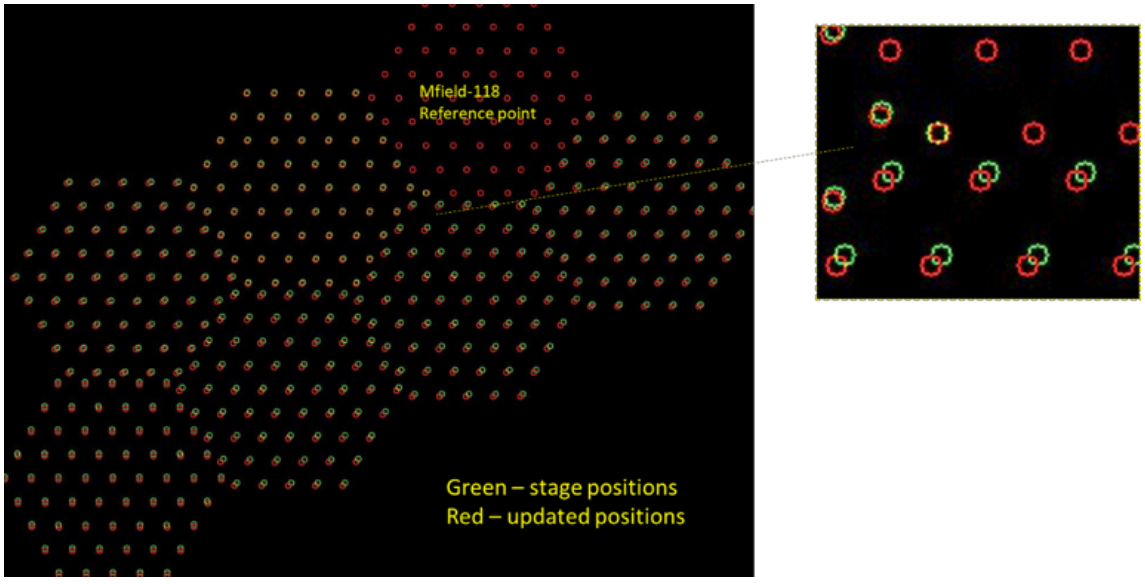

Fig. 6. mSEM bundle adjustment example. The green circle represents the stage positions of each image, and the red represents the updated positions by bundle adjustment.

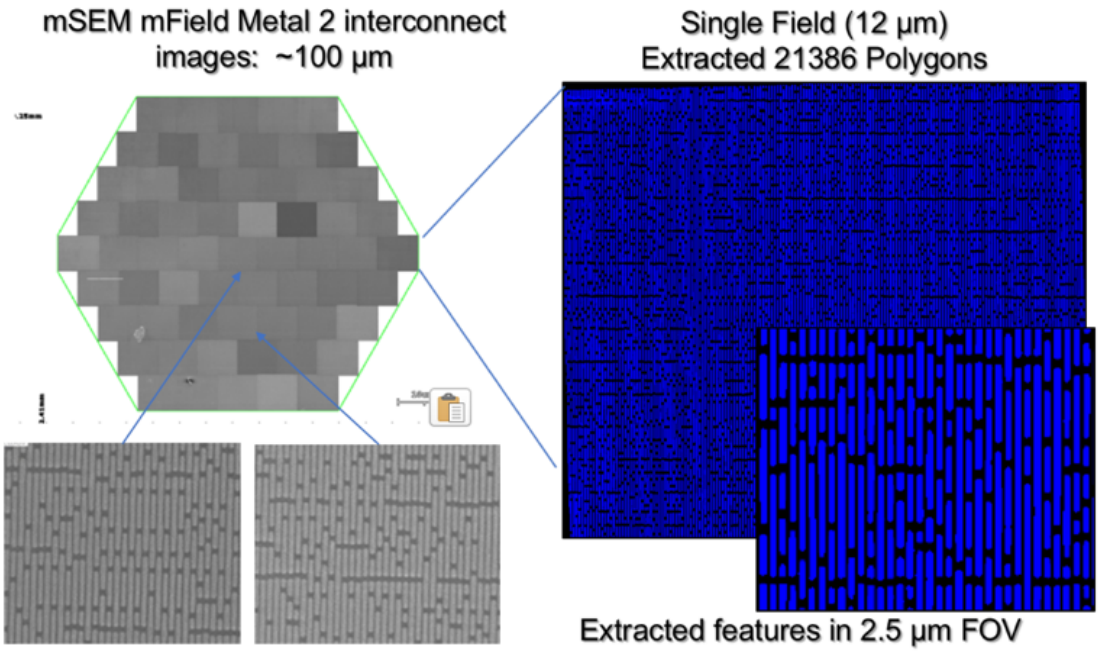

Fig. 7. Example stitched image and extracted circuit structure as polygons

images. The refinement can be extended to a physical layer or the entire layer of many physical layers.

Two problems in image stitching is worthy of discussion here. First is the overlap percentage between images. The time requirement from image capturing enforces the overlap to be small. However, calibration error, charge distortion, stage drift and positioning error may fail the image registration that few matched points be obtained.

Our solution is to extend the short side of the ROI of each image in the overlap and increase the number of matches. Second problem comes from the incorrect motion estimates between subfields across two mSEM images. The displacement between any two subfields from two mSEM images should be identical. Many of the bad alignments come from picket-fence artifacts, by which the alignment falls to a local minimum solution depending on the initial relative stage positions.

We use a majority vote approach to first segment the bad and inconsistent motions from the majority good and consistent motions. We then prewarp these images based on the majority motion and then refine the motions. In cases that bad captures happen, that motion estimates among mSEMs do not have majority vote, we will exclude these images in BA and notify the system to recapture.

IV. Results and Analysis

A. Image Processing Results

We have processed through a number of mSEM images across a number of delayered IC layers. For brevity sake, we show one example in Figure 7 with mSEM images aligned with our image processing. We also show the resulting circuit structures extracted across the chip region (e.g. metal interconnect) as polygon from the stitched images.

To improve processing speeds, image stitching is processed hierarchically. Because of the sheer number of images (e.g. 1-million single beam images for 1cm^2 die at 4nm), we recognize the need for efficient memory access. Because the algorithm analyzes image overlaps between two spatially correlated mSEM images, we programmed an indexing scheme using R-tree to index and query images in neighborhood of the image being processed. As shown in Figure 8, this in effect minimizes neighborhood search times as we scale to larger number of images.

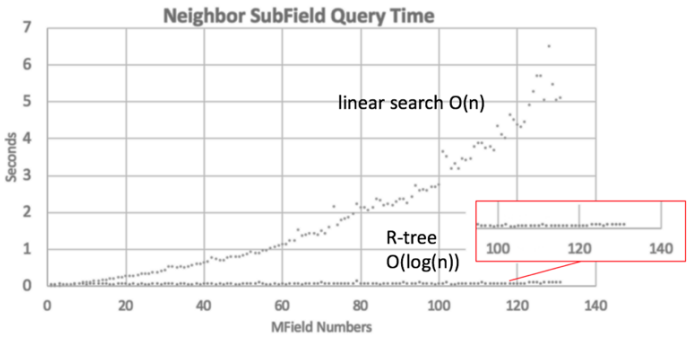

Fig. 8. Speeding up algorithm pipeline using databased indexing

B. Additional Algorithms

We also recognize the need for contextual information to improve alignment. For example, we explored the use of FFT to extract out structural based information of the circuit images. The frequency information has codified information about the dominant structure beyond what is available in the feature-based approach. This FFT analysis is done over the larger image regions instead of the overlap regions. In doing so, we can then align and stitch images based on matching frequency content of the images.

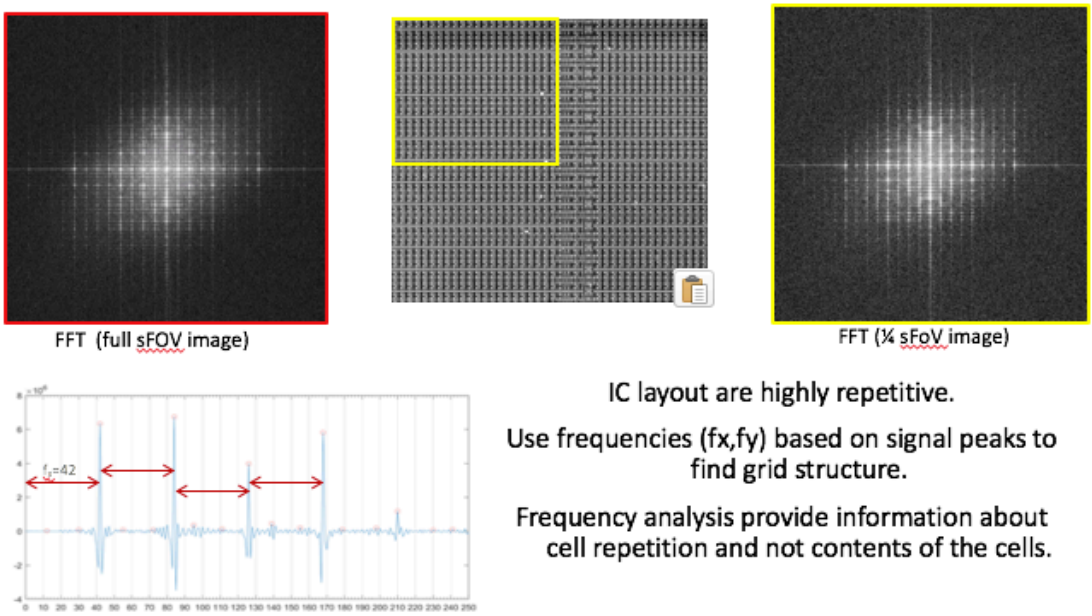

Fig. 9. Example FFT output for differently sized image regions.
We show that common structure information results in similar FFT output, which can be used for alignment.

In Figure 9, we show the 2D FFT information over a large image. If we do a similar 2D image over a smaller region of the image, we will find the same frequency signature. This is because the circuit layout is very repetitive, and circuits are often placed on a grid (for manufacturing). We can use the frequency information to line up signal peaks (e.g. along the x and y dimension) based on the grid structure. It is important to note that the frequency analysis does not include information about the contents of the circuits, but instead it provides the structural information about the circuit. In comparison to feature-based alignment, frequency-based alignment can be done at a larger global scale for lining up circuit images.

V. Conclusion

We describe a high-performance computing system (hardware and software) as companion image processing system to a multi-SEM. We focused this paper on the image alignment processing stage because there is fundamental need for robust stitching of high-resolution chip imagery to enable an integrated field-of-view of the entire chip. We describe the processing pipeline to address a number of challenges towards algorithm robustness, including low signal-to-noise and other imaging issues. We show how proper indexing can improve the search and retrieval of the design.

Even with current image processing and computer vision techniques, we acknowledge that there are more research that can be done to improve robustness. For example, we show that additional global contextual information, such as grid patterns derived from FFT analysis, can provide additional alignment markers that support registration of local cells. Additional semantic information (e.g. standard cell patterns), derived from machine learning methods, could also be used.

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