Extended Statistical Element Selection: A Calibration Method for High Resolution in Analog/RF Designs

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ABSTRACT

In this paper we propose a high resolution digital calibration method for analog/RF circuits that is an extension of the statistical element selection (SES) approach. As compared to SES, the proposed ESES method provides wider calibration range to accommodate multiple variation sources and produces higher calibration yield for the same calibration resolution target. Two types of ESES-based calibration with application in analog/RF designs are demonstrated; current source calibration and phase/delay calibration. As compared to traditional calibration methods, the proposed ESES-based calibration incurs lower circuit overhead while achieving higher calibration resolution. ESES calibration is further applied to a wideband harmonic-rejection receiver design that achieves best-in-class harmonic-rejection performance after calibration.

Keywords

Analog/RF IC design calibration, combinatorial redundancy, extended statistical element selection.

1. INTRODUCTION

As CMOS technology continues to scale, digital circuits have leveraged the corresponding technology improvements to achieve better area, speed and power. In contrast, analog circuits have scaled sub-optimally with process technology. One important limitation is transistor random mismatch in CMOS technology that degrades the analog circuit performance, specifically accuracy and yield. To combat the impact of transistor random mismatch on analog circuit performance, one method is to increase transistor size to improve matching properties [1]. However, this approach is sometimes not favored because it results in increased circuit area and decreased circuit bandwidth.

A form of sizing based on redundancy at the subcomponent level, statistical element selection (SES), was proposed in [2] to address this challenge. The SES method provides combinatorial design choices that are digitally selected, thus achieving excellent matching properties after selection. It has been shown that this combinatorial redundancy can be applied to analog designs for high resolution calibration, such as tuning input offset of a differential pair [2]. However, the calibration tuning range of SES is purely determined by transistor random mismatch, which limits the tuning range, thereby making SES unsuitable for many calibration applications.

To address this limitation and make the calibration range a design parameter, an extended statistical element selection (ESES) method is proposed here that is based on non-uniform sizing of the elements under selection. Compared to SES, ESES is shown to have wider calibration range and higher calibration resolution at the same calibration yield target.

We have applied the ESES-based high-resolution calibration method to two categories of calibration applications for analog and RF circuits, current calibration and phase/delay calibration. Our comparison of traditional calibrations methods for these applications indicates that our high-resolution digital calibration method has lower calibration circuit overhead, improved calibration resolution and flexible circuit implementation. The ESES design method was applied to a wideband RF receiver design to improve the harmonic rejection performance [3]. After ESES-based calibration, the receiver achieved best-in-class harmonic rejection ratios without extra RF front-end filtering.

The remaining sections of the paper are organized as follows. In section 2 the SES design method is reviewed and its limitations for use as a general calibration method are discussed. In section 3 we present our proposed ESES method. A study of calibration resolution and calibration range of the ESES method is also presented. Section 4 includes a number of applications for the ESES method, followed by our conclusions in section 5.

2. BACKGROUND

2.1 Statistical Element Selection

Matching properties can be improved by redundancy. A traditional method to create redundancy is to have a large population of cells to choose from. Instead of only having one cell, redundancy is based on having N cells and choosing the best one from that population. Assuming these N cells follow the same independent distribution and the success rate of each cell passing certain specifications is $P_{success}$, then the total success rate of having N cells available for selection is $1-(1-P_{success})^N$, which is significant improvement over $P_{success}$. This method was incorporated in the flash ADC design in [4] to improve ADC linearity. Although traditional redundancy can improve the yield of the analog circuit design, the cost of circuit area can be high (scales by N).

With statistical element selection (SES) that was proposed in [2], the approach is based on digitally selecting K elements from a set of N elements and sacrificing N-K elements, resulting in a combinatorial redundancy. The number of available combinations increases exponentially as N and K increase, enabling an exponential number of design choices that can be digitally selected. By having this combinatorial redundancy, the failure rate to pass certain specifications can be improved by orders of magnitude. By applying SES, Keskin et. al. lowered the standard deviation of the comparator input offset voltage by multiple orders of magnitude [2]. Therefore, the total area required to meet a specific matching criteria was lowered dramatically, thereby reducing overall area even when considering the sacrificial area that enables combinatorial redundancy. This design methodology can enable improved transistor matching at a relatively low circuit

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overhead (usually a digital controller), as demonstrated in a 14-bit current-steering D/A data converter design in [5]. The SES design method has also been regarded as an efficient design method for FinFET technologies [6] as well.

2.2 Limitations of SES

For the original SES methodology, the distribution of the combined K-element is created by the random variation of the equally-sized N elements, and a large number of combinations aggregate around the center of the design choices distribution [2]. This clustering effect creates an area of ultra-high density of combinations as available design choices for selection for the SES method, and therefore, high calibration resolution can be realized.

However, once the calibration target window deviates from the distribution center, the calibration success rate drops rapidly. This reduction is due to the decrease in the distribution density of the available design choices.

Moreover, the calibration range created by the SES method purely depends on the random variation of the individual elements. The only way to change the calibration range is to purposely change the size of the N elements, thereby changing their random variations. However, this approach is not ideal since the change in size would affect circuit performance. In short, the calibration range of the SES method cannot be set independently.

These limitations of the original SES method do not create a big problem if the equally-sized N elements are the only variation source or the strongly dominant variation source in the design. The calibrated result of the combined K-element has to cancel out the impact from other variations sources in the design. If all other variation sources are negligible, the calibration target of the combined K-element can be bounded in a very small region around the nominal design value. Also there is no need for a larger calibration range in this case to cover any outlying calibration targets. For example, a comparator design with SES-based input offset voltage calibration was shown in [2], where the input differential pair is the dominant variation source for the input offset voltage.

Once there are multiple, non-negligible variation sources or even other dominant variation sources in the design, the calibration target of the combined K-element is determined by the random variation of the other sources. The location of the calibration target can be far away from the center of the design choices distribution or simply out of the calibration range created by the random variations of the equally-sized N elements. In these cases, SES method would be less effective or even not applicable.

In summary, the original SES method has limited tuning range to counter other variation sources in the design and it is only effective if there is just one variation source in the design. Without involving another level of coarse calibration preceding the SES based calibration, it has limited application as a calibration method in systems that have multiple non-negligible sources of variation.

3. EXTENDED STATISTICAL ELEMENT SELECTION (ESES)

3.1 ESES Design Method Overview

We propose a design method called extended statistical element selection (ESES) for increasing the calibration tuning range and thus accommodating other dominant variation sources. Different from the SES design method, the ESES design method has non-uniformly-sized N elements. For example, the N elements can be sized as an arithmetic sequence. Meanwhile, the same combinatorial redundancy as the original SES method is provided by still selecting K elements out of the N elements. For this ESES method, the overall size of the combined K-element already spans a range in the nominal case without random variation considered in, and this range can be controlled by the nominal sizes of the elements as a design parameter. For example, if an arithmetic sequence is used for the elements' sizes, the distribution range in the nominal case can be controlled by the common difference of the arithmetic sequence while keeping the center value unchanged. With random variation considered, the distribution of overall size of combined K-element creates a wider calibration tuning range. This proposed ESES method will effectively trade high distribution density around the center of the design choices distribution for a wider tuning range.

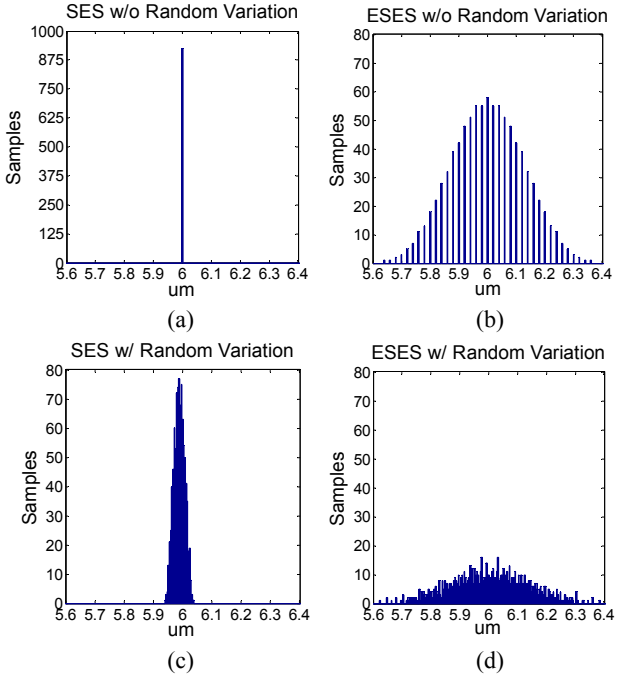

Figure 1 Design choices distributions: (a) SES method w/o random variation (b) ESES method w/o random variation (c) SES method w/ random variation (d) ESES method w/ random variation.

As an example to illustrate the wider tuning range of ESES, we apply combinatorial redundancy to transistor width calibration. The transistor under calibration is broken into multiple segments and only a subset of the segments are selected. Figure 1 shows the distributions of all available SES/ESES design choices through the combinatorial redundancy. In this example, both SES and ESES methods have parameters of N = 12 and K = 6 (selecting 6 segments out of 12 available segments) thus generating 924 available design choices. For SES, the nominal transistor width for each segment is set as 1 μm. For ESES method, nominal widths are set as an arithmetic sequence of 12 numbers centered at 1 μm and with a gap of 0.02 μm for two adjacent segments (the arithmetic sequence is 0.89 μm, 0.91 μm, …, 1.09 μm and 1.11 μm). Although there are slight nominal sizing differences, the standard deviation of all segments are set as 0.01 μm for both SES/ESES cases. The histogram bin width is fixed as 0.004 μm in Figure 1. As shown in Figure 1 (a), all design choices of SES are the same without random variation considered, thereby forming a single bin in the distribution. Figure 1 (b) shows that with ESES method, the 924 design choices create a wide distribution range even without random variation. With random variation considered, Figure 1 (c) shows that SES method creates a

relatively small calibration range, which is purely created by the segments' own random variation. However in Figure 1 (d), the ESES method creates a much wider distribution that roughly follows the shape as in Figure 1 (b), of which the shape is pre-determined by nominal transistor sizing.

3.2 ESES Calibration Resolution and Calibration Range Example

In this section we study the resolution and range of the ESES calibration method as compare with the SES method. In this example, both SES and ESES have parameters of N = 12 and K = 6. As shown in [2], different N, K settings have different calibration yield performance, calibration time (due to different sizes of searching space) and utilization ratios. A setting of N = 12 and K = 6 is picked here, but the following experiments can also be applied to different N, K settings.

For SES in this example, all elements have a nominal size of 1 μm and the standard deviation is set as 0.01 μm. Hence, the size of a combined K-element has a nominal value of 6 μm and a standard deviation of $\sqrt{6} * 0.01$ μm = 0.0245 μm. We denote this standard deviation value as σ_k and use it for normalizing the resolution and range. For ESES, the nominal sizes of the 12 elements are set as an arithmetic sequence. The average value of the arithmetic sequence is set as 1 μm. The common difference of the arithmetic sequence is denoted as d_{ESES}. The standard deviations of each element in the ESES method are calculated based on the assumption that the standard deviation of each element is proportional to the square root of its nominal size. The center value of the standard deviations of the 12 elements is also set as 0.01 μm for fair SES/ESES comparison purpose.

While performing calibration, once the overall size of the subset (the K elements that are selected) falls into a target window, the calibration process is marked as successful. The calibration target window size, denoted as T_{window}, is set in the unit of σ_k. This T_{window} value shows the calibration resolution with respect to the standard deviation of the K-element. If we assume the combination falling into the target window follows a uniform distribution, then after calibration the standard deviation of the selected subset decreases to $T_{window}/\sqrt{12}$.

The location of the center of the target window is described by its offset from the nominal design value (in this example, nominal design value is 6 μm). This offset of the center of the target window is denoted as T_{offset}. This value is also in the unit of σ_k, and it shows how far away the calibration target is from the nominal design value.

3.2.1 Ideal Calibration Target

We first study the trade-off between calibration success rate and calibration target window size when the calibration target is right at the nominal design value (T_{offset} = 0). This is the most ideal case. For the ESES method, a set of different values for common difference of the arithmetic sequence are analyzed, which are $d_{ESES} = \sigma_k/4$, $\sigma_k/2$, σ_k and $2\sigma_k$. The target window size T_{window} varies from $\sigma_k/100$ to $\sigma_k/5$ in this experiment. For each different SES/ESES setting and target window size, we run the Monte Carlo simulation with 10^5 samples. Figure 2 shows the relationship between calibration failure rate and calibration target window size. In order to have a closer look at the region where success rate is very close to 100%, failure rate in log scale are shown in this figure.

From Figure 2 we can see that the SES method shows an advantage over the ESES method in terms of lower calibration failure rate when the calibration target window size T_{window} is set as minimum. As T_{window} increases the failure rate of the ESES method improves much faster than that of the SES method. In particular, in the region where the calibration failure rate is lower than 10%, the ESES method provides a significantly higher calibration yield than the SES method. This means the ESES method outperforms the SES method even for the most ideal case of the calibration target.

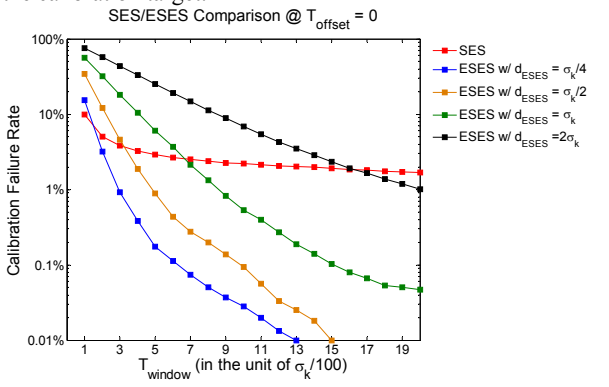

Figure 2 SES/ESES calibration failure rate vs. calibration target window when $T_{offset} = 0$.

The inefficiency of the SES method when the calibration target is right at the nominal design value can be explained as follows. Although SES provides more design choices than ESES at the center of the design choice distributions (Figure 1 (c) and (d)), which supposedly translate to higher calibration yield for the SES method at that region, the center of the design choices distribution is not the calibration target for $T_{offset} = 0$. The calibration target is a constant when $T_{offset} = 0$, which is exactly 6 μm in this example. Meanwhile the center of the design choices distribution is a random variable. It is determined by the sizes of the N elements that are available in each sample. Therefore, statistically, the center of the design choices distribution of the SES method can be far away from the nominal design value. And because SES has a very sharp distribution, as shown in Figure 1 (c), the misalignment between the center of the design-choices distribution and the nominal design value can result in a very small number of design choices at the nominal design value. Meanwhile for the ESES method, as the design choices have a much wider distribution, the misalignment between the center of the design choices and the nominal design value has less impact on the design choices density at the nominal design value. Therefore, although SES has more design choices around the center of the design choices distribution, it does not translate to a higher calibration yield as compared to ESES when the calibration target is the nominal design value.

3.2.2 Random Calibration Target

In a more realistic calibration scenario, the deviation of the calibration target from the nominal design value is determined by the random variations of other variation sources in the design. Therefore, in the next experiment we assume T_{offset} is a random number that follows a normal distribution $N(0, \sigma_T)$, where σ_T shows the total variation coming from the other variation sources in the design. Before calibration, overall standard deviation in the design, denoted as σ_{All}, can be calculated as $\sigma_{All} = \sqrt{(\sigma_k^2 + \sigma_T^2)}$. As aforementioned, after successfully performing calibration, the standard deviation can be reduced to $T_{window}/\sqrt{12}$ as the calibrated values are all bounded in a small calibration window. To quantify the benefit of the calibration method, we further define the ratio of σ_{All} and $T_{window}/\sqrt{12}$, denoted as R_{cal}, as the standard deviation reduction factor of the calibration method. For the following experiments, σ_T is set as $\sigma_k/4$ and $2\sigma_k$. The two values correspond

to two scenarios: other variation sources in the design are negligible or dominant as compared to the variations of the N-element undergoing SES/ESES based calibration process. Figure 3 and Figure 4 show the calibration failure rate vs. calibration target window size for the two scenarios respectively.

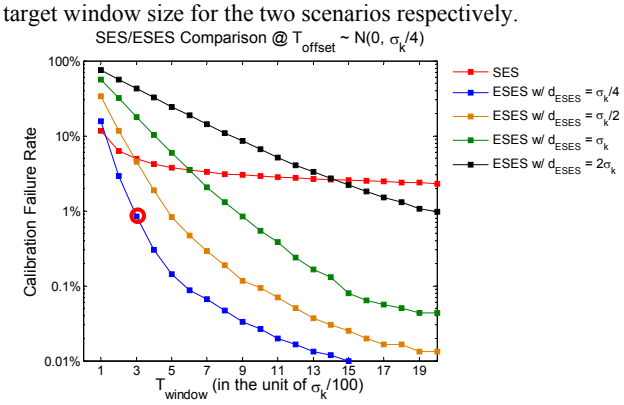

Figure 3 SES/ESES calibration failure rate vs. calibration target window when T_{offset} ~ N(0, σ_k/4).

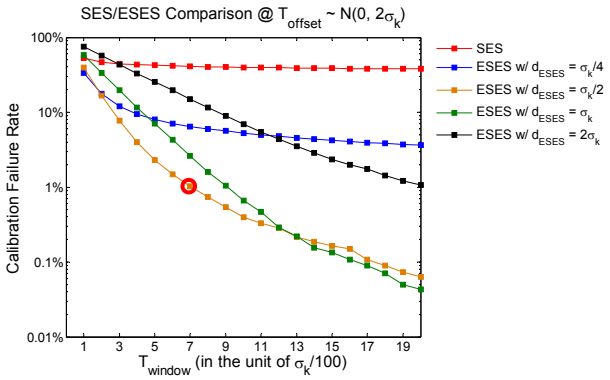

Figure 4 SES/ESES calibration failure rate vs. calibration target window when T_{offset} ~N(0, 2σ_k).

In Figure 3, where the other variation sources in the design are negligible, the calibration failure rate of the SES method is much higher than 1%. However, for the ESES method, calibration failure rate can be much lower than 1% depending on the value of calibration target window. For example, for T_{window} = 3σ_k/100, which corresponds to a standard deviation reduction factor R_{cal} of 115, the calibration failure rate is less than 1% with d_{ESES} = σ_k/4 for ESES method.

In Figure 4, where σ_T increases to 2σ_k such that other variation sources become dominant to the N-element, the SES method can no longer perform calibration effectively. On the other hand, the ESES method still exhibits very low calibration failure rate for certain calibration windows. For example, if we still target at a calibration failure rate less than 1%, we can obtain a R_{cal} of 111 when d_{ESES} = σ_k/2 and T_{window} = 7σ_k/100.

The above experiments show that the ESES method is effective to perform calibration with more than 99% calibration success rate while potentially achieving a standard deviation reduction factor of around 100. This also means that the matching property after calibration is improved by approximately 40 dB. These experiments also show that in both cases, whether other variation sources are negligible or non-negligible, the ESES method outperforms the SES method by having higher calibration yield while targeting at same calibration resolution.

While R_{cal} shows the matching improvement the ESES method can provide, σ_T (in the unit of σ_k) shows the amount of variations from other variation sources that the ESES method can handle. A higher σ_T value means the ESES method needs to provide a larger calibration range to cover the overall variations. In the following experiment, we further study how much matching improvement we can achieve while we keep increasing σ_T.

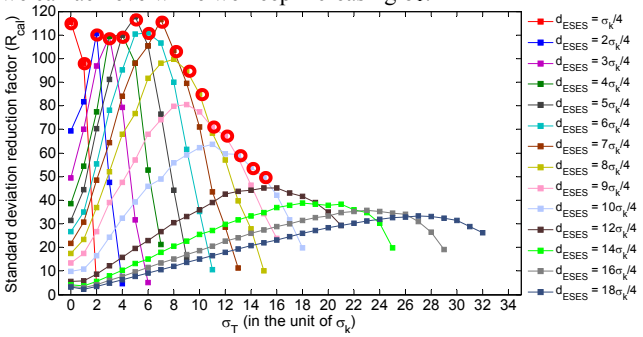

Figure 5 R_{cal} vs. σ_T for the ESES method.

Assuming our calibration yield target is greater than 99%, Figure 5 shows the relationship between standard deviation reduction factor R_{cal} and σ_T (in the unit of σ_k). As we can see from the figure, different d_{ESES} settings are needed to achieve optimal R_{cal} at different σ_T values. The ESES method can achieve an R_{cal} value around 100 when σ_T is no greater than 9σ_k. As σ_T keeps increasing, the achievable R_{cal} value decreases. In order to obtain an R_{cal} value greater than 50, σ_T can be as large as 15σ_k. In both aforementioned R_{cal} targets, the allowable σ_T value can be almost one order of magnitude larger than σ_k. These numbers show that even the variations from other sources are much larger than those of the N-element, we can achieve very large matching property improvement by using the ESES method, which leads to high-resolution calibration results. For comparison, with the same calibration yield target, an ideal 7-bit digital calibration without missing calibration codes can achieve a standard deviation reduction factor, R_{cal}, of up to 85.

For the ESES method, all of the previous simulation results are obtained by setting the average value of the elements to be 1 μm and the center value of the standard deviation of the elements to be 0.01 μm. This results in a relative standard deviation for each element to be about 1% before calibration. To validate generality of the aforementioned results, we repeated the experiments by setting the relative standard deviation of each element to be around 2%, 4%, 8% and 16% respectively and we obtained similar results as previously shown.

To summarize the results of the experiments in this section, by using the proposed ESES method we can utilize combinatorial redundancy in a non-dominant variation source to calibrate the dominant variations in the design and still achieve large improvement for the matching property. This proposed calibration method extends the usage of combinatorial redundancy for general high-resolution calibration applications. As the calibration location no longer has to be the dominant variation source, it provides the flexibility of choosing a suitable location in the design for applying combinatorial redundancy.

4. ESES APPLICATIONS IN ANALOG/RF DESIGN

4.1 Current Calibration

Traditionally, current calibration can be done by varying the bias voltage of the current source [7]. By adding a serial resistor to the gate of the current source and supplying a small tunable current flowing through that resistor, the effective biasing gate voltage of the current source can be tunable. The major overhead

of this method is the calibration DAC (CALDAC) and associated current mirror structure that can require significant area.

More directly, current adjustment can be done by adding a small tunable current source in parallel to the current source under calibration. One method is to tune the gate voltage of the added current source and use a capacitor to store the calibrated gate voltage value for use during normal operation [8]. This method can share the CALDAC among all current sources under calibration. However, the resulting calibration schemes for this method involve high analog circuit overhead, which also suffers with process scaling. Another method is to attach the CALDAC current output directly in parallel for each of the current source under calibration [9]. For high calibration accuracy, a very small current cell of least significant bit (LSB) of the CALDAC is needed for a small calibration step, which typically leads to a LSB current cell design with much larger channel length than that of the current source under calibration. As a result, the area overhead for the CALDACs is observed to be high [9].

The proposed combinatorial-redundancy-based ESES method can be applied to current calibration to achieve high calibration resolution with more than one order of magnitude matching improvement with minimal circuit overhead. Consider the conceptual circuit shown in Figure 6. The current source under calibration is split into N non-uniformly sized sub-current sources, with each one controlled by a switch and only K of the N sub-current sources are activated. During calibration, different K subsets can be tested in order to find the optimal selection from the built-in combinatorial redundancy. The number of available combinations increases exponentially as N and K increase, providing a large number of calibration choices and enabling high calibration resolution. The applied ESES method provides higher calibration range as compared to SES method to accommodate extra variation sources if any. Even in the case when other variation sources are all negligible in the design, ESES can provide higher calibration success rate, as shown in Figure 3.

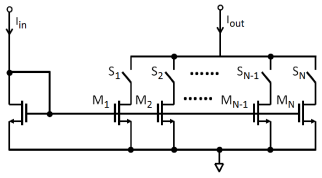

Figure 6 ESES-based current calibration conceptual circuit.

In contrast to traditional current calibration, the ESES-based high-resolution current-calibration method does not involve the overhead of a CALDAC. Other than the digital control circuit, the major overhead of this method is the sacrificed circuit area of N-K unselected sub-current sources. However, as pointed out in [2], the combinatorial redundancy dramatically relaxes the area requirement for achieving certain CMOS matching properties. As a result, even considering the sacrificial area, the total area for current source can be reduced significantly (as compared with traditional sizing) when meeting the high matching requirement.

There are various applications for the ESES-based high resolution current calibration method. One direct application for current source calibration is segmented current-steering D/A data converter, where the current matching for the thermometer-coded bits is critical for achieving good D/A linearity. The ESES-based high resolution current calibration method can be applied to the MSBs unary current sources to optimize matching properties. Another application is calibration of the transconductance of differential amplifiers. The tail current source of the differential amplifier can be split into several sub-current sources to create combinatorial redundancy. As the transconductance of the differential pair is a function of the DC bias current, by tuning the bias current, the transconductance can be effectively calibrated.

4.2 Phase/Delay Calibration

Phase/delay matching also suffers from transistor random mismatch. Most of the phase/delay calibration methods utilize one of the two existing tuning mechanisms for the delay element: a current-starved inverter [10] and a shunt-capacitor inverter [11]. These techniques were proposed originally for digital delay-locked loops or digital phase-locked loops designed with a large tuning range. However, these techniques can also be modified to have finer tuning resolution and thus find application in analog/RF designs where high timing requirements are needed for digital signals. For both tuning mechanisms, if an analog control scheme is employed, it comes with heavy circuit overhead for generating the analog control voltage and, if digital control scheme is employed, the calibration resolution is limited by the LSB of the tuning elements.

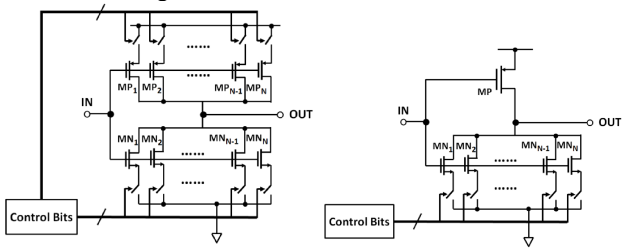

Figure 7 ESES-based phase/delay calibration conceptual circuit: (a) tunable rising and falling edge; (a) tunable falling edge only.

The ESES design method can also be applied to phase/delay calibration for high calibration resolution. Refer to the conceptual circuit is shown in Figure 7, the idea is to break the NMOS and PMOS transistors into N elements, and select a subset of them by adding big switches at their drain nodes (to minimize "on" resistance of the switch). The ESES design method with wider tuning range is suitable for phase/delay calibration since a chain of logic gates is usually involved in the design and the delay variation generally not only comes from a single stage. By using the ESES method, calibration performed in one inverter stage can potentially cover the delay variations from the entire logic chain.

Different from most of the existing phase/delay calibration methods, the circuit shown in Figure 7 (a) has the capability of tuning the rising/falling edge of the inverter output independently. If only one edge is needed for calibration, e.g. falling edge, the circuit can be simplified, as shown in Figure 7 (b).

This ESES-based phase/delay calibration can be applied to various circuit designs. The delay of asynchronous signals can be calibrated using this calibration technique. One application for analog/RF design is the calibration of a pair of differential clocks. As shown in Figure 8 (a), a pair of differential clocks CLK_IN_P and CLK_IN_N pass through a pair of tunable inverters. By calibrating both rising edges and falling edges, the even-order harmonics for the differential output can be minimized. This can improve even-order distortions for analog/RF design driven by the differential clock. Another application, as shown in Figure 8 (b), is for calibrating synchronized signals. Assume that the latch is transparent when clock is high and there is no switching activity of D when clock is high. The clock signal is passed through a tunable inverter to calibrate the rising edge for the latch's clock input, hence calibrating the transitioning timing of output signal.

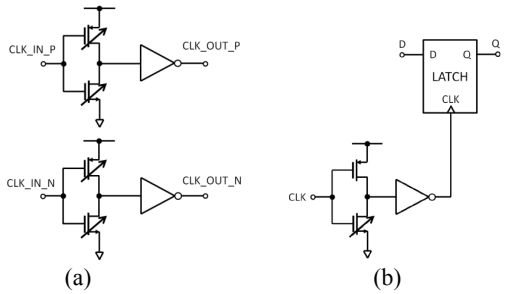

Figure 8 Conceptual circuits for high resolution phase/delay calibration applications: (a) differential signals calibration; (b) delay calibration of synchronous signals.

4.3 Circuit Design Example

For a circuit design example, a harmonic rejection receiver was presented in [3]. The harmonic-rejection scheme proposed in [12] can be applied to a wideband receiver design for rejecting interferences at local oscillator (LO)'s harmonic frequencies. However, the achieved harmonic-rejection ratio (HRR) highly depends on gain matching and phase matching. To achieve more than 80 dB HRR, simulation shows that the gain error needs to be less than 0.05% and phase error needs to be less than 0.01° (28 fs at 1 GHz).

The ESES calibration method is applied to a wideband harmonic rejection receiver design to improve HRR [3]. A circuit diagram of the harmonic rejection receiver is shown in Figure 9. Both gain errors and phase errors are coming from multiple sources in this design. For example, gain errors originate from transconductance (G_m) gain stages, transimpedance amplifiers (TIAs) and weighting resistors. The ESES method is effective in this implementation by conducting high-resolution calibration at a single variation source while covering all other variation sources in the design.

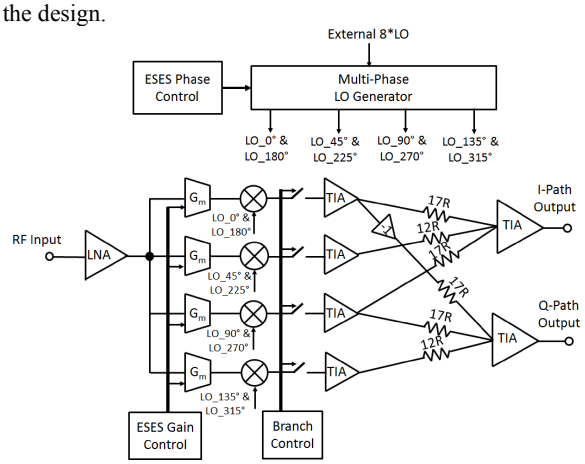

Figure 9 Harmonic rejection receiver architecture with ESES-based calibration.

To calibrate the gain errors among the multiple branches in Figure 9, ESES-based G_m calibration as discussed in section 4.1 was applied on the G_m gain stages. To calibrate the phase errors that degrade even order HRR, ESES-based differential clocks calibration presented in section 4.2 was applied on the differential outputs of the multi-phase LO generator. Similarly, to calibrate the phase errors that cause problems for odd order HRR, ESES-based synchronous signals calibration was applied within the multi-phase LO generator. More details of this design can be found in [3].

Before calibration, 2nd order HRR is around 60 dB and 3rd order HRR is around 50 dB. After ESES-based high-resolution calibration, measurement results show that they are all improved to above 80 dB, which is best-in-class performance [3].

5. CONCLUSIONS

A new calibration method for analog/RF designs called extended statistical element selection (ESES), is described in this paper. By having non-uniformly sized elements under selection during calibration process, the ESES method provides wider calibration range as compared to the original SES method such that it is capable of performing calibration in the designs where there exist multiple variation sources. The ESES method also results in higher calibration yield while having the same calibration resolution target as compared to the SES method. With the proposed ESES method, high calibration resolution in analog/RF designs can be achieved through combinatorial redundancy at the cost of very little analog circuit overhead and a digital controller.

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7. REFERENCES

[1] Pelgrom, M. J. M., Tuinhout, H. P., and Vertregt, M., Transistor matching in analog CMOS applications, *IEDM, Technical Digest,* pp. 915-918, Dec. 1998.

[2] Keskin, G., Proesel, J., and Pileggi, L., Statistical modeling and post manufacturing configuration for scaled analog CMOS, *IEEE CICC,* pp. 1-4, Sep. 2010.

[3] Liu, R., Pileggi, L., and Weldon, J. A., A Wideband RF receiver with >80 dB harmonic rejection ratio, *IEEE CICC*, pp. 1-4, Sep. 2014.

[4] Donovan, C., and Flynn, M., A "Digital" 6-bit ADC in 0.25 um CMOS, *IEEE JSSC,* vol. 37, no. 3, pp. 432-437, Mar. 2002.

[5] Liu, R., and Pileggi, L., Low-Overhead Self-Healing Methodology for Current Matching in Current-Steering DAC, *IEEE TCAS II,* vol. 62, no. 7, pp. 615-655, 2015.

[6] Vaidyanathan, K., et al,. Exploiting sub-20-nm complementary metal-oxide semiconductor technology challenges to design affordable systems-on-chip, *SPIE J. Micro/Nanolithography, MEMS, and MOEMS,* vol. 14, no. 1, p. 011007, Jan. 2015.

[7] Tiilikainen, M. P., A 14-bit 1.8-V 20-mW 1-mm2 CMOS DAC, *IEEE JSSC*, pp. 1144-1147, Jul. 2001.

[8] Bugeja, A. R., and Song, B.-S., A self-trimming 14 b 100 MSample/s CMOS DAC," *IEEE ISSCC,* pp. 44-45, 2000.

[9] Schofield, W., et al., A 16b 400MS/s DAC with <-80dBc IMD to 300MHz and <-160dBm/Hz noise power spectral density, *IEEE ISSCC,* pp. 126-127, 2003.

[10] Maymandi-Nejad, M., and Sachdev, M., A Monotonic Digitally Controlled Delay Element, *IEEE JSSC*, vol. 40, no. 11, pp. 2212-2219, Nov. 2005.

[11] Andreani, P., et al., A Digitally Controlled Shunt Capacitor CMOS Delay Line, *Analog Circutis and Signal Processing, Kluwer Academic Publishers*, vol. 18, pp. 89-96, 1999.

[12] Weldon, J., et al., A 1.75-GHz Highly Integrated Narrow-Band CMOS Transmitter with Harmonic-Rejection Mixers, *IEEE JSSC,* vol. 36, no. 12, pp. 2003-2015, Dec. 2001.