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Adverse effects of low density silicon dioxide deposited via plasma enhanced chemical vapor deposition for silicon photonic applications

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ADMINISTRATIVE INFORMATION

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1. INTRODUCTION

1.1 OVERVIEW

This technical document details results of a study into possible applications to networks using Silicon photonics. Silicon photonics denotes photonic technology based on silicon chips, exploiting optical properties of group-IV semiconductors and the design and fabrication of devices for generating, manipulating and detecting light. Silicon is usually patterned with sub-micrometer precision, into a variety of nanophotonic components. In particular, this study explored the density of silicon dioxide deposited through Plasma Enhanced Chemical Vapor Deposition (PECVD) and the resulting device performance.

1.2 SILICON PHOTONICS ADVANTAGES WHEN COMBINED WITH WDM

Silicon photonics allows for high density component integration on a single chip and it brings promise for low-loss, high-bandwidth data processing in modern computing systems. The technology combined with Wavelength Division Multiplexing (WDM) systems portends a future generation of 100+ Gbit/s networks. This is important because combining WDM with Silicon photonics makes the 100+ Gbit/s networks more cost effective than 10 Gbit/s and 40 Gbit/s networks. WDM enables multiple channel data transmission in a single fiber-optic link and can dramatically increase the aggregate data rate [1]. One of the key advantages of silicon photonics lies in leveraging standard CMOS manufacturing equipment enabling high volume production in addition to the feasibility of monolithically integrating most of the electronic-photonic components on a single chip. This significantly reduces assembly processes, which can drastically reduce component sizes [1].

1.3 SILICON PHOTONICS BACKGROUND AND LEGACY USE

Silicon Dioxide (SiO_2) is a commonly used material with applications in photonics and microelectronics. It's used in optical fibers due to its low absorption of light and by virtue of its excellent electrical insulation properties, it functions to protect silicon, block current and store charge in electrical applications. In silicon photonics, SiO_2 is typically used as a cladding material surrounding a silicon waveguide core, but it has been explored for optical cavities [2], and slot waveguides. Typical methods of SiO_2 deposition include Chemical Vapor Deposition (CVD) processes such as low pressure (LPCVD), Plasma Enhanced (PECVD), microwave plasma (MPCVD), or thermal oxidation [3]. Of these methods, PECVD systems have entrenched their place in the electronics sector because of their flexibility in depositing many thin films such as SiN, SiO, SiO_2, SiON, DLC, A-Si and poly-Si for integrated circuit applications. In the PECVD process homogenous gas phase reactions are initiated by neutral collisions with the non-equilibrium energetic electrons produced by RF plasma instead of thermal energy. Thus the deposition precursors can be produced at much lower temperatures by these homogenous reactions [4, 5], resulting in high quality films grown at 300° C to 350° C, while CVD requires temperatures in the range of 650° C to 850° C. This attribute is what makes PECVD widely employed in the semiconductor industry for overlaying thin films on temperature sensitive structures; it is also commonly used for silicon photonic applications [6–9]. However, lower deposition temperatures and higher ratios of N_2O/SiO_2 lead to less dense films, poorer step coverage and faster etch rates [10, 11].

PECVD oxides produced at lower temperatures are significantly more porous than those deposited at higher temperatures [12]. For silicon photonic applications, this combined with less than optimal step coverage and inhomogeneous coverage of 3D nanostructures [13], results in areas of lower density SiO_2 in the vicinity of silicon strip waveguides. Consequently, this material nonuniformity has been overlooked thus far in the Si nanophotonics community, especially when it pertains to

resonant structures, where an accurate cladding index distribution determines the resonant wavelength. This material nonuniformity can be a significant factor behind the discrepancy of numerical and experimental results. As an effort for accurate Si nanophotonics design, in this manuscript, SiO_2 cladding uniformity is characterized around silicon waveguides. The effect of low density SiO_2 on device performance is experimentally calculated and calibration guidance is provided for future designs involving PECVD and the Silicon on Insulator (SOI) platform. Ring resonators are used to demonstrate the deviations in device performance as these structures are key constituents of silicon photonics promising applications to modulators, amplifiers and lasers, wavelength converters, switches and Wavelength-Division Multiplexing (WDM) filters [14], in addition to possessing an excellent sensing capacity.

2. BACKGROUND

2.1 OVERVIEW

This section provides examples of the structure of chip scale components consisting of silicon waveguides clad in silicon dioxide (Figure 1). In particular, areas where lower density SiO_2 is found as a result of PECVD deposition, is denoted in the schematic. Figures 2 and 3 show scanning electron beam microscopy (SEM) images of the devices.

2.1.1 Silicon Photonics Layer Breakdown

Figure 1 illustrates the model concept of low density (LD) SiO_2 around silicon waveguides on an SOI wafer. The image depicts a typical SOI wafer consisting of a silicon handle, a buried oxide layer (BOX) and a silicon structure on top (shown as blue). The Si waveguide structure is obtained by using electron beam lithography and dry etching. Then, the silicon waveguide is covered by a SiO_2 cladding layer using PECVD (shown as light cyan). The graphic depicts two regions of PECVD SiO_2, where the region immediately adjacent to the Si waveguide is of lower density as compared to the region farther back.

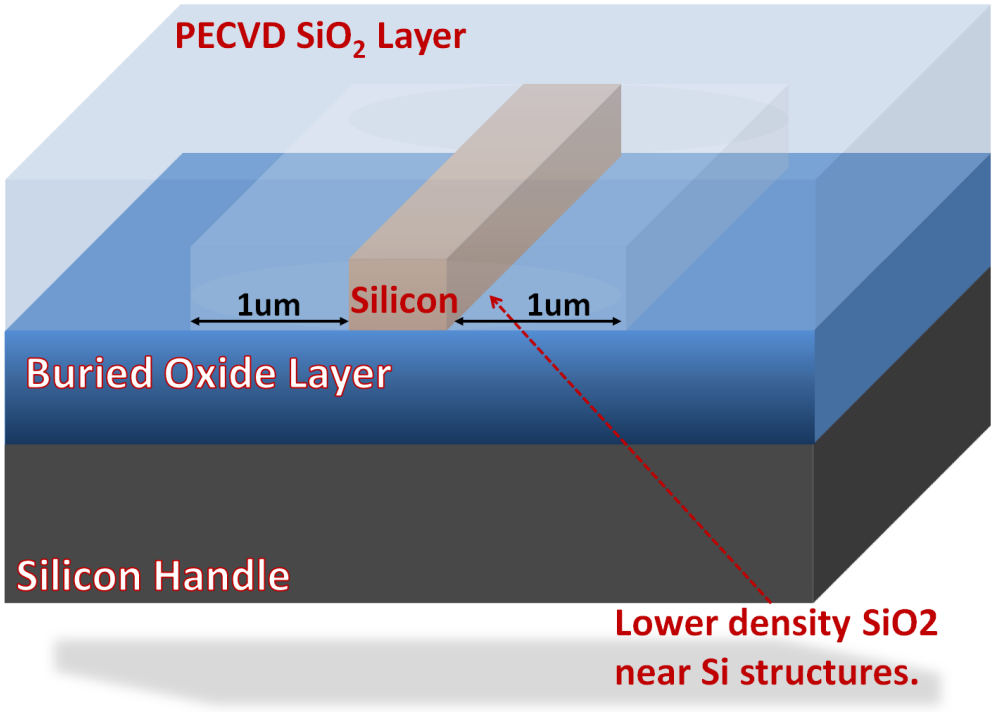

Figure 1. Graphic depicting silicon dioxide deposited with the PECVD method showing low density areas surrounding silicon strip structures. These LD areas extend out ~1 µm on each side of the silicon strip.

2.1.2 PECVD SiO_2 Covered Silicon Waveguides Detail

Figure 2 contains SEM images of PECVD SiO_2 covered silicon waveguides. The sample is composed of a Si handle, 3 µm of a buried oxide layer, silicon (already patterned) and PECVD SiO_2.

The following details the quadrant focus of Figure 2 showing the PECVD SiO_2 silicon waveguides: Figure 2 is broken down into two parts I and II. Part I shows the figure uncolored. Part II shows the figure colorized. The Figure 2, II enhanced colorized version makes it easy to see the correlation of objects in the four views relationship to each other.

(A) Two silicon waveguides at the edge of the chip (shown as blue over purple PECVD SiO_2 in Figure 2, II). The black dotted line on Figures 2 for both I and II versions represents a demarcation point between the silicon handle and oxide layers.

(B) A more zoomed in image of the waveguide appearing on the left hand side of (A). In this image, a difference between the two SiO_2 layers can be seen. The waveguide is shown as blue in Figure 2, II in all quadrants.

(C) The waveguide image appearing in (B), zoomed in even more. The silicon waveguide is visible (shown in blue on Figure 2, II, in all 4 quadrants).

(D) A close up of the silicon waveguide surrounded by BOX and PECVD SiO_2. The dome area is 2.5 µm wide.

I – Uncolored Source

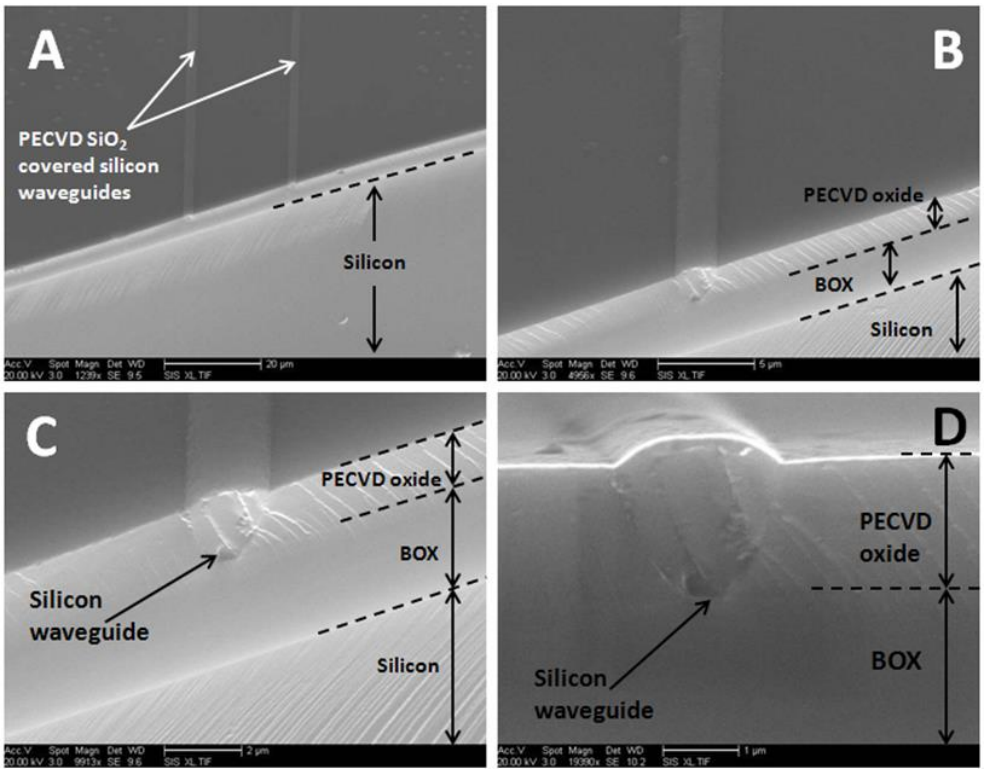

Figure 2. SEM images of PECVD SiO_2 covered silicon waveguides. Part I, uncolored version. The sample composition is silicon handle, 3 µm of a buried oxide layer, silicon (already patterned) and PECVD SiO_2.

II – Enhanced colorized version

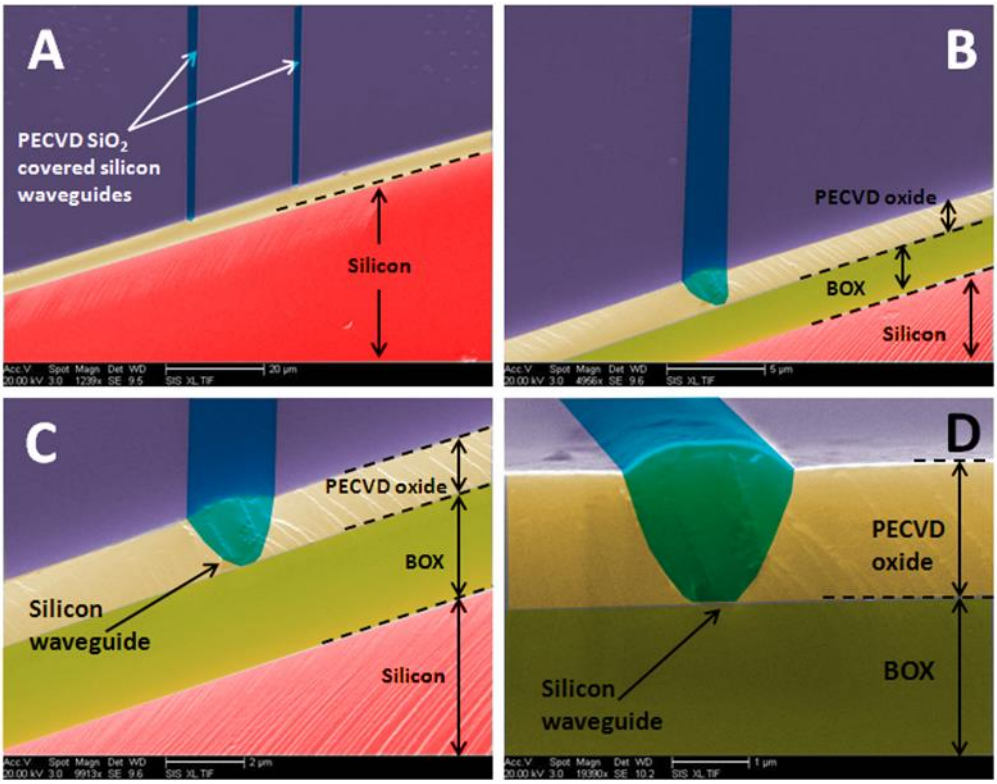

Figure Color Legend:
Purple - PECVD SiO_2 covered silicon waveguides
Gold – PECVD oxide
Lime Green – Box
Red – Silicon
Blue overlay – Silicon Waveguide, you can see the waveguide shown in four different views

Figure 2. SEM images of PECVD SiO_2 covered silicon waveguides. Part II enhanced color version. (Continued)

2.2 FABRICATION PROCESS STEPS

Samples were fabricated using a 680 µm thick silicon on insulator (SOI) wafer composed of a silicon handle, a 3µm buried oxide (BOX) layer and 250 nm of silicon placed on top of the BOX. The 3 µm SiO_2 layer aids in preventing the evanescent field of the optical mode from penetrating the silicon substrate below. Dow Corning Fox-16 electron beam (e-beam) resist was spun on the sample, ensuing in a 180 nm thick coat [15]. A hot plate bake step aided in removing the solvent. The samples were patterned with a Vistec EBPG 5200 e-beam system. Dry etch of silicon was performed using Oxford Plasmalab 100 RIE/ICP. PECVD (Oxford Plasmalab 80 Plus) was utilized to grow an 1800 nm SiO_2 cladding layer. The PECVD system was operated at 350° C with a mixture of 5% SiH_4 and 95% N_2 at 117 sccm with 710 sccm of N_2O, resulting in an average deposition rate of 72 nm/minute. The PECVD chamber pressure was 1000mT and the RF power was 20W at 13.56 MHz.

To demonstrate the low density model depicted in Figure 1, the sample was wet etched in SiO_2 etchant (Baker buffered oxide solution (BOE) with 33.5% NH_4, 7% HF, and 59.5% H_2O) for a duration of 195 seconds. SEM images of multiple devices during various fabrication process steps appear in Figure 3.

A detail of what is shown in the 4 quadrants of Figure 3 is shown in the following list:

(A) Shows unclad silicon waveguides situated on top of a buried oxide layer and prior to PECVD deposition. The ring shown is positioned on top of a buried oxide layer and prior to PECVD deposition.

(B) Depicts the sample edge showing a silicon waveguide clad in PECVD SiO_2. This image was taken at a 45-degree angle. Sample edge shows a silicon waveguide clad in PECVD deposited SiO_2.

(C) Shows the sample post wet-etch at the edge of the patterned window. There are two coupled Si waveguides partially clad in SiO_2. The etched area shows marked by a dashed red line shows a trench surrounding the silicon waveguides. The etched area, also shows a deeper trench in the vicinity of the silicon waveguides. This trench is formed due to SiO_2 near the waveguides etching at a faster rate. It can also be seen from the image that the BOE etchant has etched areas around the waveguides underneath the window of the remaining SiO_2 layer.

(D) Shows a ring resonator and two bus waveguides in the patterned area. The trench surrounding the Si waveguides is more visible in this image. The sample post wet-etch shows the exposed ring regions and a trench of fully etched SiO_2 close to the silicon structures. The etching window is marked by the dashed red lines.

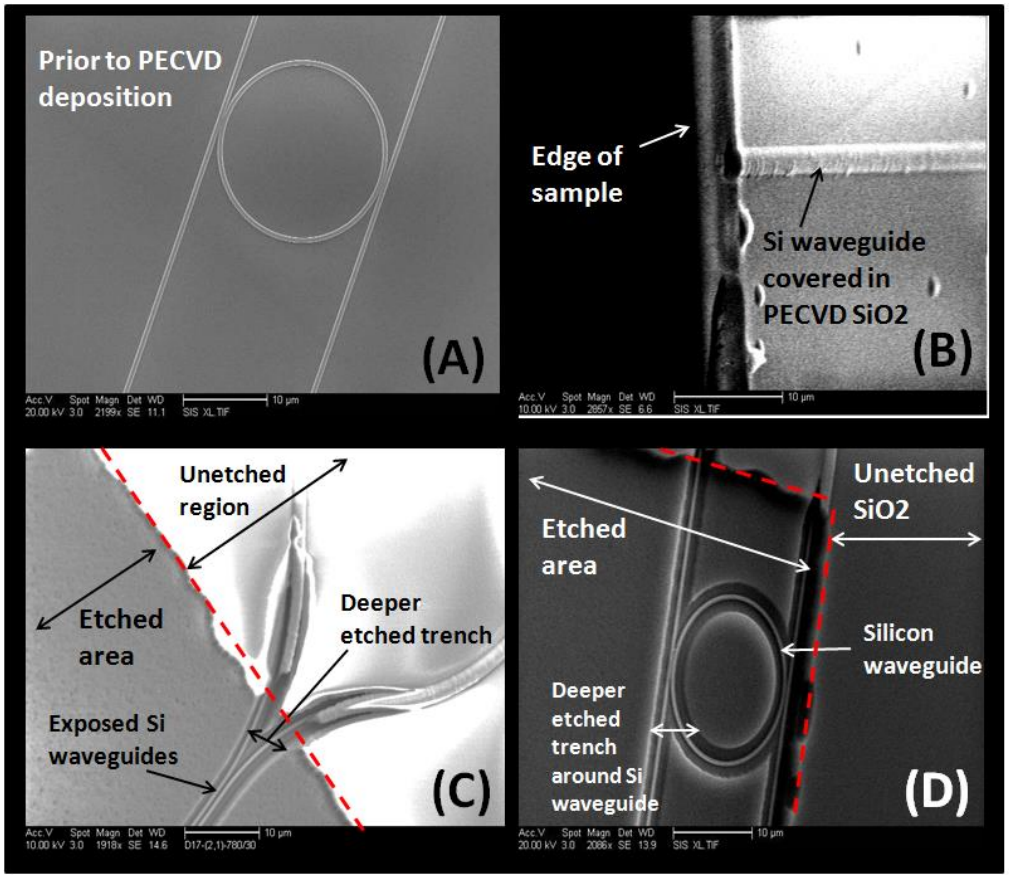

Figure 3. SEM images of multiple devices during various fabrication process steps.

3. LOW DENSITY PECVD SiO_2 ANALYSIS

The analysis below shows that (1) the width of the low density areas extends out 1µm from each edge of a Si structure, (2) the size of the LD area does not depend on the width of the Si structure, and (3) unetched silicon dioxide forms a narrow ridge when two silicon strips are approximately 2µm apart. Figure 4 presents SEM images of several silicon structures post the wet etch step. Typically, the HF etch rate is a good measure of the film's density [16]. It can be seen that only the regions immediately surrounding the silicon shapes show fully etched SiO_2 and these regions extend ~1µm from the outer boundary of the silicon form. The numbers in the figure denote particular regions and aid in identifying their measured width values. From the figure, it can be deduced that the effect is not geometry dependent and that it manifests itself regardless of the silicon structure shape.

A detail of what is shown in the 4 quadrants of Figure 4 is shown in the following list:

(A) Shows a coupling section between a ring resonator and bus waveguide. Arrow (1) points to a straight silicon waveguide with a measured width of 470 nm, arrow (2) marks a silicon ring structure of 475 nm width. The gap between a silicon waveguide and under etched SiO_2 is 910 nm wide and denoted by arrow (3). Arrow (4) shows a 912nm gap between a Si ring and under etched SiO_2 of 910 nm width

(B) Shows a silicon structure having the form of a number "5." Arrows (1) and (2) depict the silicon strip widths, which are 947 nm and 925 nm, respectively. Arrows (3), (4), and (5) denote the gap widths between the Si structure and under etched SiO_2. The gap of arrow (3), between a Si strip and an under etched island of SiO_2 is 862 nm wide. Arrow (4) points to a 968 nm gap, and the gap tagged by arrow (5) is 964 nm wide. It is expected that the gaps denoted by arrow (4) and (5) would be of similar width, since the under etched SiO_2 pin-shape appearing between them is precisely in the middle between the two silicon strips

(C) Depicts two crossed Si strips. The Si strip of arrow (1) is 1020 nm wide, while the silicon strip of arrow (2) is slightly narrower with a 845 nm strip width. Arrow (3) depicts a gap between the horizontal Si strip and under etched SiO_2, the gap is 958 nm wide; arrow (4) is a gap on the other side of the Si strip and it is 966 nm wide.

(D) Shows two coupled waveguides. The waveguides denoted by (1) and (2) are 520 nm wide. Arrow (3) points to a gap between the silicon waveguide of arrow (1) and under etched SiO_2. This gap is 1100 nm wide; arrow (4) marks a 1050 nm wide gap between the silicon waveguide denoted by (2) and under etched SiO_2.

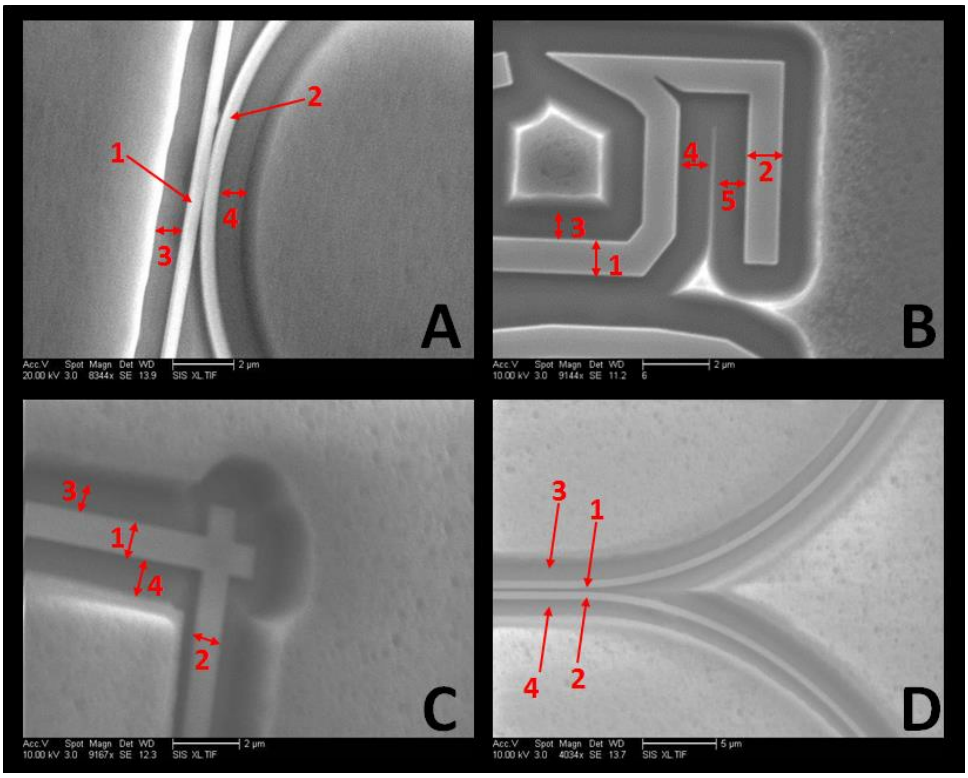

Figure 4. Presents SEM images of several silicon structures post the wet etch step (A–D) Different silicon structures post wet etch. Areas immediately adjacent to the structures are fully etched. The numbers in the figure denote particular regions and aid in identifying their measured width values.

Figure 5 depicts the silicon structures at various stages during the etch process. These SEM images show partially etched samples after 165 seconds and 185 seconds of BOE.

A detail of what is shown in the 3 quadrants of Figure 5 is shown in the following list:

(A) Shows the sample after 165 seconds of BOE. Arrow (1) points towards where the silicon waveguides are located under the SiO_2. Arrow (2) shows a gap where the SiO_2 etched faster; arrow (3) denotes a silicon waveguide peeking from underneath the partially etched SiO_2. The misplaced SiO_2 strip may be evidence of low density SiO_2 on the Si waveguide, while the trench aside the waveguide reveals the fact of lower density nature at the Si waveguide sides

(B) Shows a ring resonator after 185 seconds of BOE. Arrow (1) depicts SiO_2 positioned on top of the waveguides, while arrow (2) points towards an expanding trench.

(C) Shows a zoomed in portion of part (B) near the ring / bus waveguide interface, (1) depicts SiO_2 on top of the silicon waveguides. The width of the SiO_2 layer on top of the straight waveguide is 1307 nm, while the width of the SiO_2 layer on top of the curved waveguide is 1326 nm; (2) is a 530 nm gap formed by SiO_2 being etched at a faster rate.

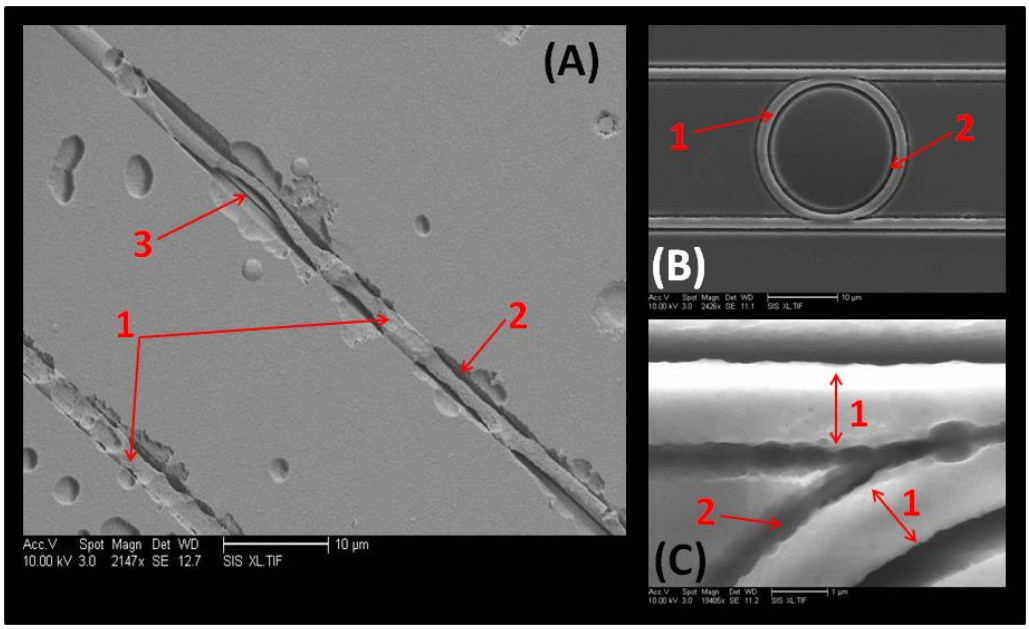

Figure 5. Depicts the silicon structures at various stages during the etch process - partially etched samples.

Figure 6 contains images taken post a 3 minute 15 second BOE bath. It can be seen that the BOE has begun to etch the buried oxide layer beneath the silicon structures.

A detail of what is shown in the 3 quadrants of Figure 6 is shown in the following list:

(A) Shows silicon structures with trenches etched immediately in their vicinity. It can be seen that the SiO_2 farther back has not been completely etched.

(B) Shows a close up of Figure 6 (A).

(C) Shows a silicon bus waveguide and a portion of a silicon ring. Arrow (1) points to a trench formed post BOE etch. The trench is 1025 nm wide. Arrow (2) marks a 496 nm wide silicon waveguide, and arrow (3) shows a 1030 nm trench formed to the inside of the silicon ring. Arrow (4) marks a 940 nm tall plateau of under etched SiO_2 located to the inside of the Si ring. Arrow (5) points to a 930 nm tall SiO_2 plateau on the outside of the silicon ring.

Figure 6 clearly shows that the SiO_2 etch rates greatly differ in the vicinity of the Si structures versus the etch rates taking place 1 µm or farther away from the Si strips. Here based on the amount of etched SiO_2, it can be deduced that the BOE etch rate 1 µm away from the waveguides was 4.5 nm/second, and in the neighborhood of the waveguides it increased to 9.2 nm/second. Figure 7 and Figure 8 further emphasize this point by providing a summary of the trench width on each side of a silicon strip and the height of the under etched SiO_2 layer measured for 10 different samples.

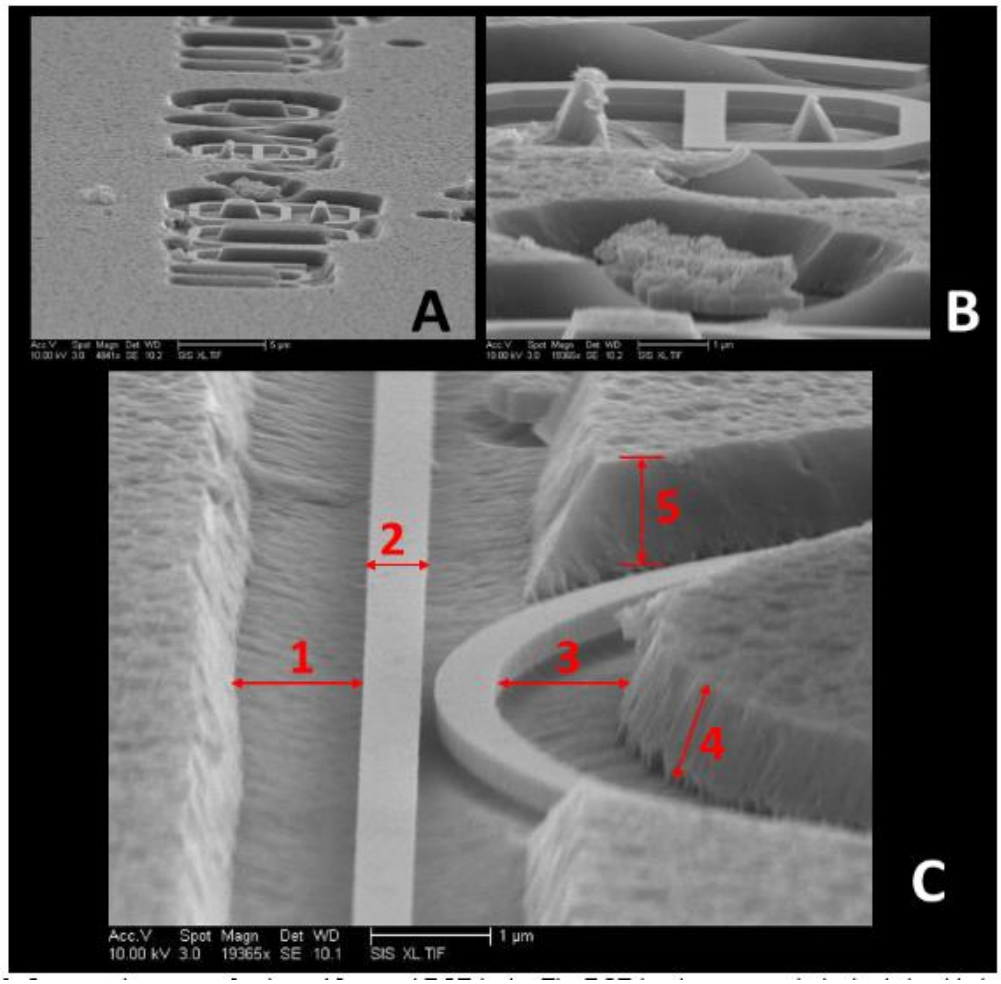

Figure 6. Images taken post a 3 minute 15 second BOE bath. The BOE shown has begun to etch the buried oxide layer beneath the silicon structures.

Figure 7 shows the measured results for the trench size on each side of a silicon structure as a function of the structure width. Each blue dot corresponds to an individual sample. The purple, dotted lines represent the standard deviation σ_{trench} = 71 nm of the trench data with a mean of $\bar{x}_{trench}$ = 956 nm. Figure 8 shows the height of the plateau of SiO_2 surrounding each over-etched trench for 10 different samples. The data is ordered by sample number. The mean of the under etched layer is σ_{etch} = 914 nm (green dotted line) and the standard deviation (purple dotted line) is $\bar{x}_{etch}$ = 45 nm.

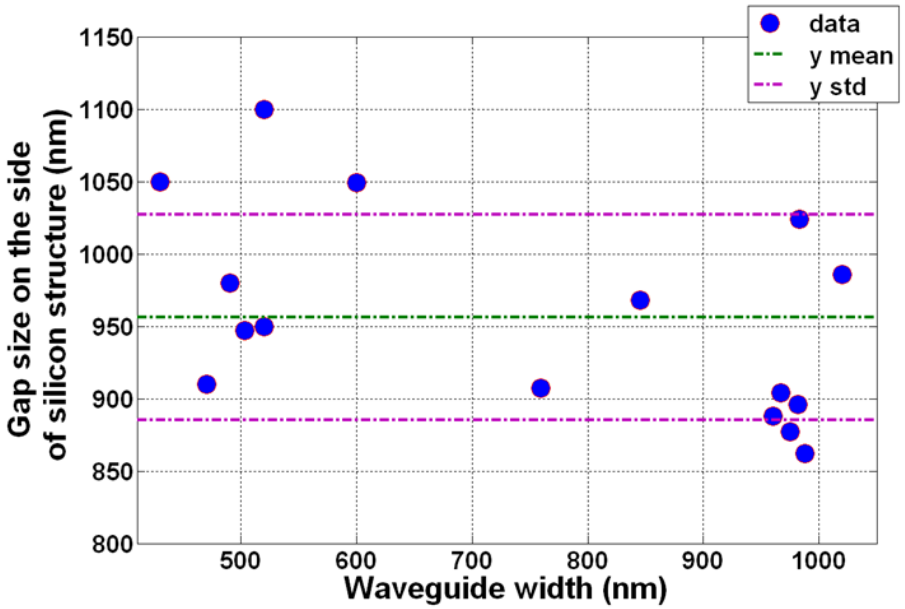

Figure 7. Trench size on each side of a silicon structure as a function of structure width. The blue dots represent measured results of individual samples. The purple, dotted lines represent the standard deviation (71 nm) of the data with a mean of 956 nm.

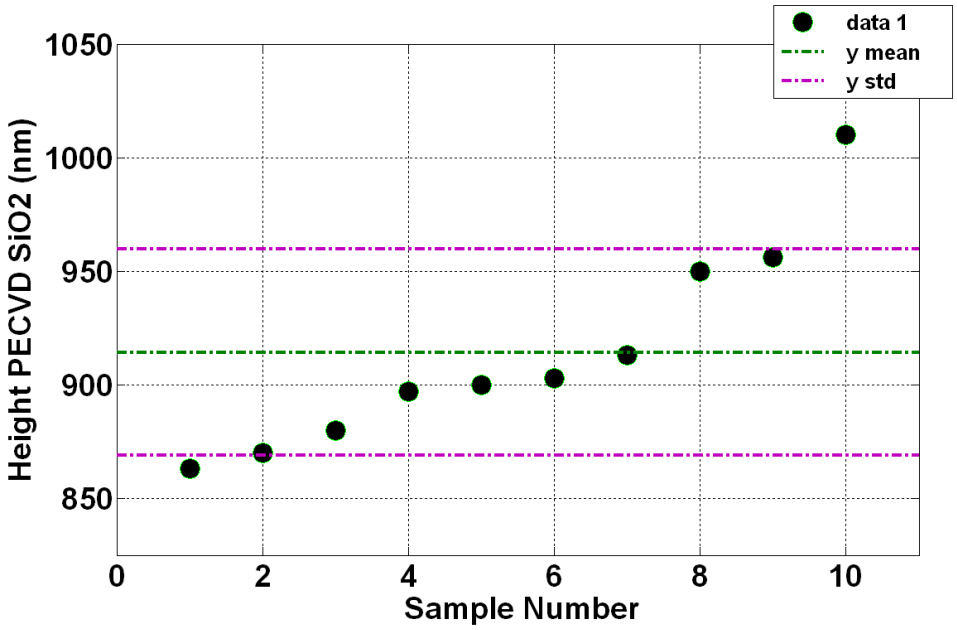

Figure 8. Height of the under etched SiO_2 layer for 10 different samples. The data is ordered from lowest to highest value. The mean of the under etched layer is 914 nm (green dotted line) and the standard deviation (purple dotted line) is 45 nm.

Figure 9 depicts an unetched Si waveguide covered in PECVD SiO_2. (A) depicts the source document unchanged. (B) is an enhanced colorized version to make it easier to see the different parts of the figure. The sample was cleaved in order to obtain this image. The Si waveguide width is 475 nm and the PECVD SiO_2 layer shown as gold in (B) is 1794 nm thick. A bulge of PECVD SiO_2 is formed directly over the Si waveguide. This bulge is 2290 nm wide and it rises to 375nm above the rest of the PECVD SiO_2 film, and extends out to 910 nm on the side of the Si strip. The image does not show visible air gaps in the vicinity of the Si waveguide, suggesting that LD SiO_2 is responsible for this effect. The LD SiO_2 regions are also not visible in this image, likely due to a low refractive index contrast between the LD SiO_2 and the higher density PECVD SiO_2 region.

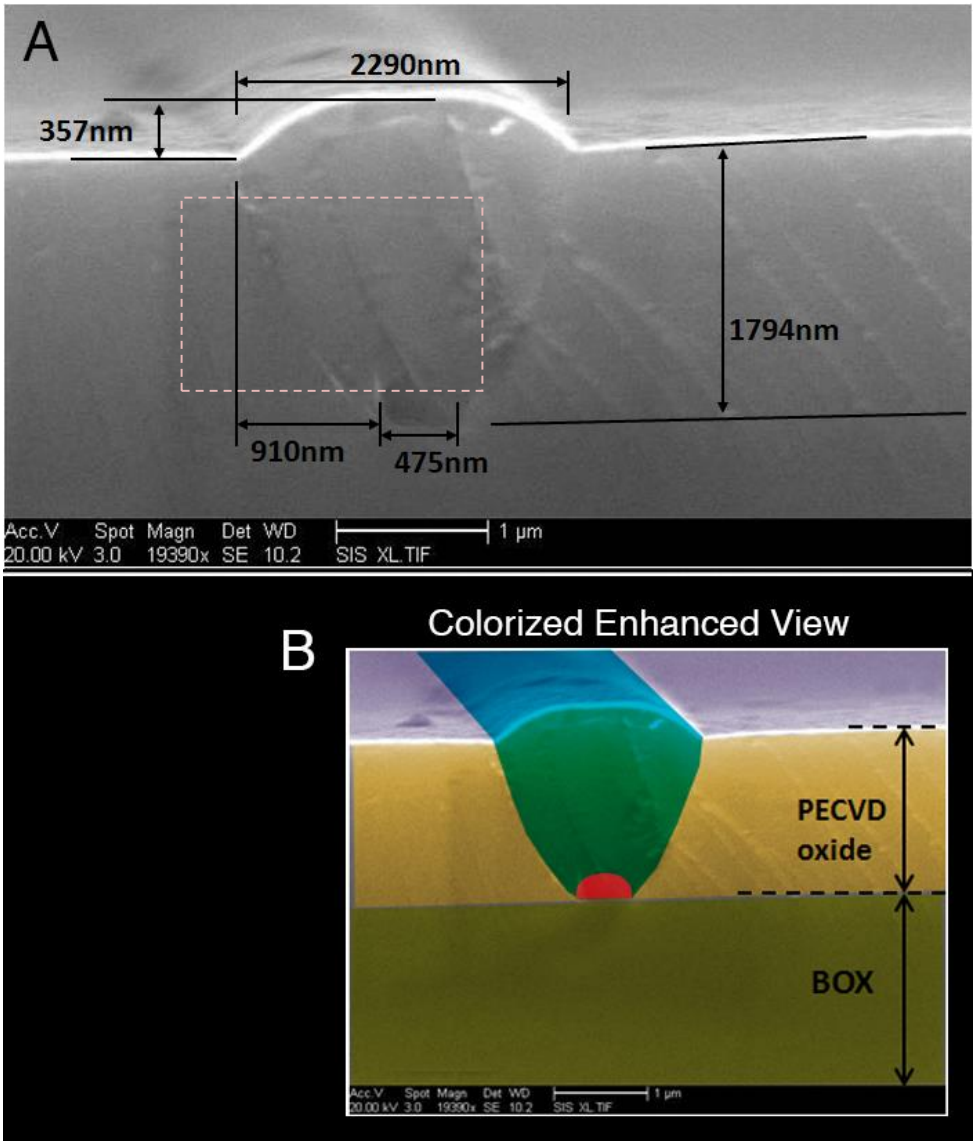

Figure 9. An unetched Si waveguide covered in PECVD SiO_2 (A, B). The Si waveguide width shown in red in (B) is 475 nm and the PECVD SiO_2 layer is 1794 nm thick (measurements shown in A). A bulge of PECVD SiO_2 is formed directly over the Si waveguide. This bulge is 2290 nm wide and it rises to 375 nm above the rest of the PECVD SiO_2 film. The protuberance extends out to 910 nm on the side of the Si strip.

4. DEVICE CHARACTERIZATION AND CALIBRATION

Samples clad in PECVD silicon dioxide and samples clad in air were examined. The calibration was performed in two steps. (1) A sample consisting of a silicon waveguide positioned on top of a BOX layer with an upper air cladding (BOX / Si / air) was measured and served to define the refractive index distribution of the Si waveguide and SiO_2 substrate within the COMSOL model; (2) the silicon waveguide sample was covered in PECVD SiO_2 (BOX / Si / PECVD SiO_2) and measured. This measured result functioned to extract the effective index of the PECVD SiO_2 layer.

In order to characterize the effects of LD PECVD SiO_2 claddings, the free spectral range (FSR) of air clad and PECVD SiO_2 clad ring resonators was measured. The FSR range was used to calculate the effective indices of the waveguide modes and the effective indices are in turn employed to obtain the LD PECVD refractive index value. For this analysis, chip-scale ring resonators were used because they are highly sensitive to refractive index variations, [17–20], down to the order of 10^{-5}–10^{-7} RIU (refractive index units). Ring resonator structures support circulating waves (travelling waves) which are evanescently coupled to the ring from a bus waveguide. The sensitivity of a ring resonator depends on the resonator Q, and the extent to which the optical mode of the waveguide interacts with the cladding. A resonance occurs when the optical path length of the resonator is exactly a whole number of wavelengths. The resonant wavelength is given by

$$\lambda_{res} = \frac{n_{eff}\, 2\pi r}{m}, \quad m = 1, 2, 3... \tag{1}$$

where n_{eff} is the effective refractive index, r is the radius of the ring and m is the order of the resonant mode. The wavelength spacing between two successive resonance dips (in the case of an all pass resonator) or resonance peaks (in the case of an add-drop filter drop port) is referred to as the free spectral range (FSR):

$$FSR = \frac{\lambda^2}{n_g\, 2\pi r} \tag{2}$$

with n_g defined as the group index and described by

$$n_g = n_{eff} - \lambda_o \frac{\partial n_{eff}}{\partial \lambda} \tag{3}$$

To study the effects of LD silicon dioxide claddings, the measured ring resonator group indices were input into a 2-D COMSOL Multiphysics finite-element model and used to calculate the refractive index of PECVD SiO_2 surrounding the silicon waveguides. This simple model works well for an accurate calibration and design of silicon structures, since the effective refractive index parameter determines not only the propagation constant of a waveguide but also the center frequency of photonic filters.

The ring resonator add-drop filter consisted of two 500 nm wide, 30μm long waveguides separated by 100 nm from a centrally situated 500 nm wide and 19.8 μm diameter ring (Figure 3 (A). Effective mode indices and propagation constants for the TE-like mode of the resonator were defined using the effective index method [21, 22]. The horizontal (TE-like) mode is preferred since it extends in the direction of the waveguide sidewalls where the LD SiO_2 appears. It is instructive that most existing SOI devices work with the TE-like polarization, since it is the ground mode of the waveguide and it

offers a stronger confinement. Tuning of the ring resonator depends on how far the mode extends into the cladding regions, the amount of space in the coupling region between the ring and waveguide, and the accrued losses (including coupling to bus waveguides).

The experimental setup is depicted in Figure 10. The sample was placed on a three axis mechanical stage allowing for precise alignment of the sample with the imaging optics. A second three axis mechanical stage served to align an optical single mode input fiber with the edge of an on-chip waveguide. Linear inverse tapers were implemented to aid in the coupling. The adiabatically widened tapers work by increasing the mode size of the waveguide to that of the fiber, and offer a low loss coupling mechanism with a predicted loss of 1.5 dB for a 100 nm tip, 100 µm long linear inverse taper [23]. An Agilent 8163B telecom-grade laser (1470–1570 nm range) coupled with a polarization scrambler and a fiber polarization controller served to measure the transmission spectrum. Waveguide output was free space imaged onto a power meter. Control of the telecom source and the power meter was automated.

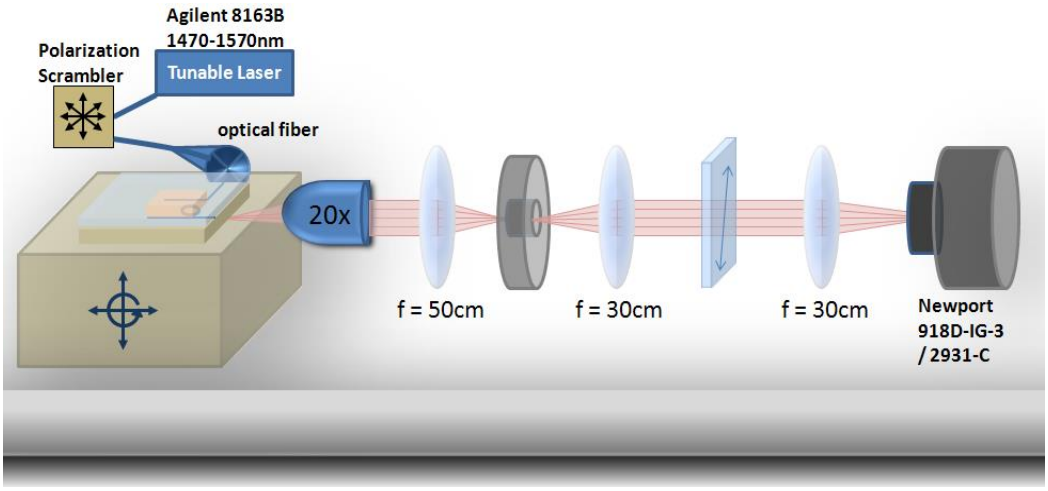

Figure 10. Measurement setup. An Agilent tunable source is fiber coupled to the on-chip waveguides and the output is free space imaged onto a detector.

Figure 11 depicts the measured response of ring resonator structures when they're clad in air (A), and in PECVD deposited silicon dioxide that covers half of the ring (B), with refractive indices of the SiO_2 layers depicted on the graphic inset.

The air clad samples served as a reference for the simulation model. Refractive indexes of the buried oxide layer, PECVD silicon dioxide layer on a planar silicon surface, and silicon at 1550 nm are n_{BOX} = 1.444 [24,25], n_{PECVD} = 1.453 [26], n_{Si} = 3.478 [27,28]. The free spectral range (FSR) of the Figure 11 air clad sample is FSR_{air} = 8.455 nm resulting in a group index of $n_{g,air}$ = 4.568. The SiO_2 clad sample possesses a FSR_{SiO2} = 7.20 nm with a group index of $n_{g,SiO2}$ = 5.364. The resonance linewidth of Figure 11 (B) is wider than that of Figure 11 (A) due to the loss associated with the SiO_2 cladding interface being positioned mid-way through the ring.

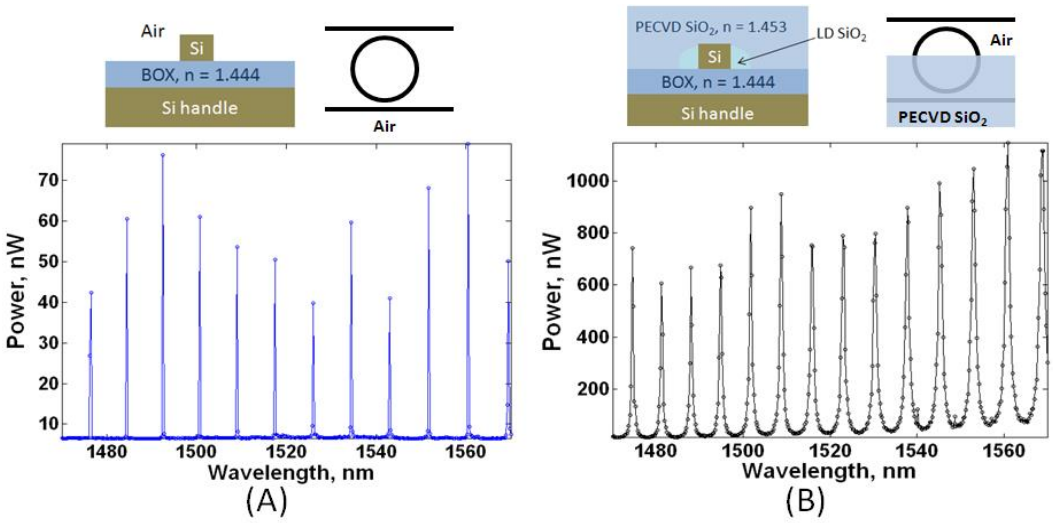

Figure 11. Measured ring resonator response for (A) sample with air cladding (1/2 open), (B) sample clad in PECVD deposited silicon dioxide. Diagrams above the measured spectra depict the sample layers and corresponding refractive indices of BOX and PECVD SiO_2.

Measured ring resonator group indices ($n_{g,air}$, $n_{g,SiO2}$) together with the measured ring resonator effective mode indices ($n_{eff,air}$, $n_{eff,SiO2}$) served to calculate the refractive index of LD PECVD SiO_2 surrounding the silicon waveguides. The ring waveguide curvature and the resulting effective index were considered using the conformal transformation method [9]. The LD SiO_2 refractive index is $n_{LD\text{-}PECVD}$ = 1.253, which is considerably lower than the anticipated value of n_{PECVD} = 1.453. The difference in refractive indices between a film of PECVD SiO_2 deposited on a planar surface and that of PECVD SiO_2 surrounding the silicon strip waveguides is Δn = -0.2, and the density of the LD SiO_2 layer was estimated to be ρ_{SiO2} = 1.27g/cm^3 using the Gladstone–Dale equation [29]. From this analysis, it can be concluded that the LD areas contain a decreased atomic concentration of Si C_{Si} < 35.2% and an increased atomic concentration of oxygen C_O > 64.8% [30,31].

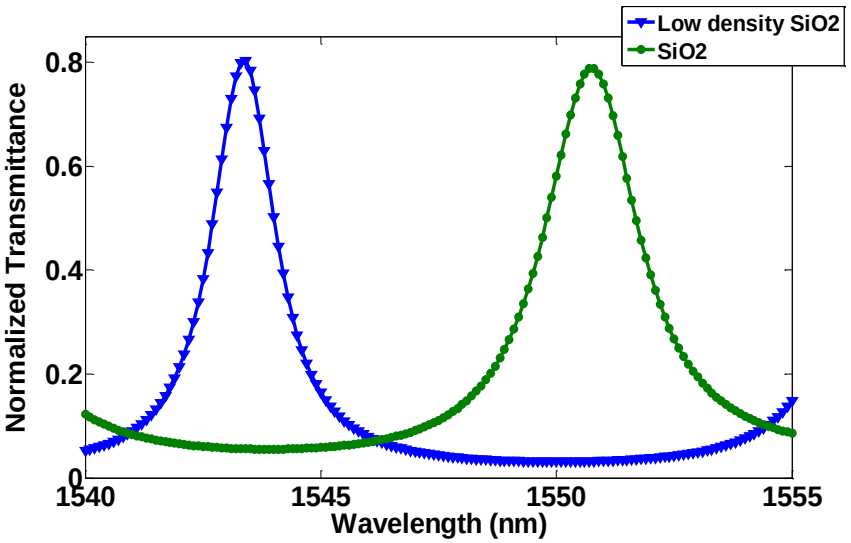

Figure 12. Resonant wavelength shift due to LD SiO_2 cladding for a Si ring of 500nm width, 250nm height and 19.8μm diameter.

Figure 12 shows the effect of this refractive index difference on a ring resonator device performance for a ring of 500 nm width, 250 nm height and 19.8 μm diameter (same parameters as those of the measured devices in Figure 11). The expected location of the resonance peak is $\lambda = 1550.7$ nm, but due to the LD SiO_2 it occurs at $\lambda = 1543.4$ nm, a 7.3nm change. In wavelength division multiplexing (WDM) or dense wavelength division multiplexing (DWDM) systems with channel spacing of > 5 nm and < 1 nm, respectively, a difference of $\Delta\lambda = 7.3$ nm will greatly influence channel location and crosstalk. For future applications relying on DWDM to support a large number of base stations connected to a central station, such as millimeter-wave-band radio over-fiber (RoF) systems [32], this effect needs to be considered.

5. DISCUSSION

Designs relying on smaller width silicon strip waveguides will be subject to a more pronounced center wavelength inconsistency due to a larger portion of the optical mode being present in the cladding region. Figure 13 (A, B) shows the fraction of TE-like and TM-like mode power density in the cladding region as a function of waveguide width. As the waveguide becomes narrower, more of the mode resides in the cladding regions. Ramifications of this include increased scattering loss due to greater interaction of the less confined mode with sidewall roughness [34–36]. Another consequence, amplified in the presence of slender silicon strip waveguides, is the location of the resonance of a ring resonator filter. Low density SiO_2 near the silicon waveguides causes for a 500 nm wide ring resonator to experience a blueshift of $\Delta\lambda = 7.3$ nm for TE-like modes, while the resonance shift for a 400 nm wide ring waveguide is $\Delta\lambda = 13.75$ nm as shown in Figure 14. Rings with geometry relying on a larger diameter will also see a more appreciable resonance difference, since $\Delta\lambda$ is dependent on the ring radius and the effective path length around the ring (Equation 1).

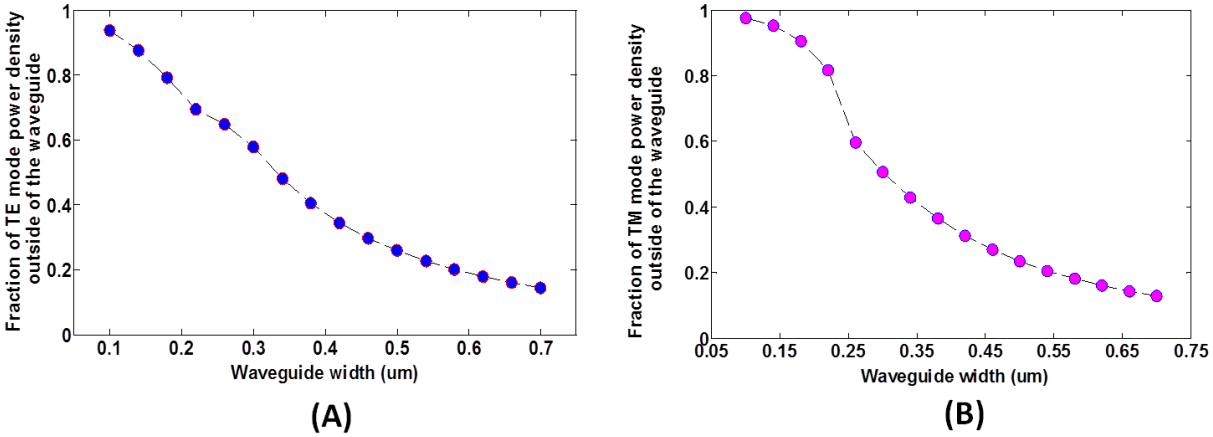

Figure 13. (A, B) The fraction of TE-like and TM-like mode power density in the cladding region as a function of waveguide width. The waveguide height is 250 nm. The indices of refraction used for this model include nBOX = 1.444, ncladding = 1.453 at λ = 1550 nm.

In this work, the effect of PECVD deposited claddings is calibrated and guidance is provided for more accurate design of silicon photonic structures considering the effects of LD SiO_2. In the presented LD model, PECVD SiO_2 is defined as two bulk areas with distinctive indices; one area with the expected SiO_2 refractive index value and the second area with the LD SiO_2 refractive index. This is a simple model and it does not consider a possible gradient distribution of PECVD SiO_2 index from the boundary of the Si waveguide. From a design perspective, this model aids in the calibration of silicon structures, since their properties are mainly determined by the effective refractive index parameter.

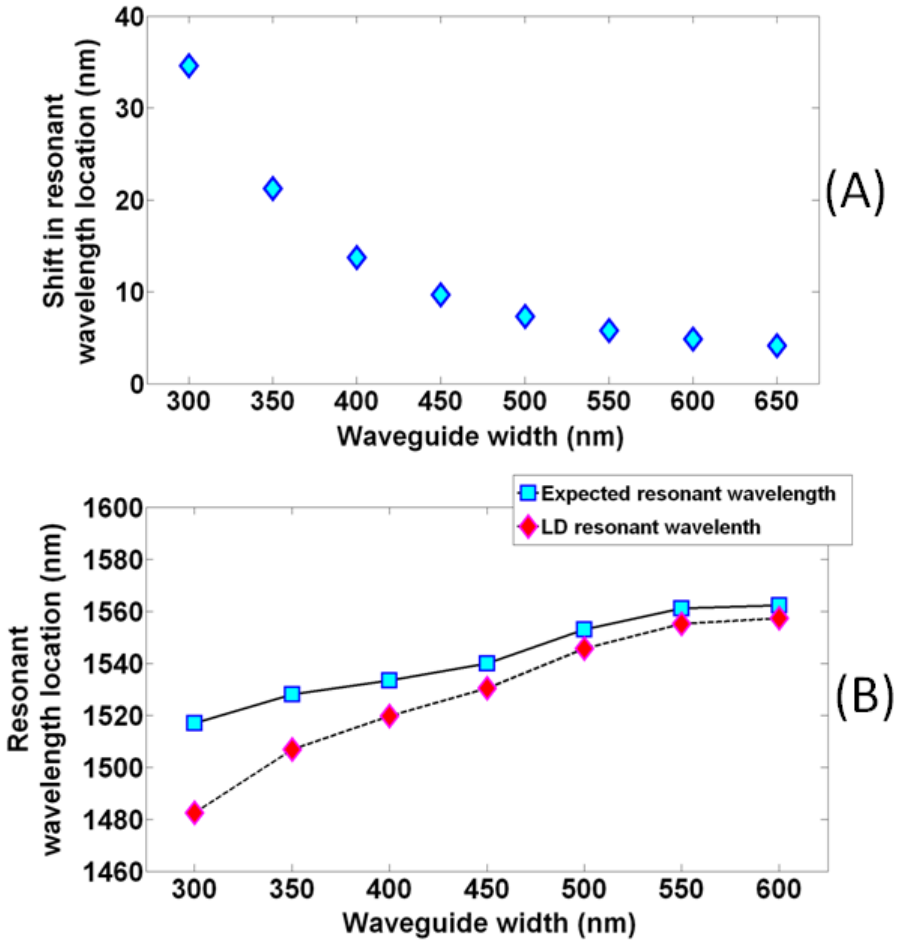

Figure 14. Resonant wavelength shift (for a ring resonator structure) due to LD SiO_2 cladding for various waveguide widths for TE-like modes. (A) Shift in nm of the resonant wavelength location. (B) Comparison of the expected resonant wavelength location and the actual wavelength location due to the LD cladding region.

6. SUMMARY

In conclusion, adverse effects of LD PECVD SiO_2 claddings surrounding silicon strip waveguides for photonic applications were reported and design calibration suggestions were provided. The LD SiO_2 regions surrounding Si waveguides etch at twice the rate as compared to the SiO_2 regions located 1 µm away from the silicon strips and show a refractive index of $n_{LD\text{-}PECVD} = 1.253$. Ring resonators, which are highly sensitive to refractive index variations, were used in characterizing the LD silicon dioxide claddings. The measured free spectral range of air clad and PECVD SiO_2 clad ring resonators was used to calculate the effective indices of the waveguide modes, and the effective indices were in turn employed to obtain the LD PECVD refractive index value in the vicinity of the silicon waveguides. A cladding refractive index difference of $\Delta n = -0.2$ between the expected PECVD SiO_2 refractive index and the LD SiO_2 refractive index in the neighborhood of the waveguides resulted in a 7.3 nm blueshift of the center resonance. This simple model aids in the calibration and design of silicon structures, since their properties are mainly determined by the effective refractive index parameter.

In the LD model, the PECVD SiO_2 was defined as two bulk areas with distinctive indices; one area with the expected SiO_2 refractive index value and the second area with the LD SiO_2 refractive index. This is a simple model and it does not consider a possible gradient distribution of PECVD SiO_2 index from the boundary of the Si waveguide. From a design perspective, this model aids in the calibration of silicon structures, since their properties are mainly determined by the effective refractive index parameter.

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14. ABSTRACT

Analysis and experimental demonstration of adverse device performance of silicon waveguides clad in silicon dioxide (SiO2) deposited through plasma enhanced chemical vapor deposition (PECVD) is presented. The PECVD SiO_2 is of lower density in the vicinity of silicon strip waveguides and it shows a refractive index of n = 1.253 and an estimated density of $\rho SiO_2 = 1.27 g/cm^3$. The etch rate of this low density (LD) SiO2 is two times higher than anticipated. It is shown that a silicon ring resonator sustains a 7.3nm resonance blue shift from the predicted center wavelength due to the LD SiO2 cladding in the neighborhood of silicon waveguides.

15. SUBJECT TERMS

silicon dioxide; cladding; ring resonator; low density; silicon waveguide; photonics; plasma enhanced chemical vapor deposition

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