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Effects of Annealing Hydride Vapor Phase Epitaxy (HVPE) Gallium Nitride (GaN) Films on Sapphire at High Temperatures

by Michael A Derenge and Kenneth A Jones

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Sensors and Electron Devices Directorate, ARL

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14. ABSTRACT

It is well known that gallium nitride (GaN) decomposes at temperatures above 800 °C without either a large nitrogen overpressure or thermally stable cap to prevent nitrogen loss. This study looks at electrical and surface topography changes in 10.5-µm hydride vapor phase epitaxy (HVPE) GaN on sapphire samples when annealed at four different temperatures and times. HVPE GaN samples were capped with a double layer aluminum nitride (AlN) annealing cap, deposited first by an 80-nm low-temperature metal-organic chemical vapor deposition film and followed by a sputtered 1-µm AlN layer. After cap removal, atomic force microscopy (AFM) topographs were used to characterize surface changes. AFM topographs at 1150 and 1200 °C showed step growth structures were still visible with slight increases in surface roughness due to polygonization with increased annealing time. Anneals at 1250 °C for 4 and 8 min and all 1300 °C show increased roughness with time. An "as received" (AR) GaN control sample and the annealed GaN were then processed into Schottky diodes. Current-voltage and capacitance-voltage measurements were taken of the diodes. Current density-voltage analysis of AR diodes showed reverse leakage decreases, knee voltage (V_K) increases, and conductance (G) decreases dependent on increasing distance from the edge of the sample. $Ø_b$, reverse leakage, V_K, and G changes were interpreted as dependent on compressive stress induced piezoelectric effects. Reverse leakage increased with anneal time and temperature. Increased tensile stress and concave bowing with temperature from differential coefficient of thermal expansion between the GaN film and sapphire substrate is believed to contribute to increasing N_d near the surface progressing from edge to center. Increases in N_d is believed to be creation of nitrogen vacancies that act as donors.

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Summary

Currently, nitride p-n junction devices are limited to vertical growth device structures. The Power Components Branch of the Sensors and Electron Devices Directorate at the US Army Combat Capabilities Development Command, Army Research Laboratory (ARL) is working on the Department of Energy's PNDIODES program to develop selective area ion doping processes for lateral p-n structures. Numerous groups, including ARL,[1,2] have been successful with silicon n-type implantation activation, but p-type implant activation, of which magnesium (Mg) is the most frequently used accepter, has not been successful. The results of this study show increases in carrier concentration (N_d) with high-temperature annealing that would compensate Mg doping.

It is believed that ion implants need to be annealed at high temperatures to reduce implant damage and activate the implanted ions. Unintentionally doped gallium nitride (GaN) was annealed without implanted ions to test if the material changed in a way to prevent Mg ion implantation.

Current-voltage electrical measurement of Schottky diodes showed a location dependence for knee voltage, conductance, and reverse leakage with distance from the edge of the sample for the as-received as well as annealed samples. Atomic force microscopy roughness measurements also had location dependence for the annealed GaN surface. Capacitance voltage measurements showed increased N_d from edge to center for GaN annealed at 1250 and 1300 °C. These location-dependent variations were attributed to piezoelectric effects caused by the stresses induced by coefficient of thermal expansion (CTE) differences between the sapphire substrate and the heteroepitaxial GaN. The larger CTE of sapphire creates tensile stresses in GaN at high temperature that deteriorate cap adhesion and contributes to nitrogen loss in GaN. The nitrogen loss compensates the p-type carriers that we are attempting to create with Mg implants. Switching to GaN substrates should greatly reduce the stresses that contribute to cap adhesion deterioration. Silicon carbide (SiC) substrates would put GaN in compression at elevated temperatures and in tension at room temperature, which might improve the GaN survivability. In the future we will work with bulk GaN or SiC substrates for Mg implantation studies.

[1] Hager CE IV, Jones KA, Derenge MA, Zheleva TS. Activation of ion implanted Si in GaN using a dual AlN annealing cap. Journal of Applied Physics. 2009;105(3). doi: 10.1063/1.3068317.
[2] Nguyen C, Shah P, Leong E, Derenge M, Jones K. Si implant-assisted ohmic contacts to GaN. Solid State Electronics. 2010;54(10):1227–1231.

1. Introduction

N-type silicon implantation activation of gallium nitride (GaN) has been successful,[1,2] but p-type magnesium (Mg) implantation has proven to be more of a challenge. Piezoelectric effects in AlGaN/GaN high electron mobility transistors (HEMTs) to create a 2-dimensional electron gas (2DEG) are well publicized.[3,4] These piezoelectric effects can be useful for creating a higher density of conduction electrons with a high electron mobility in the 2DEG at the AlGaN/GaN interface, but they can also lead to deterioration of HEMT devices near gate electrodes in the presence of high electric fields. Piezoelectric effects on barrier height ($Ø_b$) have been characterized in III-V semiconductors like gallium arsenide[5,6] and GaN.[7] We have found that stresses due to the coefficient of thermal expansion (CTE) mismatch affects the electrical properties at room temperature. We have also found CTE mismatch greatly affects changes in GaN defects when annealed at high temperatures.

As-received (AR) GaN was processed into nickel contact Schottky diodes (hereafter referred to as diodes), which were characterized by current-voltage (IV) and capacitance-voltage (CV) measurements. This study investigates high-temperature annealing by analyzing room temperature IV and CV electrical measurements and changes in atomic force spectroscopy (AFM) surface roughness measurements. We found that knee voltage (V_K) had a wide distribution that was determined to increase with distance from the edge. Carrier concentraton (N_d) was expected to be continuous with depth, but in AR samples, N_d was found to decrease near the surface. A second AR sample was made in which 220 nm of GaN was removed from half the sample to characterize bulk GaN properties away from the AR surface.

2. Procedure

A 2-inch-diameter sapphire wafer with a 10.5-µm-thick hydride vapor phase epitaxy (HVPE) GaN film was cut into 16 pieces (twelve 11- × 10.5-mm rectangles and four edge-rounded triangles [10.5-mm sides with a 1-inch radius of curvature]). All pieces had 5- × 5-µm AFM topographs measurements before depositing a dual-layer aluminum nitride (AlN) annealing cap.[8] The AlN-capped HVPE GaN was annealed in a nitrogen atmosphere using an induction furnace on a graphite susceptor according to the procedure covered in patent application US20160061528 A1.[9] The annealing schedule shown in Table 1 was for four temperatures and four times with the small triangles used at lower temperatures.

One triangle was kept for control, but it was damaged during lithographic processing. In its place, a piece from a wafer grown in the same run was used.

Table 1 Annealing schedule

Temperature (°C)	Time			
	1 min	2 min	4 min	8 min
1150	…[a]	▲	▲	■
1200	■	▲	■	■
1250	■	■	■	■
1300	■	■	■	■

Sample legend: ■ = 11- × 10.5-mm rectangle; ▲ = 10.5-mm-side rounded triangle
[a] One triangle was kept for control, but it was damaged during lithographic processing. In its place, a piece from a wafer grown in the same run was used.

The AlN cap was removed by etching in a 2-M potassium hydroxide (KOH) solution for 16 h. AFM topographs were taken near the center and edge of the annealed GaN surface. One AR sample and all the annealed samples were processed into diodes. One-micrometer mesas were dry etched ($BCl_3/Cl_2/Ar$ chemistry inductively coupled plasma [ICP] reactive ion etcher) into the 10.5-µm films for the ohmic contacts and Schottky contacts on top of the mesa.

After performing CV on AR diodes that were made on commercially available unintentionally doped HVPE GaN, we found that the top layer of GaN had a lower carrier concentration. The manufacturer was contacted about the lower carrier concentration on the surface, and they said it is from deposition after the growth process has stopped. The top layer has higher silicon (Si) and oxygen (O) contamination from the reactor walls when deposition continues during cooldown to unload. The wafer is marketed as a GaN template and structures are expected to be grown on the template. A second AR sample was used to characterize the difference in top surface and bulk HVPE by processing diodes with the same process described earlier, but on half-AR and half-etched diodes to 220 nm depth by chlorine chemistry ICP etcher.

3. Results

AFM topographs of AR and the annealed GaN surface are shown in Fig. 1. The bottom of each topograph represents the sapphire A (1 1 –2 0) and the GaN M (1 –1 0 0). Step growth lines appear parallel to the GaN M-plane. The outlier roughness of the 1200 °C 1-min (1200 °C-1m) anneal appear uncharacteristically rougher than other anneals. All other annealed samples appear to progress in surface roughness with increased anneal time (t_A) and temperature (T_A). The 1150 and

1200 °C topographs, with the exception of 1- and 8-min center(Figs. 1i and 1o), have fine etch pits that aligned parallel to the <11-20> directions. Those same exceptions had deep trenches aligned parallel to the same M-plane.

The 1250 °C topographs that still had step growth structures did not show fine etch pits along the <11-20> directions. The 1250 and 1300 °C topographs that had no visible step growth structures (Figs. 1u, 1w, 1x, and 1y) had no trenches aligned along the <11-20> directions like in Figs. 1i and 1o. Few deep thermal etch pits were observed.

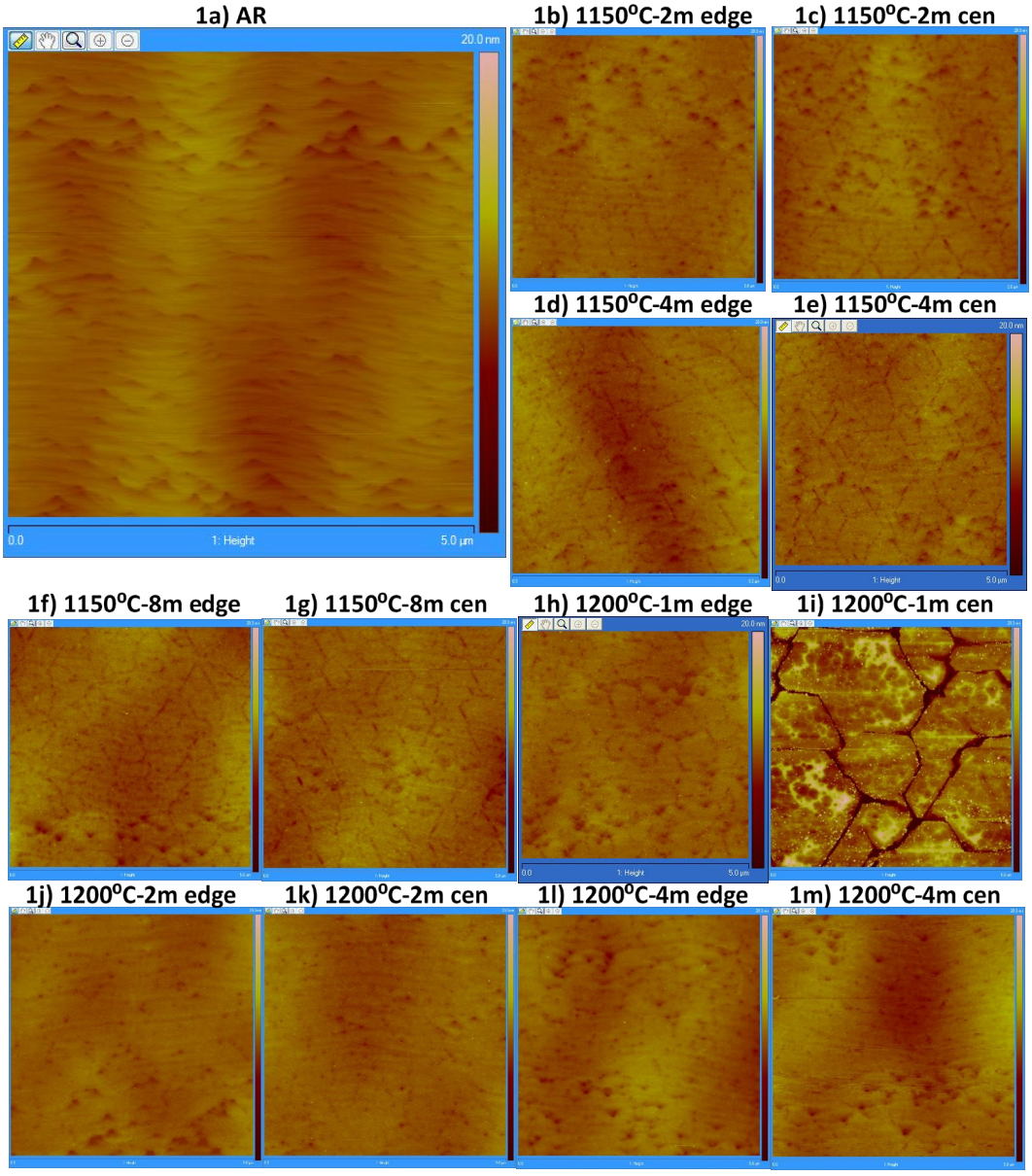


Fig. 1 AFM 5- × 5-µm topographs of characteristic AR and annealed GaN surfaces after cap removal

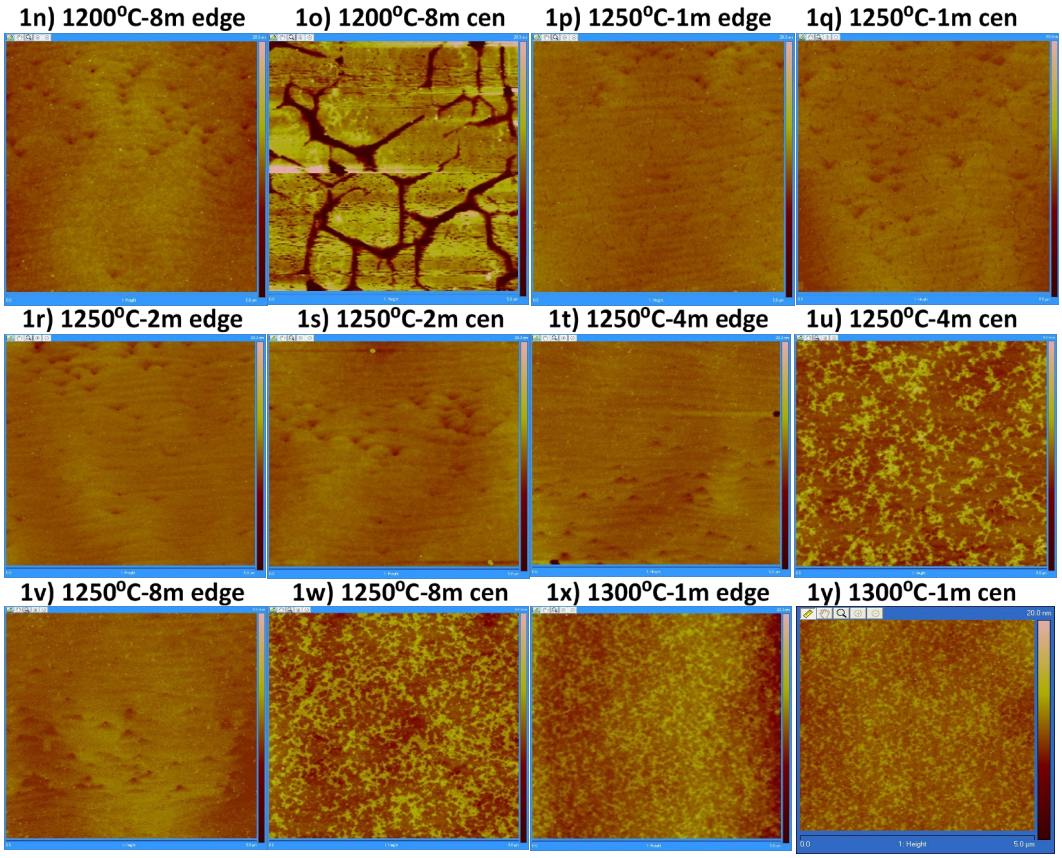


Fig. 1 AFM 5- × 5-µm topographs of characteristic AR and annealed GaN surfaces after cap removal (continued)

Table 2 gives 5- × 5-µm root mean square (RMS) roughness of the as-grown and annealed samples. Below 1300 °C roughness ranged from 0.52 to 1.2 nm with only the 1250 °C 8-min center much greater than 1. All topographs near the edge of the sample annealed at 1150, 1200, and 1250 °C still had step growth structures visible. The central 1200 °C 8-min, and 1250 °C 4- and 8-min topographs did not have step growth structures visible, which can be interpreted as GaN surface degradation. All of the 1300 °C annealed samples did not have step growth structures and roughened with increasing time.

Table 2 Average RMS roughness (Rq) of annealed GaN after cap removal derived from 5- × 5-µm scans.

Temp	Time (minutes)	Rq center	Rq edge
AR		0.69	
1150	2	0.57	0.73
1150	4	0.91	1.39
1150	8	0.61	0.88
1200	1	6.83	0.67
1200	2	0.70	0.54
1200	4	1.03	0.85
1200	8	6.03	1.03
1250	1	0.56	0.56
1250	2	0.50	0.65
1250	4	1.91	0.57
1250	8	8.84	1.00
1300	1	9.22	1.20
1300	2	5.15	1.47
1300	4	6.86	1.11
1300	8	2.62	

3.1 Electrical Results of AR Samples

AR reverse current density-voltage (JV) plots of 70-, 170-, and 270-µm diodes have median reverse leakage current density of 6×10^{-9}, 1.17×10^{-5}, and 1.77×10^{4} A/cm^2 at –5 V. Reverse leakage current increases with increasing size. No explanation is readily apparent for increased leakage density with size since 10^9 dislocations are evenly distributed. Reverse JV plots in Figs. 2a, c, and e have keys with diodes listed in order of high to low leakage and distance from the edge. Diodes near the edge leak more than diodes near the center. Figures 2b, d, and f of forward JV have V_K that increase from the edge to the center. V_K values were taken by using the least-squares method for the IV curve line after turn-on and setting y = 0 and then solving for x (mx = b). This is a good estimate as long as there is

very low forward leakage current (<1 mA/cm^2). The slope (conductance [G]) of the line has the conductance decreasing from edge to center. The smaller diodes have higher G and pronounced linear decrease in G with distance to edge.

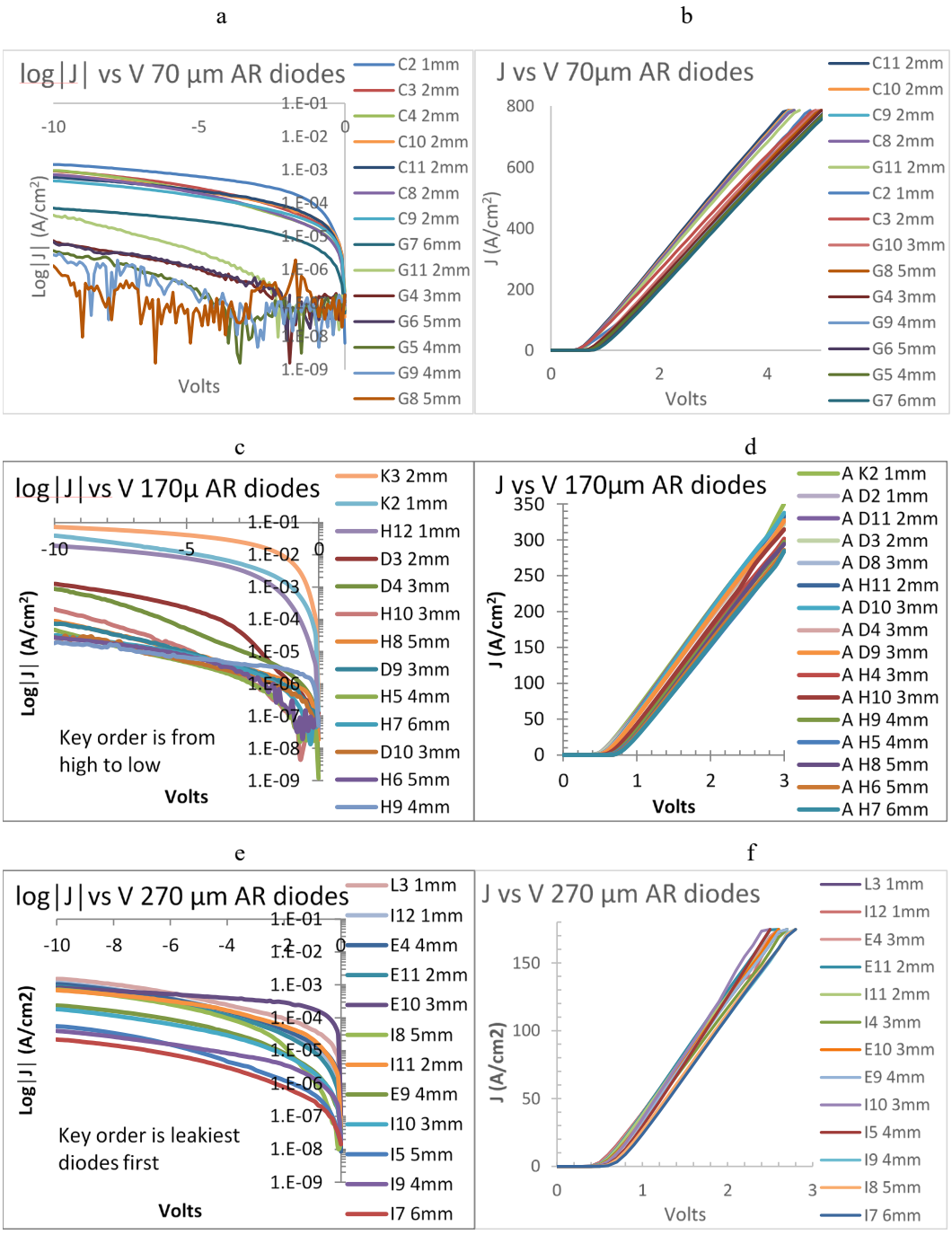


Fig. 2 J vs. V curves of AR samples for a) reverse and b) forward 70-µm, c) reverse and d) forward 170-µm, and e) reverse and f) forward 270-µm diodes

Figure 3 shows the layout of the square samples with alignment marks in the center where the columns are lettered and the rows are numbered from top to bottom. Corner triangles had to have alignment patterns near the top. Figure 4 is a CV plot of N_d versus depth, which shows that N_d has a positive slope near the surface but otherwise it is flat. N_d plots did not vary between diodes. The $Ø_b$ from CV calculations showed an increase in $Ø_b$ from edge to center for the diodes.

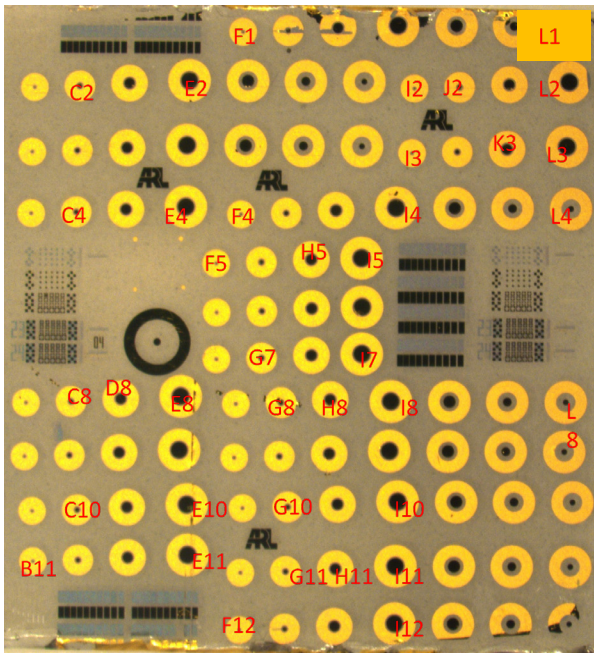


Fig. 3 Optical microscope image of processed diodes with location designation

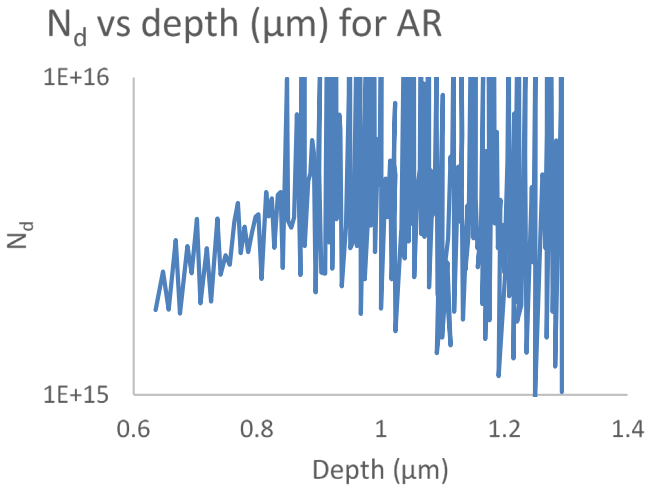


Fig. 4 N_d vs. depth plot for AR

3.2 Second AR Sample for Bulk GaN Characterization

Figure 5a reverse JV plots appear to be dispersed, but most etched samples leak less than the AR. The 170-µm diodes had median reverse leakage of 3.7×10^{-5} A/cm^2 for unetched and 9.5×10^{-6} A/cm^2 for the etched samples at –5 V.

Figure 5b forward JV plots for etched (in red font) tops were more conductive and had lower V_K in the forward bias after turn-on. The figure key is listed in order of highest to lowest G and the etched diodes are all at the top. The expanded section more clearly shows the lower V_K of the etched diodes, and Table 3 gives the range and difference in the median. G decreased and V_K increased from edge to center for etched and unetched GaN but was more evident in the unetched.

a b

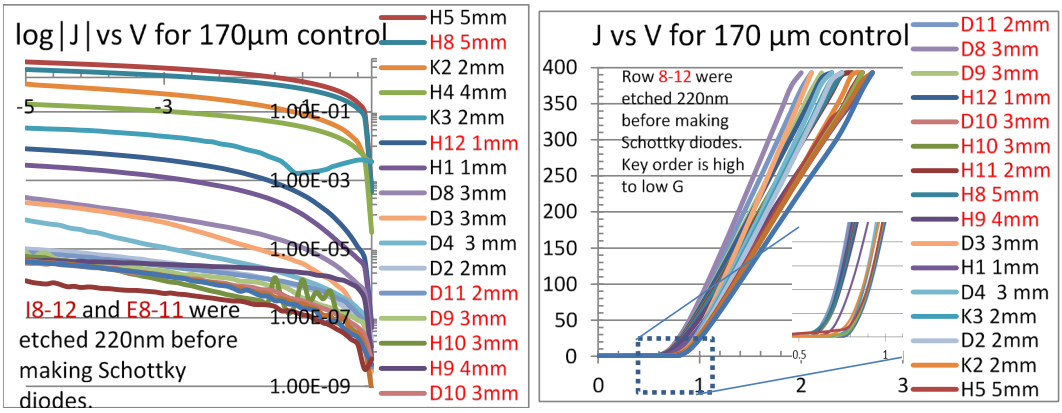


Fig. 5 a) Reverse and b) forward J vs. V plots of AR and 220-nm etched diodes. Etched diodes are indicated in red.

Table 3 Ranges for V_K on AR and etched diodes and differences between the median values

Diode size (µm)	Etched (V_K)	AR (V_K)	Δ median (V_K)
270	0.71–77	0.78–0.89	0.143
170	0.76–78	0.83–0.92	0.141
70	0.81–0.83	0.94–1.01	0.147

N_d versus depth plots of AR in Fig. 6 have decreasing N_d toward the surface while etched GaN has higher N_d and constant through depth. The 220 nm that was removed had the Si and O that was deposited during reactor cooling. Decreased N_d is contrary to expectation with vendor admission of increased Si and O concentration.

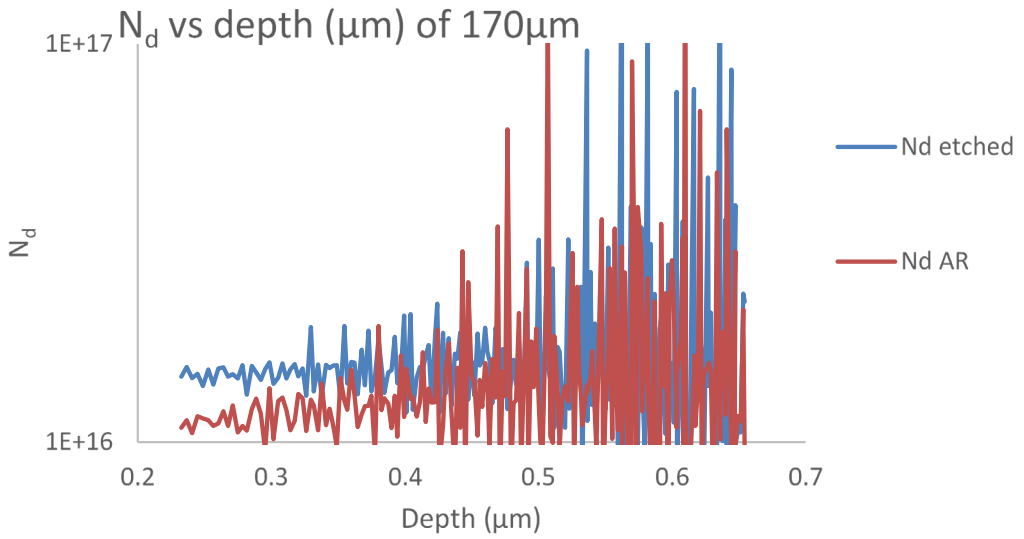


Fig. 6 N_d vs. depth for etched and AR samples

All of the annealed samples had no etching, so the unetched V_K and G values are used for comparison to annealed samples. For sake of brevity, the discussion will concentrate on 170-µm diodes.

3.3 IV of Annealed Diodes

Reverse leakage, V_K, and G values were location dependent so devices within 2 mm of edge were grouped separately from central diodes. Median values of reverse leakage current density, V_K, and G are given in Tables 4, 5, and 6, respectively, for 170-µm diode IV plots. The general trends for the grouped data from Table 4 of median reverse leakage show 4 orders of magnitude jump from an AR leakage of 1.17×10^{-5} A/cm^2 to 0.1–1.08 A/cm^2 for 2- to 8-min anneals at 1150 °C. For 1200 °C the leakage for 1200 °C 1- and 2-min are at 0.4 A/cm^2 with leakage increasing with time to 21.5 A/cm^2 at 8 min. The central diodes had higher leakage than edge diodes for longer annealing times at 1200 °C. The 1250 °C median leakage data have 2 min with lowest value. Similar to 1200 °C the edge 1250 °C diode leakage was incrementally more for 2, 4, and 8 min. The 1300 °C median leakage had 1 min with the highest leakage of 83 and the 2 and 4 min were appreciably less at 9.6 and 13. The majority of the 8-min diodes had linear IV curves with no signs of rectification.

Table 4 Median reverse leakage (in amperes per square centimeter) at –5 V for 170-µm diodes with AR median at 1.17×10^{-5} A/cm^2

T_A (°C)	1 min		2 min		4 min		8 min	
	Edge	Center	Edge	Center	Edge	Center	Edge	Center
AR	2.27E-4	9.54E-6	…	…	…	…	…	…
1150	…	…	0.11	0.96	1.65	0.25	2.26	1.15
1200	0.68	0.54	0.11	2.2	7.5	24.8	7.01	22.8
1250	12	4.81	1.76E-3	1.22	6.6	23.6	31.5	64.6
1300	120	81.5	1.89	34.5	6.9	21.2	…	…

Table 5 Median V_K with AR V_K at 0.77 V

T_A (°C)	1 min		2 min		4 min		8 min	
	Edge	Center	Edge	Center	Edge	Center	Edge	Center
AR	0.76	0.8	…	…	…	…	…	…
1150	…	…	1.07	1.15	1.10	1.17	1.07	1.13
1200	0.99	1.10	1.05	1.06	1.05	1.07	1.06	1.07
1250	1.20	1.15	1.00	1.01	1.06	1.09	0.91	0.84
1300	1.10	1.15	1.13	1.41	1.18	1.16	…	…

Table 6 Median G (in amperes per square centimeter per volt) with AR G of 261.7 A/cm^2/V

T_A (°C)	1 min		2 min		4 min		8 min	
	Edge	Center	Edge	Center	Edge	Center	Edge	Center
AR	280.7	251.3	…	…	…	…	…	…
1150	…	…	369.1	292.8	308.8	335.7	284.4	273.7
1200	365.2	358.1	431.2	398.3	381.4	344.6	286.2	292.4
1250	302.9	346.5	379.6	400.4	310.0	342	385.5	279.2
1300	262.7	281.6	324.4	259.9	283.0	219.4	…	…

Grouped V_K data in Table 5 had median V_K for 1150 °C diodes at 2, 4, and 8 min around 1.1 V, which is greater than the AR of 0.77 V. For 1200 °C anneals, the overall median V_K for 1, 2, 4, and 8 min are 1.1, 1.05, 1.06, and 1.07 V, respectively. The 1200 °C for 1 min had edge median V_K of 0.99 and central of 1.1 V. The 1 min is the highest and in the same range as 1150 °C samples, but the rest are slightly lower. The 1250 °C diodes had the same trend with 1 min having the high median values of 1.2 (edge) and 1.15 V (central). Median V_K for the 2 and 4 min were above 1 V while the 8 min was below 1 V. The 1300 °C diodes had the highest V_K values of 1.1 to 1.4 for the 1-, 2-, and 4-min anneals while the 8-min anneal produced ohmic contacts.

Table 6 median G data shows increased slope with increased anneal time with all 1150 °C diodes having greater G than the AR. The 1200 °C diodes appear to have a maximum G at 2 min at 431.2 (edge) and 398.3 (central) A/cm^2/V and decrease progressively at 4 and 8 min. The 1250 °C diodes also have a maximum G at 2 min. The 1150, 1200, and 1250 °C diodes have greater G than AR while 1300 °C have lower G closer to the AR value.

Figure 7a of 1150 °C 2-min diodes shows increased leakage at –5V from AR (1.2×10^{-5}) and location dependence of leakage is not as clear as in AR. The V_K increased from 0.83 to 0.92 for the AR (Fig. 5b) to 1 to 1.2 V after 1150 °C anneal for 2 min (Fig. 7b). The diodes near the edge have the lowest V_K and highest G. V_K increases and G decreases with distance from the edge.

The 1150 °C 4-min median reverse leakage of edge diodes is more than those near the center, but the location dependence of reverse leakage is not discernable with the interspersed distance values of the ordered key in Fig. 7c. The 1150 °C 4-min anneal had edge diode H12 (0.97 V) and K14 (0.98 V) plots of V_K less than 1 as seen in Fig. 7d, while most diodes have V_K near the median value of 1.15 V. G is more than AR, but slightly less than 2-min diodes.

The 1150 °C 8-min diodes have increased reverse leakage (Fig. 7e), decreased conductance (Fig. 7f), and V_K of approximately 1.1 with less location dependence. Two-minute annealed diodes had clear location dependence of electrical properties, but location dependence was less clear with increasing anneal time.

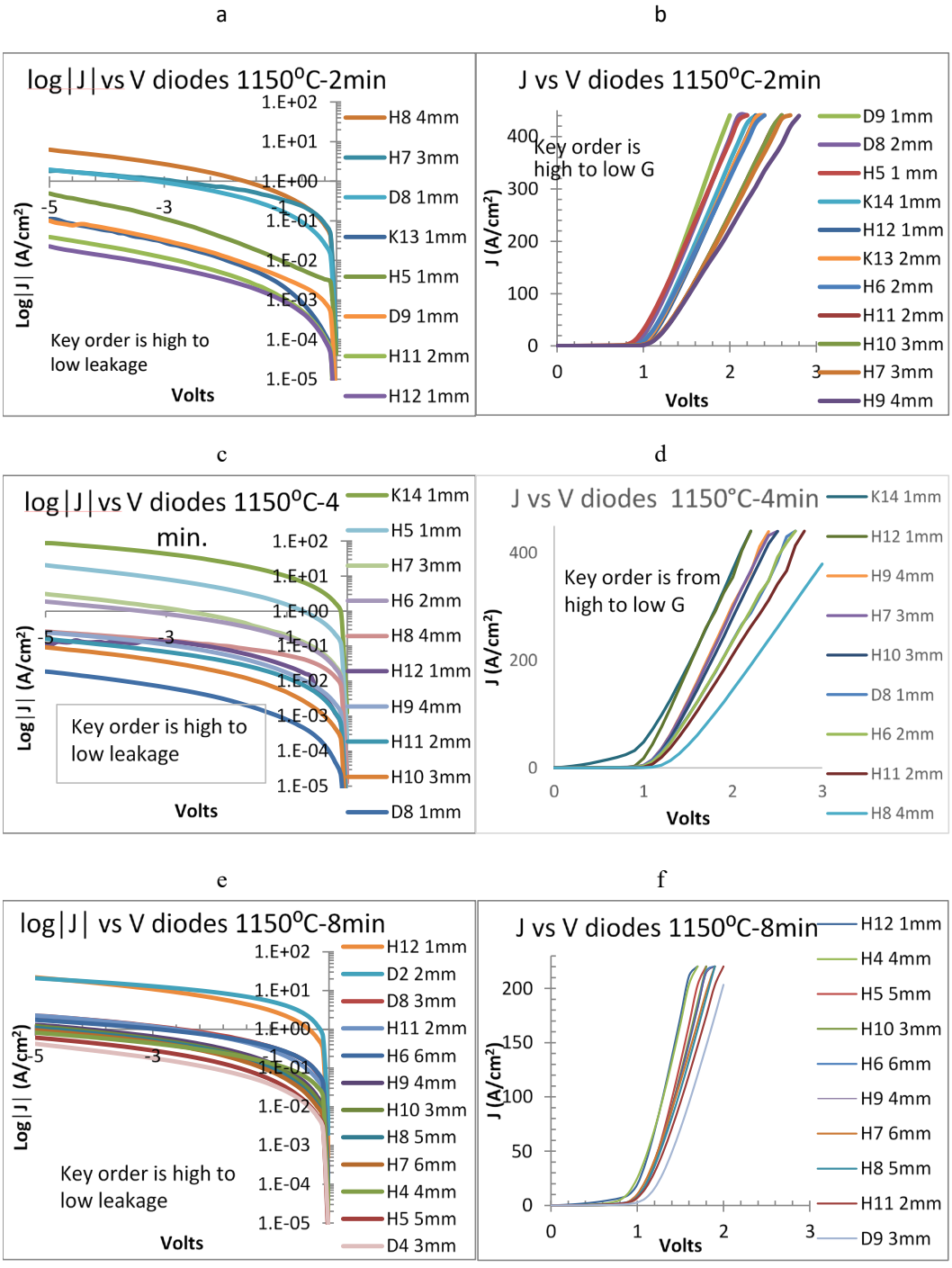


Fig. 7 J vs. V plots of diodes on 1150 °C annealed GaN diodes. a) Reverse 2 min, b) forward 2 min, c) reverse 4 min, d) forward 4 min, e) reverse 8 min, and f) forward 8 min

Figure 8a shows a reverse leakage after 1 min at 1200 °C that increases 4 orders of magnitude from 1×10^{-5}(AR) to 0.4 V at –5 V with little location dependence. At 1200 °C for 1 min H1 and H12, which are on the edge, have a V_K at 0.9 and 0.95, respectively, while the rest of the diodes annealed at 1200 °C for 1 min have a V_K of 1.1 or greater as seen in Fig. 8b. All of the diodes within 2 mm of the edge have the lowest V_K. All the plots appear to be parallel and the same G.

Figure 8c shows that the reverse leakages for the 2-min anneal are in the same range as they are for the 1-min anneal. Figure 8d shows all 170-µm diodes annealed at 1200 °C for 2 min had a V_K between 1 and 1.1 V with a median of 1.05 V. This smaller sample piece had a much-more-tightly-grouped set of forward IV plots where V_K and G had little variation.

The reverse leakage of 1200 °C 4-min diodes (Fig 8e) is an order of magnitude higher than the 2-min sample. Figure 8f forward JV of H1 and D2 have a V_K of 1 V while the rest of the diodes annealed at 1200 °C for 4 min have larger V_K with a median of 1.06 V. All but H1 are starting to have forward leakage increasing before V_K.

The reverse leakage of 1200 °C 8-min diodes (Fig. 8g) shows a pattern with the edge diodes having the lowest leakage, and the leakage increases with distance from the edge. All diodes annealed at 1200 °C for 8 min have a V_K grouped around 1.0 or greater as seen in Fig. 8h. The diodes have appreciable increases in conductance before V_K. The 1-min forward JV has an incrementally increasing V_K with similar G while the 2-, 4-, and 8-min diodes have a common V_K and distributed G.

Reverse leakage of 1250 °C at 1 min (Fig. 9a) was 6 orders of magnitude higher than AR and 1 order higher than were for the diodes that were annealed at 1200 °C. All diodes annealed at 1250 °C for 1 min had V_K greater than 1 V with a median of 1.15 V.

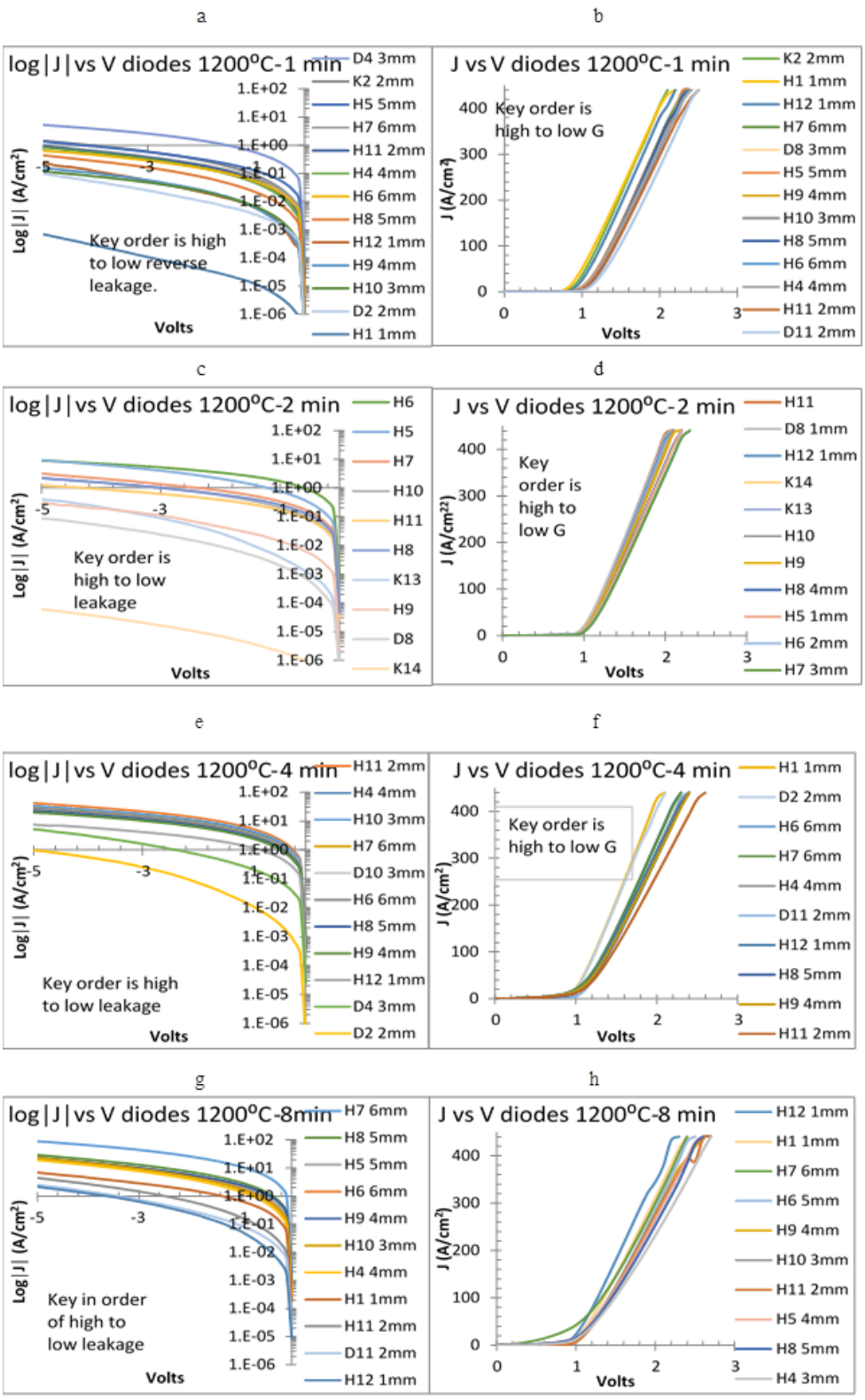


Fig. 8 J vs. V plots of diodes on 1200 °C annealed GaN diodes. a) Reverse 1 min, b) forward 1 min, c) reverse 2 min, d) forward 2 min, e) reverse 4 min, f) forward 4 min, g) reverse 8 min, and h) forward 8 min

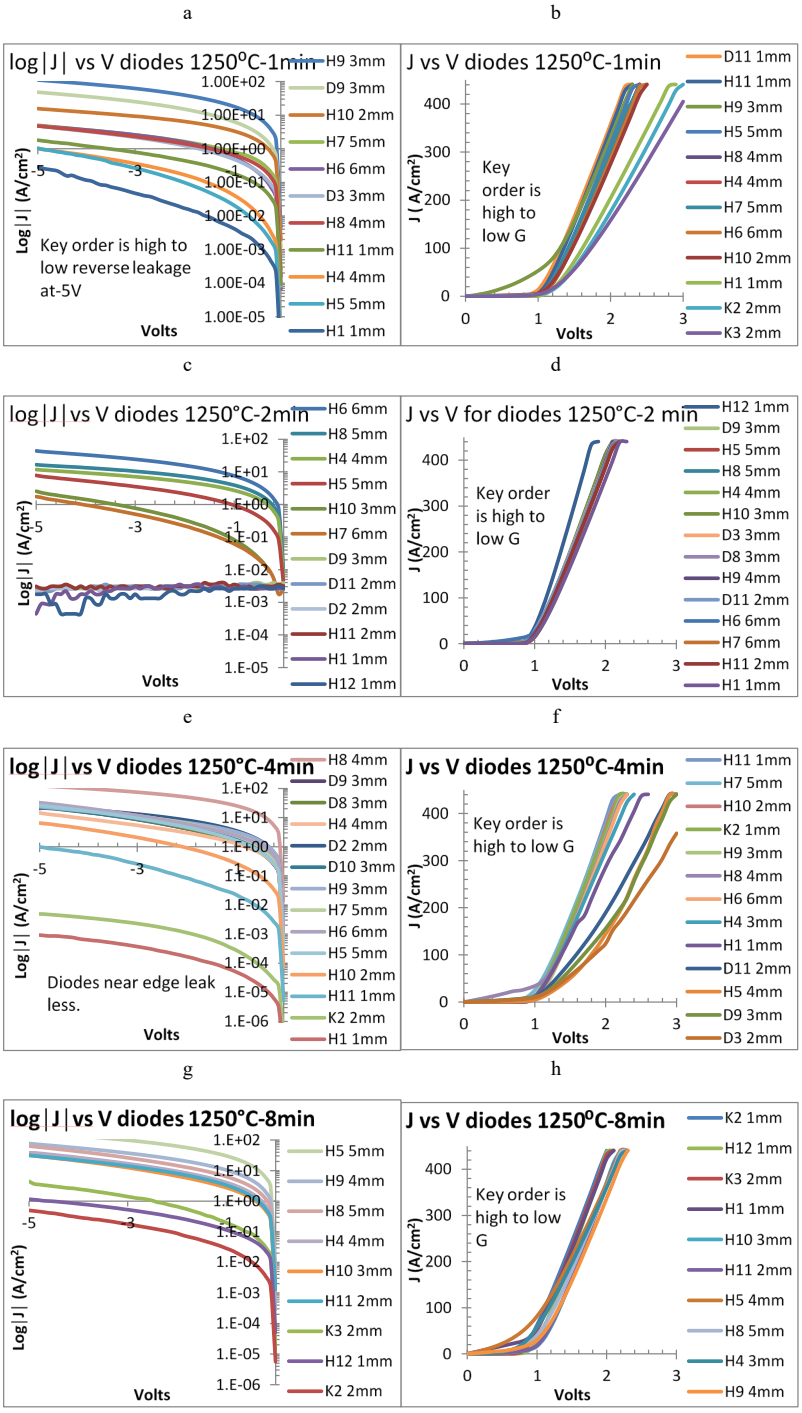


Fig. 9 J vs. V plots of diodes on 1250 °C annealed GaN diodes. a) Reverse 1 min, b) forward 1 min, c) reverse 2 min, d) forward 2 min, e) reverse 4 min, f) forward 4 min, g) reverse 8 min, and h) forward 8 min

The key of reverse JV is ordered by high to low leakage and gives distance from the edge. Figure 9c shows that the edge diodes have the lowest leakage and incrementally increase in leakage toward the center. The diodes annealed at 1250 °C for 2 min had V_K near 1 V. The forward IV curves appeared bunched together, but the center diodes had forward leakage increasing while the outer diodes appeared flat until the V_K as seen in Fig. 9d.

The 1250 °C 4-min edge diodes again have the lowest reverse leakage and the central diodes are grouped above 10 A/cm^2 as seen in Fig. 9e. There appears to be two groups of plots for this size. The H series are more conductive and have a 1.08 V V_K while the D series, which is nearer the corner, are more resistive and leak more before V_K.

Reverse leakage is progressed with time such that Fig. 9g shows central diodes leaking around 40 A/cm^2. Edge diodes, except for H1, had lower reverse bias leakage than the central or D series diodes. V_K is deceased to below 1 V while shorter anneals had V_K greater than 1 V. In Fig. 9h the diodes annealed at 1250 °C for 8 min had forward leakage before the V_K except for the edge diodes.

Figure 10a reverse leakage of H1 (near edge) was 15 A/cm^2 while the rest of the diodes measured above 80 A/cm^2 at –5V, which is greater than any lower temperature anneals. All the diodes annealed at 1300 °C for 1 min (Fig. 10b) are leaking in the forward direction before the V_K. The H series diodes are more conductive than the corner D series diodes.

Figure 10c 1300 °C 2-min diodes show edge diodes with lower reverse leakage than other diodes. Edge diodes leak less before V_K and have the highest G. Figure 10d diodes annealed at 1300 °C for 2 min had more leakage before the V_K than diodes annealed at 1 min. The IV plots are more spread out with V_K around 1 V and above.

The 1300 °C 4-min diodes have the lowest G (Fig. 10f) when compared to AR and all other anneals, but edge diodes still have highest G of this sample. Like the 1- and 2-min diodes, the 1300 °C 4-min (Fig. 10e) diodes near the edge have the lowest reverse leakage, but the rest are grouped together with a high reverse leakage.

Most diodes annealed at 1300 °C for 8 min had linear IV curves and thus did not show signs of rectification.

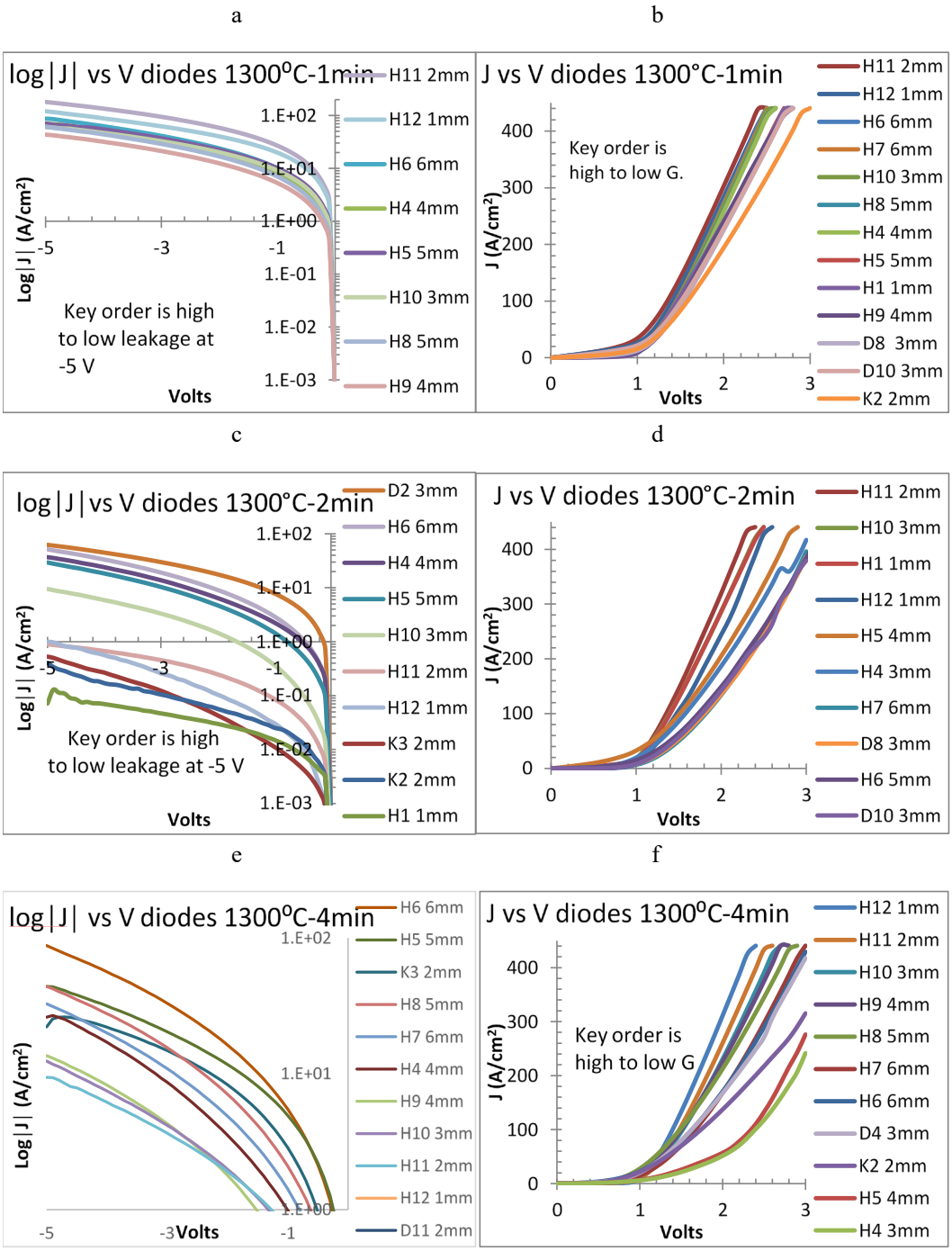


Fig. 10 J vs. V plots of diodes on 1300 °C annealed GaN. a) Reverse 1 min, b) forward 1 min, c) reverse 2 min, d) forward 2 min, e) reverse 4 min, and f) forward 4 min

3.4 Capacitance Voltage Measurements

Figure 4, the CV plot of N_d versus depth (μm) of the AR unintentionally doped HVPE GaN, reveals a decrease in carrier concentration from the bulk N_d of 5.3 × 10^{15} cm^{-3} (etched 220 nm) to 1.07 × 10^{15} cm^{-3} near the surface (0.3 μm).

The N_d plots for 1150, 1200, and 1250 °C for 1 and 2 min did not vary much from sample to sample so the plots are not given, but average values and standard deviation are given in Table 7. All annealed GaN was at least 1 order of magnitude higher N_d than AR diodes and the decreasing slope of N_d disappeared.

Table 7 Average N_d and standard deviation values for AR and 1150, 1200, and 1250 °C 170-μm diodes

T_A	1 min		2 min		4 min		8 min	
(°C)	Ave	Stdev	Ave	Stdev	Ave	Stdev	Ave	Stdev
AR	5.31E15	1.90E14	…	…	…	…	…	…
1150	…	…	4.41E16	1E16	4.28E16	8.8E15	5.00E16	7.5E15
1200	4.98E16	4.95E15	4.39E16	8.23E15	4.22E16	1.10E16	5.8E16	9.30E15
1250	5.05E16	3.10E15	5.14E16	4.24E15	5.65E16	1.17E16	5.41E17	6.65E17

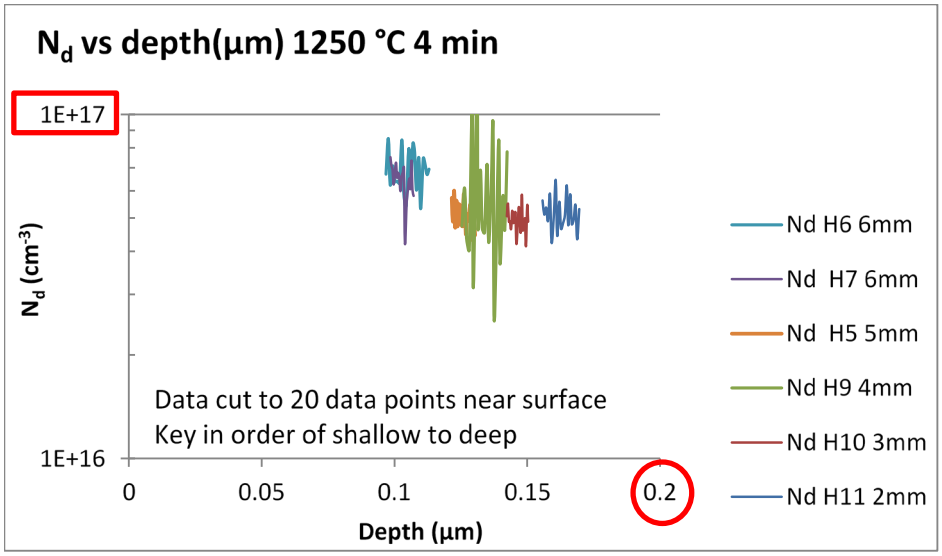
The N_d of the diodes at 1150 °C for 2, 4, and 8 min did not vary much from the mid 10^{16} cm^{-3} range, and the 2-min sample had a standard deviation of 1 × 10^{16} cm^{-3}.

The N_d of diodes at 1200 °C also stayed in the mid 10^{16} cm^{-3} range with 8 min having the highest average of 5.8 × 10^{16} cm^{-3} with a 9.3 × 10^{15} cm^{-3} standard deviation. The 8-min N_d plots had some variation with the central diodes having a slight slope to give an increase in N_d toward surface or measuring N_d with less depth.

N_d plots of diodes annealed at 1250 °C for 1 and 2 min were in the same mid 10^{16} cm^{-3} range as those annealed at 1150 and 1200 °C. The 4- and 8-min average N_d values are only slightly higher than 1 and 2 min, but the standard deviation is progressively 1 order or higher.

N_d plots of diodes annealed at 1250 °C for 4 min had an average value of 5.7 × 10^{16} cm^{-3} but that does not reveal how much the N_d plots changed. Figure 11a is plot of average N_d for diodes that shows a slight increase in N_d in diodes away from the edge. The edge diodes have level (constant N_d with depth) plots that are clearly lower, and measure deeper into the GaN bulk than the central diodes that have higher N_d as well as higher values near the surface.

a



b

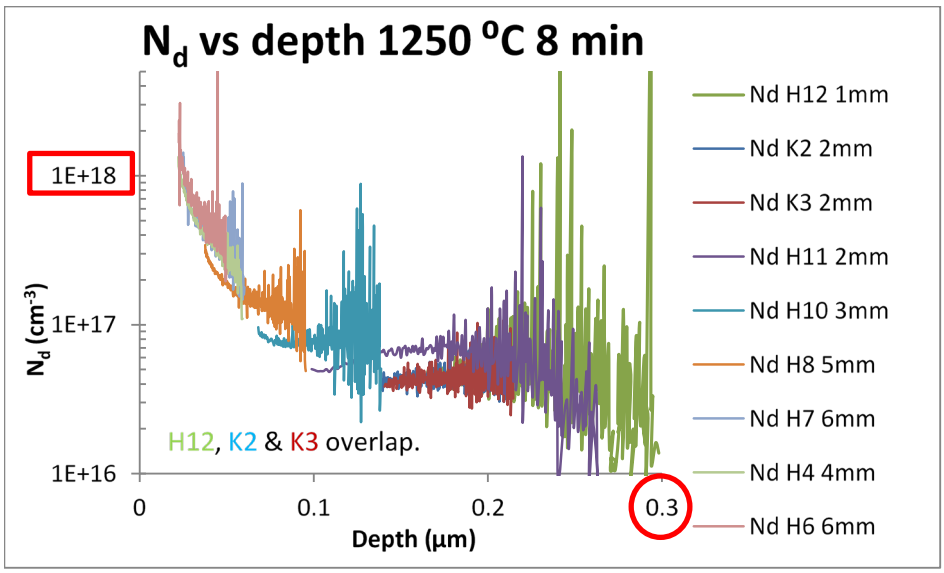
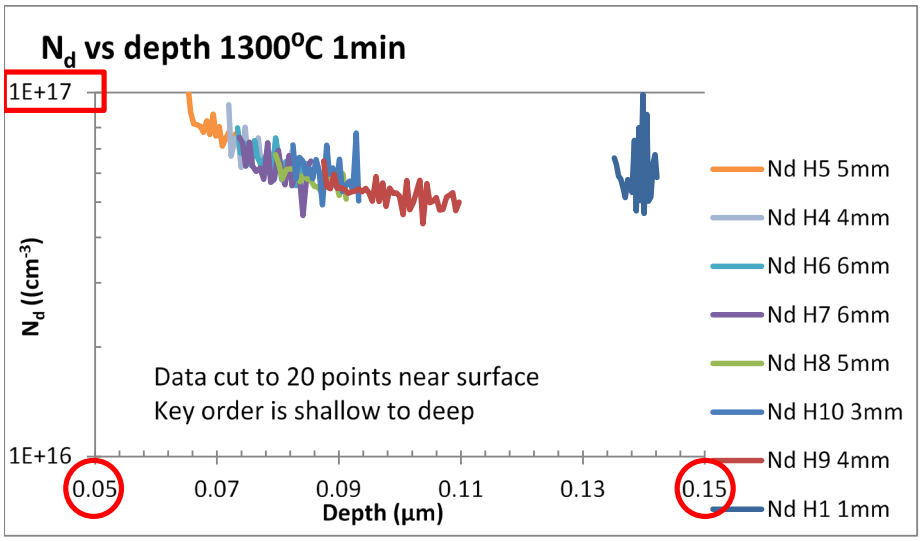


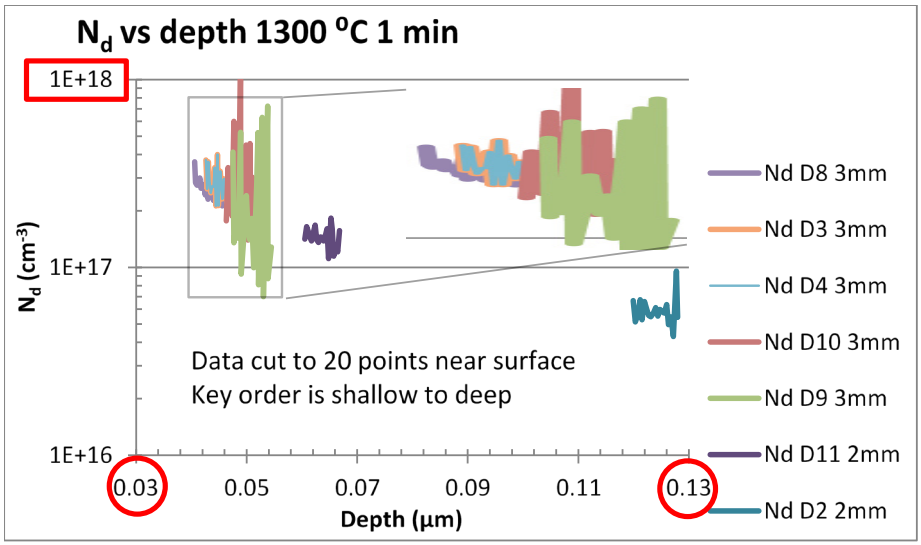
Fig. 11 CV data plots of N_d vs. depth for diodes annealed at 1250 °C for a) 4 and b) 8 min

N_d plots of diodes annealed at 1250 °C for 8 min (Fig. 11b) had an average N_d of 5.41×10^{17} cm^{-3}. These longer annealed diodes have even more pronounced difference in depth as they progress from edge to the center. The edge diodes have N_d values around 5×10^{16} cm^{-3} and a measured depth greater than 0.2 µm. The N_d plots incrementally increase with distance from the edge, and N_d values increase toward the surface. With more carriers to deplete, the interior diodes cannot measure N_d as deeply as edge diodes.

Diodes annealed at 1300 °C for 1 min had an average N_d of 9.2 × 10^{16} cm^{-3} (Fig. 12). Only H1 and D2 of the 170-µm diodes had N_d plots that did not slope up toward the surface, and they are all near the edge of the sample. All other N_d plots sloped upward and had progressively shorter length N_d plots.



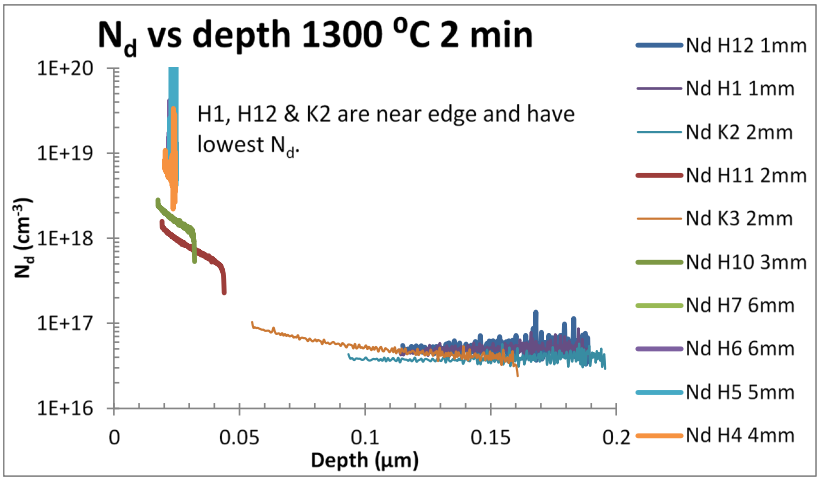
a



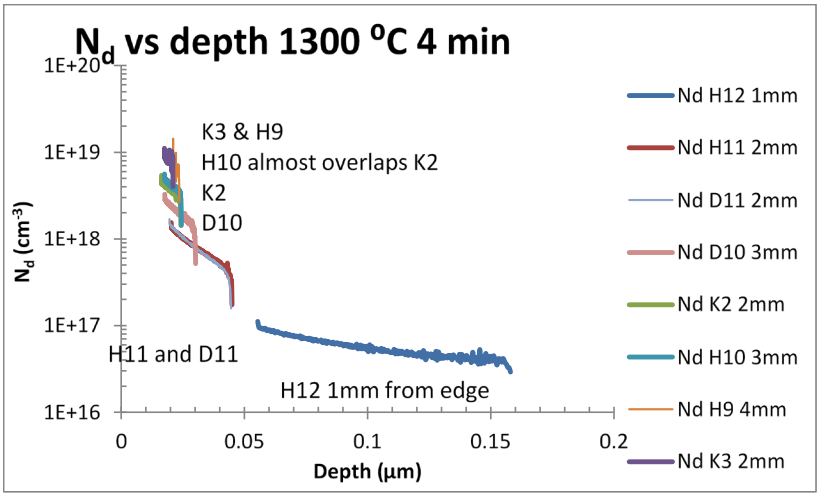
b

Fig. 12 N_d vs. depth for diodes annealed at 1300 °C for 1 min: a) H series and b) D series

Diodes that were annealed at 1300 °C for 2 min had N_d concentrations (Fig. 13a) that were around 5 × 10^{16} cm^{-3} near the edge. N_d plots for diodes incrementally increased in slope toward the surface as they moved away from the edge. The H series center diodes and the D series N_d plots are lumped together above 10^{18} at a depth of less than 0.03 µm.



a



b

Fig. 13 N_d vs. depth for diodes annealed at 1300 °C for a) 2 and b) 4 min

Diodes that were annealed at 1300 °C for 4 min had N_d values (Fig. 13b) that started around 5×10^{16} cm^{-3} near the edge and increased in slope to around 9×10^{16} cm^{-3}. N_d values for diodes incrementally increased in slope toward the surface as they moved away from the edge. The central diodes have the highest N_d values.

The diode structures that were annealed at 1300 °C for 8 min did not rectify, but they looked more like ohmic contacts.

4. Discussion

N_d plots of AR diodes showed that the surface of the GaN has lower carrier concentration near the surface and the bulk GaN has an N_d of 5×10^{15} cm^{-3}. A lower carrier concentration can explain a larger $Ø_b$, but changes in $Ø_b$ and V_K with location on an AR wafer are a challenge to interpret. Liu et.al.[7] characterized the

piezoelectric effects on GaN by hydrostatic and uniaxial stress on Schottky $Ø_b$. Piezoelectric effects could explain the change in V_K and $Ø_b$ with location from the edge. GaN, 10.5 μm thick, deposited on 430-μm sapphire around 1050 °C, has convex bows as the sample cools to room temperature. CTEs for GaN are 3.34 (300 K) to 4.05×10^{-6}/°C (700 K) and for sapphire are 3.9 (300 K) to 9.3×10^{-6}/°C (700 K).[10] GaN on sapphire has convex bow from cooling from the growth temperature of 1050 °C to room temperature. The biaxial compressive strain will cause a strain proportional to the Poisson ratio in the direction normal to the polar C plane. This strain normal to the polar C plane will cause a polarization charge. CTE, Poisson ratio, and Young's modulus are published at room temperature, but not for 400 up to 1300 °C for modeling stress and bow with Stoney's equation. The difference in CTE becomes appreciable with increasing temperature. The GaN is in compression (convex) when cooled from growth temperatures and should be in tension (concave) at any temperature above the 1050 °C growth temperature.

Stoney's equation assumes elastic deformation and stress is equally distributed in the sample. The V_K increase with distance from the edge is contrary to these assumptions. If V_K is dependent on piezoelectric effect of compressive stress, then the stress appears to be increasing with distance from the edge.

Plots of N_d versus depth of AR reveal a decrease in carrier concentration near the surface, which is where the HVPE has increased Si and O impurities. The carrier concentration was measured at 5×10^{15} cm^{-3} for AR, but all 1150 and 1200 °C annealed samples are measured to be 1 order of magnitude higher. The decreases in carrier concentration where the Si and O concentration increases do not meet expectations. The Si and O incorporated during cooling are apparently not activated dopants.

AFM images of the diodes annealed at 1150 and 1200 °C, which had step growth structures still visible, had lines of dislocations that were oriented along the intersection of the M-plane with the C-plane growth surface. These lines of dislocations are believed to be evidence of polygonization,[11] which is the migration of dislocations during annealing to form lower energy low-angle grain boundaries. It was also observed that Figs. 1i and 1o had deep trenches along these directions. The GaN appears to fail at these newly formed low-angle grain boundaries. The 1250 °C topographs with step growth structures did not show these fine etch pits. The 1250 and 1300 °C topographs that had no visible step growth structures (Figs. 1u, 1w, 1x, 1y, and 1z) had no M-plane trenches like in Figs. 1i and 1o but appeared to decompose with less preference for the M-plane.

Edge diodes in the AR leaked the most, but usually leaked the least in annealed diodes. Median reverse leakage increases with time for diodes annealed at 1150,

1200, and 1250 °C but decreases with time for those annealed at 1300 °C. CV showed that N_d increased appreciably for all but edge diodes when annealed at 1250 °C for 8 min and all 1300 °C anneals. The average N_d for 1150, 1200, and 1250 °C for 1 and 2 min stayed in the mid 10^{16} range. CV of these lower temperature anneals did not measure N_d below 110 nm, but a few of the 8-min central diodes showed N_d curving up near the surface. CV measures N_d at the end of the depletion layer. Increased N_d near the surface could explain decreases the N_d depth of depletion seen in 1150 and 1200 °C anneals for 4 and 8 min. Even though CV did not show N_d change for the low-temperature and time diodes, the increasing reverse leakage with time can be interpreted as a more sensitive measure of N_d increase near the surface/Schottky contact. The increase in Nd could be attributed to a number of complexes, stacking faults, or nitrogen vacancy (V_N). Any combination of these mobile defects allow the tunneling currents for reverse leakage.

AR diodes had the lowest V_K. Edge diodes at short anneal times at 1150 and 1200 °C had lower V_K than the interior diodes. All other annealed diodes had V_K between 1 and 1.2 with 1300 °C diodes having the highest V_K. The compressive stress of GaN films at room temperature would be expected to be greater for the higher temperature annealed samples. The ΔT for 1300 °C annealed samples is 1275 °C for calculating stress due to film CTE mismatch versus 1025 °C for the AR.

AFM topographs of central areas of 1200 °C 8-min and 1250 °C 4 and 8-min topographs did not have step growth structures visible, which can be interpreted as GaN degradation. All of these rough central areas coincide with having high reverse leakage and increased N_d. The N_d plots for diodes annealed at 1200 °C for 8 min and 1250 °C for 4 min have increased N_d, but still in the 10^{16} range. The 1250 °C for 8 min central areas have N_d in the 10^{17} range. All of the topographs of 1300 °C annealed samples had increased roughness and increased N_d values above 10^{16} range.

The AlN cap appeared to protect GaN surface before its removal. The room temperature KOH etch solution is selective for removing the low-temperature AlN film. The GaN C-plane has a dense hexagonal close-packed crystal structure with each Ga bond with three strong nitrogen bonds. After the KOH cap removal process, only the samples with increased N_d had increased roughness with no growth steps visible. This correlation might be attributed to N_d increases being V_N increases. With nitrogen bond loss, the GaN should be less selective to KOH and more easily etched.

Carrier concentration increases starting near the surface and progresses inward with time and high temperatures. If compressive stress in the AR can be correlated with

V_K and location, one might hypothesize that the stress increases from edge to center. With the interior diodes having progressively greater N_d with distance from the edge when annealed at high temperatures and longer times, one could deduce that increasing tensile stress with distance from the edge is a cause mechanism for the increased carrier concentration. Tensile stress contributes to the potential energy of high-temperature annealing to promote bond breaking and lead to nitrogen loss.

Median reverse leakage was seen to increase with time for the 1150, 1200, and 1250 °C annealed diodes, but decreased with time for diodes annealed at 1300 °C. The CV plots for central diodes of 1250 °C for 8 min and all 1300 °C times had near surface N_d values in the high 10^{18} to 10^{19} range. N_d increase in the beginning decreases resistance, but eventually reaches a point where it increases resistance. The maximum in median G was found to be at 8 min for the 1150 °C and 2 min for 1200 and 1250 °C, while 1300 °C diodes had maximum at 1 min. The 1300 °C diodes had the lowest median G in the range 229 to 271 A/cm^2/V, which is as low as the AR value of 262A/cm^2/V. The decrease in median reverse leakage for the 1300 °C diodes with time can be attributed to N_d values high enough to increase resistance.

5. Conclusions

Reverse leakage current increases with increased time and temperature for GaN annealed at 1150, 1200, 1250, and 1300 °C. This increased reverse leakage current appears to correlate well with increased N_d. The surface roughness increase coincides with increased N_d. Apparent loss of GaN KOH selectivity with increased N_d suggests that N_d increases are V_N increases. V_K is affected by the location from the edge for unannealed and annealed GaN. V_K variation is believed to be a function of piezoelectric effects on $Ø_b$ from stress variations from center to edge. Progressive increases in N_d with distance from edge are attributed to tensile stress increases toward the center and this stress induces accelerated nitrogen loss.

The edge diodes survived with appreciably less nitrogen loss than interior diodes, which gives proof that the AlN cap works. However, future annealing studies should be done on homoepitaxial GaN substrates to reduce high-temperature tensile stress accelerated decomposition caused by the sapphire substrate with appreciably higher CTE.

6. References

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List of Symbols, Abbreviations, and Acronyms

2DEG	two-dimensional electron gas
AFM	atomic force microscopy
Al	aluminum
AlN	aluminum nitride
AR	as-received
ARL	Army Research Laboratory
CTE	coefficient of thermal expansion
CV	capacitance-voltage
G	conductance
GaN	gallium nitride
HEMT	high electron mobility transistor
HVPE	hydride vapor phase epitaxy
IV	current-voltage
JV	current density-voltage
KOH	potassium hydroxide
N_d	carrier concentration
O	oxygen
$Ø_b$	barrier height
RMS	root mean square
Si	silicon
SiC	silicon carbide
t_A	annealing time
T_A	annealing temperature
V_K	knee voltage
V_N	nitrogen vacancy

1 (PDF)	DEFENSE TECHNICAL INFORMATION CTR DTIC OCA
2 (PDF)	DIR ARL IMAL HRA RECORDS MGMT RDRL DCL TECH LIB
1 (PDF)	GOVT PRINTG OFC A MALHOTRA
1 (PDF)	ARL RDRL SED E M DERENGE