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US Army Research Laboratory

Thermal Evaluation of Isolated Gate Driver for Bidirectional Power Inverter

by Miguel Hinojosa

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14. ABSTRACT
This work reports on the steps taken to evaluate a commercially available, half-bridge gate-driver board that is considered as a possible subcomponent of a 60-kW class inverter. Initial results validate the board's operation at the expected frequency while switching a silicon-carbide (SiC), half-bridge, metal-oxide-semiconductor field-effect transistor (MOSFET) module at elevated voltage and current levels with a simulated load. The board was successfully tested at 100 kHz, at room temperature, while driving a 1.7-kV, 8.0-mΩ, SiC module in a half-bridge circuit under various loading conditions. For a supply voltage of 600 V and a load of 25 Ω, for example, the maximum temperature recorded on the board was 55.2 °C with a ΔT of 33.9 °C. The preliminary thermal tests presented here, although not conclusive, suggest the gate-driver board can be used for the intended application without any modifications to the onboard components and without the need of additional cooling hardware.

15. SUBJECT TERMS
silicon carbide, SiC, bidirectional, inverter, metal-oxide-semiconductor field-effect transistor, MOSFET, thermal

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1. Introduction

The goal of this project was to evaluate a commercially available, half-bridge gate-driver board and determine the feasibility of using it as a subcomponent of a compact, air-cooled, 60-kW class inverter. This inverter would serve as a bidirectional power interface between a mobile power system and a terrestrial power system. The key specifications of the inverter are as follows:

- 60-kW bidirectional and symmetric power conversion
- Port A: 208-VAC, 3-phase, 5-wire
- Port B: 600 VDC
- Galvanic isolation between Port A and Port B
- Active-neutral techniques (unbalanced loading)
- Stand-alone and grid-connected operating modes
- Waste heat dissipated to ambient air
- Compliant to MIL-STD-461E,[1] MIL-STD-810G,[2] MIL-STD-1472F,[3] two-person lift (74 lb), and MIL-PRF-GCS600A[4]

While this inverter was being designed and built, a subtask of the project was to verify that the dual-channel, differential isolated gate-driver board, which is expected to control the various silicon carbide (SiC) switches in the system, operated properly at 100 kHz at ambient temperature without the need for complex cooling hardware. This work describes the steps taken to validate the board's operation at the expected frequency, while switching a SiC half-bridge, metal-oxide-semiconductor field-effect transistor (MOSFET) module at elevated voltage and current levels with a simulated load. This technical report is organized with the following sections: evaluation of board interface and specifications, SiC module details, initial PSPICE-program simulations, laboratory evaluations, and summary and conclusions.

2. Board Interface and Specifications

Figures 1 and 2 show the front and back sides of the CGD15HB62LP driver board with highlights of its important components. The board is powered by applying regulated, 12-VDC at Pins 1 and 2 of the 16-pin connector. From these two contacts the power is distributed to a pair of 3-W MGJ3T12150505 isolated DC-DC converter modules (Vout = +18 V, –5 V), then to the dual IXDD614YI gate driver

integrated circuits (ICs), the ISO7842 opto-isolators, all logic chips, and the rest of the auxiliary components. Pins 3 and 4 of the 16-pin connector are the high-side (HS) switch differential inputs, while Pins 5 and 6 are the low-side (LS) switch differential inputs. Pins 7 and 8 are used to detect faults, Pins 9 and 10 are for resistance-temperature-detector (RTD) measurement, and Pins 11–16 are to enable/disable the DC-DC converter power supplies, the opto-isolators, and the overcurrent monitors. (Additional details are found in a datasheet.[5]) The front side of the board also contains two terminals, JT1 and JT3, which needed attention for proper operation. The JT1 terminal feeds the HS overcurrent protection circuit, and it was connected from the top blade connector to the DC+ bus using 22-AWG stranded wire. The JT3 terminal feeds the LS overcurrent protection circuit, and it is internally connected by populating RT19 with a 0-Ω resistor.

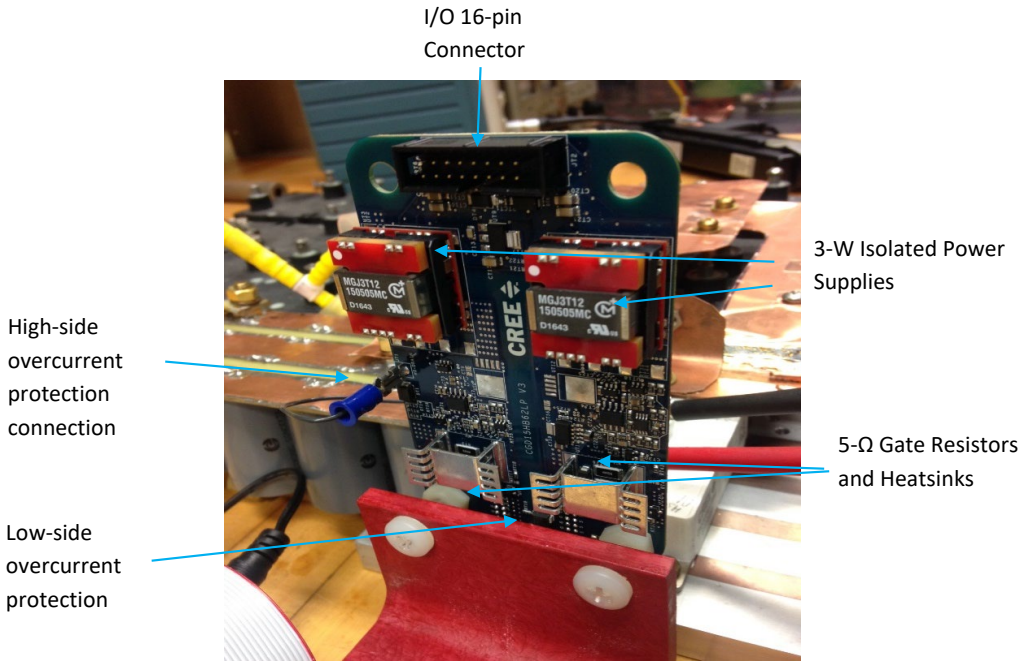

Fig. 1 Front side of the half-bridge gate-driver board

The gate driver board was supported vertically by using an L-bracket made from red fiberglass, as seen in Fig. 2. The board's gate-to-source output headers were then converted to blade connectors using an FR4 daughter board, which was mounted above the SiC MOSFET module. The driver board was mounted in close proximity to the switch module to reduce the parasitic resistance and inductance, and it was oriented vertically to permit access to the thermal camera.

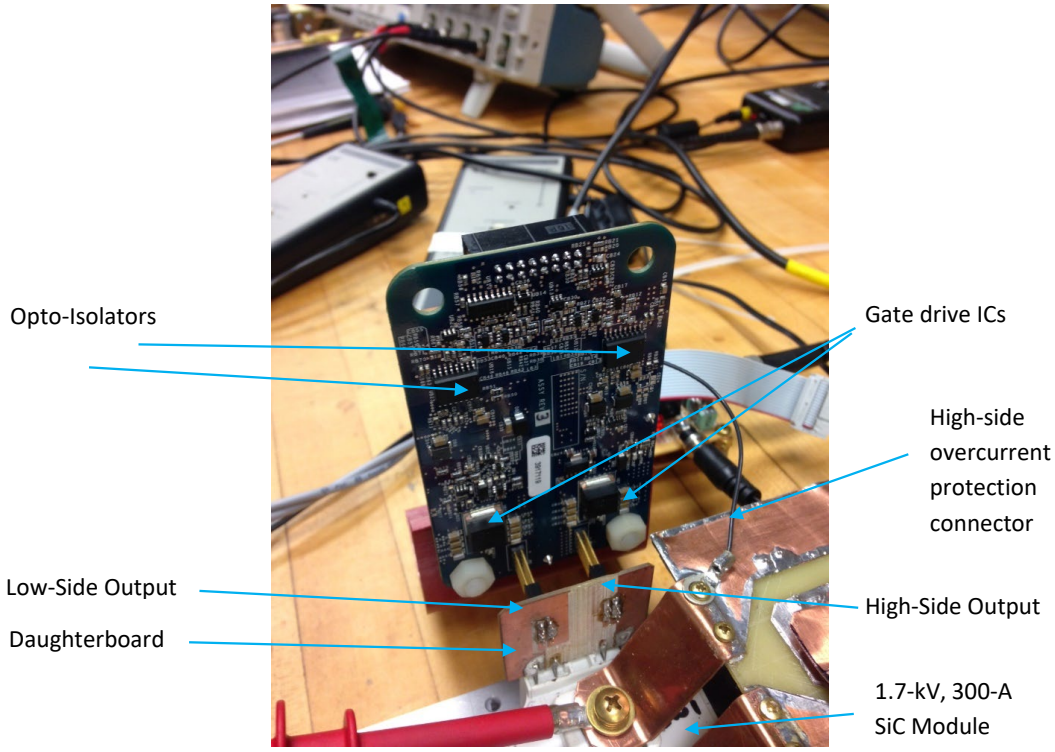

Fig. 2 Back side of the driver board

The differential inputs, which are typically used in automotive applications, are beneficial because of the increased noise immunity. However, in order to properly trigger Pins 3 and 4 for the HS and Pins 5 and 6 for the LS, respectively, a single-ended-to-differential converter board was built. Figure 3 shows the board that was built in the lab to provide BNC-connector, single-ended-to-differential conversion using the AM26LS31 IC, as well as to route power from the regulated 12-VDC supply to the gate-driver board via Pins 1 and 2 of the 16-pin connector.

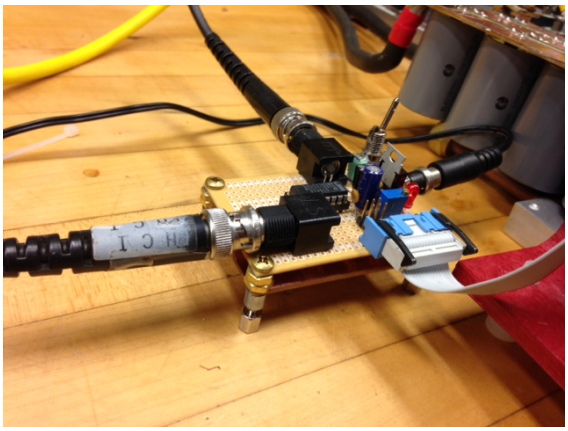

Fig. 3 Single-ended-to-differential converter board

3. SiC Module Details

In the inverter application, the gate-driver unit will be switching a CAS325M12HM2, 1.2-kV, 3.7-mΩ, 350-A SiC high-performance half-bridge module. However, due to availability and cost, a surrogate module was used in this evaluation. The test's surrogate was a CAS300M17BM2, 1.7-kV, 8.0-mΩ, 300-A SiC half-bridge module, which has similar gate characteristics, but higher on-state resistance *Rds(on),* switching losses, and avalanche breakdown voltage. Figure 4 shows an image of the 1.2-kV SiC module on the left side and the 1.7-kV SiC module on the right side.

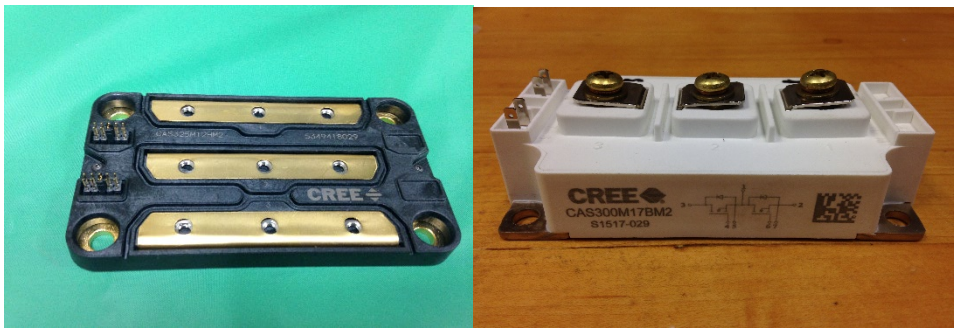

Fig. 4 A 1.2-kV, 3.7-mΩ, 325-A module (left) and a 1.7-kV, 8.0-mΩ, 300-A module (right)

The gate charge Q_G versus gate-to-source voltage *Vgs* plots found in the manufacturer's datasheets[6,7] were used to approximate the power requirements for the gate driver board. For the 1.2-kV module, the total gate charge was about 1200 nC when *Vgs* was 18 V with a drain current of 350 A and a drain-to-source *Vds* of 800 V. For the 1.7-kV module, the total gate charge was close to 1000 nC when *Vgs* was 18 V with a drain current of 300 A and a drain-to-source *Vds* of 900 V. Because the testing conditions were not the same to obtain these plots, the following assumptions were made. Figure 5 shows the effects of varying drain-source voltage *Vds* (left) and drain current *Id* (right) on generic gate-charge curves. In the first case, *Vds* is varied and *Id* is held constant (Fig. 5, left). The higher *Vds* results in a lower slope, which means more gate charge is needed to reach the overdrive voltage *Vgs*. In the second case, *Id* is varied and *Vds* is held constant (Fig. 5, right). An increase in *Id* causes a change in the Miller plateau, but shows less drastic effects on the final slope, which ultimately determines the total gate charge needed. Based on these observations on generic plots, and referring to the Q_G versus *Vgs* plots in the datasheets, although the two graphs do not show the same testing conditions (e.g., voltage and current), both plots show a *Vds* value greater than 600 V and *Id* greater than 100 A, which are expected in the inverter application. Therefore, assuming *Vds* will be less than 800 V and *Id* less than 300 A, the total gate charge Q_G will be below 1200 nC for an overdrive voltage of 18 V. Using this value as the

upper limit, the maximum gate-driver power requirements can be determined by the calculations in Eq. 1. At 100 kHz, the calculated power is 2.76 W, which will be provided by the 3-W isolated DC-DC converter in the CGD15HB62LP gate-driver board.

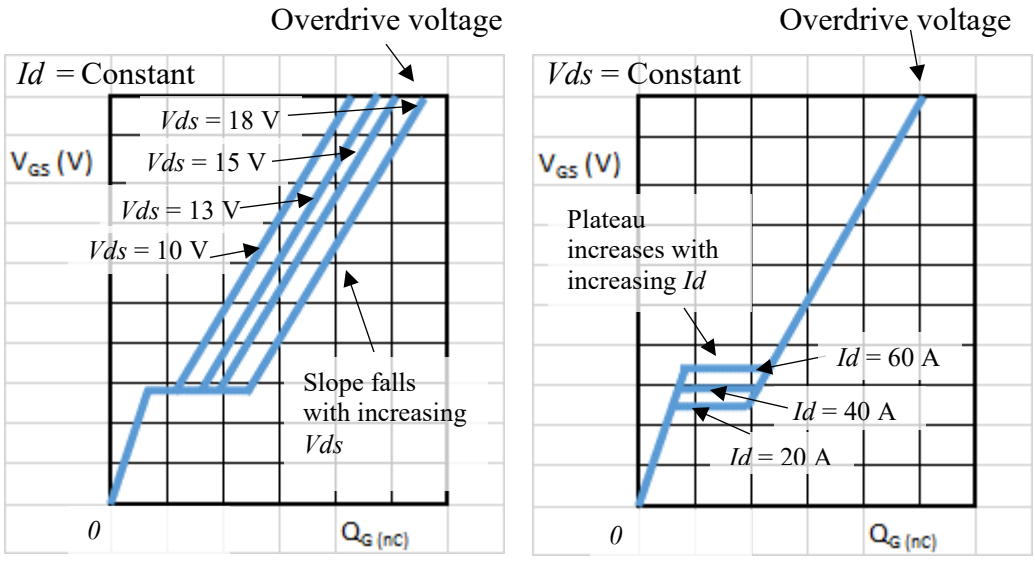

Fig. 5 Effects of voltage (left) and current (right) on generic gate-charge graphs

Gate charge power calculations

$$Q_{total} := 1200nC \qquad F_{sw} := 100kHz$$

$$V_{ghigh} := 18V \qquad V_{glow} := -5V \qquad \Delta V_g := V_{ghigh} - V_{glow} = 23\,V \tag{1}$$

$$P_{sw} := Q_{total} \cdot F_{sw} \cdot \Delta V_g = 2.76\,W$$

4. Simulations

The gate-driver switching strategy was implemented with a PSPICE SiC module and simulated using ORCAD Capture software. The half-bridge circuit (Fig. 6) that was used resembles a single-phase DC-AC inverter, except that in this case the load was mostly resistive. As in a typical half-bridge configuration, the DC supply feeds a capacitor bank, the drain of the HS MOSFET is connected to the high potential, and the source of the LS MOSFET is tied to ground. The midpoint of the module

feeds the resistive load, and the load's return path is connected to the midsection of a capacitive divider. This load configuration ensures that both switches run current through the load during alternating cycles. The gate drivers were simulated using independent voltage sources *Vpulse* (labelled Vgate in circuit) and the two drivers were configured to be out of phase at approximately 180° with a dead time greater than 100 ns. The simulated HS driver was isolated using a voltage-controlled voltage source *E* with a gain of 1. SPICE models for the CAS300M17BM2 or the CAS325M12HM2 were not available from the manufacturer, but with the use of the C2M0045170P single-device SPICE model, a module model was created. This 1700-V, 45-mΩ MOSFET was configured in parallel to obtain approximately 9 mΩ, which is close to the 8-mΩ resistance of the CAS300M17BM2 module. The subcircuit for the MOSFET module is displayed in Fig. 7.

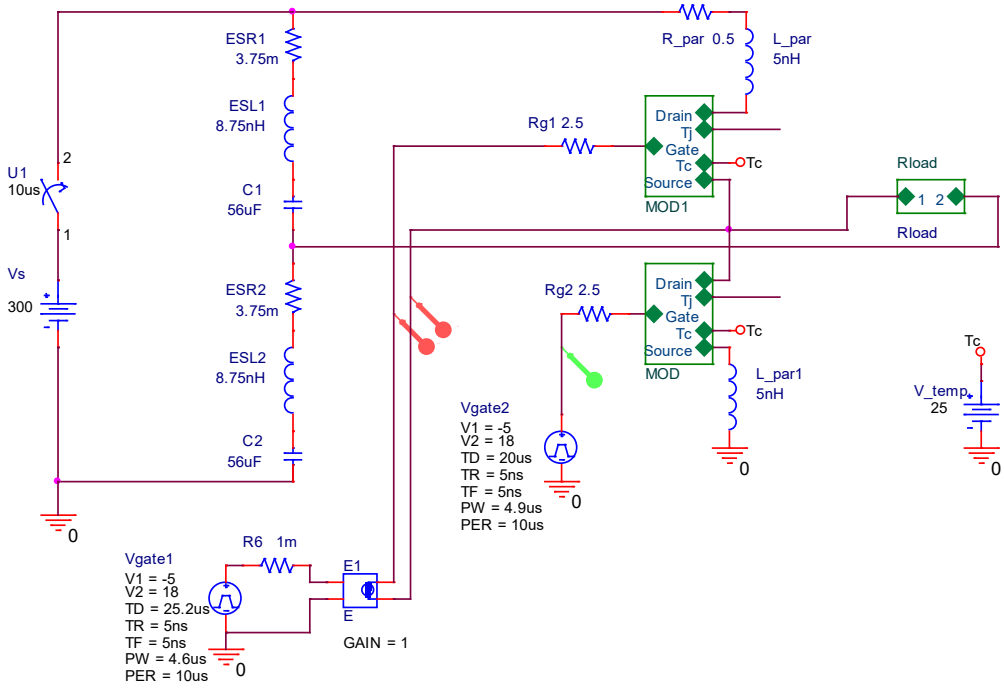

Fig. 6 Half-bridge evaluation circuit

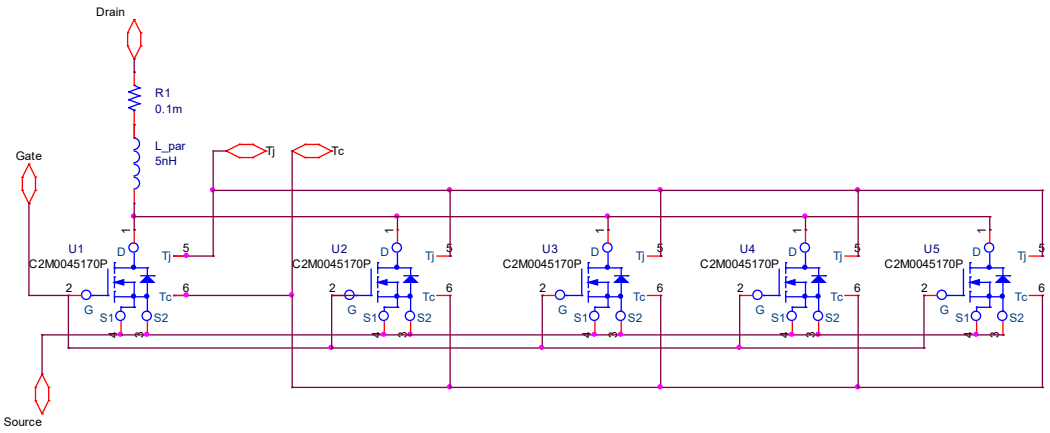

Fig. 7 Simulated 9-mΩ module with five 45-mΩ devices

The PSPICE simulations were run with 300-V and 600-V power-supply voltages and load resistances of 12.5 Ω and 25 Ω, respectively. Figure 8 shows the load circuit and simulation results at 300-V for the LS MOSFET, HS MOSFET, and the load. The load was simulated using groups of 50-Ω resistors, which were later used during the actual lab measurements. For the case where the load was 12.5 Ω and *V_supply* was 300 V, the LS *Vds* swing was from 88 mV to 294 V and the *Id* swing was from 12 A to 0 A. The average power for the LS switch was 5.5 W and the switching losses were 1.4 µJ during turn-on and 1.7 µJ during turn-off. The HS *Vds* swing was from 300 V to 84 mV and the current Id swings from 11.6 A to 0 A. The average power was 4.6 W and the switching energy losses were 1.2 µJ during turn-on and 1.1 µJ during turn-off. Based on these simulation results, it was determined that the switching and conduction losses could be easily handled by the integrated heatsink of the module and therefore no additional cooling or heatsinks were required. On the load side, the voltage swings were from –149 V to +145 V, which turned out to be asymmetric due to the slightly different delays in the pulse-width modulated (PWM) signals triggering the HS and LS MOSFETs and slightly below ±150 V due to losses. The current swing at the load was from –12 A and +11.6 A, and the total average power was approximately 1.5 kW. The simulation was also used to determine the average power per resistor, which was close 360 W, to determine if the lab modules would be able to dissipate this amount of heat. The TA1K0PH50R0K 50-Ω resistors from Ohmite were rated for 1 kW, so for this 300-V case, the load configuration was adequate.

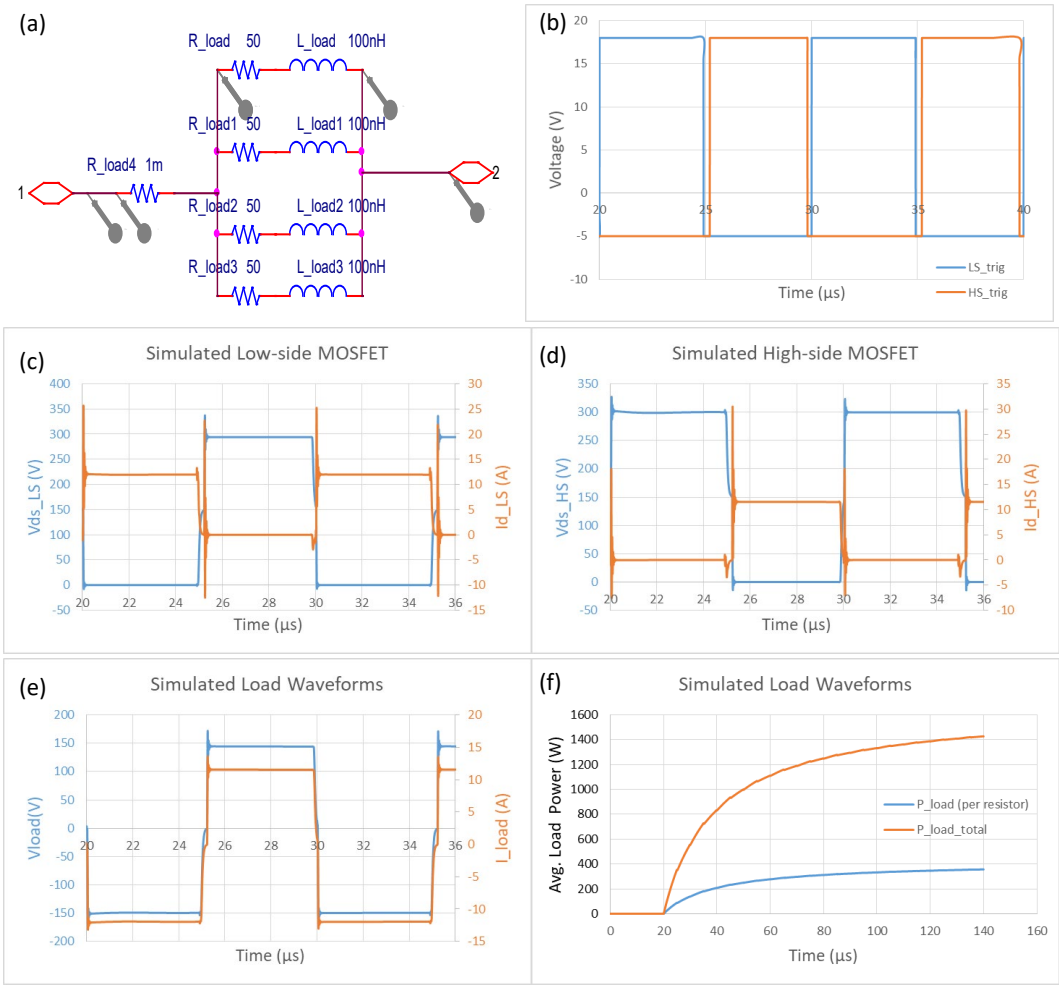

Fig. 8 a) Circuit with 12.5-Ω load and 300-V supply, b) gate-trigger signals with delays to prevent shoot-through, c) LS *Vds* and *Id*, d) HS *Vds* and *Id*, e) load voltage and current, and f) power dissipation at the load

Figure 9 shows the load circuit and simulation results where the supply voltage was 600 V and load was 25 Ω. In this case, the LS *Vds* swing was from 100 mV to 595 V and the *Id* swing was from 11.5 A to 0 A. The average power for the LS switch was 14 W and the switching losses were 1.53 µJ during turn-on and 4.3 µJ during turn-off. The high-side *Vds* swing was from 600 V to 86 mV and the current *Id* swings from 11.6 A to 0 A. The average power was 10.6 W and the switching energy losses were 2.3 µJ during turn-on and 1.7 µJ during turn-off. On the load side, the voltage swings were from –303 V to +292 V and the current swing was from –11.5 A and +11.6 A. The total average power was approximately 2.67 kW and the average power per resistor was 335 W.

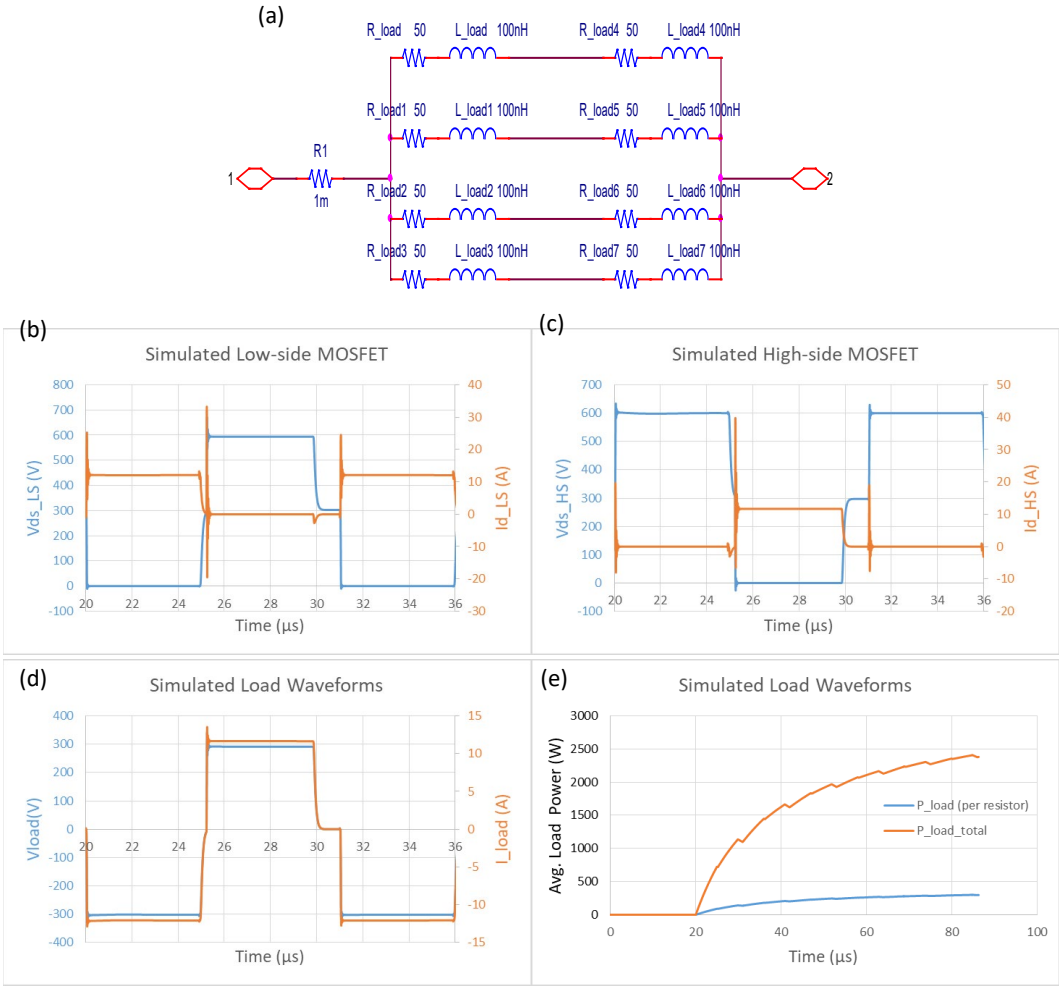

Fig. 9 a) Circuit with 25-Ω load and 600-V supply, b) LS *Vds* and *Id*, c) HS *Vds* and *Id*, d) load voltage and current, and e) power dissipation at the load

5. Lab Evaluations

The previously simulated circuits were implemented in the laboratory to demonstrate the operation of the CGD15HB62LP gate-driver board at 100 kHz with a MOSFET module under various loading conditions. Figure 10 shows this evaluation testbed along with the test equipment used to take measurements. Two synchronized Agilent 33220A function generators created the complementary HS and LS PWM signals that fed into the single-ended-to-differential converter board. From this point, the differential signals, along with the 12-V power bus, were connected to the gate-driver board using the 16-pin input/output ribbon cable. The gate-driver board sat on top of the CAS300M17BM2, 1.7-kV, 8.0-mΩ, 300-A SiC half-bridge module and connected to the HS and LS gate-source connectors. The MOSFET module terminals were connected to the Ohmite TA1K0PH50R0K 50-Ω

load resistors and to the cluster of Electronic Concepts UP36 900-V, 14-µF (×8) capacitors using 23-mil copper bus bars. Two Yokogawa 701926 differential probes measured the *Vds* voltages and a CWT 03LFB Rogowski coil-current sensor measured the current at the load. A 3-phase, 480-V, 15-kW, Sorensen Model 800/19 power supply provided the input voltages and an ANOVA A40 refrigerated circulator cooled the heatsinks of the module and load. Finally, a Fluke TiS65 infrared camera monitored and recorded the temperature change in the gate-driver board.

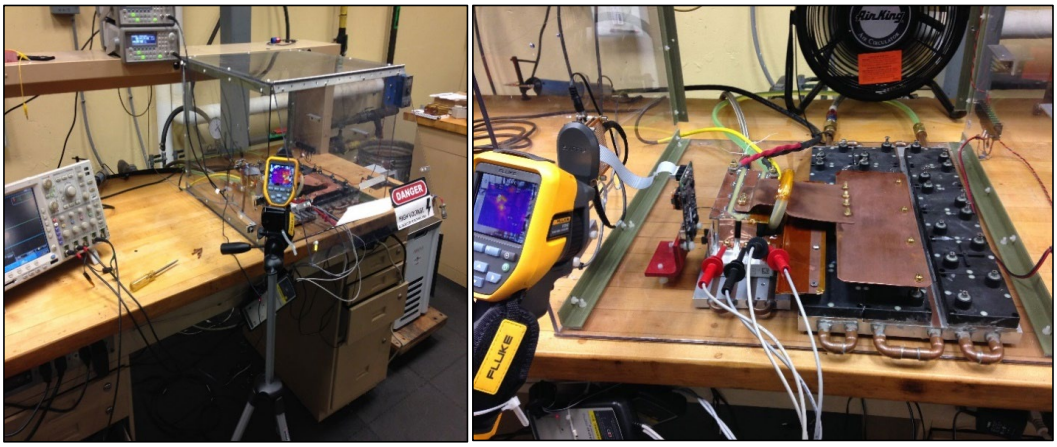

Fig. 10 Images of the gate-driver testbed

A low-voltage safety test was first performed to ensure the circuit behaved as simulated, to verify that the PWM signals were correct, and to observe if any shoot-through was taking place during the switching cycles of the LS and HS MOSFETs. The test was successfully executed and Table 1 summarizes the results when the supply voltage was set to 100 V. Figure 11 shows the waveforms taken with the oscilloscope of the LS and HS *Vds* voltages and the load current *I_load*. Figures 12 and 13 show thermal-camera images of the back and front sides of the CGD15HB62LP. Figure 14 displays a plot of the temperature versus time while the thermal camera was focused on the two IXYS gate-driver ICs. Figure 15 shows the temperature-versus-time graph of the front side while the camera was focused on the two gate resistors. The maximum temperature recorded on the board was 52.1 °C, which occurred on the front-side, with a ΔT of 29 °C.

Table 1 Summary of results for Test 1

Test conditions
V_supply = 100 V
I_supply = 1.9 A
P_supply = 190 W
I_load= –4 A, +4 A
V_gate = +18 V, –5 V
Frequency = 100 kHz, *Dty* = 50%
R_load = 12.5 Ω
Test time: 5 min

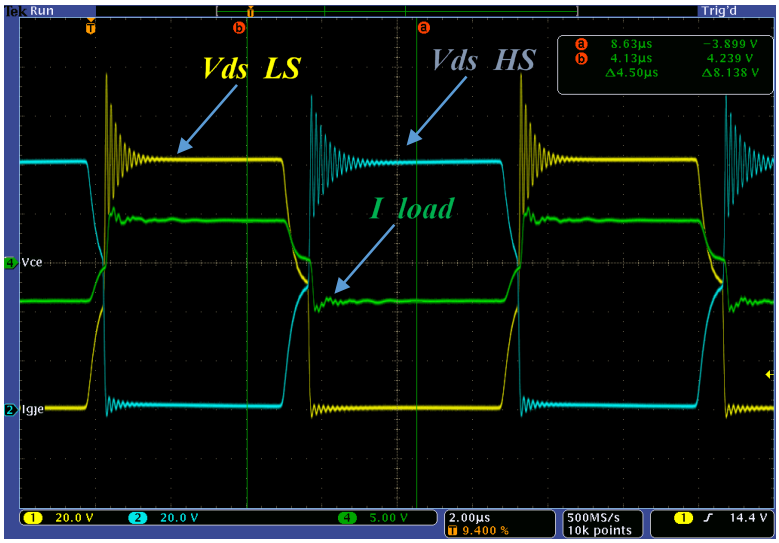

Fig. 11 Switching waveforms of the half-bridge module and load when *V_supply* was 100 V

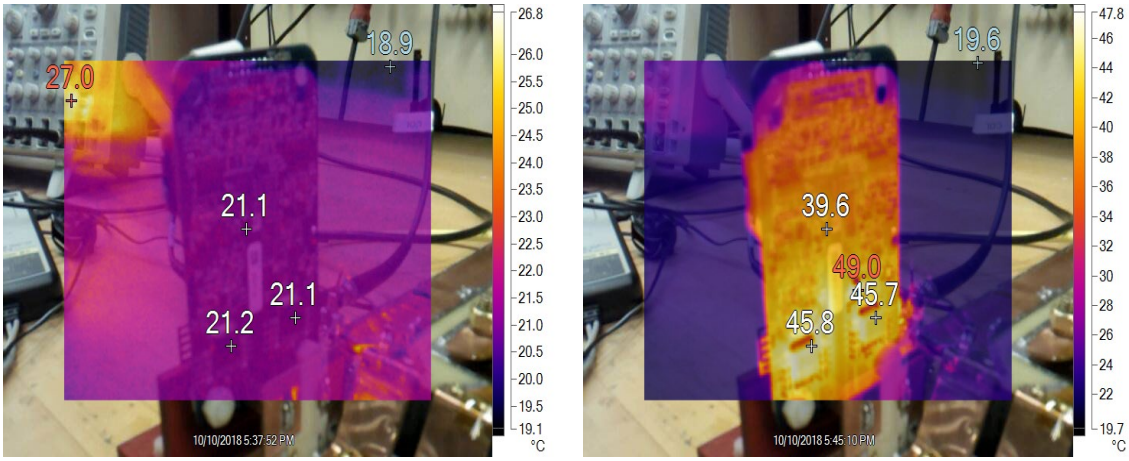

Fig. 12 Initial (left) and final (right) temperature measurements of the back side of the driver board when *V_supply* was 100 V

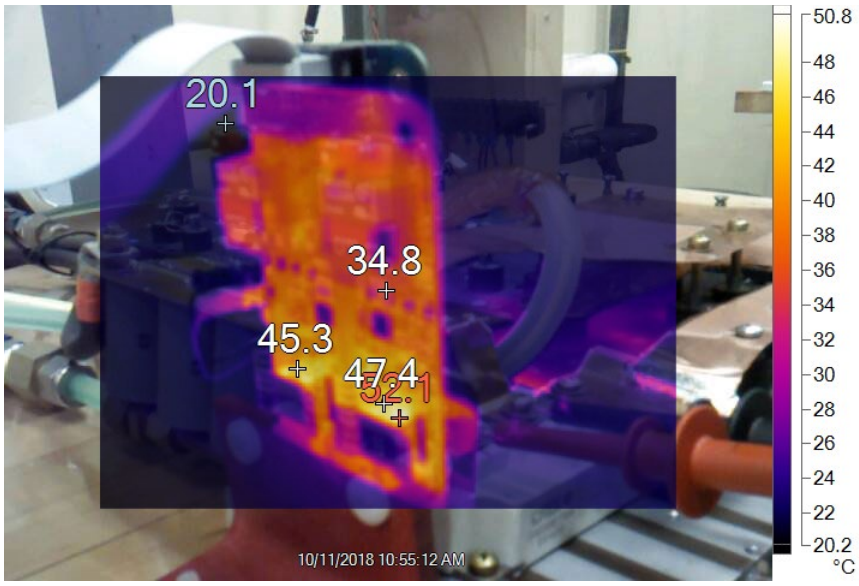

Fig. 13 Final temperature measurements of the front side of the driver board when *V_supply* was 100 V

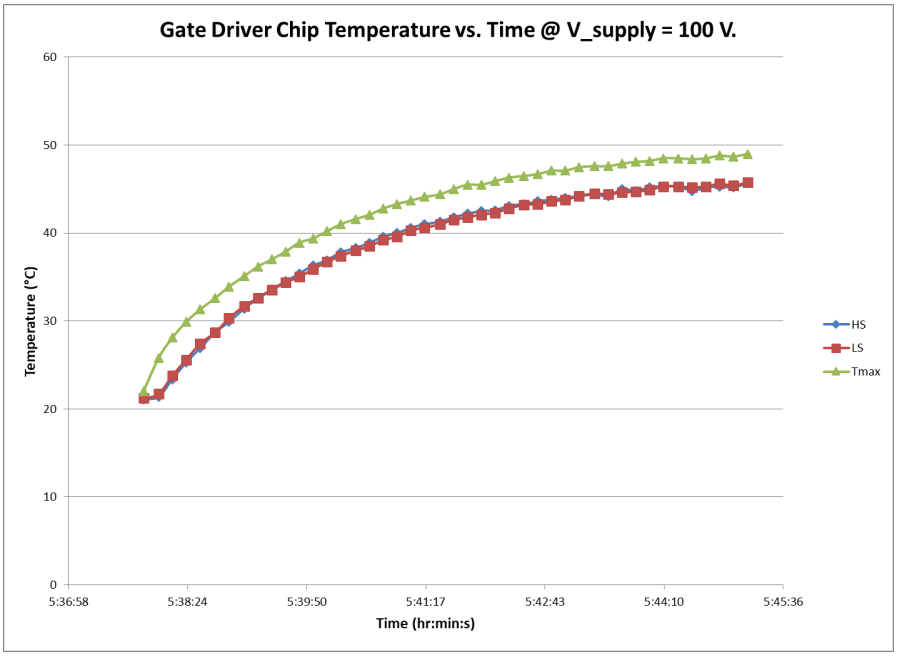

Fig. 14 Back-side temperature measurements for gate-driver ICs when *V_supply* was 100 V

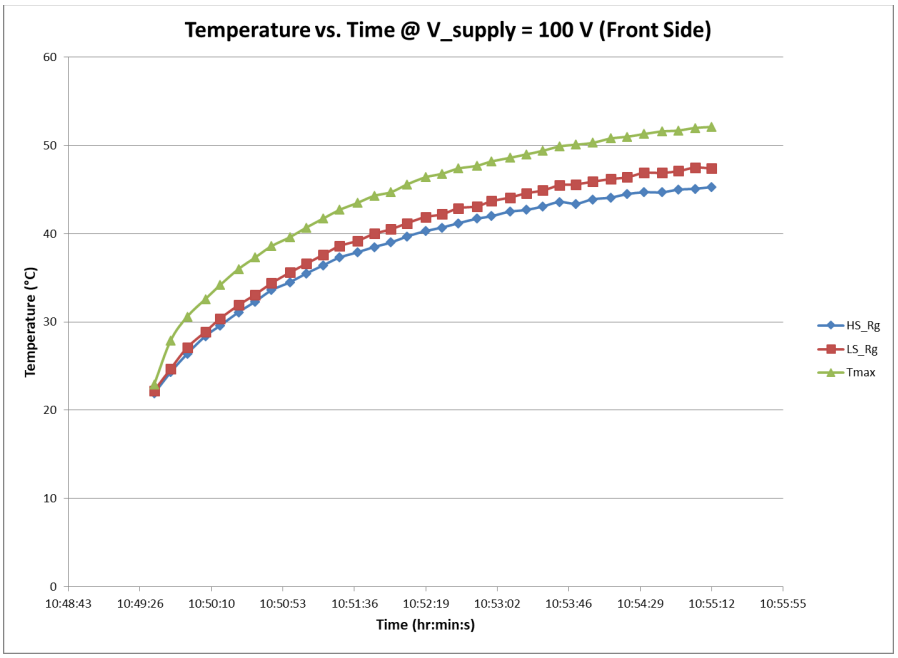

Fig. 15 Front-side temperature measurements for gate resistors when *V_supply* was 100 V

In the next test, the Sorensen power-supply voltage was increased to 300 V while the load was kept at 12.5 Ω. The test was successfully executed and Table 2 shows a summary of the results when the supply voltage was set to 300 V. Figure 16 shows the waveforms taken with the oscilloscope of the LS and HS *Vds* voltages and the load-current *I_load*. Figures 17 and 18 show the thermal images of the back and front sides of the CGD15HB62LP. Figure 19 plots the temperature versus time while the thermal camera was focused on the two IXYS gate-driver ICs. Figure 20 shows the temperature-versus-time graph of the front side while the camera was focused on the two gate resistors. The maximum temperature recorded on the board was 50.9 °C, which also occurred on the front side, with a ΔT of 30 °C.

Table 2 Summary of results for Test 2

Test conditions
V_supply = 300 V
I_supply = 5.5 A
P_supply = 1.65 kW
I_load= 11.6 A, +12.8 A
V_gate = +18 V, –5 V
Frequency = 100 kHz, *Dty* = 50%
R_load = 12.5 Ω
Test time: 5 min

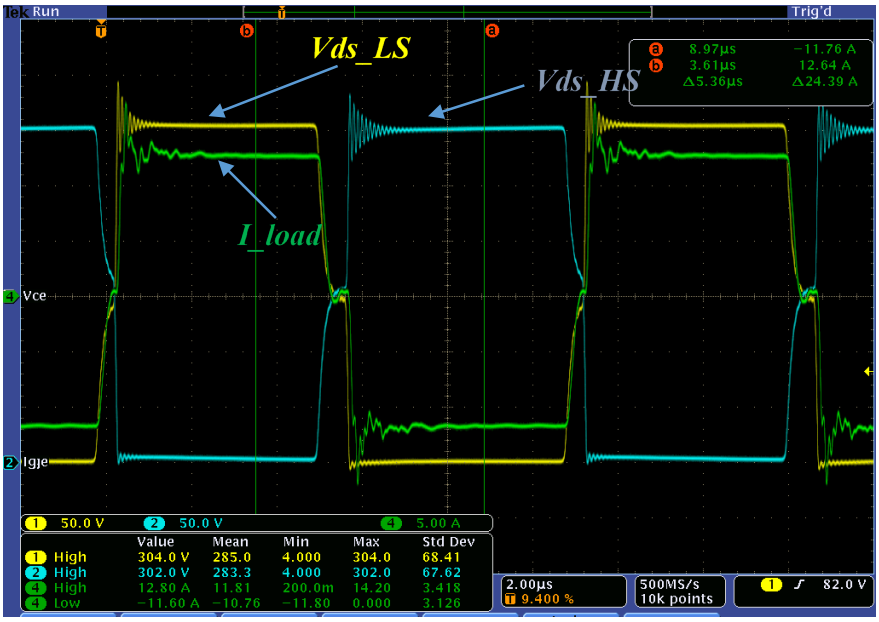

Fig. 16 Switching waveforms for the half-bridge module and load when *V_supply* was 300 V

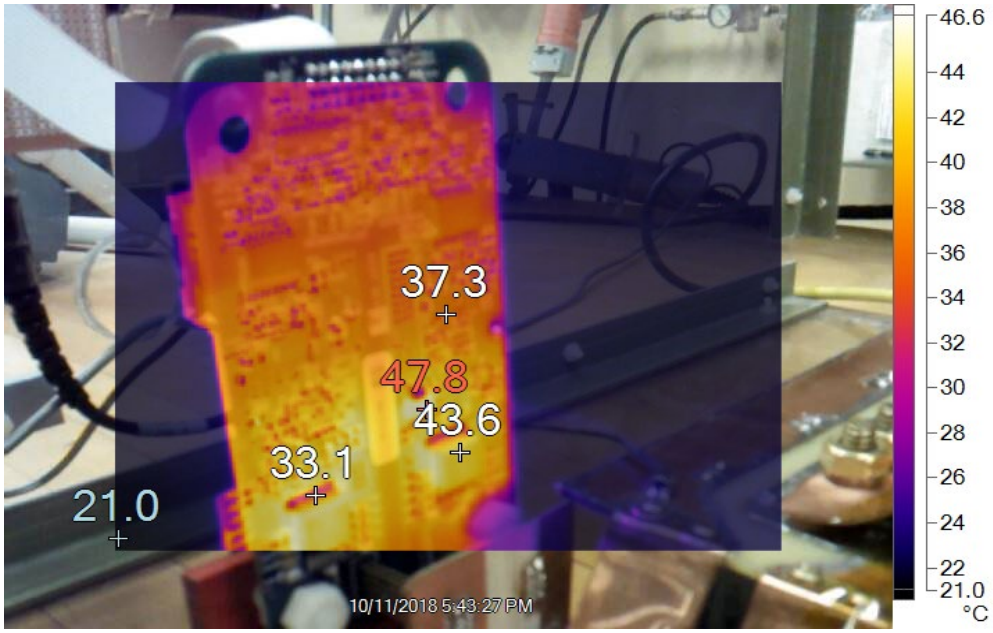

Fig. 17 Final temperature measurements of the back side of the driver board when *V_supply* was 300 V

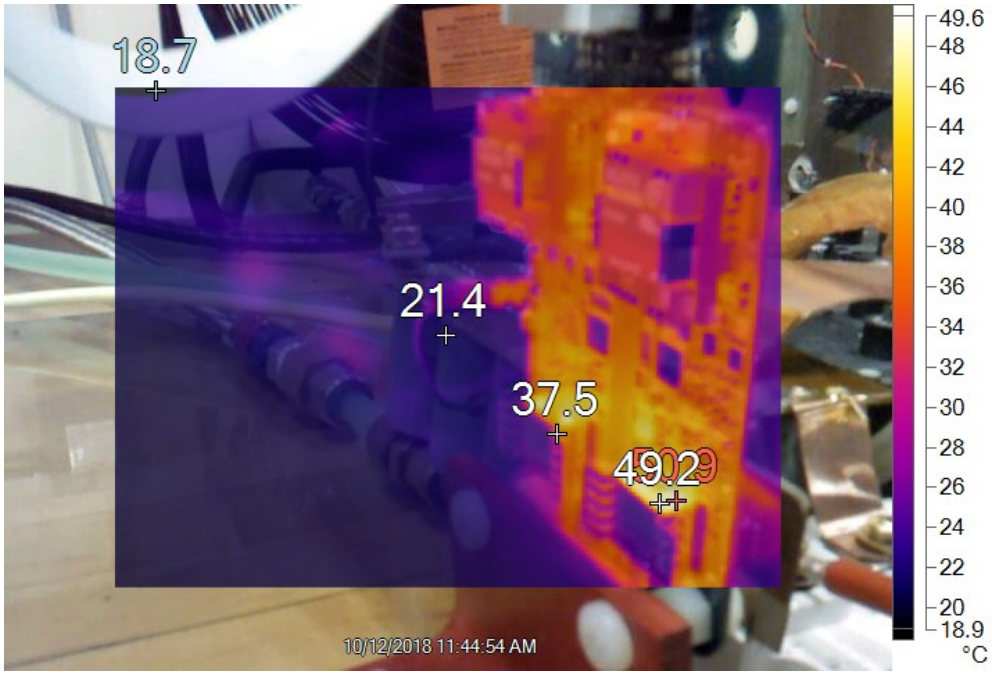

Fig. 18 Final temperature measurements of the front side when *V_supply* was 300 V

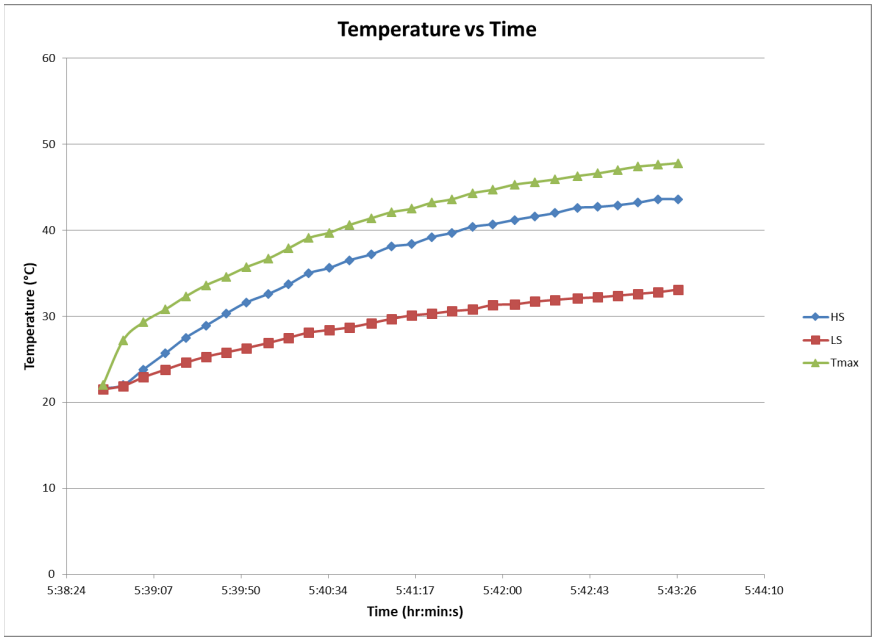

Fig. 19 Back-side temperature measurements for gate-driver ICs when *V_supply* was 300 V

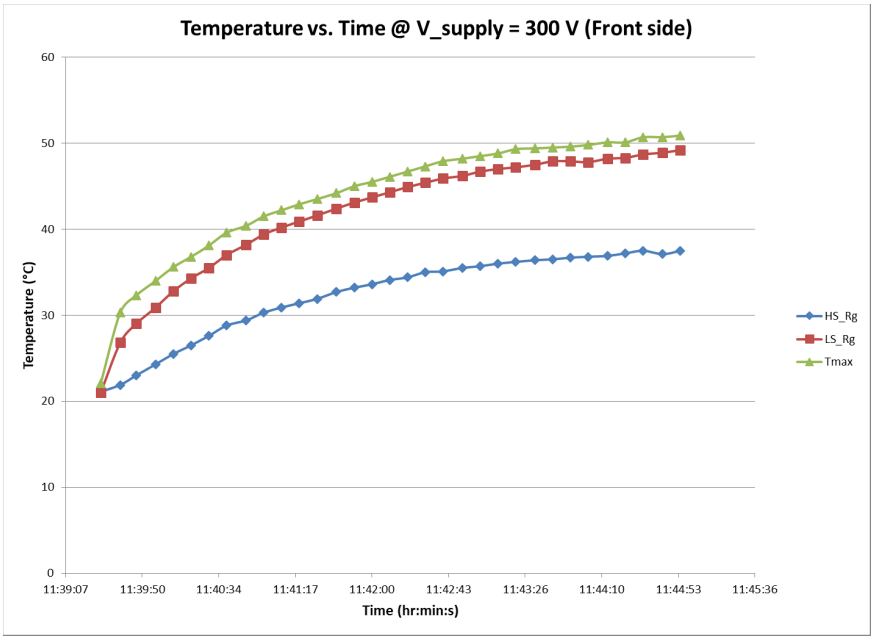

Fig. 20 Front-side temperature measurements for gate resistors when *V_supply* was 300 V

In the final case, the Sorensen power-supply voltage was increased to 600 V and the load had to be reconfigured to stay within the safe dissipation limits of the Ohmite resistors. The new load had eight 50-Ω units, which resulted in an equivalent resistance of 25 Ω (as seen in Fig. 10a). The test was successfully executed and Table 3 summarizes the results when the power supply was set to 600 V. Figure 21 shows the waveforms taken with the oscilloscope of the LS and HS *Vds* voltages and the load current *I_load*. Figures 22 and 23 show the thermal images of the back and front sides of the CGD15HB62LP. Figure 24 graphs the temperature rise versus time while the thermal camera was focused on the two IXYS gate-driver ICs. Figure 25 shows the temperature of the two gate resistors and heatsinks. The maximum temperature recorded on the board was 55.2 °C, which occurred on the front side, with a ΔT of 33.9 °C.

Table 3 Summary of results for Test 3

Test conditions
V_supply = 600 V
I_supply = 6.2 A
P_supply = 3.69 kW
I_load = +11.2 A, –10.8 A
V_gate = +18 V, –5 V
Frequency = 100 kHz, *Dty* = 50%
R_load = 12.5 Ω
Test time: 5 min

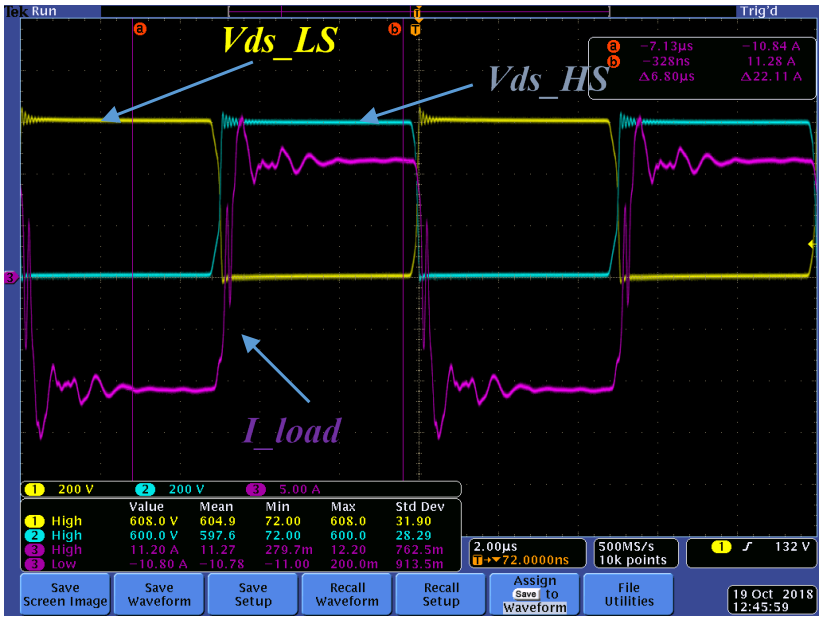

Fig. 21 Switching waveforms for the half-bridge module and load when *V_supply* was 600 V

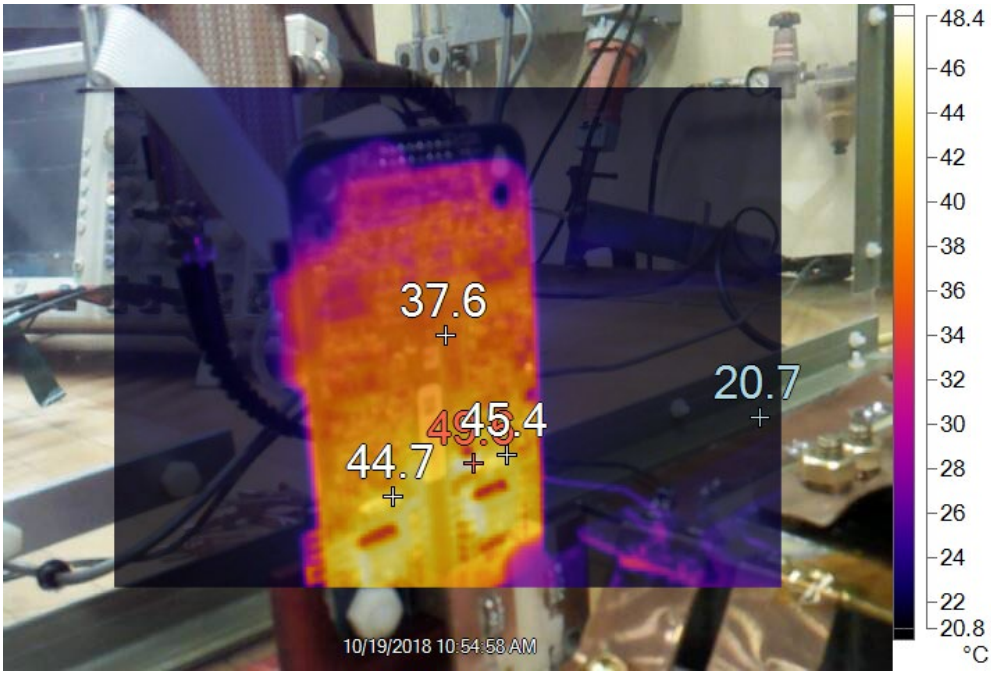

Fig. 22 Final temperature measurements of the back side of the driver board when *V_supply* was 600 V

Fig. 23 Final temperature measurements of the front side of the driver board when *V_supply* was 600 V

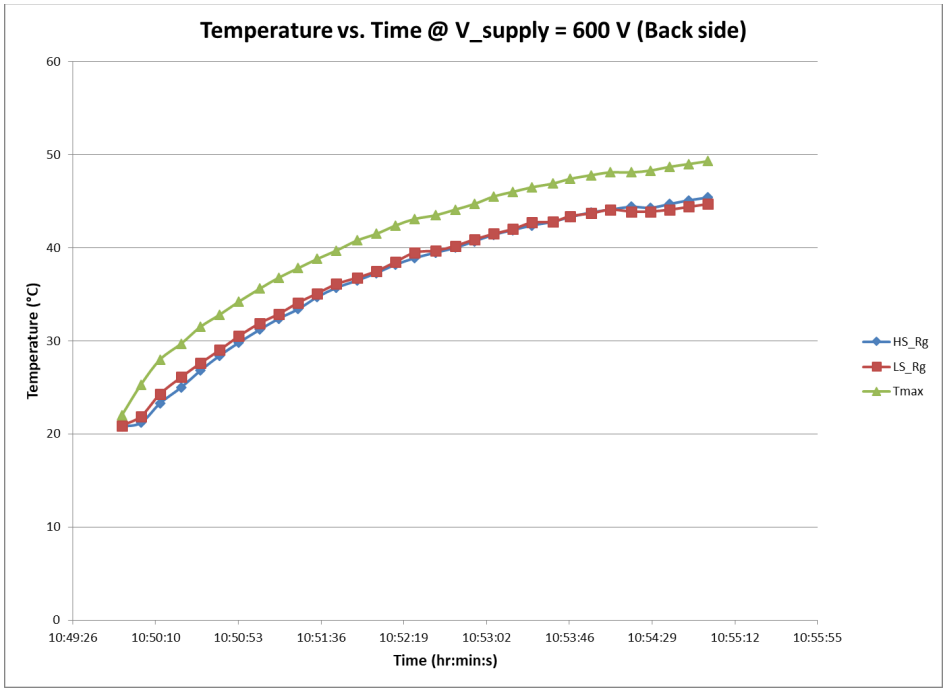

Fig. 24 Back-side temperature measurements for gate-driver ICs when *V_supply* was 600 V

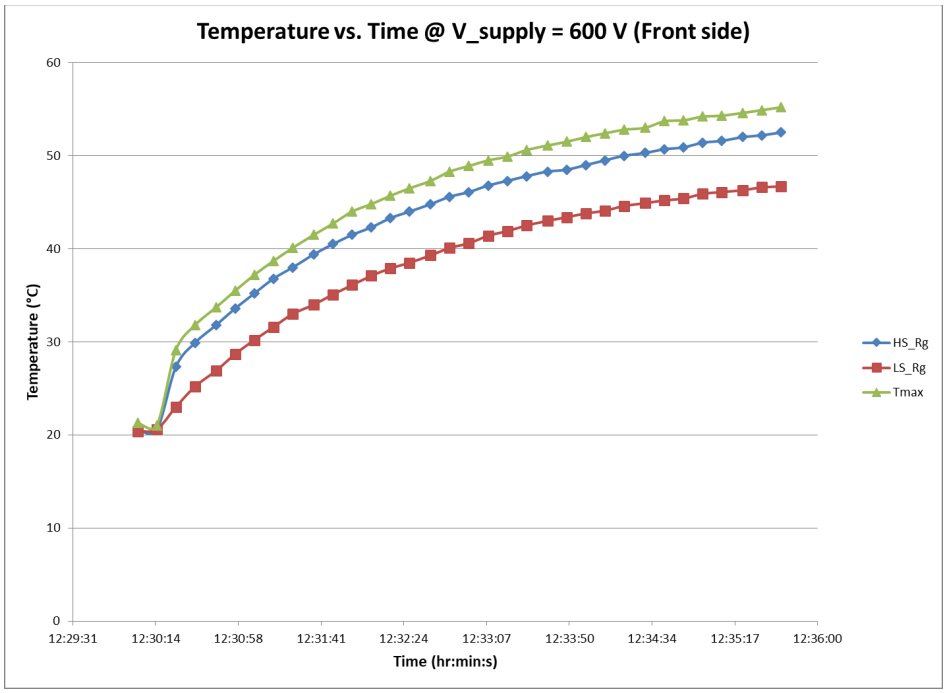

Fig. 25 Front-side temperature measurements for gate resistors when *V_supply* was 600 V

6. Summary and Conclusion

In this report, a CGD15HB62LP dual-channel, differential isolated gate-driver board was evaluated to determine the feasibility of using it as a possible subcomponent of a 60-kW class inverter. The board was successfully tested at 100 kHz, at room temperature, while driving a CAS300M17BM2, 1.7-kV, 8.0-mΩ, 300-A SiC module in a half-bridge circuit under various loading conditions. The HS and LS MOSFETS of the SiC module were driven by the CGD15HB62LP board and they were switched every 10 µs, with a 50% duty cycle, up to 600 V without any catastrophic failures. For a supply voltage of 100 V and a load of 12.5 Ω, the maximum temperature recorded on the board was 52.1 °C with a ΔT of 29 °C. For a supply voltage of 300 V and a load of 12.5 Ω, the maximum temperature recorded on the board was 50.9 °C with a ΔT of 30 °C. For a supply voltage of 600 V and a load of 25 Ω, the maximum temperature recorded on the board was 55.2 °C with a ΔT of 33.9 °C. While these tests are not conclusive, they are good indicators the gate driver can handle the intended switching frequency needed for the inverter without overheating. The on-board, 3-W isolated DC-DC converters, which are integrated with the gate-driver board, were found to be adequate for driving the surrogate load at 600 V. Future work will include long-term reliability tests and a transition to the CAS325M12HM2, 1.2-kV, 3.7-mΩ, 350-A SiC high-performance half-bridge module.

7. References

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List of Symbols, Abbreviations, and Acronyms

AC	alternating current
ARL	US Army Research Laboratory
DC	direct current
HS	high side
IC	integrated circuit
LS	low side
MOSFET	metal-oxide-semiconductor field-effect transistor
PWM	pulse-width modulated
SiC	silicon carbide

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