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MICROWAVE DUAL-CONVERSION FRONT-ENDS FOR 0.1-50 GHz RECONFIGURABLE TRANSCEIVERS

Mark Rodwell, Seong-Kyun Kim, Arda Simsek, and Rob Maurer

The Regents of the University of California, Santa Barbara

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14. ABSTRACT
We report the design and demonstration of wideband, high-dynamic-range integrated circuits (ICs) for 1-20GHz and 1-40GHz dual-conversion receivers. The ICs upconvert from 2-22GHz to a 94GHz first intermediate frequency (IF), and then downcovert to a second IF or to baseband. For a 0.5-22GHz input, the upconversion ICs have 19-29dBm IIP3, and <9dB insertion loss and noise figure. If preceded by a low noise amplifier with 12dB gain and 2dB noise figure, the receiver would have 6.7dB noise figure and 11dBm IIP3. Spurious local oscillator (LO) harmonic responses are high due to an easily-rectified design error; without this, the receiver LO spurious responses would have been c.a. -40 to 45dBc.

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1. SUMMARY

Under the Arrays and Commercial Timescales (ACT) program, in two phases, University of California, Santa Barbara (UCSB) designed widely-tunable, general-purpose transmitter and receiver integrated circuits (ICs) serving the 2-22GHz frequency band. The ICs were fabricated using a very wide-bandwidth 130nm Indium Phosphide (InP) technology.

In UCSB's approach under ACT, broad frequency coverage is obtained using a dual-conversion architecture, with the first intermediate frequency (IF) at 100GHz. This approach eliminates the image response, which otherwise prevents such broad tuning. The key challenge is dynamic range; because the 1st IF will have a relatively broad bandwidth, perhaps 1-5 GHz, jammers within 1- 5GHz of carrier will propagate though the 1st IF, before being suppressed by the 2nd IF filter. It is therefore imperative that the 1st IF have a third-order intercept point (IP3), referred to the antenna, comparable to the radio frequency (RF) front-end.

In the proposed program, after a phase 0 feasibility study, in phase 1 the IC blocks were to be designed, fabricated, and tested, with the full transmitter and receiver ICs to be fabricated in phase 2. In the actual phase 1 effort, not only did we design the individual IC blocks, but we also designed first attempts of a full receiver IC. The ICs consisted of upconversion and downconversion ICs, identical except that the downconversion IC had an IF amplifier. The ICs have a passive (diode) mixer, and a 9:1 local oscillator (LO) frequency multiplier chain. These ICs were, for the greatest part, successful. The ICs functioned properly, with the upconversion ICs showing 21-23 dBm third-order input intercept point (IIP3) and 8 to 9 dB conversion loss over most of the 2-22GHz tuning bandwidth. Although we did not measure noise figure, because the mixers are passive, the conversion loss and the noise figure should be the same.

These ICs had a few limitations which motivated the design of new ICs in phase 2. First, the phase 1 ICs had large die areas, as a consequence of the physically large band-pass filters in the frequency multiplier. The power consumption was large. Finally, the 9:1 LO multiplier chain had very high output power in the spurious harmonics adjacent to the desired 9th harmonic, hence the overall receiver would have had correspondingly strong response.

New ICs were thus designed. The IC design was started in phase 1, but completed in phase 2, with fabrication and testing in phase 2. Two design improvements were pursued: a digital/direct current (DC)-feedback frequency multiplier which reduces die area and should greatly reduce the spurious LO harmonics, and a power-combined mixer which should reduce the power consumption required for a given dynamic range. ICs using the improved mixers did not function due to oscillation. As stand-alone ICs, the digital/DC-feedback multipliers showed extremely (better than 22dB) high spurious rejection even before filtering. The overall upconversion and downconversion ICs again showed 20-25dBm IIP3, and better than 10dB conversion loss (hence noise figure) over a 1-25GHz tuning bandwidth. With degraded IP3, the upconversion IC operates well for 1-40GHz inputs, allowing construction of 1-40GHz tunable receivers. Though receiver spurious responses were between than -30dBc at some RF tunings, at other RF tunings within the 1-20GHz range the spurious LO harmonic rejection was as little as -20dBc. This was due to an easily-rectified error in the connection of cascade multiplier stages within the receiver. We believe that better than 40-45dBc rejection could be readily obtained with a minor design revision.

In the receiver demonstration, because the high-performance on-wafer IF amplifiers were not included in the passive downconversion ICs (they were included only in the active downconversion ICs, which did not work), an external commercial IF amplifier had to be used. As the available external amplifier had quite poor performance, this impaired the receiver performance. We therefore calculate the receiver performance from the measured upconversion and downconversion IC performance, assuming the simulated performance of the high performance on-wafer W-band IF amplifier. The result of this calculation, with two different gain options for the application-specific low noise amplifier (LNA), are shown in Figure 1.

With 18dB gain LNA

Receiver	units	overall	RFA1	M1	F2	IFA1	IFA2	~~IFA3~~	M2	F3	IFA4
Gain	dB	35	18	-8	-1	6.5	0	~~0~~	0.5	-1	20
Gain	linear	3162.28	63.1	0.16	0.79	4.47	1.00	~~1.00~~	1.12	0.79	100.00
Noise figure, component	dB		2	8	1	6.2	0.01	~~0~~	10	1	2
Noise factor, component	linear	2.37	1.58	6.31	1.26	4.17	1.00	~~1.00~~	10.00	1.26	1.58
IIP3, component	dBm	0	25	23	100	24.4	100	~~100~~	23	100	30
DC Power, component	mW										
antenna-referred IP3 of component	dBm		25	5	90	15.4	84.5	~~84.5~~	7.5	84	15
antenna-referred IP3 of system (in-band)	dBm	5									
antenna-referred IP3 of system (out-of-band)	dBm	5									
antenna-referred noise factor contribution	linear	2.37	1.58	0.08	0.03	0.4	0.00	~~0.00~~	0.25	0.01	0.02
system noise figure	dB	3.8									

With 12dB gain LNA

Receiver	units	overall	RFA1	M1	F2	IFA1	IFA2	~~IFA3~~	M2	F3	IFA4
Gain	dB	29	12	-8	-1	6.5	0	~~0~~	0.5	-1	20
Gain	linear	794.33	15.85	0.16	0.79	4.47	1.00	~~1.00~~	1.12	0.79	100.00
Noise figure, component	dB		2	8	1	6.2	0.01	~~0~~	10	1	2
Noise factor, component	linear	4.72	1.58	6.31	1.26	4.17	1.00	~~1.00~~	10.00	1.26	1.58
IIP3, component	dBm	0	25	23	100	24.4	100	~~100~~	23	100	30
DC Power, component	mW										
antenna-referred IP3 of component	dBm		25	11	96	21.4	90.5	~~90.5~~	13.5	90	21
antenna-referred IP3 of system (in-band)	dBm	11									
antenna-referred IP3 of system (out-of-band)	dBm	11									
antenna-referred noise factor contribution	linear	4.72	1.58	0.34	0.10	1.59	0.00	~~0.00~~	1.01	0.03	0.07
system noise figure	dB	6.7									

Figure 1: Receiver Dynamic Range Analysis with High-Gain and Moderate-Gain LNAs
This assumes the measured upconversion and downconversion IC IP3, and assumes that the noise figure is equal to the conversion loss, as is characteristic of passive mixers.

2. INTRODUCTION

The goal of the ACT program, and of the UCSB contract, is to develop transmitter/receiver front-end chip sets, of high performance, and with a very broad range of frequencies of operation and of very high dynamic range. By doing so, a single IC design can serve many Department of Defense (DoD) applications in radar, communications, and electronic warfare (EW). The result will be that new RF/microwave systems can be quickly developed, and at low system non-recurring engineering (NRE) cost, by using such ICs. The customer seeks to cover ~2-22GHz applications; in UCSB's approach we have focused on 2-22GHz as the prime application, but we designed the ICs to also support applications from 1-50GHz.

UCSB's approach, under ACT, is that classical dual-conversion transceiver, such as is widely used for broad tuning in amateur radio. In these, the received signal is first upconverted to a 1st IF, and then downconverted to either a 2nd IF or to baseband. The initial frequency upconversion places the receiver image responses distant in frequency from the tuning range, hence very broad tuning is feasible. For 1-20GHz frequency coverage, a minimum of 40GHz is necessary for the 1st IF. We have instead focused on a 100GHz first IC, as this IF frequency is readily realized in modern InP processes, and allows use of very compact high-quality 100GHz waveguide filters at the first IF. As a practical consideration, several of our experiments used a 94GHz first IF, as narrowband waveguide filters are widely available at this frequency. Ultimately, such a design choice might allow the chip set to serve applications as high as 50GHz.

3. METHODS, ASSUMPTIONS, AND PROCEDURES

We now examine the design and experimental results. These include designs in phases 1 and 2.

3.1 Approach: Dual-Conversion Receiver and Transmitter

The approach (Figure 2) is a dual-conversion receiver. The antenna is connected to an application-specific LNA operating in the desired frequency band. The receiver common module upconverts the signal to a nominal 100 GHz IF (or 94 GHz, as filters for this are more easily obtained). The filtered signal is amplified by the IF amplifier and is then downconverted to a second IF. The two mixers need local oscillators near 100 GHz. To facilitate this, the IC provides frequency multipliers which generate the 60-100GHz 1st LO and 100GHz 2nd LO from lower-frequency references. Multipliers are used in preference to phase locked loop (PLL) synthesizers, as the ICs might be used in radar, where the phase noise requirements are stringent.

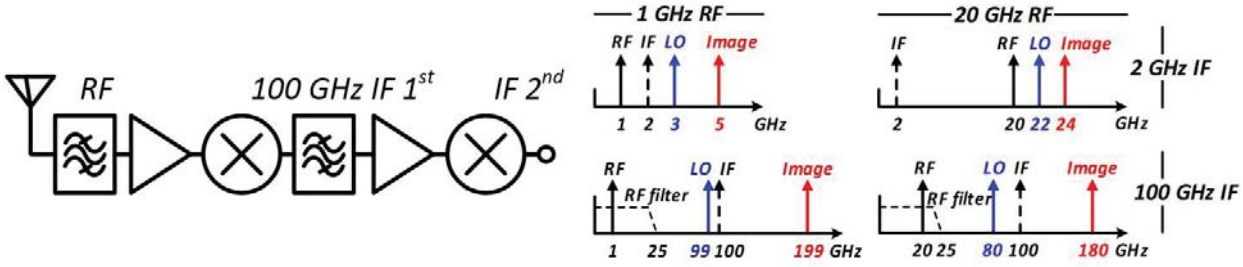


Figure 2: Dual-Conversion Receiver with a W-band First IF, Motivations, and Applications

The frequency plan is not optimum. Broader tuning range without image responses can be obtained by placing the LO above the first IF, rather than below it. The figure compares the two architectures. Unfortunately, if we place the LO above the 100GHz IF, it must then tune to 150GHz or above. Although we have designed in the past high-power 220 GHz high-power (180mW) amplifiers, this is a major design risk. Instead, we chose to place the LO below the IF, as the resulting LO frequencies are lower and the resulting IC more easily designed.

Microwave dual-conversion receivers have not seen widespread use because this would require very high LO and IF frequencies, and it becomes difficult to obtain the necessary gain and dynamic range. Such receivers are now feasible because of the recent emergence of THz-bandwidth IC processes. In an IC technology providing ~1THz transistor cutoff frequencies, the transistor has high available gain, and low noise, at 100GHz It then becomes possible to design the receiver's mixer and IF components with adequately high dynamic range. In this work, we have used Teledyne's research-level 130nm InP HBT technology. The transistors provide 1.15THz power-gain cutoff frequencies. Most notably, Figure 3, the common-emitter maximum available gain is ~15 dB at 100GHz, and the minimum noise figure is 5.0 dB. The technology also provides 3-3.5 Volts breakdown, hence moderately high-power circuits are also feasible.

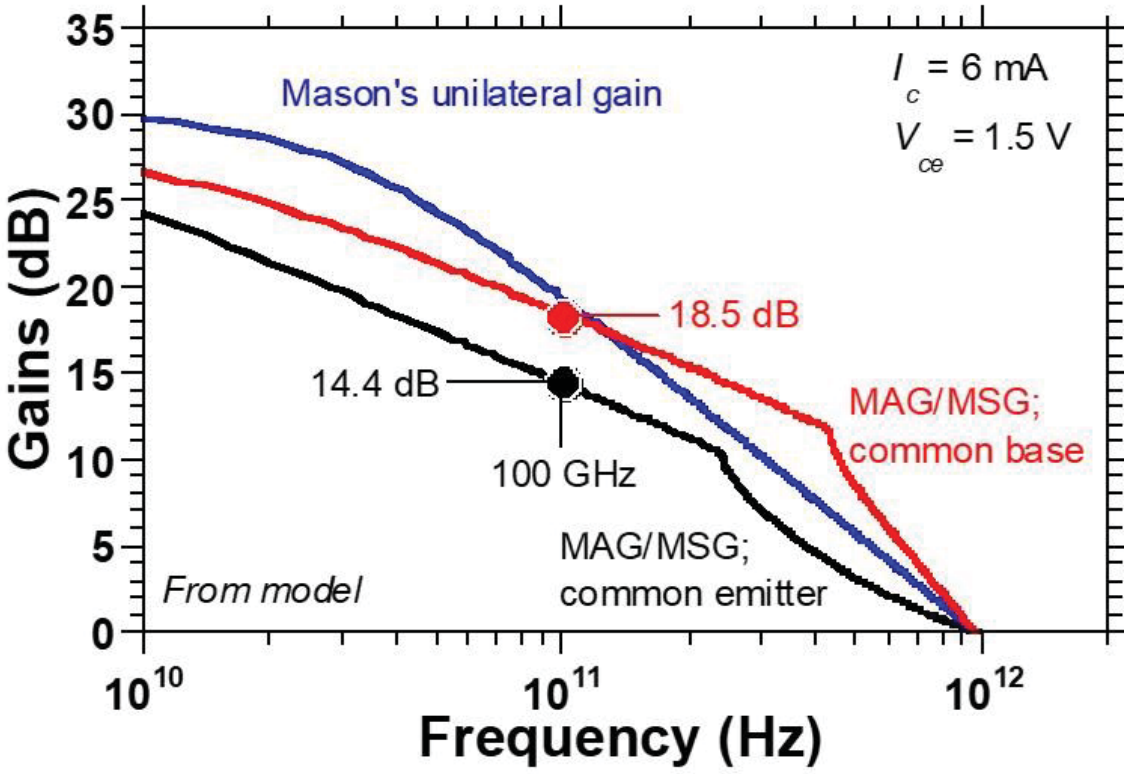


Figure 3: RF Characteristics of InP HBTs at the 130nm Node

3.2 Phase 1 Dual-Conversion Receiver Design

We first review the efforts under phase 1. The phase 1 IC architecture is shown in Figure 4. The full receiver is broken into two parts (two ICs) to ease testing. The first IC carriers the up-conversion mixer and its frequency conversion chain, while the second IC carriers the IF amplifier, the down conversion mixer (to 2nd IF in the low GHz range) and, again, a frequency multiplier chain. The design has a 2-20GHz RF, a 100GHz first IF, and requires a 98-80GHz local oscillator. The LO is generated by a 9:1 multiplier. This provides much lower phase noise than a PLL. The multiplier stages are simple logic gates. The mixers are high dynamic range designing using Schottky-like DHBT collector-base diodes. Series diodes increase the dynamic range but then require higher LO drive power.

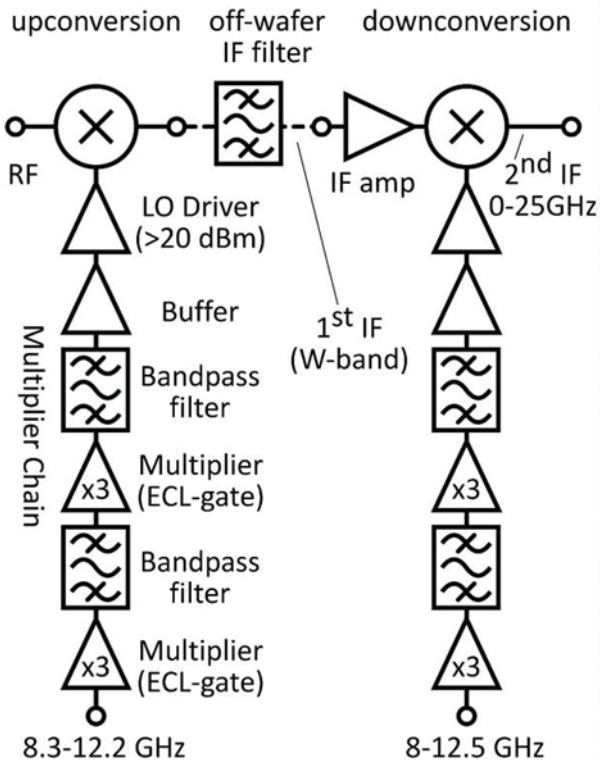


Figure 4: Key Features of the First-Generation, Phase 1 Dual-Conversion IC Design

Between the two ICs is placed the IF bandpass filter. This is an off-wafer component, a waveguide filter. We have purchased such a filter, though for convenience and cost we have selected at filter with a 94GHz center frequency. The filter is connected to the ICs with wafer probes.

We note that two very similar ICs would be used in the widely-tunable transmitter. Simply, the inputs and outputs of the IF amplifier on the 2nd IC would need to be reversed.

To tune over a 2-20GHz bandwidth with a 100GHz first IF, and a few-GHz 2nd IF, the 1st LO must tune over 98-80GHz, and the 2nd LO must be at approximately 100GHz. This is provided by low-phase-noise 9:1 frequency multipliers formed by cascaded frequency triplers. For design robustness, the triplers are in fact simple but very high speed logic gates. For high dynamic range the mixers are passive, diode designs. Fortuitously, in InP HBT IC processes, the HBT base-collector diode has Schottky-like characteristics and hence very high speed. The high-dynamic-range-mixer required a high-power LO driver.

We now consider key features of the phase 1 design in more detail. First consider the high dynamic range mixer (Figure 5). In IC receivers, one can use active (transistor) or passive mixers. Active mixers generally have lower IP3 and poor noise figure than well-designed passive mixers. The latter can have high IP3 and low loss (and hence low noise figure, as these are equal in passive mixers). In metal oxide semiconductor (MOS) technology, the passive mixer can use MOS switches. In bipolar technology, without field-effect transistor (FET) switches available, the remaining choice is the diode passive mixer. The feasible performance then depends on the

quality of the diodes available in the bipolar IC technology. In all bipolar technologies, the base emitter diode has poor high-frequency characteristics. In Si, Si/SiGe, and GaAs/AlGaAs HBT bipolar technologies, the base-collector diode suffers from severe minority (hole) carrier storage in the N+ subcollector, hence these devices have long reverse-recovery times. Some GaAs and Si bipolar IC technologies address this by having added process modules which provide Schottky diodes. In InP double heterojunction bipolar transistor (DHBT) technologies, the base-collector heterojunction blocks hole injection into the N+ subcollector, minority carrier storage becomes very small (just the ~0.2ps electron storage time in the base), and the diodes have Schottky-like characteristics. Other features of the final mixer design include 2:1 series- connected diodes, and high LO drive power, both for increased IP3, and baluns for broadband operation. The LO port tunes from 60GHz-110GHz, and the two signal ports tune from DC-40GHz and 75-110GHz.

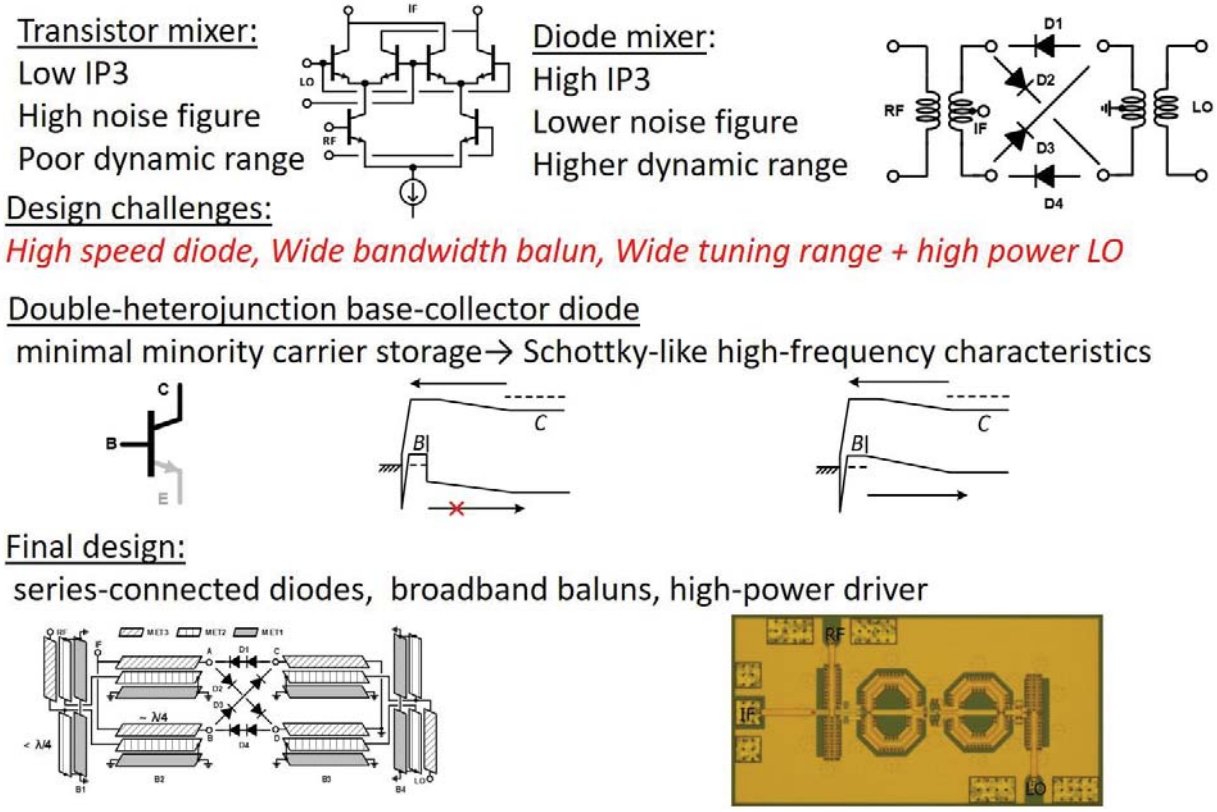


Figure 5: Design Features of the Passive Mixer

In the phase 1 design, a 9:1 multiplier chain (Figure 6) generated the local oscillator. There are two cascaded 3:1 frequency multipliers. Each is a high-speed emitter-coupled logic (ECL) gate which converts a sinusoidal input into a square-wave output. An output filter then selects the desired 3rd harmonic. The first 3:1 multiplier uses a lumped LC filter; the 2nd multiplier uses a microstrip stub filter, as lumped elements have poor Q at 100GHz. The output of the 2nd multiplier was amplified first by a series of logic gates, and then by a classic two-stage reactively-matched amplifier. This was then followed by a high- power LO drive amplifier, (not shown in Figure 6).

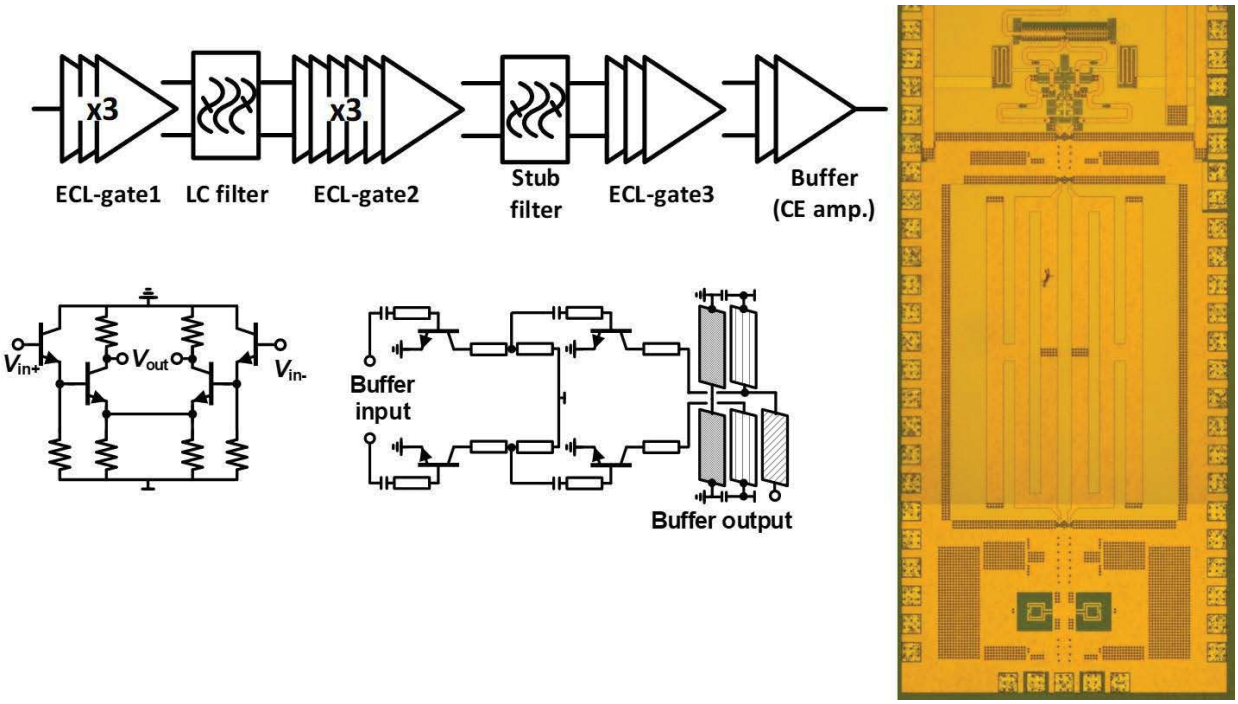


Figure 6: Topology and IC Micrograph of the 9:1 Phase 1 LO Frequency Multiplier Design

3.3 Phase 2 Dual Conversion Receiver Design

The phase 2 effort sought to improve upon the IC designs developed in phase 1. The design of these 2nd generation ICs was started during the last months of phase 1, and designs were completed and ICs fabricated and tested during phase 2.

There were two key efforts and potential improvements investigated in phase 2. The first was high dynamic range active mixers using power combining to increase the dynamic range. This effort, though successful in design, failed experimentally because the mixers oscillated during RF testing. The second effort was the investigation of digital/feedback frequency multipliers. These exploit the robust IC implementation of digital IC designs with strong harmonic suppression derived from DC negative feedback. Combined with additional passive filtering, spurious harmonics can be greatly suppressed. This would result in greatly improved spurious tuning responses in a dual-conversion receiver using LO frequency multipliers. The frequency multipliers, as independent IC test structures, were highly successful. Unfortunately, the full IC receiver implementation using these multipliers contained an error which resulted in the IC not showing the level of spurious rejection demonstrated in the frequency multiplier ICs themselves. This error is readily fixed; unfortunately, the program has concluded.

3.4 Phase 2 Dual Conversion Receiver Design: LO Multipliers

The dual-conversion receivers use multipliers, rather than PLL synthesizers, to generate the high-frequency local oscillators (Figure 9). PLL synthesizers on ICs are compact, and do not produce spurious output signals. Unfortunately, unless the loop bandwidth is made very large, the large phase noise of an on-wafer voltage-controlled-oscillator (VCO) results in substantial phase noise

in the PLL output. Synthesizers in microwave instruments obtain low phase noise by using an off-wafer yttrium-iron-garnet (YIG)-tuned oscillator. Classic multiplier chains produce low (source-limited) phase noise, but require physically large filters to suppress the unwanted (spurious) harmonics. The filters limit tuning range, and their finite out-of-band rejection results in spurious harmonic leakage which then results in receiver spurious responses.

Frequency multipliers implemented in waveguide, even today remain the dominant means of generating signals above 100GHz. Waveguide multipliers benefit from the very high filter Q's available, greatly aiding the spurious harmonic rejection. For on-wafer design, these filters can become inconveniently large. Further, on ICs, passive elements have low Q, giving poor filter selectivity, and resulting in poor spurious harmonic rejection.

The multipliers used in phase 1 (Figure 7) generated square-wave outputs. Given the 1, 1/3, 1/5,…Fourier series coefficients for a square wave, the fundamental is almost 10dB stronger than the desired 3rd harmonic; this places extreme demands on the output filter.

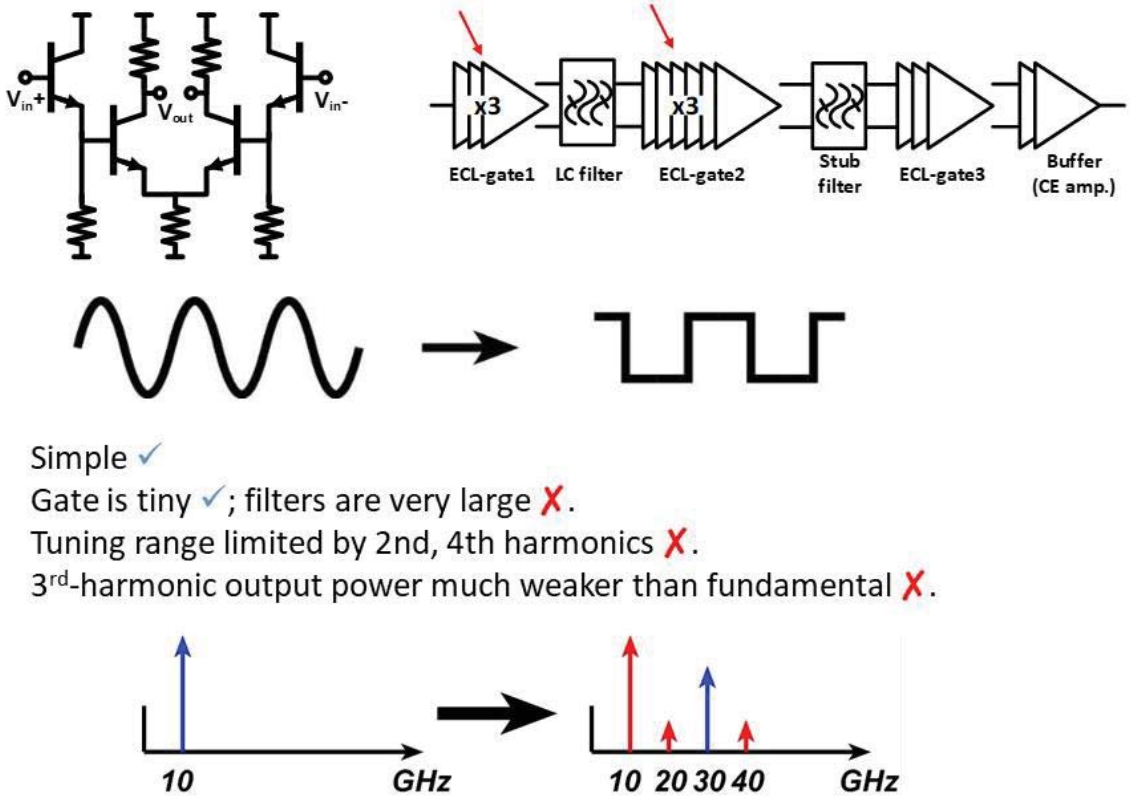


Figure 7: Limitations of the Phase 1 Frequency Multiplier Designs

We can obtain a much more favorable output spectrum by digital self- mixing (Figure 8). If a signal is mixed against itself, with 90 degree relative phase, in an ideal analog mixer, the 2nd harmonic will be produced with zero residual fundamental. Better still, if the input signal is digital (a 10101…sequence), then using this as the two inputs to an XOR gate, with a 90 degree relative delay, will produce a digital square wave at twice the frequency. The design is compact and level-insensitive. If the input square wave has exactly a 50% duty cycle, and if the phase shift is exactly 90 degrees, then the output signal will have power only at the 2nd, 6th, 10th, etc. harmonics; the suppression of nearby spurious harmonics will be excellent. We must somehow ensure these two conditions.

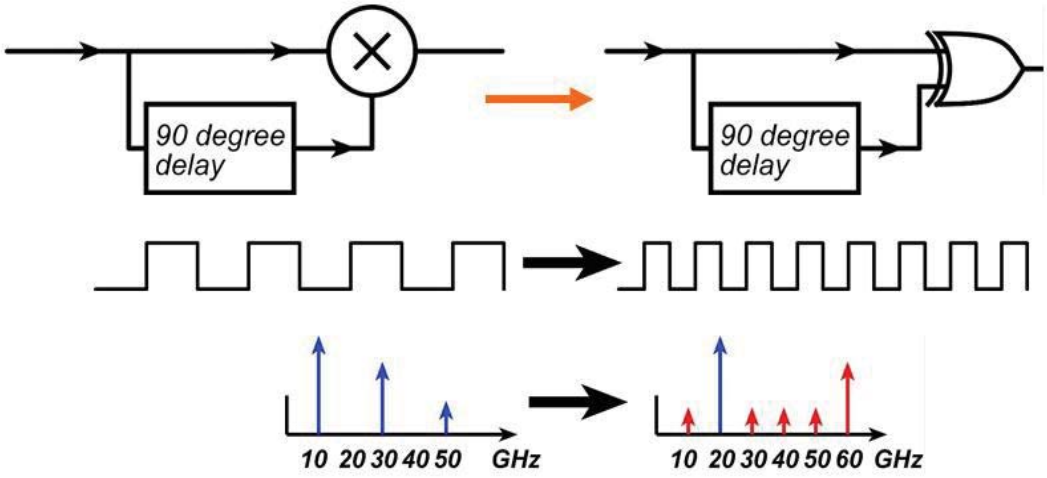


Figure 8: Frequency Multiplication by Digital Self-Mixing and the Resulting Improved Spurious Harmonic Suppression

Figure 9 examines in more detail the origin of spurious harmonics in the digital self-mixing frequency doubler. Given correct operation, the output is a 101010 square wave at twice the input frequency, and hence has outputs at 2fin, 6fin, 10fin, etc. At the input to the XOR gate there is a limiter which converts the input sinewave into a square wave. If the sinusoidal input has a DC offset, or the limiter has one, then the limiter output will be a 10101…sequence with a duty cycle differing from 50%. This will produce spurious harmonic outputs at the XOR gate output. Importantly, DC offsets in the limiter or its input will produce a nonzero DC output level from the limiter. We can measure the DC output level of the limiter and then adjust the DC input level to the limiter to force the DC output level to zero volts. This is done with an op-amp DC feedback loop. By forcing the limiter to zero DC offset, this forces the limiter output to have a 50% duty cycle, and therefore suppresses the generation of spurious harmonics in the multiplier chain.

If the relative phases of the XOR inputs differs from 90 degrees, spurious harmonics will again be generated, but this also generates a nonzero DC level at the XOR output. Again, a DC operational amplifier (op-amp) negative feedback loop is used: this adjusts the variable delay until the XOR gate has zero DC output level. This also suppresses generation of the spurious 4th harmonic.

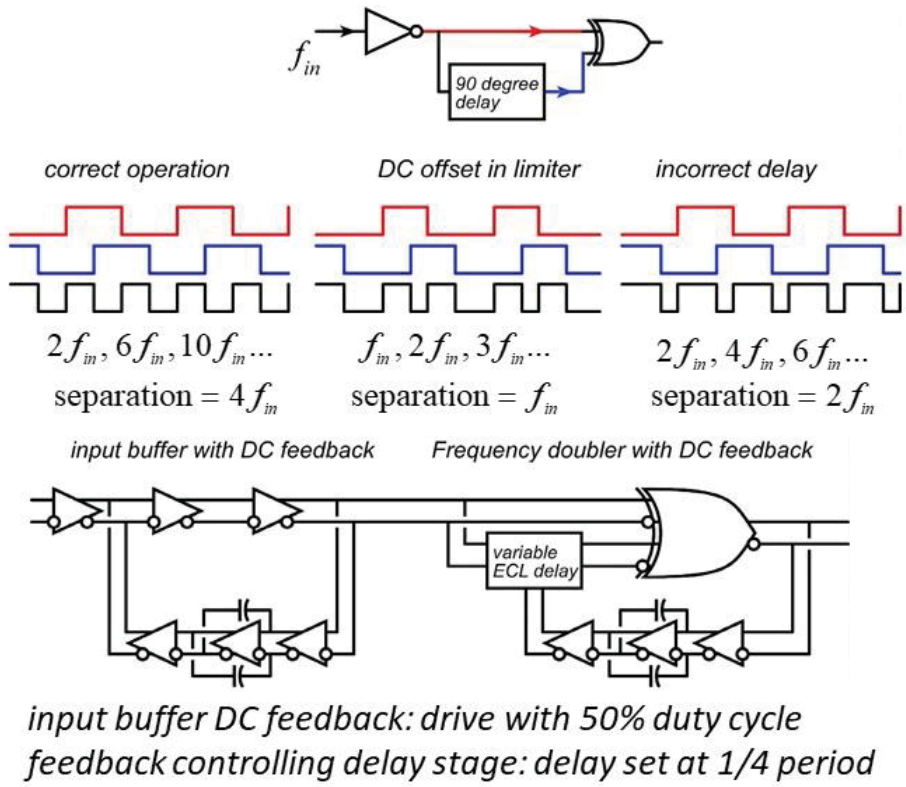
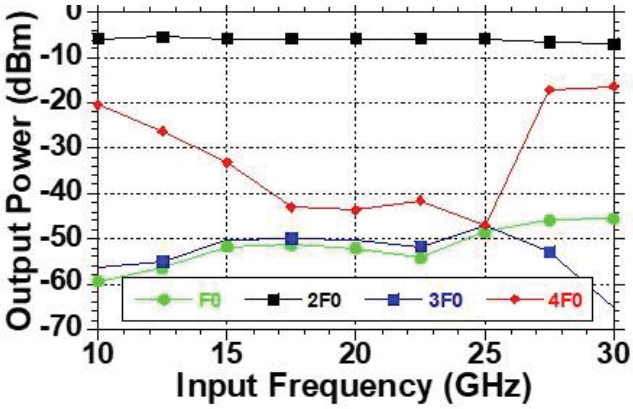
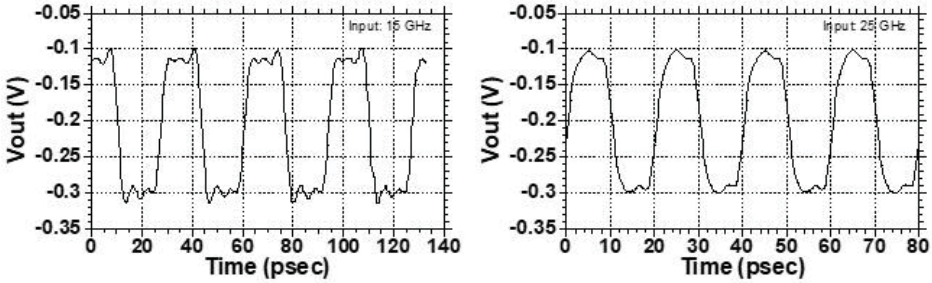


Figure 9: Origin of Spurious Harmonics in the Digital-Self-Mixing Frequency Multiplier, and Suppression of these by DC Negative Feedback

The ICs were designed with a 60-100GHz first LO tuning range and with a target 4:1 frequency multiplication ratio. This is obtained using two frequency multipliers, the first with a 15-25GHz input and the second with a 30-50GHz input. Figure 10 shows the simulated performance of the first frequency multiplier. The most-serious adjacent 1st and 3rd harmonics are suppressed by almost 40dB over the tuning range, and the more easily filtered 4th harmonic is suppressed by 25dBc over most of the tuning range.



Simulated output powers of harmonics



Simulated waveforms at input frequencies: 15 GHz (left) and 25 GHz (right).

Figure 10: Simulation the first Digital-Plus-Feedback Frequency Multiplier with a 15-25GHz Design Input Frequency Range

Figure 11 shows simulations of the 2nd frequency multiplier. Similar spurious rejection is predicted.

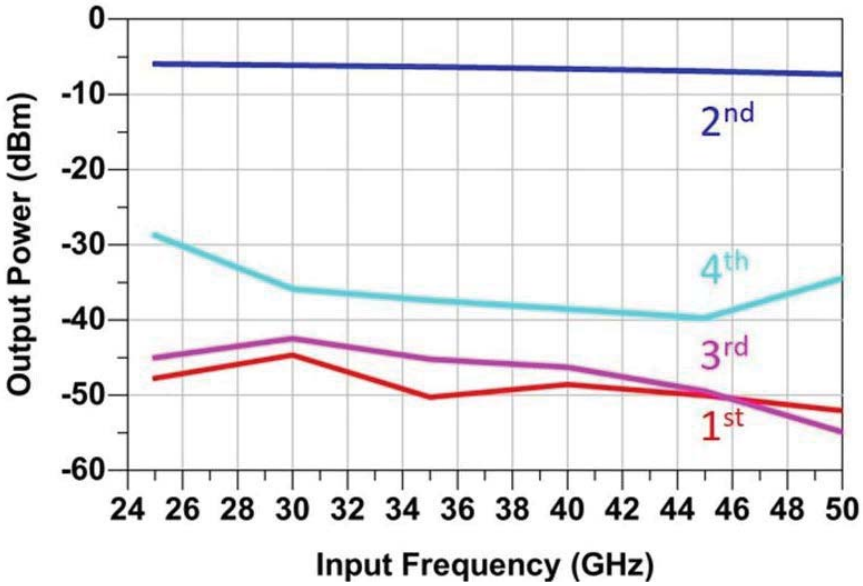


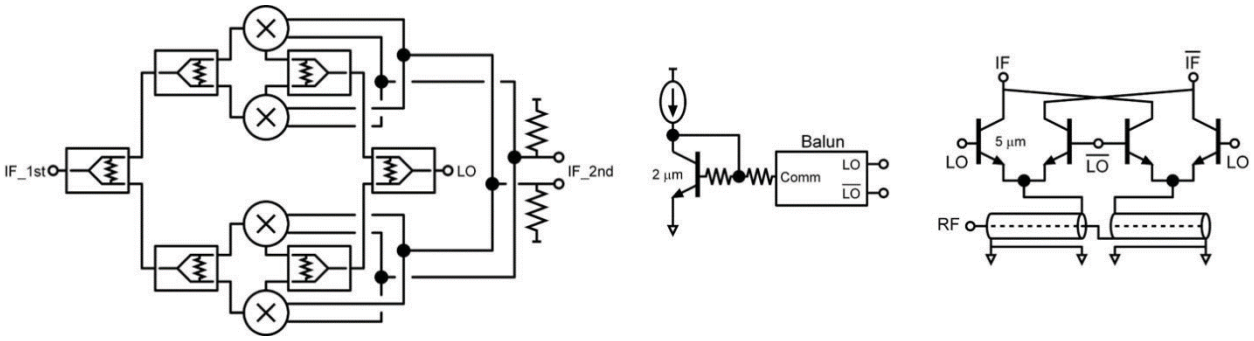
Figure 11: Simulation the second Digital-Plus-Feedback Frequency Multiplier with a 30-50GHz Design Input Frequency Range

3.5 Phase 2 Dual-Conversion Receiver Design: Power-Combined Active Mixers

The second innovation pursued in phase 2 was the use of power- combined active mixers. Passive mixers have high dynamic range, but need high LO drive power: the LO drive amplifier requires large IC die area, consumes large DC power. Active mixers, in contrast, need much less LO drive power. As a much smaller LO drive is required, this saves die area and saves DC power. Active mixers, unfortunately, have much lower dynamic range. This can be addressed by using a power-combined active mixer. If we use 4:1 combining, this increases dynamic range by 6 dB.

Figure 12 illustrates the concept. Four mixers are used. The input, at the 1st IF frequency, is distributed to the 4 mixers using a passive 4:1 power splitter network. Such power splitters are relatively narrowband, but this is of no consequence, as the 1st IF is not broadband. The outputs of the 4 mixers are combined by current summation, not power summation, as current summation is broadband. Please recollect that the 2nd IF might be selected anywhere in the DC-25GHz range. The mixers themselves resemble Gilbert-cell designs, except that the lower differential pair, which serves in a normal Gilbert cell mixer as gain and an active input balun, is replaced by a passive transmission-line balun. This improves the mixer noise figure.

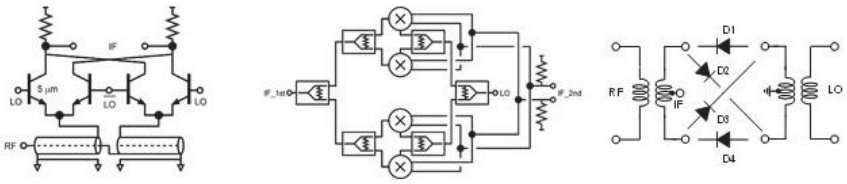
The active mixer design was also improved, with increased HBT junction areas, decreased bias current densities, and an added input second-harmonic filter. In simulations, these improved the dynamic range significantly.



(a) **(b)**

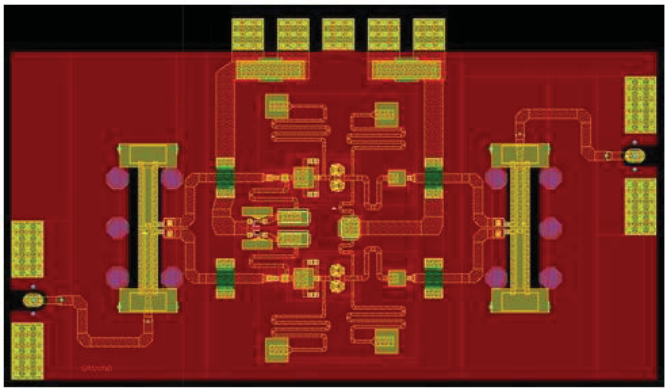
Figure 12: Power-Combined Mixer for improved Dynamic Range: Block Diagram (a) and Individual Mixer (b)

Figure 13 summarizes the results, in simulations, of an extensive design study. Power-combining improves the mixer IIP3, as expected, by 6dB. The noise figure is degraded by 1dB; this is due to power splitter losses. Overall, with power-combining, the mixer dynamic range is improved by 5dB, being now only 5dB poorer than the passive mixer. The advantage is power consumption: including the power consumption of the LO driver, the passive mixer requires 1W, while the power-combined active mixer requires only 436mW. The IF amplifier was also re-designed (Figure 14) in phase 2 for increased dynamic range.



	Active mixer	Power combining Active mixer	Diode mixer
Gain	-4.3 dB	0.5 dB	- 8 dB
Noise Figure	9 dB	10 dB	8 dB
IIP3	14 dB	20 dBm	23 dBm
DC Power	61 mW @ 2.1 V + 130 mW @ 2 V (Mixer + LO driver)	306 mW @ 3.5 V + 130 mW @ 2 V (Mixer + LO driver)	1 W @ 2 V (LO driver)

Figure 13: Outcome of Design Study: Passive vs. Active vs. Power-Combined Active Mixers



Category	Phase 1	Phase 2
HBT Cell Size	4 X 5 µm	**8 X 5 µm**
S_{21}* (dB)	6	6.5
OIP3* (dBm)	**26**	**30.8**
IIP3* (dBm)	20	24.4
I_{DC}* (mA)	100	57
P_{DC}* (mW)	200	114
Noise Fig.* (dB)	**7.3**	**6.2**
Core Area (µm X µm)	414 X 502	380 X 458

Figure 14: Design Revision of the IF Amplifier, Phase 1 vs. Phase 2

3.6 Phase 2 Dual-Conversion Receiver Design: Overall

Figure 15 shows mask layouts of the ICs designed for the phase 2 tape out. A passive upconversion block uses the diode mixer, high-power LO driver, and 4:1 digital/feedback frequency multiplier. This IC can also be used for downconversion, but we did not include a passive downconversion design incorporating the IF amplifier. The downconversion IC contained the power-combined active mixer, the 4:1 digital/feedback frequency multiplier, and the IF amplifier.

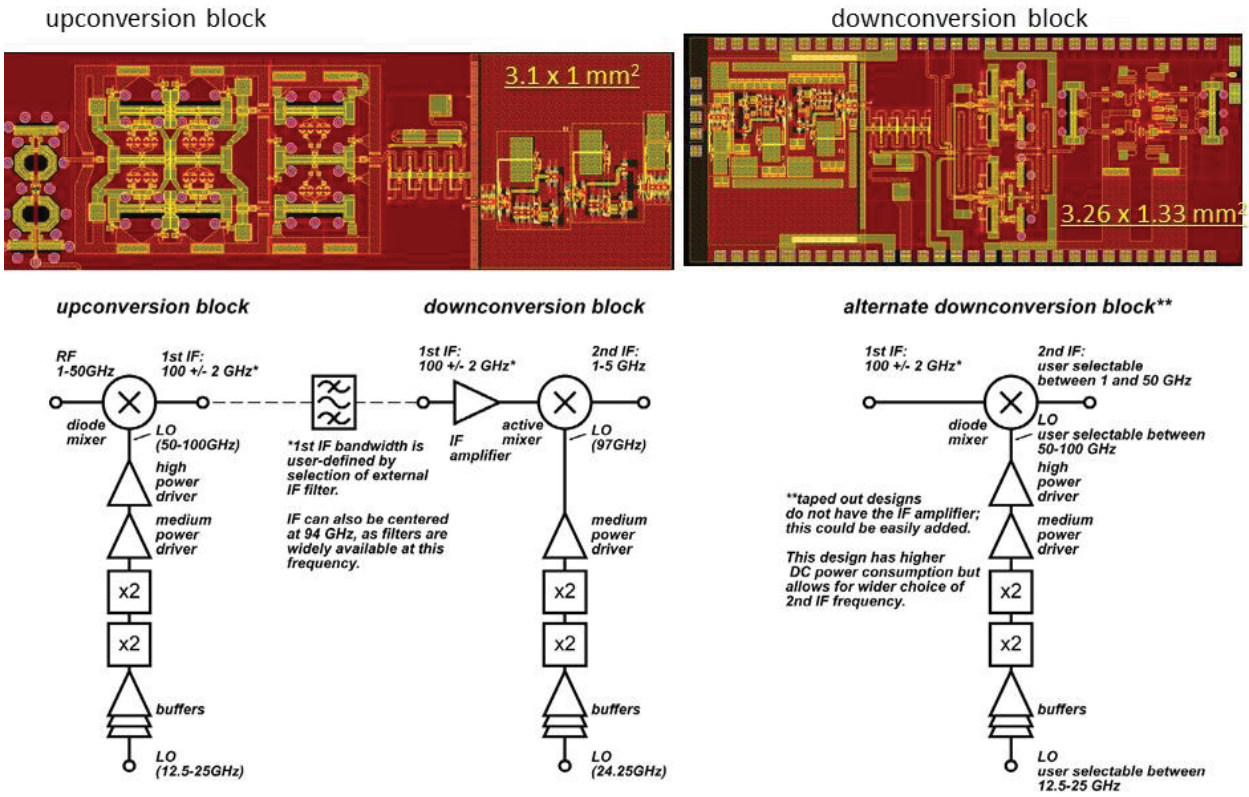


Figure 15: Phase 2 Upconversion and Downconversion ICs: Block Diagrams and IC Layouts

4. RESULTS AND DISCUSSION

We now review measurement results for the IC designs of phases 1 and 2.

4.1 IC Phase 1 Dual-Conversion Receiver Results

We now summarize the performance of the phase 1 designs. Figure 16 and Figure 17 show two amplifiers, the first IF amplifier and the second broadband high power LO driver amplifier. The pseudo-differential IF amplifier had (measured) 8dB noise figure, 6dB gain, and 21 dBm OIP3. The LO driver uses broadband series power-combining with sub-quarter-wavelength baluns, and, in simulations, produced >19dBm over 60-100GHz.

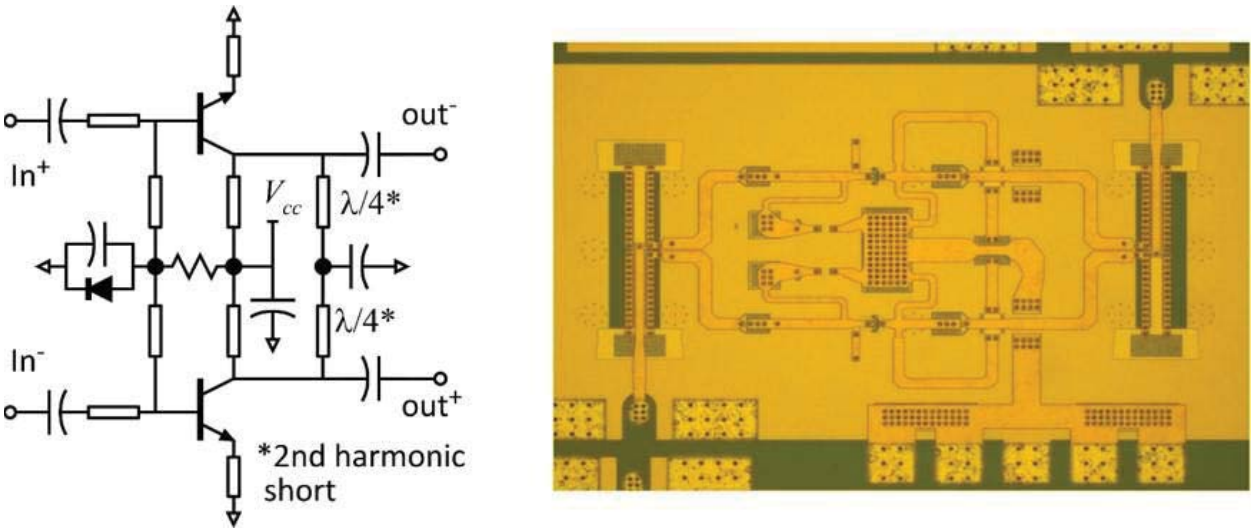


Figure 16: Phase 1 Amplifier Designs for IF Amplifier

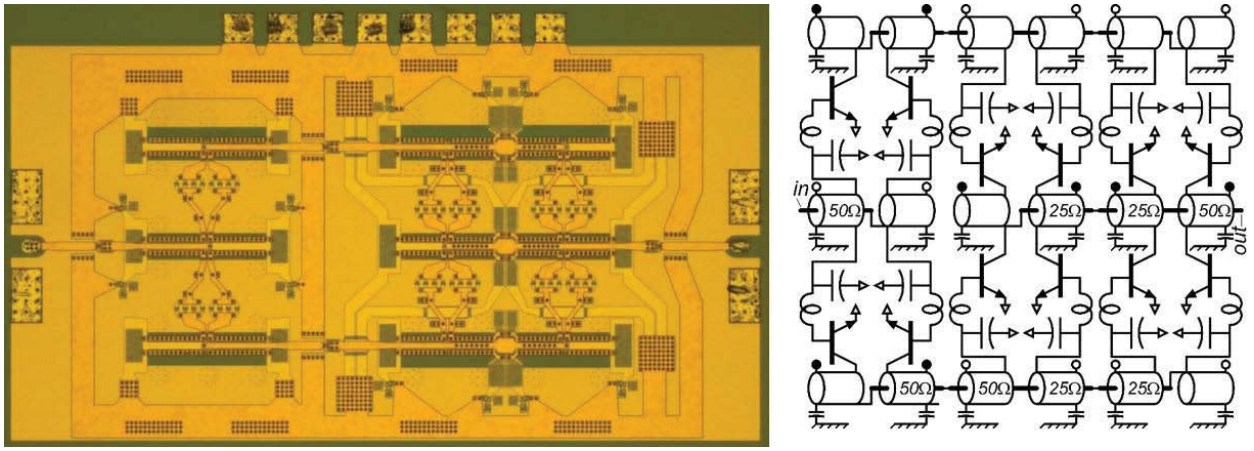


Figure 17: Phase 1 Amplifier Designs for LO Driver Amplifier

Figure 18 shows more detailed data on the phase 1 broadband LO driver. Its gain is relatively flat, at ~15dB, over 40-120GHz. At 3dB gain compression, it produced 17.5dBm at 50GHz, increasing to 21dBm at 100GHz. This driver is key to the broadband high-dynamic-range mixer.

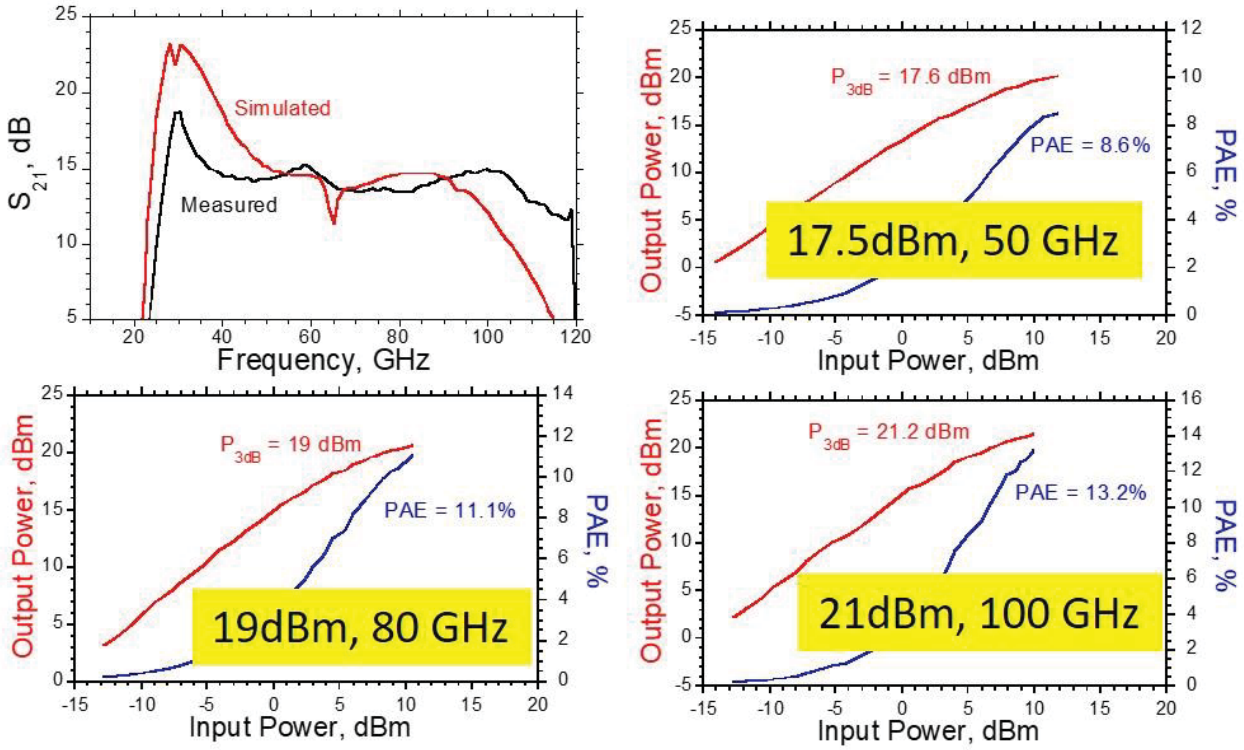


Figure 18: High-Power Broadband LO Driver in the Phase 1 ICs

Figure 19 shows measured performance, specifically output power vs. frequency (before the high-power driver) of the LO multiplier in the phase 1 designs. Output power is better than 8dBm over 75-108GHz. This is sufficient to drive the high-power LO driver into strong gain compression, producing the output drive power noted in Figure 18. Regarding power consumption, the IC draws 270 mA from a -4 V supply and 64 mA from a 2 V supply.

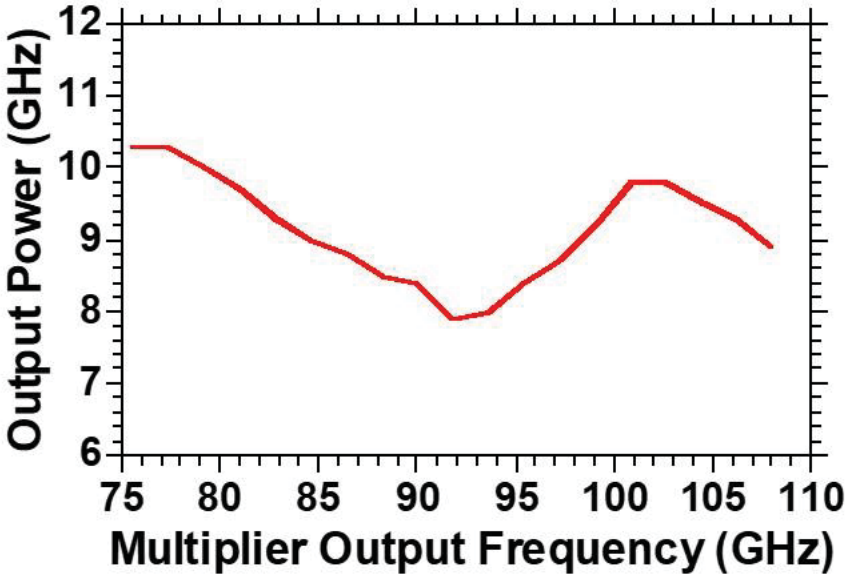


Figure 19: Output Power vs. Frequency (before the high-power driver) of the LO Multiplier in the Phase 1 Designs

We now turn to the overall performance of the upconversion IC (Figure 20). Data is shown with a fixed 200MHz input, with the 1st IF frequency tuned over 75-110GHz. This shows that the IC functions well with any choice of IF over 75-110GHz. Data is also shown with a fixed 100GHz 1st IF output, with the input RF frequency tuned from 0.5 to 22GHz. This illustrates the input RF tuning bandwidth. There is 5dB to 7dB conversion loss over bandwidth. Note that this is a passive mixer, hence the noise figure is equal to the conversion loss. The IC shows 21-24 dBm IIP3 over most of bandwidth, with a slight decrease between 20-22 GHz due to the reduced output power of the LO driver amplifier when operating at 50-80GHz,

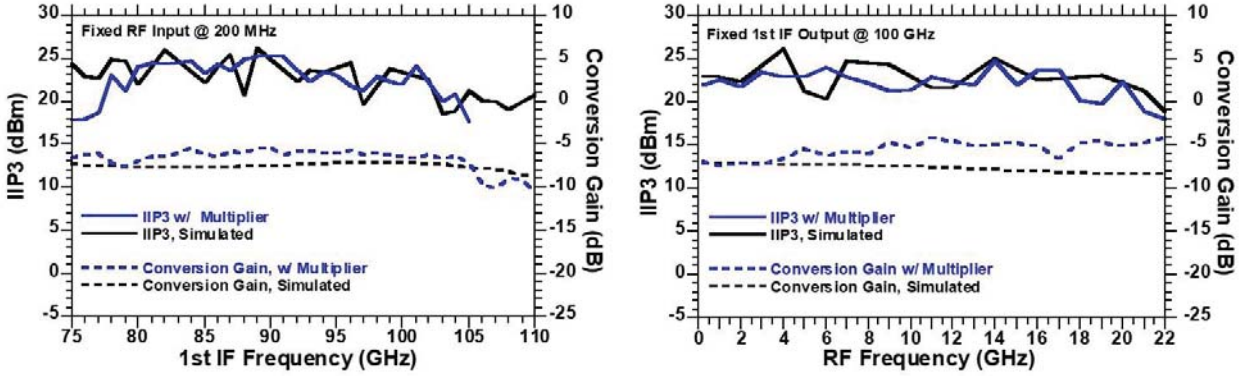


Figure 20: Measured Characteristics of the Phase 1 ICs in Upconversion

Figure 21 shows the performance of the downconversion block. The version measured had no IF amplifier. Data is shown with a fixed 200MHz 2nd IF, with the 1st IF tuned from 75-110GHz;the IC works well with any IF from 75-105GHz. Data is also shown with a fixed 99GHz first IF, and with the 2nd IF tuned from 0.5 to 25GHz; the IC works well with any 2nd IF up to 25GHz. There is 8dB to 9dB conversion loss over bandwidth and 21-23 dBm IIP3 over most of bandwidth, with a slight decrease between 20- 22 GHz, again due to the low-frequency roll off of the LO driver amplifier.

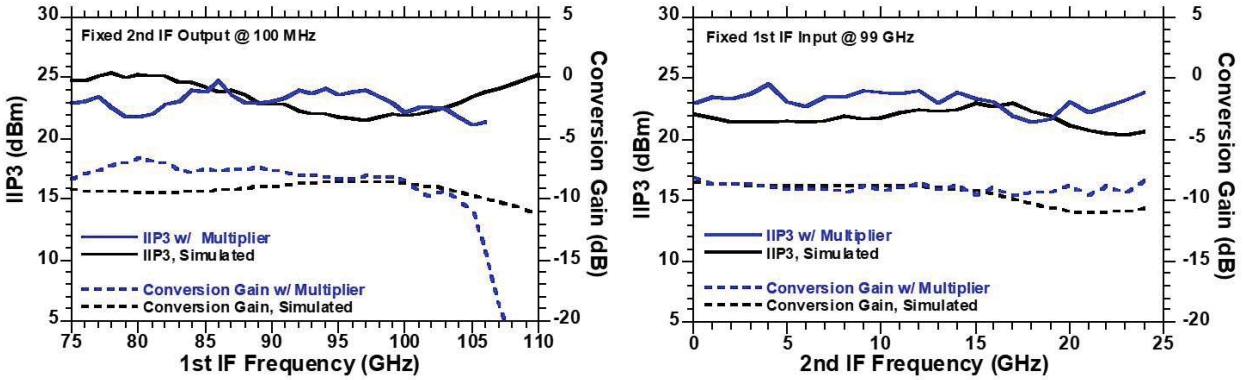


Figure 21: Measured Characteristics of the Phase 1 ICs in Downconversion

One key limit of the phase 1 ICs loss in spurious-free tuning range from spurious harmonics of the LO multiplier chain. In the phase 1 designs, these were as strong as -8.5dBc at ~8.5GHz offset from carrier. The phase 2 designs address this limitation, developing new multiplier topologies to do so. The new multipliers work as designed; unfortunately, an error in the phase 2

full IC implementation prevented demonstration on the full IC.

4.2 Phase 2 Dual-Conversion Receiver: Measurement Results

We now turn to phase 2 results. Figure 22 shows a die photograph of the downconversion IC using the power-combined mixer. In testing, it was found that the mixer oscillated, despite not showing such characteristics during simulation. This prevents useful IC operation, and hence these ICs were not further tested.

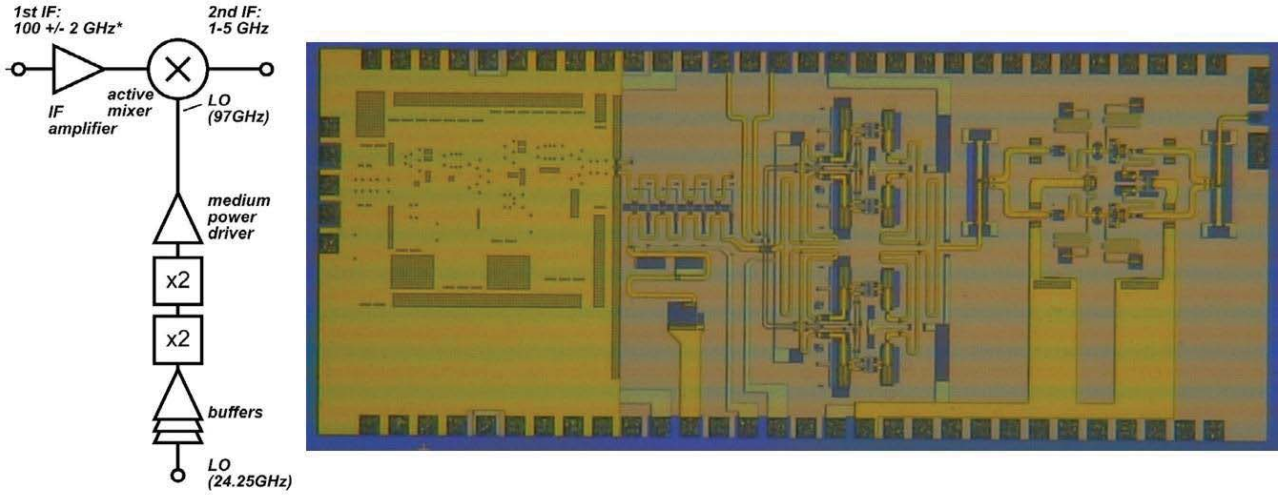


Figure 22: Phase 2 Downconversion IC using the Power-Combined Mixer
The mixers suffered from RF instability.

We now move on to the frequency multipliers. Figure 23 shows the block diagram and mask layout of the first 2:1 frequency multiplier.

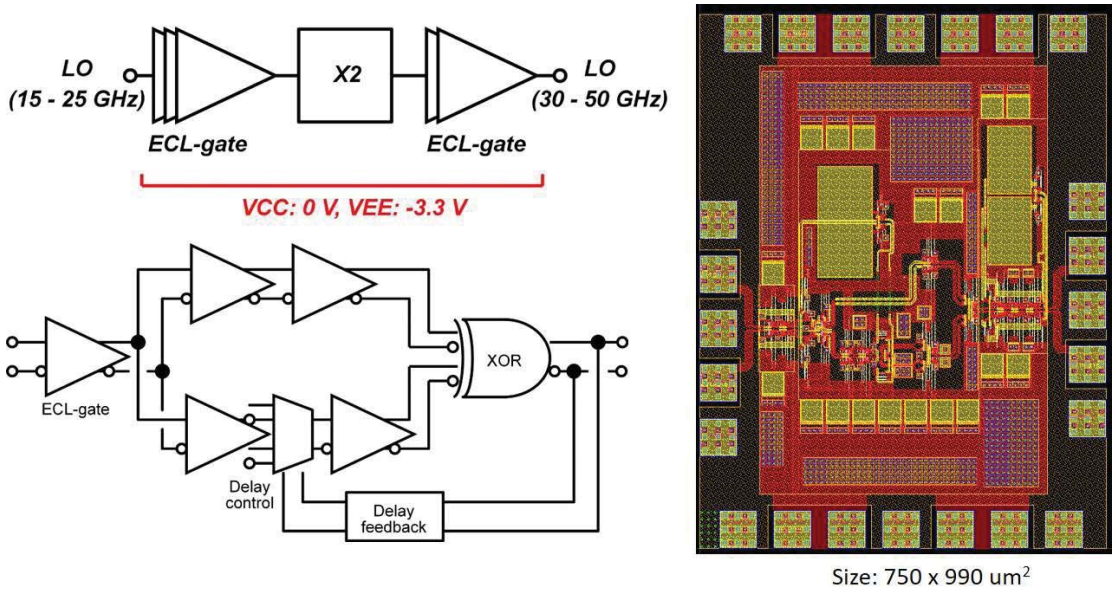
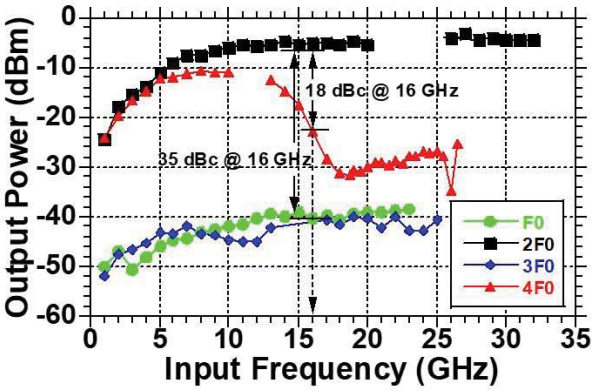
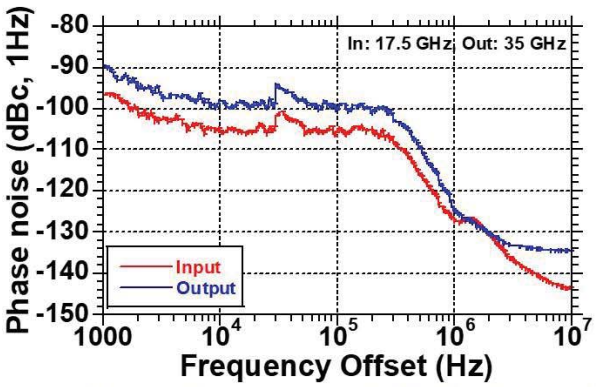


Figure 23: First Frequency Doubler Stage: Block Diagram and IC Layout

Figure 24 shows measurements of the first frequency multiplier. Available test equipment did not allow us to test all output harmonics over the full 15-25GHz target input frequency range, but the 4th harmonic is suppressed by better than 18 dB worst-case over the tuning range, and it typical better than 25dBc. The more troublesome adjacent 1st and 3rd harmonics are suppressed by approximately 35dBc. The measured phase noise is instrument-limited at -100dBc(1Hz) at 100kHz offset from carrier with a 35GHz output. This is excellent.



Output harmonic power vs Input Frequency



Measured phase noise at 17.5 GHz input and 35 GHz output frequencies.

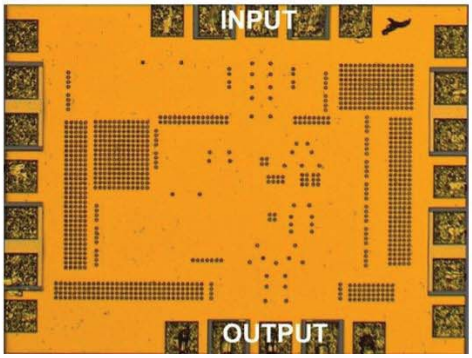


Figure 24: First Frequency Doubler Stage: Measurements and Die Photo

Figure 25 shows the block diagram and mask layout of the 2nd frequency multiplier, this is designed for a 30-50GHz input.

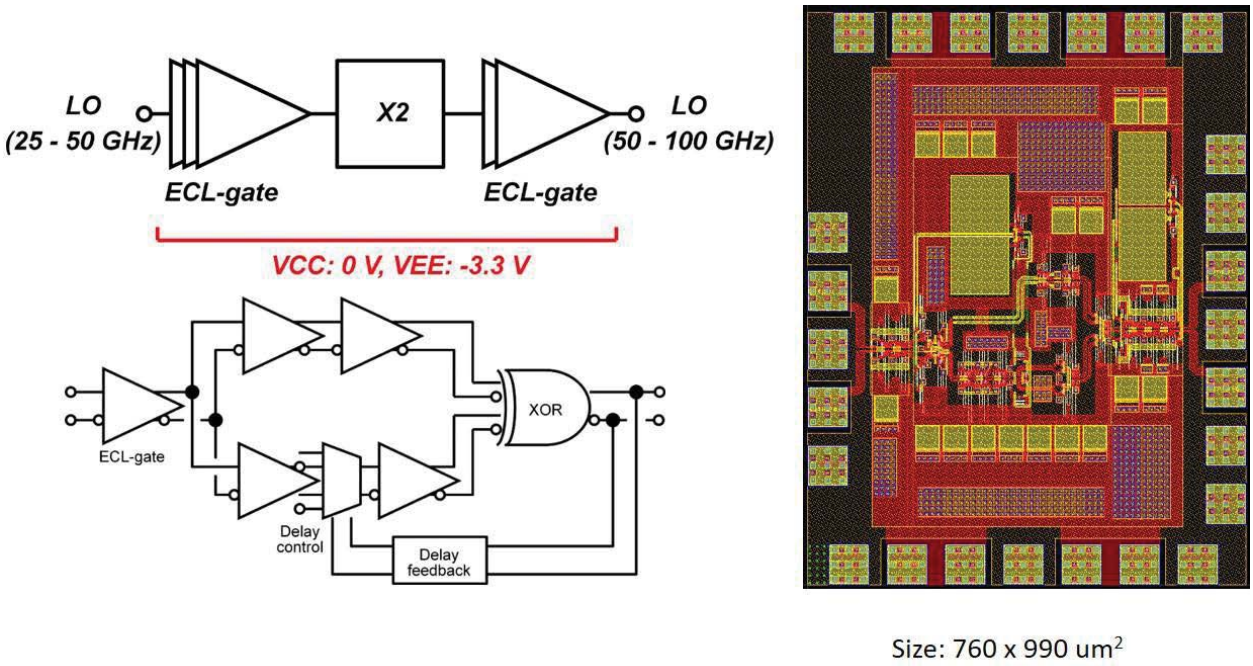


Figure 25: Second Frequency Doubler Stage: Block Diagram and IC Layout

Figure 26 shows the measured performance of the 2nd frequency multiplier. Though not as good as simulation, performance remains excellent. There is >25 dBc rejection of the 1st harmonic and at least 25 dBc rejection of the 3rd harmonic, at least when it lies below the 108 GHz limit of our high-frequency mixer. The IC draws 242 mZ from a -3.3V supply

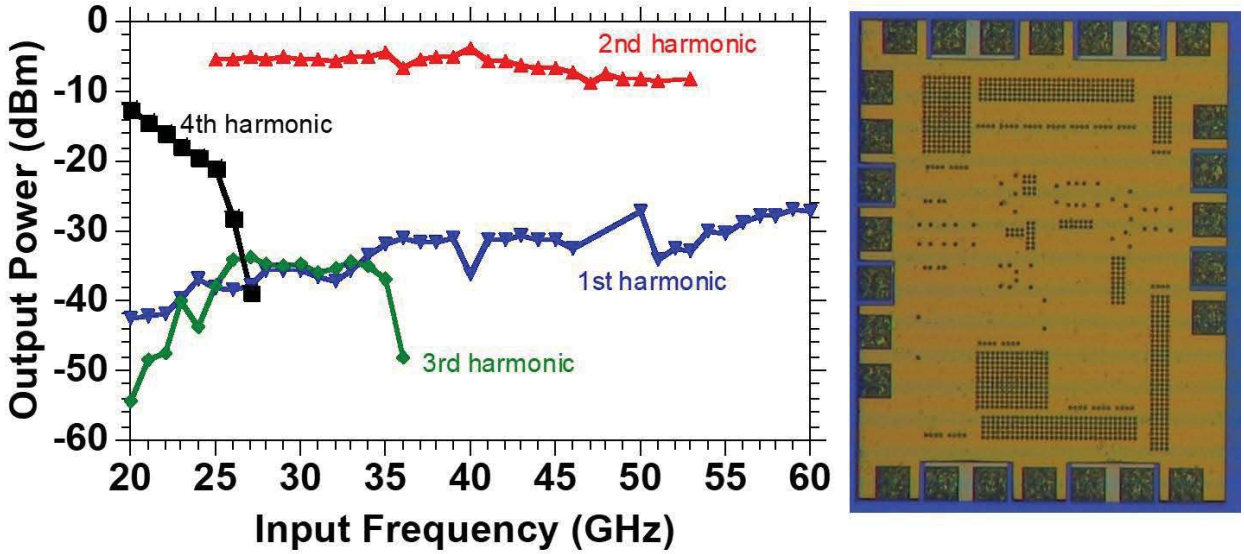


Figure 26: Second Frequency Doubler Stage: Measurements

Figure 27 shows the mask layout, block diagram, and IC photo of the 4:1 frequency multiplier, this formed from two cascaded 2:1 frequency multipliers. The IC draws 41.2 mA from a 3.3V supply, 412 mA from a -3.3V supply, and 13.6mA from a 3.3V supply. This contains a design

error which carries over to the full downconversion ICs: the DC level of the output of the 1st multiplier is not isolated from the DC level of the input of the second multiplier by a DC blocking capacitor. Because of this, the DC feedback loops of the two multipliers interfere with each other, and spurious harmonic rejection is lost.

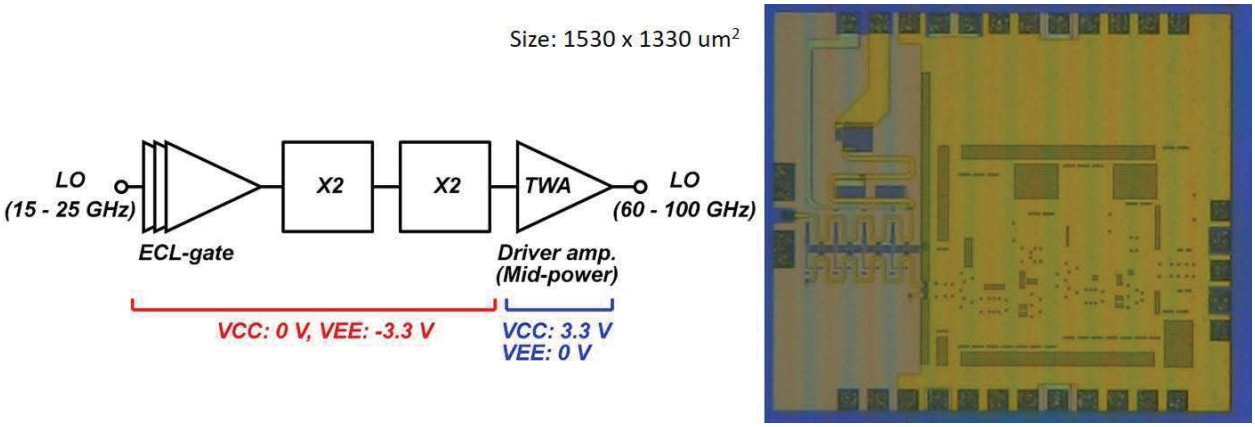


Figure 27: 4:1 Frequency Multiplier Stage: Block Diagram and Die Photo

Figure 28 shows the measured performance of the 4:1 frequency multiplier. As a result of the failure to DC isolate the two stags, the 2nd harmonic is very strong, and the 3rd and 5th harmonics are relatively strong.

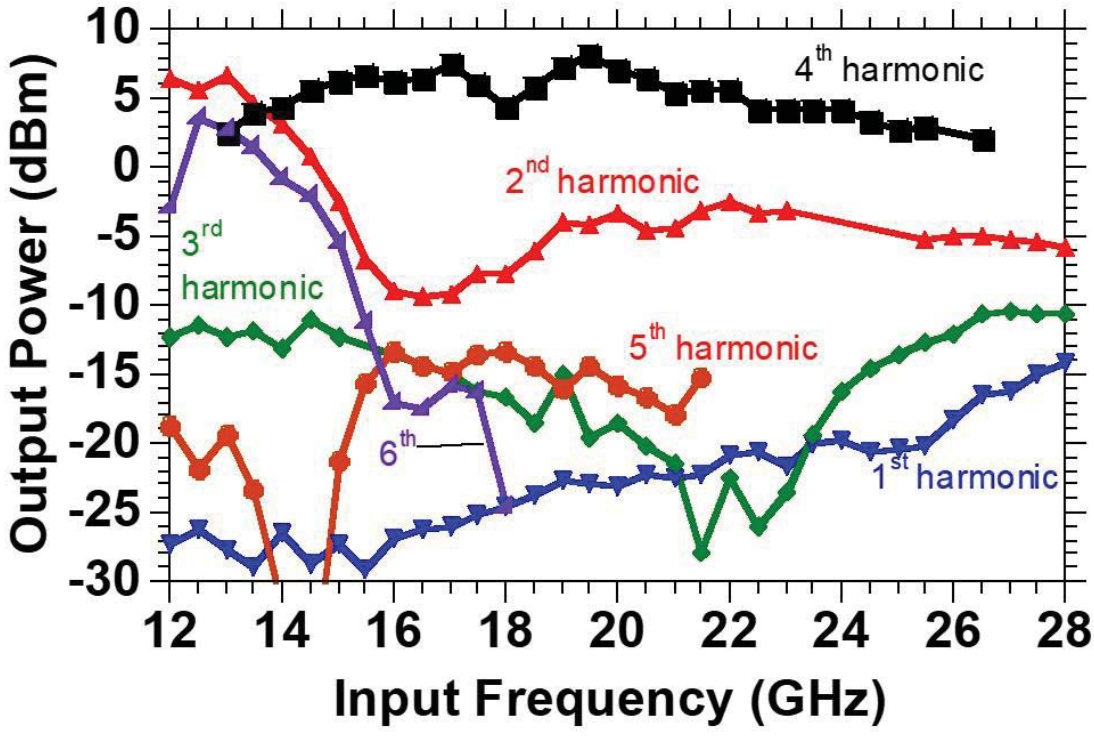


Figure 28: 4:1 Frequency Multiplier Stage: Measurements

We now turn to measured results for the version of the full ***passive*** upconversion/ downconversion ICs, these using the passive diode mixer and the digital/feedback frequency multiplier chain. Figure 29 compares the mask layout and IC photograph of the upconversion IC. The die is 3.3mm by 1.2mm. Figure 30 gives a block diagram and the DC power consumption.

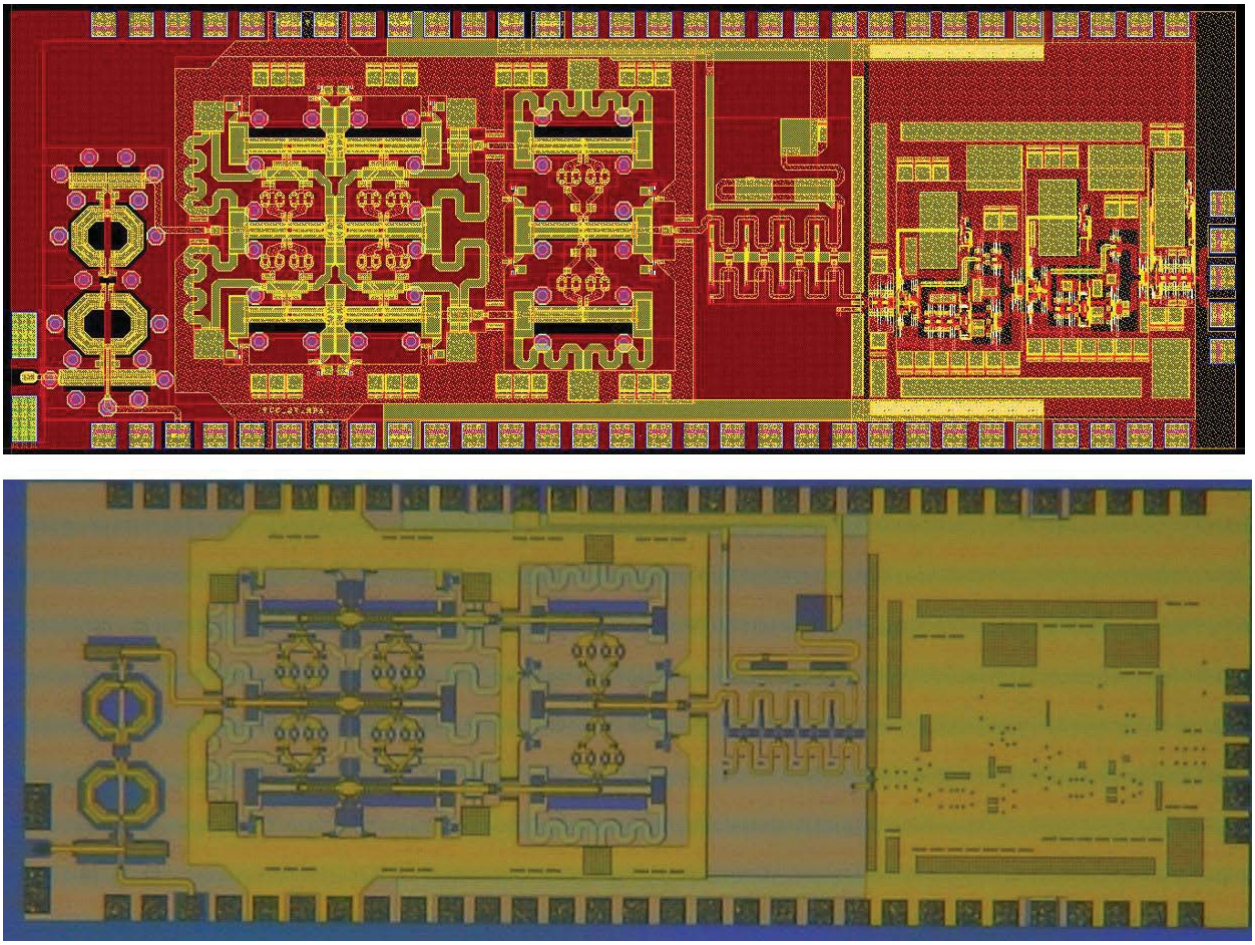


Figure 29: Upconversion/Downconversion Block using Passive Mixer: IC Layout and Die Photo

The IC is 3.31mm by 1.18mm.

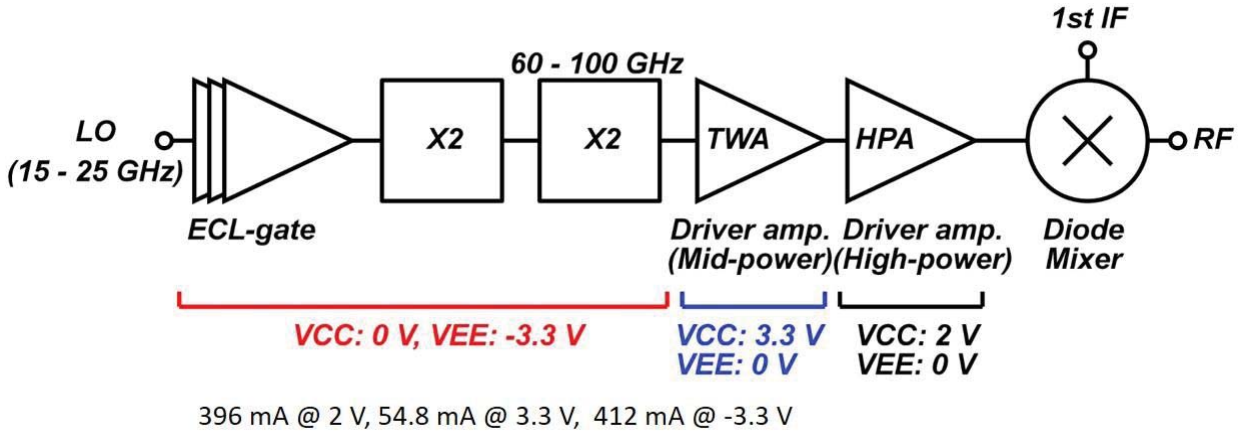


Figure 30: Upconversion/Downconversion Block using Passive Mixer: Block Diagram and Power Consumption

In a full dual-conversion receiver, two of these ICs would be used, one for upconversion and one for downconversion, with a 100GHz or 94GHz IF amplifier and filter placed between them. We first examine performance of the IC operating in upconversion. Figure 31 shows measurements with a fixed 100GHz first IF, and with the input RF frequency swept between 0.5 and 22GHz. Over this bandwidth, the IIP3 varies from ~28dBm to 19dBm, while the measured conversion loss varies from 3-6dB. This shows that the receiver works well with RF input frequencies varying over a DC-22GHz range. Because the mixer is passive, the noise figure will be equal to the measured insertion loss. We however note that the insertion loss measurement has ~+/- 2dB uncertainty, and hence state that 9dB is a conservative bound for the insertion loss hence noise figure.

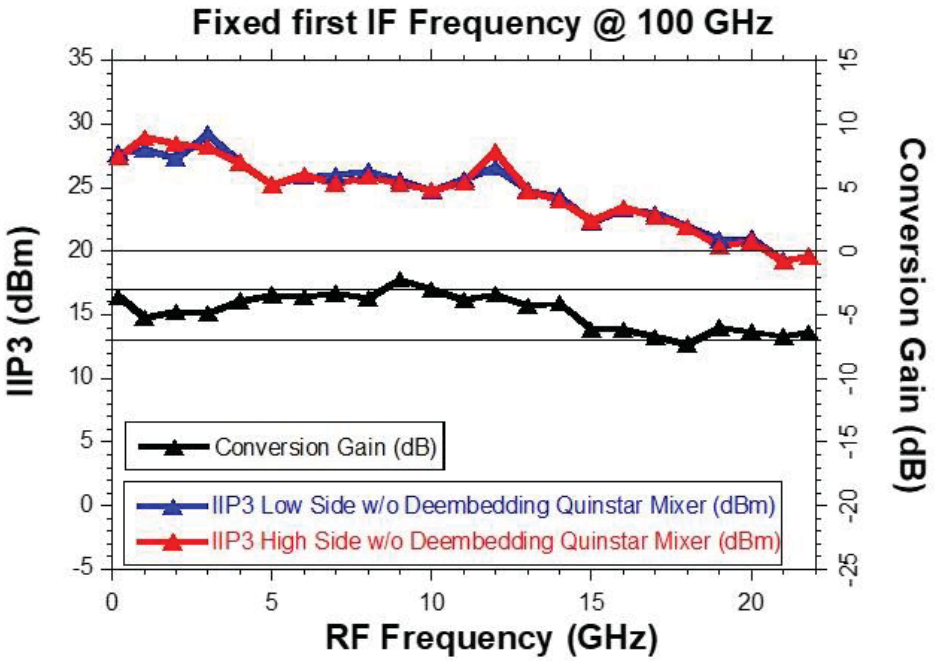


Figure 31: Upconversion Block using Passive Mixer: Measured Results with a fixed 100GHz IF Frequency

As this is critical data, the RF sweep of IIP3 and insertion loss is shown at greater magnification in Figure 32. This shows the insertion loss and noise figure with a fixed 200MHz RF input and with the first IF swept over 75-105GHz. IP3 and insertion loss are similar to the earlier measurement, showing that the IC works well for 1st IF frequencies between 75-110GHz. Figure 33 shows that the insertion loss remains small and relatively constant of over a broad DC-40GHz bandwidth, suggesting that the ICs could be used in very broadband applications. We do not have the signal sources and power combiners necessary to measure IIP3 over the 22-40GHz bandwidth.

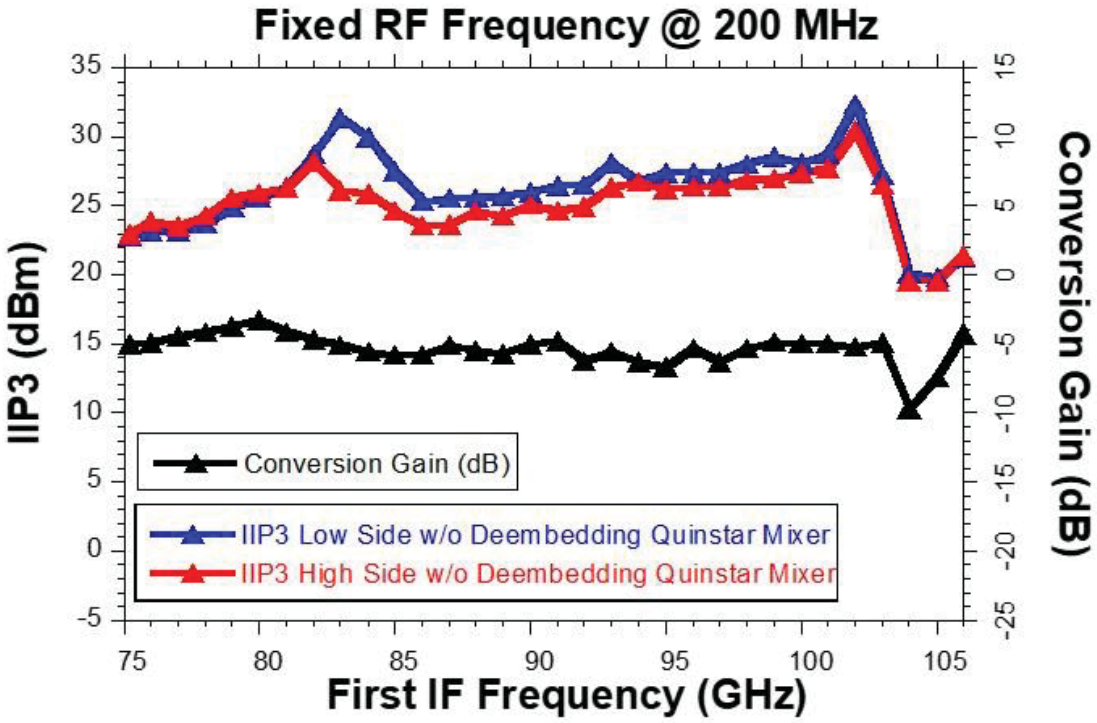


Figure 32: Upconversion Block using Passive Mixer: Measured IP3 and Conversion Gain with a fixed 200MHz RF Frequency

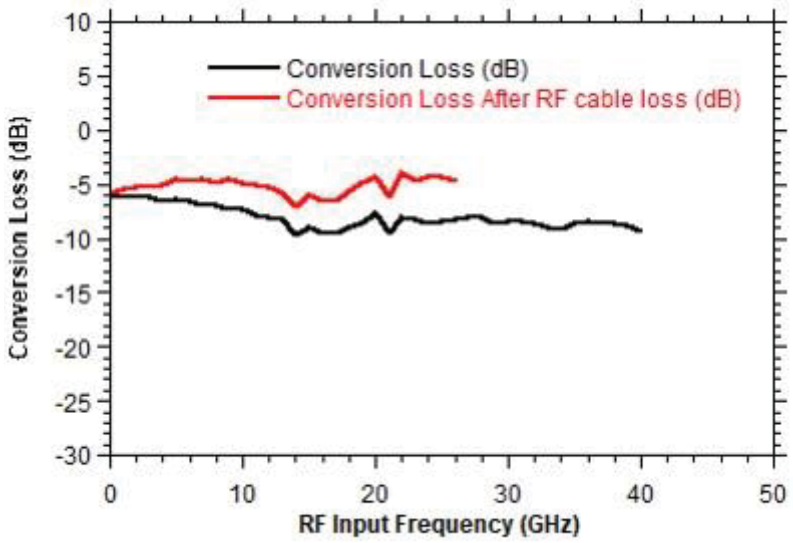


Figure 33: Upconversion Block using Passive Mixer: Measured Conversion Gain over a Broad DC-40GHz Frequency Range

The black curve includes the effect of RF cable losses on the probe bench; the red curve corrects for such losses.

In a similar fashion, we measured the frequency-conversion IC in downconversion mode, downconverting from the 1st IF to either a second IF frequency or to baseband. Figure 34 shows the downconversion block performance with a fixed 100GHz first IF, and with the second IF swept from very near DC (a few 10's of MHz) to 25GHz. The measured conversion loss, hence noise figure, is 3-6dB; given a ~ +/- 2dB measurement uncertainty, a conservative upper bound on the insertion loss and noise figure is 8dB. The IIP3 is better than 20dBm over the full measured range of second IF frequencies.

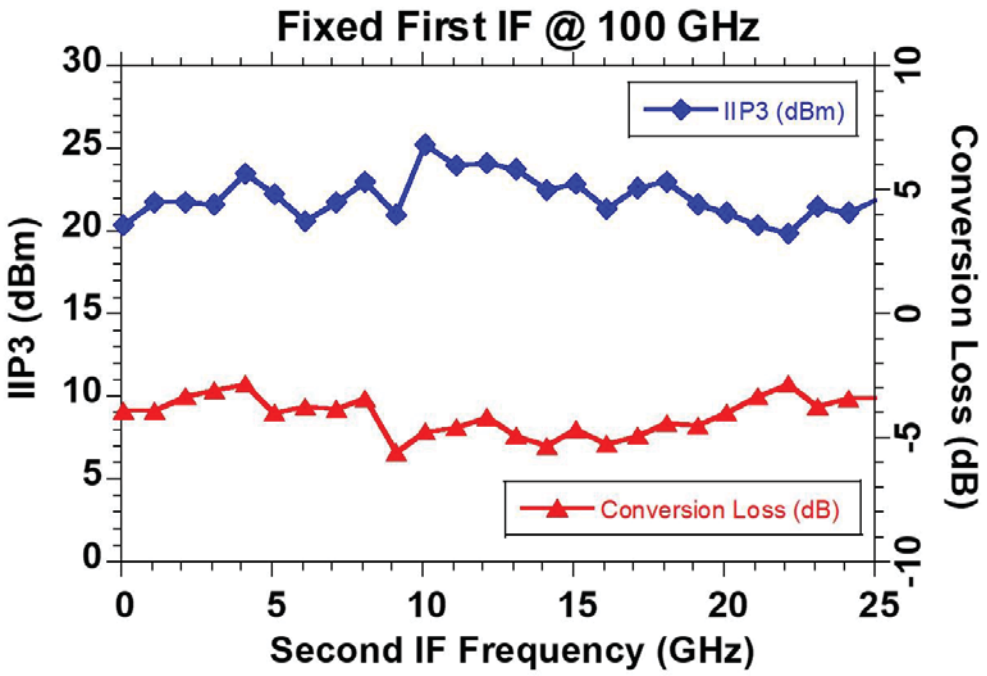


Figure 34: Downconversion Block using Passive Mixer: Measured IP3 and Conversion Gain

The final set of measurements test the spurious receiver responses with the upconversion and downconversion blocks connected with an external IF section (Figure 35). Please recollect because the high-performance InP IF amplifier was included only on the downconversion blocks which used the power-combined mixer, and that this mixer failed experimentally due to microwave oscillation. Consequently, in the full receiver demonstration, the IF section must use a commercially-available W-band amplifier. The low IP3 of this external IF amplifiers, together with the high 94GHz losses arising from the W-band probes and coaxial cables connecting the IF amplifier and filter to the two ICs, results in poor receiver dynamic range. Such losses would be much smaller in an assembly packaging the two ICs with a monolithic IF amplifier and off-wafer filter. The purpose of this measurement is therefore only to determine the receiver spurious tuning responses.

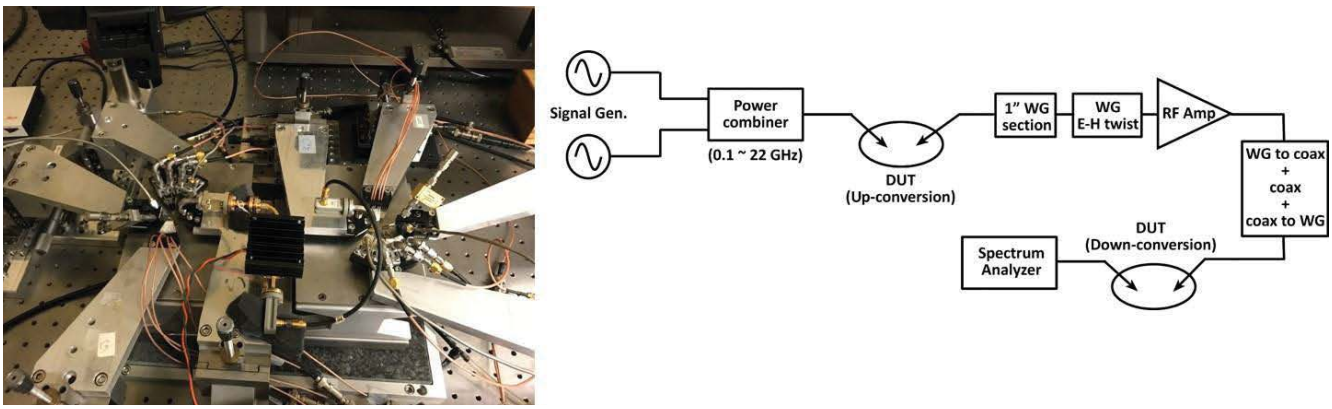


Figure 35: Full Phase 2 Dual-Conversion Receiver Measurement

The resulting data is shown in Figure 36 and Figure 37. In these measurements, the first LO frequency is first set to tune the receiver to a particular RF input frequency. With the LO frequency then held constant, the input RF frequency is then swept over a DC-40GHz bandwidth, and relative receiver response is then measured as a function of input frequency. With the receiver tuned to 2GHz, there are spurious responses below 1GHz, and at ~21GHz and 25GHz, these at slightly better than -30dBc. The latter responses are due to the spurious 3rd and 5th harmonics at the output of the LO frequency multiplier. With the receiver tuned to 10GHz, the responses due to the spurious 3rd and 5th harmonics increase to approximately - 24dBc. As the receiver is tuned to progressively higher input frequencies, the relative strength of the spurious responses due to the 3rd and 5th LO harmonics increases, and, eventually, spurious responses due to the LO 6th harmonic appears within the receiver bandwidth.

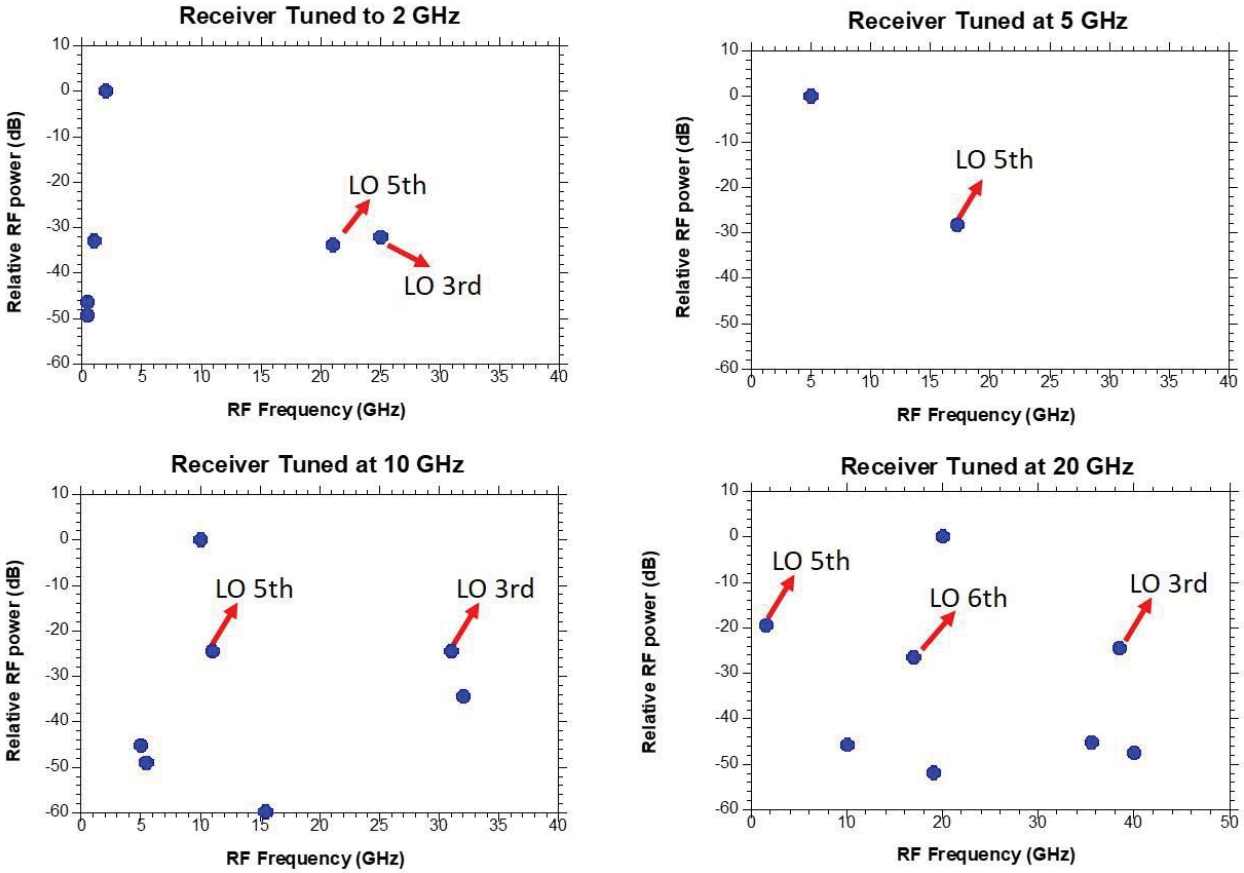


Figure 36: Full Phase 2 Dual-Conversion Receiver Measurement: Receiver Spurious Responses

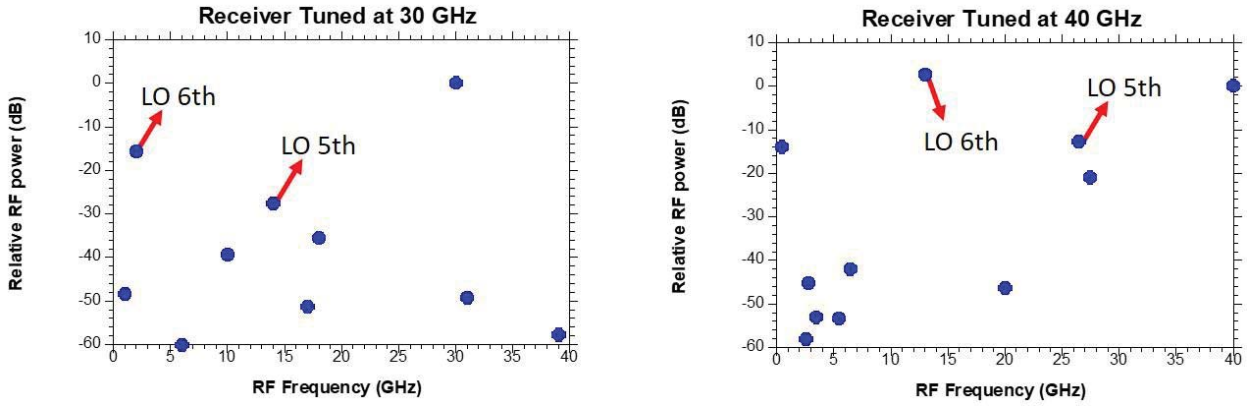


Figure 37: Full Phase 2 Dual-Conversion Receiver Measurement: Receiver Spurious Responses

Please note that the poor receiver spurious response is entirely due to the layout error in directly connecting the first and second frequency multiplier stages without DC coupling. Had this been done (Figure 24 and Figure 26), the adjacent 3rd and 5th harmonic responses would have been suppressed by -35dBc, even without filtering. With simple LC filters at the outputs of the multipliers, this could have been further enhanced. The omission of the DC blocking capacitors and filters was a simple, regrettable, and costly design error.

4.3 Discussion

The phase 1 receivers demonstrated that high dynamic range and high tuning range, sufficient for widely-tuned dual-conversion receivers, could be obtained from InP heterojunction bipolar transistor (HBT) technology at the 130nm node. Spectral purity of the phase 1 LO source frequency multiplier chain was, however, compromised by the simple multiplier architecture. The phase 2 designs used a much more sophisticated multiplier design, and, with correct implementation, can potentially provide very high spurious-free dynamic range.

In the phase 2 designs, the upconversion ICs have 19-29dBm IIP3 and better than 9dB insertion loss and noise figure over at 0.5-22GHz input RF tuning bandwidth; conversion loss remains low over a DC-40GHz bandwidth. The downconversion ICs have similar performance.

From this measured performance, we compute that, preceded by an LNA with 18dB gain and 2dB noise figure, the overall receiver would have 3.8dB noise figure and 5dBm IIP3 for signals outside the 2nd IF filter bandwidth. If the ICs were preceded by an LNA with 12dB gain and 2dB noise figure, the overall receiver would have 6.7dB noise figure and 11dBm IIP3 for signals outside the 2nd IF filter bandwidth. This is excellent performance. Had we avoided the error in interconnecting the frequency multiplier stages in the phase 2 designs, the ICs would also have had excellent spurious-free tuning range.

5. CONCLUSIONS

This work, under the DARPA ACT program, had two motivations. The first, to produce a general-purpose IC or chip set from which a wide range of custom high-performance transmitters and receivers can be quickly and cheaply developed by the simple addition of application-specific LNAs and power amplifiers having desired center frequency, output power and noise. The second to develop a widely-tunable transceiver for wideband (DC-40GHz or beyond) surveillance.

Although these goals were not demonstrated on the full integrated receiver, the individual IC blocks without question demonstrate that the two DARPA ACT goals can be attained with a dual-conversion architecture.

First, frequency conversion ICs, upconverting from DC-22GHz to 94GHz or 100GHz, and downconverting from 94 or 100GHz to any second IF between DC and 22 GHz, were demonstrated. The upconversion ICs have better than 9dB noise figure and 19-29dBm IIP3 over the tuning bandwidth. The downconversion IC performance is similar.

If we take this measured performance, we compute (Figure 1) that, preceded by an LNA with 18dB gain and 2dB noise figure, the overall receiver would have 3.8dB noise figure and 5dBm IIP3 for signals outside the 2nd IF filter bandwidth. If the ICs were preceded by an LNA with 12dB gain and 2dB noise figure, the overall receiver would have 6.7dB noise figure and 11dBm IIP3 for signals outside the 2nd IF filter bandwidth. This is excellent performance.

The dual-conversion receiver requires LO frequency multipliers, and these generate spurious harmonics which produce receiver spurious tuning responses. We have demonstrated (15-25GHz)→(30-50GHz) and (30- 50GHz)→(60-100GHz) multipliers. Even without external filters, the first of these multipliers suppresses adjacent harmonics by 35dBc, while the second multiplier suppresses its adjacent harmonics (which are more widely spaced in frequency than that of the 1st multiplier) by >25dBc. Had DC isolation and interstage filters been used in the overall receiver, the spurious tuning responses would have been suppressed by circa 40-45dBc. This would have been an excellent broadband surveillance receiver.

6. RECOMMENDATIONS

The DARPA ACT program has ended, so further effort is not possible. If the DoD has need for high-dynamic-range broadly-tunable (~0.5-40GHz) surveillance receivers, it would require very little design effort to add filters and interstage DC blocking between the two frequency multipliers. This would produce an excellent high-performance receiver.

7. BIBLIOGRAPHY

The following publications, in the literature, report work under the ACT program:

S. Kim, R. Maurer, M. Urteaga and M. J. W. Rodwell, "A High-Dynamic- Range W-Band Frequency-Conversion IC for Microwave Dual-Conversion Receivers," 2016 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS), Austin, TX, 2016, http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=7751022&isnum ber=7750996

R. Maurer, S. Kim, M. Urteaga and M. J. W. Rodwell, "Ultra-Wideband mm-Wave InP Power Amplifiers in 130 nm InP HBT Technology," 2016 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS), Austin, TX, 2016 http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=7751077&isnum ber=7750996

R. Maurer, S. Kim, M. Urteaga and M. J. W. Rodwell, "High-Linearity W- Band Amplifiers in 130 nm InP HBT Technology," 2016 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS), Austin, TX, 2016

The additional papers have been accepted for publication:

"High-Spurious-Harmonic-Rejection 32-53 GHz and 50-106 GHz Frequency Doublers using Digital Logic and DC Negative Feedback", Seong-Kyun Kim, Arda Simsek, Miguel Urteaga, Mark J.W. Rodwell, *to be presented*, 2018 European Microwave Conference - 25th - 27th September, Madrid.

"A Dual-Conversion Front-End with a W-Band First Intermediate Frequency for 1-30 GHz Reconfigurable Transceivers", Arda Simsek, Seong-Kyun Kim, Ahmed S. H Ahmed, Robert Maurer, Miguel Urteaga, and Mark J. Rodwell, *to be presented,* 2019 Radio and Wireless Week, 20- 23 January, Orlando, Fl.

LIST OF ABBREVIATIONS, ACRONYMS, AND SYMBOLS

ACRONYM	DESCRIPTION
ACT	Arrays and Commercial Timescales
DARPA	Defense Advanced Research Projects Agency
DC	Direct Current
DHBT	Double Heterojunction Bipolar Transistor
DoD	Department of Defense
ECL	Emitter-Coupled Logic
EW	Electronic Warfare
FET	Field-Effect Transistor
HBT	Heterojunction Bipolar Transistor
IC	Integrated Circuits
IF	Intermediate Frequency
IIP3	Third-Order Input Intercept Point
InP	Indium Phosphide
IP3	Third-Order Intercept Point
LNA	Low Noise Amplifier
LO	Local Oscillator
MOS	Metal Oxide Semiconductor
NRE	Non-Recurring Engineering
op-amp	Operational Amplifier
PLL	Phase Locked Loop
RF	Radio Frequency
UCSB	University of California, Santa Barbara
UCSB	University of California, Santa Barbara
VCO	Voltage-Controlled-Oscillator
YIG	Yttrium-Iron-Garnet