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HIGH REL/SPEED/HARSH ENVIRONMENT VCSEL DEVELOPMENT

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Final Report

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14. ABSTRACT
The objective of this project is to conduct fundamental research of a new Vertical Cavity Surface Emitting Laser (VCSEL) technology, specifically a High Heat Flow Cavity approach. The High Heat Flow Cavity VCSELs are expected to bring new capabilities to demanding applications requiring highly reliable, high-speed arrays that may be required to operate reliably in extreme temperature environments. Commercial space communication providers, for example, have these requirements for commercial space satellites and other military platforms. Low cost, higher efficiency laser sources would benefit many consumer applications, including medical applications, industrial applications, high-speed communications, and scientific research applications.

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Photonics; Laser; Vertical Cavity Surface Emitting Laser; VCSEL; High Speed Optical Interconnects; High Reliability

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1.0 SUMMARY

Title: High Rel/Speed/Harsh Environment VCSEL Development

Principal Investigator: Dr. Dennis G. Deppe

Research Objectives:

The overall objective of this three-year project is to conduct fundamental research and fundamental reliability studies that will lead to the development of a new Vertical Cavity Surface Emitting Laser (VCSEL) technology that can operate reliably at very high speed and would be suitable for harsh environments. Specific objectives include:

- University of Central Florida (UCF) will develop the epitaxial materials that will be used in this project that will be based on the lithographic process. The lithographic process will be adapted to 3" wafers for growth and masking to match industry needs for reliability testing. Epitaxial growths of the VCSELs will be performed and the VCSELs tested. Processing will be developed so that testing can be performed on the reliability to verify Continuous Wave VCSEL performance.

- Testing will be performed under high temperature and high current density stress conditions to determine the limits of the new VCSEL. Temperatures in excess of 200 C and operating current densities in excess of 200 kA/cm^2 will be used to determine these upper limits of reliability. These test conditions are known to exceed that possible for the existing commercial VCSEL technology now used in high speed optical interconnects.

- Packaging of VCSEL samples will also be produced. Preliminary reliability testing of the packaged samples, with reports of the findings will be produced. These reports will include deliverables on the project at intervals designated by the agency, and publications in the scientific literature and conference presentations. It is understood that this work is a research effort and is undertaken on a best-effort basis.

Synopsis of Research:

This project was funded for only Year 1 of a study of reliability and suitability of a new laser technology for applications that include very high speed directly modulated laser sources for optical communication in various space vehicles and platforms. These optical communication applications require efficient, high-speed laser sources that can produce very high reliability. The standard technology is now oxide vertical-cavity surface-emitting lasers (VCSELs) with operating speeds as high as 25 Gbps per channel. Arrays of the oxide VCSELs can be used to further increase speed and perform interconnecting and switching. Next generation VCSEL sources are targeting 50 Gbps per channel, and even higher speeds are desired. Efficiency (bit energy) is also a critical factor.

Higher speed laser sources will require higher operating current density and smaller active volume than now used for oxide VCSELs. The operating requirements will place a greater demand on laser reliability, due to the more stringent operating conditions. Laser diode reliability is usually the limiting factor in reliability of the high-speed optical data links. Space applications place even greater demands on reliability than now used in much of the commercial sectors such as data centers and high performance computers.

The new laser technology replaces the oxide aperture now used in high speed VCSELs with an oxide-free, epitaxial aperture. The epitaxial aperture is lithographic and can scale the VCSEL to small size for low bit energy and low parasitics. The new lithographic VCSEL dramatically reduces the internal operating temperature of the laser, a key parameter needed for high reliability and high speed.

In the Year 1 of this project we developed and demonstrated the new VCSEL process on 3" substrates. The 3" substrate process was being developed to enable fabrication and testing by a military supplier of high speed VCSELs that can meet military specifications. In the Year 1 the project was interrupted by downtime on the epitaxial growth system. In addition personnel changes in the Air Force Research Laboratory (AFRL) led to transfer of the AFRL program monitor to another military laboratory. As a result the project was performed only through the first year, along with a no cost extension to the project. In the no-cost extension of the Year 1 project and funding additional work was completed simulating the new VCSEL technology for applications that require high reliability. One of these is cryogenic optical links that may be used in applications of data transfer for cameras using focal plane arrays cooled to 77 K. Another is cooled to 4 K for use with superconducting computing circuits. This work is also presented and discussed in this report.

2.0 INTRODUCTION

The VCSEL's light versus current curves is the central test measurements in determining reliability. Because of their low internal operating temperatures these VCSELs produce record high power levels and record high stimulated-emission rates. The reduction in junction temperature that comes from reducing the device size and/or eliminating the oxide is also shown. For a given operating current density the junction temperature reduces for a given current density as the VCSEL size is reduced. For 3 μm VCSELs, the lithographic VCSEL is measured to have a factor of two lower temperature rises for a given operating current density, relative to the oxide VCSEL.

Extensive research shows that VCSELs generally fail through wear-out and follow an empirical trend of an acceleration factor for operating current density and junction temperature [1]-[3]. In some important cases oxide failure due to corrosion also occurs [4]. By measuring at sufficiently high temperature and current density accelerated aging results can then be used to extract an expected mean time to failure (MTTF) for the targeted operating conditions. In well-developed commercial oxide VCSELs the current acceleration factor is typically n = 2, and the activation energy is E_a ~ 1 eV from most studies. These parameters track how the VCSEL's junction temperature causes device failure. The high heat flow cavity (HHFC) dramatically drops the junction temperature for high operating current density over the VCSEL. Since the activation energy is expected to be similar or higher due to lower internal strain, this is expected to lead to increased reliability.

Preliminary studies are already indicating that the HHFC can increase reliability in harsh environments. These show that while both the commercial oxide VCSELs and the lithographic VCSELs show a decrease in power of a few percent within the first 20 hours of high temperature stress testing, the oxide VCSELs continues to fail, while the lithographic VCSELs show little change after the first 20 hours. Testing was continued on one of the lithographic VCSELs that now has operated close to 300 hours with no measurable change in characteristics. Our estimates based on junction temperature at 85C and bias current density of 50kA/cm^2 and are mean time to failures in excess of 10^6 hours using known acceleration factors for current and activation energy. The results show clear evidence of the ability for VCSELs that use the HHFC process to operate at very high bias current density at high temperature with needed reliability.

The reason for the higher reliability of the HHFC VCSEL is its lower junction temperature combined with low internal strain. At the 150 C stage temperature the HHFC VCSEL reaches a junction temperature of 167 C at the 140 kA/cm^2 operating current density. The oxide VCSEL junction temperature in contrast is close to 250 C. This ability to cool the junction increases the reliability. Therefore the HHFC VCSELs are expected to bring new capabilities to demanding applications requiring highly reliable, high-speed arrays that may be required to operate reliably in extreme temperature environments. Boeing and others for example have these requirements for space satellites and other military platforms.

VCSELs have been extensively studied for their high-speed modulation and very good modeling is available of the intrinsic frequency response. Their intrinsic response is limited by self-heating. The most important results are at 85 C or higher temperature. For military applications this upper temperature can be much higher. As the temperature increases the maximum intrinsic modulation speed becomes reduced.

The lithographic VCSEL provides greater cooling to the active junction and so has greater intrinsic speed for a given operating temperature [5]-[8]. The speed is expected to go up dramatically as the size is reduced. This is consistent with modeling for the frequency response that accounts for the temperature rise in the VCSEL. Essentially the intrinsic response increases when the bias current density can be increased to increase the stimulated emission rate. Their maximum room temperature power conversion efficiencies are close to 50%. Intrinsic responses based on stimulated emission rates, internal temperatures, and cavity bandwidths are well beyond 50 GHz for sizes less than 5 μm diameter.

The current 25G oxide VCSEL size is ~ 7 µm diameter. By reducing the device size while maintaining high efficiency, the intrinsic speed should increase significantly. The small signal bandwidth of the 3 µm lithographic VCSEL at 85 C is estimated at 90 GHz, and we expect the device to be limited in bandwidth by electrical parasitics. However, the electrical parasitics can also be reduced with decreasing device size. We estimate that the electrical parasitic limited bandwidth for the 3 µm device can exceed 50 GHz, relative to 28 GHz that has been measured for the 7 µm oxide VCSEL.

Therefore high-speed VCSEL sources in excess of 50G operating at high temperature with high reliability are an expected outcome of this technology. Electrical parasitics have also been analyzed. Reducing device size reduces electrical parasitics and increases bandwidth. Therefore controllable size reduction that comes from the lithographic process both reduces the internal device operating temperature and reduces the electrical parasitics.

High speed requires high current density, and the high current density produces high internal temperatures in oxide VCSELs for both commercial and laboratory devices [4], [8]. The results from Chalmers University [3] show the optical power vs. current for heat sink temperatures for room temperature (RT) and 85 C along with the internal device temperatures for the different operating conditions. The VCSEL obtains its highest speed at its highest bias level just before thermal rollover, or at ~12 mA for RT operation and ~10 mA for 85 C. The internal device temperature at these high drive levels reach more than 110 C for RT heat sink operation, and 150 C for 85 C operation. The data speed is above 40G for both temperatures, but sufficiently close to its maximum operating conditions that poor reliability is expected. In fact, electrical parasitics due to the 7 µm size limit its RT bandwidth to ~28 GHz, while self-heating limits the device's 85C bandwidth to ~22GHz.

The internal oxide effectively confines the optical mode and electrical current, the thermally insulating property of the buried oxide traps heat within the VCSEL cavity. The heat, which is mainly due to resistive heating and free carrier absorption that occurs in the p-mirror, gets trapped in the p-mirror due to the intra-cavity oxide layer shown in red. This trapped heat must mainly now escape downward through the oxide aperture opening. As a result of the trapped heat and heat flow, the cavity and junction temperature increase. And because high-speed VCSELs are driven to high current density, this self- heating effect is strong. At sufficiently high current density, thermal detuning of the cavity and gain lead to thermal rollover in the output power, and saturation in the stimulated emission rate. At this point the VCSEL can go no faster in speed. In fact, speed saturation occurs slightly below thermal rollover since the differential gain also decreases with increasing junction temperature.

The lithographic technology is planar with no internal oxides, and let's heat escape laterally inside the laser. The resulting device has dramatic advantages in its heat flow properties [5]-[8] which are responsible for a reduced junction temperature. The improved heat flow comes partly from eliminating the buried oxide layer that limits heat flow, but with the ability to use AlAs as the low index material in the p-mirror. AlAs is among the highest thermal conducting materials of the III-Vs. The ability to use it in the p-mirror places the high thermal conductivity AlAs layers directly at the heat sources to provide cooling through lateral heat flow. This is not possible with oxide VCSELs that must use sufficiently low Al content in the p-mirror to prevent oxidation in all but the desired oxide aperture layer. This additional cooling drops the thermal resistance of the new technology to less than half that of oxide VCSELs, and is responsible for the high power and stimulated emission rate. This improved thermal performance becomes very important in achieving high reliability at the higher current densities required for 50G and higher data speeds.

Compared to the oxide VCSELs, the high heat flow cavity that results enables very high drive current density, and the maximum current density increases as the VCSEL size is reduced. Note that the powers and drive levels of even the 4 µm VCSEL exceed the 7 µm oxide VCSEL above. The 4 µm size can be driven to 95kA/cm^2. The intrinsic response is projected to reach 50G at ~ 2 mA bias at 85 C for the 4 µm VCSEL. The 4 µm, 3 µm, and 2 µm are each of interest in speed testing in the Phase I, though emphasis is placed on the 4 µm sizes. These are the speeds needed to reach 50G, 100G and greater. Reliability testing becomes an important step in the research to verify operation under high-speed drive levels for harsh military environments.

The lithographic VCSELs show record high power and drive levels for their small sizes, as needed for high-speed operation. These are well beyond what has been possible with existing oxide VCSELs operating at high speed. The thermal rollover current density exceeds the best high-speed oxide VCSELs by almost a factor of 2. The voltage drive and differential resistances are record low values for VCSELs, and much lower than can be achieved in the oxide. Therefore the thermal properties, size scaling, and electrical resistances promise very high-speed operation. Intrinsic response curves are extracted directly from the measured results for stimulated emission and active region design and internal device temperature that set differential gain.

3.0 METHODS, ASSUMPTIONS, AND PROCEDURES

A Vertical Cavity Surface Emitting Laser (VCSEL) is a type of semiconductor laser diode. It generates a laser beam emission that is perpendicular to its top surface, in contrast to conventional semiconductor laser diodes, which are edge emitting. Since VCSELs emit from the top surface of the chip, they can be tested on-wafer, which reduces fabrication costs of the devices. High power VCSELs can also be fabricated by combining elements into large two-dimensional arrays. VCSEL technology is useful for a variety of medical, industrial, and military applications requiring high power or high energy. The larger output aperture of VCSELs, compared to most edge-emitting lasers, produces a lower divergence angle of the output beam. This makes possible highly efficient coupling to fiber optics.

In this project, we propose to investigate High Heat Flow Cavity (HHFC) Vertical Cavity Surface Emitting Lasers (VCSELs). Preliminary studies are already indicating that the High Heat Flow Cavity (HHFC) Vertical Cavity Surface Emitting Laser (VCSEL) can increase reliability in harsh environments. Studies to-date show clear evidence of the ability for VCSELs that use the HHFC process to operate at very high bias current density at high temperature with needed reliability. The HHFC VCSELs are expected to bring new capabilities to demanding applications requiring highly reliable, high-speed arrays that may be required to operate reliably in extreme temperature environments. Commercial space communication providers, for example, have these requirements for commercial space satellites and other military platforms.

Our approach is based on lithographic fabrication technology. The lithographic technology is planar with no internal oxides, and allows heat escape laterally inside the laser. The resulting device has dramatic advantages in its heat flow properties, which are responsible for a reduced junction temperature. The improved heat flow comes partly from eliminating the buried oxide layer that limits heat flow, but with the ability to use aluminum arsenide (AlAs) as the low index material in the *p*-mirror. AlAs is among the highest thermal conducting materials of the III-Vs (semiconductor element group). The ability to use it in the *p*-mirror places the high thermal conductivity AlAs layers directly at the heat sources to provide cooling through lateral heat flow. This is not possible with oxide VCSELs that must use sufficiently low aluminum (Al) content in the *p*-mirror to prevent oxidation in all but the desired oxide aperture layer. This additional cooling drops the thermal resistance of the new technology to less than half that of oxide VCSELs, and is responsible for the high power and stimulated emission rate. This improved thermal performance becomes very important in achieving high reliability at the higher current densities required for higher modulation speeds.

The Vertical Cavity Surface Emitting Laser (VCSEL) light-versus-current curve is the central test measurement in determining reliability. Because of their low internal operating temperature, VCSELs produce high power levels and high stimulated-emission rates. The reduction in junction temperature comes from reducing the device size and eliminating the oxide. For a given operating current density, the junction temperature reduces for a given current density as the VCSEL size is reduced. For 3-µm VCSEL's, the lithographic VCSEL has a factor of two lower temperature for a given operating current density, relative to the oxide VCSEL.

Compared to the oxide VCSELs, the High Heat Flow Cavity (HHFC) that results enables very high drive current density, and the maximum current density increases as the VCSEL size is reduced. The powers and drive levels of even the 4 µm VCSEL exceed the 7 µm oxide VCSELs. The 4 µm size can be driven to current densities of 95 kA/cm^2. Reliability testing becomes an important step in the research to verify operation under high-speed drive levels for harsh environments.

Studies have shown that, while both the commercial oxide VCSELs and the lithographic VCSELs show a decrease in power of a few percent within the first 20 hours of high temperature stress testing, the oxide VCSELs continues to fail, while the lithographic VCSELs show little change after the first 20 hours. Testing of a lithographic VCSEL that now has operated close to 300 hours shows no measurable change in characteristics. We estimate a mean-time-to-failure in excess of 10^6 hours based on a junction temperature at 85 °C and bias current density of 50 kA/cm^2, and using known acceleration factors for current and activation energy.

The lithographic VCSEL provides greater cooling to the active junction and so has greater intrinsic speed for a given operating temperature. The speed is expected to go up dramatically as the size is reduced. This is consistent with modeling for the frequency response that accounts for the temperature rise in the VCSEL. Essentially, the intrinsic response increases when the bias current density can be increased to increase the stimulated emission rate. Their maximum room temperature power conversion efficiencies are close to 50%. Intrinsic responses based on stimulated emission rates, internal temperatures, and cavity bandwidths are well beyond 50 GHz for sizes less than 5 µm diameter.

The current oxide VCSEL size is ~7 µm diameter. By reducing the device size while maintaining high efficiency, the intrinsic speed should increase significantly. The small signal bandwidth of the 3 µm lithographic VCSEL at 85 °C is estimated at 90 GHz, and we expect the device to be limited in bandwidth by electrical parasitics. However, the electrical parasitics can also be reduced with decreasing device size. We estimate that the electrical parasitic limited bandwidth for the 3 µm device can exceed 50 GHz, relative to 28 GHz that has been measured for the 7 µm oxide VCSEL.

Therefore, high-speed VCSEL sources operating at high temperature with high reliability are an expected outcome of this research. Electrical parasitics would also be analyzed. Reducing device size reduces electrical parasitics and increases bandwidth. Therefore, controllable size reduction that comes from the lithographic process both reduces the internal device operating temperature and reduces the electrical parasitics.

4.0 RESULTS AND DISCUSSION

4.1 Analysis of Electrical Parasitics and Continuous-Wave Measurements

Figure 1 shows a schematic illustration of the VCSEL cross section. The VCSEL uses a p-diffused channel to reduce electrical resistance into the laser. Table 1 shows estimated values for the contributions to the electrical parasitics based on the circuit model shown in the schematic of Figure 1. The pad electrode for making contact to a wire bond is not shown in Figure 1 but is included in Table 1. The estimated values in Table 1, and the circuit model of Figure 1, do not yet include all parasitic effects. There is additional diffusion capacitance due to the quantum well active region and cavity spacer. However an accurate model does not yet exist for these that can be included at this time. These are currently being studied and are expected to be reported elsewhere.

However given that it is found that the modulation speed can be quite high for this device. The motivation though is to use the oxide-free structure to enable very high reliability and overcome other issues with device scaling posed by the existing oxide VCSEL technology now relied heavily on by the Air Force on its military platforms. Bit energy and reliability are therefore key concerns and advantages of the oxide-free lithographic VCSELs.

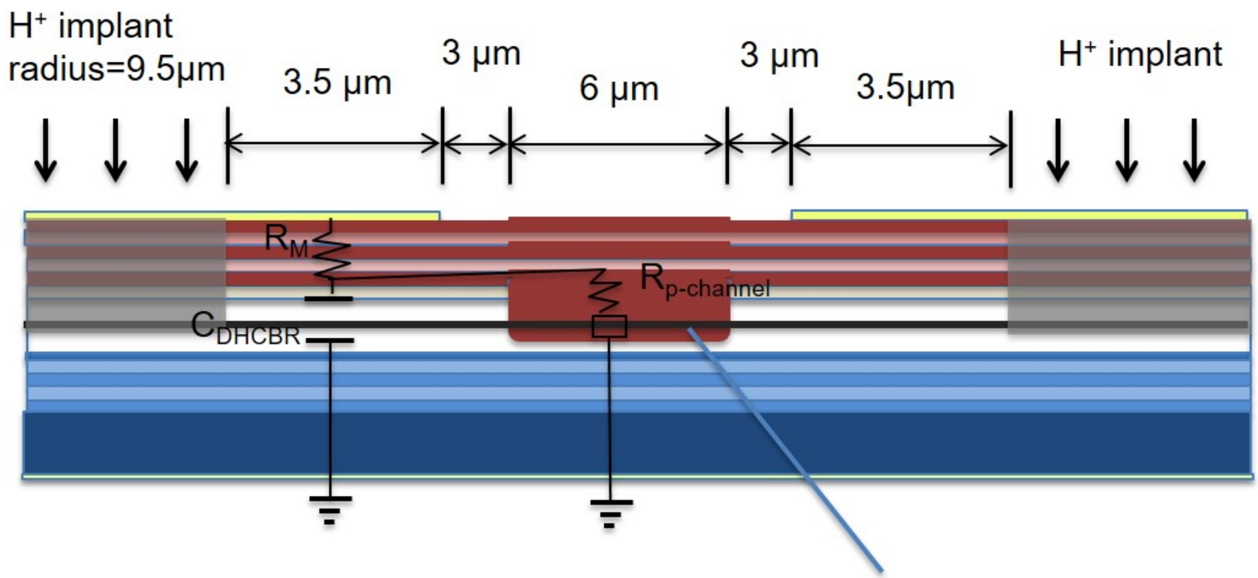

Figure 1. 6 µm Device Dimensions – p-diffused Channel

Table 1. Measured Electrical Parasitics Including Pad Capacitance for Prior Results

C_{pad}	C_{DHCBR}	R_{m}	$R_{p\text{-}channel}$	f_{3dB} (electrical)
33 fF	110 fF	51 Ω	20 Ω	68 GHz

Figure 2 shows modulation response of a 6 µm diameter VCSEL. Measured electrical parasitics including pad capacitance for circuit parameters of Figure 1 and Table 1. As long as the capacitance due to the quantum well active region remains consistent with oxide VCSELs the bandwidth is expected to be similar or greater. However we currently believe that with proper design the oxide-free VCSEL capacitance due to the active region can be even less than oxide VCSELs.

The measured results for a 6 µm VCSEL of this project are shown in Figure 3 and Table 2. One of the results found consistently is that the oxide-free VCSEL can achieve very low electrical resistance combined with high efficiency.

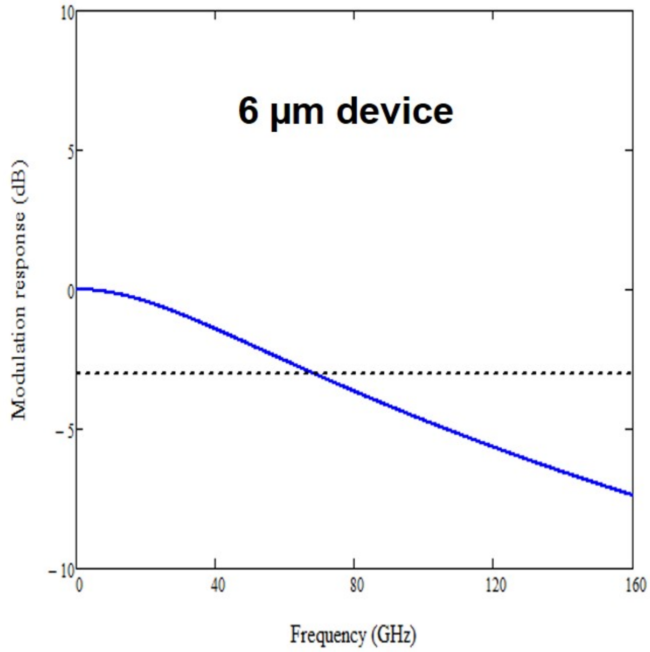

Figure 2. Modulation Response of the 6 µm Device

Figure 3 shows the results from a 6 µm diameter VCSEL. As it shown in Table 2 the differential resistance for this VCSEL is 60 Ω and the slope efficiency is over 60%. The maximum power is over 15 mW.

Table 2. Measured Parameters of 6 µm Device

	Ith (mA)	P_max(mW)	slope eff.	wall-plug eff.	Volt at 10kA/cm2
6µm	1.06	15.52	62.3%	35.7%	1.532

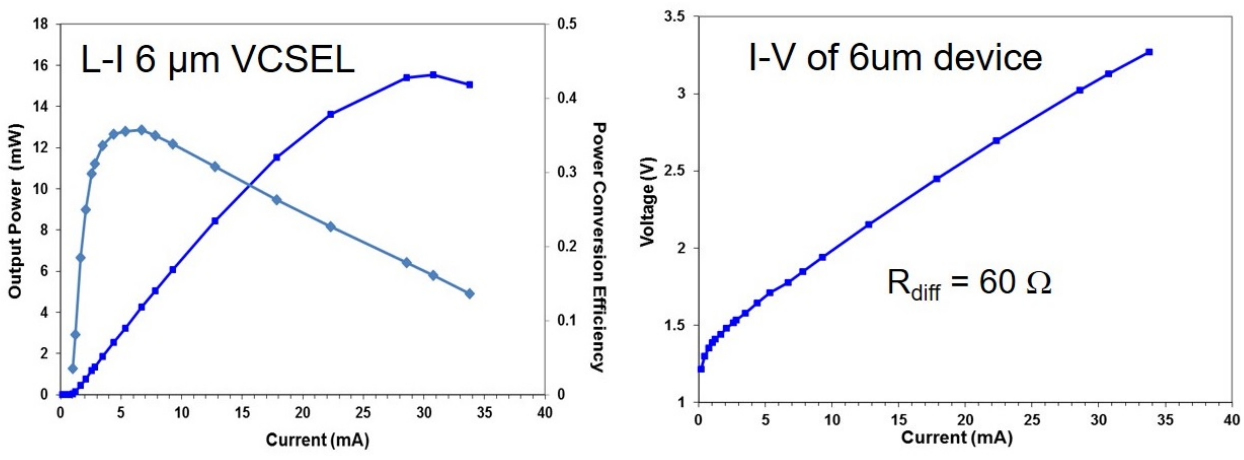

Figure 3. Power and Power Conversion Efficiency vs. Current of 6 µm Device

Different VCSEL sizes have also been studied. Figure 4 and Table 3 show the results from a 4 µm diameter VCSEL. The differential resistance for this VCSEL is 92 Ω and the slope efficiency is over 73%. The maximum power is over 12 mW.

Table 3. Measured Parameters of 4 µm Device

	Ith (mA)	P_max(mW)	slope eff.	wall-plug eff.	Volt at 10kA/cm2
4µm	0.58	12.31	73.8%	44.3%	1.453

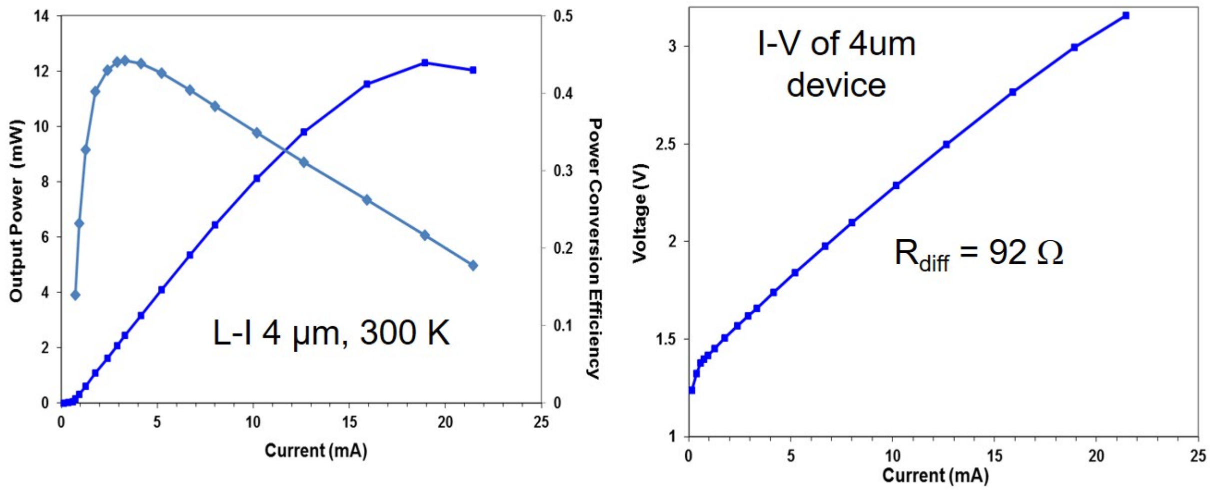

Figure 4. Power and Power Conversion Efficiency vs. Current of 4 µm Device

The results from a 4 µm diameter VCSEL are shown in Figure 5 and Table 4. The differential resistance for this VCSEL is 212 Ω and the slope efficiency is over 65%. The maximum power is 4.84 mW.

Table 4. Measured Parameters of 1 µm Device

	Ith (mA)	P_max(mW)	slope eff.	wall-plug eff.	Volt at 10kA/cm2
1µm	0.42	4.84	65.6%	32.9%	1.214

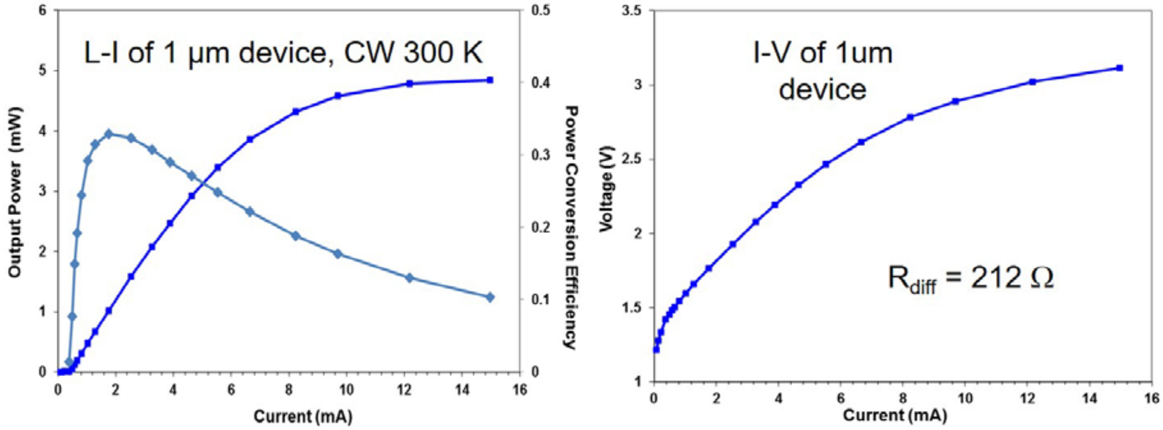

Figure 5. Power and Power Conversion Efficiency vs. Current of 1 µm Device

Small substrates were used to perform additional optimization on the internal parameters of the laser, especially the differential resistance. This optimization was quite successful and produced the lowest differential resistance to our knowledge yet reported for the various VCSEL size. Moreover, the results were obtained with lasers having high slope efficiency. The results were also obtained despite that at least the n-type mirror requires further optimization, and the p-type mirror likely also does. Figure 6 shows the results from a 6 µm diameter VCSEL. The differential resistance is only 42Ω, while the slope efficiency is over 60%. This may be record low differential resistance value**.** The maximum power is over 17 mW. This high power and high slope efficiency indicate that further reduction of differential resistance will be possible through increasing the doping of the p-mirror. Furthermore, we have optimized the n-mirror now for much lower resistance as well based on test structures.

Table 5. Measured Parameters of New 6 µm VCSEL with Reduced Mirror Resistance

	Ith (mA)	P_max(mW)	slope eff.	wall-plug eff.	Volt at 10kA/cm2
6µm	0.89	17.18	61.4%	38.9%	1.458

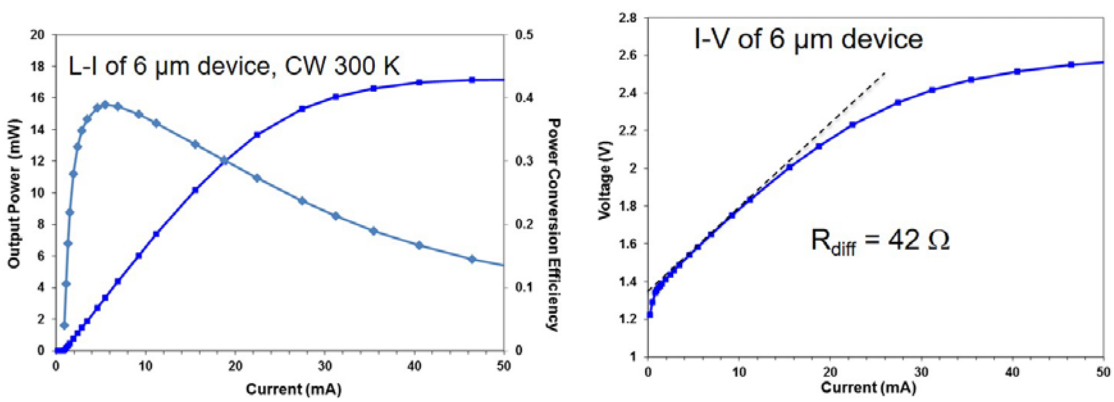

Figure 6. Power and Power Conversion Efficiency vs. Current of new 6 µm VCSEL with Reduced Mirror Resistance

Table 6 presents estimates of the VCSEL speed based on an available model of parasitics. However this only includes the electrical parasitics of the resistance and capacitance of the injected current reaching the quantum well active region of the laser. Additional effects are due to diffusion capacitance caused by the injection of electron-hole charge into the cavity spacer and are significant. These are currently being studied and are not included here.

Table 6. Parasitic Response Affected by Mirror Resistance

Mirror resistance (Ω)	f 3dB (GHz)
20	259
40	155
66.7 (from measured results)	100
80	85
100	69
150	47

4.2 Cryogenic (4 K) Performance Projections for Ultra-Small Cavity Oxide-Free QVCSELs

In the no-cost extension period we studied the potential of small-sized VCSELs to offer very low power consumption and high reliability for cryogenic data transfer. Projections are made for 4K operation based on oxide-free VCSEL sizes of 1-4 µm shown to operate efficiently at room temperature. There are growing applications for which efficient optical data transfer is made from cryogenic environments into room temperature. These include focal planes arrays and superconducting circuit that operate at 4 K [1]. Achieving high efficiency at the cryogenic temperatures is a key challenge, because of the need to reduce heating in the cryogenic environment [1]. The optical data transfer may be accomplished using a free space interconnect or through one or more optical fibers, and vertical-cavity surface-emitting lasers (VCSELs) could provide a very efficient, low cost and compact solution [2,3]. However oxide VCSELs suffer internal stress due to the oxide and have other known reliability problems and is known to cause early VCSEL failure, especially for cryogenic operation.

Oxide-free VCSELs have recently been introduced that can be scaled to micron size with record efficiency, and could provide the highest efficiency and reliable solution to optical data transfer. Laser diode simulation is now well established in its physics, and this can be applied to VCSELs to project their low temperature operation. Here we make projections of key VCSELs properties using an analysis based on the temperature dependent threshold and temperature dependent differential gain for 4 K operation. The model projects that 20 GHz small signal modulation can be achieved at 4 K at bias current at ≤ 5 μA. This extremely low bias current and the expected high efficiency at the cryogenic operation make the oxide-free VCSEL an important route for cryogenic optical interconnects.

We have previously demonstrated an experimental data on lithographic and oxide-free VCSELs as small as 1, 2, 3 and 4 μm in diameter at room temperature [4]. Figure 7 shows this experimental result at room temperature, showing measured L-I curves for the 1, 2, 3 and 4 μm diameter lithographic VCSEL under CW operation at room temperature.

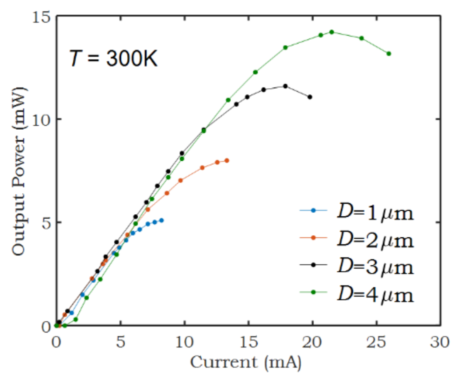

Figure 7. L-I Curves for the 1, 2, 3 and 4 μm Diameter Lithographic VCSELs Measured CW at Room Temperature

Below we can consider an oxide-free VCSEL designed with 35 n-type AlAs/GaAs quarter-wave bottom mirror pairs and one GaAs quantum well and completed with 14 p-type GaAs/AlAs quarter-wave top mirror pairs and GaAs as the substrate. This structure is designed to lase at 930 nm. Forming a set of two rate equations is the start point for modeling the intrinsic response of the semiconductor lasers. The photon numbers and the number of electrons in the active region at low temperature are obtained via solving the following two rate equations at steady-state. Equation 1 shows the rate equation for phonon numbers and Equation 2 shows the rate equation for electron numbers at low temperatures and both equations depend on temperature,

$$\frac{\mathrm{d}n}{\mathrm{d}t} = -\frac{\omega_\mathrm{c}}{Q}n + N_\mathrm{QW}\Gamma G_\mathrm{QW}\left\{\left[1 - \mathrm{e}^{-N_\mathrm{e}A(T)} - \mathrm{e}^{-N_\mathrm{e}B(T)}\right]n + \left[1 - \mathrm{e}^{-N_\mathrm{e}A(T)}\right]\left[1 - \mathrm{e}^{-N_\mathrm{e}B(T)}\right]\right\} \quad (1)$$

$$\frac{\mathrm{d}N_\mathrm{e}}{\mathrm{d}t} = \frac{I}{\mathrm{q}} - N_\mathrm{QW}\Gamma G_\mathrm{QW}\left[1 - \mathrm{e}^{-N_\mathrm{e}A(T)} - \mathrm{e}^{-N_\mathrm{e}B(T)}\right]n - \frac{N_\mathrm{e}}{\tau_\mathrm{sp}} \quad (2)$$

where $A(T) = \pi\hbar^2/(m_\mathrm{e}N_\mathrm{QW}A_\mathrm{L}\mathrm{k_B}T)$ and $B(T) = \pi\hbar^2/(m_\mathrm{h}N_\mathrm{QW}A_\mathrm{L}\mathrm{k_B}T)$. n is the photon number in the cavity, N_e is the number of electrons in the active region, ω_c is the lasing frequency in the cavity, Q is the quality factor. m_e and m_h are the effective masses of electrons and holes in the quantum wells. A_L is the area of the quantum wells, N_{QW} is the number of quantum wells in the active region, Γ is the confinement factor, T is junction temperature, k_B is the Boltzmann constant, I is the bias current, τ_{sp} is spontaneous emission life time and q is the charge of an electron. Finally by solving the above rate equations the L-I curve of the 1, 2, 3 and 4 µm diameter devices at temperature of $T = 4$ K is obtained and shown in Figure 8(a). According to this figure the threshold current decreases by decreasing the device size.

Equation 3 shows the expression for the intrinsic modulation response, derived from semiconductor rate equations,

$$H_{\mathrm{I}}(\omega) = \frac{\frac{\omega_C}{Q}(T)\Delta n(\omega,T)}{\frac{\Delta I(\omega)}{\mathrm{q}}} \approx \frac{\frac{\omega_C}{Q}(T)G_{\mathrm{diff}}(T)n_0(T)}{-\omega^2 - i\omega G_{\mathrm{diff}}(T)n_0(T) + \frac{\omega_C}{Q}(T)G_{\mathrm{diff}}(T)n_0(T)} \tag{3}$$

where G_{diff} is differential gain. It can be shown that G_{diff} is

$$G_{\mathrm{diff}} = \frac{dg_{\mathrm{st}}}{dN_{\mathrm{e}}} = \frac{\Gamma G_{\mathrm{QW}}\pi\hbar^2}{A_{\mathrm{L}}k_{\mathrm{B}}T}\left[\frac{\mathrm{e}^{-\frac{N_{\mathrm{e}}\pi\hbar^2}{m_{\mathrm{e}}N_{\mathrm{QW}}A_{\mathrm{L}}\mathrm{k_B}T}}}{m_{\mathrm{e}}} + \frac{\mathrm{e}^{-\frac{N_{\mathrm{e}}\pi\hbar^2}{m_{\mathrm{h}}N_{\mathrm{QW}}A_{\mathrm{L}}\mathrm{k_B}T}}}{m_{\mathrm{h}}}\right] \tag{4}$$

The simulation results are demonstrated in Figure 9. Figure 8b shows the intrinsic modulation response of the 1 µm diameter device lasing at 930 nm at temperature of $T = 4$ K for different bias currents.

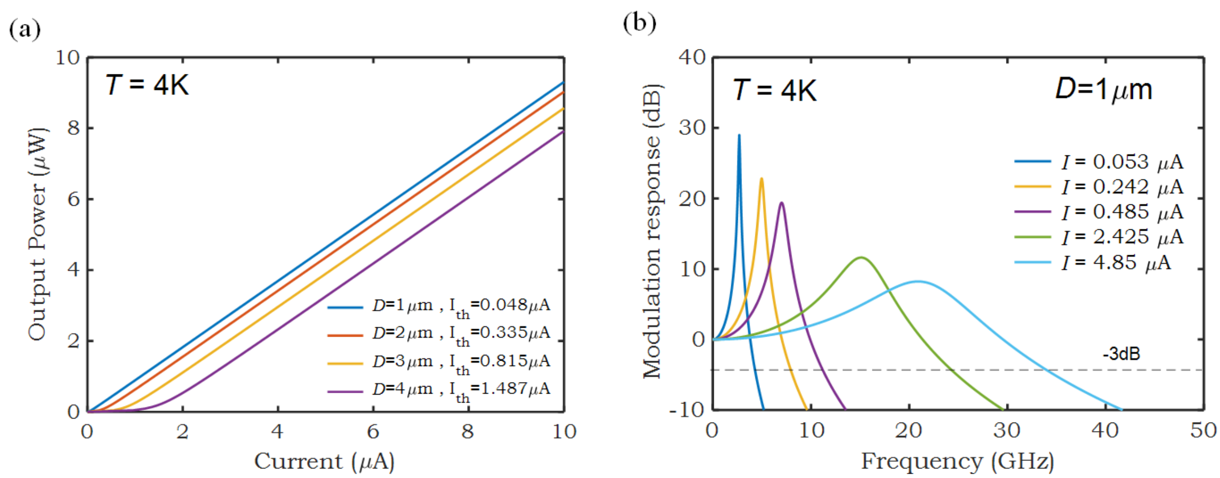

Figure 8. (a) L-I curves of the 1, 2, 3 and 4 µm Diameter Devices Lasing at 930 nm at Temperature of T = 4K. (b) Frequency Response of the 1 µm Diameter Device Lasing at 930 nm at Temperature of T = 4 K for Different Bias Currents

Figure 9 compares the requisite current to achieve the 20 GHz modulation speed for two different structures. First structure has 13 pairs p-type GaAs/AlAs quarter-wave top mirror and the second structure has 14 pairs p-type GaAs/AlAs quarter-wave top mirror. The diameters of both structures are 1 µm. According to the Figure 3 the device with 14 pairs needs less current to achieve 20 GHz modulation speed.

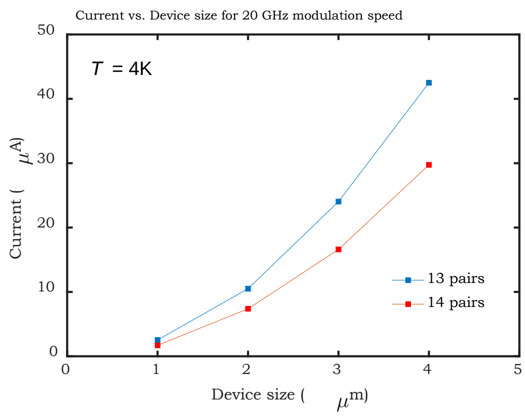

Figure 9. Current vs. Device Size for 20 GHz Modulation Speed for 1 μm Device

In conclusion we have shown an experimental data on lithographic oxide-free VCSELs as small as 1, 2, 3 and 4 **µm** in diameter at room temperature. Also we have made projections of key VCSELs properties using an analysis based on the temperature dependent threshold and differential gain for **4 K** operation.

5.0 CONCLUSIONS

In this project we have carried out initial studies on oxide-free VCSELs in growth and fabrication to develop the technology on 3” substrates for further development and foundry processing. Although the project was stopped after Year 1 was funding to departure of the AFRL program monitor who helped initiate the project, the work has continued through other funding sources. We are now working on 4” substrates that are compatible with fabrication foundries. We have also continued on the VCSEL development for additional applications that include 3-D sensing, atomic sensors, and high speed interconnects. The project with AFRL has been important in helping to launch these additional efforts. Especially useful could be the dense optical interconnects that can be used on Air Force platforms and in cryogenic high speed optical interconnects. The cryogenic interconnects can reach very low bit energy with the oxide-free VCSEL technology being developed here, and are attractive for applications in cryogenically cooled focal plane arrays and very low temperature computers based on superconductors.

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LIST OF SYMBOLS, ABBREVIATIONS, AND ACRONYMS

AFRL	Air Force Research Laboratory
CW	Continuous Wave
HHFC	High Heat Flow Cavity
RT	Room Temperature
UCF	University of Central Florida
VCSEL	Vertical Cavity Surface Emitting Laser

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