ARL-TR-8536 ● SEP 2018

US Army Research Laboratory

Broadband Model of a Stacked Power Switching Module for Parasitic Inductance Extraction

by Steven Kaplan

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REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

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1. REPORT DATE *(DD-MM-YYYY)*	2. REPORT TYPE	3. DATES COVERED (From - To)
September 2018	Technical Report	

4. TITLE AND SUBTITLE
Broadband Model of a Stacked Power Switching Module for Parasitic Inductance Extraction

5a. CONTRACT NUMBER

5b. GRANT NUMBER

5c. PROGRAM ELEMENT NUMBER

6. AUTHOR(S)
Steven Kaplan

5d. PROJECT NUMBER

5e. TASK NUMBER

5f. WORK UNIT NUMBER

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
US Army Research Laboratory
ATTN: RDRL-SED-P
Aberdeen Proving Ground, MD 21005-5066

8. PERFORMING ORGANIZATION REPORT NUMBER
ARL-TR-8536

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)

10. SPONSOR/MONITOR'S ACRONYM(S)

11. SPONSOR/MONITOR'S REPORT NUMBER(S)

12. DISTRIBUTION/AVAILABILITY STATEMENT
Approved for public release; distribution is unlimited.

13. SUPPLEMENTARY NOTES

14. ABSTRACT
Parasitic inductance due to the sizeable lead lengths and component spacing typical in planar packaging can cause significantly impaired switching characteristics. This is of particular concern in metal-oxide-semiconductor field-effect transistor half-bridge modules, due to the effects of signal overshoot that are endemic in high-speed switching applications. Multi-functional components (MFCs) used as concurrent electrical, thermal, and mechanical module elements, and implemented in a stacked module design, can reduce parasitic degradation of power switching modules over a broad range of frequencies and applications. Devices stacked between copper layers with an integrated heat sink have been modeled from 1 kHz to 100 MHz to evaluate the efficacy of this design approach. This report derives the broadband parasitic inductance of the stacked module design, using magnetic field simulations that account for wide variations in skin depth through boundary layer meshing and compares the results to a commercially available, state-of-the-art half-bridge module.

15. SUBJECT TERMS
parasitic inductance, multi-functional components, power switching, half-bridge, stacked elements, overshoot

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
a. REPORT	b. ABSTRACT	c. THIS PAGE			Steven Kaplan
Unclassified	Unclassified	Unclassified	UU	18	19b. TELEPHONE NUMBER (Include area code) 301-394-3013

Standard Form 298 (Rev. 8/98)
Prescribed by ANSI Std. Z39.18

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1. Introduction

Minimization of parasitic inductance is essential to achieving good switching performance. Power electronics circuits used in fast switching applications are particularly sensitive to parasitics, due to potential catastrophic signal overshoot, so design of these power switching devices must account for and reduce the effects of such parasitics. Wide bandgap semiconductor silicon carbide (SiC) devices are typically used to achieve high switching speeds and allow for high-temperature operation.[1] However, the advantages offered by these high-performance circuit devices can be drastically compromised by poor device packaging. Large oscillation ringing and overshoot in fast switching waveforms result from parasitic inductances in the device package and its external circuit.[2] Switching voltages in power electronics applications are typically de-rated by 50% to safely accommodate anticipated over-voltage resulting from characteristics of device fabrication and packaging. Since overshoot voltage is directly proportional to parasitic inductance, package optimization to reduce design features such as lead lengths and device spacing is desirable to mitigate the required de-rating of switching voltage as a function of switching current and speed.

2. Stacked Module Design

A typical power module layout is shown in Fig. 1 with a cross-sectional view of its various components. Note that this design employs single function components spread out over the entire package region to address the electrical, thermal, and mechanical requirements of the module. The power module being modeled in this work consists of a half-bridge configuration with stacked die and integrated cooling. The stacked elements of the module simultaneously provide thermal and electrical contact. These multi-functional components (MFCs) comprise the constituent sections that make up the power module. The module is shown in Fig. 2 next to a half-bridge circuit schematic. The half-bridge design is of particular interest because it is the foundation of many power circuits (inverters and converters). The power module, as described, is both modular and scalable to accommodate any number of configurations of diodes and switching devices. The specific half-bridge module examined here consists of two diodes and two switches, typically either insulated-gate bipolar transistors or metal-oxide-semiconductor field-effect transistors (MOSFETs). The stacked arrangement of the MFCs reduces the lengths and number of constrictive electrical paths, especially wire-bonds. The switches are packaged in series rather than the more typical anti-parallel configuration to further reduce inductance.[3]

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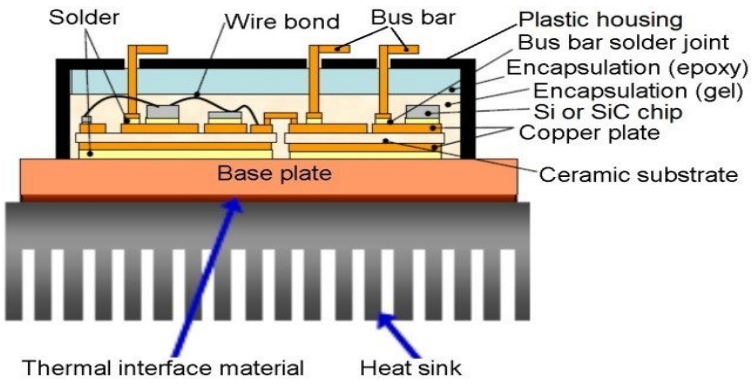

Fig. 1 Standard power module configuration[4]

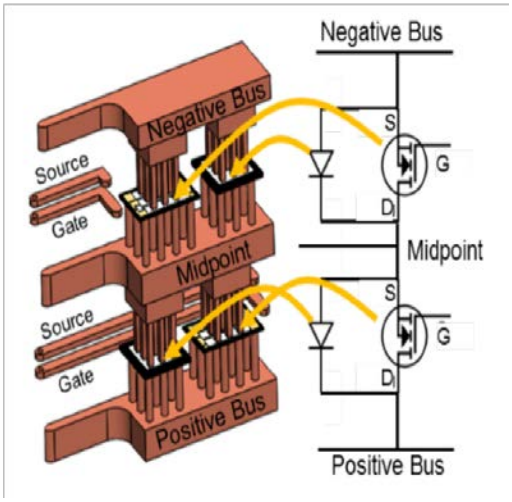

Fig. 2 Half-bridge circuit schematic indicating the location of the two switches and two diodes in the assembly

The electrically conductive layers for the power module are fabricated from copper, while all the devices are primarily SiC. The base layer acts as the positive bus in the circuit. It connects the drain of the switching device to the cathode of the associated diode. The middle layer consists of a conductor that acts as the midpoint on the circuit schematic. It electrically connects the source of the lower switching device and the anode of the lower diode to the cathode of the upper diode and the drain of the upper switching device. The top layer shown in Fig. 2 acts as the negative bus in the half-bridge module connecting the source of the upper switching device to the anode of the diode.

3. Magnetic Field Simulation Model

A robust model has been developed that accounts for the widely varying skin depth of electrical currents for each frequency component in the spectrum composing a fast pulse waveform. This is accomplished through the implementation of fine boundary layer meshing within the model geometry using COMSOL Multiphysics Simulation Software. The model is used to extract the parasitic inductance of the stacked power module over a broad frequency range, and compare it to commercially available, low-inductance planar modules. The inductance extraction required a magnetic fields simulation that was conducted within the AC/DC module of COMSOL. The simulation was performed for two cases: the first at low frequencies (1–1000 kHz) representative of the possible switching frequencies, and the second at higher frequencies (1–100 MHz), representing the higher-order time-domain waveform components that occur at the fast switching speeds anticipated for this module (switching signal rise-times on the order of a nanosecond). This broadband endeavor required implementation of a "coil geometry" approach in COMSOL, wherein finite skin depths, from a few microns up to several millimeters, are properly accounted for.

The COMSOL model geometry for the stacked power module was imported from a computer-aided design (CAD) file rendered in SOLIDWORKS, shown in Fig. 3. The purple regions represent the copper components that form the bulk of the module. The SiC MOSFETS and diodes are rendered as clear with black framing of their boundary regions. The four aluminum wire-bond connections from the source and gate lines are rendered as straight black segments. The acrylic module case, including cooling fluid ports, is outlined in gray. The module components are immersed in NOVEC 7500 engineering fluid, which resides within the outer case. The various properties of this fluid, such as dielectric permittivity and resistivity, remain manually defined in the COMSOL model. However, to adapt the COMSOL half-bridge model to frequencies below 1 MHz, certain modifications were required. It was necessary to add some artificial, though reasonable, conductivity to each of the model elements for numerical convergence during the computational phase. Refinements to the model geometry components were also implemented to allow for the finer boundary meshing needed to capture the increased skin depth of the electrical current at the lower frequencies.

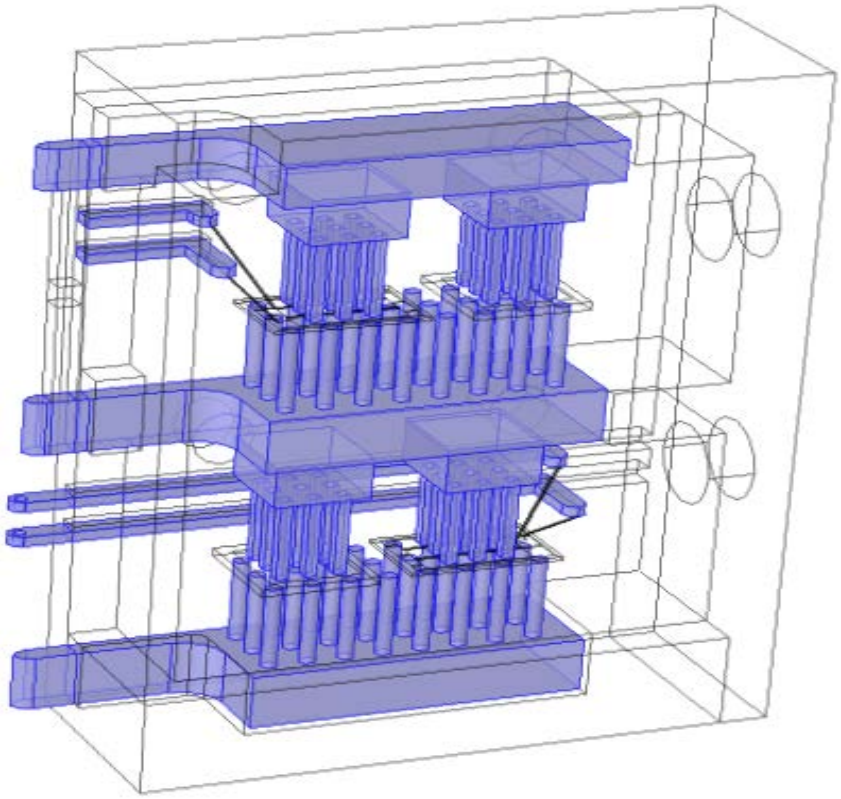

Fig. 3 Half-bridge simulation model schematic

The electrical circuit diagram corresponding to the model of the half-bridge power module is shown in Fig. 4. The magnetic field simulation analysis in the model is performed on the section of Fig. 4 enclosed in red. The negative bus represented in the model simulation corresponds to D_1 in the electrical diagram, while the midpoint corresponds to S_1D_2, and the positive bus to S_2. Note that the schematic in Fig. 4 is inverted with respect to the representation in Fig. 3.

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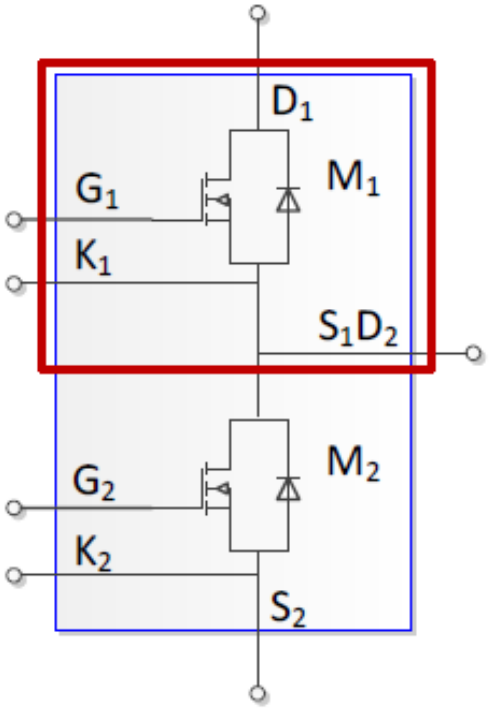

Fig. 4 Modeled half-bridge circuit, with section containing excitation port (D_1–S_1D_2) enclosed in red

4. Modeling Results

The impedances derived from the model at the port between the midpoint and negative bus-bar are tabulated in Table 1, along with the extracted parasitic inductances. The inductances show a gradual decrease with increasing frequency in the range from 1 kHz to 1 MHz. A plot of the low-frequency data from Table 1, which clearly displays this negative frequency dependence, is shown in Fig. 5. At frequencies above 1 MHz, the inductance continues to drop, approaching 5 nH at 100 MHz within the very-high-frequency (VHF) portion of the electromagnetic spectrum. The high-frequency simulation results listing the extracted parasitic inductances are detailed in Table 2.

Table 1 Impedance of power module for each frequency in model analysis

Frequency (kHz)	Impedance (Ω)	Extracted parasitic inductance (nH)
1	2.903 + 8.17e-5i	14.22
10	2.903 + 8.88e-4i	14.14
25	2.903 + 0.00232i	14.11
50	2.903 + 0.00452i	14.00
75	2.903 + 0.00668i	13.88
100	2.903 + 0.00873i	13.77
200	2.903 + 0.0170i	13.55
300	2.903 + 0.0251i	13.35
400	2.903 + 0.0332i	13.10
500	2.906 + 0.0411i	12.90
600	2.906 + 0.0490i	12.82
700	2.906 + 0.0569i	12.75
800	2.907 + 0.0647i	12.70
900	2.907 + 0.0726i	12.64
1000	2.908 + 0.0803	12.58

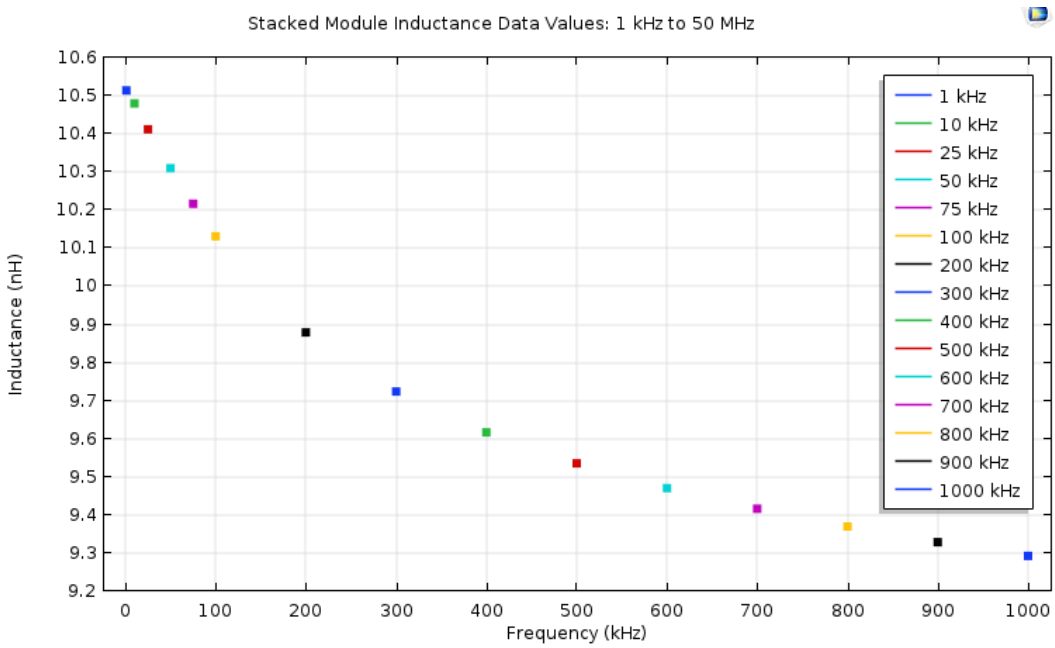

Fig. 5 Parasitic inductance values extracted from low-frequency simulation

Table 2 High-frequency impedance of power module at lumped port

Frequency (kHz)	Impedance (Ω)	Inductance (nH)
1	2.9086 + 0.079034i	12.579
10	3.0495 + 0.69469i	11.056
25	3.4244 + 1.4039i	8.9378
50	3.8443 + 2.1731i	6.9173
75	4.0652 + 2.8644i	6.0784
100	4.2100 + 3.5600i	5.6659

Figure 6 is a plot of the parasitic inductances given in Table 2, and clearly illustrates the declining inductance with increasing frequency. As the frequency rises above 100 MHz, there will be a transition of the module's reactance from positive (inductive) to negative (capacitive) (i.e., parasitic capacitance begins to dominate above 100 MHz).[5] It should be noted that the simulated parasitic inductance at lower frequencies may be overstated due to poor meshing at the conductor boundary layer subdomains. These meshing issues are being addressed by adding refinements to the conducting surface layers. Further refinements in the boundary meshing of these subdomains will be pursued in future models based on refinements in the device CAD representation and implemented as part of continuing device package optimization. In addition, comparison of simulation results to empirical data will be included as such data become available.

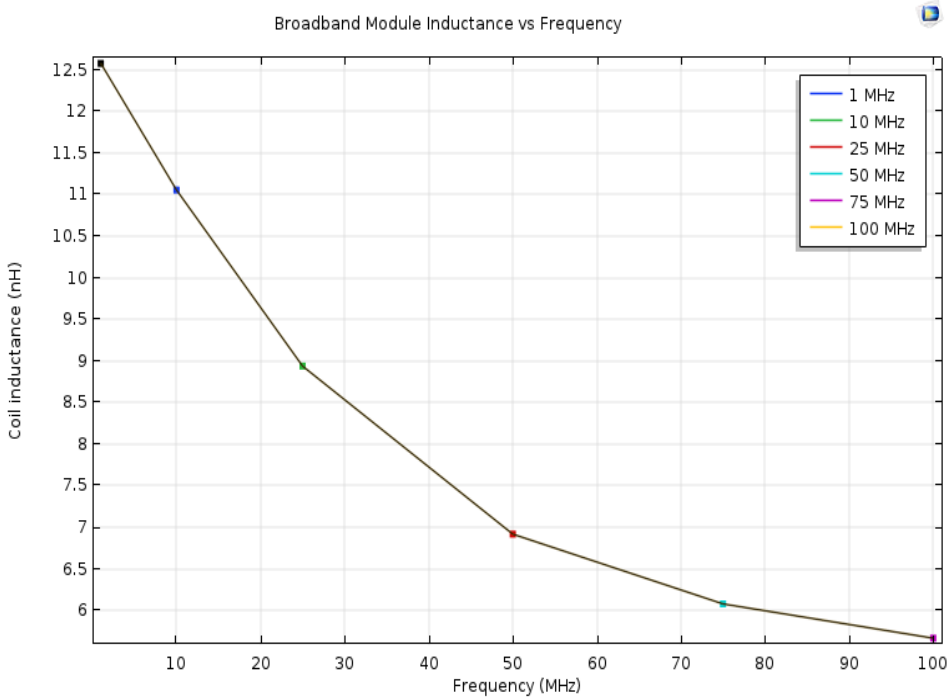

Fig. 6 Broadband plot of parasitic inductance up to VHF range

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5. Comparison to Commercial Device Modules

The modeling results listed in Tables 1 and 2 indicate that the stacked half-bridge power module design has significantly lower parasitic inductances than those of traditional planar configurations, which are typically an order of magnitude higher (50 nH or more).[6] There are state-of-the-art planar module devices, such as the one shown in Fig. 7, that advertise lower parasitic inductance. The power module in the figure is manufactured by CREE, Inc., and specifies a parasitic inductance of 15 nH, although frequency dependence and measurement details are not reported in this specification. The stacked module design simulation results in parasitic inductance values from 5.6 to 14.2 nH from 1 kHz to 100 MHz. This, then, indicates lower overall parasitics at all switching frequencies and speeds, over a broad range of applications and frequencies.

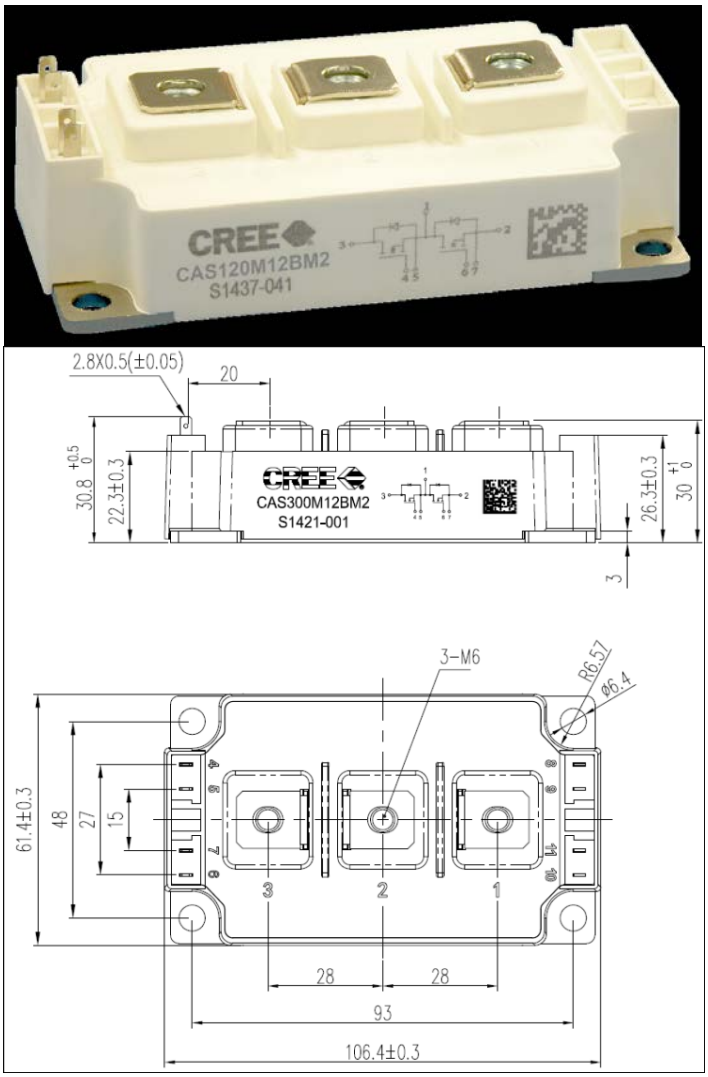

Fig. 7 Commercial half-bridge power switching module

6. Conclusions and Future Work

Broadband modeling of the impedance characteristics for a stacked half-bridge power module was performed to study the parasitic inductance produced by this design and compare it to the inductances of commercially available switching modules using traditional planar packaging. The stacked design makes use of compact MFCs in an attempt to optimize cooling, reliability, and reduction of parasitics. Magnetic field simulations using a "coil geometry" to capture skin depths from microns at 100 MHz, to millimeters in the kilohertz range, reveal that the parasitic inductance of this design is significantly lower than is generally found in standard planar module configurations. The inductance values predicted by the model ranged from about 5 to 14 nH, which is well below the usual parasitic inductance typically seen by power modules of the planar type. The modeled values are also equal to or lower than state-of-the-art planar switching modules, such as the commercial device described in this report. This reduction in inductance is due to use of compact multi-functional electrical components, as well as minimization of package interconnections and wire-bond lengths. Enhanced modeling with boundary layer meshing for improved skin-effect resolution will be performed in the future, as part of the co-engineering/co-design effort at the US Army Research Laboratory, and will incorporate empirical data comparisons as such data become available.

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List of Symbols, Abbreviations, and Acronyms

AC/DC	alternating current/direct current
CAD	computer-aided design
MFC	multi-functional component
MOSFET	metal-oxide-semiconductor field-effect transistor
SiC	silicon carbide
VHF	very-high-frequency

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