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STUDY OF SUPER DIELECTRIC MATERIAL FOR NOVEL PARADIGM CAPACITORS

by

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March 2018

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STUDY OF SUPER DIELECTRIC MATERIAL FOR NOVEL PARADIGM CAPACITORS

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TABLE OF CONTENTS

LIST OF FIGURES

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LIST OF TABLES

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LIST OF ACRONYMS AND ABBREVIATIONS

A	electrode area
a	electrode and dielectric layer contact area
ASB(I)	Afloat Staging Base (Interim)
ASBM	anti-ship ballistic missile
ASCM	anti-ship cruise missile
C	capacitance
CHDL	charge, hold, discharge, loop
CHD	charge, hold, discharge
[cm^3]	centimeter cubed
DDG	destroyer
DEW	directed-energy weapon
ds	infinitesimal displacement
dt	infinitesimal time
DT	discharge time
dV	infinitesimal voltage
E	electric field
E_{tot}	total energy
EC Lab	Electrochemistry Lab
EDLC	electric double layer capacitor
EM Railgun	electromagnetic Railgun
ε	dielectric constant
ε_0	constant relativity of free space
[F]	farad
F-SDM	fabric based Super Dielectric Material
FEL	free-electron laser
FY	Fiscal Year
[g]	gram
GTA	high purity grade (minimum 99.5% graphite)
HEL	high-energy laser

HELIOS	High Energy Laser and Integrated Optical-dazzler
I	current
[J]	joule
[kg]	kilogram
KOH	potassium hydroxide
[KW]	kilowatt
LLC	limited liability corporation
m	mass
[m]	meter
[m^2]	meter squared
[mA]	milliamp
MATLAB	Matrix Laboratory (software)
[MJ]	megajoule
[MW]	megawatt
LaWS	Laser Weapons System
NAVSEA	Naval Sea Systems Command
NPS	Novel Paradigm Supercapacitor
P_{tot}	power
P-SDM	power based Super Dielectric Material
PL-SDM	punched layer Super Dielectric Material
POA	punched-out area
q	charge
ρ	density
RFP	request for proposal
[s]	second
SDM	Super Dielectric Material
SSL	solid-state laser
t	thickness (dielectric)
T-SDM	tube based Super Dielectric Material
UAV	unmanned aerial vehicle
[W]	watt

V	voltage difference or potential
[V]	volts
v	volume

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To Danny and Luke: thank you.

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I. INTRODUCTION

The United States Navy is committed to the deployment of electric-powered directed-energy weapons (DEWs); however, limitations of current electric power storage are a major obstacle to near-term service of operational systems onboard power-limited naval vessels. Performance limitations of current generation energy storage devices cloud any apparent solution for sustained engagements requiring numerous and rapid cyclability (discharges and charges) over a lengthy duration. In essence, electrochemical storage devices (batteries and capacitors), as they are now, offer a unique but limited solution, and require improvement prior to serious consideration for implementation of commercial systems into energy magazines. Power delivery required to enable DEWs can only be met by capacitors as they are inherently more power dense than batteries. Yet the best current generation capacitors, electric double layer capacitors (EDLC), also known as supercapacitors require a physical footprint too large to accommodate onboard most naval vessels.

In this study, we examined the performance of a new variety of Novel Paradigm Supercapacitors (NPS) in detail. This new variety of NPS, PL (punched layer) Super Dielectric Material (SDM), was tested to determine i) the applicability of SDM theory to PL-SDM, and ii) if this particular type of SDM-based NPS is suitable for practical use by the US Navy. In support of the first objective, this study represents a continued effort of prior work investigating fabric based SDM [1], powder based SDM [2-5], and tube based SDM [6-10]. As with various areas of scientific study for which there exist no direct methods of measurement, such as dark matter and dark energy, the same inductive logic approach has been taken for the present study. In this case, we first applied SDM theory to identify composite materials as potential SDM, then tested each for super dielectric properties. With each material successfully exhibiting SDM behavior, the tests have reinforced the predictive character and, by logical inference, the validity of the theory.

The theory predicts any composite material that is capable of forming large dipoles via the migration of free ions in confined solution is a viable candidate for SDM. Furthermore, SDM employed in a parallel plate capacitor will create dipole fields opposite

in polarization to the dipole fields created by charges on the electrodes thereupon lowering the net field at every point in space relative to that present in the absence of the SDM. In turn, this will lower the voltage on the electrodes for any given charge density. Hence, the number of charges required on the plates to reach a voltage is substantially increased in parallel plate capacitors employing SDM. By definition, this is an increase in capacitance.

SDM stands apart from traditional dielectrics due to its unique structure and composition. Similar to SDM, ceramic dielectrics also form dipoles in opposite polarization to that of the charges on the electrodes, and this too reduces the field at all points in space. However, the dipoles created by tiny displacements of atoms within a crystal structure (ceramic) are far less than an angstrom in length. In an SDM, dipoles are created by the separation of free ions in solution resulting in dipoles of microns or even more in length. Overall, the difference in dipole length between that found in traditional dielectric crystals and that found in confined dissolved salt solutions is predicted to make the latter a far better dielectric.

In this study, potassium hydroxide (KOH) solution confined to the punched membrane in PL-SDM was predicted to be an SDM. Moreover, SDM theory predicted that where the full voltage was felt by ions in the "punched open area" (defined below) was where significant ion migration would take place. Thus, the theory predicted SDM-based capacitor performance would improve as more and more of the dielectric was open, or punched-out in the membrane. In fact, the results were agreement with the proposed model: dielectric values, energy and power density were in the class of SDM, and increased as the punched area increased. In sum, it was shown that SDM theory is applicable to PL-SDM capacitor optimization.

A. MOTIVATION

DEWs provide a "game-changing" solution to the issue of current and emerging surface, air, and missile threats. Unlike conventional weapons, they are capable of delivering a graduated response via an increase in non-kinetic energy, and offer several state-of-the-art advantages: rapid engagement, low cost per engagement, infinite depth of magazine, and low total-ownership cost [11,12]. At present, DEWs are capable against

low-end threats such as small boats and unmanned aerial vehicles (UAVs) within a range of one to two nautical miles [12-14]. The Navy envisions the technology progressing towards a surface ship missile defense system capable of defeating supersonic anti-ship cruise missiles (ASCMs) and select anti-ship ballistic missiles (ASBMs) within a range of 10 nautical miles [11,12]. DEW advancements designed to enhance warfighter survivability and close capability gaps include the following.

1. Electromagnetic (EM) Railgun

In 2012 the Navy evaluated two industry-built Electromagnetic (EM) Railgun prototypes, weapons that use electricity to generate an electromagnetic force to launch kinetic projectiles at speeds up to Mach 7.4 [12,15-18]. The current initiative is to achieve a firing rate of 10 rounds per minute at 32 [MJ] muzzle energy by fiscal year (FY) 2019 followed by even faster rates-of-fire through the use of a pulsed power capacitors with energy densities over 1 [MW/m^3] [12].

2. Laser Weapons System (LaWS)

In 2014 the United States Navy demonstrated and declared operational the first solid-state laser (SSL) weapon prototype, a 30 [kW] fiber SSL called Laser Weapons System (LaWS), onboard the USS *Ponce Afloat Forward Staging Base*, Interim (ASB(I) 15) where it successfully engaged a number of low-end surface and air test targets in an operational environment [11-13].

3. High-Energy Laser (HEL)

In June 2017 Naval Sea Systems Command (NAVSEA) issued a Request for Proposal (RFP) to procure two 60–150 [kW] High Energy Lasers (HEL) by FY 2020 in support of its High Energy Laser with Integrated Optical-dazzler and Surveillance (HELIOS) project [19-21].

4. Free-Electron Laser (FEL)

Currently, the free-electron laser (FEL) is a developmental weapon in which technology borrowed from particle colliders (used by the Department of Energy) is being

used to generate high-intensity laser light from unbound accelerated high-energy electrons for the purpose of surface-ship defense [11,22]. The goal of the program is to demonstrate scalability of the technology in order to develop a megawatt-class laser weapon with the ability to adjust laser intensity to defeat low to high-end threats, accordingly [22].

B. TECHNICAL BACKGROUND

DEWs will require hundreds of kilowatts (kW) to a megawatt (MW) of power (per shot), and possibly more when considering less than perfect efficiency levels, to achieve the desired weapons' ranges necessary for battle group operations and defense against supersonic missile threats [11,12]. One ship class, the Zumwalt class destroyer (DDG 1000), an all-electric ship capable of generating 58 [MW] of reserve power, may have the means to support shipboard operation of a DEW [23,24]. However, DEWs back fitted onto older ships, like the Arleigh Burke class destroyer (DDG 51) can only provide 150 [kW] of reserve power, and will likely require an energy magazine comprised of energy storage devices to augment the ship's existing electrical system [25]. In order to fulfill this requirement, optimal energy storage devices will need to deliver incredible amounts of power in compact sizes. Achieving a small energy footprint is not only necessary for ship integration due to space and weight restrictions, but desirable due to increased flexibility and modularity.

1. Energy and Power Density

The Ragone plot in Figure 1 shows regions of energy and power dense electrochemical storage devices. Energy dense devices such as lithium ion batteries release energy over a long period of time, whereas power dense devices such as electrolytic capacitors release energy over a short period of time. The difference between these devices is determined by each device's underlying chemical to electric conversion mechanism; reduction and oxidation reactions in batteries, and electron storage and near instantaneous release in capacitors. Although the energy and power relationship of each storage device is fixed in the transport and interaction of ions and electrons, the goal of research is to fulfill the need for optimized energy storage by means of novel materials engineering and design.

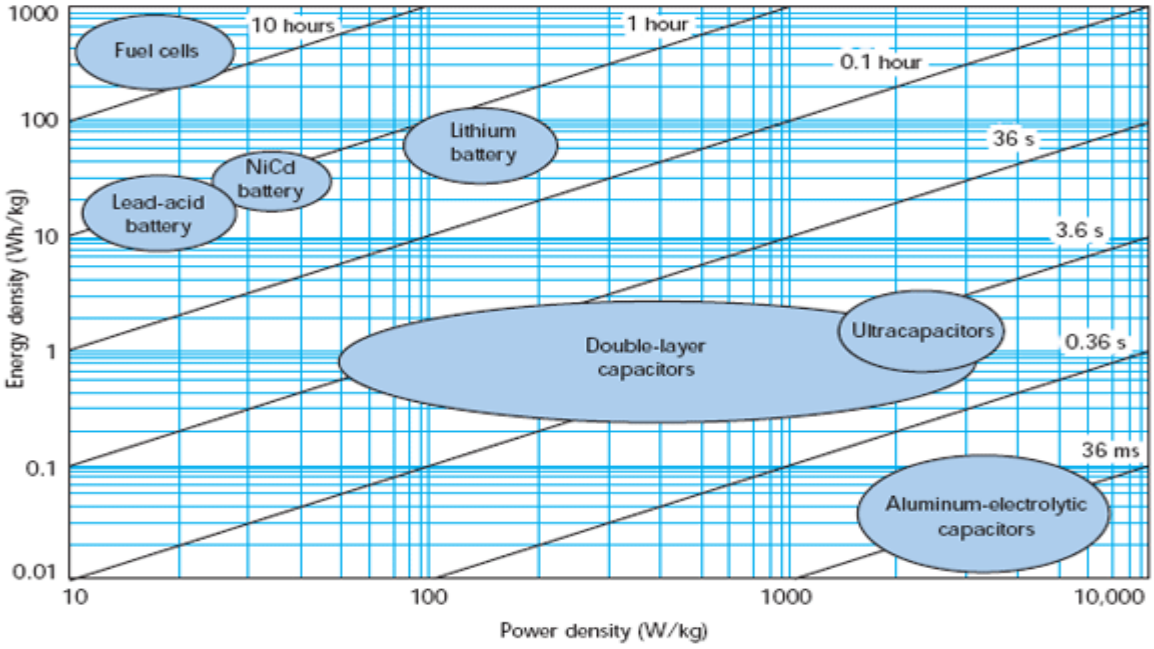


Figure 1. Ragone Chart of Electrochemical Storage Devices. Source: [26].

2. Parallel Plate Capacitor Model

To start, the most basic of capacitors shown in Figure 2 is constructed of two conductive electrodes with some surface area, A, separated by a dielectric material (also an electrical insulator) of some thickness and connected to a voltage source that when energized charges the electrodes and creates an electric field, E. An electric field is created as a result of the storage of equal and opposite charges on the electrodes. The strength of the electric field is determined by the number of electrons and the separation distance, d, between electrodes. Based on this model, an increase in capacitance, the ability to store charge, can be achieved in a prescribed number of ways.

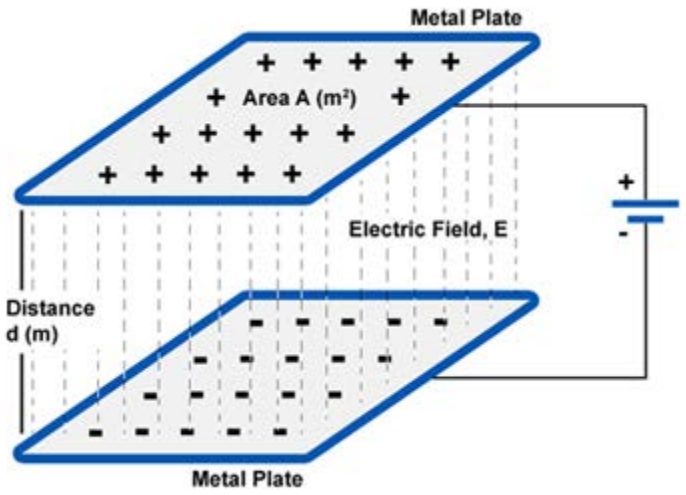


Figure 2. Parallel Plate Capacitor Model. Source: [27].

3. Current State of Technology and Strategies for Improvement

A comprehensive list of the types and varieties of capacitors available today would be too detailed and quite extensive, if only an adequate picture of the current state-of-technology is desired. In capacitor design there are a few variables in which optimization will result in increased capacitor performance [28]. Therefore, capacitors will be categorized and described by the variable (shown in the parallel plate capacitor equation) by which optimization is intended, and the strategy that is used to achieve it.

$$C = \frac{\varepsilon \varepsilon_0 A}{t} \tag{1}$$

a. Strategy I

This approach focuses on enlarging the electrode area, A, in order to increase energy storage. An extension of this logic may be to create extraordinarily large electrodes to store a vast number of electrons, but fortunately other solutions exist to address the challenge of optimization. Supercapacitors employ this method, and contain high surface area electrodes composed of high surface area electrically conductive carbons such as graphene, carbon nanotubes, carbon aerogel, and activated carbon to maximize capacitance, and minimize weight and volume.

b. Strategy II

This approach focuses on decreasing the separation distance between electrodes by shrinking the dielectric layer, t. The effect of decreasing electrode separation distance can be plainly put forward by evaluating the parallel plate equation and, also, not so evidently from the parallel plate capacitor model. First, capacitance and thickness of the dielectric layer share a relationship in which one variable will increase or decrease inversely (and proportionally) to a decrease or increase in the other variable. Second, previous discussion of the electric field between electrodes mentioned the dependence of field strength on separation distance, but saved a valid remark for inclusion here—a reduction in separation distance reduces field strength, as a result of increasing charge cancellation between electrodes of approaching proximity, and lessens the amount of energy needed to progressively add electrons to achieve charge saturation. Thus, using a thin layer of dielectric material can improve capacitance.

c. Strategy III

This approach focuses on improving the dielectric material, ε, used in capacitors. Virtually all efforts of this nature are centered on fine-tuning variations of barium titanate, a ceramic dielectric that exhibits the highest known dielectric value of any material. To quantify the difference of scale between dielectric materials used in capacitors, a comparison of dielectric values by decreasing order of magnitude follows: barium titanate and its derivatives are on the order of 1000, metal oxides such as titanium and aluminum oxides are on the order of 100, and ceramics, polymers, and glass are on the order of 1. Electrostatic capacitors employ dielectric materials of high dielectric value in conjunction with strategy II to increase capacitance.

4. Super Dielectric Material (SDM)

A dielectric material of exceedingly large dielectric value was created and studied at Naval Postgraduate School. Dielectric values were reported in the range of 10^5 to 10^{10}, orders of magnitude greater than any conventional dielectric materials [1-10]. This new class of dielectric material, Super Dielectric Material (SDM), was successfully employed in a group of capacitors collectively known as NPS. There are several types of SDM,

similar in that each contains a fluid solution containing dissolved salt, the fluid permitting rapid ion transport to create dipoles, but distinct in terms of the inert solid matrix employed to contain the solution phase. In particular, powder based SDM (P-SDM) in which the solution is physically mixed with a refractory oxide powder to create a material with a mud-like consistency, tube based SDM (T-SDM) in which the hollow titania tubes formed on the surface of titanium metal via anodization are filled with fluid, and fabric based SDM (F-SDM) in which ordinary fabrics are saturated with solution, and in the present study, PL-SDM (punched membrane) in which punched membrane is filled with salt solutions.

5. Super Dielectric Material (SDM) Theory

A review of capacitor theory is necessary in understanding the function of SDM. Parallel electrodes of equal and opposite charge create an electric field in all of space. An electric field, represented by normalized force vectors, exerts a non-uniform electrostatic force of some magnitude and direction at every point. Knowing the force (per unit charge) and particle path through a field provides a means of calculating the electric potential between two points in a field. The line integral, shown in equation 2, expresses electrical potential or voltage difference, V, as a summation of the products of field strength, E, and infinitesimally small changes in displacement, ds, between points and A and B. In a conservative electric field, electrical potential can be understood as a scalar quantity associated with the work or energy to move a particle between two points in a field.

$$V = V_B - V_A = -\int_A^B E ds \tag{2}$$

As charge accumulates on each electrode, the field strength increases everywhere leading to an increase in the work required to move charges onto the electrodes. Therefore, finding a way to reduce the voltage difference, V, while maintaining a high state of charge, q, on the electrodes will improve capacitance, C, as expressed in equation 3.

$$C = \frac{q}{V} \tag{3}$$

The theory behind the work conducted at Naval Postgraduate School is adapted from dielectric theory. To elaborate on the theory of all dielectrics: ceramic, EDLC, and SDM operate via the formation of dipoles that are polarized opposite to the dipoles formed by charges on the electrodes. The opposite polarization means the net field at any point in space around a capacitor is the sum of two fields: A) the dipole field of the charges on the electrodes and B) the dipole field of the polarized material within the dielectric. As these fields are oppositely polarized, the net field (net field = A-B) everywhere is reduced by the presence of a dielectric. The strength of a field created by a dipole is the product of the dipole length (charge separation distance) and the net charge. Thus, to minimize the field at every point in space it is advantageous to use dielectrics with large charge concentrations and large charge separation. SDM, constructed of a highly mobile ion-dense solution supported by a solid inert matrix, is advantageous for these reasons, it is designed to create the most polarizable media [29-30].

C. THESIS OBJECTIVE

The primary objectives of this thesis were to i) investigate the applicability of super dielectric material (SDM) theory to PL-SDM parallel plate capacitors for ii) the purpose of determining the value of this potential technology to the U.S. Navy. First, SDM theory was utilized in the selection of SDM material candidates for use in parallel plate capacitors. Additionally, structural modifications to the material were made to improve capacitor performance based on SDM predicated behavior of ions in solution. Second, parameters of particular interest to potential U.S. Navy applications such as cost, and energy and power density as a function of discharge time were evaluated. Thus, the focus of the program was to evaluate capacitor performance, including energy and power density, of a recently designed, simple to fabricate, low-material cost variant of the SDM family. This new form of SDM, PL-SDM, was fabricated by mechanically creating an array of holes into a low cost electrically insulating material (e.g., cellulose films) and then saturating the membranes with aqueous solutions containing high densities of free ions (e.g., potassium hydroxide solution). Parallel plate capacitors were assembled from the SDM by squeezing the solution saturated membranes between carbon electrodes. Tests to determine applicability of the SDM model to PL-SDM included studies of the effect of dielectric layer

open area, thickness, and saturation level. These tests also provided the data needed to optimize SDM performance, and confidently design the large, high voltage capacitor banks needed for advanced weapons and defense systems.

II. EXPERIMENTAL METHODS

Organization of this section, shown in Figure 3, follows the general flow of methods and equipment used in the study.

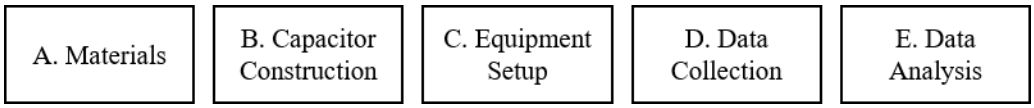


Figure 3. Organization and Process Flow

A. MATERIALS

Ten PL-SDM parallel plate capacitors, constructed from basic and inexpensive materials, were tested. Each capacitor was built with these specific materials i) Grafoil, ii) aqueous potassium hydroxide (KOH) solutions, and iii) a commercial porous filter/separator material.

1. Grafoil Electrodes

Carbon electrodes were cut out of GTA grade Grafoil flexible sheets (0.76 [mm] thick, minimum 99.5% graphite) into 2.5x2.5 cm^2 squares. Grafoil, manufactured by Graftech, is “prepared by chemically treating natural graphite flake to form a compound with and between the layers of the graphite structure” resulting in very thin (0.0762 to 1.651 [mm]) and flexible carbon-based material [31].

2. Potassium Hydroxide (KOH) Solution

The electrolyte, a 120%wt (by weight) KOH solution, was prepared by thoroughly dissolving 12 [g] of solid KOH (Sigma Aldrich) in 10 [g] of deionized water. KOH was selected for its high room temperature solubility ratio of 121:100 [g] of KOH:H_20. This ensured a high density of dissociated K^+ and OH^- ions in solution.

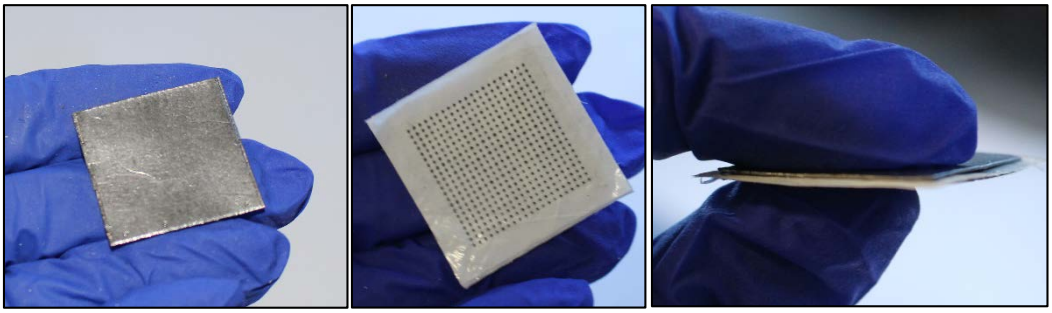
3. Celgard H1612 Membrane Separators

Celgard membrane (Celgard, LLC, USA) is an electrically insulating microporous material that is commonly used in capacitors and batteries to allow migration of electrically charged species while isolating electrodes in an electrolytic bath [4,32,33]. For this purpose, Celgard membrane was sandwiched between capacitor electrodes, and has been similarly used in other capacitor studies. Separators with 10, 100, and 441 holes were cut out of Celgard H1612 microporous membrane sheets by laser engraver (GCC LaserPro Spirit GLS) set to extremely low speed and power levels. The laser cutter made holes of equal spacing, then cut around the holes to create 2.5x2.5 or 3.0x3.0 cm^2 squares. In instances where no-hole separators were created, the laser cutter simply cut 2.5x2.5 or 3.0x3.0 cm^2 squares.

B. CAPACITOR CONSTRUCTION IN SUPPORT OF HYPOTHESIS TESTING

The capacitors were constructed to test three major hypotheses. None of the hypotheses regarded the electrodes, thus the same size Grafoil electrodes were employed in all cases. Only the structure of the dielectric layer composed of a Celgard matrix and an active dipole forming aqueous salt (KOH) solution was varied. The first hypothesis tested was that the more open area/punched out area (POA) (holes) in the dielectric matrix, the higher the capacitance, energy, power, etc. Thus, capacitors were constructed with different amounts of POA. Specifically, four different hole patterns. In all cases, the holes were the same size, only the number of holes was changed. A second hypothesis tested was that the energy and power density for aligned POA in the dielectric layer would be nearly independent of the thickness of the dielectric matrix. Thus, multiple layers with the same pattern aligned were tested. A final hypothesis was that the gross amount of aqueous KOH, above the minimum required to fill the POA, would be inconsequential. Thus, two levels of solution impregnation were studied and contrasted. The maximum saturation was achieved by immersing the Celgard dielectric matrix in 120%wt KOH solution for several seconds. This was followed by gentle shaking to remove excess solution. Immediately thereafter it was placed as the dielectric layer. The dielectric clearly was very wet, and visually it was clear some solution was transferred to the carbon electrodes. The minimum

saturation was created by placing exactly 1 drop of solution (0.049 +/- 0.004 [g]) per layer of Celgard employed in the control samples, and 6 total drops of solution (0.270 +/- 0.087 [g]) in multiple layers of Celgard employed in the experimental samples. Close examination showed no indication that the dielectrics were wet, nor was there any visual evidence of any absorption by the electrodes. Construction of PL-SDM parallel plate capacitor is shown in Figure 4.

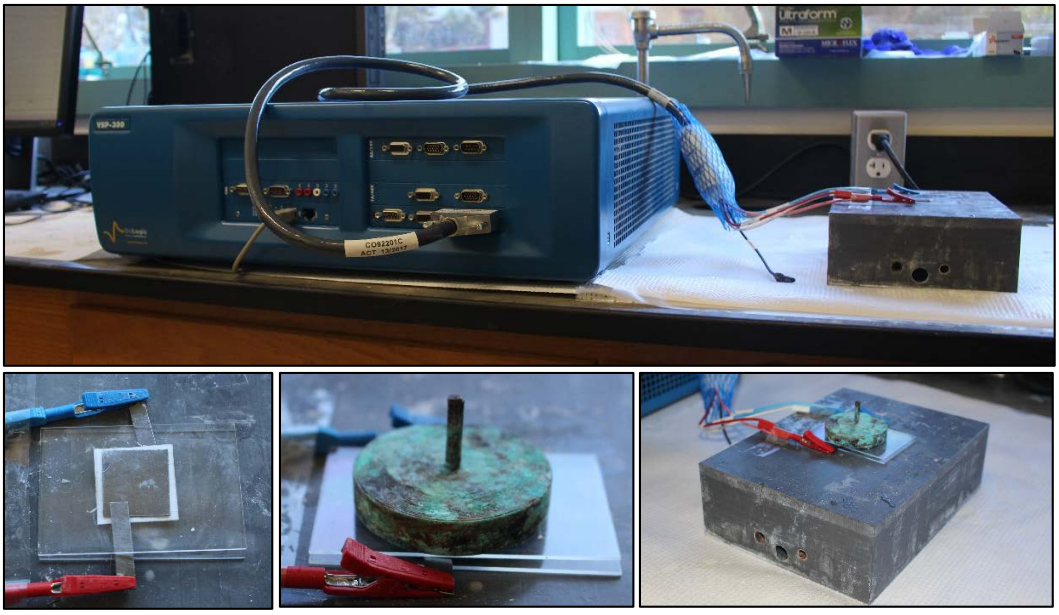


Photos from left to right show the order of capacitor construction beginning with the first 2.5x2.5 [cm^2] Grafoil electrode (left) followed by the 3x3 [cm^3] dielectric layer comprised of Celgard matrix of 441-hole POA and 120wt% KOH solution (center), and second 2.5x2.5 [cm^2] Grafoil electrode (right).

Figure 4. Construction of Parallel Plate PL-SDM Capacitors

C. EQUIPMENT SET-UP AND DESIGN OF EXPERIMENTS

The Bio-Logic VSP-300 and EC Lab 10.39 control software were used to collect and analyze data. The VSP-300 is a research grade galvanostat used to study batteries and capacitors. EC Lab control software allows the user to view and analyze in-progress and completed experimental data. In preparation for testing, the capacitor was placed onto a glass slide and transferred to a test jig. Top and bottom capacitor electrodes were connected to VSP-300 charging cables via alligator clips and extended Grafoil leads. A second glass slide was placed on top of the capacitor creating a glass-capacitor-glass arrangement followed by placement of a weight on top of the arrangement to compress all components. Equipment set-up and test jig, as discussed, are shown in Figure 5.



The Bio-Logic VSP-300 (top) was used to test capacitors. In preparation for testing, a capacitor was placed between glass slides and connected to VSP charging cables via alligator clips and Grafoil leads (bottom left), and a weight was placed on top of the glass-capacitor-glass arrangement (bottom center) to compress capacitor components. Capacitors in testing remained in this configuration on the test jig (bottom right) throughout the duration of testing.

Figure 5. Equipment Set-up and Test Jig

EC Lab offers a variety of test techniques for the user to customize based on their research needs. The Modulo Bat (MB) technique was chosen for its flexibility to implement test sequences of different control modes, limiting and recording conditions. A three-step protocol, modelled after protocols used in industry to "rate" EDLCs was used in all cases. The steps were i) constant current charge to a select maximum voltage, ii) holding the capacitor at that maximum voltage for an assigned period, and iii) discharging the capacitor at a constant current. At any particular parameter set, the capacitor was charged and discharged at least 10 times in order to determine if the values of dielectric, energy density, etc., were stable. For each capacitor, several currents were employed in the discharge step. This was done to change the discharge time/period of the process. Roughly, this corresponds to measuring the behavior as a function of frequency. In general, nine different discharge currents were used, and these were selected so that the gross discharge times ranged over at least three orders of magnitude. An ideal set of discharge times would be 100, 10, 1 and 0.1 [s]. Unfortunately, it is virtually impossible to select currents that yield

precise discharge times so the actual values only overlapped the range (100 to 0.1 [s]) of the ideal values. Later, plotting of the data showed very good agreement with simple power law relations, allowing a reasonable estimate of values to be made for any discharge time. Limiting conditions were imposed on constant current and voltage operating modes. These conditions were operating voltages of 0–2.2 or 0–2.3 [V], and hold durations of 10, 200, 400, and 600 [s]. In all cases recording conditions were 0.01 units ([V], [mA], or [s]). A summary of successfully completed experiments is provided in Table 1.

Table 1. Summary of Completed Experiments

	Capacitor				Experiment		
	Electrode Pairs	POA	Separator Layers	KOH Soln	Sequence	Operating Voltage [V]	Hold Time [s]
Control Samples	Single	Blank	Single	1 drop	CHD	0-2.3	10, 200, 600
	Single	Blank	Single	soak	CHD	0-2.3	10, 200, 600
	Triple	Blank	Single	soak	CHD	0-2.3	10, 200, 600
Experimental Samples	Single	10	Single	soak	CHD	0-2.3	10, 200
	Single	100	Single	soak	CHD	0-2.3	200, 400
	Single	100	Double	6 drops	CHD	0-2.3	10, 200
	Single	441	Single	soak	CHD	0-2.2	10, 200, 600
	Single	441	Double	6 drops	CHD	0.2.2	10
	Single	441	Double	soak	CHD	0-2.2	200
	Single	441	Triple	6 drops	CHD	0-2.2	10, 200

From here forward, a single test sequence or section(s) of a single test sequence: constant current charge (C), constant voltage hold (H), constant current discharge (D), and loop (L), will be designated CHDL or other letter combinations such as CHD or CD. A single experiment contained several continuous CHD sequences in which C and H remained the same, and D gradually increased.

1. Constant Current Charge

The EC Lab constant current charge module, shown in Figure 6, required several user-defined current parameters: constant current value, limiting and recording conditions, and testing ranges. Constant current values were refined by trial and error. Generally, capacitors made of separators with more holes were tolerant of higher current than separators with fewer holes. Therefore, constant currents from 2 to 20 [mA] depending on separator hole count were used. In Figure 6, a constant current of 5 [mA] and limiting condition of 2.3 [V] required the capacitor to reach a maximum operating voltage of 2.3 [V] using a constant current charge of 2 [mA] before proceeding to the next step. The same set of recording conditions: time and ewe (voltage), and ranges: E (voltage) range, I (current) range, and bandwidth was used throughout an experiment. This was done to ensure continuity of general testing and equipment parameters.

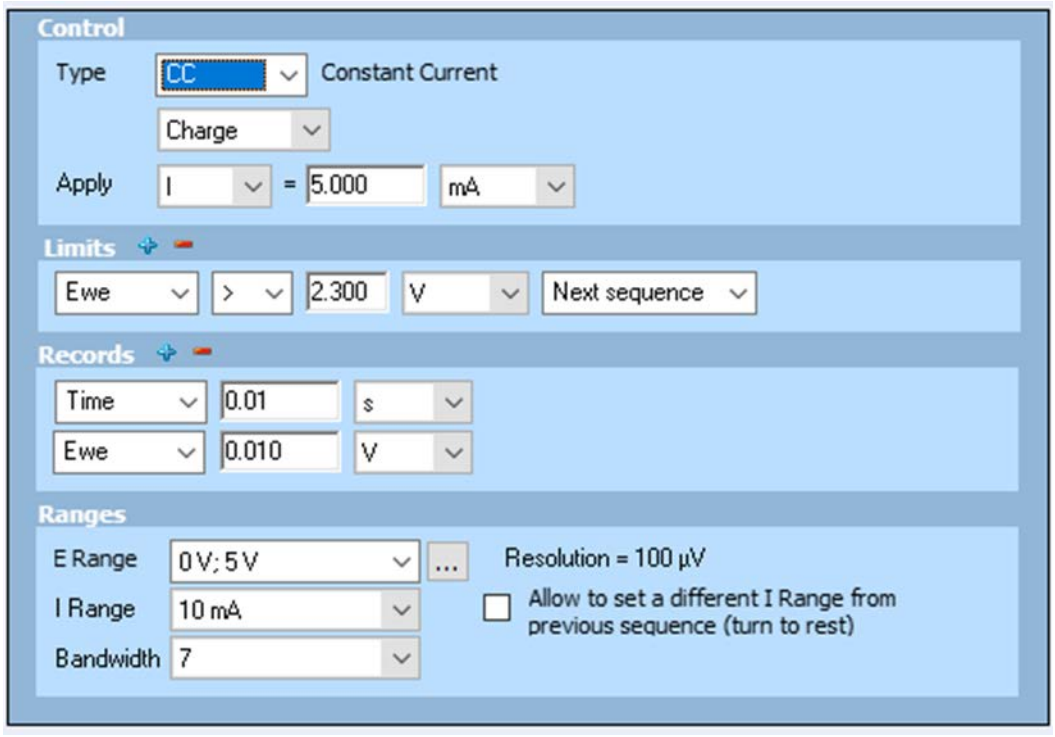


Figure 6. Example of EC Lab Constant Current Charge Module and Parameters

2. Constant Voltage Hold

The EC Lab constant voltage hold module, shown in Figure 7, required user-defined hold parameters. In this figure, a constant voltage hold of 2.3 [V] of no less than 200 [s] required the capacitor to hold its charge of 2.3 [V] for 200 [s] before proceeding to the next step. A CD sequence is sufficient for acquiring capacitor performance values; however, use of constant voltage hold is known to improve performance. Therefore, constant voltage holds of 10, 200, 400, and 600 [s] at 2.2 or 2.3 [V] were implemented to determine the effect of increasing hold time. The theoretical explanation for improved capacitor performance is included in Chapter IV.

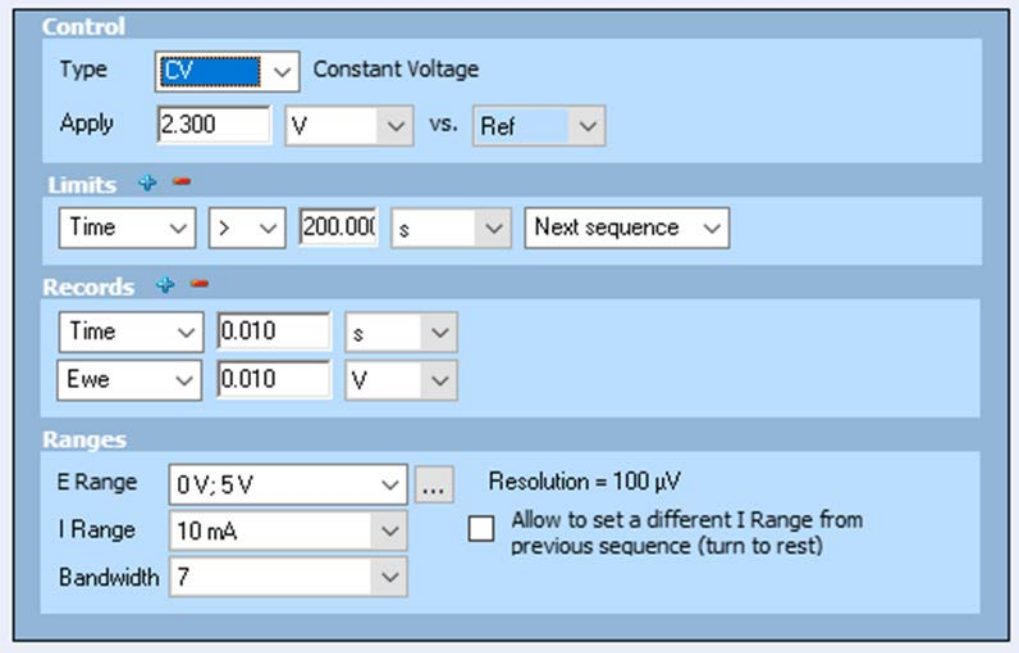


Figure 7. Example of EC Lab Constant Voltage Charge Module and Parameters

3. Constant Current Discharge

The EC Lab constant current discharge module, shown in Figure 8, required user-defined current parameters. In this figure, a constant current discharge of 100 [mA] and limiting condition of no greater than 0 [V] required the capacitor to reach a minimum operating voltage of 0 [V] using a discharge current of 1 [mA]. Over the course of an experiment constant current values were incrementally increased in order to determine capacitor performance trend. Due to limitations of the equipment, discharge time increments approaching 0.01 units sometimes resulted in unreliable discharge data, so this data was ultimately discarded.

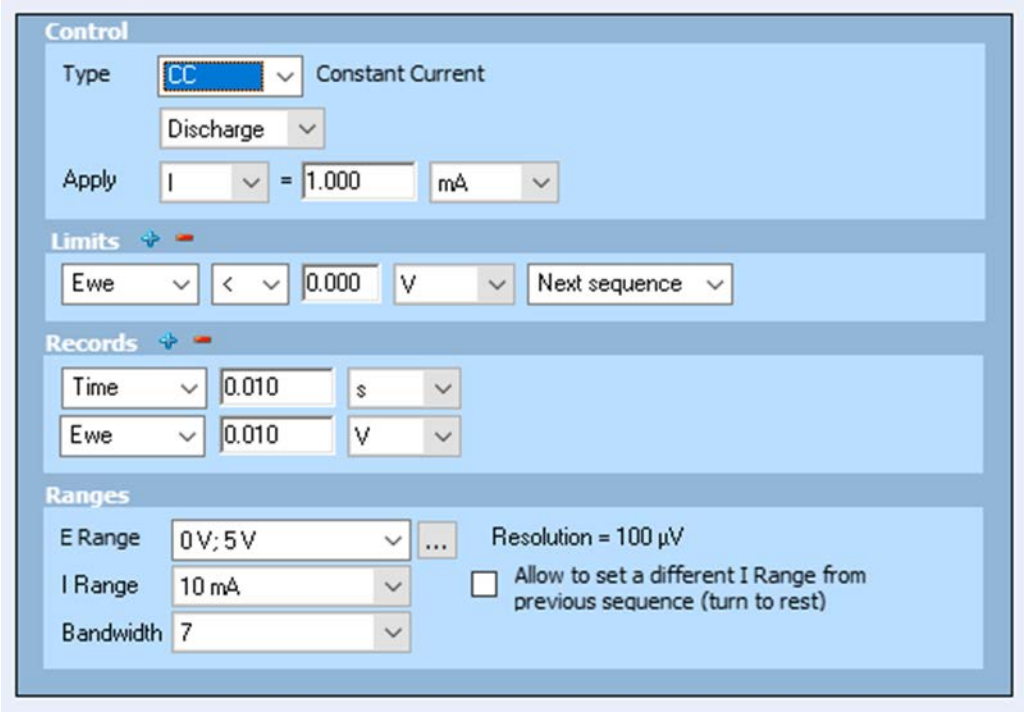


Figure 8. Example of EC Lab Constant Current Discharge Module and Parameters

4. Loop

Lastly, the EC Lab loop module, shown in Figure 9, allowed the user to specify the number of CHD sequences performed. The CHD sequence was looped a total of ten times before the next CHD sequence in the experiment was executed.

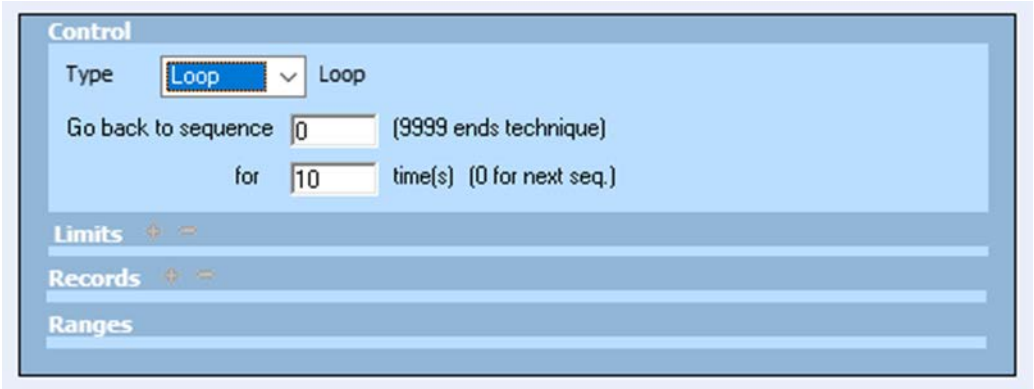


Figure 9. Example of EC Lab Loop Module and Parameters

D. DATA COLLECTION

During testing, the experimental variables, voltage and current in relation to time, were displayed in EC Lab. Three defining features of the voltage and time curve, displayed in Figure 10, showed the CHD sequence progression in terms of voltage from left to right: increasing operating voltage (from 0 to 2.3 [V]), constant operating voltage (of 2.3 [V]), and decreasing operating voltage (from 2.3 to 0 [V]).

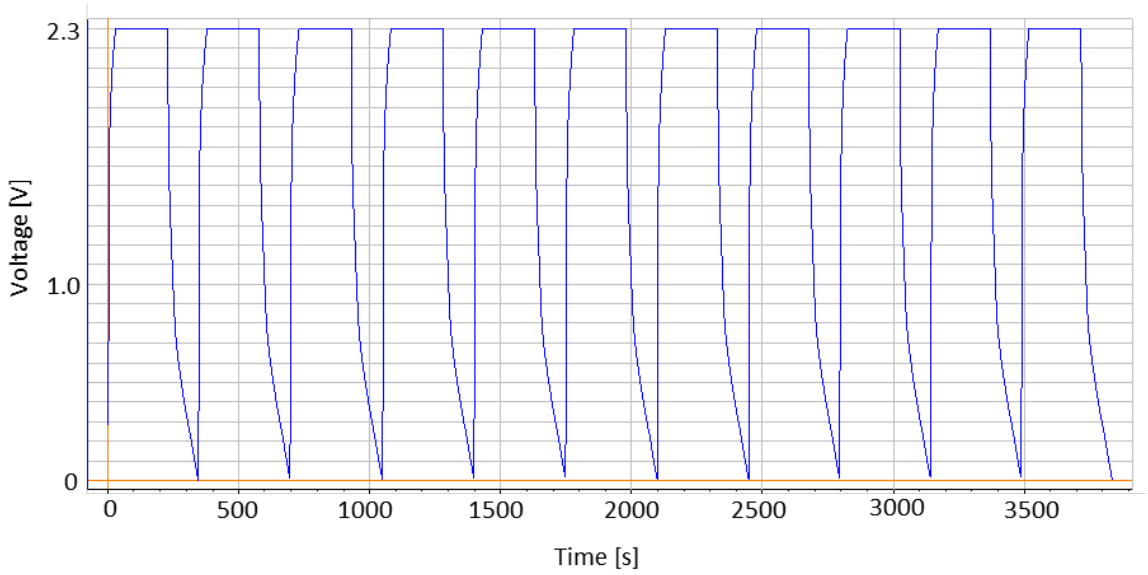


Figure 10. Example of EC Lab Data Collection (Voltage in Relation to Time)

The current and time curve, displayed in Figure 11, showed the same CHD sequence progression in terms of current from left to right: constant current, followed by decreasing current, and again constant current.

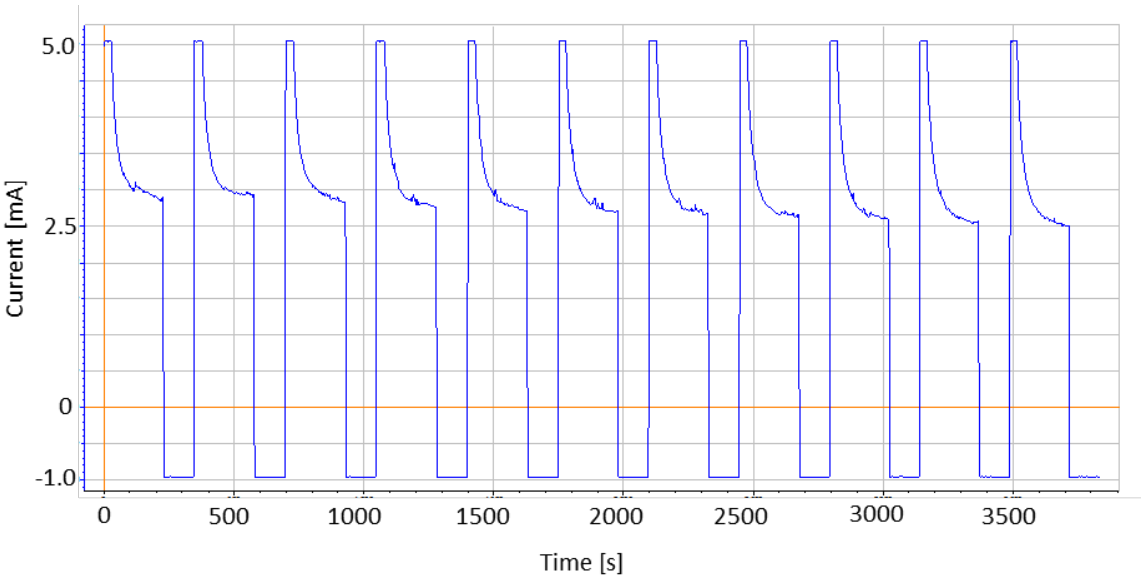


Figure 11. Example of EC Lab Data Collection (Current in Relation to Time)

The combined experimental data, displayed in Figure 12, provided a complete picture of the status of in-progress testing as well as completed experiments. Discrepancies such as excessive voltage overshoot, undershoot, current leakage, or shorts discovered during testing warranted troubleshooting of the equipment set-up, and repeated testing of the capacitor to attain characteristic experimental curves described.

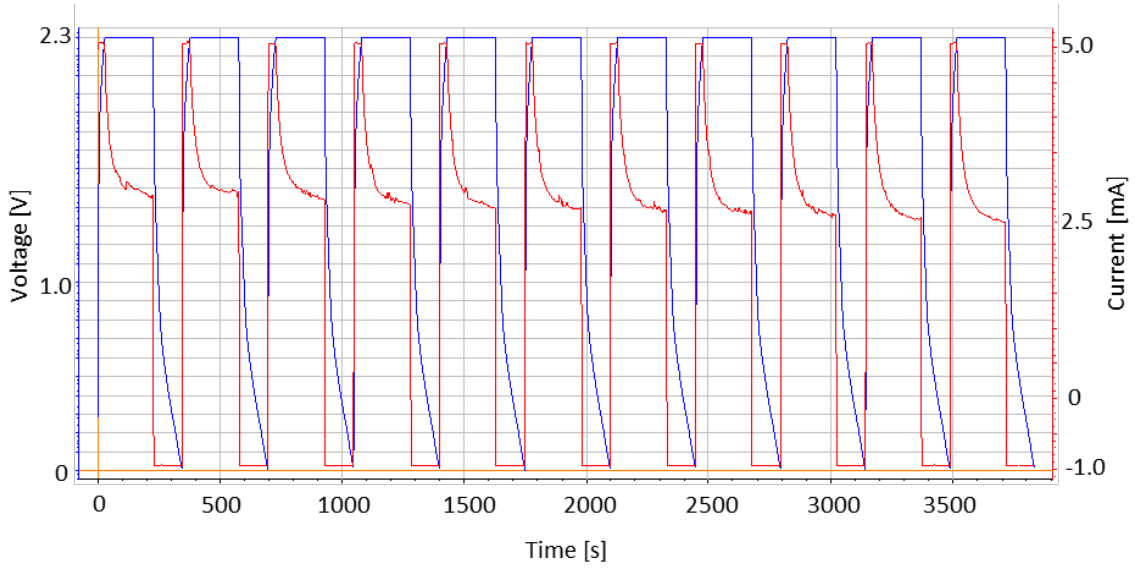


Figure 12. Example of EC Lab Data Collection (Combined Voltage and Current in Relation to Time)

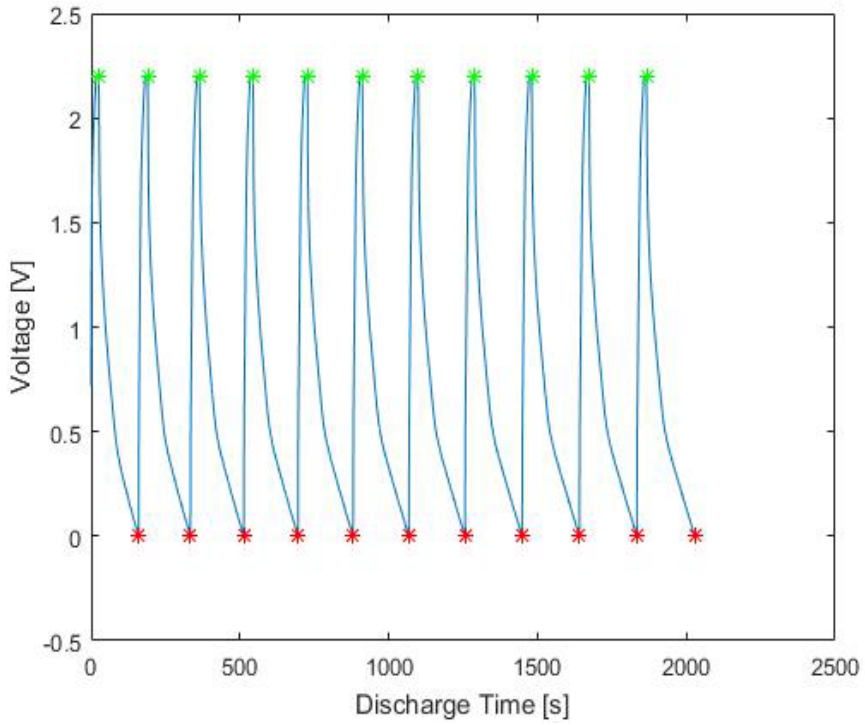
E. DATA ANALYSIS

Post-processing of the data was performed in MATLAB. Capacitor performance values: capacitance, total energy, mass and volumetric energy densities, total power, mass and volumetric power densities, and dielectric constant were calculated using the governing equations presented. Data points were calculated by averaging performance values of the last five cycles of every CHD sequence in an experiment. These data points were used to generate plots of capacitor performance.

1. Total Energy

Total energy, E, was calculated using equation 3. Total area under the discharge curves, $\int Vdt$, shown in Figure 13, were calculated using trapezoidal numerical integration of data points from the beginning to end of each discharge curve, marked by green and red asterisks, in a CHD sequence in approximate experimental time steps of 0.01 [s]. Current, I, is based on constant discharge current in [mA].

$$E_{tot} = \left(\int Vdt\right) I\left(10^{-3}\right) \tag{4}$$



Calculation of $\int Vdt$ between operating voltages, 0 and 2.2 [V] in this example, were calculated from the beginning to end of each discharge curve marked by green and red asterisks in a CHD sequence.

Figure 13. Example of Area, $\int Vdt$, Calculation in MATLAB

2. Energy Density

Energy densities were calculated using equations 4 and 5. Total energy, E, was calculated in equation 3. Volume, v, was based on the separator and electrode contact area, separator thickness, and number of dielectric layers. In all cases separator and electrode contact area, a, was 6.25×10^{-4} [m^2], and dielectric thickness, t, was 16×10^{-6} [m]. Mass, m, was based on a highly conservative separator density, ρ, of 1000 [$\frac{kg}{m}$], and known volume, v, based on area, dielectric thickness, and number of dielectric layers. Dielectric vice electrode properties and dimensions were used to calculate energy densities, because electrode charge storage does not significantly contribute to capacitance or energy.

$$Volumetric\ energy\ density = \frac{E_{tot}}{v};\ where\ v = (a)(t)(\#layers) \tag{5}$$

$$Mass\ energy\ density = \frac{E_{tot}}{m};\ where\ m = \rho v \tag{6}$$

3. Total Power

Total power was calculated using equation 6. Total energy, E, was determined in equation 3. Discharge time, DT, was based on the time it took for a capacitor to discharge between voltage operating limits.

$$P_{tot} = \frac{E_{tot}}{DT} \tag{7}$$

4. Power Density

Power density was calculated using equations 7 and 8. Total power, P, was determined in equation 6. Mass, m, and volume, v, were based on the same variables discussed in the calculation of energy densities in equations 4 and 5.

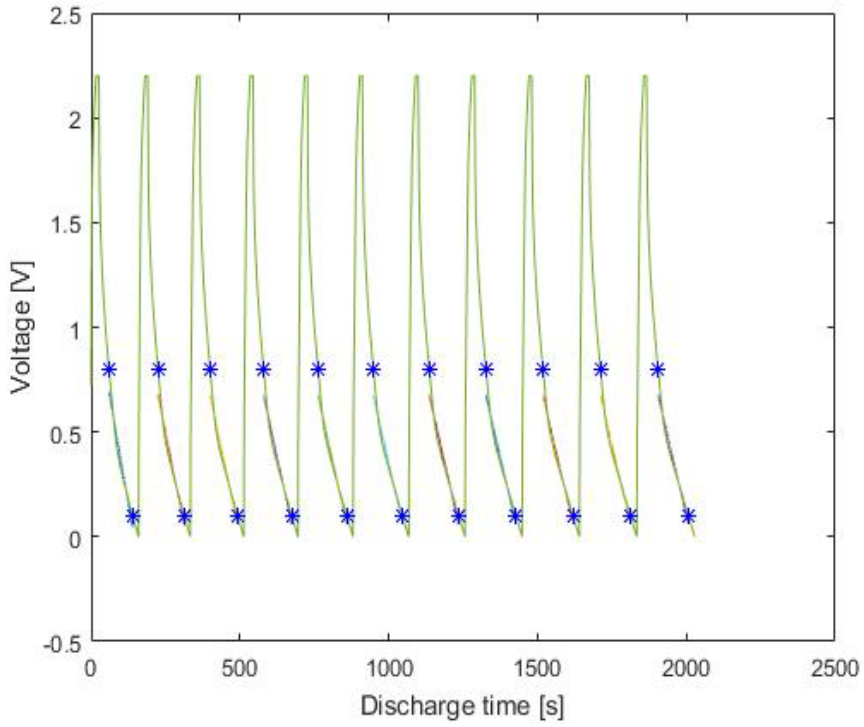
$$Volumetric\ power\ density = \frac{P_{tot}}{v} \tag{8}$$

$$Mass\ power\ density = \frac{P_{tot}}{m} \tag{9}$$

5. Capacitance

Capacitance, C, was calculated using equation 2. Current, I, was based on constant discharge current in [mA]. Discharge slopes, $\frac{dV}{dt}$, shown in Figure 14, were determined using the linear least squares method between experimental voltage values closest to 0.8 and 0.1 [V], marked by blue asterisks, for each discharge curve in a CHD sequence.

$$C = \frac{I\left(10^{-3}\right)}{\frac{dV}{dt}} \tag{10}$$



Discharge slopes, $\frac{dV}{dt}$, represented by alternating multi-color lines that best fit the data between 0.8 and 0.1 [V], marked by blue asterisks, were determined for each discharge curve in a CHD sequence.

Figure 14. Example of Slope, $\frac{dV}{dt}$, Calculation in MATLAB

6. Dielectric Constant

Dielectric constant, ε, was calculated using equation 9. Capacitance, C, was determined in equation 2. The constant, ε_0, denotes the relativity of free space, and has a value of 8.85×10^{-12} [$\frac{F}{m}$]. Area, A, is based on separator and electrode contact area of 6.25×10^{-4} [m^2]. Dielectric thickness, t, is total thickness of the dielectric layer.

$$\varepsilon = \frac{Ct}{\varepsilon_0 A} \tag{11}$$

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III. RESULTS

The experimental program was designed to test three hypotheses. First, capacitor performance (i.e., total energy, energy density, total power, power density, capacitance, and dielectric constant) is a function of POA, which is directly proportional to the number of holes (all equal in size) laser cut into a single-layer Celgard membrane sheet. Second, the total energy is proportional to the total thickness of the dielectric layer. To wit, two layers of Celgard, laser cut such that holes are fully aligned, will store more energy than an equivalent one-layer dielectric, three layers so cut will store more energy than two layers, etc. Note, this SDM theory based hypothesis predicts an outcome opposite standard theory. The standard paradigm is that the thicker the dielectric the lower the capacitance and concomitantly the total energy stored. Third, the control samples, that is samples in which Celgard used as a dielectric has no holes, will have very low total energy, energy density, power and power density relative to Celgard with holes. Moreover, the level of saturation with KOH solution of the control samples will have little or no effect. Overall the results are consistent with the SDM model. Specifically, in brief the experimental outcomes show: i) the larger the POA, the greater the dielectric values, total energy stored, etc. ii) The larger the number of stacked layers/height of POA (to a certain degree), the greater the dielectric value, the higher the total stored energy, etc. iii) The level of KOH saturation of the controls made no apparent difference.

To test these hypotheses three types of samples were tested: i) control samples, that is single separator layer, no cut holes, Celgard dielectrics with different levels of saturation, ii) single layer Celgard dielectrics with different POA, iii) two and three layer Celgard dielectrics with different POA. In all cases the same material was used for the electrodes, the same Celgard material, and the same KOH solution. The results are organized by control and experimental samples, and subcategories shown in Figure 15. Control and experimental performance plots show total energy, volumetric and mass energy densities, total power, total power density, volumetric and mass volume power densities, capacitance, and dielectric constant curves for individual capacitors, and overall trends for each group

of dielectrics tested. Data points in the performance plots represent the averaged performance of the last 5 of 10 cycles of CHD sequences in an experiment.

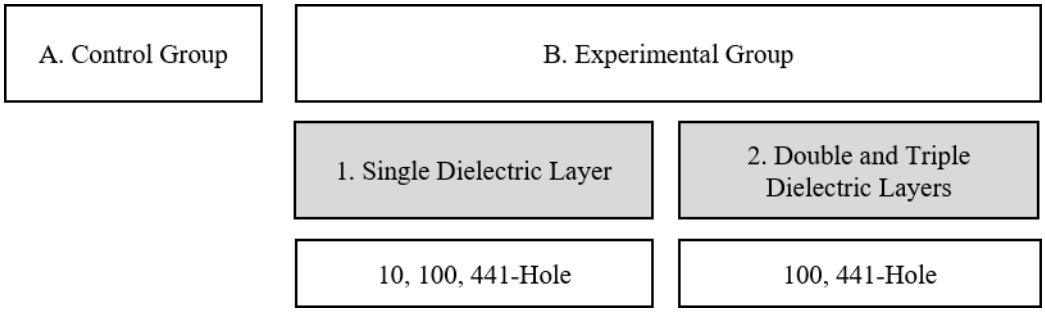


Figure 15. Organization of Results Section

A. CONTROL GROUP

Control samples were made with single dielectric layers of no-hole POA. Three control variations were constructed: two followed the maximum and minimum saturation procedures to test the effect of saturation level on capacitor performance, and one was made of six total Grafoil electrodes (three on either side of the separator layer) to test the contribution of electrode thickness to capacitor performance.

Control performance plots are displayed in Figures 16 and 23. Each performance curve is defined by a unique color coded line and marker, and a two or three term description. A two term description is used for control samples of standard build, that is one dielectric layer sandwiched between two Grafoil electrodes. For example, in the description Saturated – 10 [s], the first term indicates the level of saturation and the second term indicates the constant voltage hold duration. A three term description is used for capacitors made of six total electrodes. For example, in the series description Triple Electrodes – Saturated – 10 [s], the first term designates the capacitor build, the second term indicates the level of saturation, and the third term indicates the constant voltage hold duration in seconds. Lastly the solid black “Control Trendline” is a least squares fit of the linearized data points in the control group.

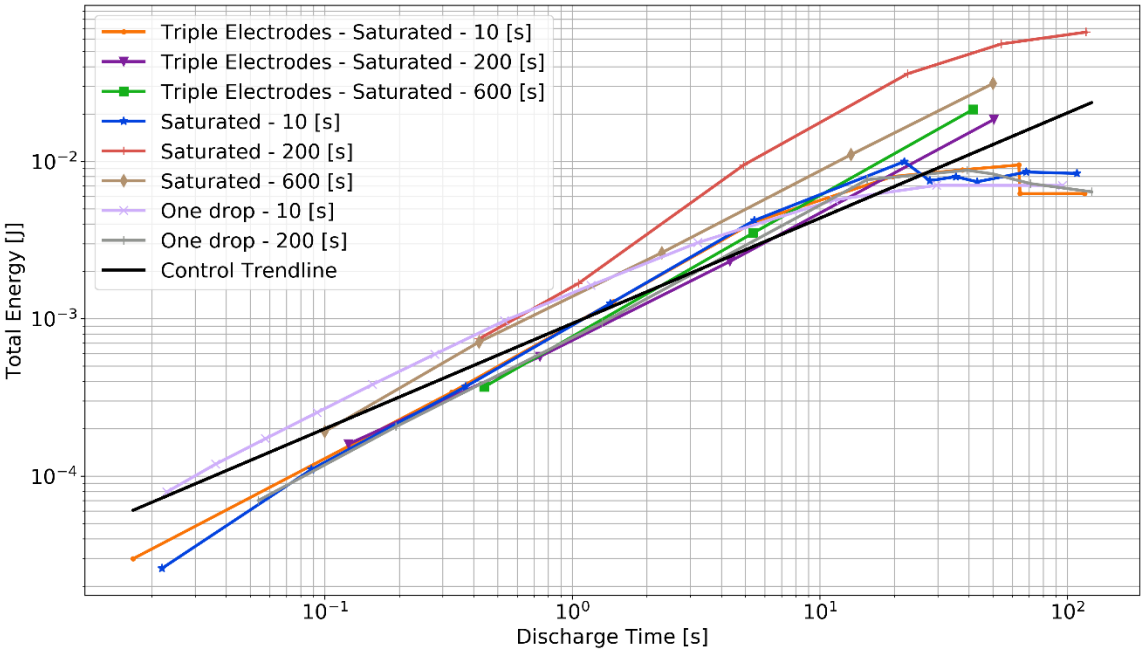


Figure 16. Total Energy of Control Group Capacitors

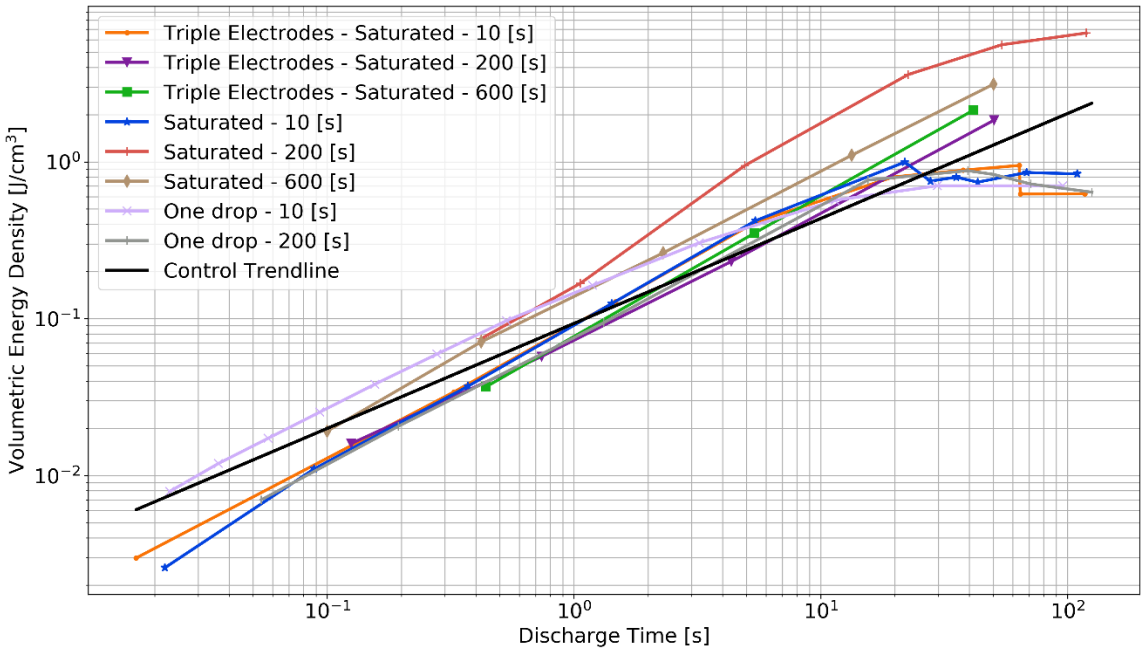


Figure 17. Volumetric Energy Density of Control Group Capacitors

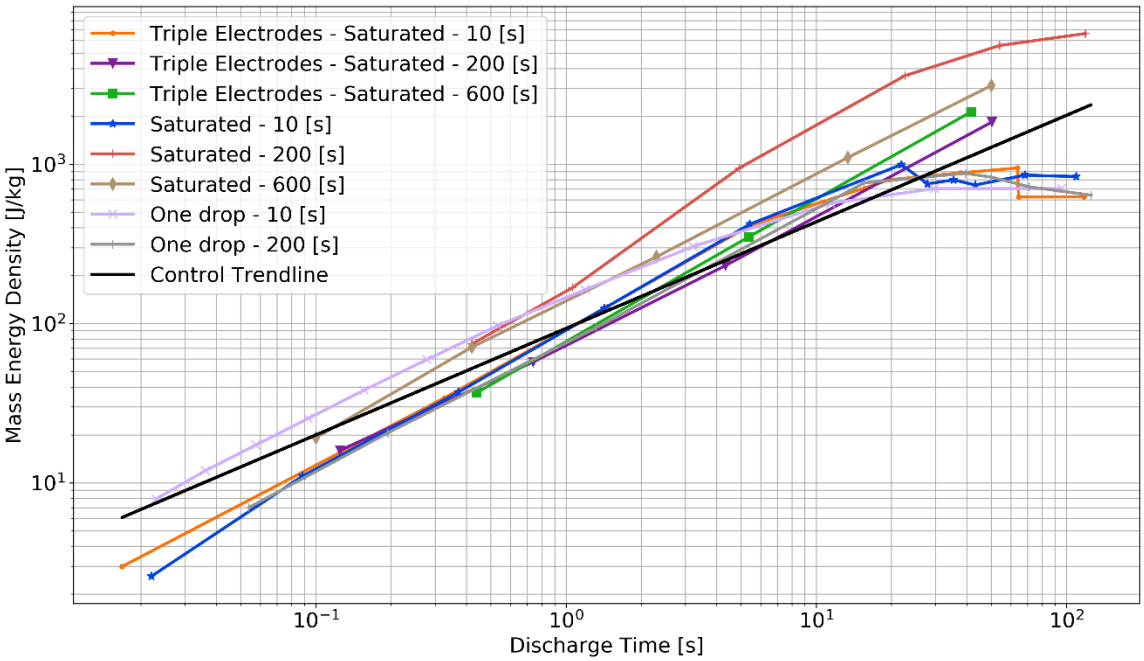


Figure 18. Mass Energy Density of Control Group Capacitors

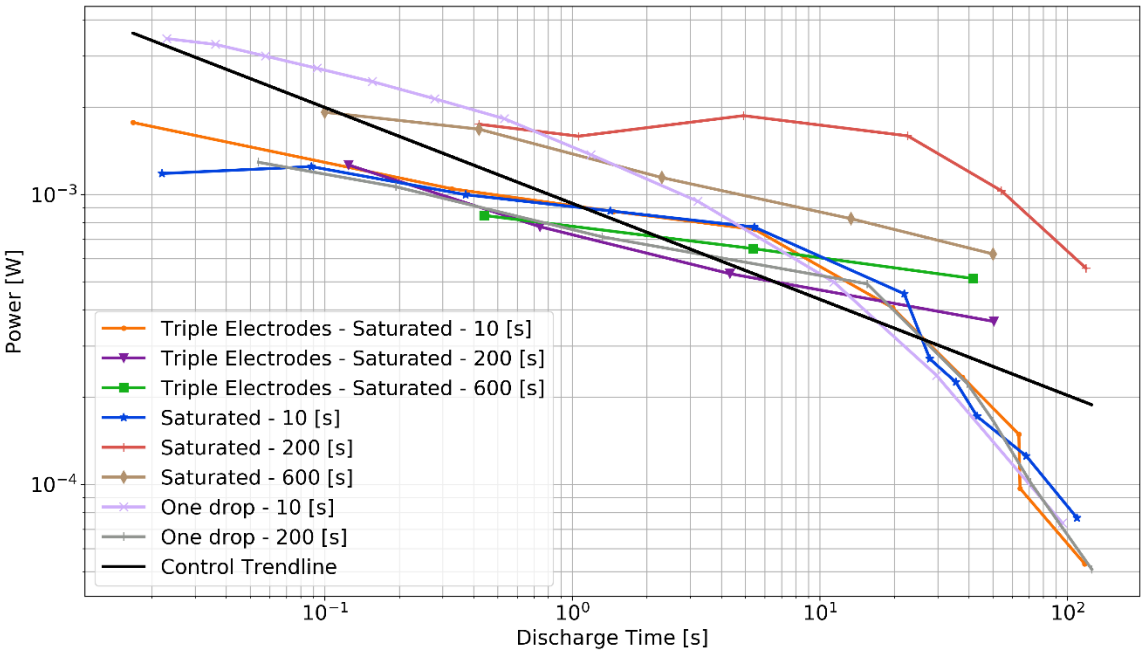


Figure 19. Total Power of Control Group Capacitors

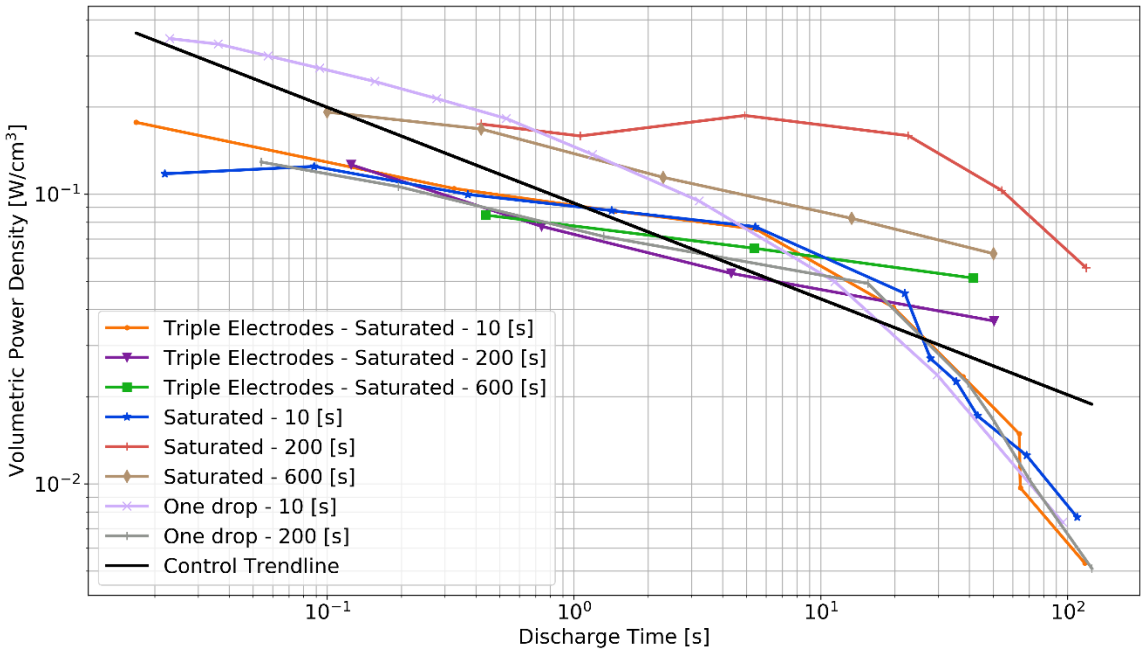


Figure 20. Volumetric Power Density of Control Group Capacitors

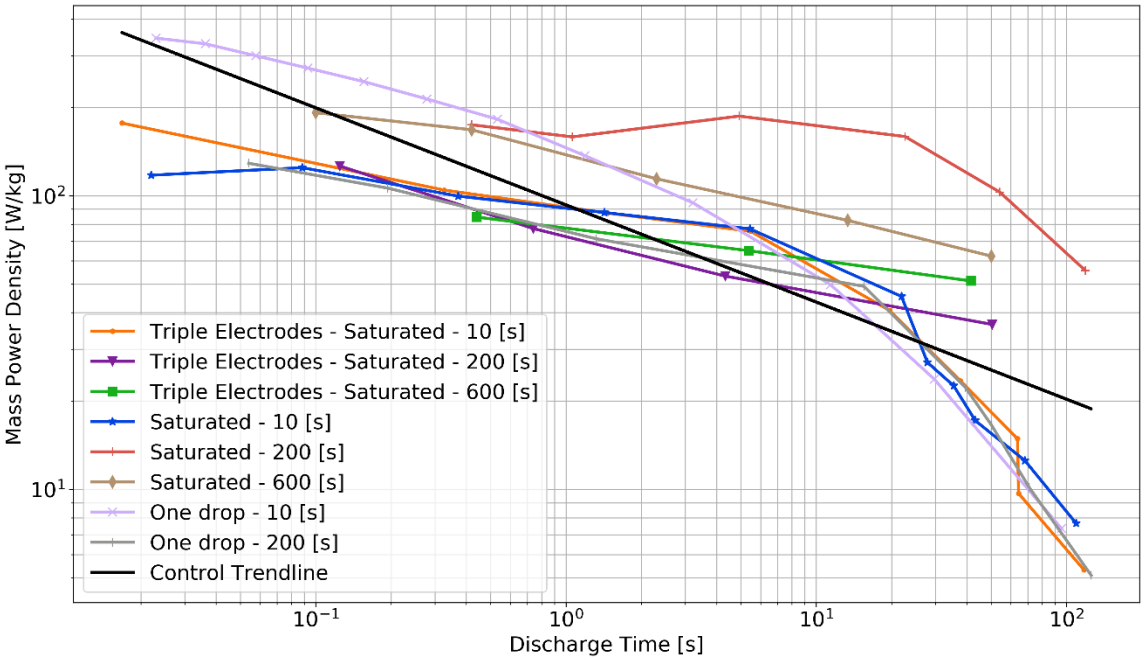


Figure 21. Mass Power Density of Control Group Capacitors

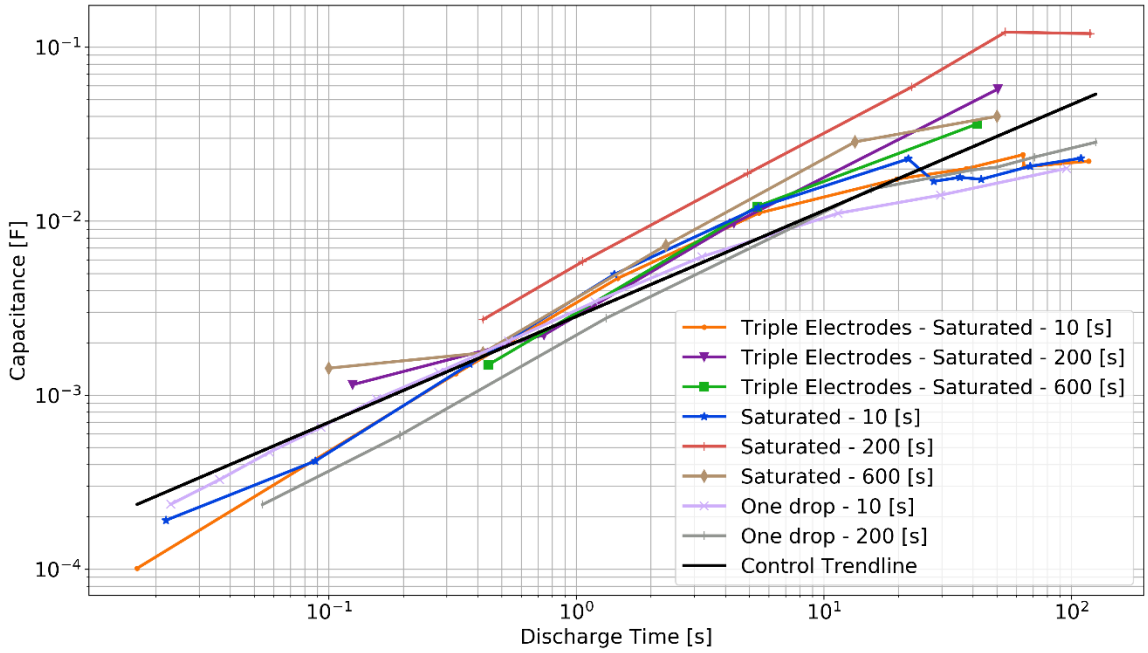


Figure 22. Capacitance of Control Group Capacitors

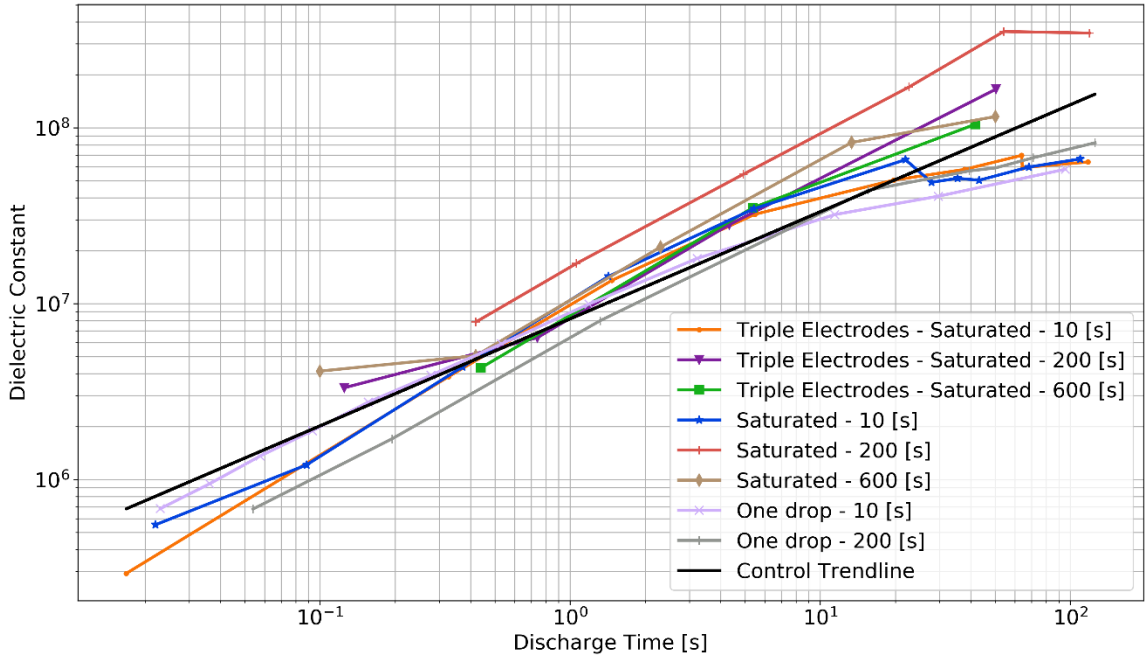


Figure 23. Dielectric Constant of Control Group Capacitors

B. EXPERIMENTAL GROUP

Experimental samples were made of single and double separator dielectric layers of 10, 100, and 441-hole POAs. Six experimental samples were constructed to test hypotheses regarding POA, aligned POA, and saturation level. In the following sub-sections, experimental samples are divided into single and double/triple dielectric layers, and respective POA.

1. Capacitors with Single Dielectric Layers of Various POA

Single dielectric performance plots are displayed in Figure 24 through 31. Each performance curve is defined by a unique color coded line and marker, and a two or three term description. For example, in the series description 10 Holes – 200 [s], the first term designates the POA, and the second term indicates the constant voltage hold duration. In two cases, a third term 'No Weight' indicates that a weight was not placed on top of the glass-capacitor-glass arrangement. This was done to determine the effect of removing compressive force on capacitor components. Lastly, the solid black "Control Trendline" was previously defined in the control group, and the dashed black "Single Dielectric Trendline" is a least squares fit of the linearized single dielectric data points.

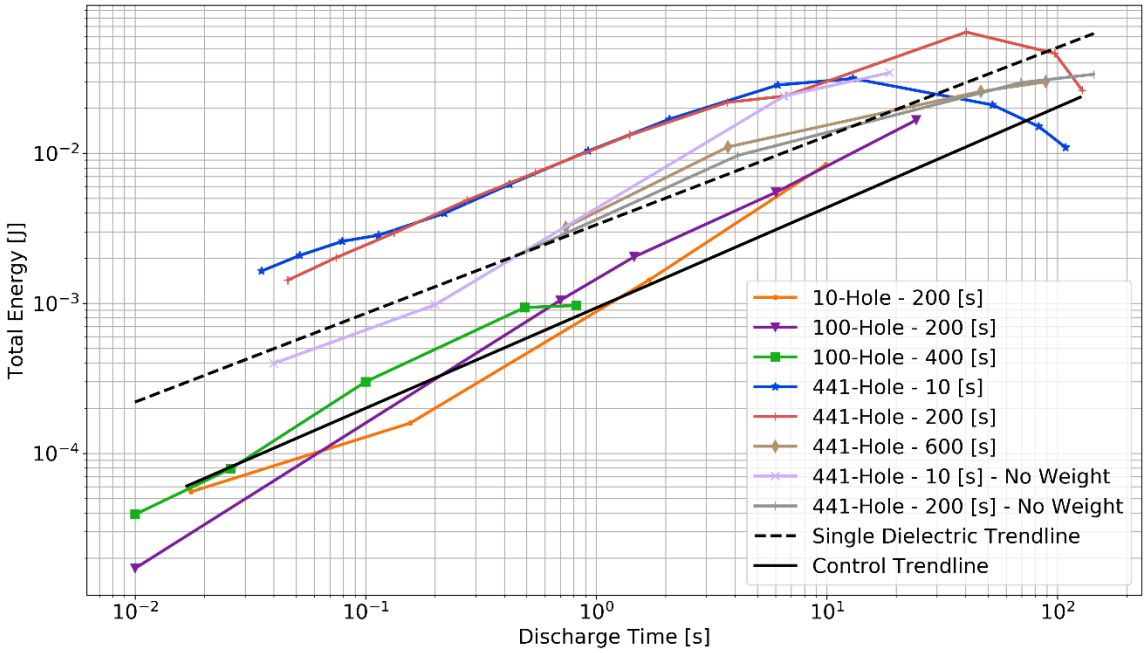


Figure 24. Total Energy of Capacitors with Single Dielectric Layers of Various POA

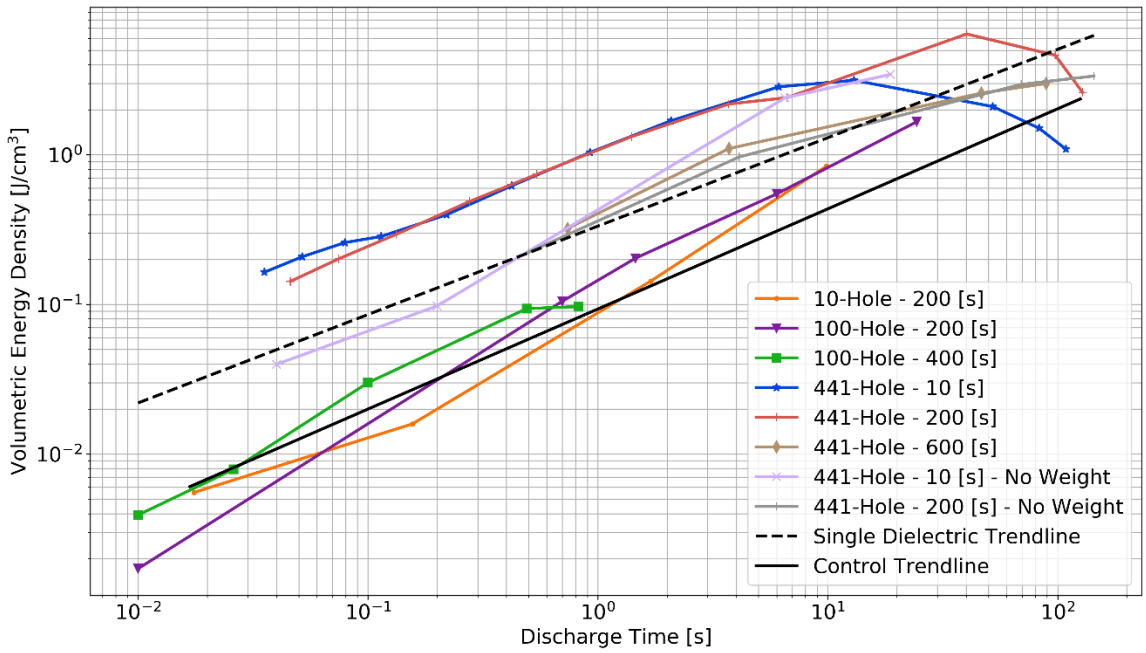


Figure 25. Volumetric Energy Density of Capacitors with Single Dielectric Layers of Various POA

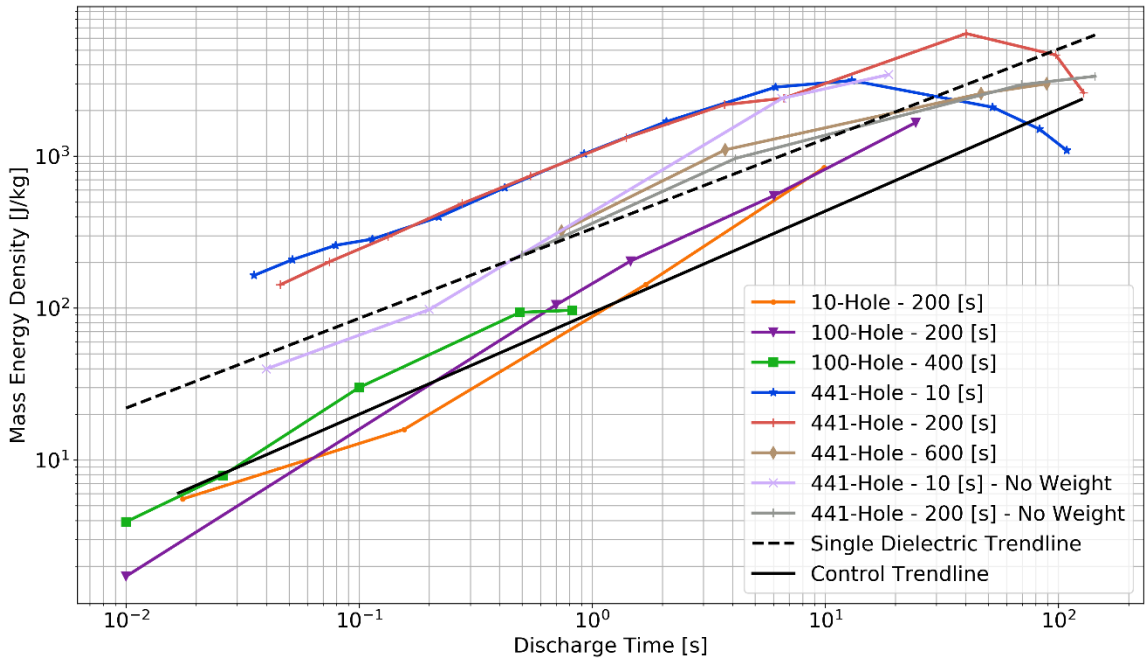


Figure 26. Mass Energy Density of Capacitors with Single Dielectric Layers of Various POA

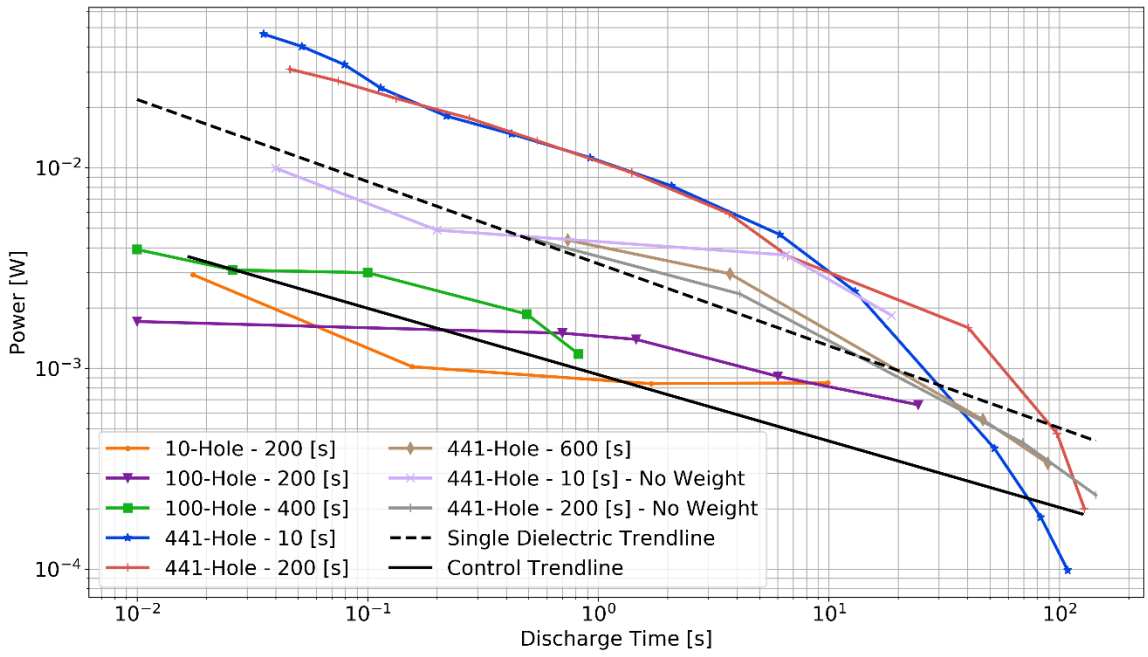


Figure 27. Total Power of Capacitors with Single Dielectric Layers of Various POA

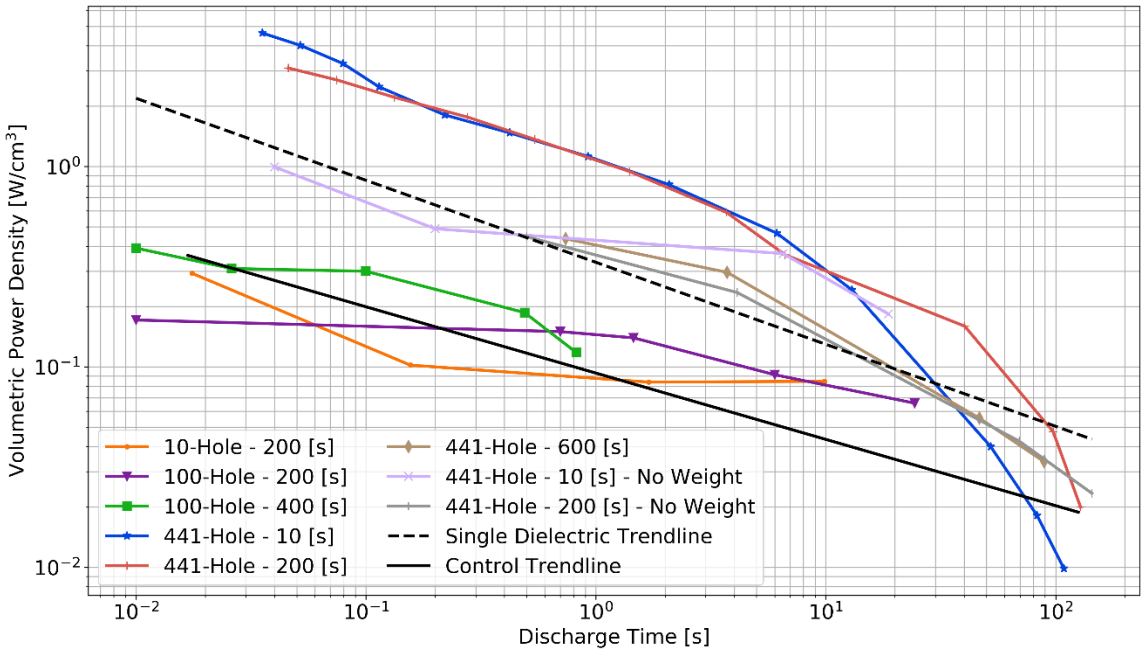


Figure 28. Volumetric Power Density of Capacitors with Single Dielectric Layers of Various POA

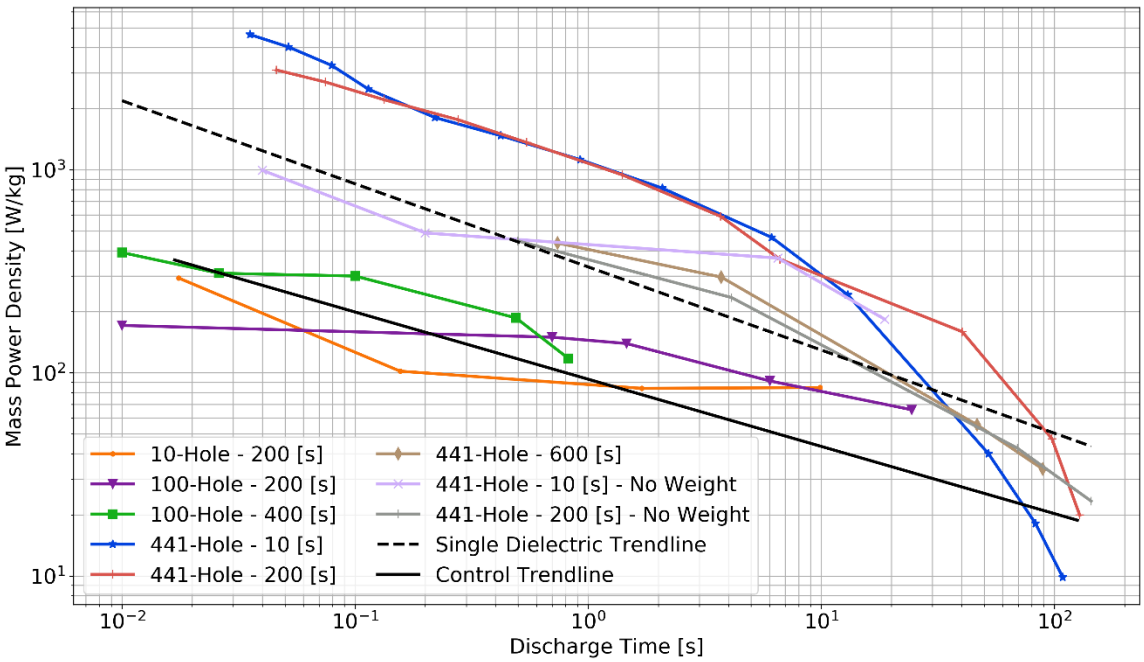


Figure 29. Mass Power Density of Capacitors with Single Dielectric Layers of Various POA

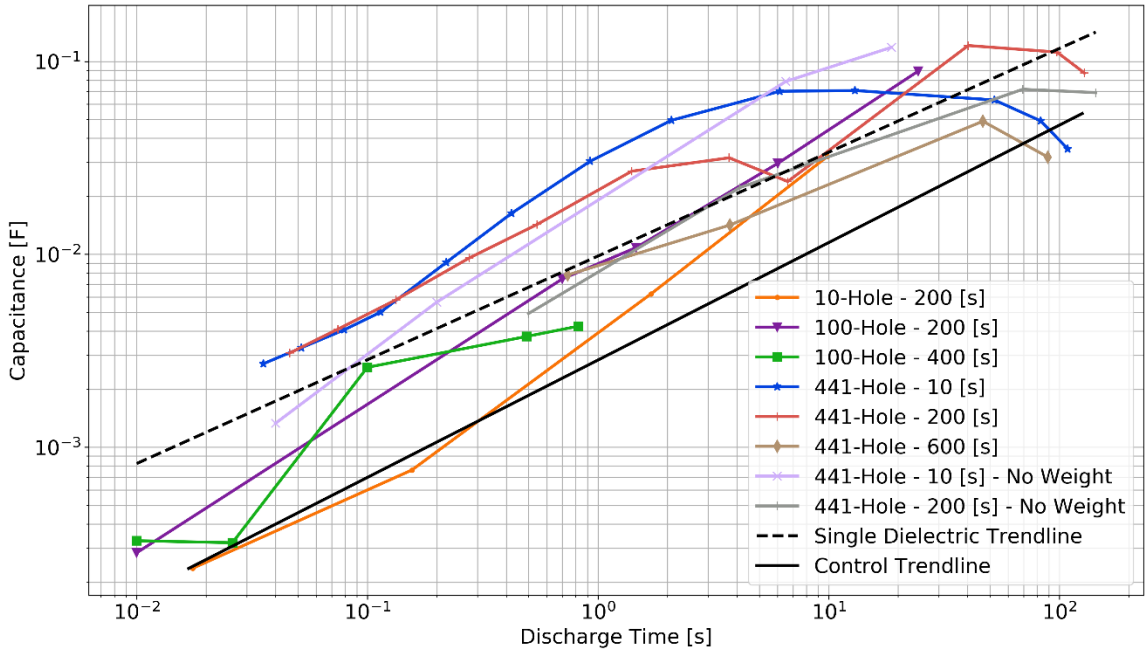


Figure 30. Capacitance of Capacitors with Single Dielectric Layers of Various POA

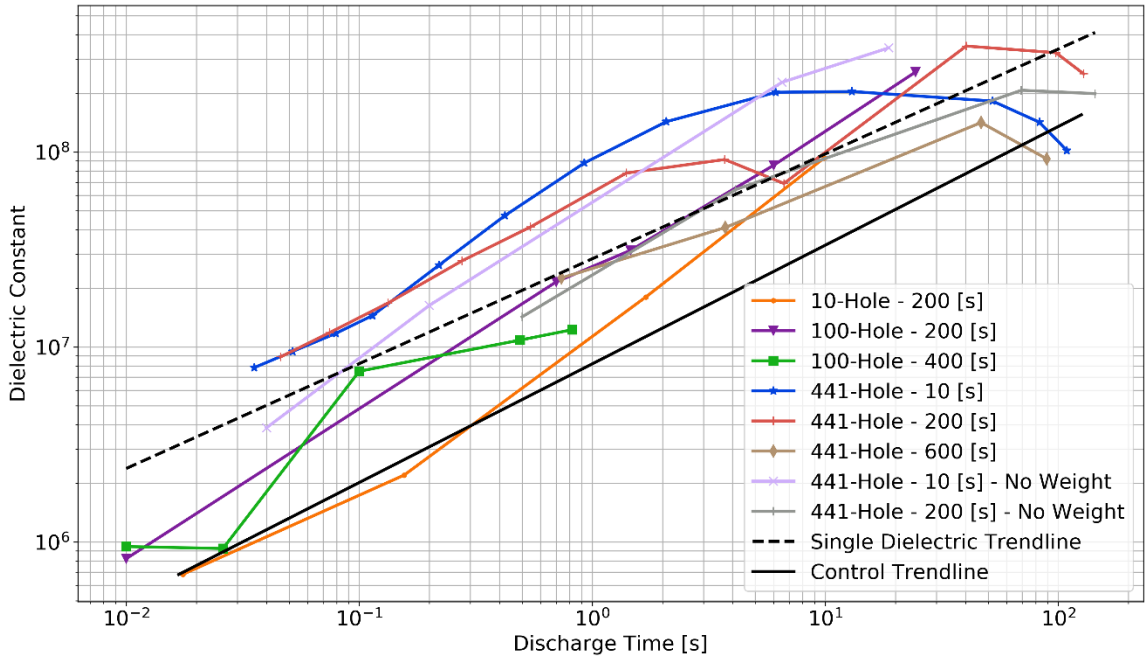


Figure 31. Dielectric Constant of Capacitors with Single Dielectric Layers of Various POA

2. Capacitors with Double and Triple Dielectric Layers of Various POA

Double and triple dielectric performance plots are displayed in Figure 32 through 39. Each performance curve is defined by a unique color coded line and marker, and a three term description. For example, in the description Double - 100 Holes – 10 [s], the first term designates the number of dielectric layers, the second term designates the number of aligned POA holes, and the third term indicates the constant voltage hold duration. Lastly, the solid black "Control Trendline" and dashed black "Single Dielectric Trendline" was previously defined, and the dotted black "Double Dielectric Trendline," is a linear least squares fit of the linearized double dielectric data points.

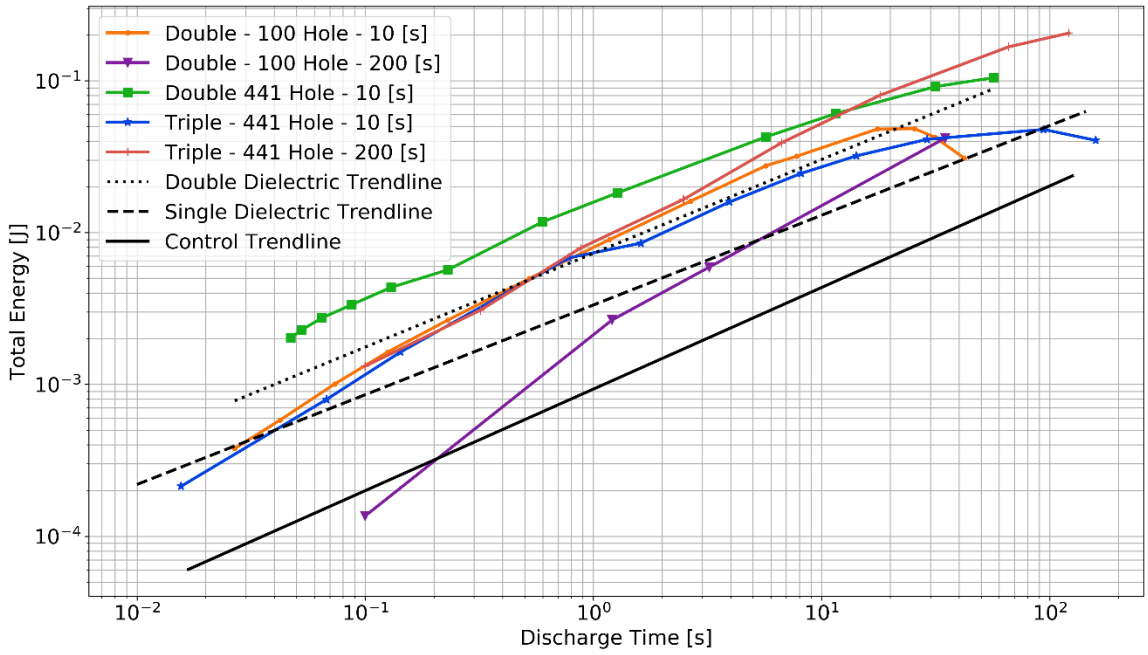


Figure 32. Total Energy of Capacitors with Double and Triple Dielectric Layers of 100 and 441-Hole POA

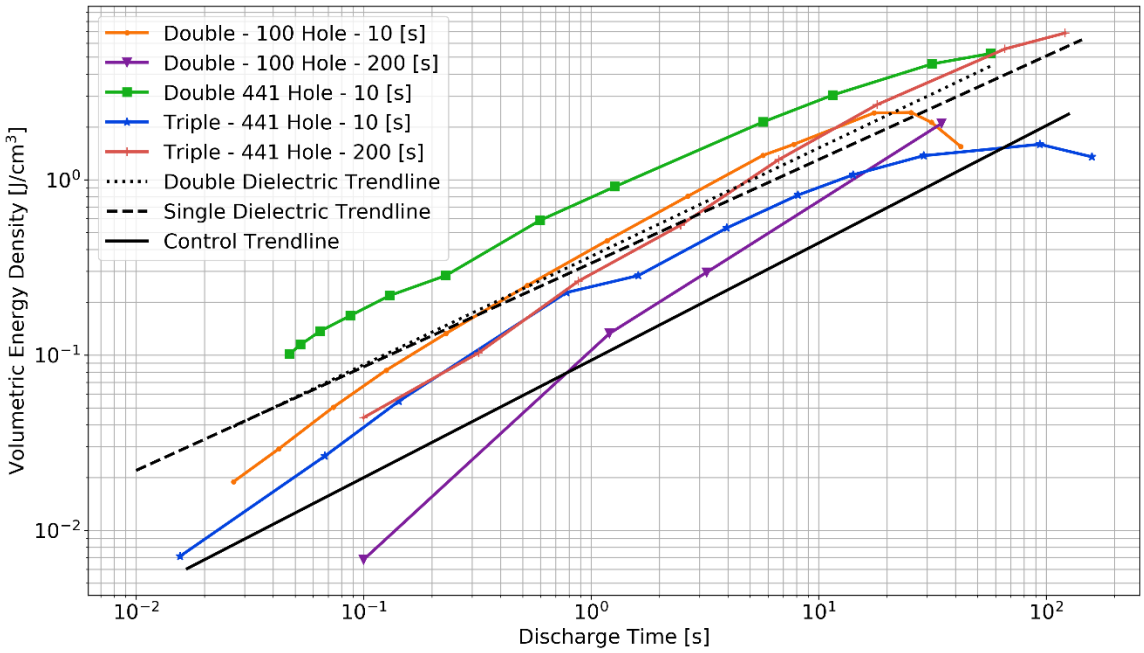


Figure 33. Volumetric Energy Density of Capacitors with Double and Triple Dielectric Layers of 100 and 441-Hole POA

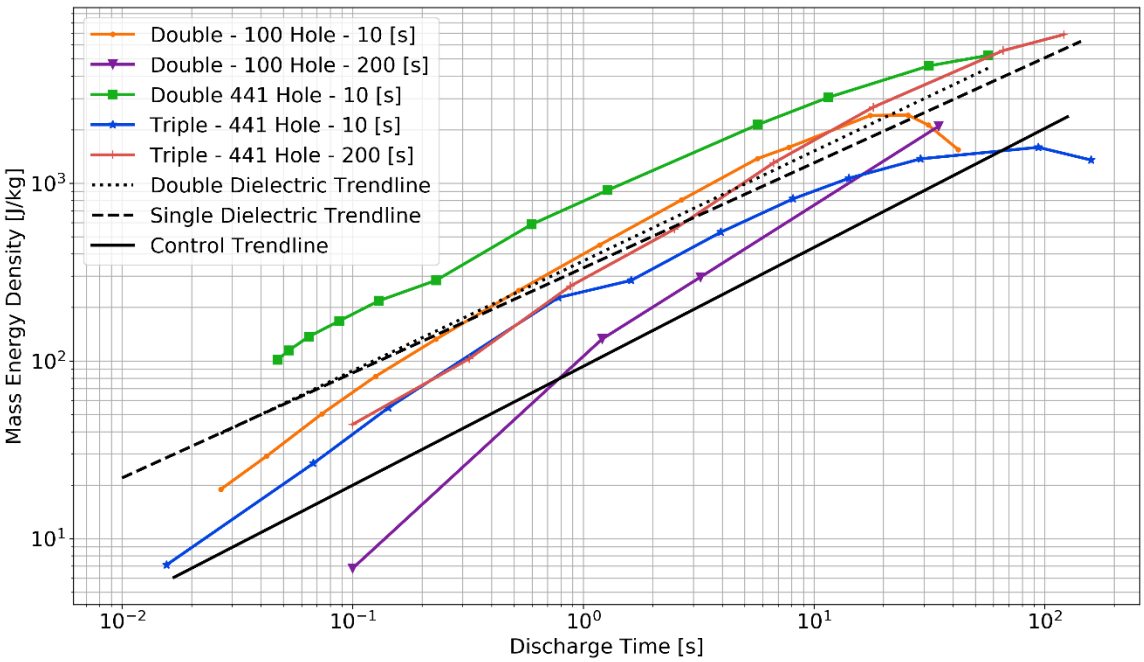


Figure 34. Mass Energy Density of Capacitors with Double and Triple Dielectric Layers of 100 and 441-Hole POA

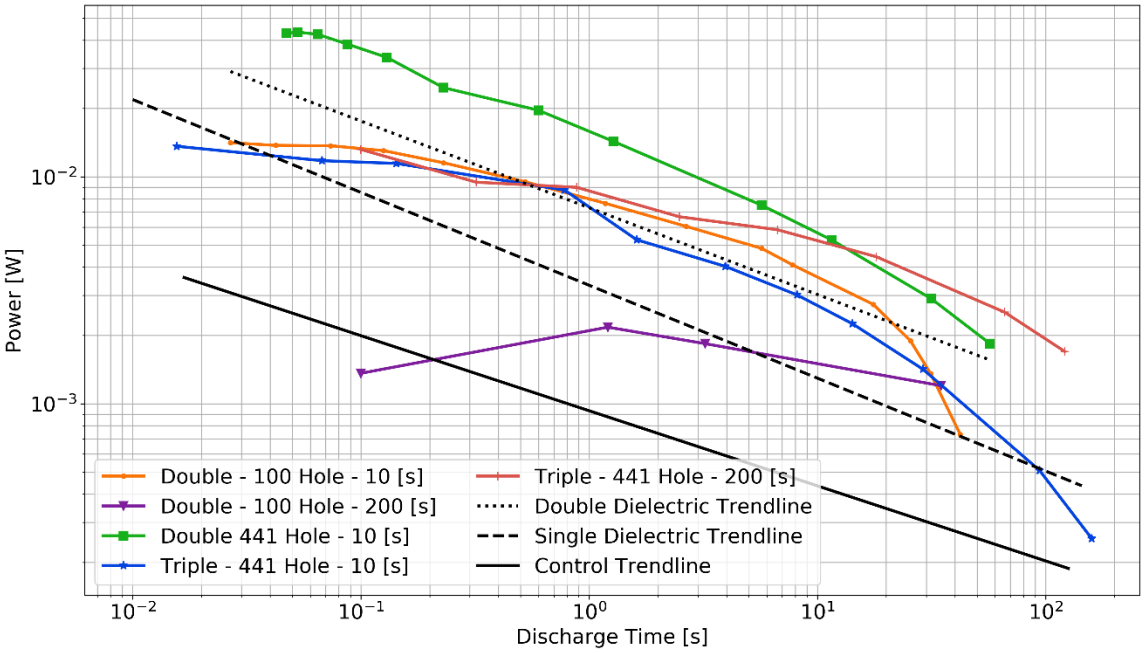


Figure 35. Total Power of Capacitors with Double and Triple Dielectric Layers of 100 and 441-Hole POA

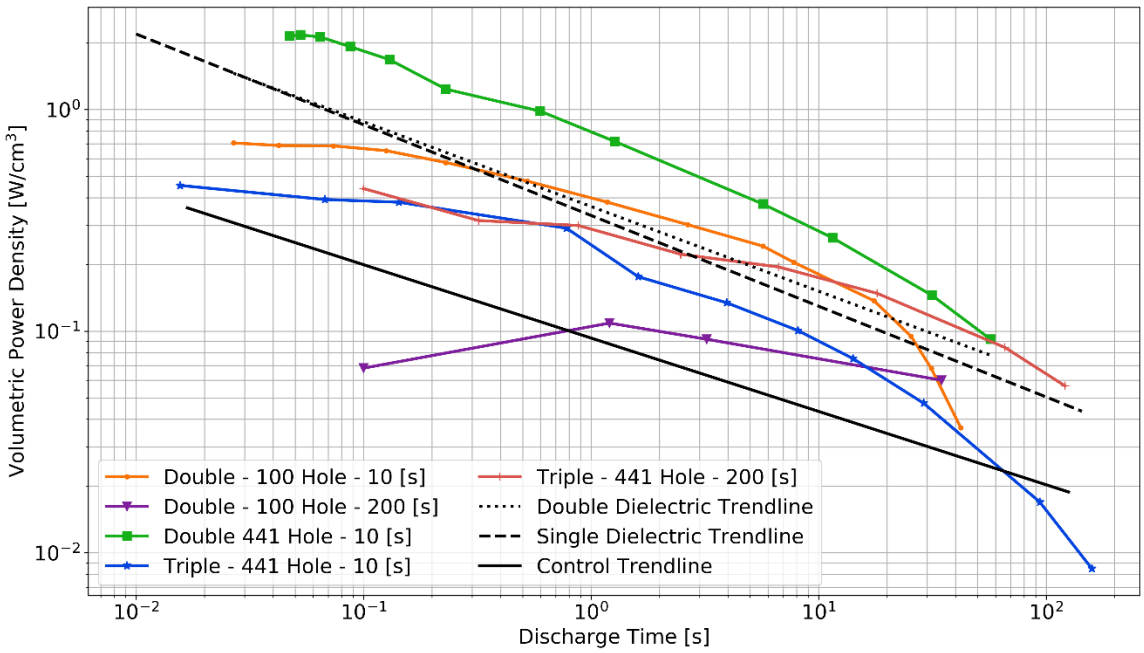


Figure 36. Volumetric Power Density of Capacitors with Double and Triple Dielectric Layers of 100 and 441-Hole POA

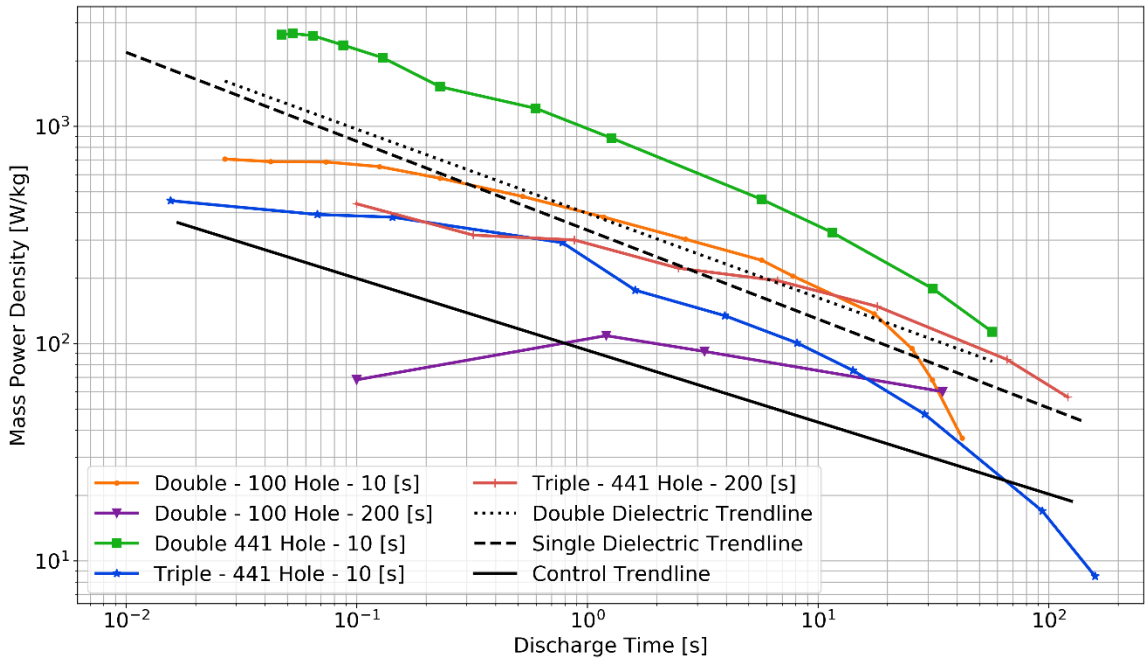


Figure 37. Mass Power Density of Capacitors with Double and Triple Dielectric Layers of 100 and 441-Hole POA

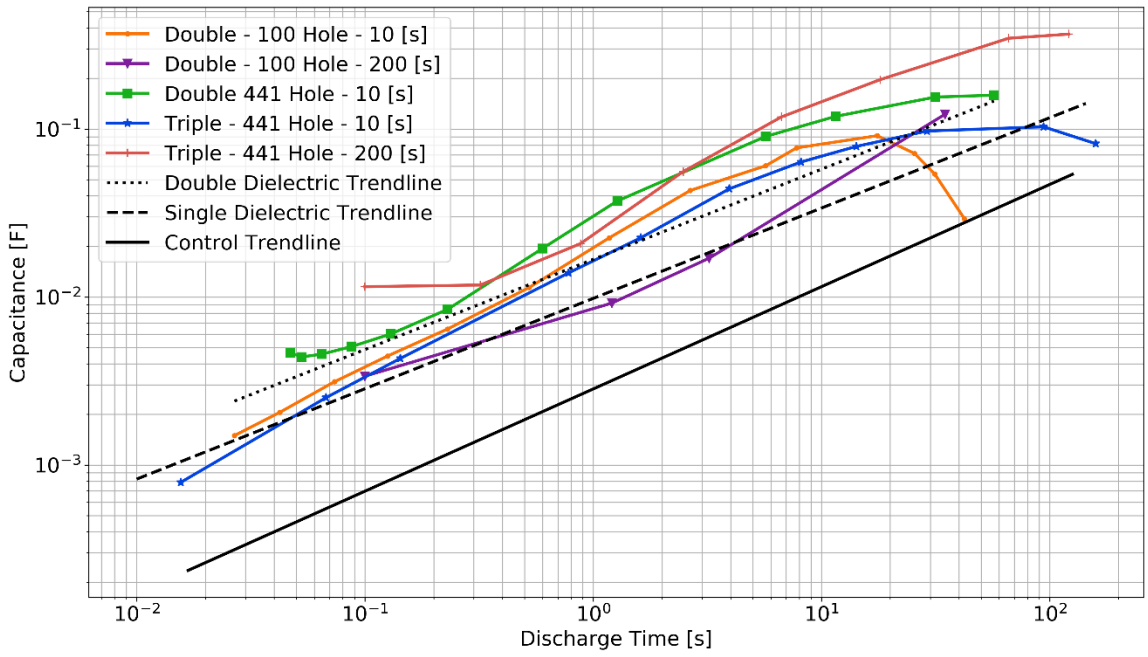


Figure 38. Capacitance of Capacitors with Double and Triple Dielectric Layers of 100 and 441-Hole POA

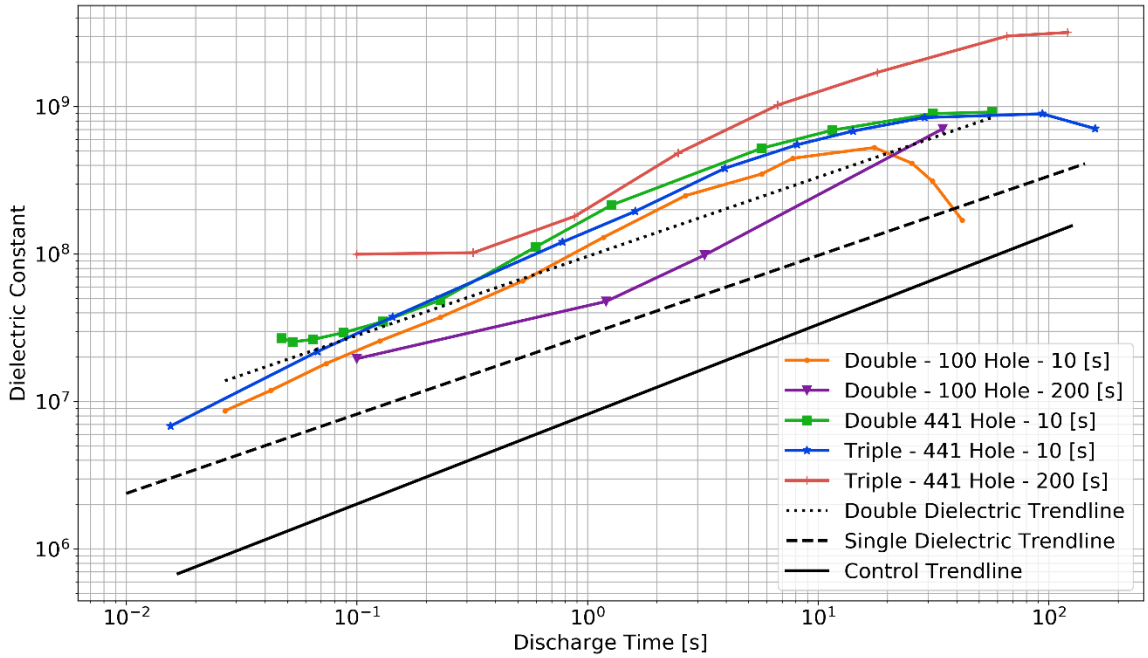


Figure 39. Dielectric Constant of Capacitors with Double and Triple Dielectric Layers of 100 and 441-Hole POA

IV. DISCUSSION

This study investigated the applicability of super dielectric material (SDM) theory to PL-SDM parallel plate capacitors, by testing several variants of PL-SDM structure and saturation designed to optimize capacitor performance. PL-SDM structure and saturation included: increasing POA number, increasing aligned-POA dielectric thickness, and varying saturation level of the dielectric layer(s) in KOH solution. The results show PL-SDM structure, constructed to increase dipole density (via an increase in POA number), and length (via an increase aligned-POA dielectric thickness), improves total energy and power, capacitance and dielectric constant. Total energy and power trends for double dielectric samples maintain a near proportional relationship to increased dielectric thickness. Correspondingly, volumetric and mass energy and power densities, which account for the designed increase in dielectric volume and mass, show a near constant curve between single and double dielectric trends. On the other hand, triple dielectric samples did not result in a proportional gain in energy and power, but did yield curves along the double dielectric trend lines. (This discussion is included below.) PL-SDM saturation, ranging in volume from 1 drop in the control group, and 6 drops of KOH solution in the experimental, to complete immersion in KOH solution for several seconds, produced negligible effect on capacitor performance. Thus, demonstrating that only a minimum volume of solution is required to achieve optimal performance. These results contradict the standard theory of energy storage where there is an inverse relationship between energy storage and dielectric thickness. It is shown that SDM theory is applicable to PL-SDM capacitor improvement. These main points along with other revelatory findings are discussed in further detail in the following sections.

A. PRIMARY HYPOTHESIS FINDINGS

1. Effect of Increasing POA

Performance curves for capacitors made with single and double dielectric layers of increasing 10, 100 and 441-hole POA show increasing performance as a function of increasing POA.

2. Effect of Aligned POA

Performance trends for double dielectric samples of combined POA show increasing total energy, total power, capacitance, and dielectric constants when compared to control trends, and single dielectric samples of combined POA. Energy and power density trends of double dielectric samples of combined POA are very similar to energy and power density trends of single dielectric samples of combined POA. The double dielectric samples exhibit an increase in total energy and power that scales proportionally to the doubled dielectric samples. Energy and power densities by definition are total energy and power values normalized by dielectric volume or mass, and scale proportionally to changes in dielectric thickness.

Triple dielectric samples of 441-hole POA did not produce the expected results of tripled performance, but fell in line with double dielectric performance trends. It is suspected that the construction method: stacking dielectric layers and adding drops of KOH solution between added layers did not effectively increase aligned-POA dielectric thickness for the purpose of increasing dipole length. The challenge of preventing slippage between dielectric layers and containment of solution within the POA contributed to this issue. As such, this method of increasing aligned-POA thickness is likely limited to just two layers or so. Consequently, triple dielectric samples did not triple dipole lengths, but instead produced dipole lengths similar to double dielectric dipole lengths, as shown in the performance curves.

3. Effect of Saturation Level

Saturation level did not have a significant influence on capacitor performance. Control and experimental samples that followed minimum and maximum saturation procedures did not produce significant differences in performance. Saturation level ranged from 1 drop of KOH solution in control samples, and 6 drops of KOH solution in experimental samples to immersing the Celgard matrix in KOH solution in both groups. The findings suggest that saturating the Celgard matrix in solution of the same ion density in varying degree did not improve performance. Therefore, meeting or exceeding some

minimum saturation level is likely of most importance to guarantying control and continuity of capacitor performance in this study.

4. Applicability of SDM Theory

In order to explain capacitor performance improvement as a function of POA, two theories were tested, accordingly. The first theory, derived from the parallel plate capacitor model, asserts capacitance is proportional to dielectric constant, electrode area, and inversely proportional to dielectric thickness. Therefore, an increase in capacitance can be achieved by an increase in electrode area (among a number of other methods). The second theory, SDM theory adapted from dielectric theory, asserts an increase in capacitance, as defined by the ratio between electrode charge and voltage, can be achieved by inserting polarizable media, specifically mobile ions supported by a solid matrix, between electrodes to effectively reduce the net electric field and voltage difference in order to increase capacitance [28].

Control samples made with single dielectrics sandwiched between two and six electrodes, and experimental samples made with single and double dielectrics of increasing POA sandwiched between two electrodes were tested. Control samples of standard (single) and tripled electrode thickness produced little difference in capacitance, and experimental samples of increasing POA showed improved capacitance curves. These findings do not support the standard model where capacitance is proportional to the total electrode area/volume/weight. The standard model is, also, of little avail to POA-based performance improvement. SDM theory, on the other hand, can provide insight into this observed dielectric behavior. In short, increasing POA hole number increases the number of areas in the SDM matrix where ions can form dipoles. In turn, the increase in dipole density increases the dipole-induced field strength, which leads to greater field minimization. Thus, the voltage difference between electrodes is further reduces, and capacitance increases as a function of POA.

Experimental samples made with double dielectric layers of increasing POA were also tested. Again, SDM theory, as opposed to the standard theory, was more applicable to the results obtained for double dielectric layers. Comparison of single and double dielectric

layers of 441-hole POA shows an improvement in capacitor performance (minus energy and power densities) as POA-aligned total dielectric thickness increased. According to the first theory, these findings are in contradiction to standard expectations of decreased capacitance and increased dielectric thickness. As previously noted, an increase in the number and length of dipoles enhances the field minimizing effect of the dipole-induced field. Thus, increasing POA-aligned total dielectric thickness by means of aligning multiple dielectric layers of the same POA number and pattern effectively lengthens the dipoles formed in the dielectric layer leading to an increase total energy storage.

5. Field Minimization

SDM theory addresses the underlying mechanism governing performance improvement in SDM-based capacitors. In effect, dielectric media sandwiched between electrodes of a given area and separation distance causes field minimization by forming dipoles through charge separation within the polarizable media. The summation of the two oppositely polarized fields, created by the electrodes and dielectric, leads to a reduction in the net field. Now that this model has been described and supported by the findings presented, it requires explanation with regard to field minimization in all of space leading to higher capacitance. Electric fields are conservative in nature, meaning the line integral of a particle traveling through an electric field along some curve of motion is path independent. In other words, the work to move a particle through an electric field depends only on the initial and final points. These properties do not change in the presence of a dielectric. Therefore, in order to preserve the conservative nature of an electric field, field reduction is not limited to the body of the dielectric but occurs everywhere [28]. Otherwise, the line integral of an electric field would be path dependent, as the work needed to move a particle between the same two points would depend on whether its trajectory was through or around the dielectric. Thus, it is necessary to reject the standard view of dielectrics where field minimization is limited to the body of the dielectric, and accept field minimization in all of space, in and around the dielectric layer, in order to retain path independence of a particle through a conservative vector field.

B. OTHER FINDINGS

1. CHD Protocol

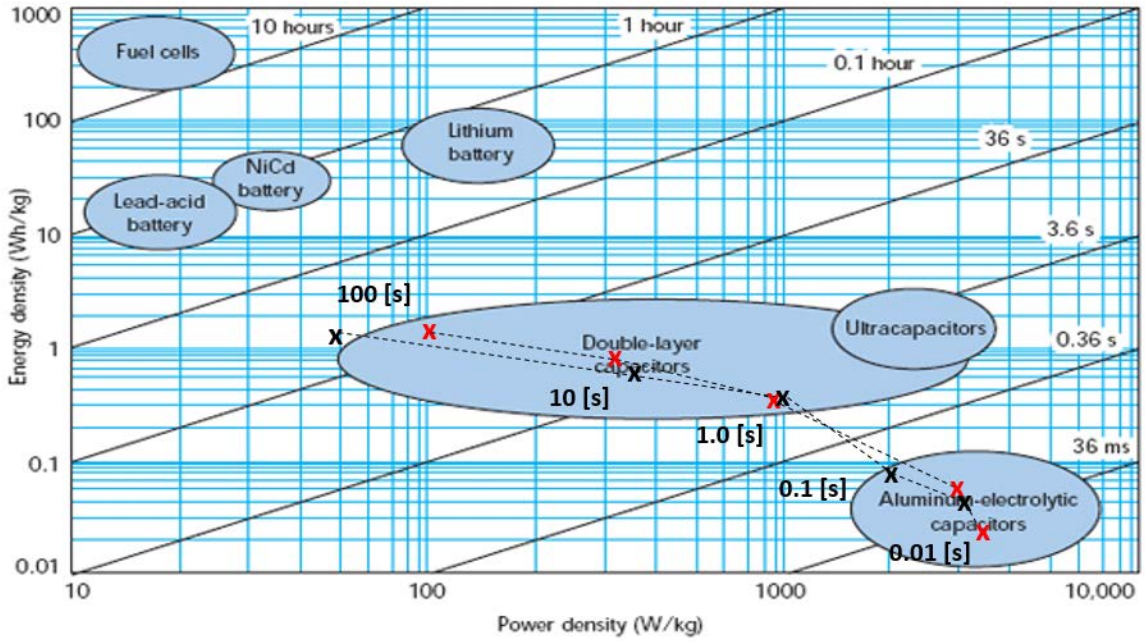
CHD protocol improves measured capacitance due the theory of dielectric improvement of capacitance [23]. In an SDM, the net length of the charge separation in the dielectric is a function of time. That is, it takes time for the minus charges to diffuse toward the positive electrode and the positively charge ions to diffuse toward the negatively charged electrode. Thus, the H step allows time for dipoles of maximum length to form, and concomitantly for capacitance to be maximized. Interestingly, CHD protocol did not have a predictable or notable effect on performance in this study. In fact, in several cases shorter constant voltage holds produced better capacitor performance curves. It is likely the constant hold durations of 10, 200, 400 and 600 [s] where excessive for the dielectric layer thicknesses studied. In addition to dipole formation in the POA of the dielectric layer(s), it is possible for dipoles to form in areas outside of the KOH-filled holes, that is between the Celgard material and electrodes creating a dipole strata of sorts. Dipoles forming between the compressed Celgard and electrode surfaces of less than $16x10^{-6}$ [m] (the thickness of a single dielectric layer) would require very short hold durations to achieve maximum ion separation. It is likely that the formation and contribution of dipoles is more complex than expected, but none-the-less its effects can be estimated using the equations put forth in Chapter 1.

2. Compressive Force

Compressive force, or the lack of compressive force exerted on capacitor components did little to influence the performance of single dielectric samples. Single dielectric samples of 441-hole POA without weight performed similarly to single dielectric samples of 441-POA with weight placed on the glass-capacitor-glass arrangement used during testing. Compression of the dielectric layer did not decrease the measured performance. Therefore, dipoles of maximum ion separation retained a length equivalent to the thickness of the $16x10^{\wedge-6}$ [mm] single dielectric layer.

3. Energy and Power Density

PL-SDM capacitor energy and power densities based on energy and power data of capacitors made with single and double dielectric layers of 441-hole POAs are displayed in Figure 40. These capacitors, as they are now, are comparable to the energy and power densities of commercial supercapacitors between discharge ranges of approximately 1 and 100 [s], but certainly would require intensive study to produce competent storage alternatives for implementation as energy magazines. Single and double dielectric energy and power density data produced roughly the same energy and power density relationship at equivalent discharge times due to a proportional increase in total energy resulting from increased dielectric thickness. Based on the findings, the energy and power density of single dielectric samples were improved by designing PL-SDM structure to increase dipole density.



The black and red markers are energy and power densities of single and double dielectric samples of 441 POA at discharge times closest to 0.01, 0.1, 1.0, 10, and 100 [s].

Figure 40. Energy and Power Density of PL-SDM Capacitors. Source: [17].

V. CONCLUSION

The sum of this work has led to a number of supporting concepts that underscore the applicability of SDM-based research to capacitor optimization. The PL-SDM parallel plate capacitor samples studied were comprised of single and multiple dielectric layers constructed of a solid Celgard support matrix of different POA saturated in ion dense KOH solution. The PL-SDM structure of each sample was varied in order to test capacitor performance as a function of POA hole number and aligned-POA dielectric thickness. The findings show that the PL-SDM structure, defined by increasing POA hole number and aligned-POA dielectric thickness, improved capacitor performance. These findings support dielectric theory and the assertion that the formation of dipoles within the dielectric acts to minimize the total electric field. Moreover, the form of the dielectric i.e., shape, size, appearance, and other physical parameters, can be designed to maximize dipole number and length in order to achieve optimal field minimization.

Design of the dielectric is key to SDM-based capacitor optimization. With this in mind, recommendations for further studies involve the modification of PL-SDM to enhance dipole formation by maximizing ion separation and dipole density. First, the use of viscous solutions or gels that support the migration of ions within the constraint of the SDM matrix would improve capacitor construction and testing. One of the major challenges of this research was testing the PL-SDM. The PL-SDM was inherently difficult to work with due to the aqueous solution and minimal containment area (POA of $16x10^{-6}$ [m] in thickness) residing within the Celgard matrix. As can be imagined, the KOH solution was difficult to contain within the boundaries of the POA. A viscous solution may also be practicable for testing dielectric improvement of capacitance via CHD protocol due to the slower formation of dipoles in viscous media. A recommendation regarding the support matrix itself, would be to design and construct an SDM variant that maximizes POA, or open areas for dipole formation, while minimizing the SDM matrix, in order to achieve capacitors of greater energy and power density. A potential design would involve the use of a highly porous sponge-like material capable of absorbing and retaining ion dense solution while providing the necessary internal framework for ion migration. In order to

address the issue of effective dielectric and open area thickness, construction of the SDM should employ a solid support matrix of the desired thickness and rigid open areas. Lastly, preliminary studies in the use of SDM on outer electrode surfaces shows promising results with regard to field minimization. This could be further explored to determine the advantages of constructing SDM-based capacitors in this fashion. In all, the work presented in this paper, along with future studies, will contribute to a small, but growing body of research at Naval Postgraduate School that shows SDM-based performance optimization is a novel and potential approach in addressing current capacitor limitations.

APPENDIX. MATLAB SCRIPT

```
clear all
clc
clf
format long

% PART 1. Read experimental data.

%   Description of variables:
%   raw_data = experimental time, current and voltage data from EC Lab
%   t = experimental time, [s]
%   I = experimental current, [mA]
%   V = experimental voltage, [V]

raw_data = xlsread('');
t = raw_data(:,);
V = raw_data(:,);
id1 = find(isnan(t));
id2 = find(isnan(V));

t([id1, id2]) = [];
V([id1, id2]) = [];

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%

%                   PARAMETERS used in test sequence(s).

% Description of variables:
% charge current, [mA]
% hold_time, [s]
% discharge current, [mA]

discharge_current = ;
c_v_h = ;
lower_bound_voltage = ;

%                       Capacitor geometry.

% Description of variables:
% area = area of electrodes [m^2]
% layers = seperator layers
% thickness = thickness of seperator [m^3]

                            area = 6.25e-4;
                            layers = ;
                            thickness = 16e-6;
                            volume = area*layers*thickness;
```

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%

% PART 2. Data Processing

    % a. Remove noise during hold periods.

    % This will aid in locating the start of each discharge leg.

    V(V>c_v_h)=c_v_h;

    % b. Find the start of the discharge legs.

        % i. Search for data points that meet discharge start
        % conditions.

        % The start of a discharge leg is located if the data point
meets
        % two conditions: 1) its equal to the upper bound voltage
        % or constant voltage hold value (these should be equal in
value),
        % and 2) if x consecutive data points to the right are not
equal
        % to the upper bound voltage or constant voltage hold value.

        V_start = zeros(1,11);
        t_start = zeros(1,11);
        for i=1:numel(V)-1
            if (V(i)==c_v_h) && (V(i+1)<c_v_h) && (V(i+2)<c_v_h) &&...
            (V(i+3)<c_v_h) && (V(i+4)<c_v_h) && (V(i+5)<c_v_h) &&...
            (V(i+6)<c_v_h) && (V(i+7)<c_v_h) && (V(i+8)<c_v_h) &&...
            (V(i+9)<c_v_h) && (V(i+10)<c_v_h) && (V(i+11)<c_v_h) &&...
            (V(i+12)<c_v_h) && (V(i+13)<c_v_h) && (V(i+14)<c_v_h) &&...
            (V(i+15)<c_v_h) %&& (V(i+16)<c_v_h) && (V(i+17)<c_v_h);
            V_start(i) = i;
            t_start(i) = i;
            end
        end

        % ii. Eliminate the data points that do not meet the
conditions.

        % Description of variables:
        % V_start = index in V array
        % t_start = index in t array

        V_start = V_start(V_start~=0);
        t_start = t_start(t_start~=0);

    % c. Find the end of the discharge legs.

        % i. Subtract all voltage data points from the lower bound
voltage
```

```
        % and sort all voltage differences as well as their associated
        % V array indices in order from lowest to highest voltage
        % difference.

        % Description of variables:
        % end_discharge = difference between voltage data point and
        %                 lower bound sorted by values closest to the
lower
        %                 bound
        % I = index of voltage data point sorted by values closest to
the
        %     lower bound

        [end_discharge,I] = sort(V-lower_bound_voltage);

        % ii. The first values in the sorted array found in part i) are
        % most likely to include the data points located at the end of
the
        % discharges (in a sequence). The end of the discharge legs are
        % located within this smaller data set if 1) the data
        % point is the very last data point in the voltage (V)
        % array (it gets assigned a variable name), 2) if the data
        % points are between the first, and second to last data points
in
        % the voltage (V) array, and the data points that have a
        % negative slope one data point to the left and have a positive
        % slope x data points to the right, 3) if the data point is the
        % second to last data point in the voltage (V) array (it gets
        % assigned a variable name).

        % Description of variables:

        % V_bitterend = voltage value of the very last data point
        % V_bitterend_I = index of the very last data point
        % t_bitterend = time value of the very last data point
        % t_bitterend_I = index of the very last data point

        % sleft = slope to the left of a data point
        % s1r,s2r,s3r... = slope to the right of a data point
        % V_end = voltage value at the end of a discharge
        % V_end_I = index
        % t_end = time value at the end of a discharge
        % t_end_I = index

        % V_last_discharge_end = voltage value of the second to last
data
        %                        point
        % V_last_discharge_end_I = index
        % t_last_discharge_end = time value of the second to last data
        %                        point
        % t_last_discharge_end_I = index

        V_end = zeros(100,1);
        V_end_I = zeros(100,1);
```

```
        t_end = zeros(100,1);
        t_end_I = zeros(100,1);

        for i = 1:100

            if (I(i) < numel(V)-7)
            a(i) = V(I(i)) - V(I(i)-1);
            b(i) = V(I(i)+1) - V(I(i));
            c(i) = V(I(i)+2) - V(I(i)+1);
            d(i) = V(I(i)+3) - V(I(i)+2);
            e(i) = V(I(i)+4) - V(I(i)+3);
            f(i) = V(I(i)+5) - V(I(i)+4);
            g(i) = V(I(i)+6) - V(I(i)+5);
            h(i) = V(I(i)+7) - V(I(i)+6);

            if (a(i) < 0) && (b(i) >= 0) && (c(i) >= 0) && (d(i) >=
0)...
                && (e(i) >= 0) && (f(i) >= 0) && (g(i) >= 0) && (h(i)
>= 0)
            V_end(i) = V(I(i));
            V_end_I(i) = I(i);
            t_end(i) = t(I(i));
            t_end_I(i) = I(i);
            end

            end

        end

        % iii. Eliminate all data points that do not meet the
conditions.

            V_end = V_end(V_end~=0);
            V_end_I = sort(V_end_I(V_end_I~=0));

            t_end = t_end(t_end~=0);
            t_end_I = sort(t_end_I(t_end_I~=0));

        % iv. Combine the voltage data into one array. The if statement
        % will determine if the very last data point or the second to
last
        % data point is the end of the last discharge. In some cases,
        % EC Lab Software will terminate the last cycle during
recharge.

            num = numel(V_end);

            for i = 1:num
                t_END(i) = t_end(i);
                t_END_I(i) = t_end_I(i);
                V_END(i)= V_end(i);
                V_END_I(i) = V_end_I(i);
            end
```

```
            for i=1:7
                I(i) = numel(V)-i;
                t_temp(i) = t(I(i));
                t_temp_I(i) = I(i);
                V_temp(i) = V(I(i));
                V_temp_I(i) = I(i);
            end

            [V_last,index] = min(V_temp);

            V_END(num+1) = V_last;
            V_END_I(num+1) = I(index);
            t_END(num+1) = t(I(index));
            t_END_I(num+1)= I(index);

% d. Plot the charge-hold-discharge curves and mark data points for the
% start and stop of each discharge leg. (This is a check to see if the
% correct discharge starts and ends were identified.)

figure(1)
plot(t, V)
hold on
plot(t(t_start(1:end)),V(V_start(1:end)),'g*');
hold on
plot(t(t_END_I(1:end)),V(V_END_I(1:end)),'r*');
hold off

% PART 3. Calculate values

%   a. Energy [J]

        % i.This uses the built-in matlab function trapz. The function
        % calculates the area below the discharge data points using the
        % trapeziodal method.

    for i=1:num+1
    X = t(t_start(i):t_END_I(i));
    Y = V(V_start(i):V_END_I(i));
    integral(i) = trapz(X,Y);
    end

    for i=1:num+1
    energy(i) = integral(i)*discharge_current*1e-3;
    vol_energy_density(i) = energy(i)/(volume*10^6); % [J/cm3]
    mass_energy_density(i) = energy(i)/(1000*volume); % [J/kg]
    end

%   b. Power [W]

    % i. This calculates the discharge time and power density.

    for i=1:num+1
```

```
    discharge_time(i) = t(t_END_I(i)) - t(t_start(i));
    end

    for i=1:num+1
    power(i) = energy(i)/discharge_time(i);
    power_density(i) = power(i)/volume;
    vol_power_density(i) = power_density(i)*10^-6; % [W/cm3]
    mass_power_density(i) = power(i)/(1000*volume); % [W/kg]
    end

%   c. Capacitance

%       i. This calculates slope during discharge between 0.8 and 0.1
[V]
%       using the linear least squares method.

%           a. Initialize a matrix of zeros for voltage and time data.
%           First determine the max length of data in a discharge leg,
and
%           create a matrix of size (max length x number of sequences).
%           Populate the matrix with the discharge data.

            len = zeros(num+1,1);
            for i=1:num+1
            len(i) = numel(V(V_start(i):V_END_I(i)));
            end

            max_V_cap =max(len);

            V_cap = zeros(max_V_cap,num+1);
            t_cap = zeros(max_V_cap,num+1);

            for i = 1:num+1
            V_cap(1:V_END_I(i)-V_start(i)+1,i) =
V(V_start(i):V_END_I(i));
            t_cap(1:V_END_I(i)-V_start(i)+1,i) =
t(t_start(i):t_END_I(i));
            end

%.          b. Determine the values closest to 0.8 and 0.1 [V] in each
%           discharge leg.

            for i=1:num+1
            [upper_bound(i),I_upper_bound(i)] = min(abs(V_cap(1:end,i)
-...
                0.8));
            [lower_bound(i),I_lower_bound(i)] = min(abs(V_cap(1:end,i)
-...
                0.1));
            end

%           c. Determine the slope for each discharge leg using linear
%           least squares method.
```

```
            for i=1:num+1
            time_data = [ones(numel(t_cap(I_upper_bound(i):...
                I_lower_bound(i),i)),1) t_cap(I_upper_bound(i):...
                I_lower_bound(i),i)];
            b = time_data\V_cap(I_upper_bound(i):I_lower_bound(i),i);
            yCalc = time_data*b;
            figure(2)
            plot(t_cap(I_upper_bound(i):I_lower_bound(i),i),yCalc);
            hold on
            slope(i)=b(2);
            end

            plot(t,V)
            hold on

for i=1:num+1
plot(t_cap(I_upper_bound(i),i),V_cap(I_upper_bound(i),i),'b*');
hold on
plot(t_cap(I_lower_bound(i),i),V_cap(I_lower_bound(i),i),'b*');
end
hold off

%           d. Calculate capacitance.

            for i=1:numel(slope)
                C(i) = abs(discharge_current*(10^-3)/(slope(i)));
            end

%           e. Calculate dielectric constant.

            for i=1:numel(C)
                dielectric(i) = C(i)*thickness*layers/(8.85e-12*area);
            end

%   d. Values for export.

    c1 = discharge_time';
    c2 = energy';
    c3 = vol_energy_density';
    c4 = mass_energy_density';
    c5 = power';
    c6 = vol_power_density';
    c7 = mass_power_density';
    c8 = C';
    c9 = dielectric';

    Values = [c1 c2 c3 c4 c5 c6 c7 c8 c9];
```

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