Steps Toward Computational Guided Deprocessing of Integrated Circuits

E.L. Principe
Synchrotron Research, Incorporated
Melbourne Beach, FL, USA
eprincipe@synchres.com

Robert Chivas, Michael DiBattista, Scott Silverman
Varioscale Incorporated
San Marcos, CA, USA

Navid Asadizanjani, Domenic Forte, Mark Tehranipoor
Florida Institute for Cybersecurity
University of Florida, Gainesville, FL, USA

Mike Marsh, Nicolas Piche
Object Research Systems,
Montreal, Canada

Abstract

We explore development of an extensible programmatic workflow combining automated adaptive CNC backside deprocessing with automated plasma FIB Gas-Assisted Delayering and montage SEM imaging. "Intelligent automation" is realized by bridging FIB-SEM instrument control with a "computational image processing engine" using a python scripting API. Tomographic reconstruction via automated back-side ultra-thinning coupled to automated gas-assisted plasma FIB delayering and automated SEM imaging is demonstrated for the first time. Further, we outline and promote development of an instrument control interface which permits secure rapid development of custom proprietary application specific modules without absolute reliance on OEM FIB-SEM hardware or software. Implementation of compressed sensing and dynamic stage scanning to allow arbitrarily large area delayering is also discussed.

Keywords *— Deprocessing, Integrated Circuits, Computational Guided Microscopy, tomography, plasma FIB, delayering*

I. INTRODUCTION

Deprocessing of ICs historically employs a variety of mechanical and chemical process tools in combination with one or more imaging modalities to reconstruct the IC architecture [1]. The typical deprocessing task extends from the centimeter to sub nanometer scale – over seven orders of magnitude in length scale. This panoscopic workflow requires the integration of a variety of repeated mechanical and/or chemical processes interleaved with a variety of data modalities which contribute layout data, structural data, chemical data and functional device data. A depiction of the traditional deprocessing workflow is illustrated in Fig1. A single monolithic tool which can accomplish the complete task of automatic deprocessing of an IC still does not exist, and practically may never be the most effective approach. Depending upon the technology and the objective of the analysis, a varying degree of mechanical deprocessing is required in addition to chemical processing which could involve reactive ion etching and/or wet chemical processing along with the image data.

In this work, we explore the development of an extensible programmatic workflow which can take advantage of evolving technologies in 2D/3D imaging, custom instrument control, image processing, as well as automated mechanical and chemical deprocessing technology.

Initial studies involved automated backside mechanical ultra-thinning of 65nm node 3.0 cm^2 Opteron IC processor chips in combination with automated montage SEM imaging and lab-based x-ray tomography and microanalysis. Static areas as large as 800umX800um were deprocessed using gas-assisted plasma FIB delayering on this device.

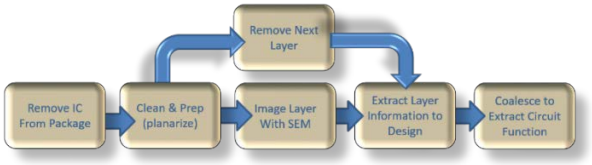

Fig. 1. Traditional deprocessing workflow based upon SEM imaging. Graphic adapted from David Weaver, et al., "Fast Mask Data Recovery to Provide Missing/Incomplete Technical Data Packages (TDP) for Obsolete ICs and Validating Trust Within ICs", GoMACTech 2011.

Later studies used smartcards as an archetype to further develop automated workflows. Smartcards represent a good architecture to discuss and develop deprocessing methods because they are as much as sixteen times smaller area than a $1cm^2$ processor and typically containing far few layers. Yet these small form factor embedded integrated circuits have rapidly become a widespread element of modern society and their security architecture represents an important problem. We demonstrate for the first time tomographic reconstruction based upon automated back-side ultra-thinning coupled to automated gas-assisted plasma FIB delayering.

Ultra-thinning the silicon substrate in the packaged device within 1-2um of the IC device significantly reduces the amount of time required for deprocessing. The computer aided backside ultra-thinning approach not only improves the success rate, as compared to manual techniques, it also allows the dense lower layers with smallest feature size to be imaged via high resolution SEM first, while the sample layers are the most uniform. Backside deprocessing has the additional

advantage that it can be possible to access the device while keeping it "alive" for in-situ electrical testing.

Common tool suites for deprocessing in a modern facility may combine x-ray tomography tools, mechanical delayering tools, chemical delayering tools, reactive ion etch tools, laser ablation systems, focused ion beam systems, IR imaging systems, electron beam based imaging systems and tools to determine elemental and chemical composition (i.e., EDS, ToF-SIMS). The overall process can be considered as an integration of sub-processes and subsystems.

More recently, with the advent of high current plasma FIB-SEM platforms with advanced Gas-Assisted Etch (GAE) chemistry; it has become more practical to perform large area delayering in-situ. This integration removes one iterative ex-situ step requiring mechanical planarization and cleaning. An instrument control interfaced based upon Python scripting allows rapid and customized automation of the FIB-SEM operations, including montage imaging and GAE delayering. This capability provides the end-user with a versatile programmatic functionality which reduces dependence upon vendor-specific software functions.

Likewise, the development of adaptive 5-axis CNC precision multi-tool grinding and polishing ushers a new level of capability and automation to IC deprocessing. The end result is an ability to perform automated backside deprocessing within 1-2um of the active area across a 25 mm x 25 mm die. To appreciate the importance of this technology, one must consider that neither a virgin packaged or extracted die is flat, but undergoes stresses and relaxation with an individual manufacturing and assembly history. As the silicon substrate is removed from the die during thinning steps, the stresses due to packaging and thick copper redistribution layers result in bending. Thus, this automated precision milling technology must actively measure both shape and thickness and dynamically adapt to the evolving surface profile while reaching a nominal 3nm RMS roughness.

A representation of this process is shown in Figure 2. The initial thickness of the device in package is 775um with a curvature that results in a measured sag of 180 um. When the process reaches its desires substrate thickness of 25um, the device has relaxed and the overall curvature of the device has reduced by nearly 55um to a measured sag of 125um.

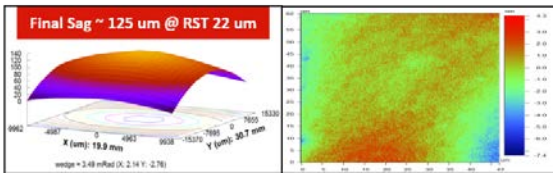

Fig. 2. The initial die is not flat and relaxes during thinning while polishing head adaptively tracks the surface (panel 1) thorugh final polish of <3nm RMS (panel 4).

The necessary key statistical data from grind and polish process steps from these advanced sample preparation tools can be fed forward to the API driving the automated plasma FIB-SEM. Such values include the remaining silicon thickness (RST) and optical measurements of die warpage at each physical location on the die. This data and the corresponding model of the substrate shape and residual silicon thickness provide guidance during delayering. Combining the evolution of automated plasma FIB-SEM platforms and automated backside milling technology enables a revision of the traditional delayering workflow, represented in Figure 3.

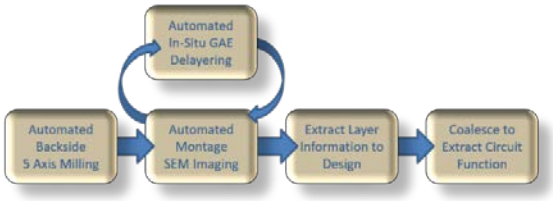

Fig. 3. A revised deprocessing workflow based upon the combination of automated backside ultra-thinning and automated plasma FIB-SEM delayering. Ultra-thinning may be performed with the chip without depackaging and frontside mechanical planarization.

The ability to perform ultra-thin automated backside preparation significantly reduces the effort as compared to frontside preparation and eliminates the typical requirement for mechanical polishing down to ~M5, prior to FIB-SEM delayering. Moreover, the sample is prepared for delayering at the highest density layer, where high resolution SEM imaging is most critical. The coupling of these two automated subsystems, involving ultra-thinning and large area plasma FIB-SEM delayering represents a step forward in the automation of IC deprocessing. Ongoing work involves enhancing the deprocessing workflow with "intelligent automation" by bridging FIB-SEM instrument control and near real-time data analysis to establish a computationally guided microscopy suite. A common python scripting API architecture between the FIB-SEM platform and the image processing and microanalysis platform permits rapid development of customized programmatic instrument control with data process integration and feedback.

II. Case Study: 65nm node Opteron IC delayering

An example of a 17mm x 18 mm die previously backside ultra-thinned by automated adaptive 5 axis CNC processing using a Varioscale VarioMill™ and inserted in a Tescan FERA plasma FIB, prior to in-situ large area delayering, is shown in Figure 4.

Initial backscatter electron (BSE) imaging at 30kV, prior to any delayering already reveals IC structure. Note the entire die while still in the package can be accommodated. In this case, no coating or other preparation was employed. The delayering process involves the use of a proprietary gas chemistry in conjunction with 15kV plasma FIB and a current density ranging from ~0.5-2.0pA/um^2. Typical GAE exposure times between imaging were 7-10 minutes per layer.

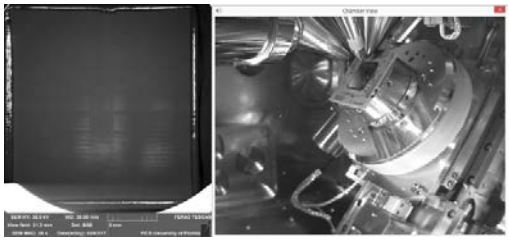

Fig. 4. At left is shown a SEM image of the entire die inside the plasma FIB. Note the IC structure is already visible in the lower right corner in the BSE image prior to any pFIB delayering. The panel at right shows the entire die and package mounted in the plasma FIB-SEM at the delayering position.

In Figure 5, a set of images are shown following removal of the first layer of residual silicon. The BSE image on the left is 5kV while the BSE image on the right, showing more detail of features at greater depth was acquired at 30kV. Both images represent a montage, each consisting of 49 images of 4096X4096 pixels. Each montage was acquired in either 26 minutes or 43 minutes, depending upon the programmer's choice of field of view (FOV) and pixel density.

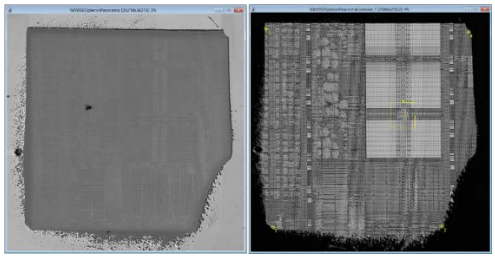

Fig. 5. Initial backside delayering to remove silicon. ~800x800um.

The BSE image at left was acquired at 5kV while the BSE image on the right was acquired at 30kV. The delayered area is approximately 800x800um. Each each shown is a montage consisting of 49 indivual images of 4096x4096 pixels each, acquired programmatically.

5kV BSE imaging following the initial removal of the residual silicon layer illustrates doping contrast, as shown in Figure 6. The panel at left shows the original montage, followed by two zoomed in regions and an inset panel in the upper right representing a cumulative horizontal profile trace defined by the region outlined in the first panel. The brighter and larger areas are the P-doped regions while the smaller and dimmer areas are the N-doped regions. This information is easily acquired from the thin silicon backside and enables the identification and placement of the NMOS and PMOS transistors during the circuit extraction function. This information has not been shown to be possible when the device is deprocessed from the frontside.

The process of sequential GAE delayering continues progressively moving through each layer, followed by automated imaging. There is full choice of the image conditions (voltage, detector, pixel density, field of view) for the montage operation. Typically, preset conditions are defined, saved and recalled programmatically by the operator. The choice of preset is based upon the optimal condition and virtually all relevant aspect of the electron column condition and other microscope parameters related to the presets are able to be saved and easily recalled through python scripting, on in the microscope GUI. Another set of 5kV/30kV images is shown in Figure 7, illustrating the gates highlighted at 5kV and looking into M1 at 30kV.

A final image pair from the Opteron case study is a montage acquired from the M1/M2 layer, shown in Figure 8. The 5kV BSE image data highlights the M1 metal layer while the 30kV BSE image montage is peaking through M2 and into M3.

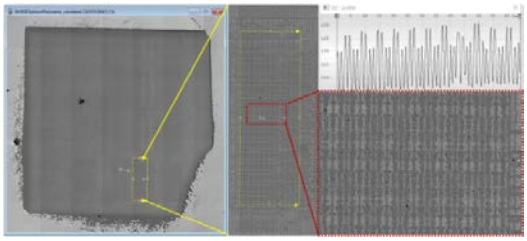

Fig. 6. 5kV BSE imaging of ~800x800um delayered area showing P and N doping contrast. Shown is a 49 image montage, each image consisting of 4096x4096 pixels.

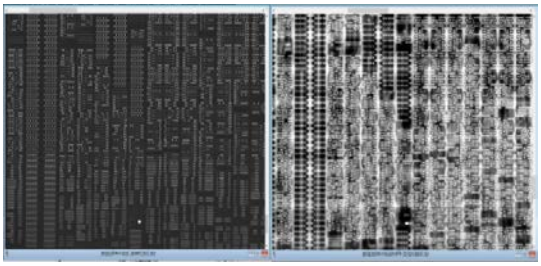

Fig. 7. Gate structures highlight at 5kV BSE, shown on the left and looking into M1 in the 30kV BSE image at right. Both images are a montage of 49 images @ 4096x4096 pixels each.

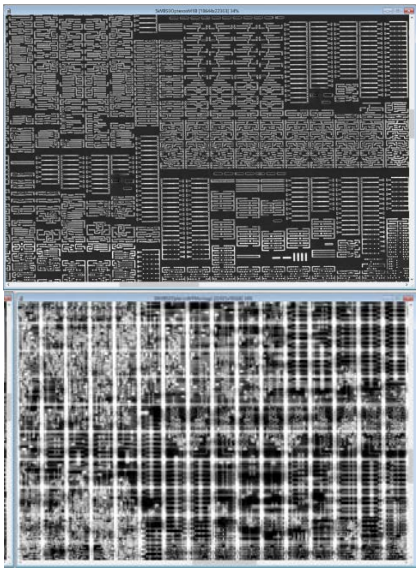

Fig. 8. Contact layer is prominent in the 5kV BSE montage image at top while the 30kV BSE image montage is looking into M2/M3 (bottom). Both images are a montage of 49 images @ 4096x4096 pixels each.

III. CASE STUDY: SMARTCARDS

A smart card (a.k.a., chip card) is any pocket-sized plastic card that contains embedded integrated circuits (ICs) for storing and transacting data. The ICs embedded in the card chip typically include a microprocessor, a crypto coprocessor, memory units, and I/O control units. Simple serial communication protocols, such as ISO7816, are typically used for data communication between card chip and terminal (or reader) [2]. The terminal is usually part of a computing system. Smart cards can be either contact or contactless. Smart cards provide personal identification, authentication, data storage, and application processing. Systems that are enhanced with smart cards are in use today throughout several key applications, including healthcare, banking, entertainment, and transportation. All applications benefit from the added features and security that smart cards provide [3-6]. For example, they may provide strong security authentication for single sign-on (SSO) [3] within large organizations.

By examining and taking apart the smart card chip, reverse engineering [7] can be exploited to figure out the internal structure and working principle, and further disclose sensitive information. In future work, we will use the proposed flow to fully RE different types of smart cards in order to understand the security primitives that maybe a candidate to be bypassed by an attacker to extract critical information. Once we know all the vulnerabilities we will look for possible solutions.

A. Automated Plasma FIB Delayering.

The first Smartcard type selected for the automated delayering testing is a microprocessor chip card from Almex Ltd. based upon Basic Card OS with 2k EEPROM and 3DES encryption [8]. The chip was depackaged by removing from the chip and mounting it on a metal backing with epoxy adhesive prior to the automated ultra-thinning process. Future work will apply CNC adaptive milling directly through the gold contact layer and mesh backing. This will also permit in-situ electrical testing.

In Figure 9 we show an overview image of the entire die acquired at 30kV and using BSE detection. Under these conditions the overall structure of the processor is evident. The approximately 400um X 400um in the lower right is the region of the die selected for initial testing of the automated plasma FIB delayering. The increased brightness is due to the initial manual thinning of the backside silicon to establish the starting point for the automated processing. The single crystal silicon typically mills very uniformly and progress can easily be monitored directly in the FIB image to determine when the device structure is exposed. In future, combining the API visualization engine, this process could also be fully automated to define the starting point for GAE plasma FIB automated delayering.

The 400um X 400um region was automatically delayered using GAE delayering chemistry in conjunction with the plasma FIB and automated montage imaging. The instrument and acquisition conditions used in for this result was 300nA@30kV and 400um FOV for the plasma FIB. The delayering cycle is programmatically set to seven minutes. The montage imaging conditions following each delayering cycle was 5kV with BSE detection using a retractable below the lens detector. The FOV for each montage tile was 100um at 4096 x 4096 pixels to generate a 5x5 image matrix. The dwell time per pixel was 1.5us. Following the acquisition of the 5kV montage, the process automatically collects a second montage using the similar image parameters, but at 30kV.

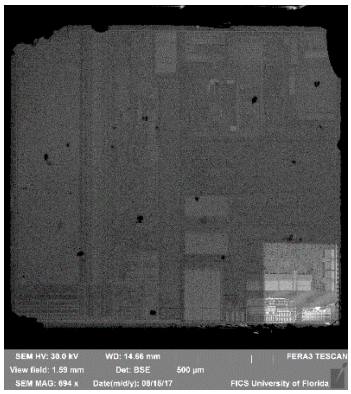

Fig. 9. 30kV BSE image depicting the entire Smartcard die structure following manual plasma FIB thinning in the lower right corner in preparation for automated plasma FIB delayering.

An API script guides the user through the five minute setup process using input prompts and both audio and onscreen printed instructions. A future version of the module will employ a compact GUI driven directly from the computational visualization engine.

The electron imaging conditions are defined by user preset and programmatically recalled through the API. The stage automatically increments in a serpentine fashion through the matrix using a pre-defined overlap (i.e., 10%) and a matrix size which depends upon the user selected FOV for the delayering area (i.e., 400um). Once all delayering and imaging cycles are complete, the system powers down the electron and ion columns. The process has run uninterrupted for up to 5 days.

A total of 25 automated delayering and image cycles were acquired from the die corner depicted in Fig 13 in the manner described above. An image pair from the beginning of the cycle is shown in Figure 10. The automated process initiated just beyond the transistor contact level. Similar to the previous series, the low kV image provides image data restricted to one layer in depth while the 30kV image data is convolved over ~3 layers. It required approximately 40 minutes to acquire both the 5kV and 30kV image matrices, a total of 50 images.

An image pair taken from the end of the data set cycle is shown in Figure 11. Finally, in Figure 12, we show what is believed to be the first tomographic data reconstruction based upon GAE plasma FIB delayering. The reconstruction is based upon the 25-layer data set taken at 5kV. But the reconstruction is just from a single montage tile, corresponding to row and column 1,2 in the 5x5 matrix. Work to complete a larger reconstruction from the complete montage is in progress. At this point, the process was concluded and another site was selected for study which yielded another 25 stack tomographic data set. Note, that is also interesting to consider the deconvolution of the 30kV in

combination with intermediate accelerating voltages to nondestructively extract tomographic data.

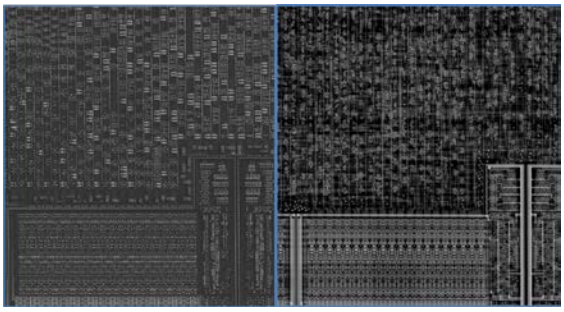

Fig. 10. Image pair from Layer 1 from a 25-layer auto delayer data set. The image at left is a 5kV BSE image and the image at right from the same nominal area is a 30kV BSE image. These images represent one tile in a 25-tile image matrix. Each image is 4096x4096 pixels and 1.5us dwell time.

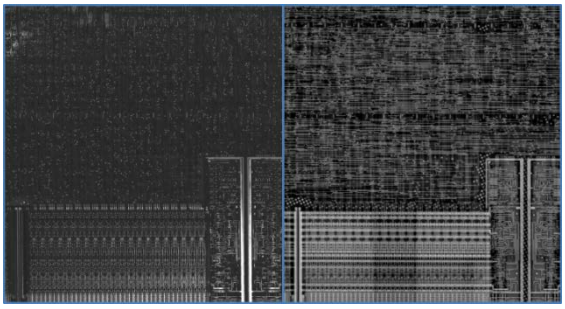

Fig. 11. A 5kV/30kV BSE image pair from Layer 25 from a 25-layer auto delayer data set. The same imaging conditions were used as described in Figure 10.

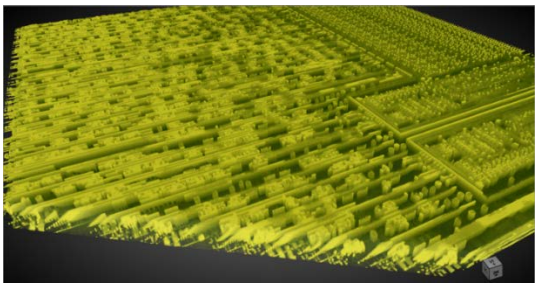

Fig. 12. Tomographic reconstruction obtained from a 25-layer automated GAE plasma FIB delayering process following automated mechanical adaptive CNC ultra-thinning to demonstrate an integrated automated workflow.

IV. Future Work: Automation of IC Deprocessing.

From this stage, the door opens to several extensions including the ability to automatically delayer multiple ROI in one session to cover an entire die. This process would combine raster scanning with stage scanning to step across a die. A combination of beam and stage scanning allows gas-assisted delayering to be processed over arbitrarily large areas. There are also opportunities to enhance speed, efficiency and reliability of the process by taking advantage of the feedback loop to the computational visualization and image processing engine. These intelligent automation processes include data validation of image data in near real-time, adaptive scanning strategies, gray scale milling and compressed sensing, to name a few.

A. Combining Beam Raster & Stage Scanning

The combination of beam scanning and stage scanning allows delayering schemes to be applied over arbitrarily large areas. Factors which limit the area which can be delayered in a plasma FIB in a single field include the minimum field of view, the gas uniformity and the concentration of the gas-assisted etch chemistry. Additional gas nozzles and gas concentrators may be employed to enlarge the uniform good area of the gas chemistry, but some stage scanning scheme will be required to cover even a moderately sized die.

The most straight forward scanning scheme is to employ a "checker board pattern" using at least two die and a suitable overlap to provide full coverage. This is currently possible. A more interesting scheme is to employ a continuous scanning strategy which permits uniform coverage over any prescribed area. When considering the scanning strategies for gas-assisted etching it is important to remember the scanning pattern is designed to provide uniform coverage as opposed to the restrictions of a line-by-line scan to acquire standard image data.

In order to evaluate various beam and stage scanning schema, we have developed a means to model and quantify ion or electron beam intensity coverage uniformity based upon relevant parameters including beam profile, beam step size, beam scan parameters, stage scan area, stage scan speed and stage scan pattern parameters.

An example output of the modeling is shown in Figure (13). Admittedly, an image depicting a uniform intensity distribution is inherently unexciting. We also are keeping details regarding the scanning schema employed proprietary at this time. The important point is we have a means to model, evaluate, and quantify both beam and stage scanning parameters prior to experimentation. Various schemas are currently in preparation for testing.

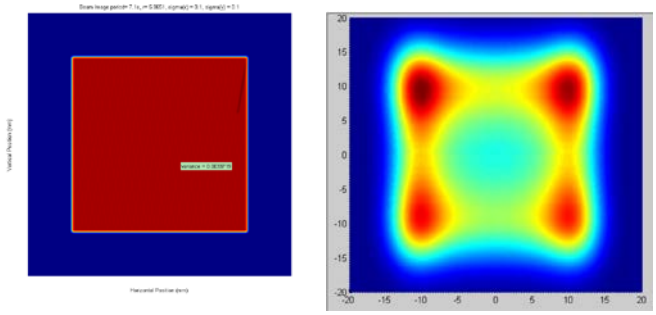

Fig. 13. Top: Modeling ion beam intensity uniformity using a combination of stage and beam scanning based upon 20x20mm stage scan and 100um2 tile areas. Right: example of poor uniformity coverage (15x15mm).

B. Compressed Sensing (CS)

Once an arbitrary sized area may be delayered in an automated fashion it is interesting to consider methods to enhance the imaging efficiency, and one such promising method is via compressed sensing. This field is expanding rapidly in the area of electron microscopy but early applications are currently restricted to dose reduction [9]. However, the challenges related to direct compressed sensing via continuous scanning techniques are well known [10]. One

of the authors (Principe) has previously explored and demonstrated methods to recover compressively sensed image data from delayered integrated circuits using theoretically modeled images [11]. An example is shown in Figure (14). CS may be applied quite effectively to IC circuits and may result in as much as a 5X increase in acquisition and would be a part of any adaptive scanning strategy within a computational guided deprocessing workflow.

Fig. 14. a) Intel Skylake 14nm processor delayered to M0 on a Plasma FIB. b) simulated image of a) with 20% of the scan data (5X faster!). c) Recovered image using Bayesian Process Factor Analysis.

Similar to the modelling applied to the beam and stage scanning described above, modelling has been applied to develop CS suitable for any electron microscope. Using proprietary methods developed by one of the authors (Principe), it is possible to perform compressed sensing acquisition with standard electron microscopes without special hardware, such as a fast beam blanker.

However, the application of these CS methods on an electron microscope requires a unique scan generator. The ideal scan generator for CS does not exist commercially and required specifications which both exceed and are differentiated from scan generators which are available from commercial vendors of electron and ion microscopes. The specifications have been created and a prototype designer has been identified. This CS project is currently seeking funding.

There is an additional benefit to the development of a stand-alone advanced scan generator of the type described above for compressed sensing, in conjunction with a general computational guided delayering tool based upon plasma FIB and electron imaging. A "CS scan generator" also provides an independent means to acquire and save image data and can be adapted to virtually any existing electron or FIB-SEM platform. Such interfaces are already available as a common interface for EDS vendors and other third-party equipment manufacturers. Common features include the ability to take both beam and stage control. This is essentially what is needed to adapt a CS scan generator for broad applications.

Acquiring and saving the CS image data through an independent CS scan generator which is coupled to a computational engine for automated delayering, in the manner demonstrated in this work, yields a powerful new paradigm for custom instrument control and rapid custom development.

Moreover, when one considers the limited hardware and software requirements to produce a plasma FIB-SEM platform which is *strictly and specifically designed and dedicated* to IC delayering, it becomes practical and economical to create a "ballroom" style IC deprocessing center which contains a suite of plasma FIB-SEM instruments coupled to programmatically extensible computational engines guiding the deprocessing, validating data, linking to image processing. It is quite feasible to integrate an electron column with a plasma FIB column with a number of stage options (laser scanning or not) into a basic vacuum chamber to produce a utilitarian plasma FIB deprocessing tool interfaced with an open source instrument control architecture. An example of an existing and eminently suitable open source instrument control architecture is EPICS (Experimental Physics Industrial Control System) [12]. This control system has extensive pre-existing control modules and broadly used throughout multiple industries, including world-wide in synchrotron communities. In this way a new paradigm is created unencumbered by the limitations of OEM vendors proprietary software and instrument control.

The next phase of our automation effort will combine the API functionality of the FIB-SEM platform and programmatically interface with the Object Research Systems (ORS) Dragonfly and Dragonfly python API [13]. In this way, a computational image processing and visualization engine is linked with the API control of the FIB-SEM and microanalysis platform.

For example, custom control modules and GUI control interfaces may be defined and operated directly within the ORS interface, as desired. Other image modalities may be easily added to the data structure, such as optical images or photoemission data. Collectively the data cube consisting of multiple image modalities form a local coordinate system which can be fed into and integrated with navigation in the FIB-SEM environment. Because Dragonfly (ORS) is not just the programmable platform for automated routines, but also a feature-rich interactive application, users can interactively monitor incoming images that are being aligned, stitched and composited in near real-time and also intervene during the execution of data collection. Users can perform near real-time measurements and data assessments that were not programmed a priori, and those results can be applied to direct subsequent steps in the deprocessing workflow.

Beyond collocating image and volume data, the interfacing of the APIs enables bi-directional processing and feedback, which is the most important element of this combination. The image processing engine can function as a distributed system coordinator, taking image data as it becomes available and performing any required distortion correction, segmentation, image stitching, montage display and visualization in near real-time. Image data may be validated and data acquisition schemes may be optimized based upon near real-time data analysis.

As an example of other possibilities, optical image data commonly provides a first level outline of the device which is useful to identify the location of memory arrays and other repeating block structures. Often, it is not necessary to SEM image each individual element of the array. The optical data, coordinated through the computational image processing engine (Dragonfly API) may direct the microscope to navigate to the block corners, refine the location of the block locations with the SEM imaging, and proceed to image selected cells at the required resolution, leaving the rest of the structure to be "filled in".

The processing may be carried further, by developing segmentation and extraction to GDSII within the same environment. There are existing software products which can accomplish reconstruction of the GDSII layout. Some are commercially available, such as Pix2Net [14] and others are internal non-commercial products, such as ARES [15]. One of the advantages of the schema being proposed here, is the open architecture and the utilization of pre-existing modules based upon Python scripting. This includes such modules as GDSPy (for GDSII creation) [16] and TomoPy [17]. Python is also easily extensible to multi-core processing and even adding multiple computer processing on-the-fly. The interface is not limited to Python scripts, but Matlab programming may also be called.

This element of the deprocessing workflow utilizes an image processing platform which also incorporates an open API for Python scripting. This API empowers not just feature extraction, image filtering, and reporting, but also 3D registration of images collected from a variety of data modalities comprised of different pixel sizes and spatial resolution into one common coordinate system for co-visualization and co-analysis of the multi-layer data set. Importantly, the end user is not limited by specific vendor software.

V. Conclusions

The coupling of plasma FIB-SEM deprocessing of devices with automated backside sample preparation using advanced adaptive computer guided backside milling provides additional key advantages in the deprocessing workflow [11]. This process enables greater success rate on lower metal interconnects and high-density transistor levels while accommodating non-planar device geometry on the sub-micron scale. Ultra-thinning in this manner significantly reduces the amount of time and manual expertise required while providing an excellent controlled starting surface for deprocessing [18], making it possible to access larger areas of the chip card to be de-processed with increased success rate, resolution and uniformity. Backside deprocessing also provides the potential to maintain a "live" device and conduct in-situ electrical testing.

We advance the processes previously developed by automation of imaging and plasma FIB deprocessing through open source custom instrument control via Python scripting. We have shown the ability to automatically perform multiple delayering and imaging cycles at multiple accelerating voltages over a user selected region of interest and user-defined inputs. We have also demonstrated, for the first time, that automated delayering performed in this controlled and repeatable manner is suitable for tomographic reconstruction.

We advocate for the development of a computationally guided microscopy workflow and platform which ideally incorporates a CS-scan generator with open instrument control architecture based upon EPICS. A variety of electron column, ion column and other hardware options are available to integrate into a platform that by design enables intelligent automation with near real-time feedback. Python scripting is, as of today, a preferred choice for many aspects of instrument control and large data processing due to broad adoption in science centers and ability to extend to multiple systems on-the-fly

Computationally guided microscopy, as currently being defined and developed here, holds the potential as a dynamic and extensible tool to adaptively acquire and analyze image data in near real-time and allow intelligent automation via interactive commands to the FIB-SEM platform to validate, as well as direct, data acquisition. Such an automated deprocessing tool can be used to reverse engineer integrated circuits and study vulnerabilities.

References

[1] M. Tehranipoor, "Physical Attacks and Tamper Resistance", ECE6095: Hardware Security & Trust University of Connecticut ECE Department

[2] Hocker III, L.O., Onset Computer Corporation, 1997. UART protocol that provides predictable delay for communication between computers of disparate ability. U.S. Patent 5,682,508.

[3] De Clercq, J., 2002. Single sign-on architectures. In Infrastructure Security (pp. 40-58). Springer Berlin Heidelberg.

[4] Smart Card Technology and Security. http://people.cs.uchicago.edu/~dinoj/smartcard/security.html

[5] Kocher, P., Jaffe, J. and Jun, B., 1999. Differential power analysis. In Advances in cryptology—CRYPTO'99 (pp. 789-789). Springer Berlin/Heidelberg.

[6] Dhem, J.F., Koeune, F., Leroux, P.A., Mestré, P., Quisquater, J.J. and Willems, J.L., 1998, September. A practical implementation of the timing attack. In International Conference on Smart Card Research and Advanced Applications (pp. 167-182). Springer Berlin Heidelberg.

[7] Kumagai, J., 2000. Chip detectives [reverse engineering]. IEEE Spectrum, 37(11), pp.43-48.

[8] https://secure.smartcardsource.com/zc314-basic-smart-card.html

[9] Andrew Stevens, Andrew, Hao Yang, Carin ,Lawrence, Arslan, Ilke, Browning, Nigel D., The potential for Bayesian compressive sensing to significantly reduce electron dose in high-resolution STEM images, Microscopy 0(0): 1–11 (2013)

[10] Anderson, Hyrum S., Ilic-Helms, Jovana, Rohrer, Brandon,Wheeler, Jason, Larson, Kurt, Sparse imaging for fast electron microscopy, Proc. SPIE 8657, Computational Imaging XI, 86570C (14 February 2013); doi: 10.1117/12.2008313; http://dx.doi.org/10.1117/12.2008313

[11] E. L. Principe et al, "Plasma FIB Deprocessing of Integrated Circuits from the Backside", FICS Research Annual Conference on Cybersecurity, March 7-8, 2017

[12] https://en.wikipedia.org/wiki/EPICS

[13] http://dev.theobjects.com/dragonfly_3_1_release/contents.html)

[14] http://micronetsol.net/

[15] https://www.blackhat.com/docs/us-15/materials/us-15-Thomas-Advanced-IC-Reverse-Engineering-Techniques-In-Depth-Analysis-Of-A-Modern-Smart-Card-wp.pdf.

[16] https://readthedocs.org/projects/gdspy/

[17] https://en.wikipedia.org/wiki/TomoPy

[18] R. Chivas et al., "Adaptive Grinding and Polishing of Silicon Integrated Circuits to Ultrathin Remaining Thickness" ISTFA 2015