

Heterogeneous Multi-Die High-Density Interconnect Stitching

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Abstract— A high-density and a highly scalable heterogeneous multi-die integration technology is presented in this paper. Central to this approach is the dense integration of heterogeneous ICs enabled by fine-pitch Compressible MicroInterconnects (CMIs) and stitch chips, which serve as the interface through which communication between active ICs occurs. A testbed is fabricated in order to characterize and demonstrate the proposed integration technology: concatenated assembly of chips using the stitch chips with fine-pitch CMIs (in-line pitch of 20 μm). Electrical characterization, including resistance and S-parameters, of the interconnects are reported as well as the assembly of testbeds. The measured results show robust and low-loss interconnections across multi-chips.

I. INTRODUCTION

IN the era of Artificial Intelligence (AI), cloud computing, Internet-of-Things (IoT), big data, and autonomous computing, there is a significant need for the seamless integration of heterogeneous multi-die in a small footprint with high-performance interconnects [1]-[4]. This need has been fulfilled until recently by integrating analog, digital, and limited sensor/MEMS functionalities into a monolithic System-on-Chip (SoC) architecture. However, the surging development costs and time associated with monolithic SoC design combined with the limited materials and heterogeneous devices that can be incorporated make monolithic processes limited. This has promoted significant research in several heterogeneous multi-die integration technologies by virtue of their integration flexibility and faster time-to-market. These technologies include silicon interposer [5]-[7], Embedded Multi-chip Interconnect Bridge (EMIB) technology [8], [9], and Silicon-Less Interconnect Technology (SLIT) [10]. However, while these approaches have clear advantages, they also have a number of challenges that may limit their utilization in multi-die microsystems. For example, silicon interposers require TSVs, which add cost, fabrication complexity, and are, in general, reticle size limited. Table I summarizes and compares key features of each of these heterogeneous multi-die integration technologies.

In this work, we propose a TSV-less heterogeneous integration technology, as illustrated in Fig. 1. Our approach seeks to form electrically concatenated ICs using

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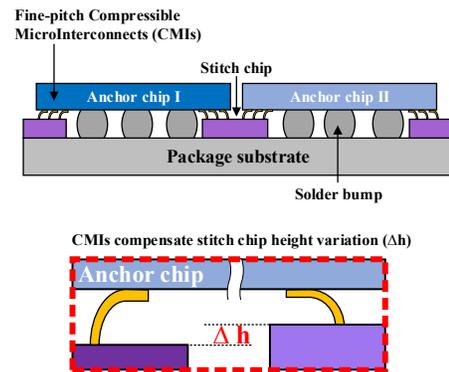


Fig. 1. Schematic of heterogeneous multi-die stitching technology enabled by fine-pitch I/Os.

heterogeneous IP blocks (from multiple foundries) enabled by 2.5D integration. To this end, we utilize a combination of solder bumps and mechanically-elastic and fine-pitch Compressible MicroInterconnects (CMIs) to robustly assemble the ICs. As shown in Fig. 1, the fine-pitch (as small as 20 μm) CMIs are used to provide the dense signaling pathways between the concatenated ‘anchor ICs’ through the stitch chips. The solder bumps with larger pitch and height are used for power delivery, signal routing between die and package, and mechanical interconnection between the anchor ICs and the package. The solder bumps also create the necessary force for the CMIs to form pressure-based reliable contacts. The stitch chips, which may contain high-quality passives and/or active circuits, in their simplest form contain only dense interconnects to interconnect nearby active anchor ICs. The anchor IC may be a logic, FPGA, MMIC, memory die (or stack), or photonic die, etc, for example. The advantages of CMIs in this heterogeneous multi-die integration approach are their ability to mechanically compensate for surface non-planarity from a substrate and stitch chip thickness variation, as a single anchor IC may be interfaced to multiple stitch chips with different thicknesses on all four edges. To be specific, the benefits of CMIs over conventional solder bump interconnects for multi-die heterogeneous integration are the following: a) CMIs are not susceptible to bump bridging [11], [12], which is a more prevalent issue as pitch is scaled down since they are pressure-based interconnects and do not reflow during the assembly

TABLE I. COMPARISON OF HETEROGENEOUS MULTI-DIE INTEGRATION SOLUTIONS

	(a) This work	(b) EMIB [8], [9]	(c) Silicon Interposer [5]-[7]	(d) SLIT [10]
Interconnect type	Compressible interconnect + Bumps	Bumps	Bumps + TSV	Bumps
Flexibility on surface/thickness variation	High	Low	Mid	Low
I/O pitch	20 μm	55 μm	30-60 μm	45 μm
System scalability	Scalable	Scalable	Limited	Limited
Agnostic to package substrate	Yes	No	-	-

process, b) owing to their mechanical flexibility, CMI can reduce the restrictions on stitch chip thickness variations and overcome surface non-planarity from an organic substrate, thus improving assembly yield and providing for unique integration options, and c) CMIs eliminate the need for strict uniformity control on microbump height. Since the proposed approach is not reticle-size limited as it is for silicon interposers and SLIT, it allows one to build highly scalable and dense electronic systems.

This paper is organized as follows: Section II describes the fabrication and assembly process of the proposed integration approach and shows images of the fabricated interconnects (solder bumps and CMIs) and the assembled testbeds. In Section III, the mechanical and electrical characteristics are measured, and Section IV concludes this paper.

II. FABRICATION AND ASSEMBLY

The overall heterogeneous interconnect stitching integration process flow is shown in Fig. 2. The integration process begins with fabricating solder bumps on the package substrate. Next, the stitch chips are assembled onto the package substrate. Lastly, the anchor dice with fine-pitch electroless gold plated NiW CMIs are flip-chip bonded onto the package substrate, as shown in Fig. 2. NiW is used for the CMIs due to its achievable yield strength (1.93 GPa); for reference, electroplated Cu, under specific plating conditions, has a reported yield strength of 136 MPa [13]. This high yield strength enables the CMI to tolerate more stress before experiencing plastic deformation during compression. The detailed fabrication process of CMIs is described in [14]. The experimental testbed is pursued in order to demonstrate the key features of the proposed heterogeneous interconnect stitching integration: assembly of chips with fine-pitch CMIs on a substrate containing stitch chips of different thicknesses and solder bumps.

In the testbed, a stitch chip on the package is emulated using a 20 μm tall step (though a larger step is possible) and the fine-pitch CMIs are fabricated on the assembled dice. The fabricated solder bumps are approximately 50 μm in height (in general, solder bumps with larger pitch can be made taller than 100 μm) and 200 μm in pitch while the lithographically defined CMIs are approximately 40 μm in height and formed on a 20 μm in-line pitch, as shown in Fig. 3. The fine-pitch CMIs provide higher I/O density for signaling between the anchor

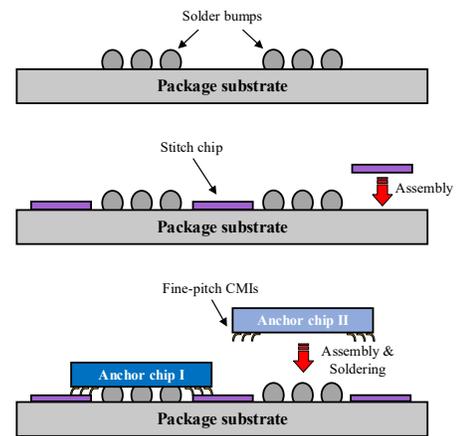


Fig. 2. The proposed integration process

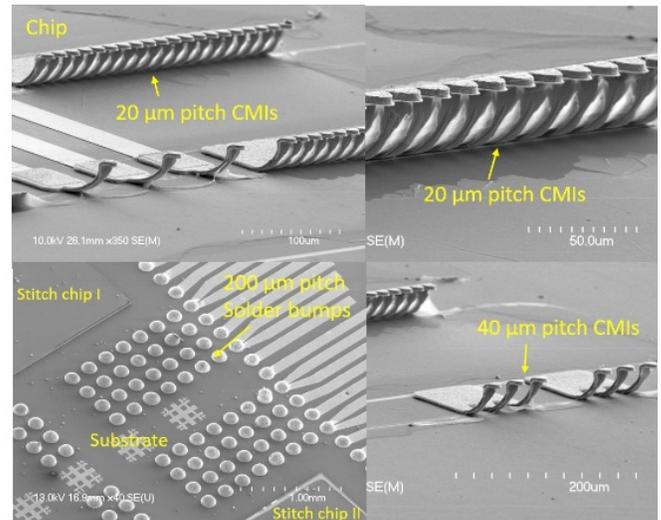


Fig. 3. SEM images of the solder bumps and fine-pitch CMIs on the substrate and chip, respectively.

dice connected through the stitch chips. An approximately tapered CMI design is adopted in order to distribute the stress along the body during deflection; this can increase the vertical elastic range of motion. The upward-curved CMI design

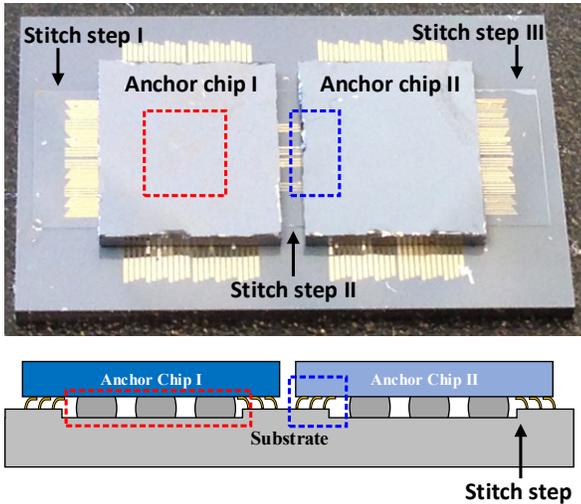


Fig. 4. Optical image and schematic of the assembled testbed

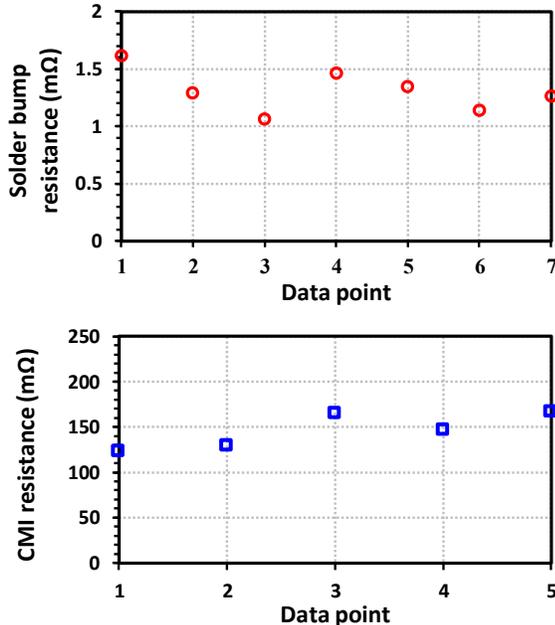
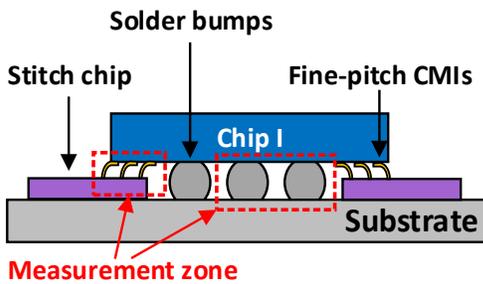


Fig. 5. Four-point resistance measurement results of the solder bumps and fine-pitch CMIIs.

ensures that the tip of the CMI remains in contact with the receiving pad during deflection (i.e., assembly).

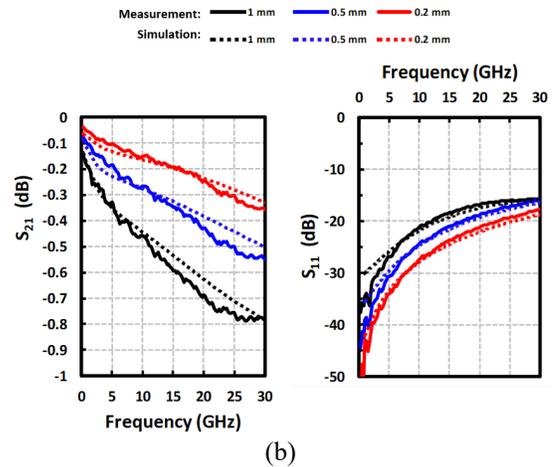
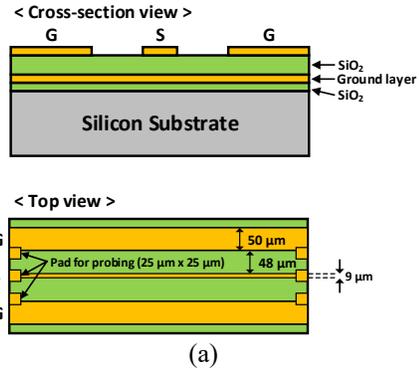


Fig. 6. Schematics of the via-free CBCPW (a) and measured S_{21} and S_{11} of the CBCPW for three wire lengths.

Optical and SEM cross-sectional images of the assembled testbed are shown in Fig. 4. The dice are assembled using a Finetech Fine placer Lambda flip-chip bonder. The two anchor dice in Fig. 4 are placed side-by-side onto the three stitch regions and the substrate. Once the dice are aligned to the substrate, the solder bumps are reflowed to provide electrical and mechanical interconnection to the substrate; the latter provides the needed force on the CMIIs for reliable interconnections. The center of the dice is bonded to the substrate using solder bumps, while two edges of the die are suspended above the silicon steps (i.e., the ‘stitch chips’) and supported by the fine-pitch CMIIs.

III. MEASUREMENTS

The four-point resistances of the interconnections after assembly were measured using a Karl-Suss probe station. Chips containing fine-pitch CMIIs were flip-chip bonded on to the substrate containing stitch chip and solder bumps, as shown in Fig. 5. The resistances of the CMIIs in contact with the gold traces on the stitch chips were measured. The solder bumps were reflowed after assembly and their four-point resistance measurements were also measured. As shown in Fig. 5, the average resistance of the CMIIs, including their contact resistance with the gold traces on the substrate, is 146.31 mΩ. The average resistance of the solder bumps is 1.31 mΩ. These four-point resistance measurement results confirm that the CMIIs maintain electrical connections between the die and the

stitch chips after they are compressed downward and form a pressure-based contact with the substrate. As noted earlier, owing to their mechanical flexibility, CMIs can compensate for any stitch-chip thickness variation or surface non-planarity of the substrate.

The RF performance of the stitch chip channels were experimentally measured by fabricating a low-loss via-free conductor backed coplanar waveguide (CBCPW) on a silicon substrate since the via-free CBCPW is simple to fabricate and has a higher cutoff frequency [15]. The measured S_{21} and S_{11} for TL lengths of 0.2 mm, 0.5 mm, and 1 mm are shown in Fig. 6. HFSS simulation results are compared with the measured results and show a good agreement. A clear trade-off between the loss and transmission line length can be observed. This motivates the need to assemble the anchors ICs with as small as gap between them as possible to minimize the interconnect length on the stitch chips.

IV. CONCLUSION

The fabrication and assembly process of a novel heterogeneous multi-die integration approach enabled by fine-pitch CMIs are presented in this paper. Electrical characterization, including resistance and S-parameters, of the interconnections through the stitch chips was performed, and measured results are presented to demonstrate early success. Four-point resistance measurement results for both solder bumps and fine-pitch CMIs show a robust signal routing between two anchor dice through stitch chips with low resistance variation. RF performance measurement results also show the need to minimize the interconnect length on the stitch chips. The approach is proposed to achieve dense signaling between ICs in addition to providing a highly scalable and flexible 2.5D heterogeneous IC integration solution that extends beyond the reticle limits of traditional multi-die integration solutions

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REFERENCES

- [1] A. Steegen, "Technology innovation in an IoT Era," in *Proc. IEEE VLSI Technol. Symp.*, Kyoto, Japan, 2015, pp. C170-C172.
- [2] J. Boeck, "IoT: the impact of things," in *Proc. IEEE VLSI Technol. Symp.*, Kyoto, Japan, 2015, pp. T82-T83.
- [3] M. Bohr, "The evolution of scaling from the homogeneous era to the heterogeneous era," *IEDM Tech. Dig.*, Dec. 2011, pp. 1.1.1-1.1.6.
- [4] G. Yeric, "Moore's law at 50: Are we planning for retirement?" *IEDM Tech. Dig.*, Dec. 2015, pp. 1.1.1-1.1.8.
- [5] G. Hellings, M. Scholz, M. Detalle, D. Velenis, M. de Potter de ten Broeck, C. Roda Neve, Y. Li, S. Van Huylenbroeck, S.-H. Chen, E.-J. Marinissen, A. La Manna, G. Van der Plas, D. Linten, E. Beyne, and A. Thean, "Active-lite interposer for 2.5 & 3D integration," in *Proc. IEEE VLSI Technol. Symp.*, Kyoto, Japan, 2015, pp. T222-T223.
- [6] N. Kim, D. Wu, D. Kim, A. Rahman, and P. Wu, "Interposer design optimization for high frequency signal transmission in passive and

- active interposer using through silicon via (TSV)," in *Proc. IEEE 61st Electron. Comp. and Technol. Conf.*, Lake Buena Vista, FL, 2011, pp. 1160-1167.
- [7] K. Saban, "Xilinx Stacked Silicon Interconnect Technology Delivers Breakthrough FPGA Capacity, Bandwidth, and Power Efficiency," Xilinx White paper: Vertex-7 FPGAs, Dec. 2012.
- [8] R. Mahajan, R. Sankman, N. Patel, D.-W. Kim, K. Aygun, Z. Qian, Y. Mekonnen, I. Salama, S. Sharan, D. Iyengar, and D. Mallik, "Embedded multi-die interconnect bridge (EMIB) -- a high density, high bandwidth packaging interconnect," in *Proc. IEEE 66th Electron. Comp. and Technol. Conf.*, Las Vegas, NV, 2016, pp. 557-565.
- [9] D. Greenhill, R. Ho, D. Lewis, H. Schmit, K. H. Chan, A. Tong, S. Atsatt, D. How, P. McElheny, K. Duwel, J. Schulz, D. Faulkner, G. Iyer, G. Chen, H. K. Phoon, H. W. Lim, W.-Y. Koay, and T. Garibay, "A 14nm 1GHz FPGA with 2.5D transceiver integration," in *Int. Solid-State Circuit Conf.*, San Francisco, CA, 2017, pp. 54-56.
- [10] W. S. Kwon, S. Ramalingam, X. Wu, L. Madden, C. Y. Huang, H. H. Chang, C. H. Chiu, S. Chiu, and S. Chen, "Cost effective and high performance 28nm FPGA with new disruptive Silicon-Less Interconnect Technology (SLIT)," *Int. Symp. Microelectronics*, San Diego, CA, 2014, pp. 599-605.
- [11] A. Yu, J. H. Lau, S. W. Ho, A. Kumar, W. Y. Hnin, D.-Q. Yu, M. C. Jong, V. Kripesh, D. Pinjala, and D.-L. Kwong, "Study of 15 μ m pitch solder microbumps for 3D IC integration," in *Proc. IEEE 59th Electron. Comp. and Technol. Conf.*, San Diego, CA, 2009, pp. 6-10.
- [12] J. Woertink, Y. Qin, J. Prange, P. L. Montesinos, I. Lee, Y.-H. Lee, M. Imanari, J. Dong, and J. Calvert, "From C4 to micro-bump: adapting lead free solder electroplating processes to next-gen advanced packaging applications," in *Proc. IEEE 64th Electron. Comp. and Technol. Conf.*, Orlando, FL, 2014, pp. 342-347.
- [13] E. Slavcheva, W. Mokwa, and U. Schnakenberg, "Electrodeposition and properties of NiW films for MEMS application," *Electrochim. Acta.*, vol. 50, no. 28, pp. 5573-5580, Sep. 2005.
- [14] P. K. Jo, M. Zia, J. L. Gonzalez, H. Oh, and M. S. Bakir, "Design, fabrication, and characterization of dense compressible microinterconnects," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 7, no. 7, pp. 1003-1010, May 2017.
- [15] M. Gibari, and H. Li, "A comparative study between via-hole and via-free grounded coplanar waveguide to microstrip transitions on thin polymer substrate," *Int. J. of Antennas and Propag.*, vol. 2015, p. 1-7, Dec. 2015.