Nanowatt Level Wake-up Receivers Using Co-Designed CMOS-MEMS Technologies

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***Abstract*—Event driven sensor nodes can spend the vast majority of their time in an asleep yet alert state that can dominate the total power budget when the node is heavily duty cycled. They thus require ultra-low power wakeup receivers that always stay on and that can detect wakeup events with high sensitivity. This paper presents a near-zero power, 8.3 nW wakeup receiver that combines the benefits of high quality factor aluminum nitride acoustic RF MEMS transformers with the complexity and sensitivity of 130nm CMOS chips including an envelope detector, comparator and low power clock to achieve -54dBm sensitivity at 457MHz.**

***Keywords*—microelectromechanical systems, CMOS integrated circuit, wireless sensor networks, wakeup receivers.**

I. Introduction

Event driven sensor nodes that spend the majority of their time in an asleep yet alert (AYA) state require ultra-low power (ULP) wakeup receivers that always stay on and that can detect wakeup events with high sensitivity. In cases of extreme duty cycling, such as in perimeter monitoring, the energy consumption of the wakeup receiver in its long AYA mode can dominate over the entire rest of the node in its relatively short active mode.

Fig. 1 shows the lifetime of a hypothetical sensing node versus its activity factor which is defined here as the number of wakeup events that occur in one hour [1]. The hypothetical node consists of a coin cell battery with the capacity of 195 mAh and self-leakage of 10 nA, a transmitter that consumes 1.35 mW and it turns on for 10 seconds after each event, and an ultra-low power wakeup receiver whose current is shown as I_{sleep}. This figure shows that we can achieve years longer lifetimes if we reduce the power consumption of the wakeup receiver down to the level of its battery self-leakage. Thus, the power of the wakeup receiver must be pushed down toward nanowatt level while maintaining acceptable sensitivity required for practical systems [2], [3].

State-of-the-art ultra-low power wakeup receivers [4] have utilized fully passive front-end architectures with zero power consumption. These systems rely on a large voltage boost that is provided by the lumped element matching network, matching the reference impedance to the high input impedance of the envelope detector. Since an inductor is an inherent element of these lumped element matching networks, it limits the overall size of the system and picks up a significant amount of ambient interference. In addition, inductors have limited quality factors for high frequency operation.

One very promising technological combination for achieving these required specs is to combine the low power detection and processing power of complementary metal-oxide-semiconductor (CMOS) electronics with microelectromechanical (MEMS) acoustic transformers that can provide high quality factor passive voltage gain at the input of the receiver. Furthermore, MEMS transformers provide robustness to ambient interference with small form factors and are shown to operate up to several gigahertz frequencies.

Various applications can benefit from sensing systems with extended lifetime. In general, as long as the argument for scarcity of the desired events holds true, they can fit within the application space aimed by this work. As an example, we can consider a ground sensor network for security purposes that is aimed at monitoring trespassers in an area. As shown in Fig. 1, a trespasser such as a truck can leave various signatures in the environment, such as emission of chemical exhaust gas, generation of heat due to fuel combustion, creating ground vibrations, or releasing acoustic waves due to the movement of mechanical parts in the engine. Therefore, a variety of sensing modalities can be implemented in each node for detecting these stimuli.

This paper will discuss the implementation of a wakeup receiver co-designed with both aluminum-nitride (AlN) based MEMS and CMOS electronics to take advantage of the best characteristics of both technologies, as shown in Fig. 2, whose front end transformer and envelope detector (ED) are discussed in further detail in [3].

II. System Design

The MEMS transformer is implemented using a suspended thin slab of AlN with 7 pairs of electrodes. It is combined with peripheral lumped elements that resonate out the input capacitance of the envelop detector while using the high quality factor of the MEMS stage to improve frequency selectivity. The photo of the MEMS device and transformer schematic are

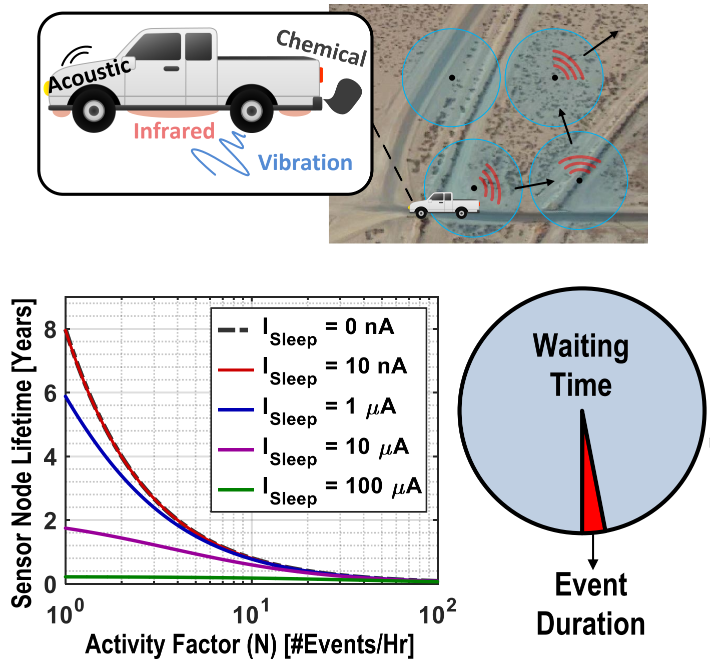

Fig. 1. Dependence of sensor lifetime on its sleep current which is determined by the power consumption of the wakeup receiver.

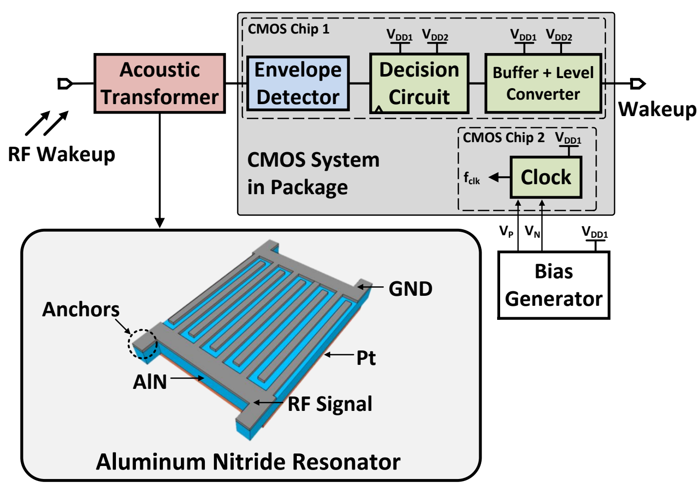

Fig. 2. 457 MHz wakeup receiver with AlN MEMS transformer and CMOS chips.

shown in Fig. 3 and the component values are given in Table I. The RF frequency of the transformer is currently limited by the discrete shunt inductance L_{tune}, and the AlN resonator has been demonstrated up to several gigahertz, but at a cost of lower passive voltage gain. For this demonstration it is tuned to 457 MHz.

The envelope detector, comparator, and clock are implemented in a standard 130nm CMOS process. The ED is a Dickson based square law rectifier (Fig. 4) [6]. There are

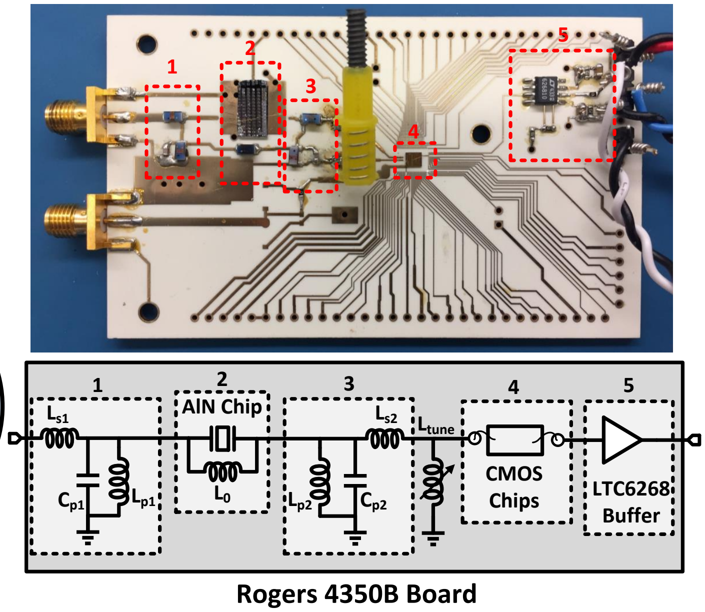

Fig. 3. Schematic of the input matching network (top), the AlN MEMs resonator (middle) and values for the peripheral devices in the matching network (bottom)

TABLE I
PARAMETERS WITH M-INDICES BELONG TO THE MEMS DEVICE MODIFIED BUTTERWORTH VAN DYKE MODEL. OTHER VALUES BELONG TO THE COMPONENTS SHOWN IN FIG. 3

$R_m(\Omega)$	38.8	$C_{p1}(pF)$	3	$C_{p2}(pF)$	3
$C_m(fF)$	8.24	$L_{s1}(nH)$	49.2	$L_{s2}(nH)$	49.2
$L_m(\mu H)$	14.7	$L_{p1}(nH)$	37.2	$L_{p2}(nH)$	14.5
$C_0(fF)$	532	$L_0(nH)$	214	$L_t(nH)$	≈90

several tradeoffs in the design of the rectifier to be considered. The metrics of importance are input impedance, which affects the achievable passive voltage gain of the transformer, voltage sensitivity, measured in $\mu v/(mv)^2$ due to the square law nature of the detector, detector noise, and response time [7]. The ED acts as a charge pump, that pushes current across the diodes as the input voltage goes positive or negative. This charge pump phenomenon can be represented at the baseband frequency as dc current sources with finite source resistance. At steady state, the current sources will charge up the voltage on the capacitors until the current through their source resistance exactly cancels out the current of the source itself. While operating in this regime the output voltage level is quadratically related to the input signal level due to the dominant second order nonlinearity of the detector diodes indicating that a doubling of input signal voltage creates a four times improvement in output signal level.

Two of the main design variables are device size and number of stages. While large devices will result in larger baseband current sources, they will have proportionally smaller source resistances, and thus voltage sensitivity is not affected much. Rather, larger devices allow for utilization of smaller number of stages in the detector enabling a faster device at the expense of voltage sensitivity. Similarly, smaller devices mean a larger number of stages which increases the overall sensitivity, but will slow down the response time and increase the input capacitance. Given these considerations, a 32 stage ED using zero threshold, thick gate oxide transistors as diodes was chosen for this design which provides a tradeoff between responsivity and response speed. Where a larger responsivity allows for greater sensitivity from the front end, while lower response speeds enables higher data rate communication.

In addition, since the ED is the major bottleneck for determining the speed and therefore latency of the receiver, it is desirable to improve its response time as much as possible. In order to achieve this goal, the coupling capacitors are designed to have larger values towards the input stages and smaller values towards the output stages. The reason for this design strategy is that from a circuit theory standpoint, the latter nodes in the chain have a larger shunt resistance to ground and therefore are slower. This means that if we load all the nodes in the rectifier chain with similar capacitors, the latter nodes will have greater time constants. Therefore the capacitors are stepped to minimize the charge time of the ED. In general, using smaller capacitors helps to reduce the overall input capacitance which enables the ED to achieve a higher output dc voltage by reducing the capacitive loading of the MEMS device.

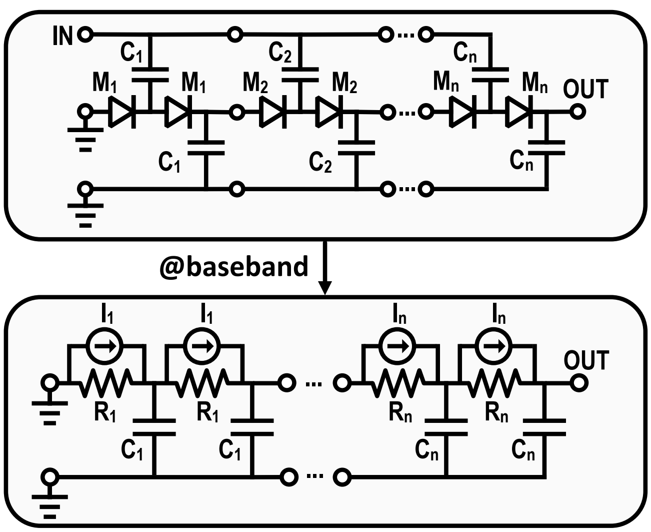

Fig. 4. Dickson based envelope detector, and its baseband charge-pump model.

Fig. 6 shows the schematic of the clocked comparator. It has a preamplifier that is implemented as a differential pair with digitally controlled weights. Where the input reffered offset of this preamplifier is controlled via a digitally weighted DAC current source attached to the reference input of the amplifier. This Input offset and the input signal from the rectifier are compared and the difference is amplified by both the preamplifier and the regenerative latch. The bias current for the regenerative latch is supplied with a DAC current source where the bias current sets the slew rate of the latch. This signal is then fed through a buffer chain which provides additional gain ensuring the output signal is rail to rail before it is captured by an output flip-flop. When the clock is low, the preamplifier is enabled, and then its value is latched in on the rising edge of the clock. Due to the head room requirements for the latch circuit and the input preamplifier the core comparator circuit requires a higher operating voltage than the digital latch which are set at 1.0 V and 0.65 V respectively.

The clock is implemented as a five stage current starved ring oscillator for minimum power consumption [6]. The operation frequency is controllable via two off-chip bias voltages enabling operation from 100 Hz to 100 kHz with a dc power consumption of <1 nW at a 1 kHz clock frequency from a 1V supply. The measurements of the clock chip are shown in Fig. 5.

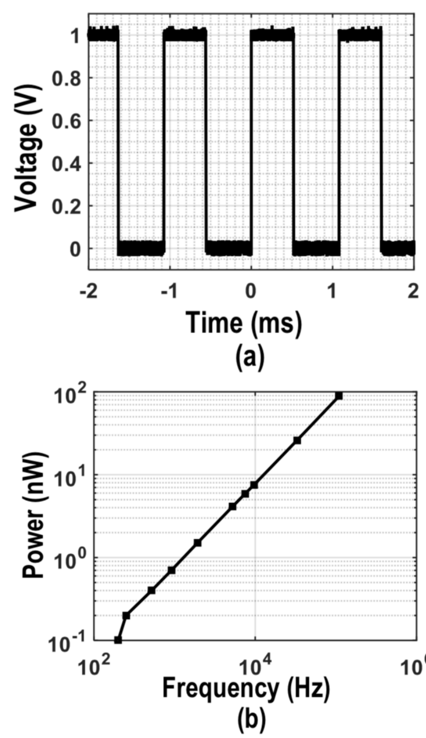

Fig. 5. Measured output waveform of the clock (a), and power vs frequency as current is swept (b).

The overall sensitivity of this system is threshold voltage limited where the envelope detector cannot provide sufficient output signal levels to trip the comparator due to process limitations in the comparator . While operating in this regime either a direct increase in the detector responsivity or an decrease in the minimum input referred offset of the comparator can provide higher levels of RF sensitivity.

The system measurement setup and die photos of the CMOS chips are shown in Fig. 7. The system's performance is

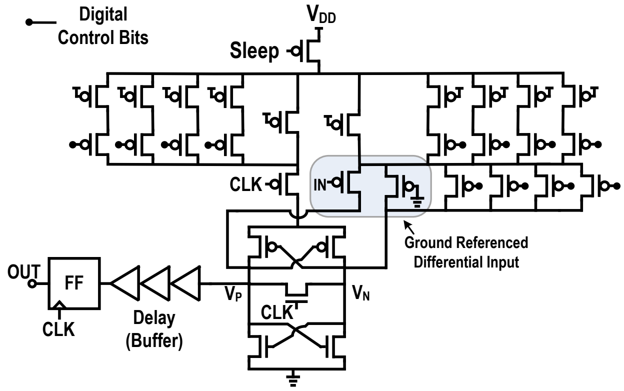

Fig. 6. Schematic of clocked comparator with digitally controlled offset enabled through a current mode digital to analog converter.

characterized using a modified receiver operating curve plot to highlight the metrics of interest for wakeup receivers, namely, the probability that the receiver will detect an incoming wakeup signal at a certain power level, and the number of false positive wakeups per hour that would cause the receiver to unnecessarily wake up the rest of the sensor node, and is shown in Fig. 8. The receiver has $> 99.9\%$ detection with -54 dBm at 457 MHz and $> 60\%$ detection with -56 dBm while maintaining low false positive rates. It consumes 8.3 nW dc power from 0.65 V and 1 V supplies. The probability of detection and the false positive rate can be improved through the use of low power correlator circuitry that can also provide wakeup discrimination of numerous nodes.

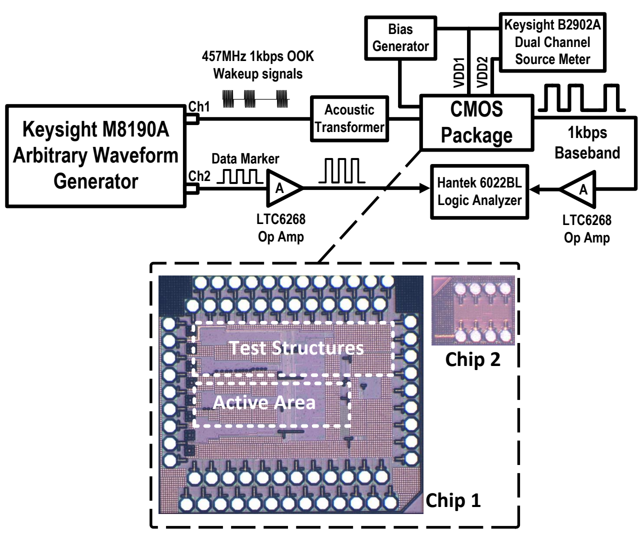

Fig. 7. Measurement setup of the wakeup receiver for 457 MHz 1kbps OOK signal and die photos of the CMOS chips.

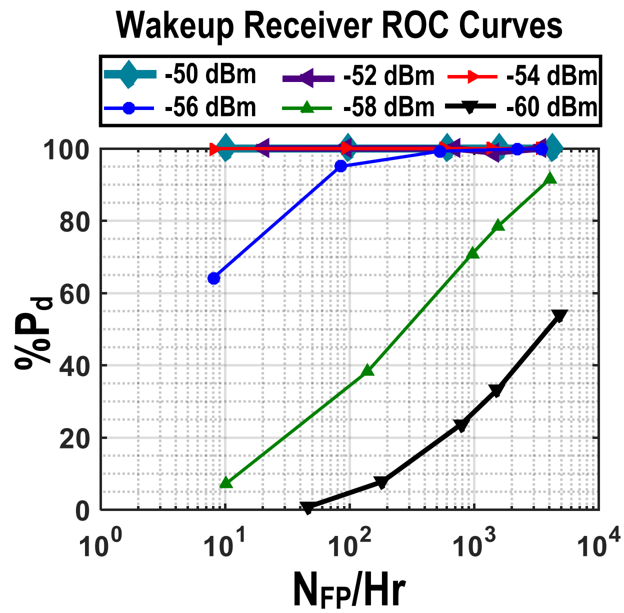

Fig. 8. System results showing perfect detection at -54 dBm sensitivity at 457 MHz.

III. Conclusion

This work demonstrated a hybrid MEMS-CMOS wakeup receiver for event driven applications. The acoustic input impedance transformer, implemented with an aluminum nitride resonator and discrete components provides passive voltage amplification going into the envelope detector and comparator decision circuit. It is capable of achieving sensitivities of -54 dBm at 457 MHz.

Acknowledgment

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