A 5nW Wake-Up Receiver With Better Than -63dBm Sensitivity via an Active Pseudo-Differential Envelope Detector

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***Abstract*—A 402-405 MHz MICS-band wake-up receiver is presented that achieves −63.8 dBm sensitivity at 4.5 nW. High sensitivity at 400 MHz is accomplished via an 18.5 dB passive voltage gain transformer filter loaded by a high input impedance ($R_{in} > 30$ kΩ), high scaling factor ($k_{ED} > 300$), 1.8 nW current re-use pseudo-balun envelope detector, while low power is achieved by operating all active circuits, including the re-generative comparator, baseband correlator, and temperature compensated relaxation oscillator in sub-threshold with a single 0.4 V supply. The chip is fabricated using 0.18 μm CMOS SOI process and achieves the highest figure of merit of all direct envelope detection-based wake-up receivers operating above 400 MHz.**

***Keywords*—LPWAN; wake-up receiver; low power; wireless**

I. Introduction

Wake-up receivers (WuRXs), used to continuously monitor the RF environment for infrequent event-driven wake-up signals, can replace the need for energy-expensive synchronization routines frequently required in conventional radio networks. WuRXs at nW power levels have been reported [1]–[3], however with moderate sensitivity. When used in low average-throughput applications (e.g., wearable temperature sensors or environmental monitors), wake-up latency, and therefore data rate, can be relaxed. Prior work has exploited such requirements to design low-bandwidth, and therefore low-noise, on-off keying (OOK) WuRXs that, along with a passive RF gain transformer filter, achieved excellent sensitivity at nW power levels [4]. However, this prior work was limited to 113.5 MHz, largely because of the low input impedance of the envelope detector (ED). While a low carrier frequency may be suitable for some applications, such as unattended ground sensor networks, it is not practical for many wearable and IoT applications. To enable operation at higher frequencies without significantly compromising sensitivity or power consumption, this paper presents the design of a WuRX featuring an active pseudo-balun ED. This new ED has higher input resistance, lower input capacitance, and higher conversion gain via a current re-use common gate (CG) architecture facilitating the design of a high passive gain RF transformer filter at 400 MHz.

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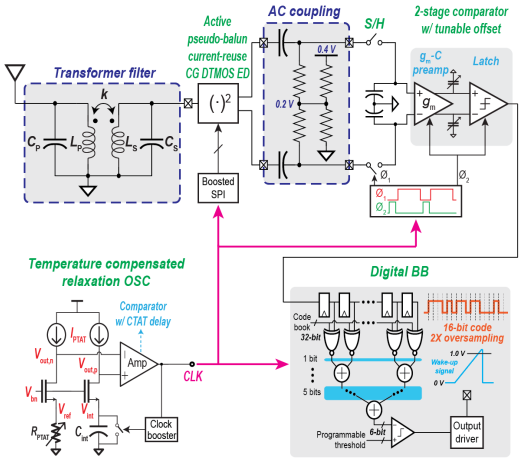

Fig. 1. Block diagram of proposed 402-405 MHz MICS band WuRX.

II. System and Circuits Implementation

The WuRX system architecture is shown in Fig. 1. To eliminate the power hungry local oscillator (LO) in conventional radios, a direct envelope detection architecture was chosen where the RF signal is directly demodulated via the 2^{nd} order non-linearity of the ED. In this section, we present the working principle of each circuit block and techniques to achieve high sensitivity at 400 MHz without sacrificing the power consumption.

A. Transformer & Pseudo-Balun Envelope Detector

To improve the sensitivity and interferer rejection of the WuRX, a 400 MHz high-Q transformer was designed. Both the primary and secondary stages resonate at the same center frequency, providing filtering and performing the impedance transformation, which results in a passive voltage gain, $A_V =$

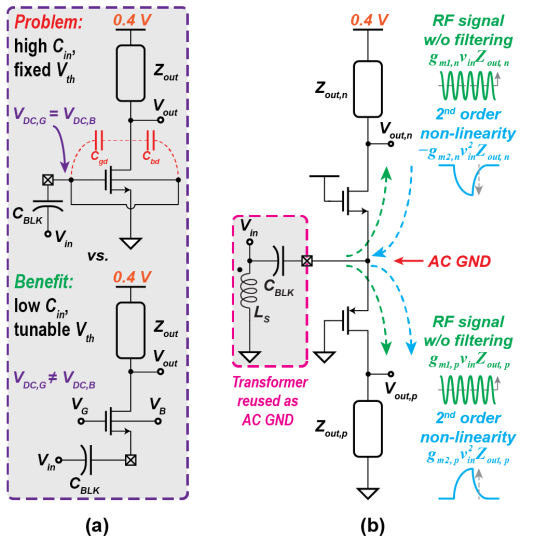

Fig. 2. (a) Comparison of DTMOS CS and CG EDs; (b) active pseudo-balun current-reuse CG ED operation.

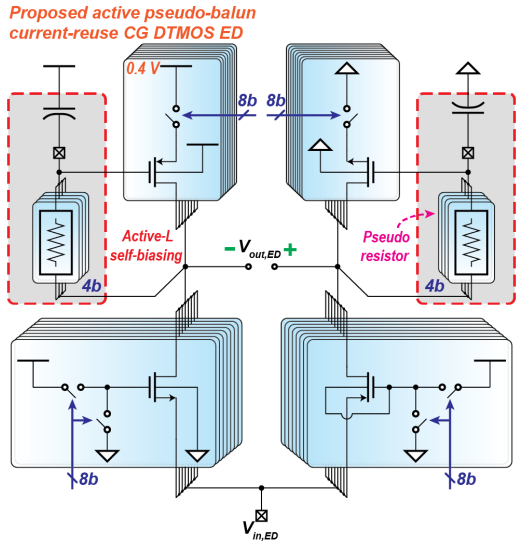

Fig. 3. Schematic of the proposed active pseudo-balun current-reuse CG DTMOS ED.

18.5 dB. The passive voltage gain is limited by the effective parallel resistance of secondary coil L_S ($R_{S,p}$) and the ED input resistance (R_{in}). Since $R_{S,p} \simeq \omega LQ$, larger inductors can achieve larger R_S; however, to maintain high gain via resonance at 400 MHz with a large inductor, a small ED input capacitance is required. For example, the transformer utilized $L_P = 6.5$ nH and $L_S = 50$ nH, necessitating $C_{in,ED} < 3$ pF. Unfortunately, this conflicts with the desire to size the ED transistors large enough to minimize the effect of $1/f$ noise at baseband given the low data rate of the WuRX (300 bps). Prior work, which utilized a dynamic threshold (DTMOS) common source (CS) ED [4], had significant C_{gd} and C_{bd} (Fig. 2a), precluding operation at 400 MHz.

In this work, we propose an active pseudo-balun ED that reduces C_{in}, increases R_{in}, and improves the ED scaling factor, k_{ED}, compared to prior work via a current re-use pseudo-differential CG DTMOS architecture. As illustrated in Fig. 2(a), compared to a CS ED, the CG ED only has the source connected to the RF input whereas both the gate and bulk nodes are connected to a DC bias voltage, which eliminates the effects of C_{gd} and C_{bd} on the input. This configuration reduces input capacitance by 47.5% in simulation while maintaining the 16% 2^{nd} order transconductance improvement of a DTMOS CS design. At nA current levels, the input resistance of a CG design is comparable with its CS counterpart, and is larger than a CS amplifier with DTMOS configuration because of the elimination of the bulk connection to the input. The new nW ED achieves an $R_{in} > 30$ kΩ at 400 MHz in simulation. Moreover, the DC bias voltages for the gate and bulk nodes can be set at different potentials for threshold voltage adjustment and freedom of transistor sizing, whereas for a CS architecture an additional off-chip capacitor and bias resistors are required, leading to extra input capacitance and a noise penalty.

Conventional single-ended EDs need either a reference ladder [4] or replica ED [1] to serve as the comparator reference voltage, which require power overhead and/or PVT tuning. Using an RC low-pass filter at the ED output as a dynamic reference is another solution, but at the expense of degraded SNR due to the pulsed nature of the baseband signal. In the proposed ED, two n- and p-type CG amplifiers are stacked in a current re-use structure (Fig. 2b) to provide single-ended to pseudo-differential conversion, eliminating the need for an explicit reference. Interestingly, the proposed ED acts as a pseudo-balun only to 2^{nd} order non-linearities: linear RF currents flow symmetrically through the n- and p- CG amplifiers to partially cancel at the outputs (and are then further filtered), yet the baseband 2^{nd} order components flow pseudo-differentially with slightly different gains due to the asymmetric loading. Compared to a fully (pseudo)-differential CS design [5], the proposed ED's input is inherently an AC ground because of the transformer and thus no bias circuits (with their additional parasitic capacitance) are required at the input. Furthermore, the current re-use pseudo-differential architecture improves the ED scaling factor, k_{ED}, by 66.6% compared to [4], and the WuRX sensitivity by 1.5 dB without a power penalty. The full ED schematic, which is depicted in Fig. 3, uses an active-inductor bias technique with MOS-bipolar pseudo-resistor feedback in the load circuits to increase output impedance and therefore k_{ED}. To overcome process variation, all transistors have 8b of tunability while the pseudo-resistor cells have 4b.

B. Baseband Circuitry and Coding

To overcome clock asyncronization, the ED output is band-pass filtered, 2× oversampled and digitized by a two-stage comparator, which includes a dynamic g_m-C preamplifier and a regenerative latch for low input-referred noise (Fig. 1). The comparison threshold voltage is programmed via two 6b capacitor DACs that also tune out the preamplifier offset

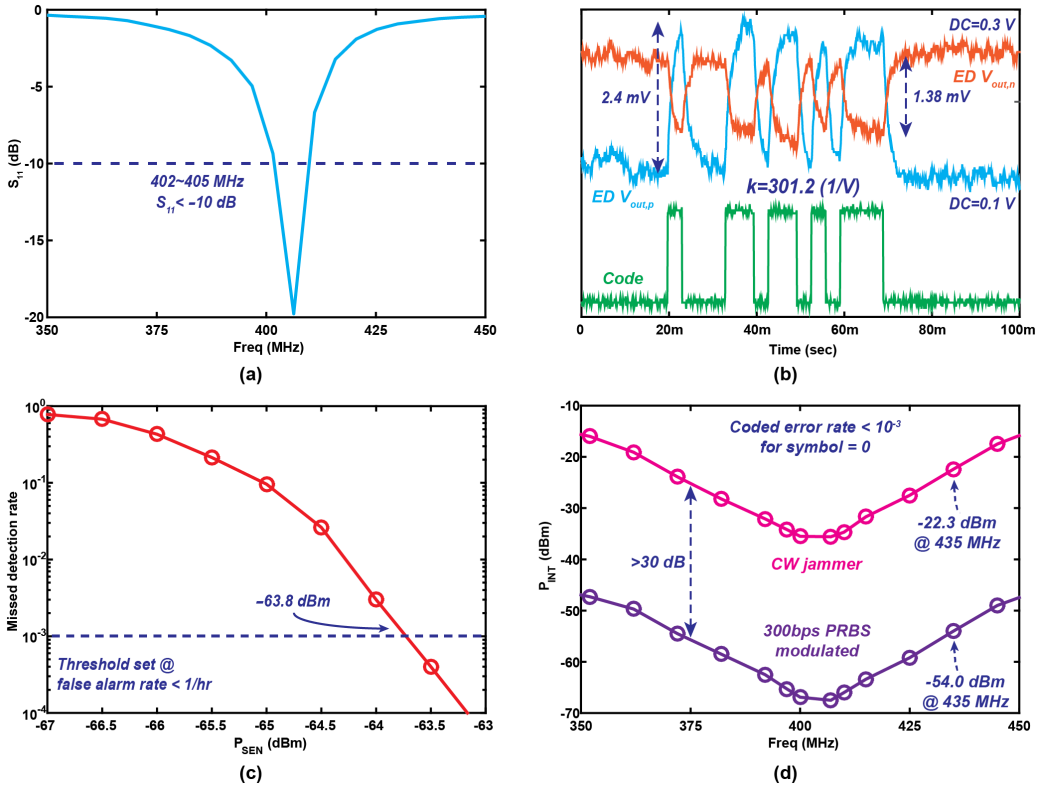

Fig. 4. (a) S_{11} measurement; (b) ED output transient waveform; (c) missed detection rate vs. input signal power; (d) interferer power vs. frequency.

voltage. Due to the unbalanced output impedances from the pseudo-balun ED, a S/H circuit was added to store the dynamic comparator kickback charge and provide balanced impedances. The comparator output is then processed by a 32b digital correlator to compute correlation against a programmable codebook. Once the value exceeds a pre-defined threshold, a charge pump generates a 1.2 V signal to indicate wake-up. The 16b signature sequence was designed to achieve the optimal Hamming distance from all of its shifted versions and from the all-0 sequence.

C. Relaxation Oscillator

A stable clock is provided for the whole system by a 1.14 nW temperature-insensitive comparator-based relaxation oscillator (Fig. 1). A PTAT reference current is generated to charge an integration capacitor C_{int} and generate a reference voltage V_{ref}. A two-stage continuous-time comparator resets the integration capacitor repeatedly after V_{int} crosses V_{ref}. Compared to conventional comparator-based oscillators, where the RC is trimmed to have a low-temperature coefficient and the comparator is designed with high bandwidth and negligible delay, this work uses a PTAT current to bias the two-stage comparator with a well-controlled CTAT delay. This CTAT delay along with the intentional PTAT RC integration time cancel to realize a periodic pattern with a temperature coefficient less than 94 PPM/°C. Since the comparator bandwidth requirement is greatly relaxed, this technique results in high power efficiency (0.94 nW/kHz).

III. Measurement Results and Conclusion

As shown in Fig. 4(a), the measured S_{11} is < -10 dB indicating good input matching across the 402-405 MHz MICS band. Transient waveforms from the 1.8 nW ED when the coded OOK signal is received are shown in Fig. 4(b), illustrating the pseudo-differential operation. The measured ED scaling factor k_{ED} is 301.2 (1/V). From the missed detection rate waterfall curve, the WuRX achieves a sensitivity of -63.8 dBm when the threshold is set to have a false alarm rate of $<$1/hr (Fig. 4c). The measured passive voltage gain of the 400 MHz transformer filter is 18.5 dB. Compared to the design of [4] with 25 dB passive voltage gain at 113.5 MHz and -69 dBm sensitivity, an additional ~ 1.5 dB improvement in sensitivity was achieved from the proposed pseudo-balun ED. The high-Q transformer filter also helps to block unwanted interferers, as the WuRX was measured to tolerate > -50 dBm 300 bps pseudo-random binary sequence (PRBS) modulated jammers, and > -20 dBm higher modulation frequency/continuous wave jammers at a 50 MHz offset without adversely affecting performance as shown in Fig. 4(d).

Table I summarizes the measurement results of the proposed WuRX and compares the results to the state-of-the-art sub-10 μW WuRXs. To compare prior ED designs with different power consumption, the ED efficiency k_{ED}/P_{ED} is computed and the proposed ED achieves the highest efficiency. This chip was fabricated in 0.18 μm CMOS SOI process and directly bonded to a PCB-mounted 400 MHz transformer

TABLE I
PERFORMANCE COMPARISON OF STATE-OF-THE-ART SUB-10 μW WURXS

	[1] RFIC'12	[5] ISCAS'15	[3] ISSCC'16		[4] ISSCC'17	[2] CICC'13	**This Work**
Technology	130 nm	180 nm	65 nm		180 nm	130 nm†	**180 nm**
Supply Voltage	1.2 V	0.8 V	1 / 0.5 V		0.4 V	1.2 / 0.5 V	**0.4 V**
Data Rate	100 kbps	100 kbps	8.192 kbps		0.3 kbps	12.5 kbps	**0.3 kbps**
Passive Gain	12 dB	13 dB	N/A		25 dB	5 dB	**18.5 dB**
ED Type	Active CS single-ended	Active CS fully-differential	Passive Dickson single-ended		Active CS single-ended	Passive Dickson single-ended	**Active CG pseudo-balun**
ED Power P_{ED}	23 nW	2.4 μW	0		2.1 nW	0	**1.8 nW**
ED R_{in}@RF	505.6 Ω	N/A	N/A		10 kΩ*	76.3 Ω	**30 kΩ***
ED Scaling Factor k_{ED} ($\frac{1}{V}$)	112.2*	1.1×10^{4*}	N/A		180.8	N/A	**301.2**
ED Efficiency k_{ED}/P_{ED} ($\frac{1}{V\cdot nW}$)	4.9*	4.6*	N/A		86.1	N/A	**167.3**
Comparator Reference	ED replica	None	RC LPF		Reference ladder	N/A	**None**
Carrier Frequency	915 MHz	2.4 GHz	2.4 GHz		113.5 MHz	403 MHz	**405 MHz**
Sensitivity	−41 dBm	−50 dBm	−39 dBm	−56.5 dBm	−69 dBm	−45 dBm	**−63.8 dBm**
RX Power	98 nW	4.5 μW	104 nW	236 nW	4.5 nW	116 nW	**4.5 nW**

† Using zero V_{th} transistors. * Post-layout simulation results. * Calculated based on provided measurement or simulation results.

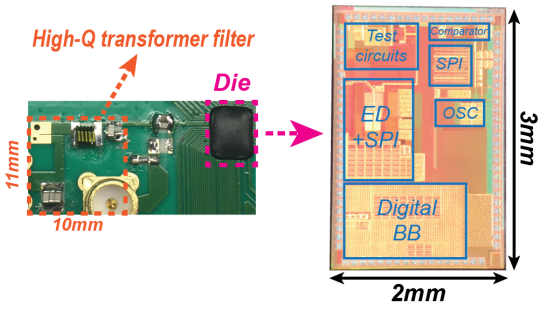

Fig. 5. Board and die photograph.

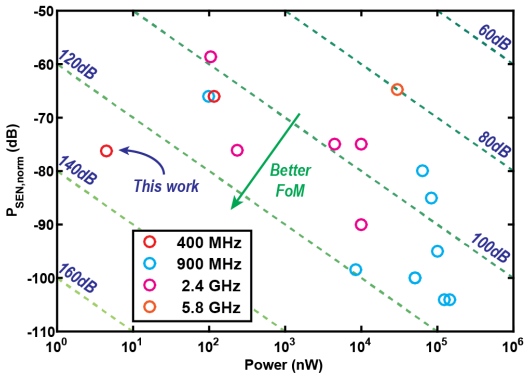

Fig. 6. Normalized sensitivity vs. power landscape with FoM contours for $>$ 400 MHz WuRXs using direct envelope detection architecture

filter, as shown in Fig. 5. To compare to prior work using direct envelope detection architecture with different data rate and therefore, baseband bandwidth, BW_{BB}, the normalized sensitivity can be computed as:

$$P_{SEN,norm}(dB) = P_{SEN} - 5\log BW_{BB}, \quad (1)$$

where P_{SEN} is sensitivity in dBm, and $5\log BW_{BB}$ is used to account for the non-linear squaring nature of EDs [6]. Moreover, considering power consumption, with (1) the following figure of merit (FoM) is derived:

$$FoM(dB) = -P_{SEN,norm} - 10\log\frac{P_{DC}}{1mW}, \quad (2)$$

A landscape of $P_{SEN,norm}$ vs. power along with FoM contours for previously published $>$ 400 MHz WuRXs using direct envelope detection architecture is shown in Fig. 6, illustrating that the proposed design achieves the highest FoM (129.7 dB) amongst prior work through a combination of excellent sensitivity (−63.8 dBm) and ultra-low power (4.5 nW), all at a practical frequency of 400 MHz.

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REFERENCES

[1] N. E. Roberts and D. D. Wentzloff, "A 98 nW wake-up radio for wireless body area networks," in *RFIC Symp.*, Jun. 2012, pp. 373–376.
[2] S. Oh *et al.*, "A 116 nW multi-band wake-up receiver with 31-bit correlator and interference rejection," in *Proc. CICC*, Sep. 2013, pp. 1–4.
[3] N. E. Roberts *et al.*, "A 236nW -56.5dBm-sensitivity bluetooth low-energy wakeup receiver with energy harvesting in 65nm CMOS," in *ISSCC Dig. Tech. Papers*, Feb. 2016, pp. 450–451.
[4] H. Jiang *et al.*, "A 4.5nW Wake-Up Radio with -69dBm Sensitivity," in *ISSCC Dig. Tech. Papers*, Feb. 2017, pp. 416–417.
[5] S.-E. Chen *et al.*, "A 4.5 μW 2.4 GHz Wake-Up Receiver Based on Complementary Current-Reuse RF Detector," in *Proc. ISCAS*, May 2015, pp. 1214–1217.
[6] X. Huang *et al.*, "Noise and sensitivity in RF envelope detection receivers," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 60, no. 10, pp. 637–641, Oct. 2013.