Code Selective Filters in CMOS Processes for Full Duplex Communication and Interference Mitigation

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***Abstract*—RF signal processing techniques based on orthogonal PN sequences can be implemented as passive circuits at the antenna to mitigate interference from co-site transmitters, multi-access interferers, or other blockers. Scaled CMOS transistors offer excellent RF switch performance as well as high-frequency, low-power signal processing. We present a 45-nm CMOS SOI code selective filter that is capable of direct sequence spread-spectrum modulation and demodulation for full duplex or frequency duplex systems with high interference requirements.**

Keywords—Code-selective Filter, CMOS, N-path

I. Introduction

Full duplex (FD) communication has been proposed as a wireless access technique that can theoretically double the capacity of a communication channel [1]. FD communication links place strict requirements on the receiver (RX) to remain sensitive in the presence of a strong in-channel blocker, most often a co-located transmitter (TX). This sensitivity is realized by cancellation of the TX signal, but imperfect cancellation of in-band signals can significantly reduce the 3 dB theoretical improvement, resulting in negligible gains. Nonetheless, the benefit of FD communication could extend beyond spectral capacity to include channel estimation and control sequences used to optimize channel estimation.

Current circuit approaches to FD communication are based on a combination of electromagnetic isolation between TX and RX ports at the antenna, active RF/analog cancellation through on-chip calibration, and digital signal processing (DSP). This solution is excellent for co-site interferers that have relatively predictable and slowly varying interference characteristics. However, in multiple access networks, the FD receiver must operate in an environment consisting not only of a cosite transmitter but also of cooperative and uncooperative jammers. Furthermore, the circuit overhead for providing interference cancellation poses a significant challenge to realize the signal-to-noise ratio (SNR) improvements at the receiver without high power consumption penalties.

This paper discusses the use of direct spread spectrum sequence (DSSS) and requirements for highly linear code-selective filters (CSF) to process DSSS signals at the antenna. In this work, DSSS coding techniques are suggested as an alternative coding approach to realize FD wireless access to simultaneously provide interference cancellation at reasonable power consumption.

II. Spread Spectrum Interefence Mitigation in Full Duplex Communication

The DSSS access approach to FD communication relies on the introduction of an orthogonal basis that can be leveraged to reject interference. Notably, a codebook of psendonoise (PN) sequences is attached to all transmissions in the FD access scheme to mask signals. The basic FD communication channel access scheme is illustrated in Fig. 1. The desired transmit signal TX_A is spread with a PN code sequence, labelled PN_A. Other cooperative (multiple access) transmit signals are encoded with orthogonal PN sequences. Both the desired and cooperating signals experience channel fading – though likely not identical - before they reach the receiver. An uncooperative jammer such as a continuous wave jammer that is not encoded with a PN sequence should also be filtered at the receiver to prevent distortion. Finally, a cosite transmit signal TX_B is spread with another orthogonal sequence PN_B. Note that in terms of signal power the cosite transmit signal will typically have the highest signal power (> 30 dBm) and therefore impose the most significant linearity limitation on the receiver. However, the TX_B signal is also easily estimated at the receiver since it is a cosite signal.

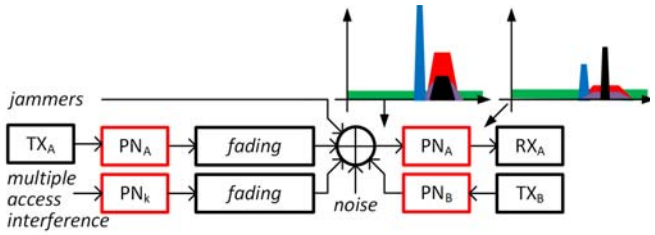

Figure 1. Channel model for direct-sequence spread spectrum for full-duplex communication. The desired signal (shown in black) is selected in the receiver while orthogonal signals (shown in red) and jammers (shown in blue) are rejected.

The optimal receiver correlates the received signal against the desired PN sequence, in this case PN_A. The resulting SNR at the receiver for the FD-DSSS system is a combination of the noise, jammers, and the residual orthogonal sequences that are spread by the received PN sequence. The SNR for the desired TX signal is

$$SNR = \frac{\int_{kT}^{kT+MT_C} \left(\left(TX_A(t') \cdot PN_A(t') \right) * h_1(t') \right) PN_A(\tau + t_o)\, d\tau}{\sigma_n^2 + \int_{kT}^{kT+MT_C} \left(\left(TX_k(t') \cdot PN_k(t') \right) * h_k(t') \right) PN_A(\tau + t_o)\, d\tau}$$

where $t' = t + \tau$. The integrate and dump function is used to correlate the signal components against the PN sequence. During each transmit symbol of period T, the N chips with period of T_c of the psuedonoise sequence are integrated. A phase shift of t_o accounts for a static skew between the transmit and receive codes. The fading channel impulse response is expressed as $h(t)$ and the noise variance is σ_n. Besides the noise, the second term in the denominator indicates the correlation of the two orthogonal PN sequences should integrate to zero to avoid reducing SNR. In the limit that no jammers are present and the channel model offers only loss, the SNR reduces to the common form $SNR = v_{RX}^2 / 2\sigma_n^2$ where v_{RX} reflects the RX power that reaches the receiver.

Simulations in Fig. 2 plot the SNR as a function of the integration period (shown here as a function of the chip period) and the relative strength of the TX signal and the RX signal. The plot indicates that relatively strong interference from a multiple access user is mitigated as the integration period increases. In other words, the symbol rate should decrease to accommodate the stronger TX signal.

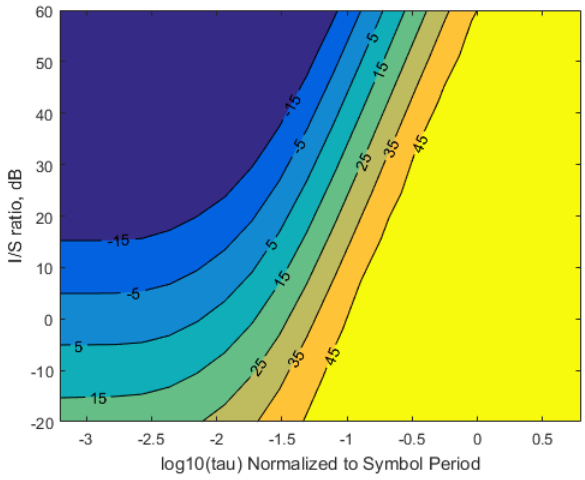

Figure 2. Contour plot of SNR as a function of integration time constant and difference between power levels for the RX and TX for 16-length Walsh codes.

In the presence of a more general fading channel, the signal power must be maximized with respect to the fading channel impulse response $h_1(t)$. Realistically, tracking the fading channel of other cooperative multiple access signals might be unrealistic and result in an unavoidable SNR degradation. However, the TX_B signal is anticipated to be strong and, therefore, must be filtered to realize high SNR.

III. Circuit Architectures for Code Selective Filters

To enable FD, orthogonal signal processing should occur before strong interference generates distortion in the receiver, presumably at the low-noise amplifier. For DSSS signal processing to occur at the antenna, circuit techniques are required that operate with high linearity and low insertion loss. The RF correlation must be performed in a matched filter that filters not only the out-of-channel blockers but also passes the desired spread spectrum PN code. Here, we investigate a code selective filter (CSF) based on linear, time-varying circuits. We propose a family of CSFs based on the desire to achieve a code pass or code reject response.

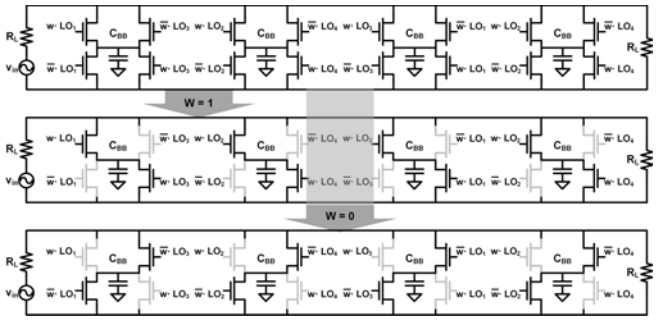

Figure 3. Model of a shunt code selective filter based on the linear, time-variant N-path circuit.

A. Code Selective Filters

A shunt CSF is illustrated in Fig. 3 based on an $N = 4$ path filter. In an N-path filter, the differential RF input signal is sampled onto a bank of capacitors with a $1/N$ duty cycle, non-overlapping clocks. The filter response can be tuned based on the clock frequency [2-4]. In the code-selective filter, the sampling occurs from ANDing the clock waveform and the PN sequence value w. During the k^{th} clock phase, the modulated clock signal determines whether the RF signal is connected to the positive or negative RF line and sampled onto the baseband capacitor, C_{BB}. Subsequently, the baseband voltage on the capacitor is then remixed with the clock phase to the output. The code domain N-path was previously presented in [5] and [6] with the later to show the reduction in LO leakage that could be achieved through PN spreading.

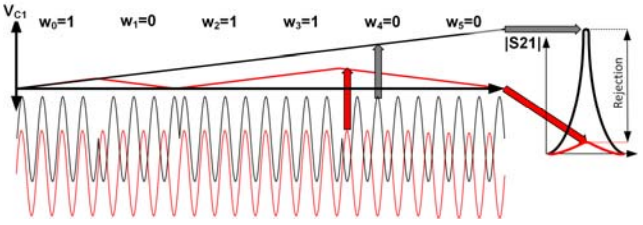

Figure 4. Illustration of the code-selective filter as distinguished from an N-path filter. Orthogonal codes are integrated to zero charge on the capacitor reducing the impedance that is seen by the RF signal.

To explain the operation of the CSF, Fig. 4 illustrates two RF signals in black and red. One is modulated with a BPSK DSSS that matches the code sequence that modulates the CSF.

For the matched RF signal (in black), the RF signal continues to charge the baseband capacitor, resulting in a linear increase in the baseband voltage. As the voltage increases, it becomes harder to charge the capacitor from the RF signal and the RF impedance produced by the filter increases. For the orthogonal RF signal (in red), the integration results in zero voltage over the full period of the PN sequence. This results in an average impedance which is much lower than the matched code case. The result is an RF signal correlation that produces code-domain behavior that controls the impedance of the RF filter. The fundamental insight is that a frequency response – such as a band-pass filter or pass-band filter – can be realized at the same frequency band depending on the code sequence.

The baseband capacitor shown in the CSF generates an *RC* time constant associated with the capacitance value and the load impedance. This time constant is equivalent to the integration time constant shown in Fig. 2. To maintain the same SNR as the relative power between the jammers and desired signal increases, the baseband capacitor should be controlled. Consequently, the baseband capacitor is typically chosen based on the symbol period of the transmitted data. It is important to note that the chip period T_c of the PN sequence is much shorter than the symbol period. The bandwidth of the DSSS TX signal is therefore much wider than the signal bandwidth, and, consequently, the filter band pass or band reject response. To illustrate this point, a simulation of the baseband signal attenuation is shown in Fig. 5 with a model of the switch resistance and baseband capacitor. If the circuit operates as an *N*-path filter, the response of the filter is to pass a signal that falls "near" the LO frequency at 1 GHz with little attenuation. The *N*-path response indicates a passband filter with a 10 MHz bandwidth. If the filter is instead operated as a code selective filter with a 64-length Walsh code, the CW signal is now attenuated by 15 dB, indicating rejection of an orthogonal sequence.

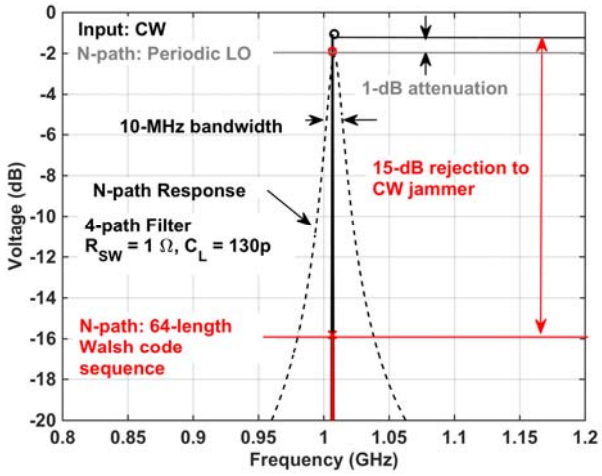

Figure 5. Frequency response of the CSF in the presence of a CW input when 1) the switches are modulated as a period 1/N clock (dashed line/black) and 2) the switches are modulated with a PN sequence.

Several critical implementation features of the code selective filter must be addressed, however, including 1) reciprocal mixing that is introduced by the pseudonoise signals at the switches, 2) filter linearity, and 3) signal processing algorithms that allow for code synchronization. To the second and third points, an important feature of this architecture is the to select a process that offers excellent RF operation while being switched at the RF carrier frequency.

The power requirements of a shunt CSF can readily be calculated from the performance requirements and parameters of the switch circuit process. The power consumption is bounded by the digital power consumption required to clock the *N*-path switches.

$$P_{DC} \geq NCV_{DD}^2 f_{LO} = cN\tau_{SW} P_{1dB} f_{LO} REJ$$

The second equality is found from relating the capacitance on the gate to the switche's off capacitance, the voltage (clock) swing on the switches to RF signal power in terms of P_{1dB}, and the load impedance and on-resistance to the out-of-band rejection (*REJ*) of the filter. A constant *c* is added to correct for missing factors in this relationship. A fundamental feature of the power consumption is the switch time constant, τ_{SW}, found from the product of the switch on resistance and off capacitance ($R_{ON}C_{OFF}$).

IV. CMOS Processes for RF Signal Processing

While the implementation of a time-varying filter could be envisioned in a number of integrated circuit processes to satisfy different requirements, the key feature is the intimate integration of the digital PN sequence generation, LO generation, and a high-performance RF switch. Standard CMOS processes will generally address the first two demands while a high-voltage switch (conceivably GaN) offers the best linearity.

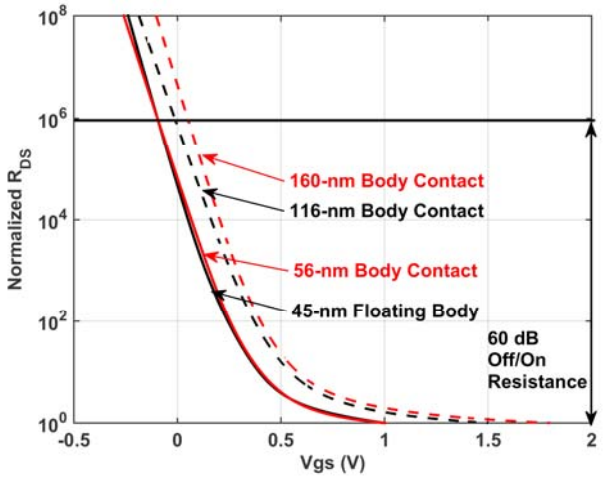

Figure 6. ON resistance of n-FET devices in SOI CMOS for different device configurations at different channel lengths.

However, routing of LOs between a CMOS and GaN *N*-path circuit poses a significant packaging problem related to spurious electromagnetic signals. To address the switch

performance, scaled SOI CMOS at 45-nm and finer lithography allows excellent RF switch performance. Notably, SOI CMOS has been adopted for commercial RF front-ends such as antenna tuners where similar high power (~30 dBm) and higher linearity requirements persist. Recent work on *N*-path filtering has been explored with CMOS SOI processes and demonstrated excellent IIP3 [7][8].

The ON resistance for different devices is illustrated in Fig. 6 for different device variants. While the 45-nm floating body device conventionally has the highest f_T, the switch time constant, as measured by the $R_{ON}C_{OFF}$ product, increases from around 54 fs for the 45-nm floating body device to only 64 fs for the 160-nm body contact device. The relatively small increase in time constant is also offset by the higher off resistance in the 160-nm body contact device for V_{DS} = 0. Unless the 45-nm floating body device is driven with negative voltage swing, the on resistance of these devices is basically compromised.

V. CMOS Implementation for RF Signal Processing

An example of the CSF concept has been illustrated under the DARPA SPAR program. A code-reject filter is designed that addresses cosite jamming from a local transmitter tagged with a known PN sequence. To reject the transmitter, a shunt filter is constructed with the GlobalFoundries 45-RF CMOS SOI process. The chip includes an LO signal generator to generate the 1/*N* duty clocks and digital logic to AND the PN sequence with the 1/ *N* clocks. The design of the 4-path filter follows earlier work in the literature, however, uses 116-nm body-contacted devices due to a simulated 1-dB IIP3 improvement over 45-nm floating body devices. The chip microphotograph measures 1.6 mm by 1.2 mm and is dominated by capacitor area. The chip requires 10 mW when operated a frequency of 1 GHz. The chip is mounted on a PCB with an on-board quarter wave transmission line that inverts the large impedance presented by the shunt filter to a low impedance when the codes of the filter and the input RF signal are matched.

Measurement of the frequency response of the CSF is shown in Fig. 7. If no code is modulated against the LO clock signals, the shunt filter produces a "notch" response (shown in black) due to the impedance inversion of the quarter-wave line. The depth of the notch indicates rejection exceeding 20 dB for frequencies near 1 GHz.

If a 16-length PN sequence is applied to the LO generator, the CSF now only provides the band reject for signals with a matching code. In the case that the PN sequence is orthogonal to the input RF code, the filter allows the signal to pass as shown in Fig. 7 in red. Note that the insertion loss of the stand-alone filter is 3 dB.

The filter operation is illustrated in Fig. 8 for different codes. When the code selective filter is a matched to the Walsh code used to tag the RF input signal the signal passes through the filter (shown in blue). If the code selective filter is not tagged with a PN sequence, i.e. operates in *N*-path mode, the rejection of the TX signal occurs only over a relatively narrow signal bandwidth. Finally, if an orthogonal sequence is used, in this case a 13-length Barker code, 18.6 dB of rejection is measured. It is important to note that this rejection is broadband, covering more than 300 MHz.

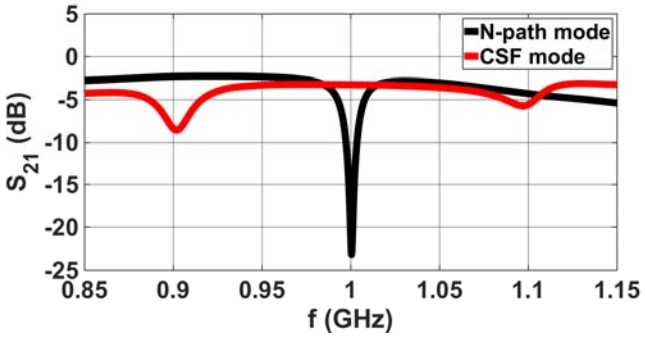

Figure 7. Frequency response of the CSF in the presence of a CW input when 1) the switches are modulated as a period 1/N clock (dashed line/black) and 2) the switches are modulated with a PN sequence.

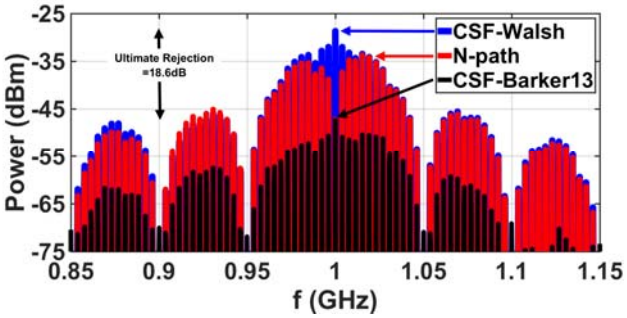

Figure 8. Comparison of the filter rejection for different code states illustrating the potential for wideband signal rejection.

Conclusion

This paper describes the requirements of DSSS signal processing for FD communication and illustrates a code-selective filter circuit technique that can realize in-band signal rejection. A 45-nm CMOS SOI circuit is illustrated that achieves more than 18 dB of TX signal rejection with a low power consumption.

Acknowledgment

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