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US Army Research Laboratory

Greyscale Photolithography for Multilayer PZT Microelectromechanical Systems (MEMS) Device Applications

by Delaney M Jordan, Robert R Benoit, Gabriel L Smith, and Ronald G Polcawich

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14. ABSTRACT
We present development of a process to perform greyscale photolithography on a 2.55-µm thick photoresist in order to transfer tiered and sloped structures into multilayer thin films using a single-ion mill etch. Applications include access to buried layers, such as electrodes in a stack of multilayer lead zirconate titanate (PZT), or ramps for routing signal lines over large step heights. Current state-of-the-art processing requires a separate photolithography step and an ion mill etch for each layer of the substrate, which can be costly and time-consuming. The greyscale process was tested on three silicon wafers with a stack of four PZT thin film layers of either 0.25-µm thickness or 0.5-µm thickness per layer, with platinum or iridium oxide (IrO2) electrodes above and below each layer. Process variables including resist rehydration, focus of the exposure, and UV cure/bake temperature were optimized to produce the best greyscale profile through the thickness of the resist.

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greyscale lithography, multilayer PZT Stacks, lead zirconate titanate, MEMS, microfabrication

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Preface

This document reports on the methods and best practices for performing greyscale lithography using a Heidleburg direct-write laser (DWL) system owned and operated by the US Army Research Laboratory (ARL). The techniques involved are not specific to multilayer lead zirconate titanate ($Pb(Zr_xTi_{1-x})O_3$ (PZT)) stacks and can therefore be readily extended to any multilayer composite thin film. This document was created with the expectation that fellow researchers will use it to achive similar photolithography results for their own microfabrication applications; therefore, its primary focus is the lithography process. The electrical characteristics of the PZT films are described in detail in Benoit et al.[1]

Acknowledgements

The authors would like to thank Mr S Isaacson and Mr J Martin of the ARL for their roles in the fabrication of the PZT stack; Mr C Bach of Heidelberg Instruments and Dr M Roy of the ARL for their support of the Heidelberg DWL 200; and Dr S Bedair of the ARL for her role in the design of the microelectromechanical systems (MEMS) devices.

1. Introduction

Micromachining techniques for wafer substrate processing are constantly pushing the limits of microfabrication technology. Photolithography, which enables transfer of such small designs, is traditionally known as a binary technique, since each area of the wafer is either completely protected from or completely exposed to the radiation source. Single layer thin film lead zirconate titanate ($Pb(Zr_xTi_{1-x})O_3$ (PZT)) microelectromechanical systems (MEMS) have been shown to improve the performance of a wide range of sensors and actuators for robotics, RF devices, and power conversion.[2] Using this process to transfer a staircase pattern to a wafer requires a photolithography step and an etch for each stair step.[3]

More recently, the successful microfabrication of multilayer PZT and platinum (Pt) has prompted a requirement to electrically address individual metal layers or connect alternating layers to make bi-directional actuators, sensors, and capacitors. Smith et al. previously demonstrated conceptual and experimental techniques to etch and access individual layers of metal and dielectric stacks with a single mask and ion-mill step.[4] This approach relies on greyscale lithography to ion-mill low-aspect ratio ramps (Fig. 1a) or multilevel steps (Fig. 1b) into a multilayer stack of alternating non-conductive/conductive dielectric/metal materials. Once etched (Fig. 2), the wafer can be wet etched with a chemically preferential etchant that will clear the dielectric from the metal regions. This exposes the individual metal layers for subsequent connection with standard Au trace routing so that voltage may be applied to these layers (Fig. 3a). This greyscale transfer process was accomplished with a High Energy Beam Sensitive (HEBS) glass greyscale test mask[5] in bare silicon (Si) wafers and in Si wafers with a 4-layer stack of PZT and Pt on Si substrates coated with 0.5 μm silicon dioxide. In both cases the scanning electron microscope (SEM) micrographs show clear evidence of pattern transfer of the discrete greyscale steps into the multilayer material (Fig. 3b). Since ion milling is a physical process, it extends to all metal/dielectric capacitive stacks.

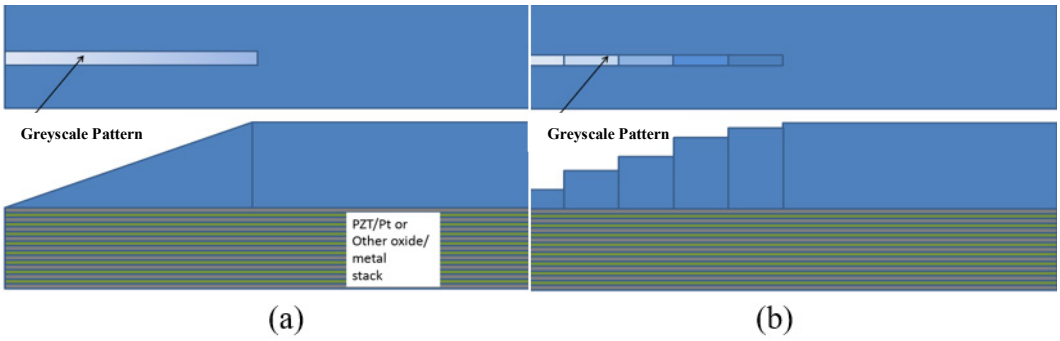


Fig. 1 Ramped greyscale resist pattern in (a) fine gradation (256 levels) between gray level on a stack of alternating layers of metal and oxides and (b) stepped grey coarse gradations (7 levels) between level. Lighter color represents thinner resist.

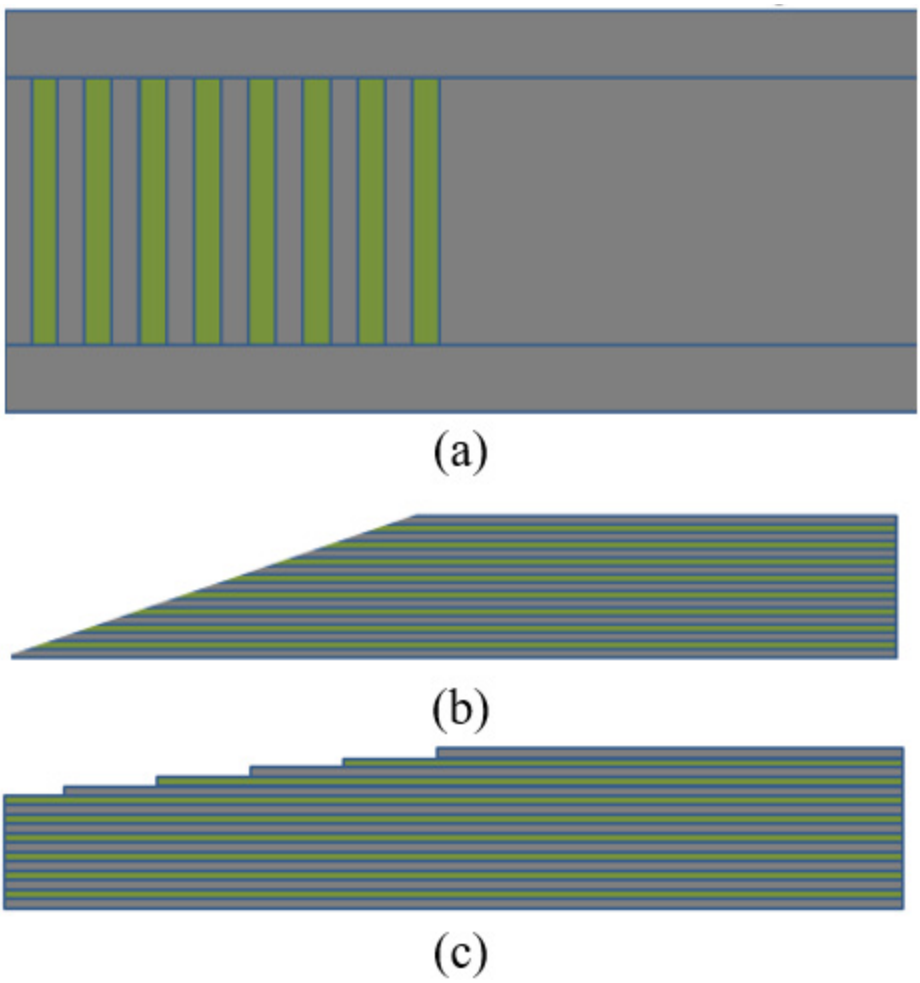
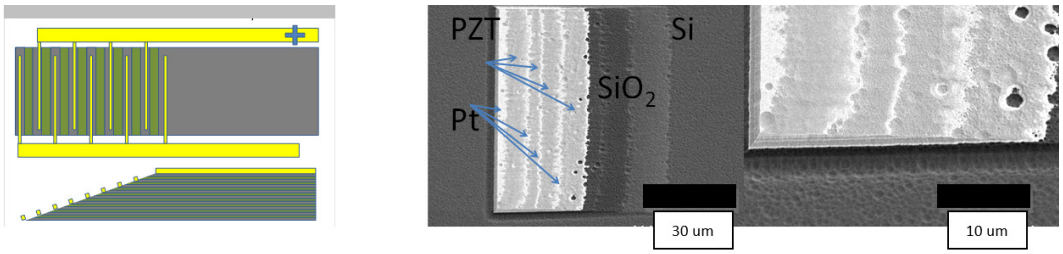


Fig. 2 Desired wafer profile after ion milling. (a) top and (b) side views of ramped profile from Fig. 1a, c) side view of ion-milled profile from Fig. 1b.



(a) (b)

Fig. 3 Exposed metal layers. (a) Top and side view of ramped pattern with a notional interdigitated electrode multilayer stack and (b) SEMs of exposed metal layers in 4-layer 0.25-um PZT/Pt stack from a single ion mill. The greyscale pattern in this case was generated using HEBS glass.

While the HEBS glass is effective for implementing greyscale lithography, at approximately $2,000 per 4-inch mask plate, it is also quite costly. DWL greyscale (DWLG) lithography, an economical and flexible alternative for rapid device prototyping, is a microfabrication technique that uses a laser beam, modulating its intensity as it scans across the resist surface, leaving the photoresist partially exposed so that a proportional thickness remains after the resist is developed. This report presents a process for performing greyscale lithography on multilayer PZT/Pt/IrO2 wafers using a Heidelberg DWL 200. The DWL 200 has a theoretical range of 256 intensity (or grey) levels and a lateral resolution of 0.25 µm. Each grey level in the design corresponds to a specific thickness. This technique enables MEMS designers to create patterns in resist with a single lithography step that can be etched into the layer(s) below. The reduced number of processing steps dramatically decreases fabrication time and mitigates misalignment effects, enabling the rapid realization of multilayer PZT MEMS devices. Access to the intermediate electrodes in these devices permits higher capacitance densities through parallel wiring, bidirectional actuation of movable devices, and increased control of physical displacement with applications in micromechanical logic and tunable RF circuits.

2. Methods

Multilayer PZT wafers were fabricated according to the process described by Sanchez et al.[3] in order to achieve highly (001) textured films. Four-layer PZT stacks at thicknesses of either 0.25 µm or 0.50 µm per layer, with a bottom electrode of 320/1000-Å thick TiO_2/Pt and intermediate and top electrodes of 500-Å thick IrO_2 (Fig. 4), were deposited on Si substrates with 5000-Å thick thermal SiO_2. Process development was performed with 6-inch Si wafers of (100) orientation, then adjusted using multilayer PZT wafers before final etching.

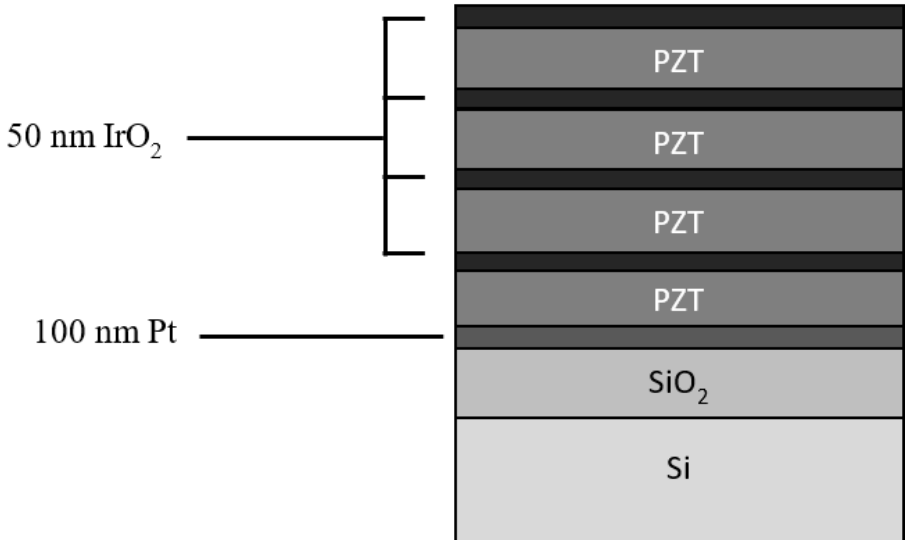


Fig. 4 Cross-sectional diagram of a multilayer PZT stack

The wafers were coated with 2.75-µm Clariant AZ5214E photoresist using an EVG 120 automated resist processing system. A double-coat process (i.e., each photoresist spin performed at 1250 rotations per minute) was used to achieve the desired thickness. A Heidelberg DWL 200 with 5-mm write head in greyscale mode was used to pattern the photoresist, where grey level 0 was zero exposure and grey level 255 was full exposure. Some electrode features were designed to function as ramps that exposed the full thickness of the PZT stack; others were designed to expose only certain buried electrodes. After the exposure, the image was developed in AZ300MIF developer solution. To prepare for ion milling, the wafer was UV cured at 175 °C using an Axcelis UV photostabilizer to further harden the resist. (Because the photoresist thickness actually shrank approximately 0.2 µm after UV curing, the final maximum thickness was 2.55 µm.) This thickness was chosen so that each grey level would correspond to 10 nm of photoresist (255 grey levels × 0.01 µm = 2.55 µm of photoresist). A 4wave Inc. 4W-PSIBE ion beam etch system was used for the single ion milling step. A secondary ion–mass spectrometer endpoint detection system stopped the ion milling process after exposing and removing the bottom Pt layer. Subsequently, the resist was removed with an O_2 plasma in a Metroline M4L Plasma Asher/Etcher.

The primary methods used for analysis included visual examination with an optical microscope, scanning of electron microscopy (SEM) images, and stylus profilometry to evaluate the accuracy of the process when compared to the design. The development time and uniformity at the die and wafer levels were also monitored. To accelerate iterative design, only 6 die were written onto the wafer, distributed evenly around the center and from center to edge. This enabled short write times of 30 min while still providing uniformity and resolution data.

3. Results and Discussion

3.1 Photoresist Rehydration

Photoresist development times varied wildly after exposure, ranging from several minutes to over an hour, until the following standard resist rehydration process was consistently used. After coating, each wafer remained in ambient conditions in the cleanroom for over 12 h to enable rehydration of the resist. This increased uniformity across the wafer, as well as repeatability of results and development times between wafers. Placing the wafer in water prior to exposure had the same effect as no rehydration at all, likely because leaving the wafer in ambient conditions allows it to reach equilibrium with the humidity value in the room (typically 40% at 21 °C). Consistent with the results, literature suggests that the optimal rehydration state of the wafer is 45–50%, and Heidelberg Instruments recommends at least 12 h of rehydration in air before exposure.[6] Rehydration values significantly above or below the ideal cause extended development times and poor uniformity.

An experiment was conducted to decrease the rehydration time by submerging the entire wafer in water before and after exposure. The results (listed in Table 1) indicate that rehydration in water does not drastically reduce the development time, but 15 min of rehydration does optimize the uniformity of photoresist development (i.e., the time between clearing the first and field and last field) across the wafer.

Table 1 Rehydration tests for development of photoresist exposed by DWGL

Trial	Rehydration before (min)	Rehydration after (min)	Development time (min:s)	Time between first and last fields (min:s)
None	0	0	6:57	1:02
Before	15	0	5:42	0:14
Both	15	15	5:38	0:23
After	0	15	6:44	1:14
Before	30	0	6:15	0:35

3.2 Stripe Overlay

The Heidelberg DWL 200 writes along the y-direction in stripes 200-µm wide (when using the 5-mm write head), causing visible “stripe lines” in partially and completely exposed regions positioned at the gaps between sequentially written stripes (Fig. 5). This problem was due to insufficient overlap between stripe lines, leaving lines of underexposed (and thus underdeveloped) resist. Overdeveloping

the resist could remove the stripe lines, but would wash out the highest (i.e., thinnest) grey levels. This issue was resolved by changing the focus and ramp settings in the tool. (Focus modifies the convergence point of the laser between two different stripes; ramp adjusts the exact width between stripes during exposure.) Initial trials had used the intensity, focus, and ramp settings that were set for mask writing mode, which was optimized for a 1-µm film of AZ1518 photoresist.[7]

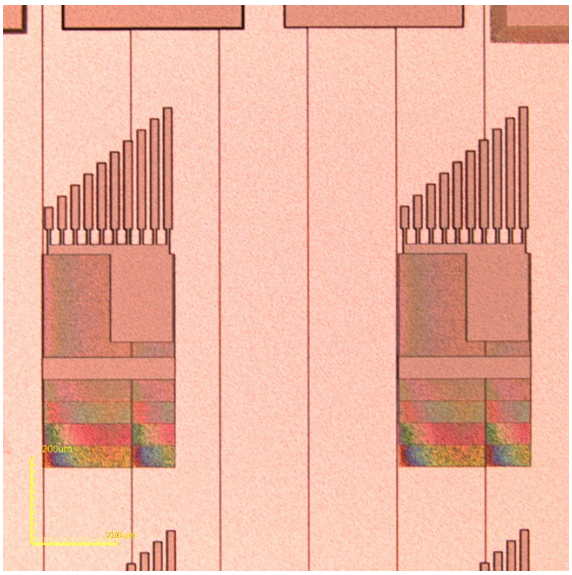


Fig. 5 Greyscale pattern after development, with visible stripe lines and chromatic changes in resist thickness

To optimize the focus, the center fields of an 11 × 11 grid with one die per field were written, varying focus values in steps of 5 units from –20 to 60*, encompassing the initial value for mask writing mode of 0. After development, visual inspection revealed that a focus value of 20 neither underexposed nor overexposed the stripe edges. This process was repeated, varying the ramp value by 0.1 units from 362.65 to 364.65 around the initial value of 363.65*. Unlike the focus value, high ramp values produced the image shown in Fig. 6a and low values produced that shown in Fig. 6c. The process was again repeated, varying the ramp value by 0.01 units from 363.55 to 363.70. The ramp value required adjustment after changing to a PZT substrate; the best values for Si and PZT were 363.92 and 363.60, respectively (Fig. 6b). Profilometry was used to determine that level 236 was the highest resolved grey level that was not washed away during development (Fig. 7).

* Note: Heidelberg does not use units for these values.

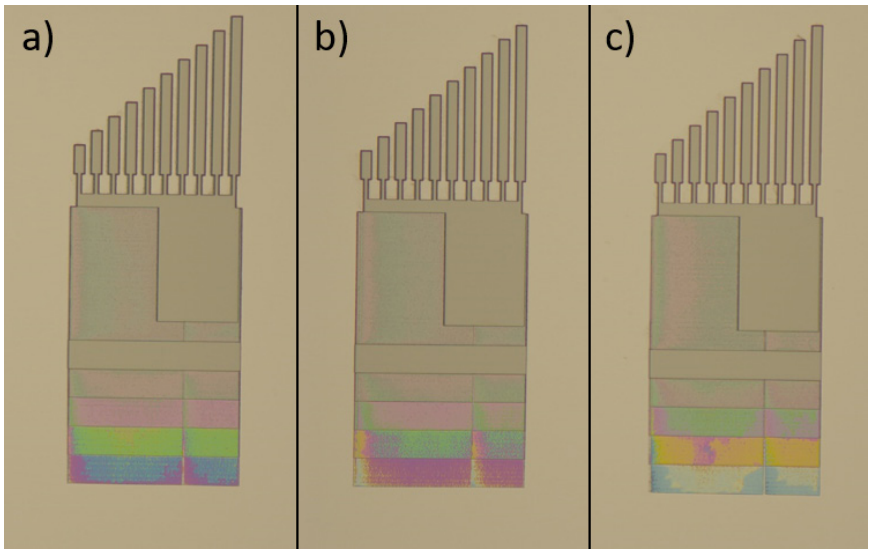


Fig. 6 Optical images of exposures on PZT coated substrates with a) ramp = 363.55, b) ramp = 363.60, and c) ramp = 363.65. Since there are gaps in the resist at the stripe line in a) and c), b) is the optimal setting.

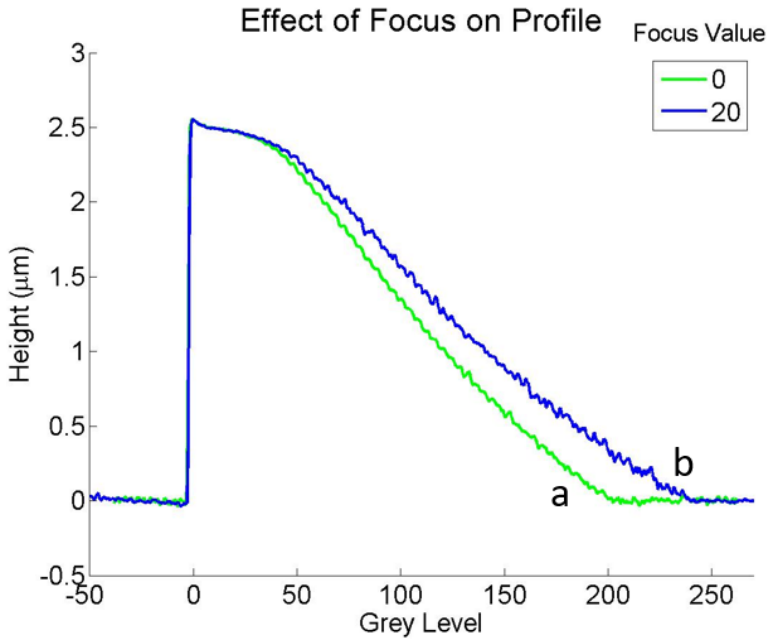


Fig. 7 Staircase profile a) before focus and ramp optimization (overdeveloped to remove stripe lines) and b) after focus and ramp adjustment

A linear chromatic aberration was still visible in the partially exposed areas of resist after focus and ramp optimization, and stylus profilometry verified that the stripe edges disrupted the pattern height by up to 100 nm (Fig. 8). Subsequent pattern

designs placed all electrode contact areas inside a single stripe line to avoid edge effects.

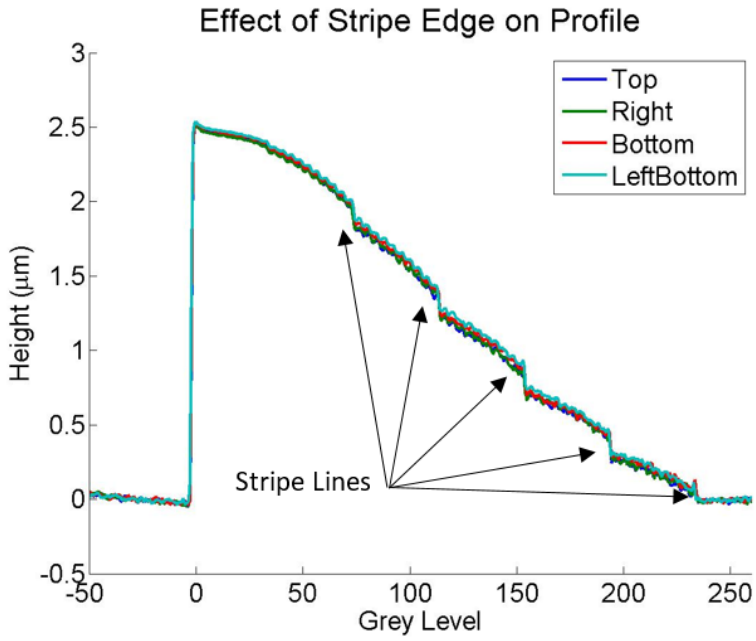


Fig. 8 Profile of a ramp using 64 grey levels scanned in the horizontal direction with respect to the wafer flat. Even after optimization, discontinuities at stripe boundaries appear every 200 µm.

According to Heidelberg Instruments*, stripe lines can be diminished by using the n-over feature and scaling the laser intensity. The n-over feature offsets successive strips by a distance of

$$\frac{W(n-1)}{n}, \tag{1}$$

where W is the stripe width and n is the n-over value. For example, an n of 4 will overlap two 200-µm stripes by 150 µm, thus quadrupling the time to expose the same area on a wafer. This option was explored briefly with an n of 10. Though there were no stripe lines in completely exposed regions, 10 times the stripe lines were observed in partially exposed regions (Fig. 9). Because the amount of time the n-over feature added to each write was excessive, it was not investigated further.

* Personal correspondence with Heidelberg.

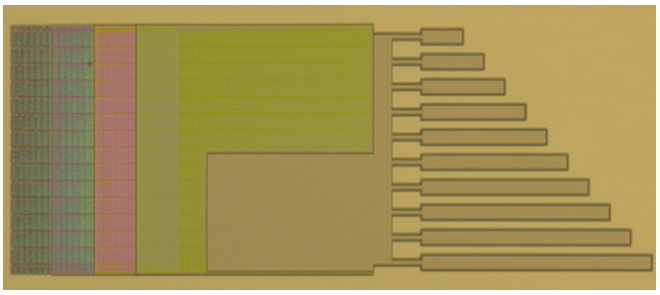


Fig. 9 Photoresist exposure with n-over value of 10

3.3 UV Cure

A bake/UV cure step was used to harden the resist prior to milling with the ion beam. The resist coating spin speed was chosen to produce a height of 2.55 µm after curing, such that each grey level would correspond to a height change of 10 nm, and all stylus profilometry was done after curing to ensure an accurate characterization of the resist profile. Bake temperature was also investigated (at 150 °C, 175 °C, 200 °C, and 220 °C), the outcome being that temperatures over 175 °C caused delamination and flaking of the resist. Although this did not appear to affect the integrity of the photoresist, it did produce particles that affected the pattern on the wafer. Different baking temperatures could result in different etch rate selectivity, which was not investigated.

3.4 Ion Milling

After the greyscale process was optimized on PZT substrates, the wafers were etched by ion milling to a depth exceeding 1.25 µm (for design of the PZT stack with 0.25-µm layers) or 2.25 µm (for design of the PZT stack with 0.50-µm layers). Stylus profilometry determined that the lowest grey level that would be transferred into the substrate without remaining in the excess resist was 134 for the 1.25-µm stack and 78 for the 2.25-µm stack. This means that the usable range of grey levels that would be transferred into the substrate was not the theoretical 256, but only 102 for the 1.25-µm stack or 158 for the 2.25-µm stack. The profilometry also revealed a slight selectivity in the etch rates of the substrate and the resist (Fig. 10). The ratio of PZT etch rate to resist was 1.5:1; i.e., the resist height had to be 1.5 times less than the desired height of the structure. This information was used to modify the design such that any feature that exposed an intermediate electrode layer was written with the experimentally determined grey level corresponding to the height position of that electrode in the stack.

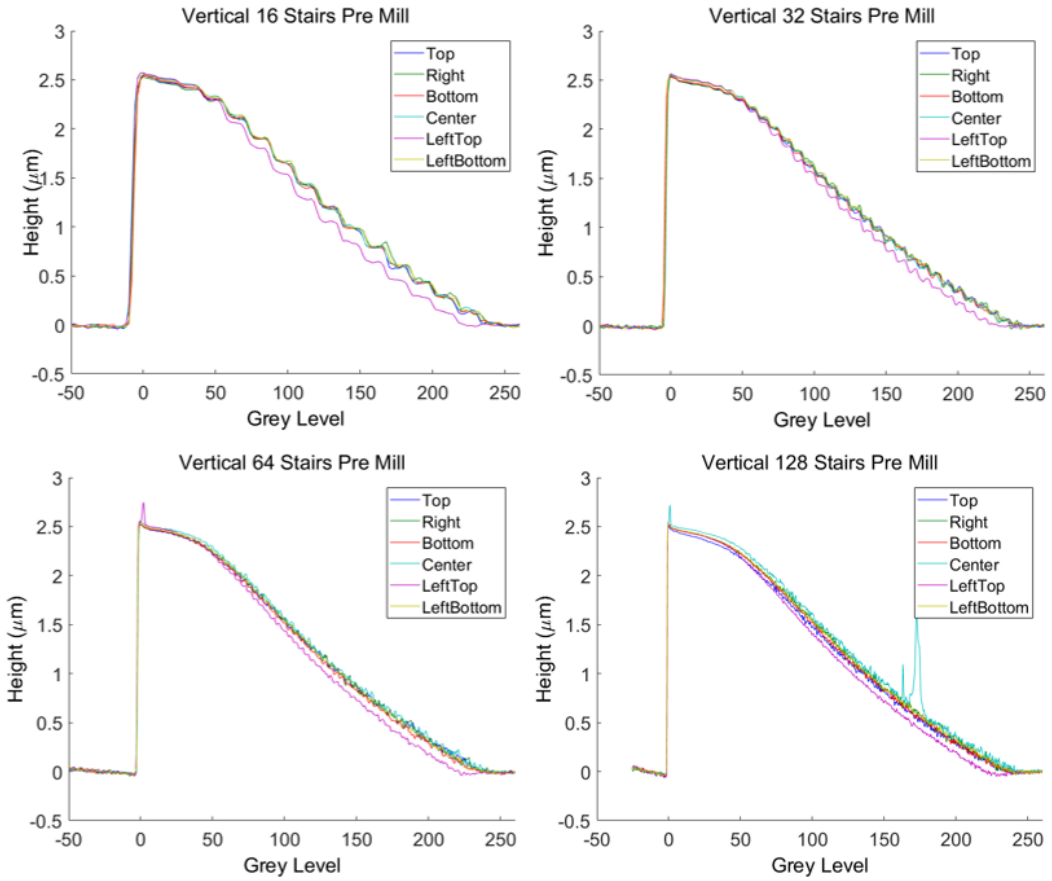


Fig. 10 Optimized resist profiles showing cross-wafer variation of photoresist height and resolution of greyscale lithography process with Heidleburg DWL 200. Note that each grey level step is 20 µm wide; therefore, horizontal scale is not the same for each plot.

3.5 Photoresist Roughness

Exposing an entire 6-inch wafer took 4.5 h and the single-ion mill etch per wafer took between 2 and 4 h. Though lengthier than an individual exposure and ion mill for the binary resist process, this is a significant time savings over the multi-mask, multi-etch process and precludes the potential for misalignment between layers. Roughness of grey levels in the resist was an issue, however. Traditional binary photolithography produces smooth, straight edges, while the greyscale exposure creates roughness in the photoresist as seen in the photoresist ramp in Fig. 11. This is a characteristic of the high-contrast nature of AZ5214 photoresist, which makes it extremely susceptible to minor variations in DWL laser intensity. In fact, as shown in Figs. 10 and 12, the stair patterns are not linear across the entire grey level spectrum. Roughly the upper 75 and lower 75 grey levels follow a nonlinear curve, which is very similar to the contrast curve of standard photoresist.[8] The degree of non-linearity in future work might be reduced by using a lower contrast photoresist.

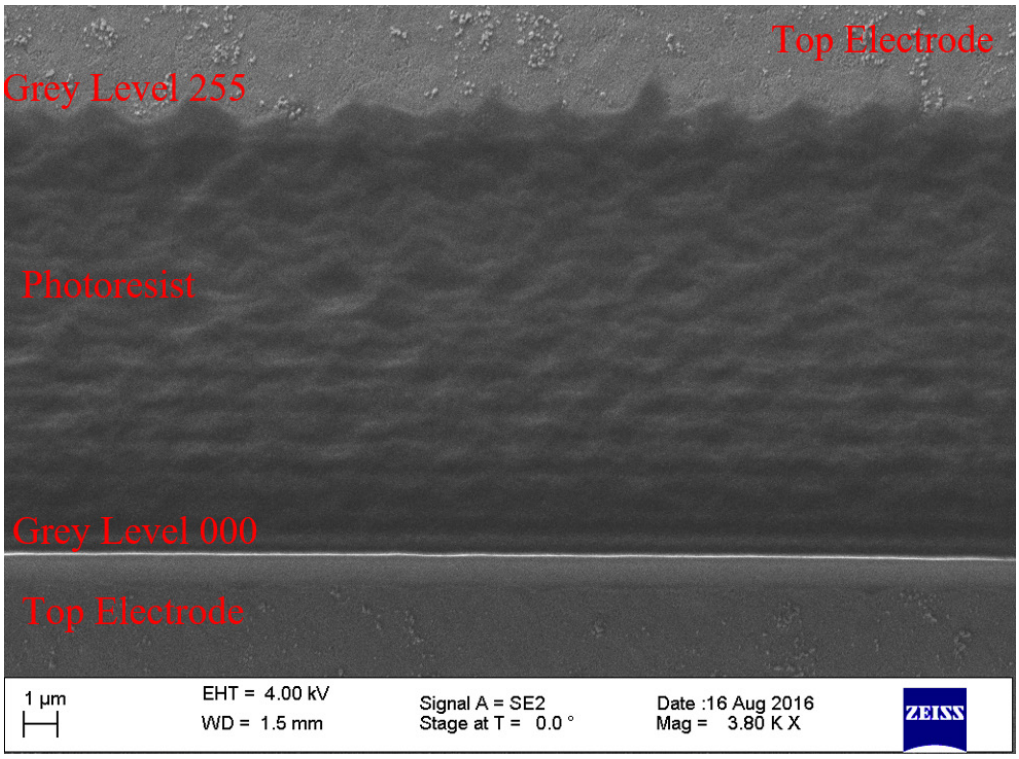


Fig. 11 SEM of photoresist ramp showing how resist is roughened after exposure. Grey level 000 corresponds to zero exposure; grey level 255 is full exposure.

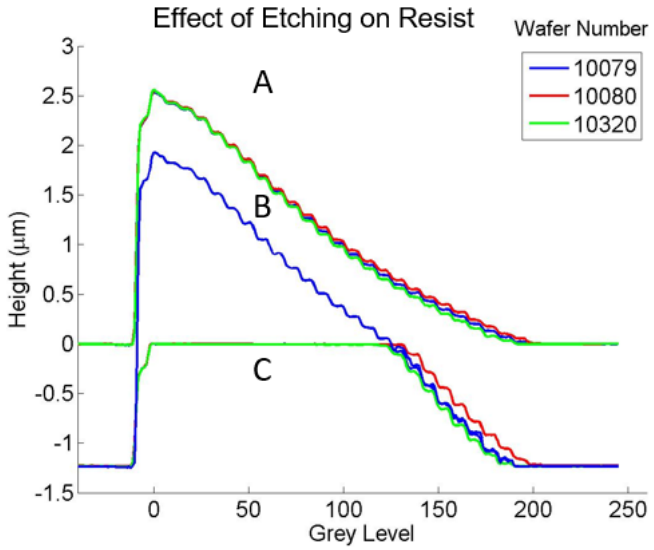


Fig. 12 Staircase profiles of the a) resist before etch, b) etched resist and substrate before removing resist, and c) the substrate after etch (c).

The exact surface profile of the photoresist is transferred into the substrate, which causes uncertainty during subsequent micromachining. A given resist step can have

as much as ±50 nm of surface roughness, while stylus profilometry (Fig. 10) reveals that resist height can vary over 100 nm across a wafer after development. These two errors combine to produce a final variation of possibly over 300 nm in resist thickness for a given photoresist level across a wafer. This poses a problem, because the buried electrodes used in this research are only 50 nm thick, while the PZT films used in this work were 250 nm thick, leaving little room for error. In other words, if grey levels are not properly chosen, then it is possible to expose two successive electrodes by ion milling (Fig. 13). This can result in unwanted electrical shorting of those two electrodes during subsequent metallization. It is possible for lower contrast photoresist to reduce the sensitivity of the resist to small fluctuations in laser intensity and increase the resolution of the greyscale lithography process. However, another solution is to under-mill the structure, leaving PZT on top of the desired electrode, protecting it. The PZT can then be wet-etched away, leaving a pristine electrode (Fig. 14).

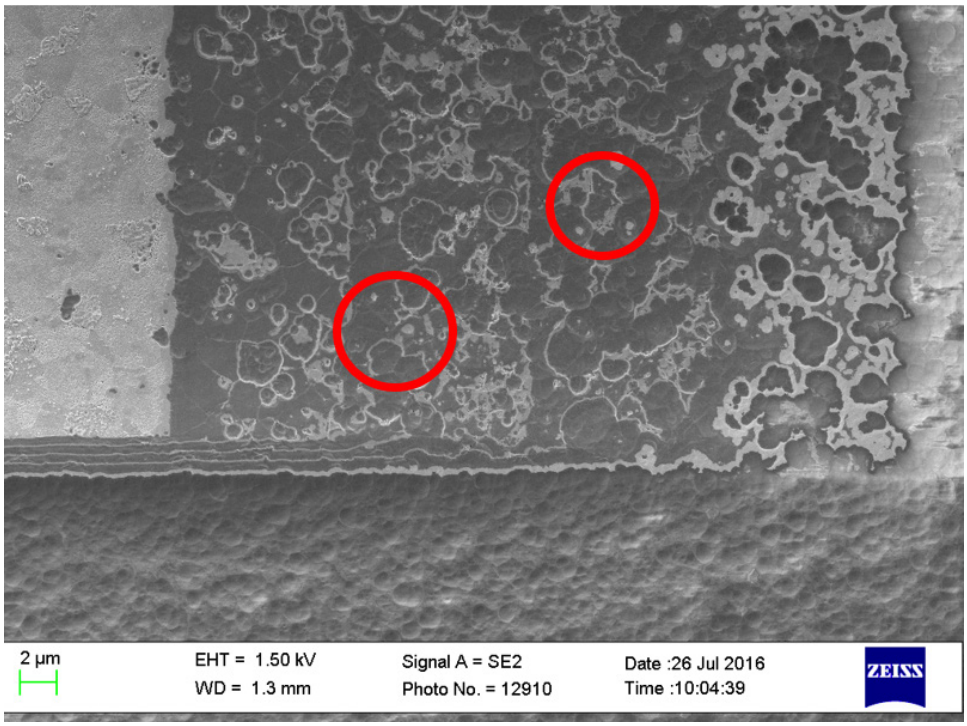


Fig. 13 SEM showing regions where photoresist roughness has led to exposure of multiple electrodes in the same location. This can lead to electrical shorts later in the fabrication process.

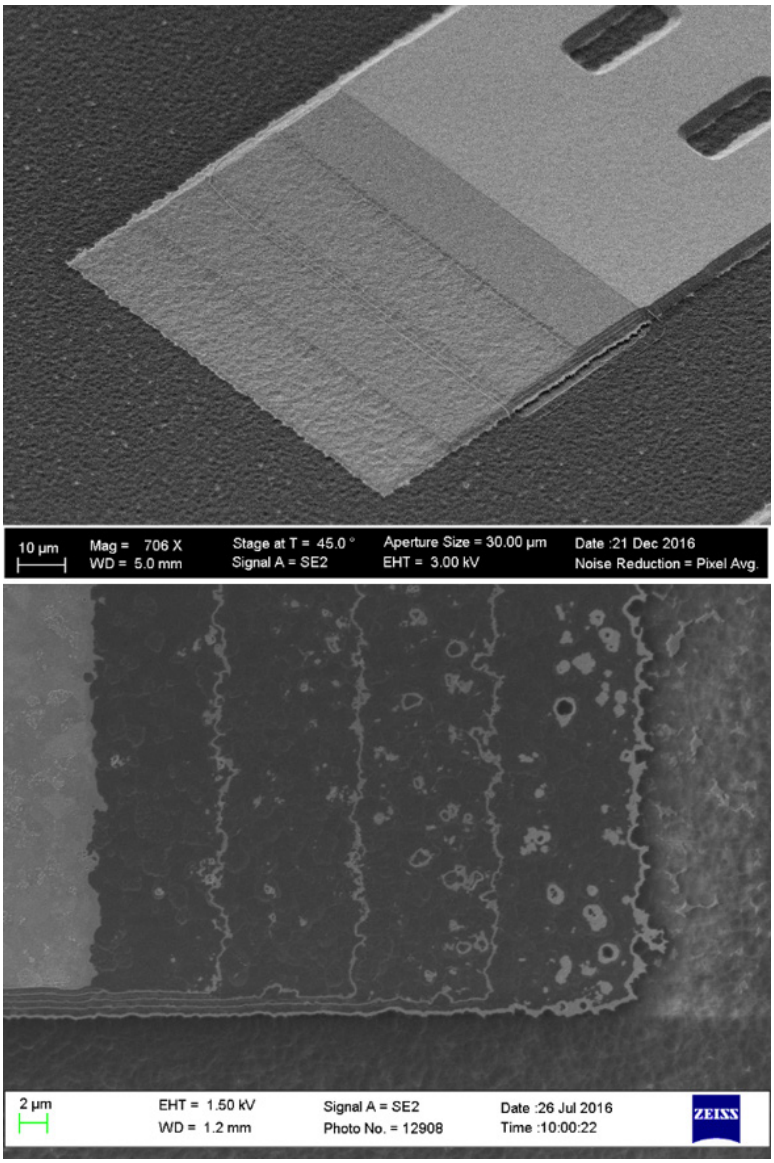


Fig. 14 Ion milled staircase pattern in 0.5 µm (left) nd 0.25 µm (right) thick PZT layers. PZT remains over each electrode by targeting the grey level corresponding to just below the next electrode up in the stack. This protects the desired electrode from being ion milled, leaving PZT which can be removed with a quick wet etch.

4. Conclusion

This technical report demonstrates the successful use of greyscale lithography to transfer tiered and sloped structures into a PZT stack using a single ion mill etch, and should serve as a resource for the characterization of other resist thicknesses. The rehydration of the resist and the focus of the laser beam were the most important process variables, although the focus could not entirely alleviate the stripe line issues. Specific adjustments can be made to accommodate the error in

the lithography process, such as placing electrodes inside a single stripe line and using a longer ramp to create more distance between exposed electrodes. This decreases the likelihood of shorting a device when it makes contact with the electrodes in subsequent microprocessing steps, which could result from the uneven edges between grey levels. Stylus profilometry was the most important analysis tool because it measured the usable grey levels that neither washed out during development nor remained in the excess resist after etching. It also provided information on the selectivity of the ion mill, which was necessary for precision in design.

Future work will create multilayer PZT devices using the greyscale lithography process and evaluate higher capacitance densities, bidirectional actuation, and increased control of physical displacement that are theoretically possible with this technique. Another application to investigate is the creation of tapered sidewalls for routing lithographically patterned signal lines over large step heights, as a potential replacement for air bridges. Although this process for the optimization of greyscale lithography must be repeated if any changes are made to the substrate identity or to the resist thickness, due to differences in reflection and absorbance of the laser beam. However, the successful application of this technique will significantly reduce the time, number of masks, and fabrication steps previously required to create multilayer PZT MEMS devices.

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List of Symbols, Abbreviations, and Acronyms

ARL	US Army Research Laboratory
CAD	computer-aided design
DWL	direct write laser
DWLG	DWL greyscale
HEBS	high energy beam sensitive
IrO2	iridium oxide
MEMS	microelectromechanical systems
Pt	platinum
PZT	lead zirconate titanate
RF	radio frequency
SEM	scanning electron microscope
Si	silicon
UV	ultraviolet

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