# 16 Element 1GHz Input 4 Simultaneous Beam 100MHz Bandwidth Digital Beamformer in 40nm CMOS

Michael Flynn, Sunmin Jang, Jaehun Jeong and Rundao Lu
Electrical Engineering and Computer Science
University of Michigan
Ann Arbor, MI 48109

***Abstract*— A 16 element, 1GHz IF input, digital beamformer (DBF) generates four independent simultaneous beams, with 100MHz bandwidth. DBF has several advantages over analog beamforming, including higher accuracy and multiple beam generation however, single-chip DBF has been limited due to high power consumption and large die area. A new architecture combines efficient Continuous-Time Band-Pass Delta Sigma Modulators (CTBPDSMs) with Interleaved Bit-Stream Processing (IL-BSP) to save 80% of power and area. The measured SNR of the 16 array is 59.6dB SNR which corresponds to an 11.2dB array gain. The measured beam patterns are near ideal.**

***Keywords—Digital beamforming, ADC, bitstream processing continuation time bandpass ADC.***

## I. Introduction

Beamforming spatially filters a desired signal from interfering signals arriving from different directions. This is especially useful when the desired signal and interferer are close in frequency. Another advantage is that beamforming improves the SNR of the received signal by 3 dB for each doubling of the number of antenna elements. However, power consumption, area, and routing complexity are bottlenecks in the implementation of efficient beamforming systems. Beamforming introduces a time delay in each receive path to form a beam. For narrowband signals, this delay can be approximated as a phase shift. Digital beam forming (DBF) is more accurate, facilitates sophisticated beamforming operations (e.g. tapering) and supports multiple simultaneous beams. To enable an efficient implementation of DBF, in [1] we introduced a new DBF architecture based on continuous-time band-pass ΔΣ modulators (CTBPDSMs) and bit-stream processing (BSP). This paper reports on further work presented in [2] which doubles the number of elements to 16, increases the bandwidth to 100MHz and doubles the number of simultaneous beams.

## II. Bitstream Processing Beamforming

We combine bandpass continuous time sigma delta ADCs with bit-stream processing for efficient digital beamforming. Bistream Processing (BSP) performs Complex Weight Multiplication (CWM) in the digital domain for the highest accuracy and flexibility [1]. It supports multiple beams and performs advanced functions such as adaptive beamforming and array calibration. The Continuous-Time Band Pass Delta Sigma Modulator ADCs or CTBPDSMs in this work directly digitize a relatively high 1GHz IF from the antenna elements. Continuous-time (CT) operation relaxes op-amp bandwidth requirements and provides a resistive input, which is relatively easy to drive in a system. Furthermore, a CT modulator relaxes the receiver front-end filtering by providing implicit anti-alias filtering. BSP operates directly on the 5-level quantizer outputs of the modulators for efficiency and small die area.

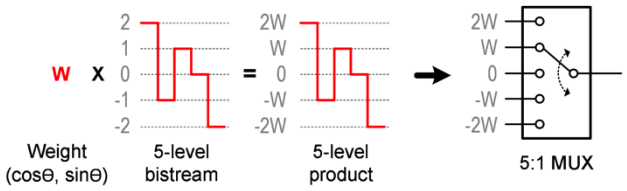


Fig. 1. Complex weight multiplication through bitstream processing

BSP replaces multipliers with simple MUXs for multiplication with a bit-stream as shown in Fig. 1. The five-level stream which consists of -2, -1, 0, +1, and +2. The bit-stream controls a MUX to multiply the input bit-stream by a multi-bit coefficient, W. When the value of the five-level stream is negative, the sign of W is inverted to implement multiplication by -1. When the value of the five-level stream is +2, W is left shifted to multiply by +2. When the value of the five-level stream is -2, both sign inversion and 1 bit left shift are performed to implement multiplication by -2. The sample rate of the CTBPDSMs is four times the 1GHz MHz IF to exploit simple MUX-based multiplication for direct down-conversion (DDC).

Fig. 2(a) summarizes the mathematical operations of DDC and phase shifting by complex weight multiplication (CWM). The I/Q outputs of the down-mixers are weighted, and combined to generate phase-shifted I/Q outputs. In our BSP approach, the digital outputs of the CTBPDSMs are directly processed before they are low-pass filtered and decimated to enable MUX-based implementation of DDC and phase shifting. As a result, eight MUXes (Fig. 2(b)) replace six multipliers and two adders (Fig. 2(a))

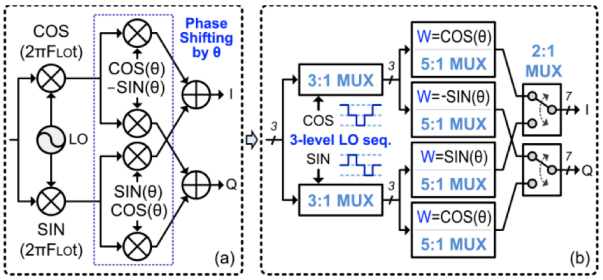


Fig. 2. (a) Mathematical operations of DDC and CWM, and (b) MUX-based BSP implementation ing

*Digital Down-Conversion with a 3:1 MUX:* Choosing a CTBPDSM center frequency of $f_s/4$ greatly simplifies the design of DDC [7], since the LO signals, cos[nπ/2] and sin[nπ/2], are now represented by only three values (-1, 0, and +1). DDC (Fig. 4(a)) is performed with a simple 3:1 MUX: pass-through, zero, and sign-change. Moreover, after multiplication by the 3-level LO signals (-1, 0, or +1), the down-mixed 5-level CTBPDSM outputs are still represented by five levels (-2, -1, 0, +1, and +2).

*Phase Shifting with a 5:1 MUX:* We expand the multiplier-less single-bit DSP, proposed more than two decades ago in [3] to 5-level streams. Since all five levels of the down-converted signals are powers of 2, only 1b left-shift (<<1) and sign-change are required for multiplication. The 5-level output of the down-mixer determines the 5:1 MUX operation on the stored weight (i.e. sign-change, zero, and 1b left-shift). In this way, a 5:1 MUX performs multiplication for phase shifting with programmable weights. The result of this multiplication is a 7b output. In addition, since the 3-level I/Q LO sequences are alternately zeroes, only the I or the Q output of the down-mixer is non-zero at any time. Therefore, in [1] the two 2:1 MUXes simply implement the two adders in Fig. 2(a). Overall, the four multipliers and two adders required for phase shifting are implemented with 6 MUXes, greatly reducing complexity

## III. Bitstream Processing Beamforming

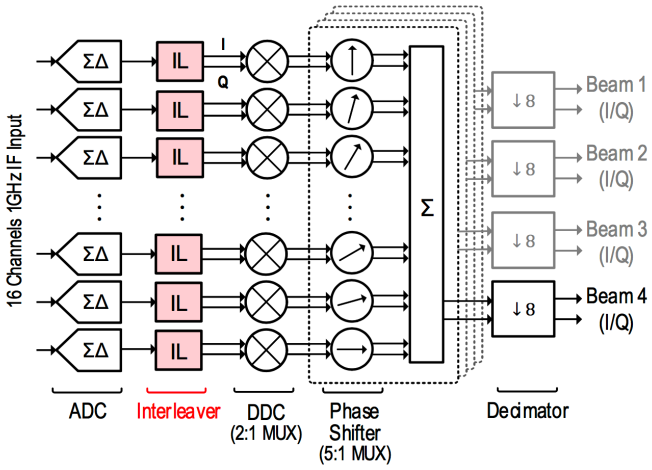


Fig. 3. Full beamforming system prototype.

A new Interleaved (IL) BSP architecture makes the 4GHz ADC sampling rate practical. A 4GHz ADC produces a 4GHz bitstream and logic operation at this speed is very challenging, especially for adders and decimators. Extensive clock buffering and pipelining might enable operation at high speed, but this consumes a lot of die area and power. Instead, IL-BSP takes advantage of the 0's in the sampled I/Q mixing signals to halve the digital clock rate without any loss in performance or accuracy. As shown in Fig. 4, the interleaving operation (IL) reduces the data rate from 4GHz to 2GHz. Direct Down Conversion (DDC) produces baseband I and Q streams. The outputs of CWN are summed and decimated to form each beam.

In the prototype, IL-BSP approach reduces die area and power consumption by 80% compared to conventional DSP. This is because BSP efficiently performs multiplication with multiplexers and reduces the number of decimators from the number of ADCs to the number of beams.

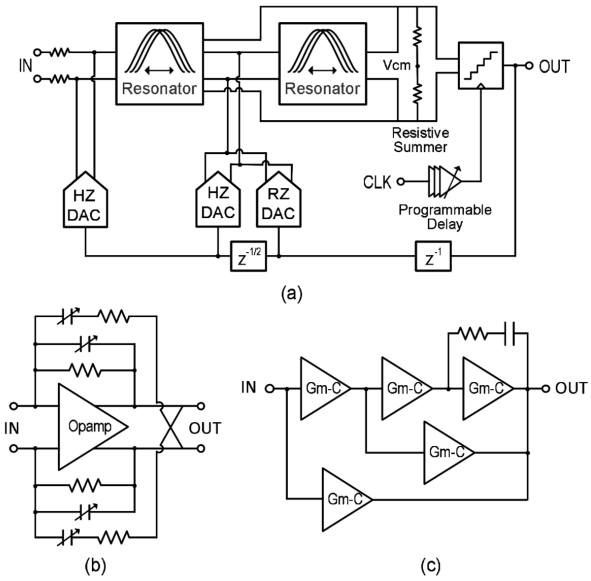


Fig. 4. (a) 4GS/s continuous time bandpass ADC, (b) single opamp resonator and (c) opamp.

The ADC area and power consumption have a huge bearing on the die area and power consumption of the entire beamformer. We tackle these at the system and the circuit level. At the system level, we take advantage of the signal processing gain of the large ADC array to improve the SNR of the overall beamformer. Since noise and random mismatch errors are uncorrelated, we benefit from a near-ideal 11.2dB array SNR improvement. The fourth-order CTBPDSM in Fig. 4 (a) uses compact single op-amp RC resonators instead of bulky LC-tank resonators to save power and area. The resonator center frequency is tuned with 3-bit trim capacitors (Fig. 4(b)). The op-amps use a 3-stage nested Gm-C structure which gives a good tradeoff between bandwidth and gain.

## IV. Prototype Device

The prototype 16 element beamformer is implemented in 40nm CMOS, packaged in an 88 lead QFN package and occupies a core area of 0.22mm$^2$. This area includes the 16 CTBPDSMs and 4-beam bit-stream DBF circuitry. A die photo is shown in Fig. 5.

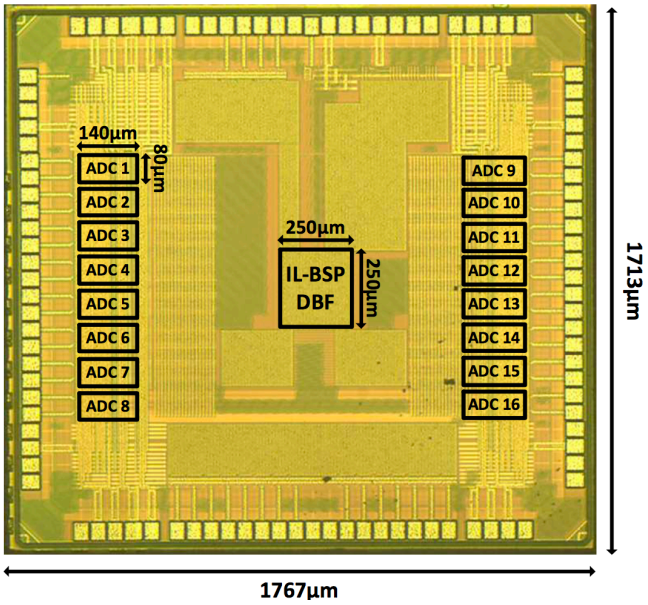


Fig. 5. Die photo of 16 elment, 4 beam beamformer

The average measured single ADC ENOB, for 16 ADCs in a beamformer IC, is 7.7 bits over 100MHz bandwidth. The overall 16 element array achieves a measured ENOB of 9.4 bits.

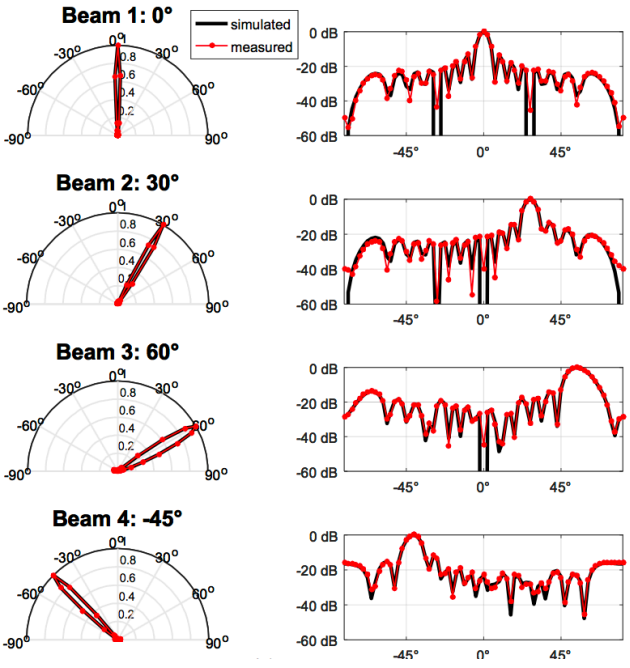


Fig. 6. Wired measurements of beam patterns.

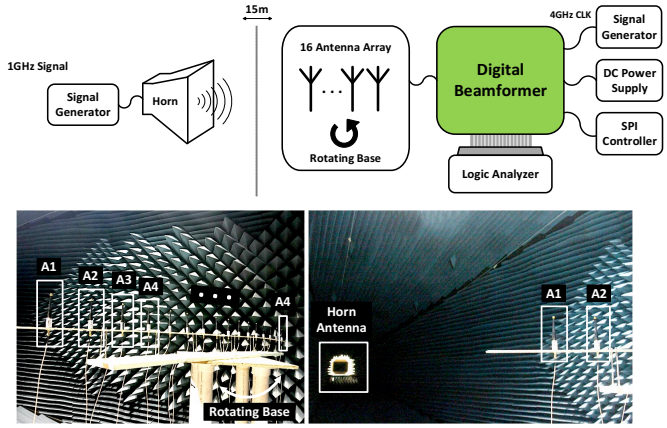


Fig. 7. Anechoic chamber test beam pattern measurement setup

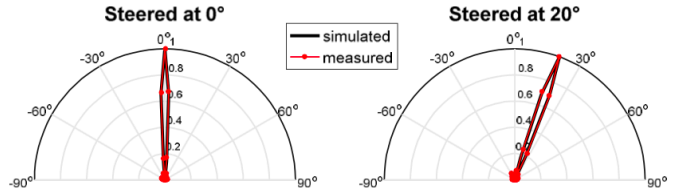


Fig. 8. Anechoic chamber measurements of beam patterns.

Beam patterns are measured with a benchtop setup and in an anechoic chamber. We use an array of Direct Digital Synthesize (DDS) ICs (Fig. 9) to generate the 16 test inputs to the prototype device. Fig. 6 shows the measurements of the four simultaneous beams. The measured beam patterns are near-ideal. Fig. 7 shows the anechoic chamber test setup and Fig. 8 shows the anechoic chamber measurements. In this test, a horn antenna provides a 1GHz RF input to a 16 element linear array. The antennae are connected directly to the ADC inputs without any RF stage. This shows the advantage of the CT input of the ADCs.

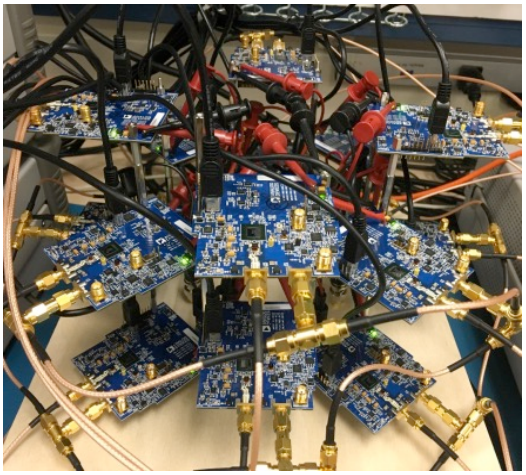

Fig. 9. 16 AD9164 DDS boards generate 16 synchronized 1GHz signals.

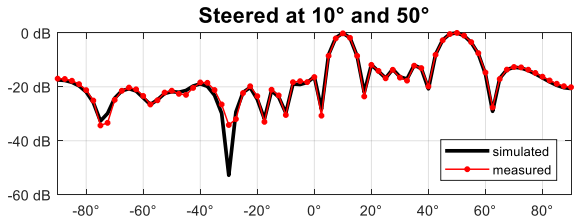


Fig. 10. Beam patterns with two main lobes (input frequency: 1.006GHz).

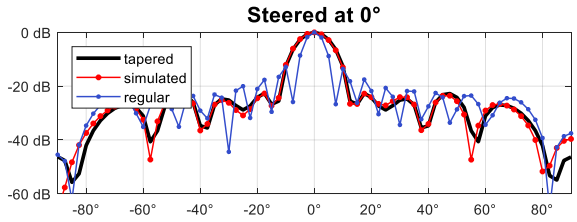


Fig. 11. Measured tapered beam patterns (input frequency: 1.006GHz).

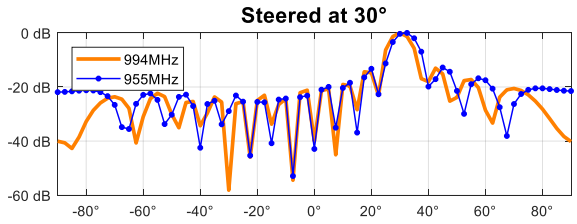


Fig. 12. Measured beam patterns over +/- 50MHz bandwidth (input frequency: 994MHz and 955MHz).

Digital beamforming is both flexible and accurate. Fig. 10 shows measurements of a beam pattern with two main lobes. Fig. 11 shows a measured tapered beam pattern. Fig. 12 shows beam patterns for two input frequencies that are separated by 50MHz. The small difference in the two patterns is due to squinting.

The prototype IC consumes a total of 312mW (16 CTBPDSMs: 244mW, DBF: 68mW). The 16 elements prototype has more elements and beams than any other published single-chip digital beamformer. The prototype DBF has a low Power/(Beams*Elements*Bandwidth) of 0.05mW/MHz, comparable to the best analog beamformers and a record low Area/(Element*Beam) of 0.003mm$^2$.

## V. Acknowledgments

This work was supported by DARPA ACT. We acknowledge the advice and support of Troy Olsson, Kyle Bunch, Ben Epstein and William Chappell of DARPA. The authors thank Berkeley Design Automation for simulation software, and Analog Devices for providing DDS devices. The authors thank Fred N. Buhler for his kind help.

## References

[1] J. Jeong, N. Collins and M. P. Flynn, "A 260 MHz IF Sampling Bit-Stream Processing Digital Beamformer With an Integrated Array of Continuous-Time Band-Pass Delta Sigma Modulators," in IEEE Journal of Solid-State Circuits, vol. 51, no. 5, pp. 1168-1176, May 2016.

[2] S. Jang, J. Jeong, R. Lu and M. P. Flynn, "A 16-element 4-beam 1GHz-IF 100MHz-bandwidth Interleaved Bit-Stream digital beamformer in 40nm CMOS," 2017 IEEE Radio Frequency Integrated Circuits Symposium (RFIC), Honolulu, HI, 2017, pp. 124-127.

[3] P. W. Wong, and R. M. Gray, "FIR filters with sigma-delta modulation encoding," *IEEE Transactions on Acoustics, Speech and Signal Processing*, Jun., 1990.