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14. ABSTRACT
The 2016 IEEE Lester Eastman Conference of High-Performance Devices was held at Lehigh University Aug. 2-4, 2016. The technical program includes 3 keynote speeches, 13 invited talks, 26 contributed talks (19 by students), and 25 posters (17 by students). The conference proceedings with 15 selected papers
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Report Title

Final Report: Research Area 4.1 Nano- and Bio-Electronics: Lester Eastman Conference on High-Performance Devices

ABSTRACT

The 2016 IEEE Lester Eastman Conference of High-Performance Devices was held at Lehigh University Aug. 2-4, 2016. The technical program includes 3 keynote speeches, 13 invited talks, 26 contributed talks (19 by students), and 25 posters (17 by students). The conference proceedings with 15 selected papers
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electronics, normally-off devices, bioinspired energy storage, wide-bandgap electronics), digital logic devices (low-power and energy-efficient logic switches, new materials, phenomena, and devices concepts for next-generation logic), optical emitters (infrared emitters for communication and sensing applications, lightemitting diodes for solid-state lighting and visible light-based communication, ultraviolet light-emitting diodes for disinfection and sensing, lasers, quantum-cascade lasers), photovoltaics and photodetectors (high-efficiency and flexible photovoltaics, photonic techniques for energy generation and transmission, high-quantum-efficiency photodetectors, avalanche photodiodes), bioelectronics and microelectromechanical systems (bioelectronics, chemical/biological sensors, micro-electromechanical devices and systems). There were approximately 90 participants, including 61 from the academia, 16 from the industry, and 12 from the government. Among all the participants, there were 35 students and 17 women. Foreign participants include 8 from Japan, 2 from Korea, and one each from Germany, Greece, Sweden, Pakistan, and Vietnam.

Enter List of papers submitted or published that acknowledge ARO support from the start of the project to the date of this printing. List the papers, including journal references, in the following categories:

(a) Papers published in peer-reviewed journals (N/A for none)

Received Paper

TOTAL:

Number of Papers published in peer-reviewed journals:

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Received Paper

TOTAL:

Number of Papers published in non peer-reviewed journals:

(c) Presentations

Number of Presentations: 0.00

Non Peer-Reviewed Conference Proceeding publications (other than abstracts):

Received Paper

TOTAL:

Number of Non Peer-Reviewed Conference Proceeding publications (other than abstracts):

Peer-Reviewed Conference Proceeding publications (other than abstracts):

Received Paper

TOTAL:

Number of Peer-Reviewed Conference Proceeding publications (other than abstracts):

(d) Manuscripts

Received Paper

TOTAL:

Number of Manuscripts:

Books

Received		Book
06/02/2017	1.00	Jonathan Felbinger. , Piscataway, New Jersey: IEEE Xplore, (2016)

TOTAL: **1**

Received		Book Chapter

TOTAL:

Patents Submitted

Patents Awarded

Awards

Graduate Students

NAME	PERCENT_SUPPORTED

FTE Equivalent:
Total Number:

Names of Post Doctorates

NAME	PERCENT_SUPPORTED

FTE Equivalent:
Total Number:

Names of Faculty Supported

NAME	PERCENT_SUPPORTED	National Academy Member
James Hwang	0.00	
FTE Equivalent:	**0.00**	
Total Number:	**1**	

Names of Under Graduate students supported

NAME	PERCENT_SUPPORTED
FTE Equivalent:	
Total Number:	

Student Metrics

This section only applies to graduating undergraduates supported by this agreement in this reporting period

The number of undergraduates funded by this agreement who graduated during this period: 0.00

The number of undergraduates funded by this agreement who graduated during this period with a degree in science, mathematics, engineering, or technology fields:..... 0.00

The number of undergraduates funded by your agreement who graduated during this period and will continue to pursue a graduate or Ph.D. degree in science, mathematics, engineering, or technology fields:..... 0.00

Number of graduating undergraduates who achieved a 3.5 GPA to 4.0 (4.0 max scale):..... 0.00

Number of graduating undergraduates funded by a DoD funded Center of Excellence grant for Education, Research and Engineering:..... 0.00

The number of undergraduates funded by your agreement who graduated during this period and intend to work for the Department of Defense 0.00

The number of undergraduates funded by your agreement who graduated during this period and will receive scholarships or fellowships for further studies in science, mathematics, engineering or technology fields: 0.00

Names of Personnel receiving masters degrees

NAME
Total Number:

Names of personnel receiving PHDs

NAME
Total Number:

Names of other research staff

NAME	PERCENT_SUPPORTED
Anne Nierer	0.04
FTE Equivalent:	**0.04**
Total Number:	**1**

Sub Contractors (DD882)

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Scientific Progress

The conference was held at Lehigh University Aug. 2-4, 2016. The technical program includes 3 keynote speeches, 13 invited talks, 26 contributed talks (19 by students), and 25 posters (17 by students). The conference proceedings with 15 selected papers were published by IEEE through its Xplore online archive. Topics covered in the conference include high-frequency devices (high-frequency electronics, Schottky devices, Bloch-wave oscillators, vacuum electronics, high-frequency passive components), power switching and energy-efficient devices (high-power electronics, normally-off devices, bioinspired energy storage, wide-bandgap electronics), digital logic devices (low-power and energy-efficient logic switches, new materials, phenomena, and devices concepts for next-generation logic), optical emitters (infrared emitters for communication and sensing applications, light-emitting diodes for solid-state lighting and visible light-based communication, ultraviolet light-emitting diodes for disinfection and sensing, lasers, quantum-cascade lasers), photovoltaics and photodetectors (high- efficiency and flexible photovoltaics, photonic techniques for energy generation and transmission, high-quantum-efficiency photodetectors, avalanche photodiodes), bioelectronics and micro-electromechanical systems (bioelectronics, chemical/biological sensors, micro-electromechanical devices and systems).

There were approximately 90 participants, including 61 from the academia, 16 from the industry, and 12 from the government. Among all the participants, there were 35 students and 17 women. Foreign participants include 8 from Japan, 2 from Korea, and one each from Germany, Greece, Sweden, Pakistan, and Vietnam. Companies represented include Crystal IS, HRL Labs, Intel, IQE, Lehighton Electronics, Matheson, Northrop Grumman, Raytheon, Teledyne Scientific, Fujitsu (Japan), Toyoda Gosei (Japan), and COMSATS Institute (Pakistan). Government entities include Army Research Office, Army Research Lab, Office of Naval Research, Navel Research Lab, Department of Energy, National Renewable Energy Lab, Sandia National Lab, and National Institute of Information and Communication Technology (Japan).

During lunch on Aug. 2, an invited talk on “Recent Trends in US Patent Litigation” was given by a patent attorney. On the evening of the same day, a special event “Women in Engineering” was attended by approximately 10 men and 10 women. On Aug. 3, a keynote speech was given by a program manager from the Department of Energy on its R&D programs, including special programs for university-industry collaboration. Over the conference banquet on the same day, an invited talk was given on “The Rise and Fall of Bethlehem Steel – A High-Tech Company a Century Ago.”

The conference brought together leading scientists and engineers from academia, industry, and government who are at the frontiers of electronic device and circuit research and development, for cross-fertilization of different technologies. The conference provided an intimate, intensive, single-track, and multi-disciplinary environment, which is so unique that equivalent results cannot be obtained at regular meetings of professional societies or other major international conferences. The rapid pace of electronic technology evolution compels a merger of traditionally separated technical areas, including microwave power circuits, low-power digital electronics, optoelectronics, power switching, etc., which collectively have become the foundation of today's electronic technology.

The conference is based on highly interdisciplinary research involving physics, chemistry, materials science, mechanical engineering, and chemical engineering. The conference is of interest to those active in 1) aerospace, 2) bioengineering, 3) communication, networking and broadcast technologies, 4) components, circuits, devices and systems, 5) engineered materials, dielectrics and plasmas, 6) fields, waves and electromagnetics, 7) photonics and electro-optics, and 8) power, energy and industry applications.

The conference proceedings and list of participants are attached, including a group photo.

Technology Transfer

2016 Lester Eastman Conference on High Performance Devices (LEC)

Proceedings

2 - 4 August 2016

Lehigh University
Bethlehem, PA, USA

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0800	**REGISTRATION OPENS**
0830	**INTRODUCTION** – *Grace Xing, Siddharth Rajan, James Hwang* **WELCOME TO LEIGH** – *Fil Bartoli, Chair, ECE Department, Lehigh University*
0900	**KEYNOTE:** III-V Nanowire FETs on Si for RF Applications – *Lars-Erik Wernersson, Lund University, Sweden*
0945	**KEYNOTE:** The New World of Lighting: Solid-State Lighting and Beyond– *Jeff Tsao, Sandia National Laboratory*
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1145	Optimization of High-Speed CMOS Optical Modulators with Interleaved Junctions – *Dinis Cheian, Massachusetts Institute of Technology [STUDENT]*
1200	**LUNCH BUFFET–David Radulescu - Recent Trends in US Patent Litigation**

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1400	**INVITED:** Chemically and Mechanically Exfoliated MoS_2 for Electronic & Opto-electronic Devices – *Anupama Kaul, University of Texas, El Paso*
1430	Band Gap Engineering in GaN-Based Semiconductor with Dilute-Anion Incorporation for Visible Light Emitters – *Chee-Keong Tan, Lehigh University [STUDENT]*
1445	Room temperature CW operation of GaN-based VCSELs – *Kenjo Matsui, Meijo University [STUDENT]*
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1615	Polarization Induced Holes for Ultraviolet Emitting Devices – *Toshiki Yasuda, Meijo University [STUDENT]*
1630	Pseudomorphic LEDs on AlN Substrates Emitting at 235nm – *Leo Schowalter, Crystal IS, Inc.*
1700-1900	**POSTER SESSION AND RECEPTION**
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P2	Monte Carlo Modeling of Ultra-Fast Operating BDT based Logical Device – *Jean-François Millithaler, UMASS LOWELL*
P3	High Frequency N-Polar GaNPlanar MIS-HEMTs on Sapphire with High Breakdown and Low Dispersion – *Xun Zheng, University of California Santa Barbara [STUDENT]*
P4	Cross Sectional Observation of Slant Field Plates Integrated to InAls/InGaAs HEMTs – *Tomotaka Hosotani,* Research Institute of Electrical Communication, *Tohoku University [STUDENT]*
P5	Growth and Characterization of Single Crystalline InNGrown on GaNby RF Sputtering for Robust Schottky Contacts – *Vache Harotoonian, UC-Davis [STUDENT]*
P6	Full-wave Hydrodynamic Modeling of Terahertz Plasma-wave HEMT Emitters – *Shubhendu Bhardwaj, Electicaland Computer Engineering, The Ohio State University [STUDENT]*
P7	Power Gain at THz Frequencies Employing Grating-gate RTD-gated HEMTs – *Hugo Condori, University of Utah [STUDENT]*
P8	Uncertainty Quantification and the Role of Non-parabolicity in Shaping the Nature of the Electron Transport Processes within Zinc Oxide – *Stephen O'Leary, The University of British Columbia*
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P11	Single Junction GaAs Solar Cells Grown by Hydride Vapor Phase Epitaxy – *John Simon, NREL*
P12	Integration of Site-controlled InAs Quantum Dots in Nanowire Architectures Towards Building Efficient Data Networks – *Ayesha Jamil, COMSATS Institute of Information Technology*
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P20	Electrical Characterization of Atomic Layer Deposited SiO2/ß-Ga_2O_3 Interface – *Ke Zeng, Electrical Engineering Department, University at Buffalo (SUNY) [STUDENT]*
P21	Pulsed Power Evaluation and Simulation of High Voltage 4H-SiC PType SGTOs – *Aderinto Ogunniyi, U.S. Army Research Laboratory [STUDENT]*
P22	Thermal Breakdown of III-N HEMTs on different substrates – *Michael Shur, Rensselaer Polytechnic Institute [STUDENT]*
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WEDNESDAY, AUGUST 3

MORNING: Room 101 STEP Building
DIGITAL AND BIO ELECTRONICS – WedAM
Chairs: *Shriram Shivaraman and James Hwang*

0800	**REGISTRATION OPENS**
0830	**INVITED:** Negative Capacitance Transistors – *Sayeef Salahuddin, UC Berkeley*
0900	**INVITED:** New Materials to Push the Limits of Moore's Law – *Tomás Palacios, MIT*
0930	Overcoming Heterogeneity, Alignment, and Contact Challenges to Realize High-Conductance Carbon Nanotube Array Field-Effect Transistors – *Michael Arnold, University of Wisconsin-Madison*
0945	Experimental approach for feasibility of superlattice FET – *Yasuyuki Miyamoto, Tokyo Tech*
1000	**BREAK**
1030	**INVITED:** Thin-Film Transistors for Flat-Panel Display Backplanes – *John Wager, Oregon State University*
1100	Low-Temperature Characteristics of $In_{0.7}Ga_{0.3}As$ PHEMTs – *Dae-Hyun Kim, Kyungpook National University, [STUDENT]*
1115	Preliminary Results for Broadband Electrical Detection of Bacteria – *X. Du, Lehigh University*
1130	Solution Dispersed 2D Layered Materials for in vivo Biosensing Applications – *Ridwan Hossain, University of Texas El Paso [STUDENT]*
1200	**LUNCH BUFFET**

WEDNESDAY, AUGUST 3

AFTERNOON Room 101 STEP Building **POWER DEVICES** – Session WedPM Chairs: *Rongming Chu and Travis Anderson*	
1300	**INVITED:** Electrical and Thermal Properties of Field-Plated Ga_2O_3 MOSFETs with High Breakdown Voltage – *Man-Hoi Wong, National Institute of Communication Technology, Japan*
1330	**INVITED:** Diamond: an Ultra Wide Bandgap Semiconductor for Power Electronics and Energy Conversion – *Robert Nemanich, Arizona State University*
1400	Diamond Based Schottky PIN Diodes with Breakdown Voltage > 750V – *Maitreya Datta, Arizona State University [STUDENT]*
1415	Towards the High Voltage Operating Potential of ß-Ga_2O_3 MOSFETs – *Neil Moser, George Mason University [STUDENT]*
1430	Effect of Carrier Lifetime Enhancement on the Performance of Ultra-High Voltage 4H-SiC PiN Diodes – *Sauvik Chowdhury, Rensselaer Polytechnic Institute [STUDENT]*
1445	**BREAK**
1515	**INVITED:** Current Status of Vertical GaN Power Devices on GaN Substrates – *Toru Oka, Toyoda Gosei, Japan*
1545	Comparison between GaNtrench MOSFETs with $(11\bar{2}0)$ a-plane and $(10\bar{1}0)$ m-plane sidewalls – *Chirag Gupta, University of California Santa Barbara [STUDENT]*
1600	Experimental Realization of GaN PolarMOSH: SiC versus GaN substrates – *Mingda Zhu, Cornell University [STUDENT]*
1615	Heterostructure-Engineered Ohmics-based UBWG Al0.75Ga0.25N Channel MISFET – *Sanyam Bajaj The Ohio State University [STUDENT]*
1630	Device Characteristics of AlN/Al0.85Ga0.15N High Electron Mobility Transistor with Regrown Ohmic Contact – *Albert Baca, Sandia National Laboratories*
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THURSDAY, AUGUST 4

MORNING: Room 101 STEP Building **HIGH FREQUENCY DEVICES** – ThuAM Chairs: *Keisuke Shinohara and Yasuki Miyamoto*	
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0830	**INVITED:** Demonstration of Amplifier Circuit Gain at 1THz with 25nm InP HEMT TMIC Process – *Gerry Mei, Northrop Grumman*
0900	**INVITED:** InAlGaN/GaN-HEMT Device Technologies for W-band High-Power Amplifier – *Kozo Makiyama, Fujitsu*
0930	Effect of Gate Sidewall Capacitance on N-Polar GaN Cap MISHEMT Performance – *Steven Wienecke, University of California - Santa Barbara [STUDENT]*
0945	Current Gain Above 10 in III-Nitride Tunneling Hot Electron Transistor – *Zhichao Yang, The Ohio State University [STUDENT]*
1000	Towards AlN/SiC platform high performance GaN QW HEMTs – *SM Islam, Cornell University*
1015	First Observation of Repeatable Room Temperature Negative Differential Resistance in GaN Resonant Tunneling Diodes – *Jimy Encomendero, Cornell University [STUDENT]*
1030	**BREAK**
1100	**INVITED:** The European DOTSEVEN (0.7 THz SiGe HBT) project: Technology, Modeling and Applications – *Micheal Schroter, Technical University Dresden*
1130	Plasmonic Detection of Short Terahertz Pulses – *Michael Shur, Rensselaer Polytechnic Institute*
1145	Low-dispersion 180° Phase Shifter Using Two Synchronized MEMS Switches – *Vahid Gholizadeh, Lehigh University [STUDENT]*
1200	$BaSnO_3$ Based Transistors for High Frequency Applications – *Zhanbo Xia, The Ohio State University [STUDENT]*
1215-0130	**LUNCH BUFFET - AWARD ANNOUNCEMENTS, CONFERENCE CLOSING REMARKS**

Preface

Professor Lester Fuess Eastman (1928–2013) helped to build an extensive, global community of scientists and engineers studying and developing compound semiconductor materials, devices, and circuits [1–2]. Following service in the Navy as a radar specialist, he returned to upstate New York and earned his B.S. ('53), M.S. ('55), and Ph.D. ('57) degrees at Cornell University, and subsequently joined the engineering faculty. He recognized the promise of semiconductor materials and devices for microwave applications and undertook pioneering study and early commercialization of compound semiconductor devices, including supplying GaAs distress beacons for downed pilots. In 1965, he organized the first annual, informal Conference on Active Microwave Effects in Bulk Semiconductors in New York City (as Ithaca is not known for its winter tourism) and, in 1967, served as Chairman of the First Cornell Biennial Conference on Engineering Applications of Electronic Phenomena: High Frequency Generation and Amplification [3]. The scope of this biennial conference – and his group's research – broadened over the years to incorporate optoelectronic and power devices and their applications. The name of the conference also evolved to reflect IEEE EDS sponsorship, beginning in 1981, to the eponymous IEEE Lester Eastman Conference on High Performance Devices in 2002, out of recognition for his seminal contributions to the field.

Presentation and dissemination of new ideas and state of the art results have remained the hallmark of this conference. The intent of the proceedings has shifted, in recent years, from a comprehensive record toward rapid publication [4–14]. Key discoveries have been unveiled at this conference, including Prof. Eastman's pioneering work on ballistic transport [15]. Throughout his career, he anticipated pivotal shifts from vacuum tubes to solid-state microwave electronics and subsequently to the nitride materials family. In this spirit, this year's conference featured mm-wave, THz, IR, and UV sources and detectors; biological sensors; beyond-CMOS logic devices; and wide bandgap power switches.

To many, Prof. Eastman was instantly recognizable: sitting in the front row of the lecture hall, an imposing figure with a legal pad. Among a career of accolades, he was named a Fellow of the IEEE in 1969, appointed the John L. Given Foundation Chair Professor of Engineering in 1985, and elected to the National Academy of Engineering in 1986. As an advisor, Les conveyed his curiosity and enthusiasm, shared his love of culture, and instilled a nugget of his vast intuition for physical phenomena. He left an indelible impression on those given the pleasure to collaborate with him, study under his tutelage, discuss the latest results at a workshop, or just sign the visitors' register in his office.

Innovation was a theme throughout this year's conference. At a lunchtime seminar, David Radulescu presented on trends in optoelectronic patent litigation. During the conference dinner on the former research campus of the Bethlehem Steel Corporation, once the second largest steel producer and largest shipbuilder in the world, a duo of former employees presented artful pictures and anecdotes from the company's rise, many projects and capabilities, ultimate failure to innovate, and demise after a century in business. The Local Chair, Prof. Hwang, picked up the story of how the city, failing company, and Lehigh University worked together to incubate new technologies and industries. Prof. Eastman, who took great interest in the life and corporate endeavors of distant relative George Eastman, would have enjoyed this narrative. From the mountaintop research campus turned technology incubator, participants could see the again-vibrant downtown and, through the clear skies, to the far side of the verdant Lehigh Valley.

Jonathan Felbinger
Raytheon Company
IEEE Senior Member & "Eastman index" #124

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2016 Lester Eastman Conference on High Performance Devices (LEC)

Awards

Prof. Eastman actively encouraged his students to present at conferences to gain exposure and win recognition. In this spirit, student presenters received travel support and the Best Student Paper and Best Poster were awarded at the conclusion of the 2016 Lester Eastman Conference on High Performance Devices.

Best Student Paper Award:

Effect of Gate Sidewall Capacitance on N-Polar GaN Cap MISHEMT Performance

S. Wienecke, B. Romanczyk, M. Guidry, H. Li, E. Ahmadi, K. Hestroffer, X. Zheng, S. Keller, U. K. Mishra
Department of Electrical and Computer Engineering, University of California, Santa Barbara, CA 93106
Tel: (805) 893-8956, Fax: (805) 893-8714, Email: swienecke@engineering.ucsb.edu

Best Poster Award:

Single Junction GaAs Solar Cells Grown by Hydride Vapor Phase Epitaxy

J. Simon, K.L. Schulte, N. Jain, M. Young, M.R. Young, D.L. Young, A.J. Ptak
National Renewable Energy Laboratory, Golden, CO 80401
Tel: 303-275-3898, e-mail: john.simon@nrel.gov

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Optimization of High-Speed CMOS Optical Modulators with Interleaved Junctions

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***Abstract*— Modern microprocessors performance is often limited by the data delivery rate through conventional electrical interconnects. Optical interconnects offer a viable path to relieving this interconnect bottleneck and significantly increasing the capability of modern computers and datacenters. Here, we present a model and experimental validation for the high-speed performance of CMOS optical modulators using interleaved junctions. This model is benchmarked against two generation of CMOS modulators. The model uncovers the underlying bandwidth limitations of existing devices and suggests improvements that would enable 35 GHz optical modulators in microelectronics CMOS.**

Keyword— modulator; bandwidth; CMOS; photonics

I. Introduction

Advances in CMOS have enabled modern processors to operate at much faster speeds than electrical interconnects can deliver data [1]. Optical interconnects offer a viable path to realizing such high performance interconnects. Recently, the first microprocessor with integrated photonic interconnects was demonstrated [2]. This initial demonstration was for 2.5 Gbps links between a dual-core RISC V CPU and off-chip memory with a total of 15.6 pJ/bit energy consumption. Recently, the 45 nm photonic toolbox was updated with a 13 GHz modulator [3]. This modulator exploits a new geometry of interleaved junction— the T-Junction – for plasma effect modulation of the optical resonance in a silicon microdisk (Fig 1). The toolbox also contains a 32 GHz detector, thus the bandwidth bottleneck is still set by the modulator's performance [4].

Here, we present a model and experimental validation for the high-speed performance of CMOS optical modulators using interleaved T-Junctions. This model is benchmarked against two generations of CMOS modulators. The model uncovers the underlying bandwidth limitations of existing devices and suggests improvements that would enable 35 GHz optical modulators in microelectronics CMOS.

II. The T-Junction

A. The Interleaved Junction

The three junction geometries, typically used in modulator design, are: lateral, vertical, and interleaved junction. The lateral junction, with concentric rings of doped material, is difficult to contact in a ring modulator fabricated from a single layer of silicon where the optical mode will be in the immediate vicinity of the metal contacts, increasing the optical loss. The vertical junction manufacturing process is challenging due to the small thickness of the silicon layer (<100 nm) and the fact that SOI MOSFETs rely on lateral junctions. The interleaved junction is both easy to manufacture and contact in a microelectronics CMOS process. Moreover, the lithographic precision allows the interleaved junction to have a width smaller than the thickness of the silicon, thus the modulation efficiency can be increased beyond what the vertical junction has to offer. The interleaved junction is the most convenient junction design for native CMOS processes.

B. The T-Junction

An interleaved PN junction, as presented in [5], can be modeled using a distributed RC circuit. Since the modulators are operated in reverse bias, the dominating capacitance is the junction's depletion capacitance, C_{jun}. The dominant resistance, in our electrical model, is the radial resistance of the P and N spokes, $R_{n,p}$.

In a junction, C_{jun} plays two important roles. First, as mentioned above, C_{jun} is part of the RC product which

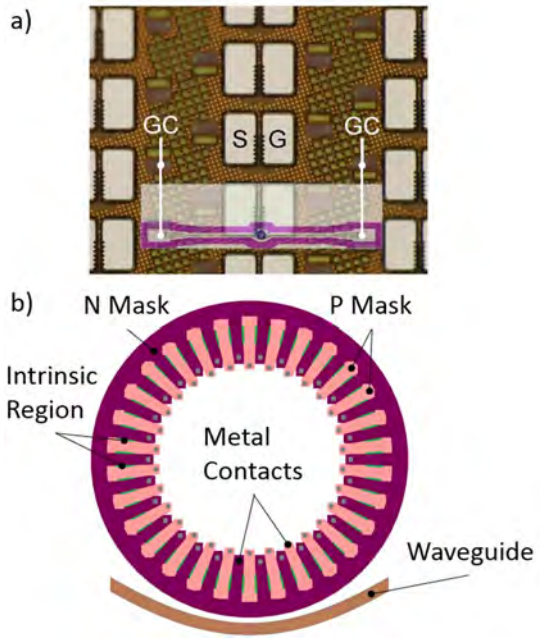

Fig. 1. a) A microscope image of the modulator with GC— grating couplers, S— signal pad, and G— ground pad. b) The modulator layout with N mask in purple, P mask in pink, intrinsic regions in green, metal contacts in grey, and waveguide in brown.

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determines the 3dB bandwidth of the modulator. However, C_{jun} also determines the strength of the optical modulation as measured by the Extinction Ratio (ER). The degree of refractive index variation for a given voltage swing induced by carrier density modulation is directly related to the depletion capacitance: $C_{jun} = dQ/dV$, where Q is the charge stored in the capacitor. Thus, it would appear that there is a fundamental trade-off between the ER and the bandwidth — a larger ER requires a larger C_{jun} and hence a smaller bandwidth.

We can decouple the two variables by realizing that the optical mode is not present throughout the volume of the silicon microdisk (Fig. 2a)). The mode travelling through the modulator is concentrated towards the outer rim in order to avoid overlap with the metal contacts on the inner rim. Therefore the capacitance located within the 0.9 μm from the metal contacts, where there is little optical field overlap, does not contribute to optical modulation.

The main idea behind the T-Junction design is to diminish the capacitance in the regions where the optical mode is not present. We place intrinsic regions between the P and N spokes, in order to diminish the capacitance that does not contribute to modulation (Fig. 2b)). The intrinsic regions will slightly decrease the width of the conducting spokes and thus increase the $R_{n,p}$. However, the decrease in C_{jun} will be greater than the increase in $R_{n,p}$, as long as width of the spoke is much larger than the depletion region, and the intrinsic region widths. This will increase the bandwidth, without decreasing the ER. The T-Junction also maximizes the capacitance in the regions where the optical mode is located. Finally, the T-junction allows us to increase the doping of the portion of the conducting spokes that do not overlap the optical mode.

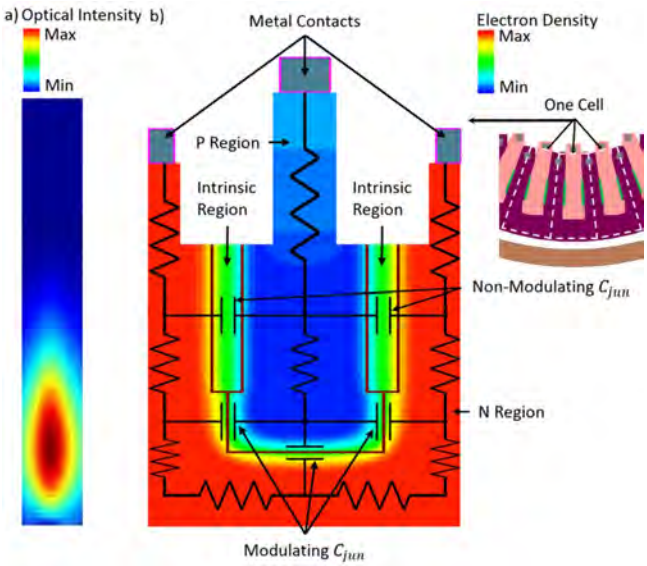

Fig. 2. The lengths of figures a) and b) are scaled identically. a) Cross section of the modulator. The optical mode is concentrated towards the outer rim of the modulator, away from the metal contacts on the top. b) Top view of a cell of the modulator. A snapshot of the electron density in the simulated device. The electrical schematics represents the equivalent RC circuit. The intrinsic regions help minimize the capacitance that does not contribute to the modulation.

III. Results and Discussion

Using the T-Junction concept, we have recently demonstrated the fastest modulator in an unmodified CMOS process ("zero-change" CMOS), with a bandwidth 5x higher than the previous PN junction [3], [5]. Next, we present the numerical and analytical models that have been developed to predict the behavior of the modulators. Sentaurus, a device simulator developed by Synopsys, was used to solve the transport equations. We have simulated only a cell of the whole PN ring, and imposed periodic boundary conditions on that cell, to recreate the behavior of the whole ring (Fig. 2b)). The model correctly predicts the 3dB bandwidth of the previous generation of modulators, anticipating a 3.8 GHz bandwidth versus the measured 2.5 GHz in [5]. The model also, correctly predicts the behavior of the T-Junction modulator, including the optimal operating voltage in order to achieve the highest bandwidth (Fig. 3a)).

The optimal voltage occurs when the decrease in capacitance with reverse bias, cannot compensate for the increase in resistance of the spoke. The conducting spokes begin to pinch-off as the depletion widths increase with bias (Fig. 3b)).

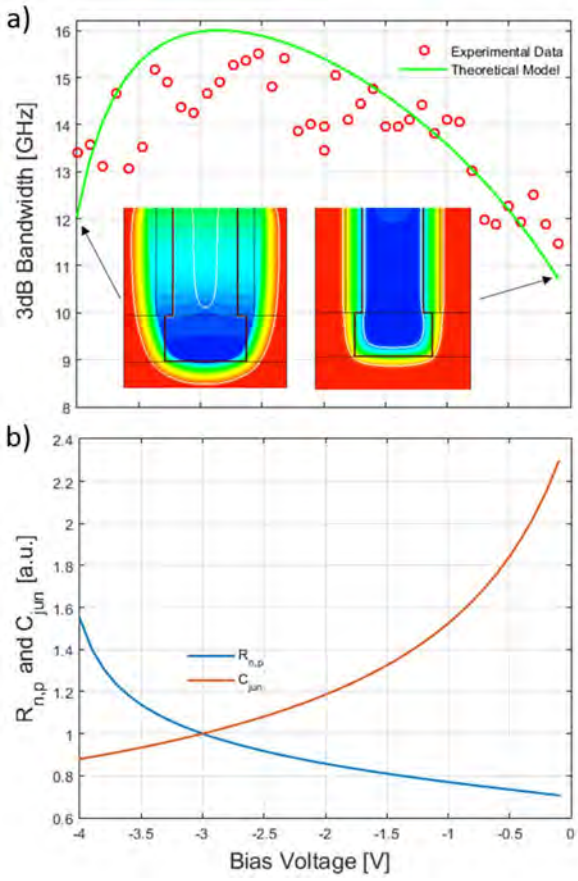

Fig. 3. a) The theoretical model predicts the experimental behavior. The model was also able to predict the optimal voltage of operation. The white outlines on the devices represent the boundaries of the depletion regions. b) With higher reverse bias, the decrease in C_{jun} cannot compensate for the increase in $R_{n,p}$. The spokes begin to pinch-off as the depletion widths increase with bias.

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Once we have verified the accuracy of our models for the T-Junction modulator, we proceed to optimizing the geometry and doping of the junction, to further increase the speed. We have optimized over doping— the conclusion being that the larger the doping, the faster the device. If we neglect the changes in mobility, the RC product of the modulator would decrease as $1/\sqrt{N}$. The decrease of the RC product with doping, is verified by the models, even if we take the mobility change into consideration (Fig. 4). The higher the doping— the faster the device. The increase in doping is only limited by the amount of loss that we can tolerate.

We did not vary the radial length of the junctions because the length is constrained to separate the optical mode from the metal contacts along the inner rim (Fig. 2a)). In all designs the length of the junction was kept at the minimum of 1.2 μm.

We optimized over the widths of the intrinsic, N, and P regions. Increasing the width of the N and P regions allows us to decrease the junction resistance along the length of the spoke. However, once the width is increased significantly, the resistances along the width of the junctions start to increase. Increasing the width of the intrinsic region will decrease the non-modulating capacitances but will, once again, increase the resistances along the width of the junction. Therefore, both the width of the junctions and the width of the intrinsic regions have an optimal point, which minimizes the RC product. The final design predicts a 3dB bandwidth above 35 GHz (Fig. 5).

There are several factors that limit us in achieving an even faster device. The doping cannot be increased arbitrarily because this would increase the optical loss in the ring. The set length of the junctions, the finite resistivity of the doped regions, and increase in lateral resistances set the limit on the T-Junction performance.

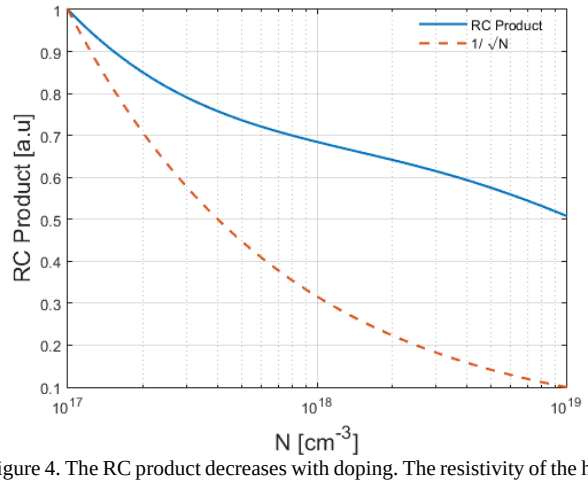

Figure 4. The RC product decreases with doping. The resistivity of the holes and electrons decreases faster than $\sqrt{N}$— the rate at which C_{jun} increases with doping. The higher the doping the faster the device, the downside of the increased doping is the increase in optical loss. In the plot above, the N and P doping have been assumed to be equal.

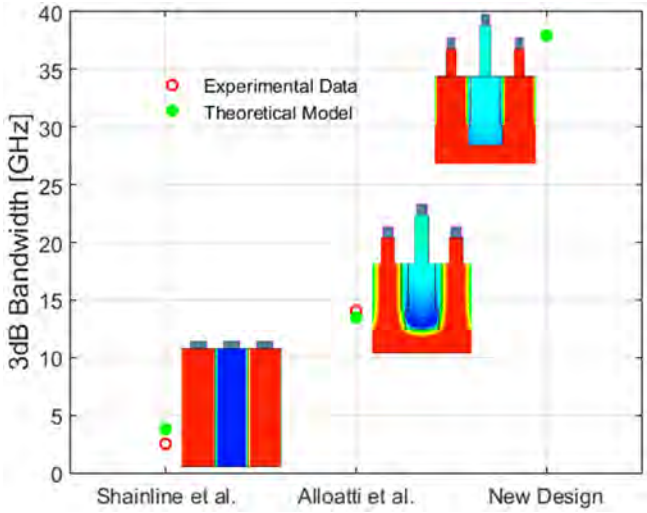

Figure 5. The theoretical model has been used to successfully predict the bandwidth of two generation of modulators, at 1V reverse bias. The new design promises to have a 3dB bandwidth exceeding 35 GHz.

IV. Conclusions

This work has focused on analyzing the T-Junction, and on optimizing its performance. The T-Junction is a new junction design that allows the designer to decouple the 3dB bandwidth and the ER. The T-Junction has demonstrated its superior bandwidth compared to other CMOS modulators.

In summary, we have created a model that successfully mimics the behavior of two generations of modulators. Using this model we further optimized the design parameters to obtain a modulator operating above 35 GHz.

Acknowledgement

We acknowledge support by DARPA POEM under award HR0011-11-C-0100 and contract HR0011-11-9-0009. The views expressed are those of the authors and do not reflect the official policy or position of the DoD or the U.S. Government.

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Chemically and Mechanically Exfoliated MoS_2 for Electronic & Opto-electronic Devices

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***Abstract*—Two-dimensional (2D) layered nanomaterials such as graphene and transition-metal dichalcogenides (TMDCs) have attracted tremendous attention over recent years due to their unique properties and potential for numerous applications. Here we have characterized the properties of chemically exfoliated 2D molybdenum disulphide (MoS_2) that was dispersed in organic solvents. Optical absorption spectra of the solution dispersions revealed the presence of excitonic peaks at characteristic energies. Besides electronic transport measurements on drop-cast samples, these dispersions were also used to form p-n junction devices on p-type Si substrates. At the same time, MoS_2 was also mechanically exfoliated from the bulk crystal and the flake was then placed onto pre-patterned electrodes using a visco-elastic stamping process. A few layer MoS_2 photodetector device was fabricated and characterized using a broadband white light source and transport was measured over a wide range of temperatures.**

Keywords—2D layered materials, MoS2, photodetectors, solution dispersion, chemical exfoliation, mechanical exfoliation

I. Introduction

The hexagonal honeycomb lattice of two-dimensional (2D) graphene represents the thinnest material we know of to date. At the same time, this membrane-like material is 5X stronger than steel owing to the strong in-plane sigma bonds. The sp^2 bonding of carbon atoms in graphitic carbon nanomaterials generally affords them exceptional materials properties, such as a high-charge-carrier mobility, high-thermal conductivity and excellent mechanical flexibility, which make them attractive for a range of applications [1-4]. It is interesting to note that fullerenes - the lowest dimensional form of carbon nanomaterials - were the first to be discovered amongst the graphitic carbon nanomaterial family by Kroto *et al.* [5] in 1985, followed by carbon nanotubes in 1991 by Iijima [6], while graphene remained elusive until recently despite being the basis for the other forms of carbon nanomaterials. Graphene exhibits a high mobility > 100,000 cm^2/V-s at room temperature and a high thermal conductivity of 5 x 10^3 W/m-K. It has an ultra-high current carrying capability ~ 1 x 10^9 A/cm^2. Due to its flexibility, strength, high conductivity, transparency and low cost, graphene has been proposed as a replacement for indium tin oxide for solar cells [7], and organic light emitting diodes, as well as in touch screens [8]. The large surface area to volume ratio of graphene suggests that it also has promise in ultra-capacitor applications [9].

Recently, layered 2D crystals of other materials similar to graphene have been realized which include insulating hexagonal-BN (band gap ~5.5 eV) and transition metal di-chalcogenides (TMDCs) such as metallic NbS_2 and semiconducting MoS_2. The TMDCs consist of hexagonal layers of metal M atoms sandwiched between two layers of chalcogen atoms X with stoichiometry MX_2 (e.g. for MoS_2, M = Mo, X = S).

One of the most widely explored non-graphene 2D layered material is MoS_2 where high-performance transistor devices have been constructed from monolayers of MoS_2. Besides high performance transistor devices, MoS_2 has been demonstrated in a wide ranging applications such as gas sensors, photovoltaics, photodetectors, and flexible electronics, given its interesting electronic, mechanical and optoelectronic properties. An important characteristic of MoS_2 is that its energy bandgap E_g varies as a function of the number of layers, showing indirect band gap characteristics with E_g ~ 1.2 eV in the bulk (valence band maximum at the Γ point) to direct band gap transition with E_g ~ 1.8 eV for monolayers (valence band maximum at K point). Excitonic effects have also been observed in MoS_2 and some other TMDC [10-12]. These intriguing characteristics of MoS_2 make it a promising candidate for electronics and optoelectronics applications. In this paper, we present characterization results on the optical and electronic properties of chemically exfoliated MoS_2, which have also been applied to p-n junction devices. We also present results on photodetectors formed using mechanically exfoliated MoS_2.

II. Solution-based Dispersions of MoS_2

A. Chemical Exfoliation of 2D MoS_2

Liquid phase exfoliation of MoS_2 was conducted in isopropanol-alcohol (IPA), IPA mixed with surfactant ethyl cellulose (EC) and stabilizer terpineol (T). The dispersions with various formulations were prepared in vials, as shown in Figure 1. Each vial had a density of 5 mg.mL^{-1} of MoS2 in powder form which was subsequently sonicated and centrifuged to yield solution S1 in IPA only, S2 solution in IPA and EC, and S3 solution in IPA, EC and T. The sonication time used was 297 min and centrifugation was conducted at 2000 r.p.m for 30 min. After forming the

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solutions, optical absorption spectroscopy was used to decipher the optical properties of the dispersions.

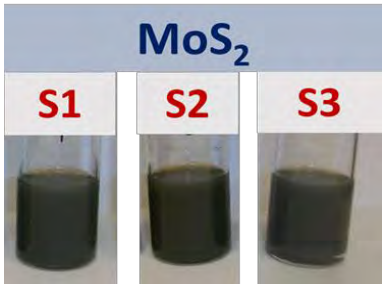

Figure 1. Vials S1, S2 and S3 are dispersions of MoS2 after sonication and centrifugation in the following: S1 in IPA only; S2 in IPA and EC; and S3 in IPA, EC and Terpineol.

B. Optical & Electronic Property Characterization

The optical absorption of the samples was measured using a CARY 5000 UV-visible-near IR spectrophotometer. The spectra obtained showed interesting signatures of potential excitonic behavior. To determine the optical properties of exfoliated MoS2 dispersed in solvents, drops of the solutions were cast onto a 1 x 1 inch glass slide. The selected drops taken at the top and the bottom of these solutions were dried at 100 °C to drive off the solvent. As reported recently by Backes *et al.* [13] centrifugation causes the particles to mass separate, where the thinnest and smallest flakes are likely to be at the top of the vial and the heavier flakes are at the bottom.

Here, we investigate the optical absorption characteristics for dispersions taken from the top and the bottom of the vial for solution S1 and S2, as shown in Figure 2. In solution S1 for the IPA solvent, two distinct absorbance peaks are observed at 1.8 eV and 2 eV, respectively at the top and the bottom of the vial. They correspond to the A and B exciton peaks [10]. The C exciton is more evident in the bottom of the solution around 2.7 eV (Fig. 2a-right).

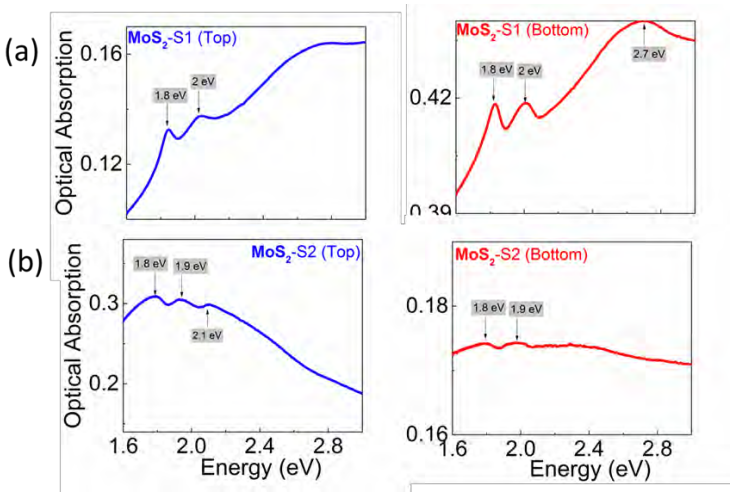

Figure 2. Optical absorption of MoS2 liquid exfoliation in (a) IPA solution taken at the top (left plot) and the bottom (right plot) and (b) IPA+EC solution retrieved at the top (left plot) and the bottom (right plot).

Sponsor: Air Force Office of Scientific Research (AFOSR).

In case of the IPA mixed with EC surfactant, optical absorbance A and B peaks appear at 1.8 eV and 1.9 eV at the top and the bottom of the solution and the C exciton is more distinct at the top of the solution around 2.1 eV (Fig. 2b-left). The comparison of the optical absorption characteristics in Fig. 2a and (b) shows the surfactant EC may suppress some of the excitonic characteristics of solution dispersed MoS_2.

To study the electronic transport of solution-dispersed MoS_2, two probe measurements were used to electrically contact the drop-cast MoS_2 on SiO2/Si substrates, where the samples were annealed at 400 °C for 30 min. The distance between the tungsten probe tips was ~ 500 μm. Figure 3 depicts the I-V characteristic of solution S3 up to 20 V at room temperature, where moderate current levels of up to 3 μA were measured at 20V. The transport shows a nonlinear behavior at low voltages (< 2 V) with an exponential conduction mechanism that could be attributed to thermoionic emission and/or tunneling effects in these MoS_2 flake ensembles.

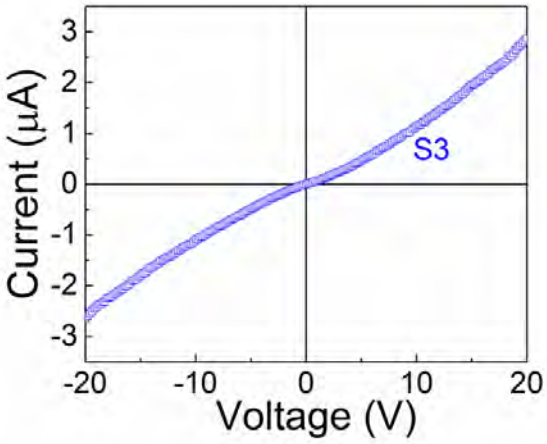

Figure 3. I-V characteristic of liquid exfoliated MoS_2 in IPA+EC+T solvent for dispersion S3.

We have formed p-n junction devices from the formulated dispersions on p-type Si substrates which show a turn-on voltage V_t ~ 3 V; these device characteristics are discussed in more detail in [14].

III. Mechanical Exfoliation

A. Device Structure and Fabrication

Besides liquid exfoliation, we have also formed devices of MoS_2 using mechanical exfoliation for photodetector applications. The metal contact selected for the fabrication of this device was Mo, which from previous work has shown to be a low contact resistance material to MoS_2 [15], and minimizes the Schottky barrier height to enhance the performance of MoS_2 for photodetector applications. The fabrication process involves the alignment of the few-layered MoS_2 flake onto the substrate with pre-patterned Mo electrodes, as shown in Fig. 3, using a viscoelastic stamping process [16]. This adaptation of the visco-elastic stamping process in our lab, makes the flake transfer more efficient compared to manual alignment which can be time consuming

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and tedious and often results in a low-yield for contacting individual micron-sized flakes.

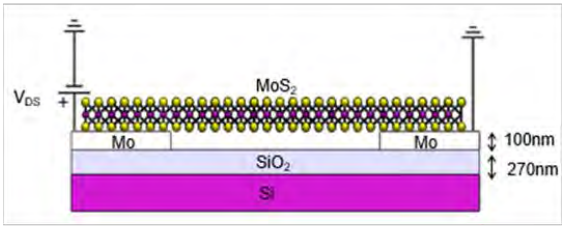

Figure 4. MoS_2 photodetector schematic in cross section.

B. Electronic and Opto-electronic Device Characterization

After fabricating the device in Fig. 4, we conducted device measurements on this few-layer, mechanically exfoliated MoS_2 for photodetector applications. The electronic and opto-electronic device characterization was conducted using a Lakeshore CRX-4K probe stage where temperatures can be controlled from 6 K to 346 K, and a low noise semiconductor parameter analyzer, the Keysight B1500A, was used for the electronic transport measurements. Figure 5 shows the electronic conductivity response of the device over this entire range of temperature. The conductivity decreases as the temperature decreases, which is expected for a semiconducting material.

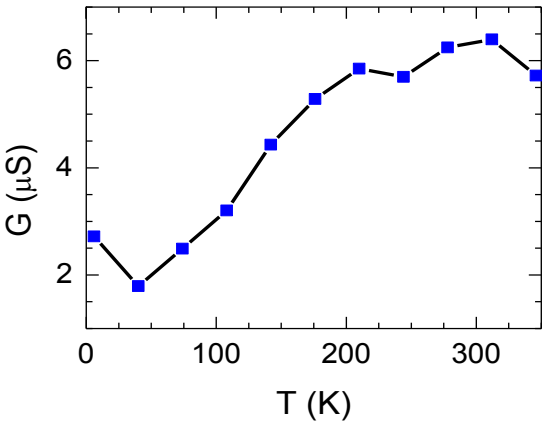

Figure 5. Conductivity of device vs temperature at a drain-source voltage of 1 V.

The opto-electronic response of this device was measured as a function of the optical power using a broad band white light source. The device under test was exposed to increasingly higher power levels of the incoming white light source under vacuum conditions and the photocurrent and photoresponsivity was measured at 300K. The photocurrent I_{ph} is defined as the difference between the current under exposure of light I_{light} and the dark current I_{dark} ($I_{ph} = I_{light} - I_{dark}$).

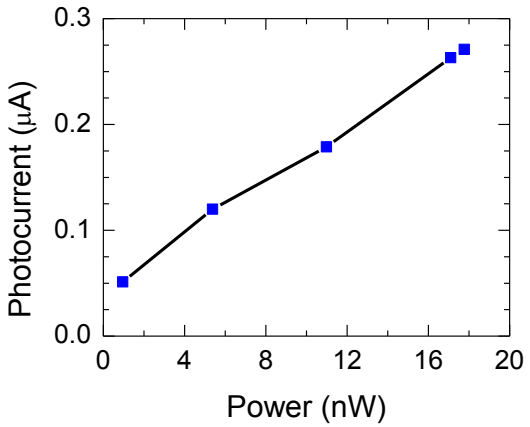

Figure 6. Optical response of photodetector at 1 V which shows the photocurrent of device increases as the intensity of the incoming source increases.

From the data in Fig. 6, it is clear that the MoS_2-based device under test is responsive to a broad band white light source, where the photocurrent increases as the optical power is increased from 0.5 nW up to about 18 nW. We elaborate more on the electronic and opto-electronic response of these mechanically exfoliated devices in [17].

ACKNOWLEDGMENT

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Experimental approach for feasibility of superlattice FETs

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***Abstract*—Steep subthreshold-slope (SS) devices are attracting much interest because of their capability of reducing the power dissipation in digital ICs. However, the mechanism for obtaining a steep SS often interferes with the low on-resistance that is required for a high on-current. The introduction of a doped superlattice into the source was recently proposed as a solution to this problem. However, to our knowledge, no one has yet reported an experimental trial for the same. In this study, by using vertical double-gate metal-oxide-semiconductor field-effect transistor (MOSFET) fabrication processes, we fabricated FETs with an n-doped InGaAs/InP superlattice source, to confirm the feasibility of the superlattice FET. A superlattice FET with a 16-nm-wide mesa was fabricated. The observed *I–V* characteristics showed an on/off ratio of over 10^6, which is necessary for observing the features of the superlattice FET. However, a plateau in the *I–V* characteristics (which is a feature of the superlattice FET) was not observed.**

Keywords—Superlattice FET, steep slope, vertical FET, double gate, InGaAs/InP

I. Introduction

Steep subthreshold-slope (SS) devices have attracted much interest for their ability to reduce power dissipation in digital ICs. Tunnel field-effect transistors (TFETs) have recently attracted much attention because of their steep SSs [1,2]. However, the mechanism for obtaining a steep SS often interferes with the low on-resistance required for obtaining a high on-current. To solve the problem of tunnel resistance in steep-SS devices, the introduction of a doped superlattice into the source was recently proposed [3]. However, to our knowledge, no experimental trial on superlattice FETs has been reported so far. In this study, we fabricate FETs with an n-doped InGaAs/InP superlattice source to confirm the feasibility of superlattice FETs.

II. Simulation

If the scattering in the channel is ignored, the drain current due to the electrons injected into the channel by the doped superlattice source can be determined by the barrier at the channel bottleneck or at the top of the source channel potential. The doped superlattice source changes the density of states by forming a miniband structure. To calculate the current from the doped superlattice source, we use the Tsu–Esaki model [4] in which the transmission probability in the superlattice is calculated by assuming zero electric field in the superlattice and ignoring the scattering. The n-InGaAs layer behind the superlattice, which has a Fermi level equal to that of the superlattice, supplies the electrons. The transmission probability across the channel bottleneck is assumed to be a unit step function, i.e., if the electron energy is larger than the barrier, the probability is unity; otherwise, the probability is zero. Because the obtained energy of the electron is not very low, we must account for the nonparabolicity of the energy bands. The α-parameters of InGaAs and InP are 1.18 and 0.75, respectively.

The mechanism for obtaining a steep SS is explained in Fig. 1. To switch from the OFF state to the ON state, the barrier height is lowered to increase the number of electrons injected from the source. When the barrier height is located within the minigap, no change is observed in the current on lowering the barrier height because no electrons are located in the minigap. Further lowering of the barrier height results in the barrier height crossing the lower miniband. The lower miniband has a large electron density because its energy is close to the Fermi level. Thus, this crossing causes an abrupt increase in the current.

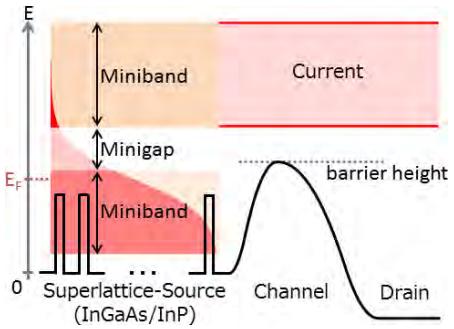

Fig.1. Schematic band diagram of a superlattice-based FET. When the barrier height is located within the minigap, a plateau is observed in the *I–V* characteristics.

When the gate controllability is identical, the barrier height at the channel bottleneck is equal to the gate bias. Thus, the

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relation between the barrier height and the drain current (shown in Fig. 2) is almost the same as that in the I_D–V_G characteristics. As shown in Fig. 2, the superlattice FET achieves a steep slope by using the minigap of the doped superlattice [3,4]. In the case represented in Fig. 2, we use a superlattice of 10 layer pairs formed by the 2-nm-thick InGaAs well and the 1.4-nm-thick InP barrier, assuming a Fermi level at 0.45 eV in the source, and a drain voltage of 0.2 V. As a reference, an FET without a superlattice is also shown. A change in the drain current, from 2 mA/μm to 100 nA/μm, is obtained by a potential change of less than 0.2 eV. In Fig. 2, a clear plateau can be observed when the top of the barrier height at the channel bottleneck is located in the minigap (as shown in Fig. 1).

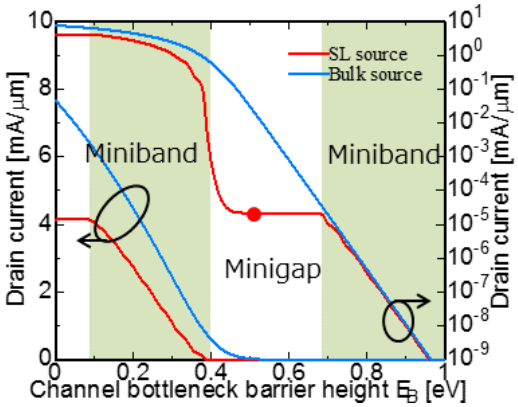

Fig.2. Calculated relation between the barrier height at the channel bottleneck and the drain current [4].

Another problem in observing the steep-slope region in the FET operation is the interface state density of the MIS structure. As the interface state density degrades the SS, direct observation of the steep slope becomes difficult at high interface state densities. However, a plateau (a feature of superlattice FETs) can be observed. Thus, we design the structure to observe the plateau. When we use a 3-nm-thick InGaAs well and a 0.8-nm-thick InP barrier, we can expect to observe a clear plateau when the on/off ratio is larger than 6×10^5 (as shown in Fig. 3).

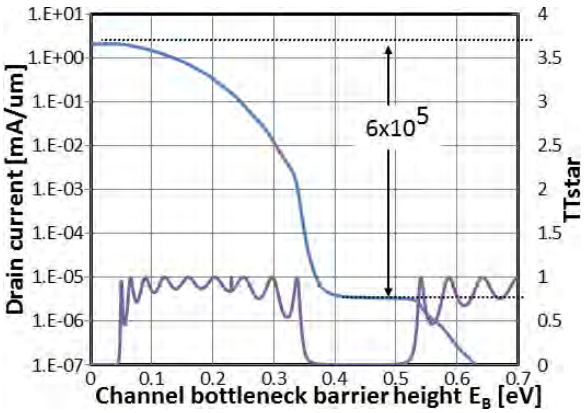

Fig.3. Calculated relation between the barrier height at channel bottleneck and drain current for clear observation of the plateau.

III. Fabrication Process

The schematic cross-section of the fabricated structure is shown in Fig. 4. The epitaxial structure was grown by metalorganic vapor phase epitaxy. The carrier concentration in the n-InP source region behind the superlattice was 5×10^{18} cm^{-3}, and the superlattice was doped in the well-region only with a doping concentration of 3×10^{19} cm^{-3}. The carrier concentration in the n-InGaAs drain was 1×10^{19} cm^{-3}.

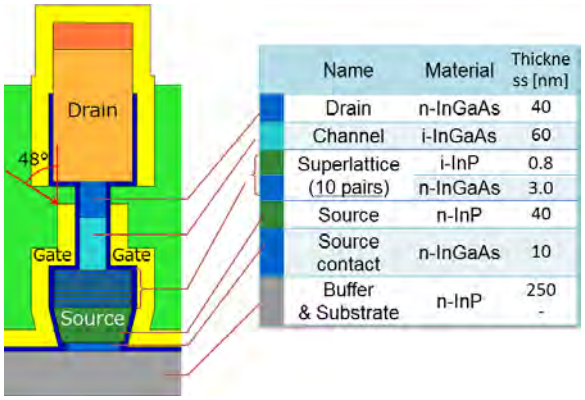

Fig.4. Schematic cross-section of fabricated structure

The fabrication process for the device was almost identical to the fabrication process reported for the double-gate InGaAs MOSFETs [5–7], except for the insertion of a doped superlattice between the source and the channel. After the sputtering of the drain electrode using a Cr mask patterned by an electron beam, the drain electrode was etched by reactive-ion etching (RIE) using CF_4 as shown in Fig. 5(a). Then, the InGaAs and InP layers were etched by CH_4/H_2 inductively-coupled-plasma–RIE (ICP–RIE) as shown in Fig. 5(b). After removal of the InP layer (Fig. 5(c)) by wet etching ($HCl:H_3PO_4$ = 1:7), the InGaAs channel layer was undercut as shown in Fig. 5(d) ($H_3PO_4:H_2O_2:H_2O$ = 1:2:40). Then, Al_2O_3 was deposited by atomic layer deposition. Just after deposition, post-deposition annealing was carried out at 350°C for 90 s. After forming the source contact, the gate electrode was formed by tilted evaporation (60°) (Fig. 5(e)). Then, the device was covered using BCB and wiring of the drain contact exposed by the etch-back was carried out (Fig. 5(f)). Finally, post-metallization annealing was carried out at 300°C for 90 s.

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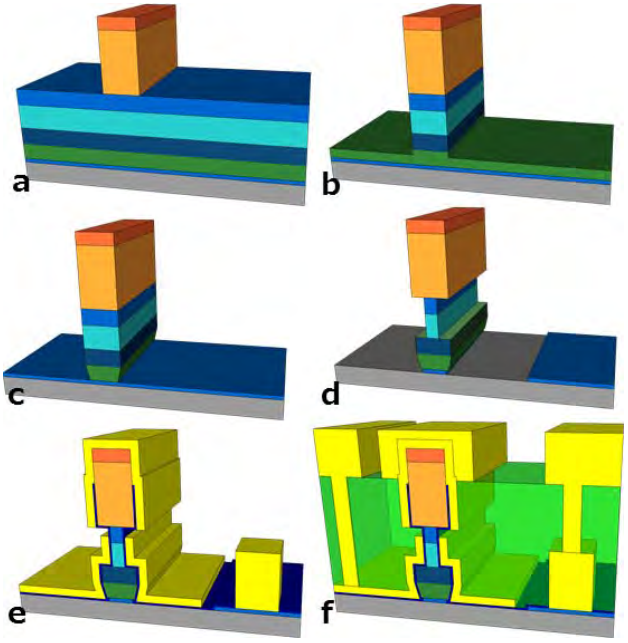

Fig.5. Process flow

The scanning electron microscope (SEM) cross-sectional view of the fabricated device is shown in Fig. 6. We confirmed a mesa (or body of double-gate MOSFET) of 16-nm width, surrounded by a 7.5-nm Al_2O_3 layer and a metal gate.

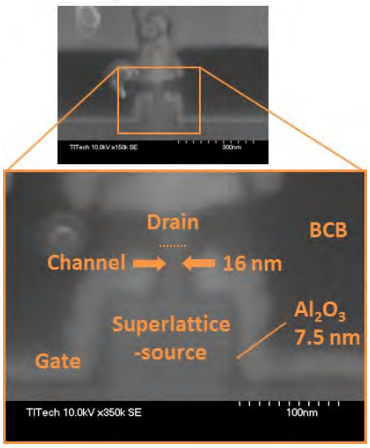

Fig.6. SEM cross-sectional view of the fabricated device with 16-nm wide mesa.

IV. Experimental Results

The observed I_d–V_d characteristics are shown in Fig. 7. Current modulation by the gate bias was confirmed. However, the presence of a large output conductance was also confirmed. The open-circuit voltage gain obtained from the ratio of transconductance to output conductance was less than unity. This degradation can be explained by the band bending due to the space charge in the channel, when the channel is not sandwiched by the gate metal [7]. In the SEM cross-sectional view in Fig. 6, it can be observed that the gate metal does not cover the channel mesa region completely. When the connections to the source and drain were reversed, a higher open-circuit voltage gain was confirmed (due to a lower output conductance) although the obtained transconductance was shown to be degraded due to the high source resistance (as can be observed in Fig. 8).

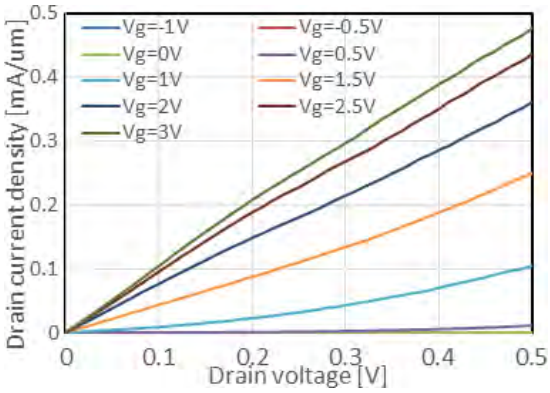

Fig.7. Observed I_d–V_d characteristics of the fabricated device. Mesa width is 16 nm.

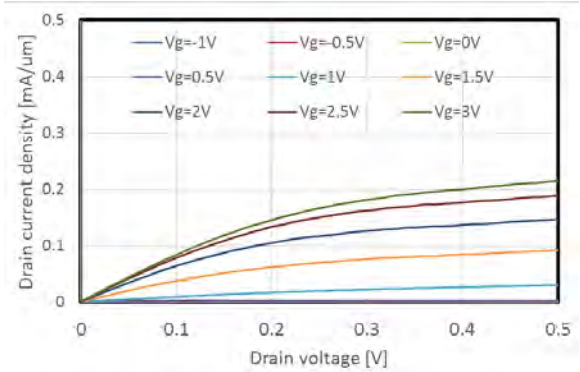

Fig.8. Observed I_d–V_d characteristics of the fabricated device. The device is identical to that in Fig. 6. However, the connections of the source and drain are reversed from those in the configuration in Fig. 7.

We confirmed a narrower width as shown in Fig. 9. The mesa width in Fig. 9 is observed to be 7 nm. However, the current modulation by the gate bias was not confirmed in this device. In comparison with Fig. 6, the gap between the gate metal and the insulator can be confirmed in Fig.9. By the gap formed between channel and gate, no gate controllability of current can be explained. By too steep oblique angle in the gate evaporation with taking lateral undercut extent, this gap may be explained. Precise alignment of an oblique angle of evaporation with stable control of lateral undercut extent is required for stable operation.

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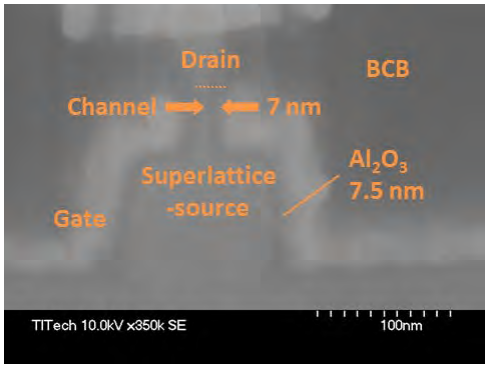

Fig.9. SEM cross-sectional view of the fabricated device with a 7-nm-wide mesa.

The observed I_d–V_g characteristics are shown in Fig. 10. The minimum SS is 209 mV/dec. This large value can be explained by the short-channel effects and by the large interface state density of the MIS structure, because a lower SS was observed when the mesa width was 54 nm. The on/off ratio at a drain voltage of 0.05 V was over 10^6. Thus, the on/off ratio stipulated in the design (6×10^5) was achieved. However, no plateau of current was observed in this experiment. It may be because of the inhomogeneous barrier in the channel due to the short-channel effect. However, the most probable explanation is that the poor coherency of the electrons for forming the superlattice was disturbed due to doping.

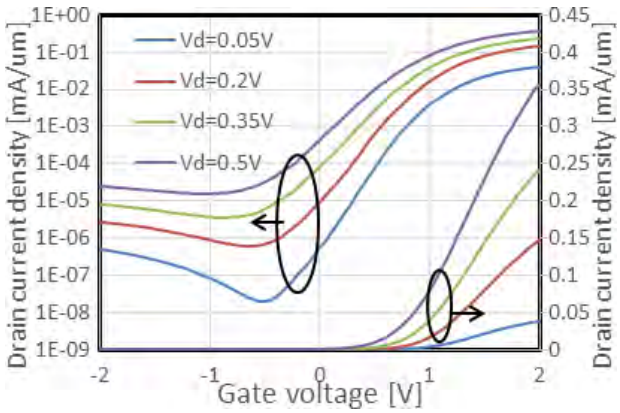

Fig.10. Observed I_d–V_g characteristics of fabricated device. The device is identical to the one in Fig. 6.

V. Conclusions

To confirm the feasibility of the superlattice FET, an FET with an n-doped InGaAs/InP superlattice source was fabricated. The target of the experiment was the observation of a plateau in the *I*–*V* characteristics, resulting from the limitations in the interface state density. The fabricated superlattice FET with a 16-nm-wide mesa demonstrated an on/off ratio of over 10^6, which is required to observe the features of the superlattice FET in the I_d–V_g characteristics. However, the plateau (as a feature of the superlattice FET) was not observed. The most probable explanation is that the poor coherency of electrons, to form the superlattice, was disturbed due to doping. Reduction of doping level or another pairs of gate electrodes on the side of the superlattice [8] may solve the poor coherency of electrons.

Acknowledgment

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Low-Temperature Characteristics of $In_{0.7}Ga_{0.3}As$ PHEMTs

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***Abstract*—In this paper, we report on temperature dependent DC characteristics of $In_{0.7}Ga_{0.3}As$ Pseudomorphic-HEMTs (PHEMTs) on InP substrate. First, we have fabricated the $In_{0.7}Ga_{0.3}As$ PHEMTs with various values of L_g, ranging from 10 μm to 2.5 μm. The fabricated device with L_g = 2.5 μm exhibits excellent subthreshold-swing (SS) of 64 mV/decade at room temperature. Note that this is close to 60 mV/decade, which is a theoretical limit at room temperature in a FET configuration. Next, we have measured current-voltage characteristics at various values of temperatures, from 300 K to 80 K. Finally, we have investigated the temperature-dependent DC characteristics of the $In_{0.7}Ga_{0.3}As$ PHEMTs, in terms of output, subthreshold, and transconductance characteristics.**

Keywords—III-V, InGaAs, PHEMT, Low-Temperature

I. Introduction

Pseudomorphic-High-Electron-Mobility-Transistors (PHEMTs), based on indium-rich $In_xGa_{1-x}As$ (x>0.53) material systems, display excellent carrier transport properties such as high electron mobility (μ_n) and injection velocity (v_{inj}) [1]. Due to their excellent electron's carrier transport properties, it leads to outstanding high-frequency and high performance logic characteristics. Indeed, significant efforts and achievements have been made on a variety of InGaAs PHEMTs by many different research groups in the world, for the past decade [2-5]. For certain applications, it is obvious that the device needs to have a stable operation with a wide range of temperatures. This requires several measurements and characterizations of the device for each temperature. Several efforts and progress have been made on the temperature dependent characterization of the InGaAs PHEMTs [6].

In this work, first we have fabricated and characterized the $In_{0.7}Ga_{0.3}As$ PHEMTs on InP substrate. Then, we have investigated the temperature-dependent scaling behavior of the fabricated $In_{0.7}Ga_{0.3}As$ PEHMTs from 300 K to 80 K. In particular, we have extracted several figure-of-merits (FOMs) for the $In_{0.7}Ga_{0.3}As$ PHEMTs.

II. Experiments

Figure 1 shows a schematic cartoon of the $In_{0.7}Ga_{0.3}As$ PHEMTs. All the epitaxial layers were grown by Molecular-Beam-Epitaxy (MBE), which is an InGaAs/InAlAs quantum-well (QW) structure on a semi-insulating InP substrate. We used a 5 nm thick $In_{0.53}Al_{0.42}As$ schottky barrier. For source and drain ohmic contacts, we used a heavily doped n^+ $In_{0.53}Ga_{0.47}As$ capping layer and ohmic metal stack of Mo/Ti/Pt/Au. We fabricated the $In_{0.7}Ga_{0.3}As$ PHEMTs with various values of L_g, from 10 μm to 2.5 μm.

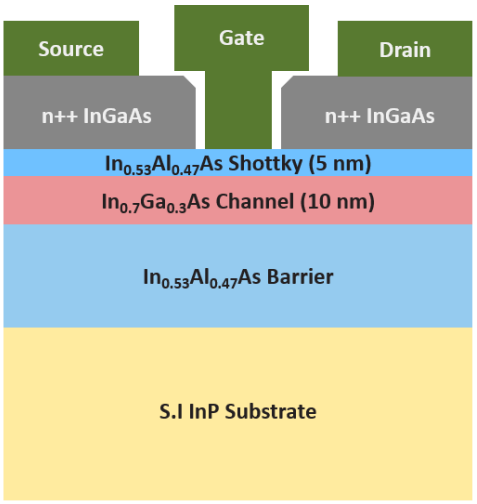

Fig. 1. Schematic cartoon of the $In_{0.7}Ga_{0.3}As$ PHEMTs

Figure 2 shows the temperature dependence of the output characteristics for the $In_{0.7}Ga_{0.3}As$ PHEMT with L_g = 2.5 μm. Gate-to-source voltage (V_{GS}) is swept from 0.5 V to -0.5 V in -0.2 V steps. Dotted lines in this plot are for the drain current (I_D) at 80 K, and the solid lines at room temperature. It is obvious that the on-resistance (R_{ON}) of the device goes down when the temperature decreases. Also, the device shows better current driving capability at 80 K. In comparison to [7], the device in this work does show any evidence of kink effect, which is a sudden increase of I_D with V_{DS}. This result helps stable operation at low-temperature.

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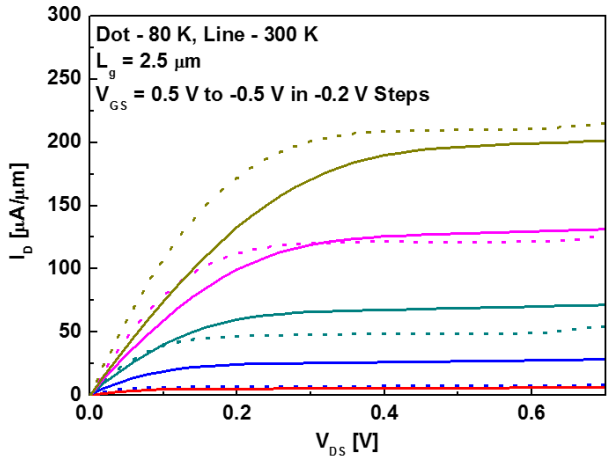

Fig. 2. Output Characteristics at 80 K (dotted lines) and 300 K (solid lines) with L_g = 2.5 µm.

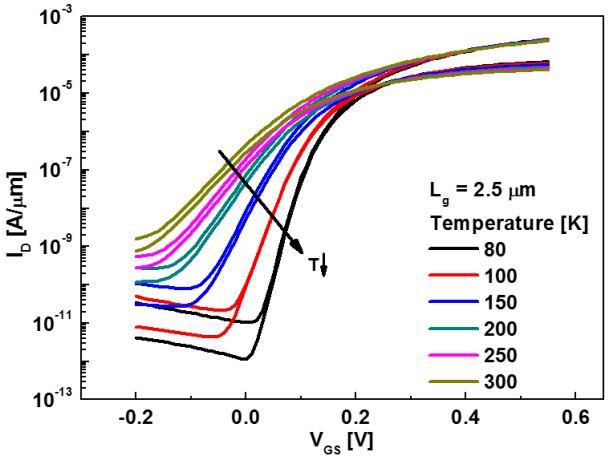

Fig. 3. Temperature dependence of the subthreshold characteristics with L_g = 2.5 µm.

Figure 3 shows the temperature dependence of the subthreshold characteristics for the same device with L_g = 2.5 µm. Drain-to-source voltage (V_{DS}) is swept from 0.05 V to 0.5 V in 0.45 V steps, at various values of temperatures (300 K, 250 K, 200 K, 150 K, 100 K and 80 K). The fabricated device with L_g = 2.5 µm shows excellent subthreshold swing (SS) of 64 mV/decade at room temperature. Note that, for long channel devices, theoretical limit of SS is about 60 mV/decade at room temperature, indicating the SS value in this work is close to the theoretical limit of SS in a FET configuration. Looking at temperature dependent subthreshold characteristics of the $In_{0.7}Ga_{0.3}As$ PHEMT, it is obvious that SS decreases with temperature, according to the Boltzmann relationship [8].

Next, we have investigated the temperature dependent DC characteristics of the $In_{0.7}Ga_{0.3}As$ PHEMTs. **Figure 4** shows the temperature dependent transconductance (g_m) characteristics for the same device with L_g = 2.5 µm, at V_{DS} = 0.5 V. Measured temperatures are the same as in the previous subthreshold characteristics data. Measured g_m increases as temperature goes down. The improvement in g_m comes from the increase of the carrier transport properties in $In_{0.7}Ga_{0.3}As$ channel layer and the decrease of parasitic source and drain resistances (R_S and R_D) as temperature decreases. The reduction of R_S and R_D with temperature is because electron's mobility in the S/D access region also increases as temperature goes down [9].

Figures 5 (a), (b), and **(c)** summarize SS, R_{ON} and maximum transconductance (g_{m_max}) against temperature, respectively. As shown in **Figure 5 (a)**, the fabricated device shows excellent SS characteristics, such as 64 mV/decade at T = 300 K, as mentioned earlier. Clearly, the value of SS decreases gracefully with temperature. For example, SS goes down to 17 mV/decade at T = 80 K. Furthermore, from the temperature dependent SS characteristics of the $In_{0.7}Ga_{0.3}As$ PHEMTs, we attempted to estimate a value of the interface-trap-density (D_{it}) at the Schottky gate interface. In principle, D_{it} can be correlated to the function of SS as in Equation (1). By using the slope of the **Figure 5 (a)**, we extracted the value of the D_{it}.

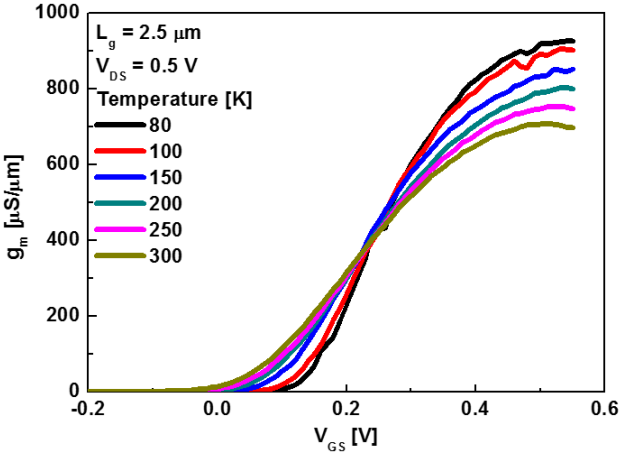

Fig. 4. Temperature dependence of the transconductance characteristics with L_g = 2.5 µm.

$$D_{it} = \frac{C_{ox}}{q}\left[\frac{SS \times q}{2.3k} - 1\right] \quad (1)$$

By using the slope of the **Figure 5 (a)**, we extracted the D_{it}**.** In this way, the extracted value of the D_{it} is around at 5×10^{11} $eV^{-1}cm^{-2}$. As shown in **Figure 5 (b)**, when the temperature decreases, R_{ON} also continues to decrease.

Figure 5 (c) shows g_{m_max} against temperature, with L_g = 2.5 µm to 10 µm. Due to the reduction of R_S and R_D, which is manifested by the decrease in R_{ON}, the extrinsic g_{m_max} improves as temperature decreases. This is also in part because of the improvement in the carrier transport properties in the $In_{0.7}Ga_{0.3}As$ quantum-well channel as temperature goes down.

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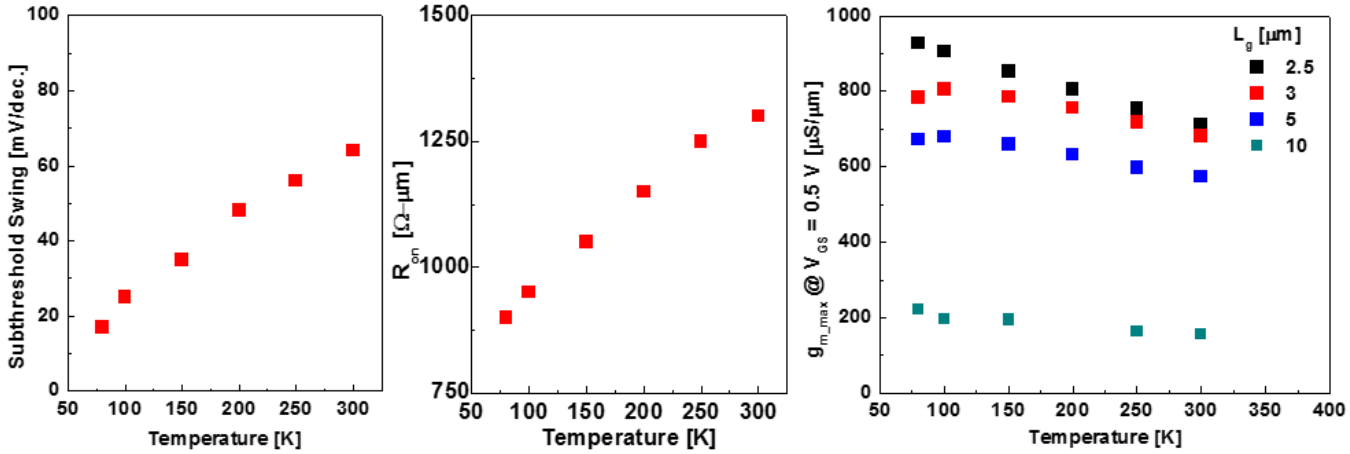

Fig. 5. SS characteristics against temperature with L_g = 2.5 μm, (b) R_{ON} against temperature with L_g = 2.5 μm and (c) g_{m_max} against temperature with L_g = 2.5 μm to 10 μm.

III. Conclusion

We have fabricated and characterized the $In_{0.7}Ga_{0.3}As$ PHEMTs. The device with L_g = 2.5 μm shows excellent subthreshold swing = 64 mV/decade, close to the theoretical limit. Then, we have measured I-V characteristics of the $In_{0.7}Ga_{0.3}As$ PHEMTs at various values of temperatures, from 300 K to 80 K. As expected, SS goes down to 17 mV/decade at 80 K. Next, we have carefully investigated the temperature-dependent scaling behavior in terms of output characteristics, subthreshold characteristics and transconductance characteristics. In particular, we have extracted SS, R_{ON}, g_{m_max} for the $In_{0.7}Ga_{0.3}As$ PHEMTs and investigated their temperature-dependent scaling behavior. Using temperature-dependent SS behavior, we have estimated the value of D_{it} to be around 5×10^{11} $eV^{-1}cm^{-2}$ at the Schottky gate interface.

Acknowledgment

This work was supported by the BK21 Plus Project through the Ministry of Education, Korea, under Grant 21A20131600011, by a grant from the R&D Program for Industrial Core Technology funded by the Ministry of Trade, Industry and Energy, Republic of Korea (Grant No. 10045216), and this investigation was financially supported by Semiconductor Industry Collaborative Project between Kyungpook National University and Samsung Electronics Co. Ltd.

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Preliminary Results for Broadband Electrical Detection of Live Bacteria

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***Abstract*—For the first time, broadband (0.5–20 GHz) electrical detection of live bacteria was successfully demonstrated on E. coli, despite their being small and adherent compared to mammalian cells such as Jurkat T-lymphoma human cells that had been detected by using a similar coplanar waveguide in conjunction with a microfluidic channel. Critical to the success was in suppressing the background drift of the insertion and return losses to the order of 0.01 dB. Presently, it is estimated that approximately 10^4 E. coli were required to yield a statistically significant signal in the insertion/return losses. Therefore, to detect a single bacterium, the measurement sensitivity and the background stability need to be further improved by orders of magnitude in the future.**

Keywords—Biological cells; biosensors; microfluidics; microwave measurements; sensitivity.

I. Introduction

Rapid detection of bacteria is of increasing importance due to the emergence of antibiotic-resistant bacteria, foodborne infections, and bioterrorism. Traditionally, bacteria detection involves time-consuming culture techniques or chemical means, and often requires labeling that can alter the properties of bacteria under test. By contrast, broadband electrical detection can be fast, compact and label-free as has been demonstrated on mammalian cells [1], [2]. However, due to the small size and adherent nature of bacteria, electrical detection of bacteria presents new challenges. This paper is the first report on how these challenges were overcome, so that small yet statistically significant signals could be obtained from bacteria.

Broadband electrical detection across decades of frequencies can have additional advantages. For example, based on the different polarization mechanisms [3], live and dead cells can be differentiated at megahertz frequencies, cell types can be identified at gigahertz frequencies, and surface functionality can be detected at terahertz frequencies as illustrated in Fig. 1. Thus, broadband electrical detection can yield a wealth of information for insight into the electrical properties of a cell. However, many challenges remain for broadband electrical detection of cells, such as impedance matching, calibration, modeling, and data analysis. For example, broadband electrical detection of single cells involves measurements highly mismatched in both size and impedance.

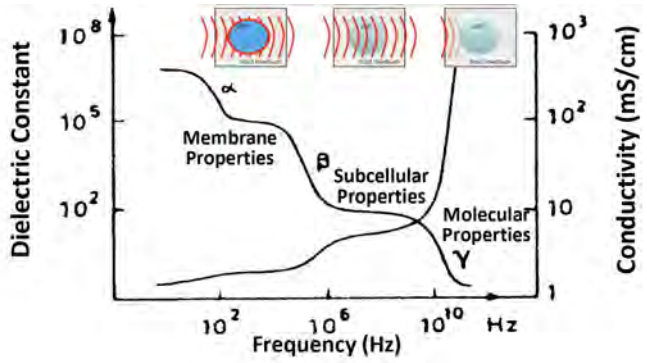

Fig. 1. Schematic illustration of broadband dispersion of the dielectric properties of a biological cell showing transitions between different polarization mechanisms at different frequency ranges and length scales.

Typically, broadband coplanar waveguides (CPW) with width on the order of 100 μm are used [1], [2], which require careful transition down to the order of 1 μm to match the cell size. At microwave frequencies, the capacitance of the cell membrane (~1 pF) [4] is largely bypassed, so that the electrical properties of the cell are dominated by the cytoplasm resistance (~10^5 Ω) [5], which is orders-of-magnitude higher than the characteristic impedance (Z_0 = 50 Ω) of typical microwave measurement systems. These challenges are especially acute in broadband measurement for which the signal-to-noise ratio is usually much lower than that of narrowband resonance [6] or interference [7] measurements. Despite these challenges, broadband detection has recently been demonstrated on mammalian cells down to the single-cell level [8], [9].

Previously, for broadband detection of multiple mammalian cells, we have successfully used [2] dielectrophoresis (DEP) to trap the cells in the gaps between the center and ground electrodes of a CPW. Once the cells were trapped and broadband measurement in terms of insertion loss $|S_{21}|$ and return loss $|S_{11}|$ was completed, the DEP signal was turned off and the cells were quickly released. This allowed the measurement to be quickly repeated without cells to establish the instantaneous background signal even if it would drift over time. From the difference between the two consecutive measurements, small yet statistically significant cell signals could be obtained. In the present measurements, the adherent nature of bacteria precludes DEP and bacteria can be stuck in

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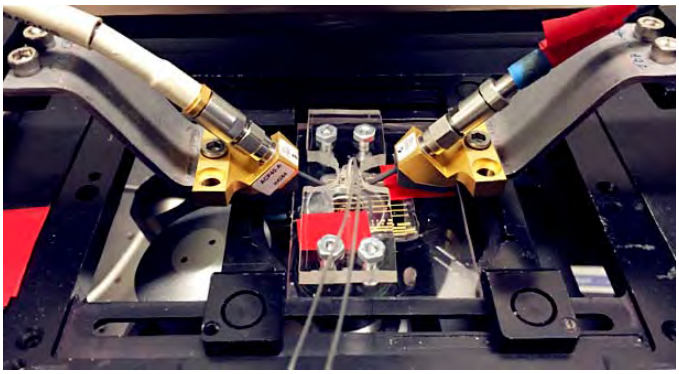
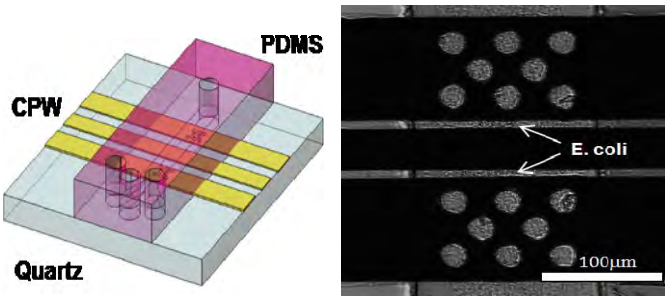


(a)



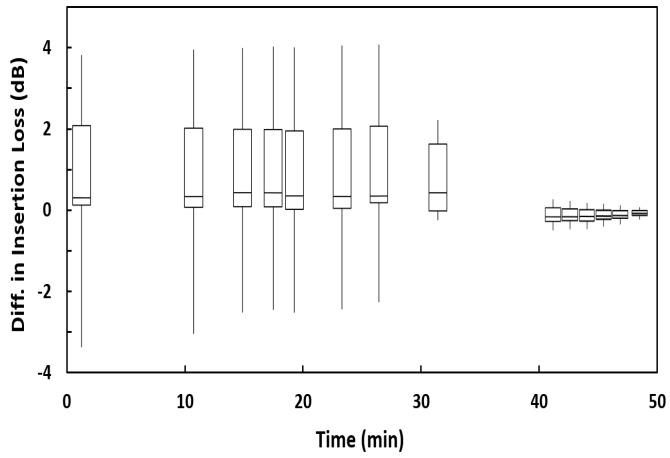
(b) (c)

Fig. 2. (a) Photograph of the CPW under test on top of an inverted microscope. (b) Schematic of the CPW intersected by a PDMS microfluidic channel at a right angle. (c) Micrograph of E. coli bacteria trapped between the center and ground electrodes of the CPW. Perforations in the ground electrodes are for viewing only without any electrical function at the frequencies of interest. Vertical lines beside perforations delineate microfluidic channel.

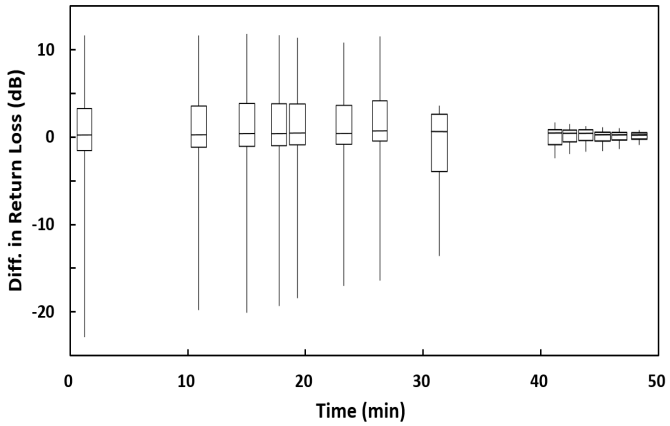
the CPW gaps without DEP, which are difficult to rinse off. To overcome such challenges, broadband measurements without cells were first repeated many times until a steady state was established without the aforementioned background signal drift. Thereafter a high concentration of bacteria was flown over the CPW until a steady number of them were trapped, and broadband measurement was repeated many more times to ensure a stable signal with the bacteria. The difference between the averages with and without bacteria was deemed the bacteria signal.

II. Experiments

Based on a homemade microwave probe station on top of an inverted fluorescence microscope, the present test setup for bacteria, shown in Fig. 2(a), is similar to that used for mammalian cells [9], [10]. As shown in Fig. 2(b), the device-under-test (DUT) comprises a CPW patterned in 2-μm-thick gold on 635-μm-thick quartz, and a polydimethylsiloxane (PDMS) cover 5-mm wide, 8-mm long and 4-mm thick. The PDMS cover is molded with a 20-μm-deep, 150-μm-wide, and 5-mm-long micro-fluidic channel on its underside, which intersects the CPW at a right angle. The CPW is 1-cm long with the widths of center electrode, electrode spacing, and ground electrodes being 40 μm, 10 μm and 100 μm, respectively. The DUT was tested by using an Agilent Technologies 5230A precision network analyzer and a pair of



(a)



(b)

Fig. 3. Time evolution of median, standard deviation, minimum, and maximum differences between 0.5 GHz and 20 GHz of (a) insertion loss $|S_{21}|$ and (b) return loss $|S_{11}|$ of lysogeny broth (without any bacteria) from that measured 50 min after lysogeny broth was flown across the CPW.

Cascade Microtech ACP40 GSG probes. For proof of principle, the bandwidth was limited to 0.5–20 GHz. The input microwave signal power was approximately 1 mW.

As model bacteria, the strain of E. coli PHL 628 was cultured overnight in a lysogeny broth (4-g NaCl, 4-g tryptone, and 2-g yeast extract in 400 ml H_2O) at 37°C while shaken at 200 rpm. The E. coli culture was thrice centrifuged at 1800 rpm for 20 min and re-suspended in fresh lysogeny broth. The final concentration was estimated to be 2×10^9 cell/ml by optical density measurement. The final bacteria suspension was injected through the microfluidic channel by a Fusion 400 syringe pump at the rate of approximately 1 ml/min. Before the bacteria suspension were flown through the microfluidic channel, the lysogeny broth was flown at the same rate to establish the background signal level. The background signal was monitored every few minutes until a steady state was reached after approximately 1 h. As shown in Fig. 3, the background drift was initially on the order of 1 dB, which was eventually reduced to the order of 0.01 dB.

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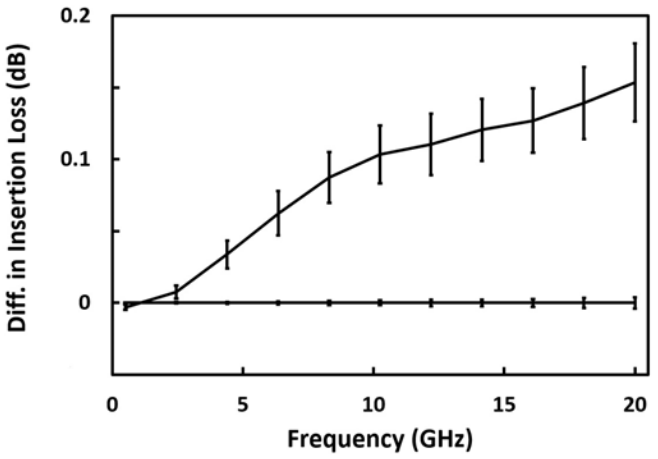
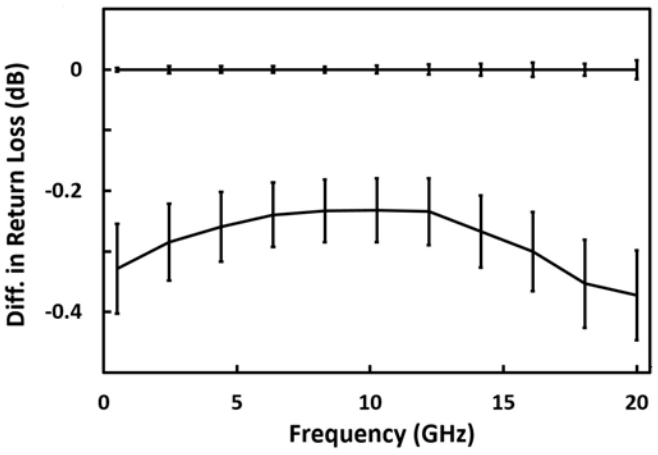


(a)



(b)

Fig. 4. Average and standard deviation of the differences from the background signals in (a) insertion loss $|S_{21}|$ and (b) return loss $|S_{11}|$ with approximately 10^4 live E. coli bacteria trapped in the CPW. Standard deviations of the background signals with lysogeny broth only and without any E. coli are plotted on the horizontal axis for comparison.

Once a stable background was established, the microfluidic flow was switched to the E. coli suspension. However, it took 14 min to flush out the lysogeny broth in the dead volume and for E. coli to reach the CPW. During this period the background continued to be monitored every 2 min, and the standard deviation of seven consecutive measurements was found again to be on the order of 0.01 dB across the band as plotted on the horizontal axis of Fig. 4. The average of these seven measurements were then used the background to subtract the subsequent data measured after E. coli reached the CPW and a stable number of them was trapped there after another 6 min as shown in Fig. 2(c). The number of trapped E. coli was estimated to be on the order of 10^4, giving their size of approximately 1 μm³ and the volume of 150 μm × 10 μm × 2 μm × 2 between the center and ground electrodes of the CPW inside the microfluidic channel. After a stable number of E. coli was trapped in the CPW, broadband measurement was repeated thirty-one times at 1-min intervals and their average, after subtracting from the average of the seven background measurements prior, is deemed the E. coli signal.

III. Results and Discussion

Fig. 4 shows the difference of the measured insertion and return losses of approximately 10^4 E. coli from that without any bacteria. It can be seen that the difference is much larger than the standard deviation of either the E. coli signal or the background signal. Additionally, the difference varies smoothly across the band of 0.5–20 GHz without spurious resonances, which would facilitate quantitative fitting with an equivalent-circuit model to extract the basic dielectric properties of E. coli as previously done for mammalian cells [2], [9], [10]. Qualitatively, with E. coli, the insertion loss increased while the return loss decreased, which are consistent with the trends for mammalian cells.

IV. Conclusion

In summary, for the first time, statistically significant signals on the order of 0.1 dB were obtained from 0.5 GHz to 20 GHz for approximately 10^4 E. coli, which is a major advance of the broadband electrical detection technique previously developed for mammalian cells. Qualitatively, the E. coli signals showed consistent trends with that of mammalian cells. Quantitatively, fitting with an equivalent-circuit model is needed to explain such a result and to extract the basic dielectric properties of E. coli as previously done for mammalian cells. This preliminary result serves as the basis for improved broadband detection of bacteria.

Acknowledgment

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Solution Dispersed 2D Graphene & MoS_2 for an Inkjet Printed Biocompatible Photodetector

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***Abstract*— Two-dimensional (2D) layered materials have shown promise for a wide range of semiconducting devices which can be formed not only on rigid Si substrates but also low-cost, flexible and biocompatible substrates. In this paper, we have tested the biocompatibility of various 2D materials, such as graphene and MoS_2 in several organic solvents. Specifically, these materials have been dispersed in Isopropyl Alcohol (IPA), a mixture of Cyclohexanone/Terpineol with a 7:3 ratios (C/T), and N-Methyl-2-pyrrolidone (NMP). The electrical properties were characterized of all drop cast solutions. For preliminary analysis of the electrically-conducting dispersions of graphene and MoS_2, the solutions were drop cast onto thin, flexible and polyethylene terephthalate (PET) and polyimide films. Mouse embryonic fibroblast cells (STOs) were used to perform biocompatibility assays. Optical microscopy was used to gauge the degree of biocompatibility of all of the formulated dispersions. We also highlighted an inkjet printed photodetector which can be considered as a future possibility for *in vivo* photo sensing applications.**

Keywords—Inkjet Printing; Biocompatibility; 2D material; MoS_2; Graphene; Photodetector; in vivo

I. Introduction

Two dimensional layered materials such as graphene and molybdenum di-sulfide (MoS_2) have attracted considerable attention due to their unique electrical properties [1] which are used to improve the performance of various nanodevices. In addition, these materials are potentially biocompatible and may have potential for biosensing applications. Their materials properties include large surface area, tunable energy band diagram, high electron mobility, photoluminescence and stability in liquid media [2,3]. One of the approaches to obtain 2D materials such as graphene and 2D-molybdenum di-sulfide (MoS_2) is through top-down liquid exfoliation, where these materials are dispersed in different solvents through appropriate sonication and centrifugation conditions [4,5,6]. Inkjet printing has become one of the most attractive additive techniques capable of forming micron sized devices with the increasing potential for commercialization of low cost device platforms. The process involves one or more nozzles that eject pico volumes of material onto a substrate in a quick and precise manner [7]. It also allows the deposition of very small volumes of ink, in the picoliter range, in a rapid procedure, achieving high pattern precision and resolution with reasonable reproducibility. Dionisi et al. have studied the inkjet printing method for biomedical purposes using a conventional inkjet printer [8]. In particular, the authors have determined the conditions for good adhesion and conduction of the silver ink on biocompatible polyimide substrates. Medina-Sanchez et al. proposed an integrated and functional Field effect transistor based biosensor consisting of a nano-silver ink mostly deposited by inkjet technology [9]. Pavinatto et al. have fabricated an all printed and flexible gold biosensor for detection of antioxidants [10]. Printed biosensors are also well acknowledged in literature [11, 12]. Other biosensors, like biocompatible photodetectors to fight retinal degenerative diseases, like retinal pigmentosa, age related macular degradation are still using conventional methods such as standard thin film fabrication and lithography [13,14]. Prototype devices demonstrated a minimal feature size of 30 μm. Using inkjet printing to fabricate these photosensitive devices for biomedical applications is a new approach, which is presented in this paper. Here, we have studied 2D materials such as graphene and MoS_2 with two flexible substrates-polyethylene terephthalate (PET) and Polyimide films and conducted a biocompatiblity analysis. Microscopy was used to gauge the degree of biocompatibility of all of the formulated dispersions. We also demonstrated the photosensitive response of the printed MoS_2 resistors. The work focused on proper ink dispersion, annealing conditions and sterilization technique.

II. Experimental Method

A. Ink Preparation

We have established a less energy intensive shearing process for the direct exfoliation of bulk graphene and MoS_2 powder into few-layer Graphene/MoS_2 nanosheets that combines the 8 hours of sonication with a centrifugation technique. The inks were produced through this process in one of three different solvents either isopropyl alcohol (IPA), a 7:3 ratio of Cyclohexanone/Terpineol (CT) or n-methyl-2-pyrrolidone (NMP). 10mg/ml graphene/MoS_2 powder were added to the 10ml of solvent that also included an initial concentration of 4w% of ethyl cellulose (EC) in IPA, 2.5 w% in CT, and 6 w% in NMP. The mixtures were treated for 8 hours in a Branson Ultrasonicator. EC also was added in the solutions to control the printability for the dispersions.

B. Preparing the Sample

The inks were drop cast onto a thin PET or polyimide film and annealed. The annealing process is needed to improve conductivity, and in addition, through it solvents are removed it which could act as leachable toxins. The materials were then cut into a square shape about 1cm x1cm in dimensions and placed in 12-well tissue culture plates and attached using either superglue for the PET samples, or polyimide tape to

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ensure the material remained in place for an extended period of time. The plates were then placed inside a biological hood under UV light for 25 minutes to sterilize the samples.

C. *Biocompatible Assays*

Uniformly cut pieces of the material being tested were placed inside 12 well cell culture plates and attached using either superglue for the PET samples, or polyimide tape to ensure the material remained in place for an extended period of time. Fig. 1 is showing the schematic diagram of the incubated cells sitting on the drop cast samples.

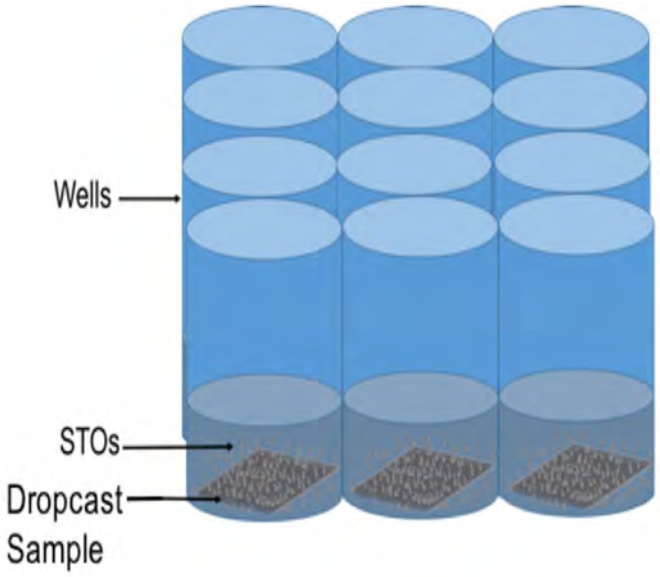

Fig. 1: Schematic diagram of the incubated fibroblast cells on top of the drop cast samples

Superglued samples were allowed to dry for 24 hours. Control tests concluded that the superglue would not affect the growth of the cells if properly shielded with the PET. Mouse embryonic fibroblasts were seeded in triplicate at a density of 10,000 cells per well and cultivated using DMEM medium augmented by 10% FBS in a humidified incubator at 37°C and 5% CO2 until 70% confluence was reached. Images of the cells were taken using phase microscopy.

D. *Electrical Properties*

To check the electrical properties of the graphene and MoS_2 solutions, the inks were drop cast onto flexible polyimide film as described above. It has a high thermal stability up to 400°C unlike the PET which starts degrading at 120°C.

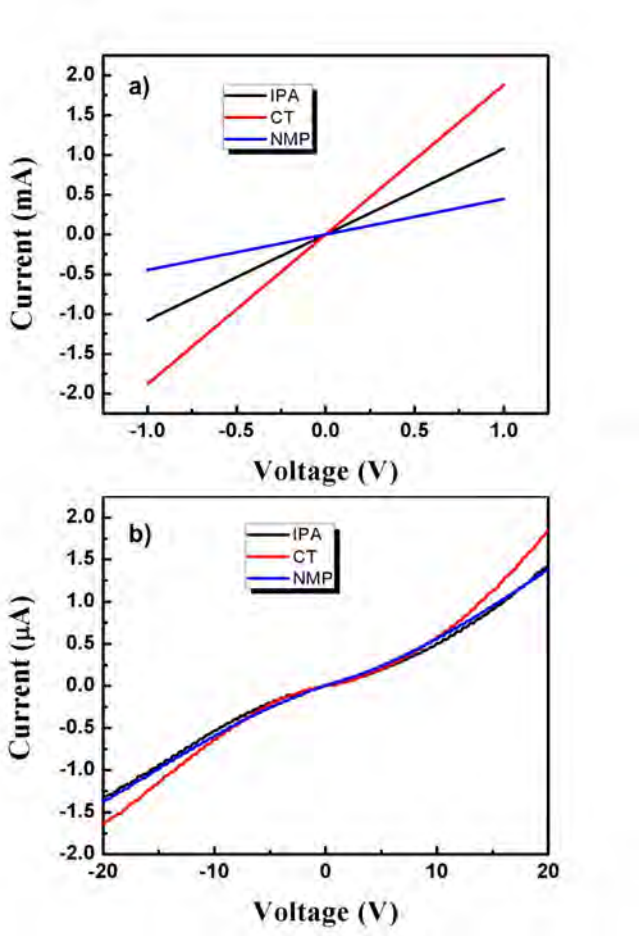

Fig. 2: IV characteristics of drop cast samples of three different solvents using a) Graphene ink b) MoS_2 ink

The solutions were drop cast on the polyimide films and annealed at 300°C for 1 hour, after which point the electrical properties were characterized. The IVs of the printed resistor were measured for a probe spacing of 1mm. Photocurrent responses of the inkjet printed MoS_2 resistor were measured in the dark and then exposed to varying light intensity ranging from 7 mW/cm^2 to 22 mW/cm^2.

E. *Inkjet printing*

For our experiment we used the Dimatix Materials Printer (DMP-2800 Series) that uses a piezo-based jetting cartridge with 16 nozzles that are spaced 254 μm apart. The graphene and MoS_2 inks were obtained by their dispersal in the CT with the proper sonication and centrifugation technique. For the graphene and MoS_2 ink 15 and 30 passes, respectively have been printed with periodically cleaning the print head. Fig.3 shows the printed resistor pattern for both graphene and MoS_2 ink dispersed with CT.

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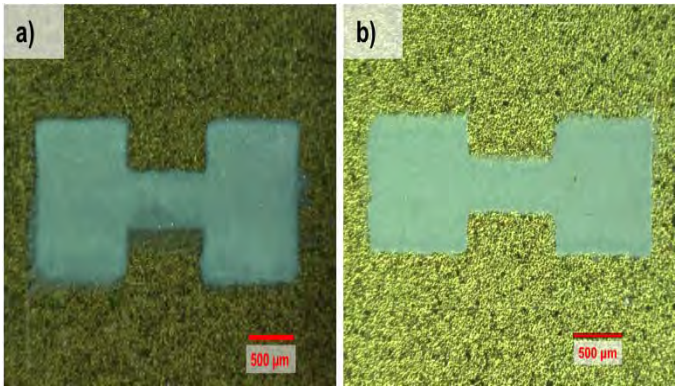

Fig. 3: Printed Resistor pattern with both a) MoS_2 and b) Graphene ink

III. Results

Of all six drop cast solutions, as shown in Fig. 2a and Fig. 2(b). From the I-V characteristic, at 1 V the graphene sample with CT was showing 1.6 mA current which is one order of magnitude higher than the NMP and slightly higher than the IPA. Whereas MoS_2 sample with CT also exhibits a higher current than the IPA or the NMP sample. From this data we were motivated to choose CT for the inkjet printing solvent.

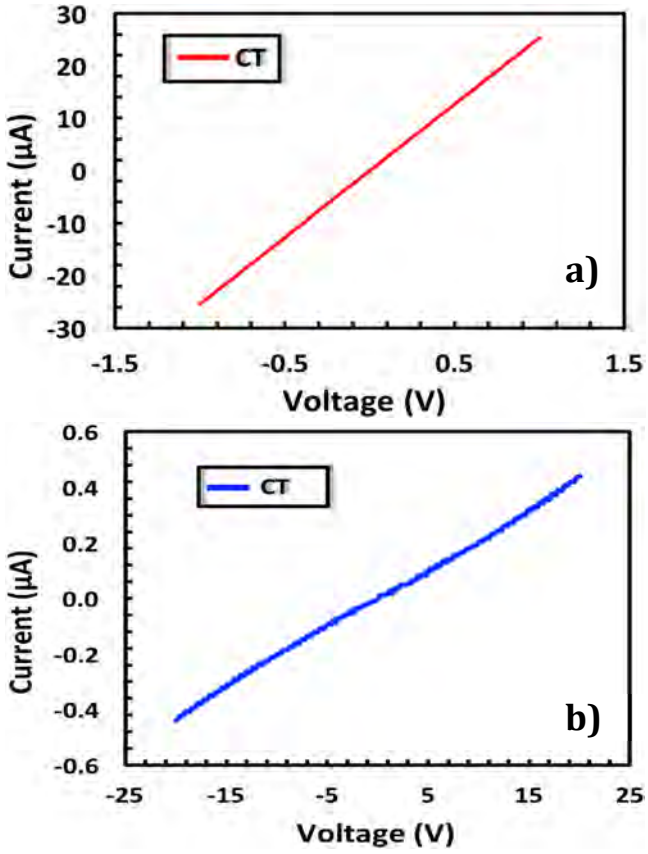

Fig. 4: IV chracteristics of printed Resistor Pattern of a) Graphene b) MoS_2 ink

The graphene resistor showed ohomic behavior while the MoS_2 showed non linear behavior as shown in Fig. 4. The graphene ink printed resistor displayed a current level of 25 µA with a conductivity of 326.32 S/m, indicating a high conductive ink. On the other hand MoS_2 ink printed resistor exhibited a current level of 0.45 µA with a conductivity level of ~2.5×10^{-3} S/m.

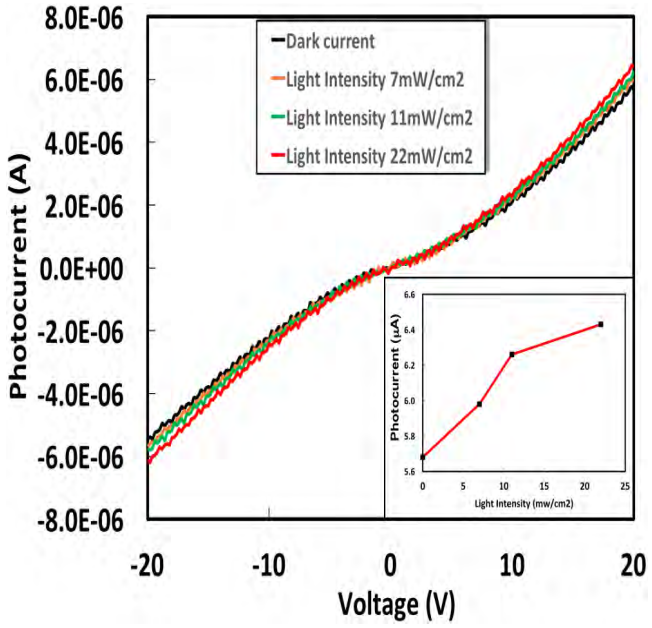

Fig. 5: Photoresponse of MoS_2 printed Resistor on Flexible polyimide film.

Shown in Fig. 5 is a photocurrent response of an inkjet printed MoS_2 resistor at 20 V, taken in dark and then exposed to high light intensity. The light source used in the photocurrent measurement experiment was the LEDR/4 type illuminator which has a color temperature of 6500K. The inset in fig. 5 shows a photocurrent response with different light intensity in mW/cm^2 where 0 is indicating dark current and with the light intensity of $22mW/cm^2$ highest photocurrent 6.5 µA has been found in this experiment. We note that, while this response does not appear to be stable, in our future efforts we will design a device architecture that would allow for a more robust photocurrent response.

Fig. 6 (a) depicts an optical microscopy image of cells growing near a MoS2 sample prepared using CT deposited onto polyimide. Cells are growing near the sample and display normal shapes. Fig. 6 (b) illustrate the PET sample where cell did not proliferate and showing big dead cell zone around the sample.

In contrast, cells exposed to graphene and MoS_2 deposited onto PET samples showed a “dead zone” around the edges where no cells proliferated. This is a sign of some toxic material leaching from the samples. The gap was only present around PET and would often be accompanied by small dead circles further away from the material. The cell morphology near samples on polyimide film indicated better

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biocompatibility compared to the cells grown near the PET samples. For all the six polyimide samples the cells grew around the samples with high confluence. These samples appear more biocompatible, possibly due to the higher annealing temperature of 300°C, which may have led to better solvent evaporation from the material.

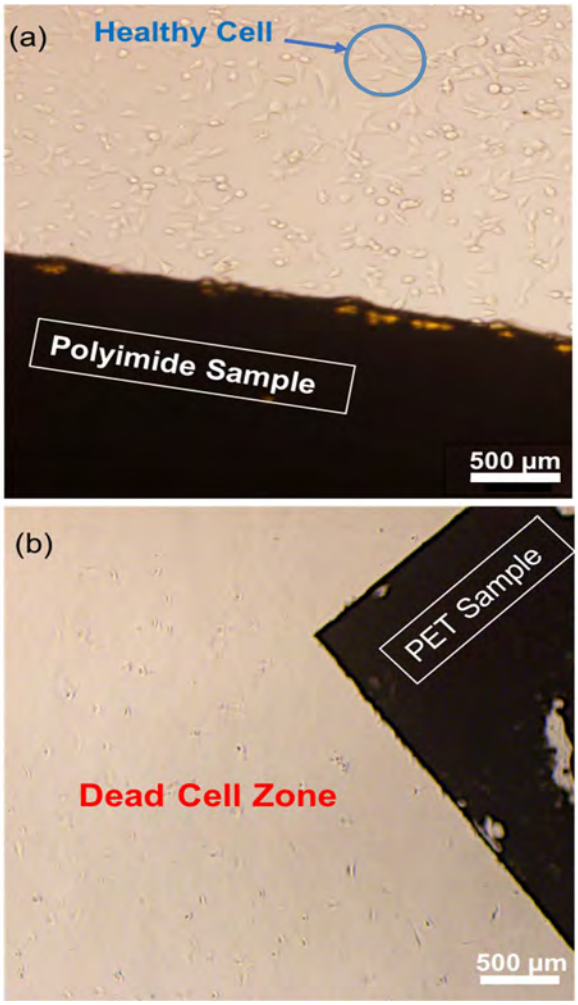

Fig. 6: Example of Optical microscopy of (a) polyimide sample showing high cell (STOs) confluence, (b) PET sample showing big dead cell area.

When observing polyimide film, and either CT, IPA or NMP were used as the solvent, both graphene and MoS_2 resulted in a confluence rate between 70-98 % where as PET samples showed a confluence rate between 15-60 % which is significantly lower. Moreover, wells containing MoS_2 on the polyimide film had a large amount of cells growing on the material, further indicating high biocompatibility.

Our future approach will be utilizing the Inkjet printing technique to fabricate hetero-junction photodetector for *in vivo* biomedical application.

IV. Acknowledgments

We would like to thank Julio Rincon from the Biomedical Device, Delivery, and Diagnostic Laboratory at the University of Texas at El Paso for help with the microscopy. Support is acknowledged from the University of Texas System Faculty Science and Technology Acquisition and Retention (STARS) award (EC284802) for the acquisition of equipment in the establishment of the Nanomaterials and Devices Lab (NDL) at the University of Texas, El Paso (UTEP). We also thank the Army Research Office (ARO) (grant number W911NF-15-1-0425) that enabled us to pursue this work.

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Effect of Carrier Lifetime Enhancement on the Performance of Ultra-High Voltage 4H-SiC PiN Diodes

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***Abstract*—A long minority carrier lifetime is desirable to improve the on-state performance of ultra-high voltage 4H-SiC bipolar devices. This paper presents a study of lifetime enhancement processes applied to lightly doped, free-standing 4H-SiC substrates. An optimized carbon implantation and annealing process is developed, which resulted in a lifetime of 9.7 µs (increased from 2.1 µs in as-received wafers). PiN diodes were fabricated on these wafers, which show improved on-state performance as compared to diodes fabricated on as-received wafers.**

Keywords—silicon carbide; high voltage; minority carrier lifetime; pin diode

I. INTRODUCTION

In recent years, silicon carbide (4H-SiC) PiN diodes have been a topic of intensive research for the development of ultra-high voltage (breakdown voltage ≥ 10 kV) power rectifiers, owing to the many attractive material properties of 4H-SiC such as high critical electric field, low intrinsic carrier concentration, high thermal conductivity and indirect bandgap with relatively long carrier lifetime [1]–[3]. Continuous improvements have been made in the development of techniques to enhance the minority carrier lifetime in 4H-SiC, such as high temperature thermal oxidation [4] or carbon implantation and annealing [5]. By employing such lifetime enhancement methods, coupled with proper junction termination designs, ultra-high voltage (UHV) diodes with breakdown voltage up to 27 kV and low forward voltage drop and differential on-resistance have been demonstrated [3].

The fabrication of 4H-SiC n-type bipolar devices such as n-channel insulated gate bipolar transistors (IGBTs) or gate turn-off thyristors is difficult due to the poor quality and high resistivity of heavily doped p-type 4H-SiC substrates. To circumvent this problem, we have demonstrated lightly doped free-standing 4H-SiC substrates by epitaxial growth of a thick n-type layer on an n^+ substrate, followed by substrate removal. We have successfully demonstrated PiN diodes, conventional IGBTs, and bi-directional IGBTs fabricated on such FSS wafers [6]–[8]. To further improve the on-state performance of these high voltage bipolar devices, it is necessary to increase the minority carrier lifetime to achieve better conductivity modulation in the on-state.

In this paper, we present for the first time, a study on the effect of lifetime enhancement processes on lightly doped free-standing 4H-SiC wafers. Two methods for lifetime enhancement have been studied, namely carbon implantation and high temperature oxidation. Various experimental results on the optimization of lifetime enhancement processes and lifetime measurement by optical methods on bare 4H-SiC wafers are reported in Section II. Based on these results, implanted anode pin diodes were fabricated on selected wafers, using processes described in Section III. A comparison of the electrical characteristics of diodes fabricated on as-received and lifetime enhanced diodes is presented in Section IV. To our knowledge, this is the first demonstration of carrier lifetime enhancement in free-standing, lightly doped 4H-SiC wafers.

II. CARRIER LIFETIME ENHANCEMENT

In this study, we have investigated two approaches towards increasing the minority carrier lifetime in free-standing 4H-SiC wafers, namely (a) carbon implantation and annealing and (b) high temperature dry oxidation. A comparison of the two lifetime enhancement techniques, as applied to FSS wafers, is presented in this section.

A. Carbon Implantation and Annealing

To study the effect of carbon implantation and annealing on carrier lifetime, two samples were prepared with different carbon implant doses (CLD – carbon light dose and CHD – carbon heavy dose). Carbon implant schedules were chosen to result in a uniform carbon concentration up to a depth of 0.25 µm with a concentration of 5×10^{18} cm^{-3} and 5×10^{20} cm^{-3} for CLD and CHD samples respectively. All carbon implants were performed at 600 °C on both sides of 180 µm thick 4H-SiC FSS wafers. After carbon implantation, a graphite capping layer was deposited on both sides of the wafer to protect the surface during high temperature drive-in annealing [9]. Drive-in annealing was performed at 1600 °C for 30 minutes in argon. It has been shown that for annealing temperatures higher than 1600 °C, *in-situ* generation of carbon vacancies overcomes the effect of carbon implantation, and results in a

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smaller increase in lifetime [5]. After annealing, the graphite cap was removed by a low temperature dry oxidation (900 ºC, 2 hours). The carbon implanted layer was removed by reactive ion etching (RIE) to a depth of 0.5 µm. Carrier lifetime was measured both optically using microwave photoconductivity decay (MPCD).

A comparison of the MPCD measurement on as-received, CLD and CHD samples is shown in . Clearly, from the longer decay of photoconductivity, the carrier lifetime was increased on both carbon implanted samples. The initial fast decay that is observed is due to surface recombination. The lifetime measured on the as-received, CLD and CHD samples was 2.12 ± 0.07 µs, 9.72 ± 0.58 µs and 9.47 ± 1.80 µs respectively. It can be seen that increasing the carbon dose did not have a significant effect on lifetime enhancement, suggesting that for these samples, a carbon doping of 5×10^{18} cm^{-3} can create enough interstitials to eliminate carbon vacancies. For 4H-SiC wafers with a smaller starting lifetime (i.e. higher concentration of $Z_{1/2}$ defects), higher carbon dose may be necessary to supply enough carbon interstitials. As shown in [10], MPCD measurements are strongly affected by surface recombination velocity, hence the lifetime estimated by this method represents a lower limit to the bulk recombination lifetime. The CLD sample was subjected to additional annealing for 2 hours at 1600 ºC, but no change in lifetime was observed. Although the experimental results presented here are from FSS wafers, similar results were obtained on 4H-SiC wafers with n^+ substrate as well.

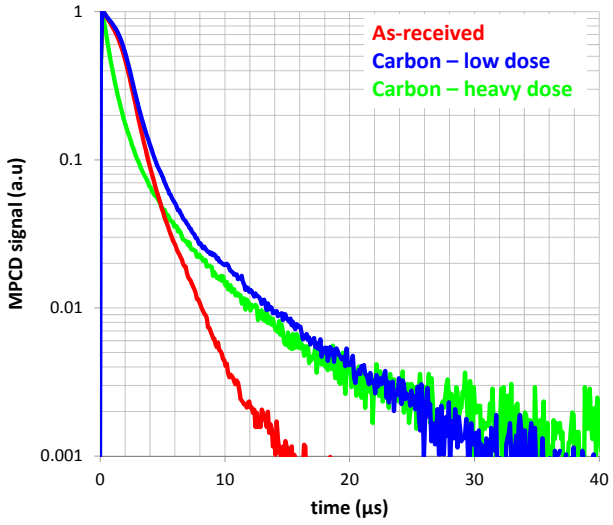

Fig. 1. MPCD measurements on as-received and carbon implanted 180 µm thick FSS 4H-SiC wafers. No passivation layers are used in these measurements.

B. High Temperature Oxidation

The effect of high temperature oxidation treatment on carrier lifetime of 4H-SiC FSS samples is discussed in this section. Dry oxidation was performed at 1400 ºC on FSS samples for different durations from 48 hours to 72 hours. After dry oxidation, the thermally grown SiO_2 layer was removed by wet etching in buffered HF and MPCD measurements were performed. The result of the MPCD measurement is shown in Fig. 2. After a 48 hour oxidation at 1400 ºC, the lifetime increased from 2.1 µs to about 6.0 µs. The same sample was then re-oxidized at 1400 ºC for an additional 24 hours (total oxidation duration = 72 hours) and the MPCD measurement procedure was repeated. No additional enhancement in lifetime was observed. The reasons for the smaller enhancement in carrier lifetime than values reported in literature [3] are unknown. Two possible reasons may be:

(a) The furnace used for high temperature oxidation has an alumina tube, which results in faster than expected oxidation rates due to sodium contamination [11]. Sodium enhanced oxidation (SEO) is known to result in very high channel mobility and low interface state density [12], [13]. Sodium enhanced oxidation may results in the generation of fewer carbon interstitials, which will result in a smaller increase in lifetime.

(b) Surface recombination may the limiting factor in the MPCD measurement on these samples. In some samples, the surface became very rough after high temperature oxidation (light reflection was not specular after oxidation and cleaning). A low surface roughness is critical for good channel mobility and oxide reliability in MOS gated devices such as IGBTs. Further CMP may be necessary to recover a smooth surface that can be used for UHV IGBT fabrication, after lifetime enhancement using the high temperature oxidation process.

Due to the smaller lifetime enhancement as well as the increase in surface roughness observed after dry oxidation, this method was not used for lifetime enhancement for any of the PiN diode wafers.

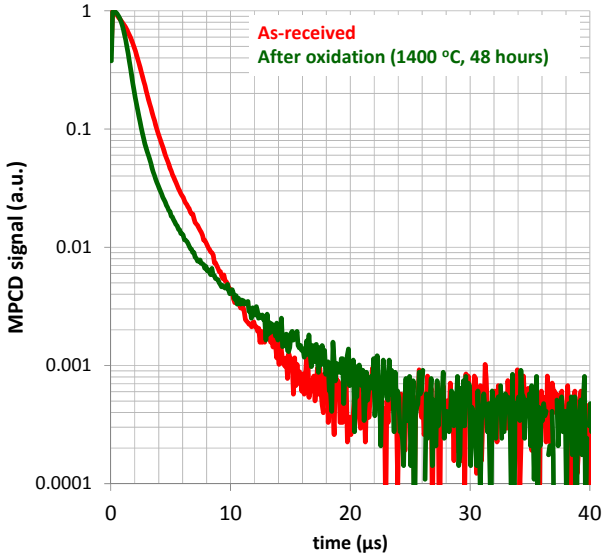

Fig. 2. MPCD measurements on as-received and oxidized 180 µm thick FSS 4H-SiC wafers. The measurement was performed after removing the thermally grown oxide layer.

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III. Device Fabrication

To quantify the effect of increased carrier lifetime on the electrical characteristics of UHV bipolar devices, implanted anode pin diodes were fabricated and characterized. The diodes were fabricated on 4H-SiC wafers with a thick n-type epitaxial layer (thickness = 180 µm, doping = 2×10^{14} cm^{-2}) grown on n^+ substrates. Carbon implantation and annealing was performed on one sample using the same process as the CLD sample described above. The anode region was formed by aluminum ion implantation with a box profile (depth = 0.6 µm, dose = 3.8×10^{15} cm^{-2}). A multiple-zone single-implant (MZ-SI) junction termination extension (JTE) region [14] with a width of 500 µm was formed by aluminum ion implantation (depth = 0.6 µm, dose = 3×10^{13} cm^{-2}). All implants were carried out at a temperature of 600 ºC. Activation anneal was performed at 1675 ºC for 30 minutes in argon ambient with a graphite capping layer. 1 µm thick SiO_2 deposited by PECVD followed by nitric oxide anneal (1175 ºC, 2 hours) was used as the field oxide. P-type and n-type ohmic contacts were formed by Al/Ni/Al and Ti/Ni/Al metal stack respectively, annealed for 2 min in argon at 1050 ºC. Finally, a 200 nm Ti/ 400 nm Mo metal stack was deposited and etched as the pad metal layer followed by a 400 ºC, 30 minute anneal in Ar/H_2. The diameter of the active area of the diodes was 200 µm.

IV. Electrical Characteristics

The forward I-V characteristics of pin diodes on as-received and lifetime enhanced samples are shown in Fig. 3. The on-state voltage drop (V_F) and differential specific on-resistance ($r_{on,diff}$) at an on-state current density of 50 A/cm^2 are shown in Fig. 4. From these result it is clear that there is an improvement in on-state performance for pin diodes on lifetime enhanced wafers, but only at elevated temperatures. At 200 ºC, the differential on-resistance for lifetime enhanced pin diodes is about 35 mΩ.cm^2, compared to 51 mΩ.cm^2 for as-received wafers. The differential on-resistance can be approximated by:

$$r_{on,diff} = \frac{dV}{dJ} \approx \frac{1}{qn^*(\mu_n + \mu_p)}$$

where n^* is the average excess carrier concentration in the drift layer, q is the electronic charge, μ_n is the electron mobility and μ_p is the hole mobility. Substituting the measured differential specific on-resistance values, n^* can be estimated to be about 5.4×10^{17} cm^{-3} and 3.7×10^{17} cm^{-3} in lifetime enhanced and as-received wafers respectively. At room temperature, the performance of pin diodes on both as-received and lifetime enhanced wafers is nearly identical.

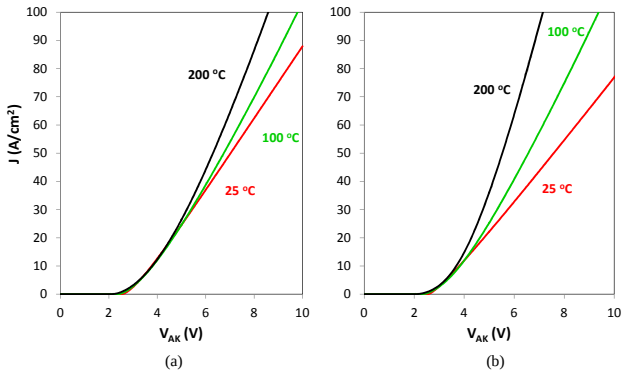

Fig. 3 Typical forward I-V characteristics at 25 ºC, 100 ºC and 200 ºC for 4H-SiC pin diodes fabricated on (a) as-received and (b) lifetime enhanced wafers

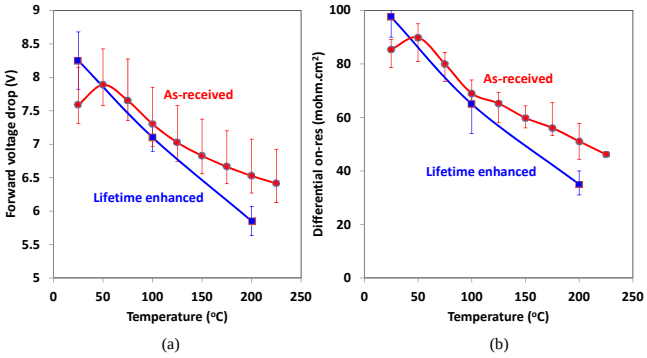

Fig. 4 (a) Forward voltage drop (at 50 A/cm^2) and (b) differential specific on-resistance for 4H-SiC pin diodes fabricated on as-received and lifetime enhanced wafers

The carrier lifetime extracted by open circuit voltage decay (OCVD) measurements on these diodes is shown in Fig. 5. Although the lifetime measured by MPCD on the starting wafers was nearly 10 µs, the lifetime measured by OCVD on fabricated devices is only about 3.2 µs at room temperature. This indicates that lifetime decreases during the device fabrication process, most likely during the high temperature annealing step, which has been shown to generate additional $Z_{1/2}$ and $EH_{6/7}$ defects.

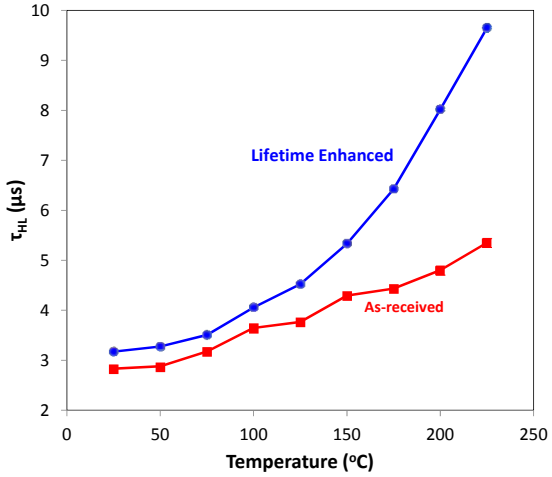

Fig. Carrier lifetime extracted by OCVD measurements on 4H-SiC pin diodes fabricated on as-received and lifetime enhanced wafers

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V. SUMMARY

.In summary, we have investigated two lifetime enhancement processes for lightly doped, free-standing 4H-SiC wafers. The carrier lifetime in the as-received wafers was about 2.0 – 2.5 µs, which was increased to 9.7 µs following carbon implantation and annealing. High temperature dry oxidation at 1400 ºC resulted in a smaller increase in lifetime to about 6 µs. Implanted anode pin diodes were fabricated on carbon implanted wafers to assess the effect of lifetime enhancement on the electrical characteristics of high voltage bipolar devices. At elevated temperatures (200 ºC), diodes fabricated on lifetime enhanced wafers show significant improvement in on-state characteristics such as a lower V_F and $r_{on,diff}$. OCVD measurements also confirmed a higher carrier lifetime in the lifetime enhanced devices. These results demonstrate that such lifetime enhancement techniques can be successfully used to improve the performance of UHV devices fabricated on FSS wafers such as IGBTs and GTOs.

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Comparing Buffer Leakage in PolarMOSH on SiC and Free-Standing GaN Substrates

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***Abstract*—GaN MOSHEMT or MOSFET on top of conducting (drift layer and drain electrode) layers is a building block for vertical GaN VDMOS power transistors. GaN MOSHEMTs incorporating a polarization-doped p-AlGaN layer as the back barrier on top of conducting layers is named as PolarMOSH. In this work, we present a comparative study of PolarMOSH fabricated on SiC and free-standing GaN substrates. PolarMOSH wafers epitaxially grown on SiC substrates are found to suffer from large leakage currents, with or without Mg doping in the back barrier. Much lower leakage currents are achieved when PolarMOSH wafers are grown on free-standing GaN substrates. The large reduction of buffer leakage current is attributed to the much reduced dislocation density brought by free-standing GaN substrates. The PolarMOSH fabricated on free-standing GaN substrates has a current On/Off ratio $> 10^{10}$ thanks to the low leakage current.**

I. Introduction

Free-standing GaN substrates with continuously improved quality and lowered cost have paved the way for realizing vertical GaN power devices, promising high conduction current but low on-resistance, high blocking voltage and fast switching speed. GaN Metal-Oxide-Semiconductor High Electron Mobility Transistor (MOSHEMT) or MOSFET on top of conducting (drift and drain electrode) layers is an essential element for vertical GaN VDMOS power transistors. GaN MOSHEMTs with a polarization-doped p-AlGaN back barrier on top of conducting layers is named as PolarMOSH. It is a building block for the novel vertical GaN device PolarMOS [1], which takes advantage of the unique polarization properties of GaN for power applications. The cross section schematics of both PolarMOS and PolarMOSH are illustrated in Fig. 1.

Experimental realization of HEMTs with a p-type back barrier grown on unintentionally-doped (UID) GaN or n-GaN has been challenging due to the high buffer leakage as well as difficulty in junction placement due to Mg. In metal-organic chemical vapor deposition (MOCVD) growth, Mg tends to incorporate in subsequently grown layer [2], [3], resulting in compensation effects that prevent formation of two dimensional electron gas (2DEG). Chowdhury *et al.* [4] showed that the Mg diffusion could be suppressed through insertion of an AlN layer or a C doped GaN layer. However,

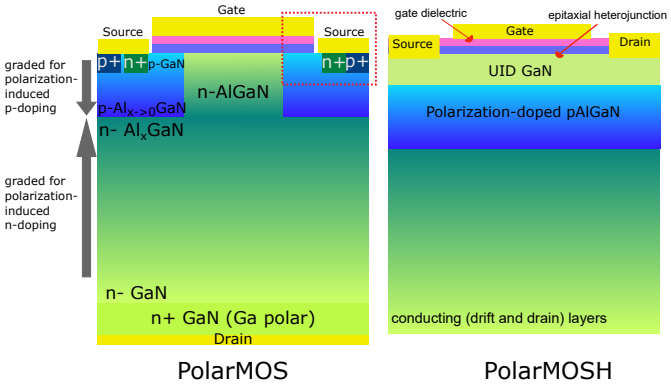

Fig. 1. Cross section schematics of PolarMOS (left) and PolarMOSH (right). PolarMOS is a novel vertical GaN power transistor [1]. PolarMOSH is a GaN MOSHEMT with a polarization-doped p-AlGaN back barrier on top of conducting layers. It is a building block for PolarMOS, as illustrated by the red rectangle in the left figure.

in their experiments, Mg doping is carried out through ion implantation and the subsequent layers were regrown using molecular beam epitaxy. The regrowth interface often has high densities of impurities due to exposure to the atmosphere, which leads to high leakage current [5].

Here we present the first realization of PolarMOSHs, on free-standing GaN substrates and illustrate the adverse effect of dislocations on buffer leakage by comparing PolarMOSHs grown on SiC and GaN substrates. The experiments started with PolarMOSH epitaxial structures grown on SiC substrates, which show a persistently large buffer leakage current since the p-$Al_xGa_{1-x}N$ barrier does not effectively block leakage current between 2DEG channel and the underlying layers due to excessive amount of dislocations ($\sim 10^9$ cm^{-2}). The involvement of Mg doping is found to prevent the formation of 2DEG channel as well as alloyed ohmic contacts. Then the PolarMOSH epitaxial structure was carefully improved to reduce the effects of Mg doping on the 2DEG channel and grown on free-standing GaN substrates. The fabricated PolarMOSHs on free-standing GaN substrates show a high current On/Off ratio of $> 10^{10}$ and a low drain leakage current

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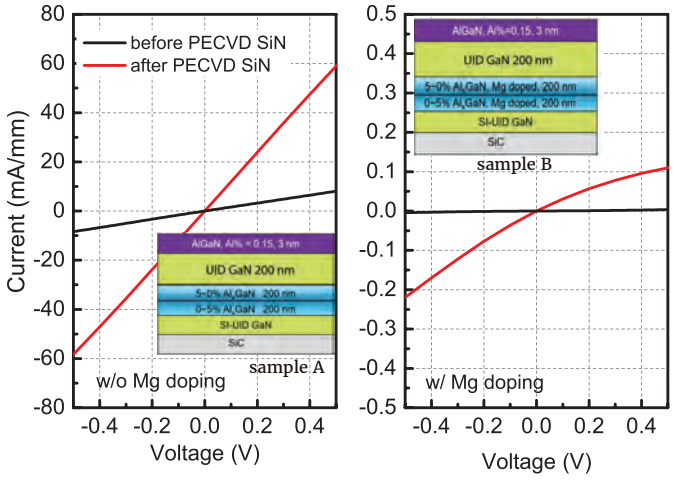

Fig. 2. Comparison of *I-V* characteristics of a pair of ohmic contacts (2 μm separation) before and after 20 nm PECVD SiNx deposition on (left) sample without Mg doping and (right) sample with Mg doping. Mg doping causes large decrease in measured currents.

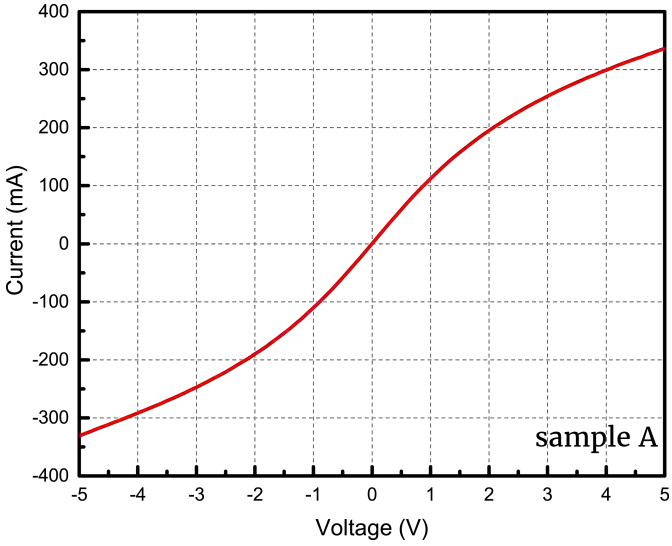

Fig. 3. *I-V* characteristics of a pair of ohmic contacts (2 μm separation) after 20 nm PECVD SiNx deposition on sample without Mg doping. $I > 300$ mA/mm at 5 V bias.

of < 1 pA/mm .

II. Experiments and Discussions

Two epitaxial structures were first designed to study the effects of graded $Al_xGa_{1-x}N$ and Mg doping. Both structures were grown on SiC substrates by MOCVD, consisting of a high-resistivity UID GaN layer, 0∼5% graded $Al_xGa_{1-x}N$, 5%∼0 graded $Al_xGa_{1-x}N$ (with or without Mg), 200 nm UID-GaN, 3 nm $Al_{0.15}Ga_{0.85}N$, while the only difference between the two device structures is the Mg doping in the back barrier. The epitaxial structures were designed for enhancement-mode (E-mode); 20 nm plasma-enhanced chemical vapor deposition (PECVD) SiNx, which is found to increase the 2DEG concentration thus reduce sheet resistance [6], was deposited after Ohmic contacts formation (alloyed Ti/Al/Ni/Au). Figure 2 shows the comparison of *I-V* characteristics of ohmic contacts before and after SiNx deposition on both samples. As can be seen from both plots in Fig. 2, 20 nm PECVD SiNx is effective in increasing measured current density for both epitaxial structures. However, the measured current density values are quite different. While the current through a pair of ohmic contacts separated by 2 μm could reach 60 mA/mm at 0.5 V bias on the sample without Mg doping, it barely exceeds $\sim$ 0.2 mA/mm on the sample with Mg doping.

Fig. 3 shows the *I-V* characteristics a pair of ohmic contacts separated by 2 μm on the sample without Mg doping, showing a conduction current > 300 mA/mm at 5 V bias. This $I-V$ behavior indicates that the channel 2DEG is compensated by Mg in the sample with Mg-doped back barriers, which is similar to Fe-doped or C-doped back barriers. Secondary ion mass spectrometry (SIMS) measurements (not shown here) show a residue Mg level of 1×10^{17} cm^{-3} near the 2DEG channel region.

Figure 4 shows the comparison of buffer leakage currents, with an excessive leakage current observed on both samples at 20 V bias. Device isolation on both samples are realized through 100 nm Cl_2 based dry etching using reactive ion etching (RIE). The buffer leakage test structure includes a pair of mesa isolated ohmic contacts separated by 10 μm. Although the Mg doping reduces the buffer leakage current at low bias voltage range, the leakage currents are within the same order of magnitude at 20 V. The large dislocation density in GaN grown on SiC substrates have most likely resulted in the buffer leakage current increase as the bias voltage increases. To identify whether the leakage current flows through the buffer layer below the $Al_xGa_{1-x}N$ back barrier, additional etching of 700 nm on the PolarMOSH sample is carried out after PolarMOSH fabrication. The leakage current after 100 nm and 800 nm mesa etching is plotted in comparison in Fig. 5. Also plotted in Fig. 5 is the leakage current on a GaN-on-Si HEMT [7], [8]. A 10^5X reduction in leakage current is observed when the etch depth is increased from 100 nm to 800 nm, suggesting that the $Al_xGa_{1-x}N$ layer and the UID GaN layer above contributes to most of the leakage current. However a further study is required to find out the exact amount of leakage current for each leakage path denoted in the upper inset plot in Fig. 5. The leakage current after 800 nm deep etching is still orders of magnitude larger than the GaN-on-Si HEMT, which has an impurity-doped semi-insulating GaN buffer layer. This indicates that the leakage path through the $Al_xGa_{1-x}N$ to the underlying SI-UID layer (as illustrated in the lower inset plot in Fig. 5), is due to the excessive amount of dislocations.

Following the mesa etch of 100 nm by RIE, the subsequent PolarMOSH fabrication process includes: gate lithography and RIE etching of PECVD SiNx, 20 nm Al_2O_3 deposition by atomic layer deposition (ALD) and gate metal deposition. The

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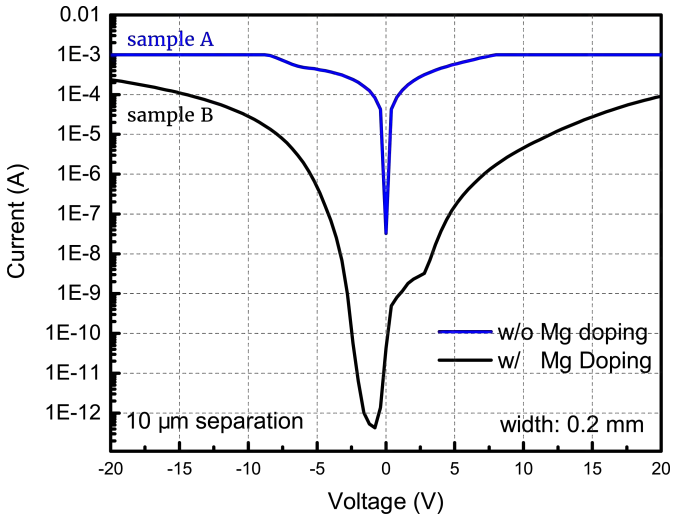

Fig. 4. Buffer leakage current comparison between sample A (without Mg doping) and sample B (with Mg doping). Although Mg doping reduces leakage current at low voltage bias, both samples show large leakage current at 20 V.

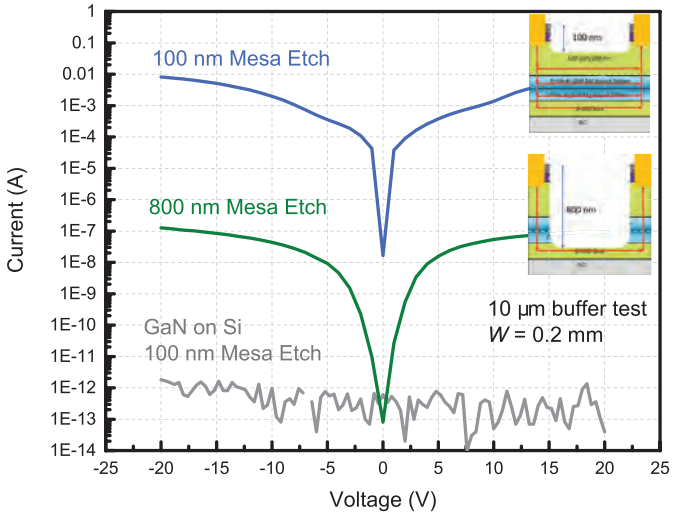

Fig. 5. Leakage current comparison between sample A with 100 nm and 800 nm mesa etching. Also plotted is the leakage current on a GaN-on-Si HEMT [7], [8]. A large leakage current reduction is observed after deep etching, although the reduced leakage current is still orders of magnitude larger than that on the GaN-on-Si sample. The possible leakage path after 100 and 800 nm etching are denoted as red arrow lines in the inset plots.

I_D-V_D characteristics of the PolarMOSH fabricated on the sample without Mg doping is shown in Fig. 6 along with its cross-section schematic. Although a clear gate modulation of drain current is seen from the plot, indicating the presence of electron channel, the excessive buffer leakage current prevents a complete turn-off of the drain current.

We have recently successfully demonstrated a series of GaN-on-GaN p-n diodes, which show unity ideality factor, avalanche breakdown and a record-setting figure-of-merit BV^2/Ron of $>$ 16 GW/cm^2 [9]–[11]. This indicates that growing the PolarMOSH device structure on bulk GaN substrates (dislocation density $\sim 10^6$ cm^{-2}) is attractive in solving

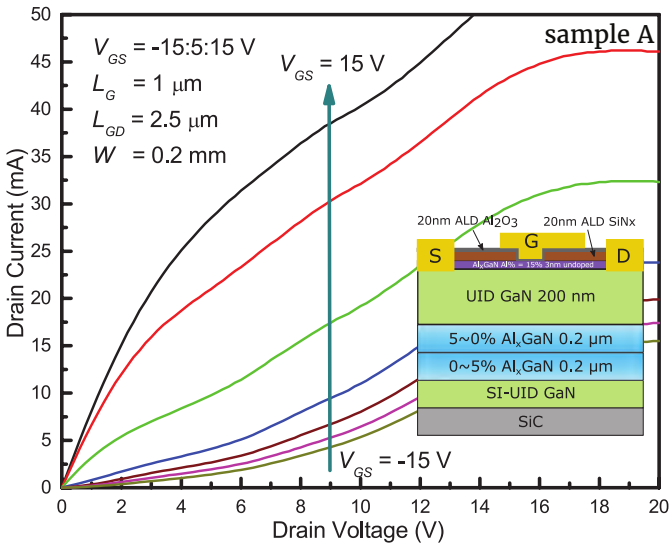

Fig. 6. $I_D - V_D$ characteristics of MOSHEMT fabricated with sample A (No Mg doping). Clear gate modulation of drain current is shown. Large leakage current inhibits complete turn-off of drain current.

the buffer leakage issue. As illustrated in Fig. 7 (a), the epitaxial structure, starting from the GaN substrate, includes: 7 μm Si doped n type GaN, 1 μm graded $Al_xGa_{1-x}N$ with polarization induced doping, 400 nm Mg doped graded $Al_xGa_{1-x}N$, 400 nm UID GaN, 20 nm $Al_{0.15}Ga_{0.85}N$ and 2 nm GaN cap. This epitaxial structure is designed for depletion mode thus a quicker evaluation of the 2DEG channel is possible; the top AlGaN barrier thickness can be reduced for E-mode devices. The PolarMOSH fabrication process is similar to that carried out on SiC substrate, except that the D-Mode epitaxy design eliminated the need of PECVD SiNx to form ohmic contacts. The fabrication process flow includes: ohmic contacts through Ti/Al/Ni/Au deposition and rapid thermal annealing, mesa isolation by dry etching, Al_2O_3 deposition by ALD and gate metal deposition.

The I_D-V_G characteristics of the fabricated PolarMOSH on free-standing GaN substrates is plotted in Fig. 7 (b), with the inset figure showing the cross section schematic. It is seen that an On/Off ratio $> 10^{10}$ and a drain off-current < 1 pA/mm are achieved. The large On/Off ratio, enabled by the low leakage current through the Mg doped graded $Al_xGa_{1-x}N$ layer as well as gate oxide, shows that the current blocking capability of Mg doped graded $Al_xGa_{1-x}N$ is vastly improved when grown on free-standing GaN substrates. This improvement in leakage current could be attributed to the much lower dislocation density in GaN grown on GaN substrates compared to GaN grown on SiC substrates [12], 1×10^6 cm^{-2} versus 1×10^9 cm^{-2}. As dislocations provide a vertical leakage path between the 2DEG above the p-layer and the conducting layer below the p-layer, reduction in dislocation density results in a reduction in measured buffer leakage current. The sharp turn-on behavior of drain current at $V_G \sim 5$ V also shows that the compensation effects by Mg is limited.

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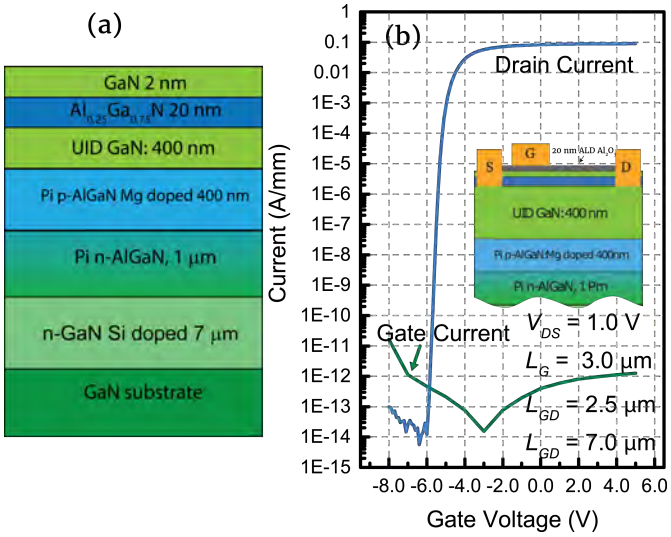

Fig. 7. (a) Epitaxial structure of PolarMOSH on free-standing GaN substrates. (b) The $I_D - V_G$ characteristics of the fabricated PolarMOSH. The inset figure in (b) shows the cross section schematic of the fabricated PolarMOSH.

III. Conclusion

In conclusion, we compare the leakage current behavior of PolarMOSH fabricated on SiC and free-standing GaN substrates. It is found out that the PolarMOSH fabricated on SiC substrates suffers from a large buffer leakage current. Though Mg doping in the graded $Al_xGa_{1-x}N$ back barrier reduces the leakage current, the channel residue Mg concentration is too high to form a 2DEG after depositing SiNx. The PolarMOSH fabricated on free-standing GaN substrates, shows a low drain leakage current of < 1 pA/mm and a high On/Off ratio of $> 10^{10}$. The much improved leakage characteristics could be attributed to the lower dislocation density of GaN grown on free-standing substrates than on SiC substrates. The device performance improvement shows the benefits of the superior quality of free-standing GaN substrates.

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InAlGaN/GaN-HEMT Device Technologies for W-band High-Power Amplifier

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***Abstract*—We demonstrated an excellent output power (P_{out}) density performance using a novel InAlGaN/GaN-HEMT with an 80-nm gate for a W-band amplifier. To eliminate current collapse, a unique double-layer silicon nitride (SiN) passivation film with oxidation resistance was adopted. The developed discrete GaN-HEMT achieved a P_{out} density of 3.0 W/mm at 96 GHz, and we fabricated W-band amplifier MMIC using the air-bridge wiring technology. The P_{out} density of the MMIC reached 3.6 W/mm at 86 GHz. We proved the potential of the developed InAlGaN/GaN-HEMT experimentally using our unique device technology. With the aim of future applications, we developed a novel wiring-inter-layer technology. It consists of a cavity structure and a moisture-resistant dielectric film technology. We demonstrated excellent high-frequency performances and low current collapse originating in humidity-degradation using AlGaN/GaN-HEMT. This is also a valuable technology for InAlGaN/GaN-HEMT.**

Keywords— HEMTs; Millimeter wave devices; Millimeter wave transistors; Amplifier; MMICs; Wireless communication; GaN; InAlGaN;

I. INTRODUCTION

GaN-HEMTs have a potential as devices for high-power millimeter-wave amplifiers [1-2]. A high-output GaN power amplifier can be used in a high-capacity wireless network with a coverage over a radius of several kilometers. In addition, high-capacity wireless networks play an effective role in emergency communication security. High-capacity wireless communication requires a higher-frequency carrier but the atmospheric attenuation increases when the frequency is higher than 100 GHz. Therefore, W-band (75-110 GHz) is an appreciated frequency range for wireless communication. This requires high-power amplifiers (PAs) for long communication distances, and small antennae [3-5]. Until to now, we have developed AlGaN/GaN-HEMT for W-band amplifiers, and its P_{out} density reached up to 1.5 W/mm at 96 GHz. To increase power density, many researches have been carried out. These showed that an approach towards increasing power density is to adopt an In-based nitride semiconductor HEMT[6-9].

In order to develop a W-band amplifier, the development of a wiring technology is also important. An amplifier monolithic microwave integrated circuit (MMIC) requires a low capacitive wiring interlayer technology. Up to now, we developed a cavity structure using benzocyclobutene (BCB). This technology improved high-frequency performances but BCB had a poor moisture resistance. To our knowledge, moisture causes degradation of the semiconductor. Our experimental results shows that it causes a current collapse of GaN-HEMT.

II. GAN-HEMT DEVICE TECHNOLOGY

A. HEMT structure for high-output amplifier

A HEMT uses an In-based nitride semiconductor material as a barrier material that achieves a high carrier density exceeding 1.6×10^{13}cm^{-2} because of its high polarization charge density. On the other hand, the carrier density of our conventional AlGaN/GaN-HEMT is 1.0×10^{13}cm^{-2}. Therefore, our approach towards increasing the power density of the amplifier involves adopting an In-based nitride semiconductor as a barrier layer of a HEMT. According to our experimental results, InAlGaN/GaN-HEMT, a high Al composition barrier, is an attractive material. Fig. 1 shows the two-terminal gate forward characteristics of InAlN/GaN-HEMT and InAlGaN/GaN-HEMT, and Fig. 2 shows atomic force microscope (AFM) images of the InAlN barrier surface of InAlN/GaN-HEMT and the InAlGaN barrier surface of InAlGaN/GaN-HEMT.

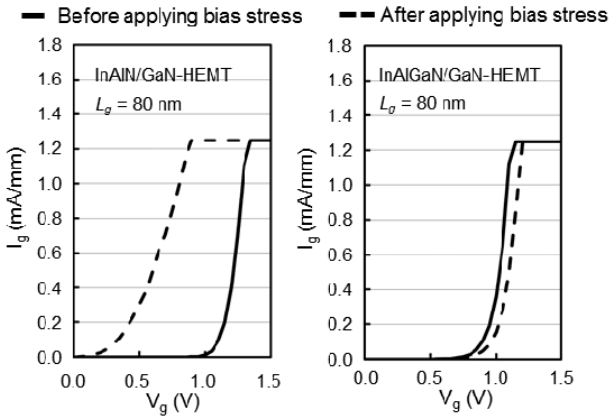

Fig. 1 Two-terminal gate forward characteristics. InAlN Schottky interface degradation of InAlN/GaN-HEMT occurred by a bias stress (applied max. Vg = 2 V, Vd = 20 V)

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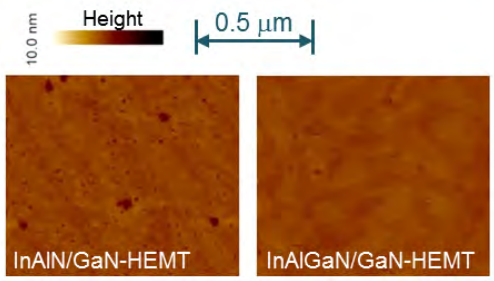


Fig.2 AFM images. Pits reach up to the vicinity of the GaN channel. These cause degradation of the Schottky interface of the InAlN barrier and gate metal. The InAlGaN barrier can decreases the pit density.

To our knowledge, theses pits are generated by the pit-origin on the AlN interlayer. We concluded that these pits cause degradation of the Schottky interface performance. These experimental results show that a part of the current InAlN Schottky interface of the barrier degraded because of bias stress similar to the bias stress that is seen in the amplifier operation. According to the MOCVD crystal growth mechanism, Ga atoms suppress the generation of these pits. Therefore, we concluded that the InAlGaN barrier is adequate in the present situation, although improve the quality of InAlN barrier lattice matching the GaN channel is expected.

B. Device Technology

A device structure and process technologies have been developed. A low-trap passivation, offset overhanging gate structure was adopted. Fig.3 shows the developed device structure. In-based barrier generates a large amount of two-dimensional gas density even if the thickness decreases. We adopted an InAlGaN barrier layer in our developed device.

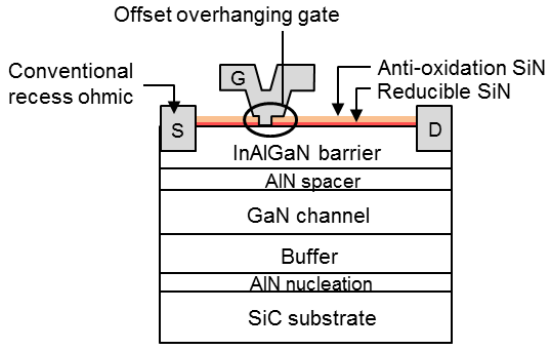
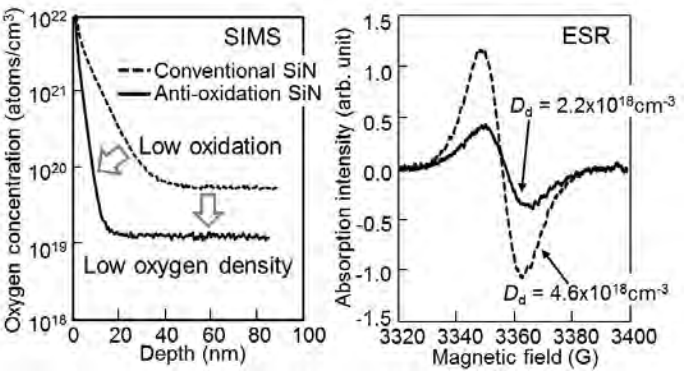


Fig. 3 Cross-sectional view of developed InAlGaN/GaN-HEMT. Surface was covered with low-trap double-layer passivation film.

To suppress a current collapse, a double-layer silicon nitride (SiN) passivation film was adopted. This consists of reducible SiN lower-layer and anti-oxidation upper-layer. This is one of the key technologies for improving the current collapse. The reducible lower-layer was developed to decrease Ga oxide on the surface of AlGaN/GaN-HEMT [10]. It decreases the trap density on the surface of the semiconductor. Furthermore, we developed an anti-oxidation upper layer to decrease trap density in silicon nitride and on the surface of the passivation film. Fig. 4 (a) shows the oxygen concentration depth profile. The measured results show that the developed anti-oxidation SiN prevents itself from oxidation. These chemical properties decrease the electron trap density in silicon nitride and on the surface of the passivation film. The measured results as shown in Fig. 4 (b) are supported by a decrease in the measured dangling bond density.



(a) SIMS (b) ESR

Fig. 4 Oxygen and dangling bond density (D_d) in anti-oxidation silicon nitride were evaluated by SIMS and electron spin resonance (ESR).

C. Current Collapse

Fig. 5 (a) shows the pulse-IV characteristics of our conventional AlGaN/GaN-HEMT, and Fig. 5 (b) shows that of the developed InAlGaN/GaN-HEMT. The current collapse of InAlGaN/GaN-HEMT was very small although that of both types of devices was decreased. In general, the electric field near the 80-nm gate increases, and it increases a current collapse.

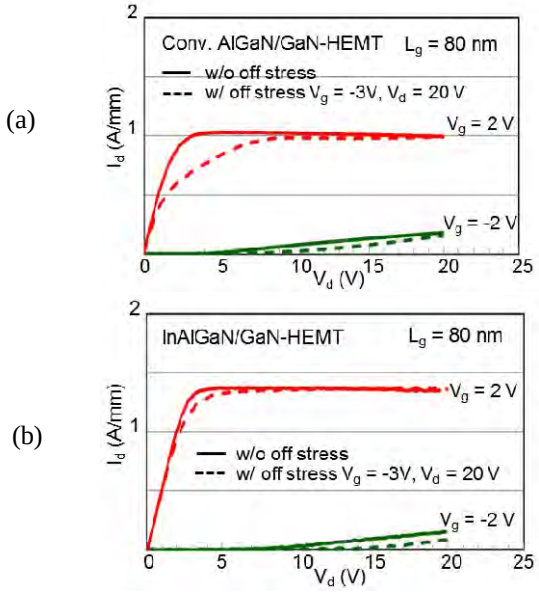


Fig. 5 Pulsed-IV characteristics were measured. Experimental results showed an extreme low current collapse in an InAlGaN/GaN-HEMT.

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These experimental results indicate that a large conduction band discontinuity (ΔE_c) between the InAlGaN barrier and GaN channel (AlGaN/GaN: 0.38 eV, the InAlGaN/GaN: 1.25 eV) suppressed the hot electron transfer from the channel to the surface trap on the device. Thus, this improvement of current collapse indicated that a chemical mechanism and a physical mechanism improved it. This result shows potential for improvement in the P_{out} density [11].

D. Power charactristics of HEMT and MMIC

Fig. 6 shows the P_{out} performances of the fabricated InAlGaN/GaN-HEMT using a W-band load-pull measurement system with pre-matched circuits. The developed HEMT demonstrated an excellent P_{out} density of 3.0 W/mm at 96 GHz with 20 V, under a continuous wave (CW) operation.

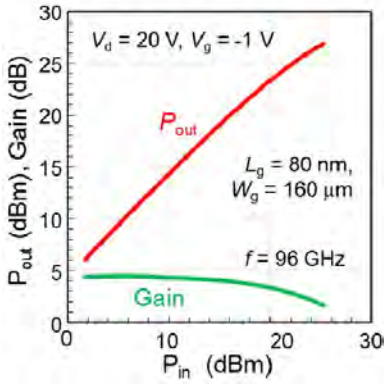

Fig. 6 Discrete InAlGaN/GaN-HEMT demonstrated an excellent P_{out} density of 3.0 W/mm at 96 GHz with 20 V, under CW operation.

Next, we fabricated a W-band high-power-density monolithic microwave integrated circuit (MMIC) PA using developed 80-nm InAlGaN/GaN HEMTs. The MMIC consisted of two-stage cascade units, each of which had two transistors with the same gate periphery for a high-gain and low-loss matching circuit using air bridge wiring. The MMIC under CW operation achieved a maximum P_{out} of 1.15 W, a P_{out} density of 3.6 W/mm, and a maximum PAE of 12.3% at 86 GHz as shown in Fig. 7.

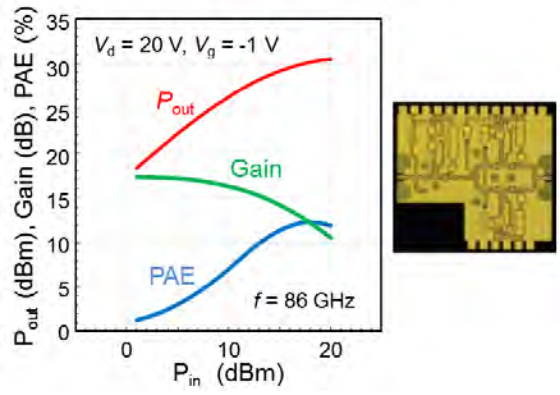

Fig. 7 P_{out} density of amplifier MMIC reached up to 3.6 W/mm, and the maximum PAE of 12.3%, at 86 GHz, CW operation.

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The fabricated InAlGaN/GaN-HEMT amplifier MMIC in this work realized both the highest frequency and the highest P_{out} density operation [12].

III. Novel Wiring Technology

Our currently developed W-band amplifier MMIC adopts the air-bridge wiring technology. Therefore the surface of the device comes into contact with the air. To our knowledge, the moisture in the air causes a current collapse. However, even low-k wiring-interlayer cannot be used in a W-band amplifier MMIC because the parasitic capacitance originating in the wiring interlayer degrades the high-frequency performance. For mass production, an innovative wiring technology is desired.

A. Cavity strucute and moisture resistance

Until now, we developed a cavity structure using benzocyclobutene (BCB) [13]. This structure is adopted in our current ultra-high-frequency InP-HEMT integrated circuits as shown in Fig. 8. It decreased the parasitic capacitance around the gate electrode. This improves high-frequency performances, but BCB has a poor moisture resistance. To our knowledge, moisture causes a degradation of electric characteristics of devices, and also causes a current collapse of GaN-HEMT.

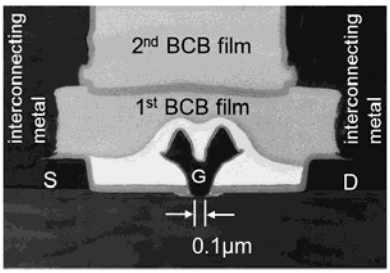

Fig. 8 Cavity structure adopted in InP-HEMT IC

To adopt the cavity structure in W-band GaN-HEMT MMIC, a hydrophobic methylsilsesquioxane (MSQ) -based wiring interlayer film was adopted instead of a BCB wiring interlayer. Fig. 9 shows a cross-sectional view of the developed AlGaN/GaN-HEMT and photographs that show the water contact angles. These results indicate that the MSQ-based wiring interlayer film kept the hydrophobicity even in the side wall of the contact hole.

A high-temperature and high-humidity test has been performed. The results indicate that a hydrophobic MSQ-based wiring interlayer film prevented the ingress of moisture. It suppressed the degradation originating in moisture, and achieved a low current collapse as shown in Fig. 10 [14].

Furthermore, the cavity structure decreases the parasitic capacitance around the gate electrode and improves high-frequency performance. It improves the high-frequency performance of a AlGaN/GaN-HEMT as shown in Fig. 11 [15]. This cavity structure can be applied to InAlGaN/GaN-HEMT and various other HEMTs.

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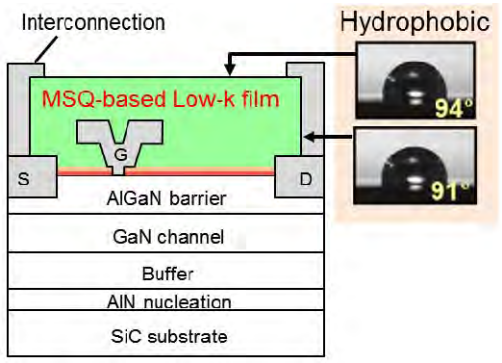

Fig. 9 MSQ-based wiring interlayer film achieved excellent hydrophobicity even in the side-wall of the contact hole.

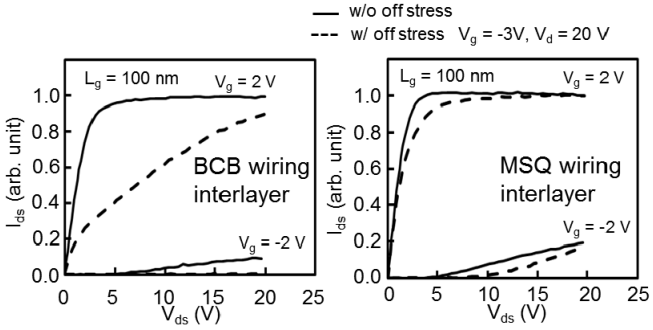

Fig. 10 Pulse IV characteristics after 60 min humidification test. MSQ-based wiring interlayer film achieved low current collapse.

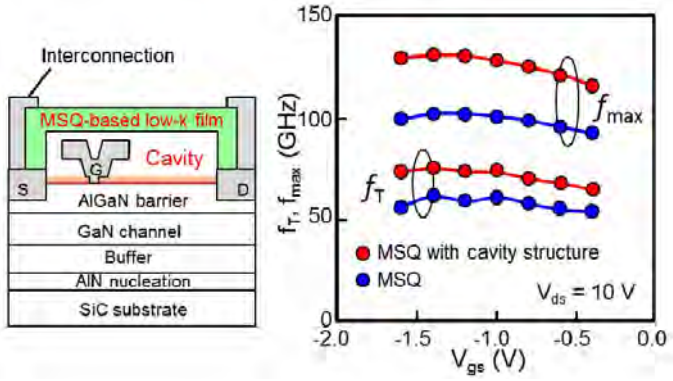

Fig. 11 Cross-sectional view of AlGaN/GaN-HEMT. An MSQ-based low-k film with cavity structure was adopted, and the cavity structure achieved a high-frequency performance.

IV. Conclution

In summary, fabricated InAlGaN/GaN-HEMT demonstrated an excellent P_{out} density of 3.0 W/mm at 96 GHz with 20 V under a CW operation. The P_{out} density of the amplifier MMIC reached 3.6 W/mm, with a maximum PAE of 12.3%, at 86 GHz. Furthermore, our cavity structure prevented the device from suffering moisture degradation, and improved high-frequency performance. This wiring technology is an encouraging candidate for W-band amplifier MMIC.

Acknowledgment

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Low-dispersion 180° Phase Shifter Using Two Synchronized MEMS Switches

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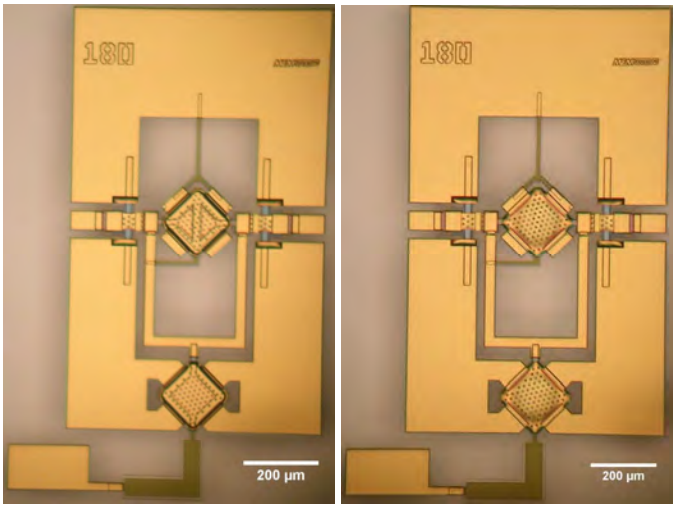
***Abstract*—Previously, the design of our novel low-dispersion phase-shifter unit cell with two asynchronous MEMS switches was limited to 90°, so that four unit cells (90°, 90°, 90° and 45°) with a total of eight MEMS switches were required for a 3-bit phase shifter. This not only increased the size and loss of the phase shifter, but also decreased its yield and reliability. Recently, we hypothesized that by using two synchronized MEMS switches, the phase shift of a unit cell could be extended to 180° so that only three unit cells (180°, 90° and 45°) with a total of six MEMS switches would be required for a 3-bit phase shifter. This paper confirms the hypothesis with measured characteristics of a fabricated 180° phase-shifter unit cell. The measured characteristics compare well with both equivalent-circuit model prediction and three-dimensional finite-element electromagnetic simulation, provided the worse-than-expected loss from individual MEMS switches is taken into account. The results provide the proof of the design principle, so that with improved MEMS fabrication process such as thicker metallization, the switch loss can be reduced and low-dispersion phase shifters can be realized with compact size, low loss, low cost, and high reliability.**

Keywords— Metamaterials; micro-electromechanical systems; microwave filters; phase shifters; tuning; switch.

I. INTRODUCTION

Low-dispersion phase shifters are key components for electrically large phased-array radar and communication systems. Unlike true-time-delay phase shifters with linear dispersion, low-dispersion phase shifters can be designed by switching between right-handed (low-pass) and left-handed (high-pass) states to achieve a constant phase shift over a wide bandwidth [1]. However, the implementation of low-dispersion phase shifters with MEMS switches has been challenging. The designs to date suffer from either high insertion loss [2] or high dispersion [3], [4]. Most important, they all occupy a large area and use a large number of MEMS switches, which negatively impact the yield and reliability, especially in view of the relatively immature RF MEMS technology. This paper reports proof of principle for the 180° unit cell of our previous hypothesis with only two MEMS switches [5]. By further improving the MEMS fabrication process this unit cell paves the way to realize the design of phase shifters with smaller size and fewer MEMS switches while having lower dispersion and insertion loss.



(a) (b)

Fig. 1. Micrographs of a 180° unit cell with two (a) actuated and (b) unactuated MEMS switches in series and shunt configurations, respectively. The unit cell is approximately 1.5 mm × 1 mm.

II. DESIGN PRINCIPLE

Fig. 1. shows the micrographs of the fabricated 180° unit cell in both actuated (through) and unactuated (delay) states. The design is based on a coplanar slow-wave structure with defected ground tightly wrapped around two single-pole-single-throw MEMS capacitive switches. The two MEMS switches, in series and shunt configurations, respectively, are simultaneously actuated to switch the unit cell from the delayed state to the through state [3], [5]. Both MEMS switches have a square-shaped movable electrode with four long and narrow slits along each side, so that the movable electrode is anchored only at the four corners in the north, south, east and west directions of Fig. 1. This not only makes the MEMS switch more compact, but also increases its tolerance of variations in temperature and residual stress [6]. The series switch differs from the shunt switch mainly by splitting the stationary electrodes into two halves as shown in Fig. 1(a). Pull-in voltage for the series switch differs from that of the shunt switch by approximately 5 V (37 V vs. 32 V) because of approximately 25% smaller stationary electrode.

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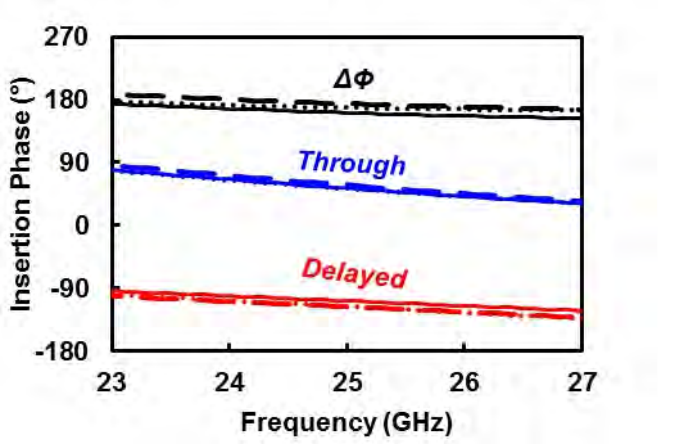
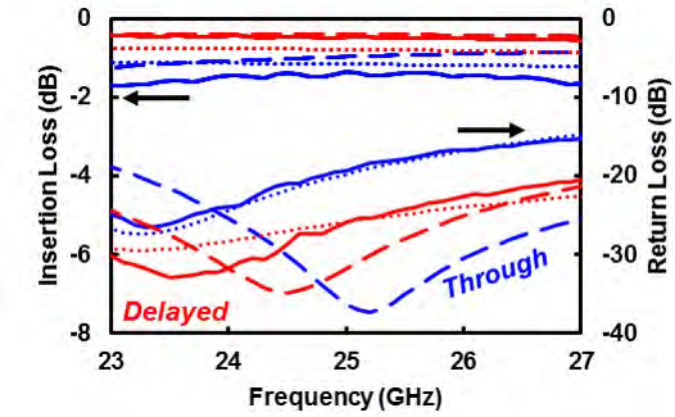


(a)



(b)

Fig. 2. Measured (solid), equivalent-circuit modeled (dotted), and 3D electromagnetics simulated (dashed) (a) insertion phase ($\angle S_{21}$) and (b) insertion loss ($|S_{21}|$) and return loss ($|S_{11}|$) of the 180° unit cell.

This difference in pull-in voltage is tolerable as all switches are overdriven at 40 V.

III. Results and Discussion

Fig. 2 compares measured characteristics of the 180° unit cell with that modeled by using the equivalent circuit of Fig. 3, as well as that simulated by using a three-dimensional finite-element electromagnetic simulator HFSS. It can be seen that across the band of 23−27 GHz, the insertion phase is 165° ± 10°, the insertion loss is less than 1.7 dB, and the return loss is greater than 15 dB. The insertion loss is greater than the simulated value of 1 dB mainly because the loss of the MEMS switch is 0.8 dB instead of 0.4 dB when it is tested individually. Further there is a frequency shift toward lower frequencies in the measured unit cell which is mainly due to greater MEMS capacitances than the designed values.

The equivalent circuit of Fig. 3 is a compact model of the unit cell. It is based on a T-network and models the series and shunt MEMS switches as variable capacitors. All losses associated with the circuit were lumped into series and shunt resistors. Metal-insulator-metal fixed capacitors were modeled

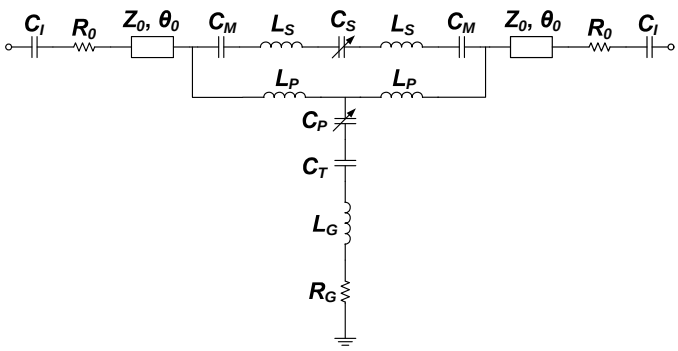


Fig. 3. Extracted equivalent circuit of the 180° unit cell.

TABLE I
180° UNIT-CELL EQUIVALENT-CIRCUIT PARAMETER VALUES

Symbol	Measured		Designed	
	Thru	Delay	Thru	Delay
C_I (fF)	312		275	
R_0 (Ω)	3.3		1.5	
Z_0 (Ω)	43		45	
θ_0 (°)	25@25 GHz		25@25 GHz	
C_M (fF)	240		220	
L_S (pH)	160		160	
C_S (fF)	290	19	260	16
L_P (pH)	200		190	
C_P (fF)	1325	150	1200	130
C_T (fF)	---		---	
L_G (pH)	60		60	
R_G (Ω)	1.4		1	

by C_M and C_I. Input/output interconnects and other distributed circuit element were modeled by ideal transmission line sections with characteristic impedance Z_0 and electrical length θ_0. The microstrip inductors were modeled by L_S, L_P, and L_G. When the series and shunt MEMS switches are actuated, C_S and C_P are large and the series path is more capacitive while the shunt path is more inductive. This resembles a high-pass filter or the left-handed transmission line. As the result, the microwave signal passes straight through the series MEMS switch. On the other hand, when the series and shunt switches are unactuated, C_S and C_P are small and the series path has high impedance, so the microwave signal detours through the shunt MEMS switch with series inductors and shunt capacitors resembling a low-pass filter or right-handed transmission line.

Table I compares the equivalent-circuit model parameters of the 180° unit cell extracted from the measured data with that designed by using HFSS. It can be seen that the measured unit cell exhibits greater loss and capacitance than the design values, which is probably because of greater dielectric constant for the insulators used in the MEMS switches, as well as extra radiation loss from sharp corners and circuit discontinuities.

Additional loss was associated with the greater-than-expected loss tangent of the substrate. The substrate loss tangent was extracted from 1-mm-long and 4-mm-long coplanar waveguides fabricated with the phase shifter on the

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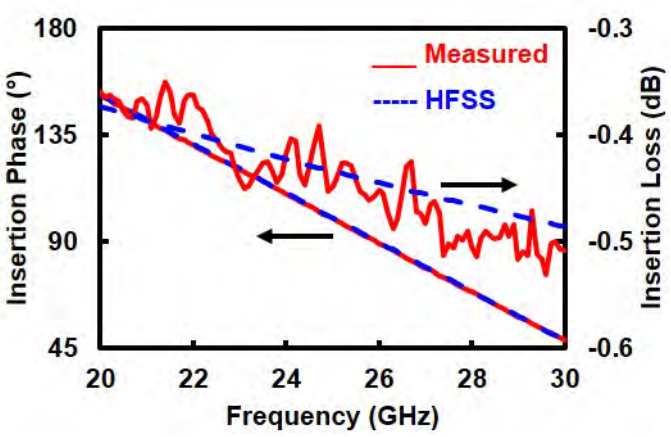

Fig. 4. Measured (solid) and simulated (dashed) insertion phase ($\angle S_{21}$) and insertion loss ($|S_{21}|$) of a 4-mm-long coplanar waveguide line.

same substrate. The lines were simulated using HFSS and the loss tangent of the substrate was adjusted to obtain the best fit to the measured insertion loss and phase as shown in the Fig. 4. The results confirm that the substrate loss tangent is approximately 0.006 which was neglected in the original for HFSS design.

Further studies are required to quantify and reduce different loss mechanisms. Despite the greater-than-expected loss, the present 180° unit cell outperforms similar designs reported in the literature [2]−[5] in terms of insertion loss, number of MEMS switches, size, and phase flatness.

IV. Conclusion

In summary, the proof of principle was presented for achieving 180° phase shift with low dispersion by using only two MEMS switches. This breakthrough in unit-cell design will be the foundation for realizing low-dispersion phase shifter with minimal number of switches and hence, low loss, low cost and high reliability.

Acknowledgment

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Monte Carlo Modeling of Ultra-Fast Operating Ballistic Deflection Transistor

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***Abstract*—This paper presents Monte Carlo simulations of a unique non-linear device called Ballistic Deflection Transistor. A self-consistent model for surface charges has been used and has shown a remarkable efficiency to reproduce the non-linearity. A dynamic analysis is completing the transistor study. Results are showing very good response to an ultra-fast excitation. These are confirming Terahertz performances of our device, leading to the development of more efficient logical computing circuits.**

Keywords—Ballistic Deflection Transistor; Monte Carlo; Terahertz.

I. INTRODUCTION

The increase of general information demand, in terms of quantity and speed, challenges the actual technology and any way to improve drastically the overall efficiency is required. The National Science Foundation has launched this year a new solicitation in order to find and finance emerging technology for future energy-efficient computing. Among the field of semiconductor devices, the Ballistic Deflection Transistor (BDT) [1] could have a significant impact, providing a new way to design existing processor, simpler, faster and with smaller power consumption.

Indeed, the BDT's unique design, obtained by simply etching trenches on InAlAs/InGaAs heterostructure, offers two different output which can be, at the same time, at two different current levels, one high and one low. This can considerably simplify logical design by reducing the number of transistor and thus decreasing the energy required. The active medium is located in a two dimensional electronic gas, allowing an ultra-fast carrier motion. The switching effect is performed by the depletion of one drain channel in favor of the other one, enhanced by two strategically placed gates. The steering of electrons is finally aided by a triangular deflector in the middle of the device. The ballistic carrier movement

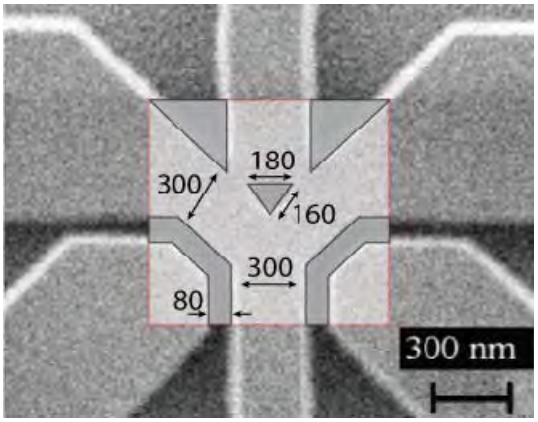

Fig. 1: SEM image of BDT with channel width 300nm and trench of 80nm. The design for MC simulations has been drawn directly over, keeping all dimensions identical.

associated with a non-linear behavior would allow the transistor to theoretically operate at Terahertz (THz) frequency [2].

The objective of this article is to present an appropriate simulation method able to predict the operating frequency of the BDT, taking into account the physical mechanisms involved in the non-linearity.

II. SIMULATED DEVICE

The BDT, presented in Fig. 1, is a six contacts device composed of a grounded source VS, three drains (V_{TD}, V_{LD} and V_{RD}) biased with 1.0 V and two strategically placed lateral gates biased in push-pull configuration (V_{LG}=-V_{RG}). The purpose of the top drain is to pull-up electrons and the associated leak current is very small compared to the other drains, which are the output terminals. The equilibrium is achieved when the two gates are biased at 0.0 V, dividing electron flux equally between the two opposite terminals. When a negative voltage is applied to one gate, the enhanced electric field

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progressively pinches off the corresponding drain channel and increases the electron flow on the opposite side by pushing the electrons towards the positively biased gate. This later current start to decrease when the negative gate voltage is high enough to pinch off the source channel, ultimately reaching 0 A at high V_G. A symmetric response will occur on the opposite drain contact by applying the negative bias to the other gate [3, 4]. An SEM image of the BDT as well as its transfer characteristic are shown on figure 1 and 2, respectively. In this case, the channel width is equal to 300 nm and the trench width to 80 nm. Fabrication indications can be found in [3]. The theoretical study has been performed by means of Monte Carlo (MC) simulations and has already brought interesting information in terms of geometry and material optimizations [5]. Our interest here is the high frequency modeling, which will be seen in the following.

III. Monte Carlo Simulator

The simulator tool [6] is based on MC method, using the Maxwell-Boltzmann statistics, self-consistently coupled with a 2D Poisson Solver. The accuracy is accounted by using a doping of $N_{db}=5\times10^{16}cm^{-3}$ and a time step is 1 fs, which is below the dielectric relaxation time. The size of meshes of 5×5 nm is considered, chosen smaller than the Debye length for the chosen carrier concentration. The device is simulated from the top-side point of view, see Fig. 1. The value of the permittivity is adjusted to reproduced the air (ε=1) while taking into account the absence of semiconductor substrate. The simulator is then able to correctly capture the gate-to-channel coupling of the electric field, providing the best fit with the experimental measurements and the semiconductor [7]. All experiments and simulations have been performed at room temperature.

IV. Surface Charge Model

In order to correctly apprehend the high frequency model, it is important to take a look first at the surface charge model. This charge is located at the interface dielectric/semiconductor and is implying a depletion in the channel. A high carrier concentration situated in an area will induce a high surface charge value, while a low electron density will induce a low . This effect has to be taken into account in order to correctly simulate our device. Using the same surface charge everywhere won't be enough to accurately reproduce the non-linear behavior as we can see on Fig. 2. On this figure is presented the comparison of the experimental right drain current as a function of the left gate voltage and the MC

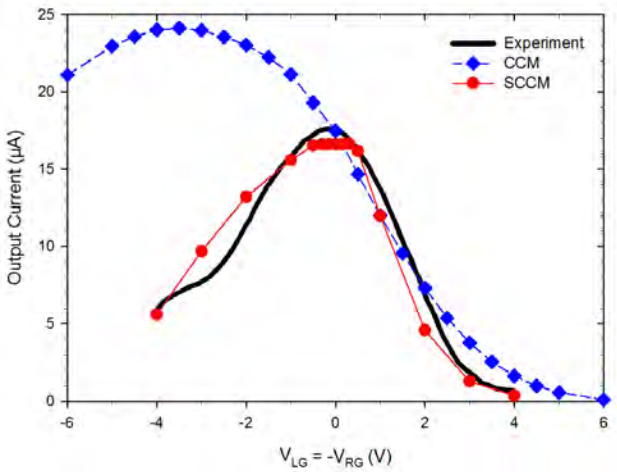

Fig. 2. Experimental and MC transfer characteristics of a BDT (W=300nm) of right output drains I_{RD}, using both model of surface charge, constant (CCM) and self-consistent (SCCM).

results. While the simulated current at equilibrium and for positive left gate bias is similar to the real one, the current at high negative left gate bias is overestimated by a constant charge model (CCM). On the contrary, we can see that simulations performed with a model that gives the opportunity to all surface charges to adapt their value in function of the surrounding electron density (SCCM) shows a very good agreement with the experiment, with a very well reproduction of the bell-shape and the pinch-off. More information can be found in [8]. The only limitation is that surface charges have to be constantly updated in order to stabilize. Thus simulations are demanding a higher amount of computation time to obtain the correct output current for each input gate voltage.

V. Very High Frequency Model

As we have seen, the MC simulator is very accurate in dc mode and is able to correctly reproduce the non-linearity of BDT but the basis of the self-consistent surface charge model and the long computational time required is conflicting with a conventional high frequency analysis. To overcome this problem a special way has to be is used. Two long enough simulations are made on two symmetric polarizations in order to let the σ charge to stabilize and deliver the correct current. Then the two surface charge distributions (σ1 and σ2) are extracted. A square-wave excitation is finally applied between these two points, associating the σ charge distributions for each bias.

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Fig. 3 illustrates this technic on the transfer characteristic of a smaller device, with a width of 100 nm. This result has been obtained by simply reducing the size of meshes of the bigger device. One can see that the maximum current has decreased from 18 µA to 2.7 µA and the pinch-off voltage from -4 V to -0.6 V. The surface charge 2D map of σ1 is shown on Fig. 4, as well as the carrier distribution for the same gate bias. We can observe electrons steered in the right drain, offering a high current, while the left drain is almost completely depleted, with thus a small output current. As the device is symmetric, for σ2 these maps will be mirrored as respect to the Y-axis.

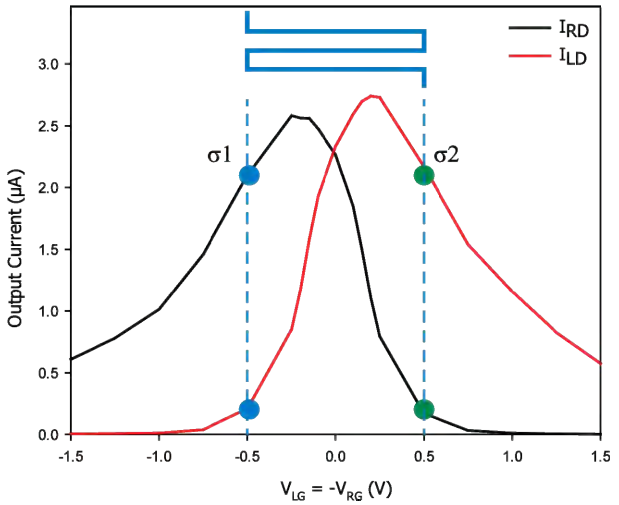

Fig. 3. Transfer characteristic of optimized short width channel W=100 nm. Illustration of square-wave input.

The application of the square-wave frequency on gates implies two different cases. In the first one, or mode 1, the surface charge distribution changes, from σ1 to σ2, instantaneously with the bias, leading to an ideal case where the time constant is very short. The second scenario, or mode 2, is occurring when the switching frequency is so fast that surface charges aren't able to follow and the resulting sigma distribution is becoming an average σ=(σ1+σ2)/2. The time constant is then acknowledged as very long. These two modes are considered limits of real behavior, as very little is known about the velocity of increase or decrease of surface charges value.

VI. Results

Fig. 5 shows the dynamic response of a BDT with W = 100 nm, in a range of gate bias V_{LG} = [-0.5:0.5] V. The two output currents I_{RL} (right) and I_{LD} (left) are

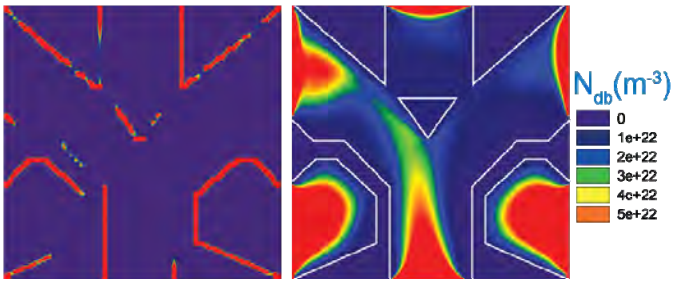

Fig. 4. Surface charge distribution σ1 and its associated carrier density two-dimensional map. As the device is symmetric, for σ2, these maps will be mirrored as respect to the Y-axis.

shown for an input square-wave frequency of 200 GHz, and for the two considered modes of operation. The dashed lines represent the two levels of current, low and high, of drain contacts that are symbolized by dots on Fig. 3. We can see that the mode 1, where surface charges are instantaneously changed with the gate bias, is able to reach both level, as expected. Mode 2 is the case where the input surface charge is an intermediate value of σ1 and σ2. We see that it is also following the mode 1 with a slight difference of current. This can be explained by the value of the surface charges not high enough to sufficiently deplete the according drain channel, thus letting more carrier to pass. As these two modes are extreme cases, we expect the real behavior to be in midway.

On Fig. 6 is represented the right drain output current

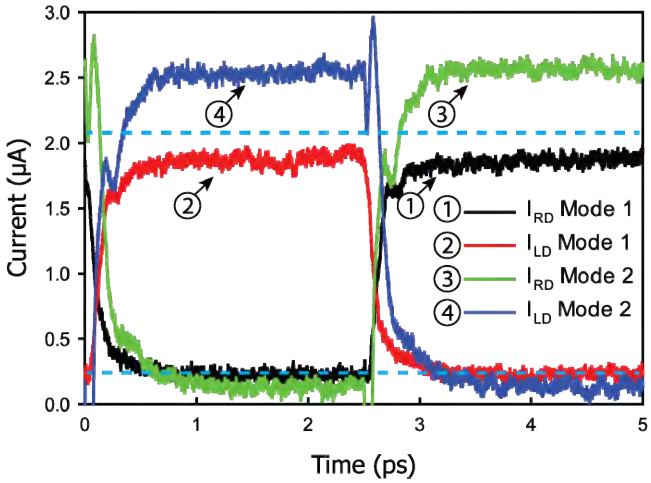

Fig. 5. Current output responses for a 200 GHz input gate frequency with use of mode 1 and 2. The channel width is W=100 nm. Dashed lines represent the two current levels.

for both modes and where the input frequency reaches 1 and 2 THz. While the ideal mode 1 is able to follow the THz excitation, with a slight decrease of the high current,

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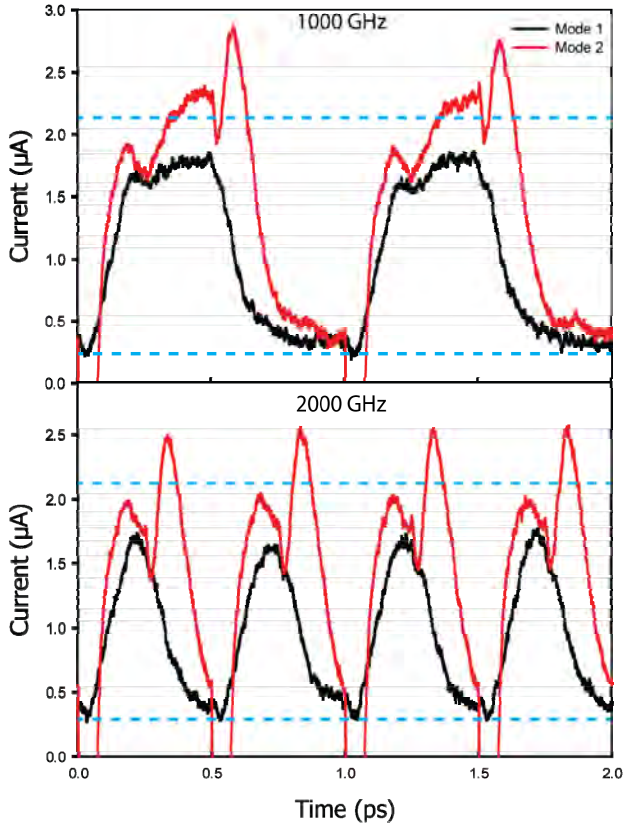

Fig.6. Right drain output current response for an excitation of 1000 and 2000 GHz, and for the two models. The channel width is W=100 nm. Dashed lines represent the two current levels.

we can see that mode 2 begins to have difficulties, at 1 THz, to correctly reach the two current levels, especially the lowest one, and at 2 THz, fails to respond properly.

Modes 1 and 2 are only limit cases and they don't reflect the reality. Little is known about increase and decrease of surface charges and further study would be necessary. In any case, we still obtain pretty good approximation of BDT frequency response in the Terahertz range. These performances can lead the BDT to new kind of ultrafast processing logical design.

VII. Conclusion

Monte Carlo simulations have been performed on Ballistic Deflection Transistors. A self-consistent surface charge model is required in order to correctly reproduce the non-linear behavior. Moreover, an ad-hoc way has been used to combined these surfaces charges dependence with an external bias excitation for studying the dynamic response. Results show great performances in the Terahertz frequency range of operation.

Acknowledgment

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High Frequency N-Polar GaN Planar MIS-HEMTs on Sapphire with High Breakdown and Low Dispersion

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***Abstract*—N-polar planar GaN metal-insulator-semiconductor high-electron-mobility transistors (MIS-HEMTs) grown by metal-organic chemical vapor deposition on sapphire substrate with a high combination of power cutoff frequency (f_{max}) and three-terminal breakdown voltage (BV_{DS}) as well as a decent DC-to-RF dispersion control are demonstrated. Compared to previously reported N-polar planar HEMTs, devices presented in this letter not only maintain comparable f_{max}/BV_{DS} of 221 GHz/116 V, but also exhibit a mitigation of drain current collapse and ON-resistance dispersion. In addition, a higher output power of 5.43 W/mm at the same $V_{DS,Q}$ = 25 V and a reduction of efficiency drop with increasing $V_{DS,Q}$ were achieved by load-pull measurements at 10 GHz.**

I. Introduction

GaN-based high-electron-mobility transistors (HEMTs) have exhibited outstanding performance for RF power amplification [1]. In the Ga-polar orientation, the wide bandgap of GaN and the reliable passivation have enabled output power densities of 32.2 W/mm at C-band [2] and 10.5 W/mm at Ka-band [3]. By taking advantages of ultra-low contact resistance [4], strong electron confinement by the built-in back-barrier [5], improved vertical scalability [5], and reduced field by introducing an AlGaN cap [6], N-polar planar MIS-HEMTs grown by metal-organic chemical vapor deposition (MOCVD) have demonstrated great potential in extending power applications to Ka-band and beyond by achieving high current/power gain cutoff frequencies (f_T/f_{max}) and high breakdown simultaneously [7]. However, the devices reported in [7] show a serious decline in power-added efficiency (*PAE*) with increasing quiescent drain-source voltage ($V_{DS,Q}$), probably due to the strong DC-to-RF dispersion caused by the degradation of the passivation layer under high electrical and thermal stress [7]. In this letter, with improved quality of the SiN_x passivation layer, the devices manifest a mitigation of drain current (I_D) collapse and ON-resistance (R_{ON}) dispersion, leading to a steeper rise of output power (P_{out}) and a reduction of efficiency drop with increasing $V_{DS,Q}$.

II. Device Fabrication

The N-polar GaN HEMTs studied in this work were grown by MOCVD on (0001) sapphire substrate with a mis-orientation angle of 4° toward the sapphire a-plane [8] using growth conditions similar to those reported in [7]. The epitaxial structure and device cross-section are depicted in Fig. 1, and consist of a semi-insulating GaN buffer, a graded AlGaN back-barrier doped with Si, a 0.7 nm AlN interlayer [9], a 12 nm unintentionally doped (UID) GaN channel, and a 2.6 nm $Al_{0.46}Ga_{0.54}N$ cap. After the epitaxial growth, a two-dimensional electron gas (2DEG) density of 1.1×10^{13} cm^{-2} and an average mobility of 1097 $cm^2/(V{\cdot}s)$ were obtained by Hall measurements using Van der Pauw geometry at room temperature.

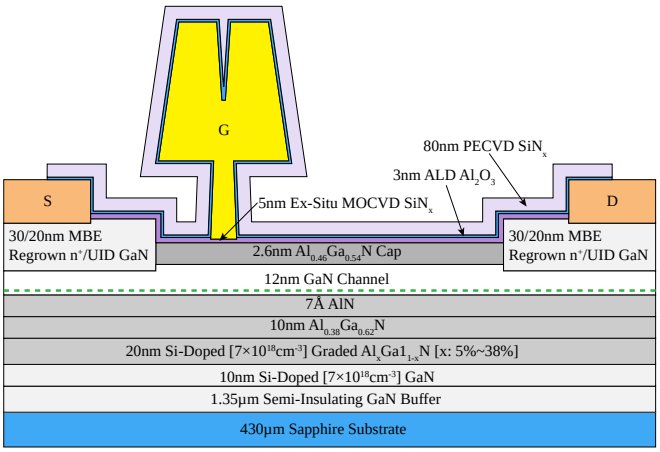

Fig. 1. Cross-sectional schematic of the N-polar planar MIS-HEMTs.

Devices were fabricated starting with a regrown contact process as follows. First, a SiO_2 mask deposited by plasma-enhanced chemical vapor deposition (PECVD) was patterned by an i-line stepper and an inductively coupled plasma (ICP) dry etching. After etching the AlGaN cap layer, 20/30 nm UID/Si-doped (~1×10^{20} cm^{-3}) GaN layers were area-selectively regrown on top of the GaN channel by plasma-assisted molecular beam epitaxy (MBE). Then, the SiO_2 mask was stripped in HF, followed by a MOCVD SiN_x dielectric deposition at 1020 °C. Device isolation was then accomplished by an ion implantation. For the deposition of

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TABLE I
A COMPARISON OF REFRACTIVE INDEX, FILM COMPOSITION, BUFFERED HF ETCH RATE, AND [N]/[Si] RATIOS OF SiN_x FILMS DEPOSITED IN [7] AND IN THIS WORK

SiN_x	n	Composition	Etch Rate (nm/min)	[N]/[Si] by XPS	[N]/[Si] by (1)
In [7]	1.94	$Si_{43.3}N_{49.9}O_{6.9}$	60.6	1.153	1.386
This work	2.06	$Si_{44.4}N_{48.6}O_{7.0}$	25.2	1.095	1.221

ohmic contact metal, the MOCVD SiN_x under the ohmic regions was first etched using a CF_4-based ICP dry etch. Then, the fluorine-based etch damage was removed by a BCl_3/Cl_2 low-power GaN etch in reactive-ion etching (RIE) followed by a wet etch in dilute HCl, after which 20/100 nm of Ti/Au was deposited by an electron-beam physical vapor deposition (EBPVD). Next, T-gates with 220 nm stem height were formed using a two-step electron-beam lithography (EBL) process [10], followed by a 30/500 nm of Ti/Au deposition by EBPVD and liftoff. Series of HEMTs were simultaneously fabricated with respect to nominal dimensions including gate width (W_g), gate length (L_g), gate-source spacing (L_{gs}), gate-drain spacing (L_{gd}), and top-gate length ($L_{g,top}$). Finally, devices were passivated with a 3 nm Al_2O_3 using an atomic layer deposition (ALD) and a subsequent 80 nm of PECVD SiN_x using a deposition condition different from that used in [7]. Similar bilayer surface passivation and/or gate insulator techniques have been investigated in Ga-polar HEMTs [11], [12]. The thin Al_2O_3 also acts as an etch-stop layer for an optional gate-recess process [13] performed on the devices other than those discussed in this letter on the same sample. The quality of the PECVD SiN_x was characterized by refractive index (n) at 632.8 nm from spectroscopic ellipsometry measurements, film composition from X-ray photoelectron spectroscopy (XPS), and etch rate in buffered HF (4-8% HF and 30-36% NH_4F), as shown in Table I. Compared to the SiN_x film in [7] with an etch rate of 60.6 nm/min, a much lower etch rate of 25.2 nm/min was yielded and therefore indicates an improvement of the quality of the passivation layer in this work. The lower etch rate could be explained by two possible mechanisms involved with the lower [N]/[Si] ratio of the film calculated from the XPS analysis or from an empirical expression using the static refractive index [14],

$$\frac{[\mathrm{N}]}{[\mathrm{Si}]} = \frac{4(n_{\text{a-Si:H}} - n_{st})}{3(n_{st} + n_{\text{a-Si:H}} - 2n_{\text{a-Si}_3\text{N}_4})} = \frac{4(3.3 - n_{st})}{3(n_{st} - 0.5)} \quad (1)$$

where n_{st} is the static refractive index (1.898 and 1.992 for SiN_x in [7] and in this work respectively), $n_{\text{a-Si:H}}$ = 3.3, and $n_{\text{a-Si}_3\text{N}_4}$ = 1.9. One is that SiH units at the surface must be oxidized to SiOH before they can be etched making the etching more complicated and slower [15], and the other is that more N–H bonds could accelerate the etching reactions [16].

III. RESULTS AND DISCUSSION

In order to get higher mobility, the devices under study were intentionally oriented such that the conduction in the channel

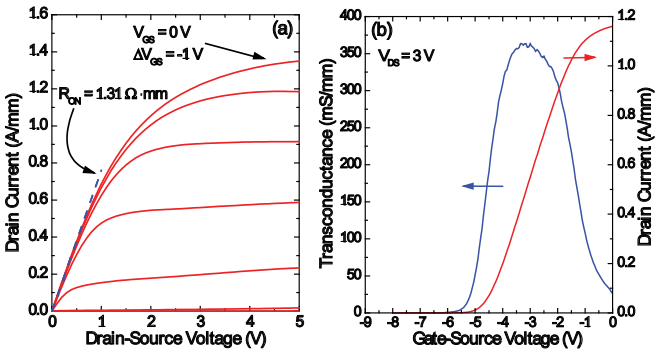

Fig. 2. (a) Output and (b) transfer characteristics of Device A.

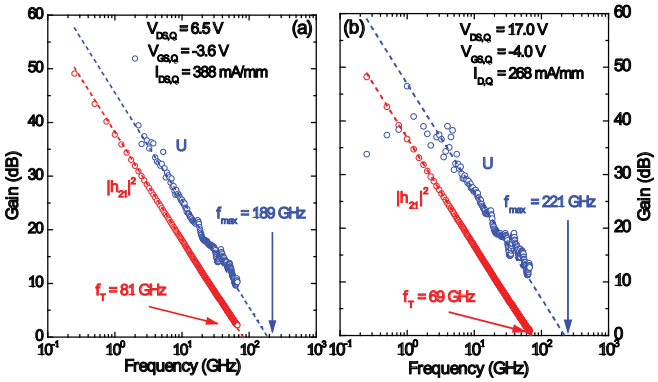

Fig. 3. (a) Peak f_T and (b) peak f_{max} of Device A.

is parallel to the multiatomic steps formed by the growth on vicinal substrate [8]. A combination of capacitance-voltage (C-V) measurements and gated transfer-length measurements (GTLMs) exhibits a 2DEG density of 1.3 × 10^{13} cm^{-2}, a mobility of 1728 $cm^2/(V{\cdot}s)$, and a sheet resistance of 277 Ω/□ at V_G = 0 V. A metal-2DEG contact resistance of 230 Ω·μm was yielded by transfer-length measurements (TLMs).

The DC characteristics of the device with W_g = 2 × 25 μm, L_g = 100 nm, L_{gs} = 300 nm, L_{gd} = 1.60 μm, and $L_{g,top}$ = 450 nm (Device A) are shown in Fig. 2, including a maximum I_D of 1.35 A/mm at V_{GS} = 0 V and V_{DS} = 5 V, an R_{ON} of 1.31 Ω·mm, a peak extrinsic transconductance (g_m) of 363 mS/mm at V_{DS} = 3 V. The device also shows a threshold voltage (V_T, defined by the linear extrapolation of I_D-V_{GS} from peak g_m) of −4.4 V at V_{DS} = 1 V, a pinch-off voltage (V_p) of −6.9 V, an excellent minimum subthreshold swing (SS) of 78 mV/dec, and a low drain-induced barrier lowering ($DIBL$) of 33 mV/V.

The extrinsic-level small-signal characteristics of Device A, as demonstrated in Fig. 3, were obtained by de-embedding pad parasitics using an open-short (OS) method. By extrapolating the small-signal current and power gain at −20 dB/dec, while a peak f_T of 81 GHz was yielded at $V_{DS,Q}$ = 6.5 V and quiescent drain-current $I_{D,Q}$ = 388 mA/mm, a peak f_{max} of 221 GHz was obtained at $V_{DS,Q}$ = 17.0 V and $I_{D,Q}$ = 268 mA/mm.

An OFF-state three-terminal breakdown measurement using a drain-current injection technique [17] was performed on Device A at a constant I_D of 1 mA/mm, as shown in Fig. 4(a).

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To prevent catastrophic damage to the device, a 10 kΩ series resistor was connected to the drain during the measurement. By taking the voltage drop on the resistor into account, a drain-source breakdown voltage (BV_{DS}) of 116 V was obtained. Without using the resistor, a higher BV_{DS} of 157 V was yielded by a device with similar dimensions (Device B, W_g = 2 × 75 µm, L_g = 90 nm, L_{gs} = 300 nm, L_{gd} = 1.61 µm, and $L_{g,top}$ = 450 nm), as shown in Fig. 4(b).

The high composition of f_{max}/BV_{DS} of 221 GHz/116 V of Device A compares well with that of devices reported in [7], thereby exhibiting great promise for power amplification at Ka-band and beyond. Since f_T/f_{max} are limited by the parasitic resistances in this work, further improvement in small-signal performance is expected by scaling down the source-drain spacing and optimizing the regrown contact resistance.

Double-pulsed-*IV* measurements with pulse width/period of 200/700 ns were performed on the device with W_g = 2 × 25 µm, L_g = 80 nm, L_{gs} = 300 nm, L_{gd} = 1.37 µm, and $L_{g,top}$ = 400 nm (Device C), taking quiescent gate-source voltage ($V_{GS,Q}$) of −6 V as a high-field OFF-state condition and I_D-V_{DS} characteristics acquired at [$V_{GS,Q}$, $V_{DS,Q}$] = [0 V, 0 V] as a reference unaffected by DC-to-RF dispersion. As seen in Fig. 5(a), while typical I_D collapse and R_{ON} increase occur near ON-state, I_D higher than the reference current was observed at semi-ON states and thereby indicates the existence of an "anti-dispersion" mechanism which needs to be investigated further to draw conclusions about the physical origin. With different quiescent bias points, I_D at V_{GS} = 0 V and at the knee-voltage as well as the ratio of the drain-current reduction ΔI_D to the reference drain-current I_{D0} ($\Delta I_D = I_{D0} - I_D$) are used to evaluate the absolute and relative I_D collapse respectively. Similarly, R_{ON} at V_{GS} = 0 V and the ratio of the ON-resistance increase ΔR_{ON} to the reference ON-resistance R_{ON0} ($\Delta R_{ON} = R_{ON} - R_{ON0}$) quantify the absolute and relative R_{ON} dispersion respectively. Such quantities of both of Device C (with a knee-voltage of 4 V) and the device fabricated in [7] (W_g = 2 × 75 µm, L_g = 100 nm, L_{gs} = 200 nm, L_{gd} = 1.00 µm, $L_{g,top}$ = 400 nm, and with a knee-voltage of 3 V) are plotted in Fig. 5(b, c). Compared to the device in [7], the mitigations of I_D collapse and R_{ON} increase of Device C demonstrate the improvement in DC-to-RF dispersion control as a possible consequence of the better quality of SiN_x passivation layer.

Large-signal performance under deep class-AB operation at 10 GHz with $I_{D,Q}$ = ~100 mA/mm was obtained by the measurements using a passive tuner-based load-pull system on the device with W_g = 2 × 75 µm, L_g = 90 nm, L_{gs} = 300 nm, L_{gd} = 1.61 µm, and $L_{g,top}$ = 450 nm (Device D), as shown in Fig. 6. Larger W_g of Device D compared to that of Device A or Device C is necessary to provide a higher current for a load power match under high voltage operation. The load match condition was selected to balance between the highest P_{out} and the highest *PAE*. A peak P_{out} of 4.55 W/mm and an associated *PAE* of 56.5% were yielded by a power-sweep at $V_{DS,Q}$ = 20 V, as shown in Fig. 6(a). To make a comparison, the power sweep of the device report in [7] at the same $V_{DS,Q}$ is included in Fig. 6(a) as well, and the less dispersive device in this work

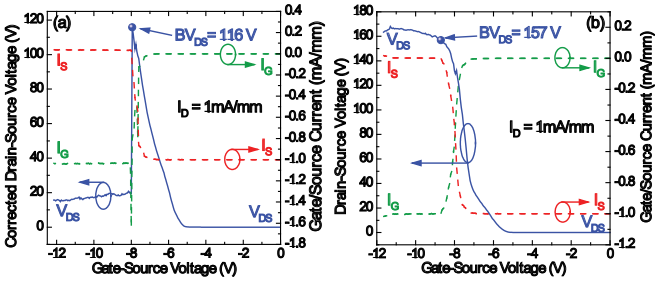

Fig. 4. OFF-state three-terminal breakdown measurements using a drain-current injection technique on (a) Device A with a drain-side 10 kΩ series resistor (corrected V_{DS} = measured V_{DS} − voltage drop on the resistor) and (b) Device B without a drain-side series resistor.

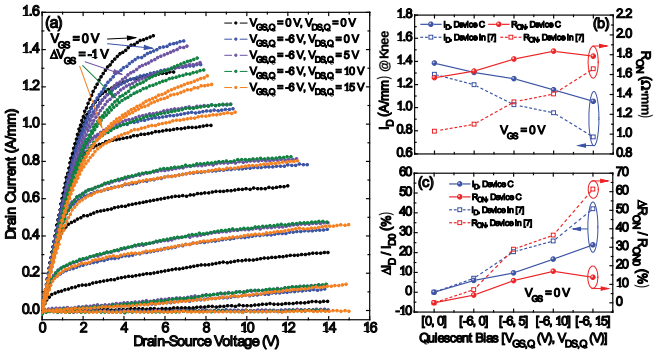

Fig. 5. (a) Double-pulsed-*IV* measurements of Device C; (b) absolute and (c) relative I_D collapse and R_{ON} dispersion comparison between Device C and the device fabricated in [7].

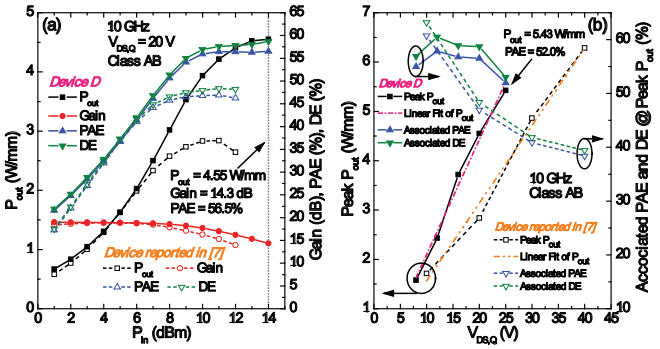

Fig. 6. Large-signal performance at 10 GHz of both Device D and the device reported in [7]: (a) power-sweeps at $V_{DS,Q}$ = 20 V and (b) dependence of peak P_{out} as well as associated *PAE* and *DE* on $V_{DS,Q}$.

clearly presents improvements in peak power, peak efficiencies and gain compression. With $V_{DS,Q}$ = 25 V, a higher peak P_{out} of 5.43 W/mm was obtained at an input power (P_{in}) of 12 dBm by a load-pull process, as shown in Fig. 6(b). During such load-pull process, a sharp increase of gate leakages was found for some reflection coefficient points at load-port (Γ_L), and therefore indicating a degradation of the gate dielectric and resulting in unimproved P_{out} with increasing $V_{DS,Q}$ beyond 25 V. Fig. 6(b) demonstrates the dependence of peak P_{out} as well as associated *PAE* and *DE* on $V_{DS,Q}$ at 10 GHz of both of Device D and the device reported in [7]. Two observations

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can be made on this figure to demonstrate an improved DC-to-RF dispersion control in large-signal operation. First, while P_{out} scales well with $V_{DS,Q}$ for both of the devices, Device D exhibits a steeper slope of 0.233 W/(mm·V) in comparison to 0.157 W/(mm·V) of the device reported in [7]. Second, although Device D has lower efficiencies at low $V_{DS,Q}$ regime owing to the higher R_{ON}, it drops much slower with increasing $V_{DS,Q}$ (note that the drop of *PAE* and *DE* at $V_{DS,Q}$ = 25 V of Device D is partly due to the low P_{in} and mis-matched Γ_L in the associated load-pull process). The earlier gate dielectric degradation of the Device D could be also attributed to the improved dispersion control, since less negatively charged states, which cause the dispersion, exist to mitigate the high filed at the depletion region.

IV. Conclusion

While maintaining a high combination of f_{max} and OFF-state three-terminal breakdown voltage, devices on sapphire in this letter exhibit improved DC-to-RF dispersion control by using a higher quality SiN_x passivation layer in comparison to the previous reported devices with similar design, thereby making N-polar GaN planar MIS-HEMTs more promising for power applications at Ka-band and beyond. Further improvements are expected by scaling down the source-drain spacing, optimizing the contact resistance, and replacing the substrate of sapphire by SiC [7].

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A High Responsivity SnO_2 Hollow Nanospheres Based Ultraviolet Photodetector

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***Abstract*— Hollow spherical nano structures have shown great potential in the field of optoelectronics. As a wide band gap material, SnO_2 has electrical and optical properties well suited for its use in fabrication of ultraviolet photodetectors. This paper presents the synthesis and characterization of SnO_2 hollow nanospheres. The spheres are used as active material to fabricate a UV photodetector. The electrical characteristics of the device have also been presented. The fabricated detector exhibits a peak UV responsivity of 2680 A/W and high external quantum efficiency of 9.8 x 10^5%. This paper shows SnO_2 hollow nanospheres as a promising material for fabricating high sensitivity ultraviolet photodetectors.**

Keywords—tin oxide, hollow nanospheres, UV photodetector, high responsivity

I. Introduction

Metal oxide nanostructures have been used in numerous fields for photodetection, chemical and gas sensing, opto-electronic and magnetic devices [1-4]. Specifically ZnO, Ga_2O_3, WO_3 and NiO have been exhaustively used as nanoparticles, nanowires, nanocubes, nanodiscs, nanorods, nanoflowers and even quantum dots to form the active material in UV photosensors. SnO_2 is a direct wide band gap (E_g=3.5 eV – 4.6 eV) n-type semiconductor metal oxide, which has gained increasing importance for the applications stated above. This is because SnO_2 is chemically stable, nontoxic, has a high electron mobility and large exciton binding energy of 130 meV [5].

Hollow inorganic nanospheres have been extensively studied for their applications as carriers for drug delivery, nanoreactors, anode material for lithium ion batteries and photocatalysts for more than a decade [14-16]. Recently a lot of interest is generated in the use of hollow metal oxide nanostructures as building blocks of photodetectors due to their ability to efficiently harvest light, high surface to volume ratio, and unique electron transport properties. These structures are also compatible with fabrication techniques for photodetectors on flexible substrates [7]. Many synthesis methods for hollow nanospheres have been proposed which include the use of polymeric templates or sacrificial templates [6]. These methods are complicated and require a long time for completion as the process includes steps of synthesizing templates, coating then with the inorganic material and finally dissolving or burning off the template. The coated material then maintains the shape of the template producing a hollow structure. Therefore, a template free one-pot method is an attractive alternative to synthesize such structures.

In this paper, we present a SnO_2 hollow nanospheres based ultraviolet photodetector on a quartz substrate. Details of material synthesis along with material and device characterization are reported. The fabricated device shows high responsivity to ultraviolet light, excellent external quantum efficiency, high photocurrent, and a good signal to noise ratio.

II. Experiments

A. Fabrication

SnO_2 hollow nanospheres are synthesized using an environmentally friendly one pot hydrothermal method [7-8]. In a typical process, 27.3 ml of ethanol and 2.7 ml of DI water are added to 0.5 ml concentrated hydrochloric acid (36.5 – 38%). $SnCl_2.2H_2O$ is dissolved in the solvent till a clear solution is obtained to get a molar concentration of 30 mM. This solution is sonicated for 30 minutes and transferred to a 45 ml Teflon lined stainless steel autoclave and heated at 200°C for 24 hours. The autoclave is then cooled naturally to room temperature. The products are centrifuged and washed 6 times with DI water and ethanol and dried in vacuum overnight.

To fabricate the photodetector, a 30 mg/ ml dispersion of the hollow spheres is prepared in ethanol by sonication for 15 minutes. A thin layer of the hollow spheres is coated on quartz substrate using dynamic spin coating method. The device is then transferred to an e-beam system where Cr/Au interdigitated electrodes (20/200 nm) are evaporated on the thin film using a shadow mask. Finally, the detector is wire bonded using Epo-Tek H20E conductive epoxy. A 3D device schematic is shown in Fig. 1.

B. Experimental Setup

A Carl Zeiss Ultra 1540 dual beam scanning electron microscope (SEM) is used to study the diameter and morphology of the hollow spheres. The X-ray diffraction (XRD, Bruker D8-Discover) patterns are recorded using Cu Kα radiation. A Shimadzu UV-Vis 2550 spectrophotometer with a

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deuterium lamp (wavelength: 190-390 nm) and a halogen lamp (wavelength: 280-1100 nm) is used to measure the absorption spectrum. The photoluminescence (PL) spectrum is obtained with a Spex Fluorolog Tau-3 spectrofluorometer with a Xenon lamp. The excitation source is fixed to the wavelength of 330 nm. The time response and I-V characteristics of the fabricated photodetector are measured using an HP 4155B semiconductor parameter analyzer and 335 nm UV LED. A Shimadzu UV-Vis 2550 spectrophotometer, Newport 1928-C optical power meter and Keithely 6487 picoammeter are used to record the responsivity of the photodetector. All measurements were performed at room temperature in air.

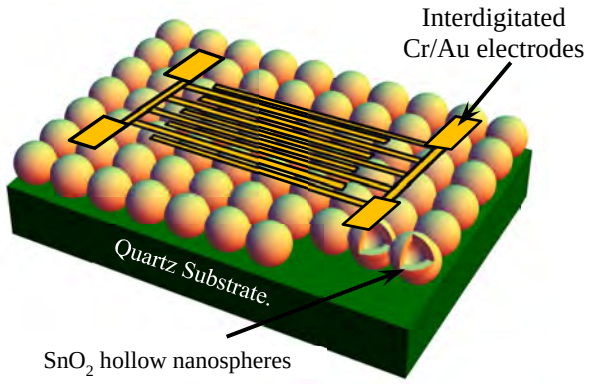

Fig. 1. Schematic of fabricated SnO_2 hollow nanospheres based photodetector.

III. Results and Discussion

High resolution SEM images (scale 200 nm) of the hollow nanospheres on quartz substrate are shown in Fig. 2. It can be seen from the SEM images that the spheres are hollow, uniform in size, and have an average diameter of approximately 150 nm.

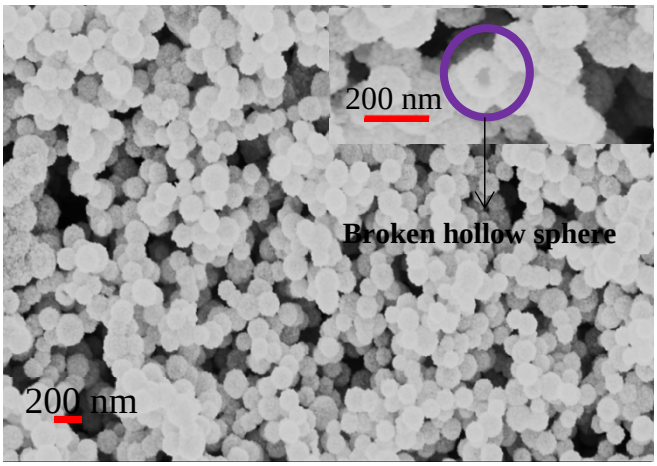

Fig. 2. SEM image of the SnO_2 hollow nanospheres. The image in the inset shows a broken sphere (circled) which shows the hollow morphology of the synthesized spheres.

The formation of hollow spheres is achieved by Ostwald ripening mechanism which states that the hollowing of the spheres is driven by reduction of total surface energy [8-10]. The hydrolysis of the tin salt in the ethanol-water solvent results in the formation of nanoparticles which when subjected to hydrothermal treatment form solid spheres. Prolonged hydrothermal treatment results in the hollowing out or ripening of the solid spheres to form the hollow nanospheres. This process is shown in Fig.3.

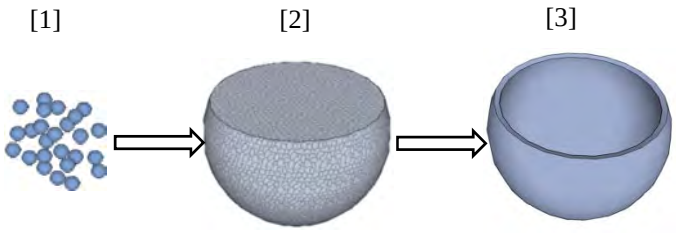

Fig. 3. Schematic diagram showing the formation of hollow spheres by Ostwald ripening mechanism. The hydrolysis of tin salt forms tin oxide nanoparticles [1]. Hydrothermal treatment of these nanoparticles forms a solid sphere [2]. Increasing the time of hydrothermal treatment results in a hollow sphere due to Ostwald ripening [3].

The particles at the core of the spheres have higher surface energy and therefore dissolve more readily. Then through ionic mass transport they move out of the sphere via interstitials in the crystallites forming the surface of the spheres and recrystallize on the surface crystallites [11]. Infact, on close inspection of the SEM images, we can see that the nanospheres are composed of SnO_2 nanoparticles which are approximately 20 nm in size.

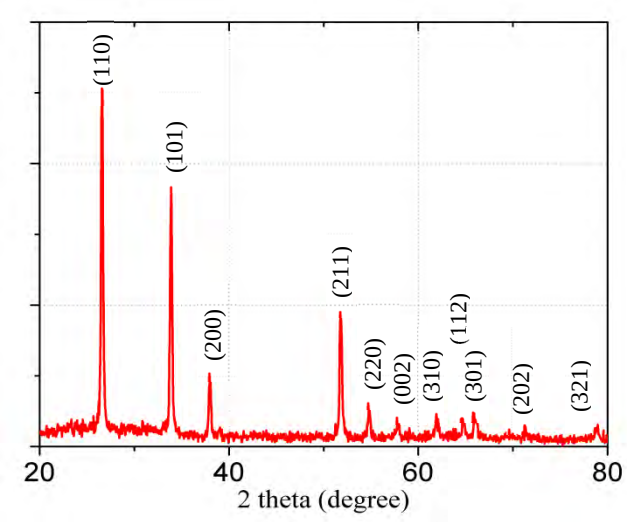

Fig. 4. XRD pattern of SnO_2 hollow nanospheres.

The XRD pattern of the SnO_2 nanospheres is shown in Fig. 4. The spheres are crystalline tetragonal rutile phase tin oxide and all peaks of the spectrum are well matched to the reference JCPDS card no. 41-1445. The absorption and PL spectra are recorded to study the optical characteristics of the hollow spheres. Fig. 5 a) shows the absorption spectrum of the SnO_2 hollow nanospheres. The absorption cut off edge is

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approximately at 310 nm beyond which absorption drops off

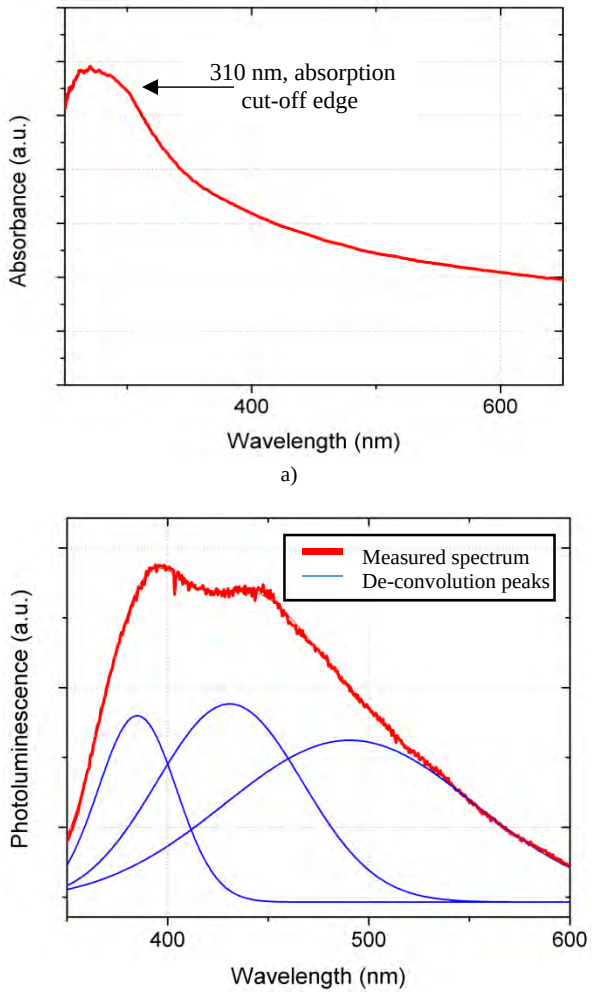

Fig. 5. Optical characterization of SnO_2 hollow spheres, a) absorption spectrum and b) photoluminescence spectrum pattern.

abruptly. The absorption in the UV region is more than three times the absorption in the visible region which makes this material ideal for fabrication of visible blind detectors with good signal to noise ratio.

The PL spectrum of the material is shown in Fig. 5 b). The spectrum shows peaks at 395 nm and 442 nm and a tail that extends well into the visible region. This predicts that the spectrum is composed of multiple peaks and hence a de-convolution of the spectrum is performed. This shows peaks at approximately 385 nm, 431 nm and 491 nm. The peak in the UV range at 385 nm can be assigned to near band edge UV emission. Defects in the material like dangling bonds and tin interstitials add defect energy levels in the band gap of the material. These energy states act as auxiliary transition paths for charge carriers and produce the PL peak at 431 nm. The peak at 491 nm is a broad peak which can be attributed to the parasitic green photoluminescence generated by oxygen vacancies in tin oxides. These deficiencies have been reported in most metal oxides and are generated by an electron trap

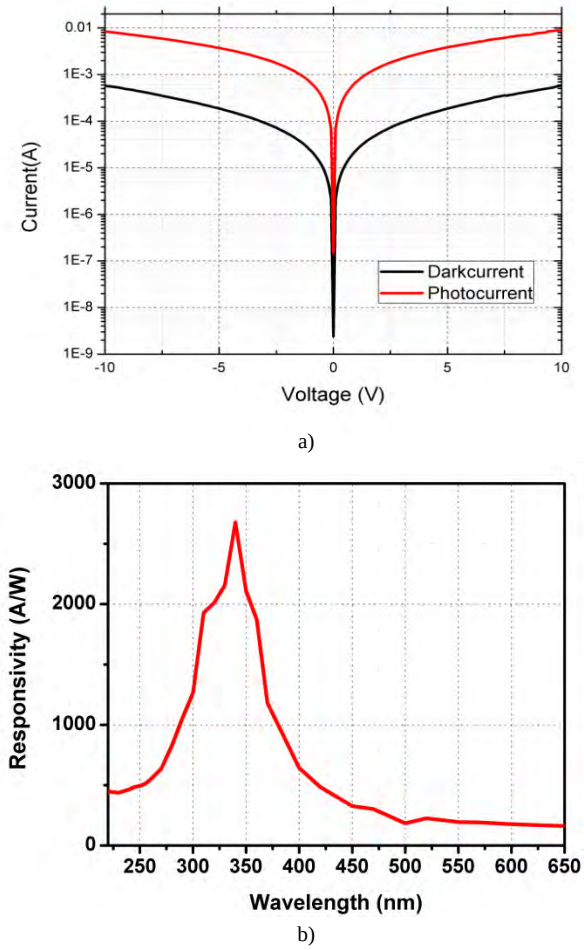

Fig. 6. Electrical characterization of SnO_2 hollow nanospheres photodetector, a) I-V characteristics and b) photo responsivity.

formed when an oxygen atom breaks free from the lattice [17-18].

To investigate the electrical characteristics of the device, responsivity, transient response and the current-voltage (I-V) response of the device have been recorded. Fig. 6 a) shows the photocurrent and dark current of the device measured for a voltage sweep from -10 V to 10 V. It is seen that the photodetector is sensitive to UV light and detector current increases approximately 20 times on exposure to UV light.

The photo responsivity of the detector is shown in Fig. 6 b). The photodetector is sensitive to UV light and gives a peak responsivity of 2680 A/W at a wavelength of 340 nm. This wavelength corresponds to a bandgap of approximately 3.65 eV which in the expected value for nano-scale tin oxide material. The high responsivity can be attributed to the large surface-to-volume ratio of the nanospheres which results in many surface states that act as traps for electrons. The oxygen in the atmosphere adsorbs on the surface of the spheres and captures these trapped electrons forming a depletion region at the surface. When light is incident on the device, photogenerated holes move to the surface and recombine with the electrons, desorbing the oxygen molecules. However, the

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photogenerated electrons will continue to contribute to the photocurrent until they can recombine with a hole. As the hole is regenerated only when oxygen adsorbs on the surface again, the lifetime of the hole is prolonged. This charge separation produces the large photoconductive gain of the detector [5, 19]. The responsivity of the device can be used to calculate the external quantum efficiency (EQE). EQE is an important parameter that is defined as the ratio of charge carriers generated by the incident light to the number of incident photons. It is dependent on the responsivity of the detector at any given wavelength by the following relation in (1).

$$EQE = \frac{R_\lambda hc}{\lambda e} \quad (1)$$

where, R_λ is the responsivity of the detector at wavelength λ, h is Planck's constant, c is speed of light and e is electronic charge. The photodetector presents excellent peak EQE of 9.8x 10^5 % at 340 nm.

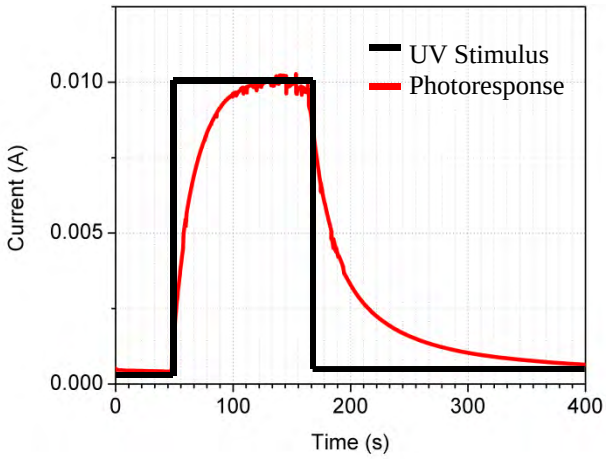

Fig. 7. Time response of photodetector when UV stimulus is applied intermittently. The rise time and fall time of the detector is calculated as 38 seconds and 137 seconds respectively.

Fig. 7 shows the transient response of the photodetector. A 335 nm UV LED was turned on and off manually for UV stimulation to obtain the time response. The photo carriers are generated as explained above and charge transport occurs by the electrons tunneling from one sphere to the next [12-13].

IV. Conclusion

This paper reports a high performance SnO_2 hollow nanospheres based ultraviolet photodetector which can find use in high sensitivity photo detection applications. Specifically, this device is created for improved bio-hazard detection in the context of a hospital room. Future work will explore coating the hollow spheres with graphene to improve the transient response of the device.

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MoS_2 Synthesis and High-Performance Broadband Photodetector

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***Abstract*—In this work, we report on the vapor-based synthesis of molybdenum disulphide (MoS_2), which is one of the most widely studied two-dimensional (2D) layered materials since the large body of work conducted on the quintessential layered material, graphene. In addition, we have fabricated and characterized a MoS_2 photodetector which was formed using a visco-elastic stamping technique. This device exhibits a low Schottky barrier height of ~27 meV and a photoresponsivity of 1,314 A/W at room temperature using a broad band light source with irradiance power of 0.134 nW at 5 V drain-source voltage. Our results show the promise of MoS_2 for photodetectors and a range of other applications.**

Keywords—MoS₂; CVD synthesis; broadband photodetector; high photoresponsivity

I. Introduction

Molybdenum disulphide (MoS_2) has been one of the most widely explored layered materials over the past several years. High-performance transistor devices have been constructed from monolayers of MoS_2 that serve as the channel region. The MoS_2 layered material is composed by stacks of 6.5Å thick molecular membrane comprised of molybdenum atoms that are sandwiched between two layers of sulfur atoms to yield a hexagonal motif. The 2H-MoS_2 is the most stable polytype and it is found in nature [1]. It contains layers centrosymmetric to each other creating a hexagonal structure (Fig. 1). This diamagnetic semiconductor material has been utilized as a gas sensor, FET transistors, photovoltaics, photodetector, and flexible electronics due to its sensitivity toward environmental markers, and its exceptional mechanical and optoelectronic properties [2], [3]. An important characteristic of MoS_2 is that its energy bandgap E_g varies as a function of the number of layers, showing indirect band gap characteristics with $E_g \sim 1.2$ eV in the bulk (valence band maximum at the Γ point) to direct band gap transition with $E_g \sim 1.8$ eV for monolayers (valence band maximum at K point) [4]. The bandgap can also be tuned by applying an external electric field. In addition, several mechanisms contribute to the generation of the photocurrent in MoS_2: the photovoltaic effect, the photoconductivity, and the photothermoelectric effect, even under sub-band gap illumination, attributed to the mismatch in the Seebeck coefficients between the contacts and the semiconductor [5], [6]. Moreover, it has been demonstrated the presence of persistent photoconductivity in MoS_2 [7]. These intriguing characteristics make this material an exceptional candidate for optoelectronic applications [8].

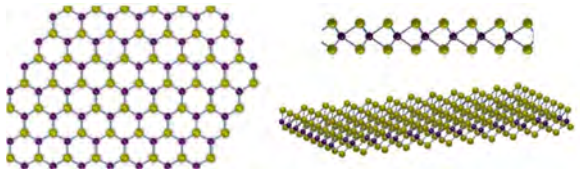

Fig. 1. MoS_2 monolayer in top, side and 3D view; yellow spheres represent the Mo atoms and purple spheres represent S atoms.

In this work, we report on the vapor based synthesis of MoS_2, and the fabrication and optoelectronic characterization of a mechanically exfoliated MoS_2 photodetector using a visco-elastic stamping process [9]. The device characterization experiments involved the characterization of the electronic transport properties of MoS_2 as a function of temperature over a wide range from 6 K to 346 K. The optoelectronic properties were also measured as a function of the irradiance for a broadband white-light source at room temperature under vacuum.

II. Vapor Phase Synthesis of MoS_2

The synthesis of layered materials, including the MoS_2, is a research area of interest which allows the realization of high quality materials. The different approaches to synthesize these materials are through micromechanical cleavage, liquid exfoliation, and vapor phase synthesis, also known as chemical vapor deposition (CVD). The first method is useful for conducting research to understand inherent material properties and unveil new physics, for example, at interfaces in heterostructures. The second approach is scalable, but it may lead to some contaminants from residual solvents that may still be present in the deposited films. Finally, the third approach, CVD synthesis, has the potential to yield high crystalline quality layered materials which can be beneficial for advancing state-of-the-art semiconductor device research for the electronics industry. .

Here, we report on the synthesis of MoS_2 using CVD, based with an in-house designed single zone system that can

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be adapted for operation as a two-zone furnace. The process consists in a modification of process in reference [10]. For material specifics, 400 mg and 800 mg of MoO_3 and S, respectively were used as the precursors. Our substrate material was a 270 nm SiO_2/Si wafer that was cleaned using piranha to remove any residual surface contaminants. The MoO_3 was positioned in the center of the furnace, and the substrate was placed on top of it with the polished side facing down while the S was placed 17 cm upstream. Fig. 2 illustrates the set-up of the materials and location within the furnace. After a purge cycle, the reaction chamber was stabilized at 760 Torr with a constant UHP N_2 flow of 200 sccm, which served as the carrier gas.

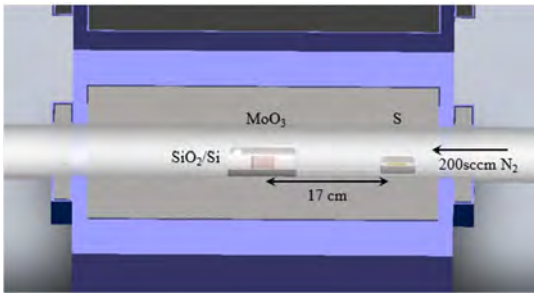

Fig. 2. Position of substrate and both precursors MoO3 and S in 4" quartz tube on furnace.

Once the initial conditions are set, the thermal cycle of the furnace was initiated using a profile shown in Fig. 3. Since the pressure increases when the sulfur is evaporated, the pressure is maintained at a stable value during the process by manipulating the outlet valve. The temperature profile for each precursor and pressure during the process are shown in Fig. 3. The reaction mechanism seems to be as follows: at the beginning both precursors are evaporated and the MoO_3 is reduced to MoO_2 with S at temperatures between 650 and 850 ºC [10]. Subsequently, MoO_2 and S react to form MoS_2, and growth on the surface of the substrate, generating some oxisulfides subproducts extracted by fume exhaust.

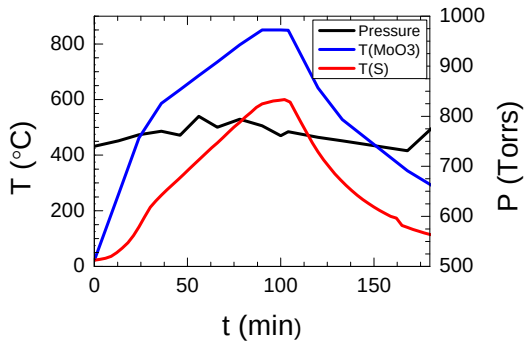

Fig. 3. Temperature profile of precursors and pressure in reaction chamber during the synthesis process.

The synthesized flakes are shown in Fig. 4 exhibiting triangular shapes. Its monolayer character was confirmed using Raman spectroscopy, where the two strong vibration modes peaks, the E^1_{2g} and A_{1g}, peaks are at 388.4 cm^{-1} and 488.4 cm^{-1}, respectively, with a difference between the two peaks Δk of 20 cm^{-1} indicative of single layer MoS_2 from prior work [11].

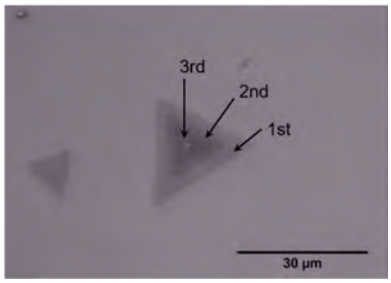

Fig. 4. Optical image of CVD MoS_2 domains. The flake on the left is monolayer while the flake in the center has one, two and three layers. The nucleation site is the white dot at the center of the triangle

The films synthesized in this process were not utilized for the fabrication of our device due to the limitations in fabrication facilities during the development of this work. Instead, mechanically exfoliated MoS_2 was used for the fabrication of our device where the cleanliness and crystal quality are optimum. For future work, the synthesized MoS_2 photodetector will be compared with the one reported here.

III. Photodetector Fabrication

The fabrication process of the device involves using a standard photolithography process for metal contact pattering on the 270 nm SiO_2/Si for high optical contrast between the substrate and the flake [12]. Next, 100 nm of Mo was deposited using sputtering, followed by a metal lift-off process. Afterwards, the alignment of the MoS_2 flake onto the substrate with electrodes was done using a dry viscoelastic stamping process (set-up in Fig. 5) [13], allowing a simple and clean process for transferring 2D flakes onto arbitrary substrates (Fig. 6). This adaptation of the viscoelastic stamping process in our lab was conducted using a Karl Suss MJB3 mask aligner, which makes the flake transfer more efficient compared to manual alignment that is time consuming, tedious and often results in a low-yield for contacting individual micron-sized flakes.

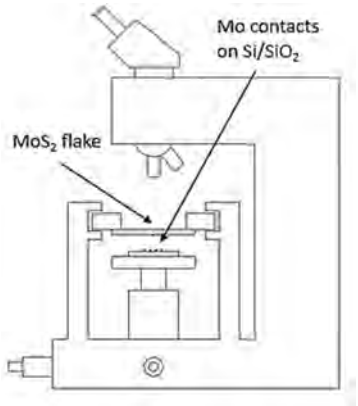

Fig. 5. Set-up for alignment and transfer of MoS_2 flake by viscoelastic stamping using PDMS gel film and mask aligner Karl Suss MJB3.

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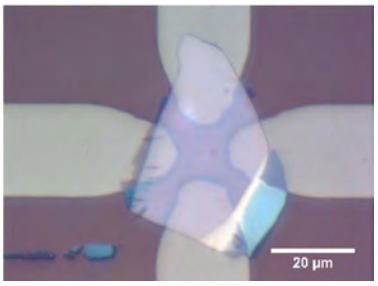

Fig. 6. Optical image of the device. The micromechanically exfoliated MoS_2 flake is stamped on SiO_2/Si substrate with Mo contacts.

IV. OPTO-ELECTRONIC CHARACTERIZATION

The electronic and opto-electronic device characterization was conducted using a Lakeshore CRX-4K probe stage with temperature control from 6 K to 346 K, and a low noise semiconductor parameter analyzer, the Keysight B1500A. The electrical transport measurements were conducted using two horizontal Mo terminals, as shown in Fig. 6. The area of the flake obtained is 1,237.48 µm^2, and the photodetector channel length and width are ~17 and 12 µm, respectively. In Fig. 7, the (IV) characteristic of the device from V_{DS} = -10 to 10 V is shown.

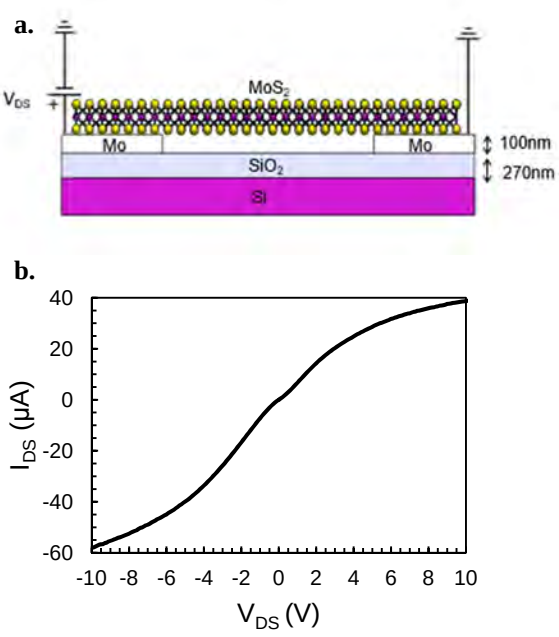

Fig. 7. a. Schematic of device showing MoS_2 monolayer, b. IV characteristic curve of MoS_2 photodetector under vacuum at room temperature with V_{DS} from -10 to 10 V

Two-terminal electrical transport measurements were done as a function of temperature. In order to reduce hysteresis due to absorption of gases and moisture, the device was left under vacuum (~10^{-6} Torr) for two weeks [14]. In addition, a cycle of electrical annealing was run to reduce the contact resistance. After these two procedures, the IV characteristics were acquired every 34 K starting at 6 K, which is the base temperature of the system using compressed helium in a closed cycle refrigerator; the data was gathered up to a maximum of 346 K (Fig. 8) in this case. As the temperature is increased the IV curve approximates to ohmic contact behavior.

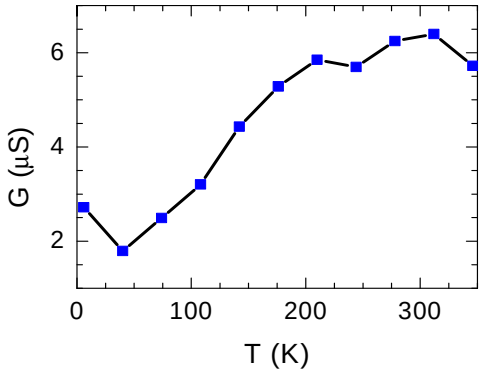

Fig. 8. Conductivity obtained from two-terminal IV characteristic curves of device in function of temperature at V_{DS} = 1V

Subsequently, the device under test was exposed to varying light intensities using a broadband source under vacuum conditions at 300 K to study the photocurrent behavior and the photoresponsivity, which are key figures of merit for gauging photodetector response. The photocurrent I_{ph} is defined as the difference between the current under exposure I_{light} of light and the dark current I_{dark}

$$I_{ph} = I_{light} - I_{dark} \quad (1)$$

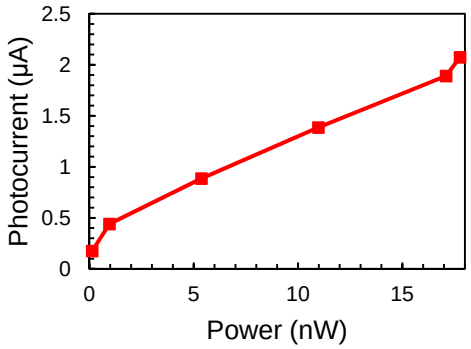

Fig. 9. Photocurrent of device at V_{DS} = 5 V at different broadband source irradiance intensities.

Moreover, the photoresponsivity is defined as the input-output gain is calculated by Equation 2 in units of current per incident light power.

$$R = \frac{I_{ph}}{P_{light}} \quad (2)$$

The optical response of the device is shown in Fig. 10 for a V_{DS} of 5V.

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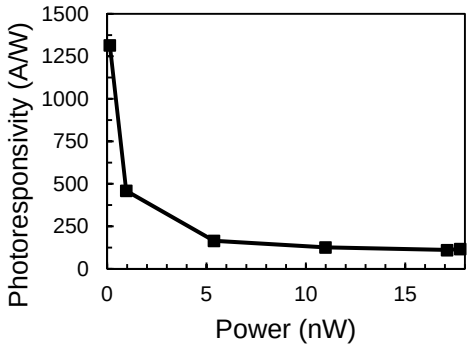

Fig. 10. Photoresponse of device at V_{DS} = 5 V with the highest magnitude of 1,314.45 W/A obtained at the minimum irradiance power of 0.134 nW.

The Table 1 shows a comparison between previous reports on MoS_2 photodetectors in which our work (first row) shows the highest photoresponse, magnitude at 5 V under vacuum at 300 K with a white light source, even though our device is two terminal under a relatively low voltage. This photoresponsivity is resulted due to the reduced lattice mismatch between the metal contacts used and the flake [15] and the clean and all-dry MoS_2 flake transfer method. Also, the photocurrent generated could be driven mainly by photothermoelectric effects since our device is composed by indirect a bandgap semiconductor [5], [6].

Table 1. Comparison on previous reports of MoS_2 photodetectors.

MoS_2	**Device**	**R (A/W)**	**λ (nm)**	**Ref.**
Bulk	2 terminal V_{DS} = 5 V	1,314	White light	[9]
2D	3 terminal FET V_{DS} = 1V V_G = 50V	$8x10^{-3}$	532	[3]
2D	3 terminal FET V_{DS} = 8V V_G = -70V	880	561	[16]
2D	3 terminal FET V_{DS} = 5V V_G = 100V	1,000	532	[17]
2D	3 terminal FET V_{DS} = 1V V_G = 100V	780	532	[18]
Bulk	2 terminal V_{DS} = 15V	$10x10^{-4}$	White light	[19]
Bulk	3 terminal FET V_{DS} = 1V V_G = -3V	$110x10^{-3}$	633	[20]

V. Conclusions

In this work, it has been demonstrated the CVD synthesis of MoS_2 and the fabrication of a multilayer mechanically exfoliated high-performance MoS_2 photodetector. It exhibits a high photocurrent for broadband light source. These results are promising which show a higher photoresponsivity (880 W/A) than three terminal 2D MoS_2 reported previously with a light source of 561 nm [16].

Acknowledgment

Support is acknowledged from the University of Texas System Faculty Science and Technology Acquisition and Retention (STARS) award (EC284802) for the acquisition of equipment in the establishment of the Nanomaterials and Devices Lab (NDL) at the University of Texas, El Paso (UTEP). We also thank the Air Force Office of Scientific Research (grant number FA9550-15-1-0200) that enabled us to pursue this work, and Dr. Deidra Hodges who provided assistance in the deposition of the metal using sputtering. G.K. and J.L.C. would like to acknowledge the support by the Energy Frontier Research Center (CCDM) funded by the U.S. Department of Energy, Office of Science under Award #DE-SC0012575.

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Pulsed Power Evaluation and Simulation of High Voltage 4H-SiC P-Type SGTOs

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***Abstract*— Future Army pulsed power applications semiconductor devices that will meet requirements for high-power, low weight and volume, and fast switching speed. The following paper presents the pulsed power evaluation of high voltage silicon carbide (SiC) super gate turn-off (SGTO) thyristors. These devices are well suited for high voltage, high temperature pulsed power and continuous power electronic systems. A pulse-forming network (PFN) circuit and a low inductance, series resistor-capacitor (LRC) circuit were developed to evaluate both the fast dI/dt capability and the pulse safe operating area (SOA) of the SiC SGTO. Transient simulations of the high voltage SiC SGTOs were also performed on a narrow pulse LRC circuit to investigate the device's switching behavior under extreme pulsed conditions.**

Keywords—Silicon carbide; Gate Turn-off Thyristor; Pulsed power; pulse-forming network; safe operating area

I. INTRODUCTION

Silicon carbide's (SiC's) enhanced material properties are paving the path for next generation power devices that will be used in various power electronics and pulsed power applications [1-3].. The Army pulsed power systems require the power devices to operate at fast speeds, high temperature, and high power density. SiC has various attractive properties compared to its silicon counterpart. Silicon carbide's material properties advantages such as a high critical field, high saturation velocity, high thermal conductivity, high energy bandgap, large elastic modules makes it extremely favorable for pulse switching systems and applications [1-4]. Due to its excellent conductivity modulation capability, Super-gate turn-off thyristors (SGTOs) are well suited for multiple applications that require fast *dI/dt* switching at extremely high peak current levels. The U.S. Army Research Laboratory (ARL) is interested in understanding the switching behavior of high power silicon carbide bipolar devices subjected to elevated current densities at unique time-scales in the microsecond and millisecond regime through modeling and simulation. Accurate physics-based SiC models and simulations are extremely essential and will enable better optimization of SiC device designs leading to enhanced device performance.

This work presents the pulse power evaluation and numerical transient simulation of high voltage SiC SGTO thyristors. The SGTOs evaluated in this paper are subjected to two different switching conditions. The transient simulations were performed utilizing a physics-based, technology computer aided design software. The simulation investigates the fast *dI/dt* switching capabilities of the SGTO in a narrow pulse LRC circuit.

II. DEVICE STRUCTURE

The SGTO devices investigated in this research were designed and fabricated by Wolfspeed, a Cree Company. The SGTOs have asymmetrical structures enabling a forward blocking capability of 10 kV and 15 kV. The forward blocking capability of the SGTO is primarily dependent on the thickness and doping concentration of the drift region of the device. The cross-sections of the SGTOs are shown in Figs. 1 and 2. These devices were fabricated on an 350 µm n+ SiC substrate. This resulted in the SiC SGTOs having the anode terminal on the topside and cathode terminal on the bottom side. These devices were also designed to have very high turn-on gain. A p-type buffer layer doped approximately 5e17 cm^{-3}, 4 um thick was grown on a SiC substrate. Low doped, p-layer of 90 µm (10 kV SGTO) and 120 µm (15 kV SGTO) was grown. The doping of the drift layer for both devices were within 2e14 cm^{-3}. Following this was the growth of n-type base layer, doped at approximately 1e17 cm^{-3}. The thickness of the base layer was 2 µm. Lastly, a heavily doped (>1e19cm^{-3}) p+ anode layer of thickness 2 µm was grown. Further design details of the devices characterized and evaluated in this research has been published by Wolfspeed and ARL and can be found in the following references [3-5].

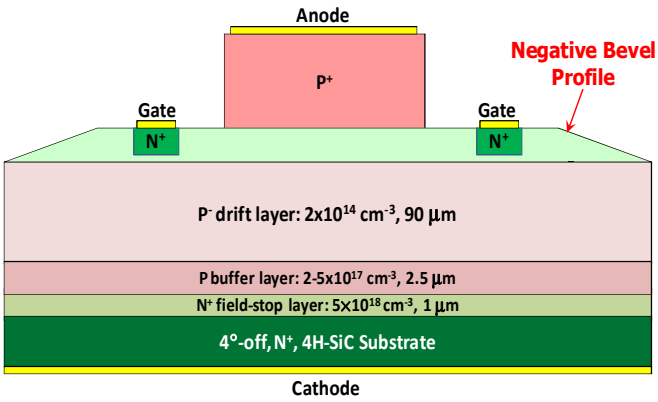

Fig. 1. Cross-section view of 10 kV, 1.0 cm^2 SiC Super-GTO. Note: the gate is anode referenced in SiC SGTO.

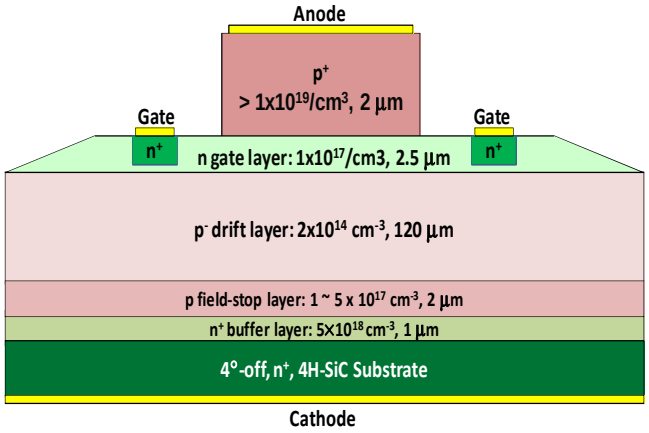

Fig. 2. Cross-section view of 15 kV, 1.0 cm^2 SiC Super-GTO. Note: the gate is anode referenced in SiC SGTO.

III. DEVICE EVALUATION

A low inductance, series resistor-capacitor (LRC) circuit and pulse-forming network (PFN) circuit were developed to evaluate the fast *dI/dt* capability and the narrow pulse safe operating area (SOA) of the SiC SGTO.

A. LRC Circuit

The pulse circuit implemented to analyze the fast *dI/dt* capability of the SiC SGTOs was a low inductance, series resistor-capacitor topology depicted in Fig. 3. The circuit inductance distribution was reduced by using a wide anti-parallel bussing configuration between the capacitor and the load. A low capacitance, Maxwell energy storage capacitor rated for 150 nF and used for rapid, high-current discharge was used to briefly store the charge voltage before the SGTO was triggered into the ON-state. The circuit load was comprised of HVR large-area bulk ceramic disk resistors designed to withstand high power and high energy.

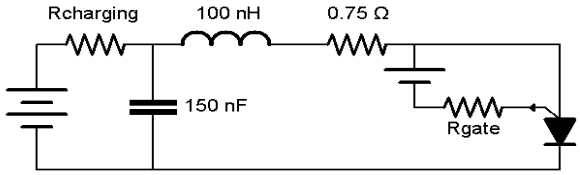

Fig. 3. Low inductance, series resistor-capacitor circuit schematic for evaluating the fast dI/dt characteristics of the SiC SGTO s

B. PFN Circuit

An automated pulse forming circuit unit was developed to evaluate the long-term reliability and safe operating area of high voltage SiC SGTOs at a 100us square pulse-width at 0.5 Hz rate, creating more 1^2t stress in the devices. The PFN was developed from discrete inductors and capacitors in order to generate the 100 µs full width half-maximum (FWHM) pulse used to evaluate the SiC SGTOs' pulse switching characteristics. The 10-stage Rayleigh pulse forming network was matched to a 0.5 Ω load which provides the 100 µs pulses. The PFN has a total capacitance of 85 µF and can be charged to 15 kV for a maximum pulse energy of 9.563 kJ. A simplified circuit schematic of the PFN is shown in Fig. 4. An expanded description of the system can be found in the following references [6-8].

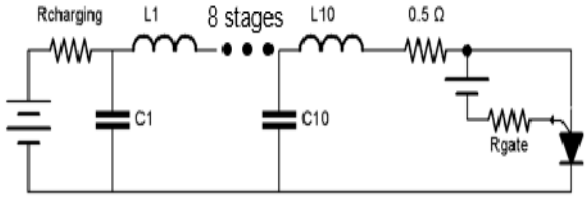

Fig. 4. Simplified 10 stage PFN schematic for evaluating the long term reliability and safe operating area characteristics of the SiC SGTOs

IV. EXPERIMENTAL RESULTS AND DISSCUSION

This section highlights the switching characteristics of the SGTO devices when implemented in a LRC and PFN circuit topology. The spreading velocity is the rate at which the plasma spreads across the area of the thyristor. This device parameter is essential for determining the switching rate of the SGTO and the maximum *dI/dt* capability of the SGTO. The turn-on delay of the SGTO is affected by increasing the gate current. For the maximum *dI/dt* characterization of the 10 kV and 15 kV SGTO, a peak gate current of 400A/µs was used to drastically reduce to turn-on delay, which accelerates the conductivity modulation process in the device, maximizing the peak current flowing through the device at a given charge voltage.

A. 10 kV SiC GTO

The maximum peak *dI/dt* achieved with the 10 kV SiC SGTO utilizing the LRC is illustrated in Fig. 5. The *dI/dt* was 11 kA/µs measured across the 10-90% ratio of the peak

current pulse. The maximum peak current attained with the 10 kV SiC SGTO in the LRC circuit was 1.830kA (2.5 kA/cm^2). At 1.830kA, the device approached saturation in the LRC circuit due to the fast rate of current rise at the current level.

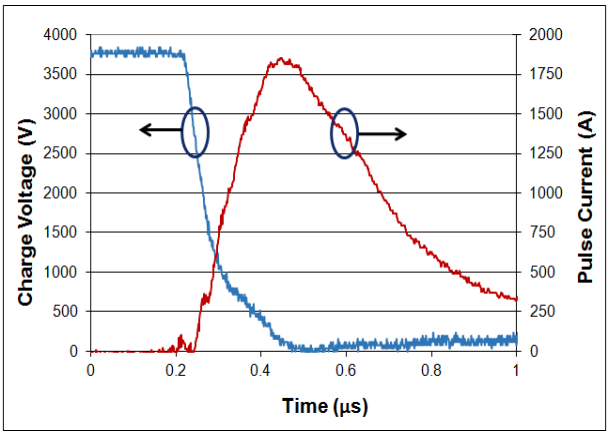

Fig. 5. Maximum dI/dt capabiity of the 10 kV SGTO. the peak dI/dt in LRC circuit was reached at a current amplitude of 1830 A. The dI/dt measured from 10-90% of maximum current level was 11 kA/µs.

A safe operating area level with respect to peak pulsed current with a FWHM pulse-width of 100 µs was established with the 10 kV, SiC SGTOs at a peak current of 2.0 kA (Fig. 6). This device achieved over 100,000 pulses at a nominal current level of 2.0 kA. The current rising edge dI/dt was 0.350 kA/µs at 2 kA. It is important to note that the current rise edge was not limited by the SiC SGTO but by the output inductance of the PFN design. the device performed reliably without any significant degradation at pulsed current levels up to 2.0 kA (Fig. 6). At peak current levels above 2.0 kA, an abrupt shift in the device forward voltage was observed. It was believe that the forward voltage shift was attributed to the device over-heating and thermal runaway. The increased peak power and peak energy dissipation in the SGTO above 2 kA ultimately lead to the catastrophic failure of the device.

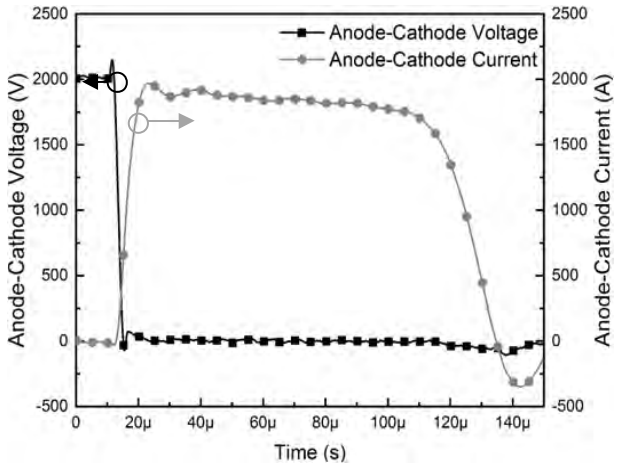

Fig. 6. 2.0 kA pulse current discharge in 10 kV SGTO utilizing a 10 stage PFN Circuit

B. *15 kV SiC GTO*

The thicker epilayer thickness of the 15 kV SGTO compared to the 10kV SiC SGTO increases the turn-on delay and on-resistance, which reduces the dI/dt and peak current handling capability of the device as shown in Fig. 7. The maximum peak dI/dt achieved with the 15 kV SiC SGTO utilizing the LRC circuit is illustrated in Fig. 7. The dI/dt was 8kA/µs measured across the 10-90% ratio of the peak current pulse of 1.37 kA (2.6kA/cm^2). At 1.370 kA, the device approached its current saturation limit in the LRC circuit due to the current rate of rise time (*dI/dt*).

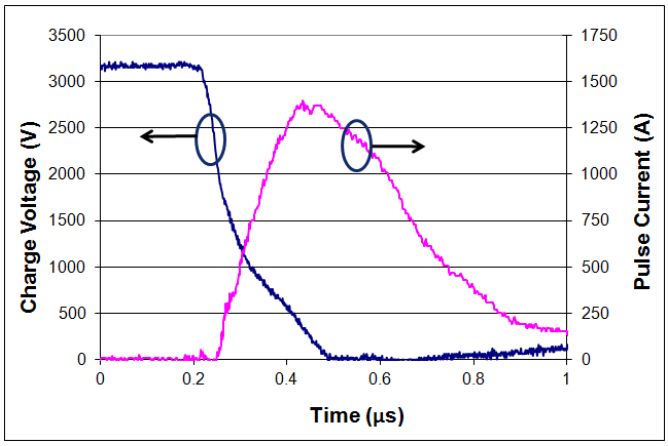

Fig. 7. Maximum dI/dt capability of 15 kV SGTO: the peak dI/dt in LRC; circuit was reached at a current amplitude of 1370 A. The dI/dt measured from 10-90% of maximum current level was 8 kA/µs.

The baseline peak current level of 2 kA with a 100 µs square pulse-width was used to access the safe operating area level of the 15 kV, SiC SGTOs as shown in Fig. 8. The 15 kV SGTO device achieved over 70,000 pulses at a nominal current level of 2.0 kA, however it degraded drastically, implying that the SOA for the 15 kV devices is less than 2 kA.. The failure modes are similar to those observed with the 10 kV SiC SGTO and has been recently published in [8].

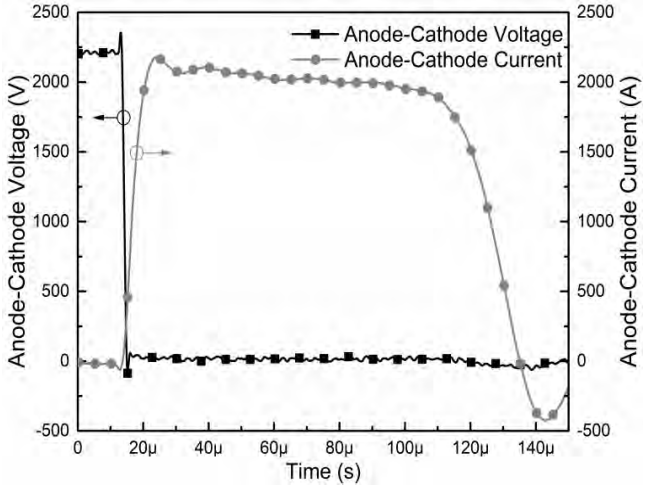

Fig. 9. 2.0 kA pulse current discharge in 15kV SGTO utilizing a 10 stage PFN Circuit

V. Simulation Results and Analysis

As mentioned previously, the gate current affects the turn-on delay of the GTO. Fig. 10 illustrates the gate current comparison as a function of the gate resistor. The series gate resistance used on the SGTO ranged from 10 Ω, 1.5 Ω, and 0.75 Ω. These gate resistors corresponded to peak applied gate currents of 10 A, 64 A, and 128 A, respectively. The gate current rise rate at 10 ohm (10 A peak) was 200 A/µs, while the gate current rise rate rising at 1.5 ohm (64 A peak) and 0.75 Ω (128 A peak) was approximately 400 A/µs. Fig. 10 shows that simulated gate current rising edge results agrees fairly well with the experimental results.

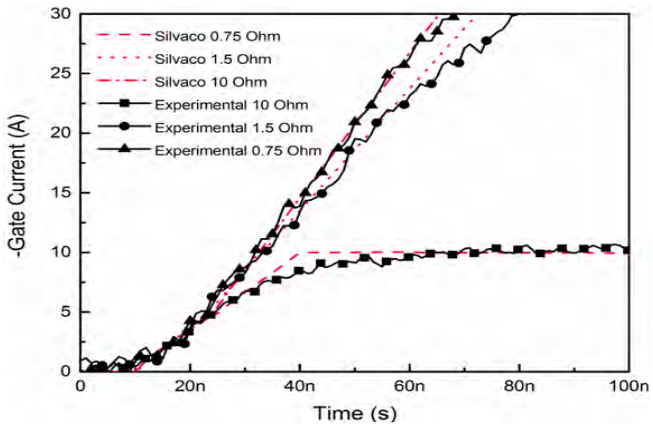

Fig. 10. Experimental v. Simulation of the rising edge of different gate drive currents used to determine minimum turn-on delay.

Fig. 11 depicts simulation of 10 kV SiC SGTO as a function of gate resistance. The simulation was done with a charge voltage of 3 kV. The simulated results show that the SGTO is triggered-on slightly faster when utilizing a low gate resistance. Furthermore, the variation in peak current is approximately 153A between the gate resistance of 10 Ω and 0.75 Ω.

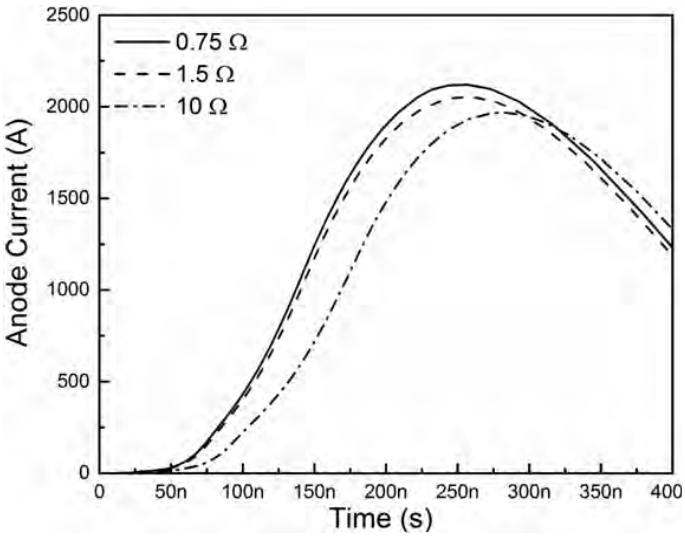

Fig. 11. 10 kV SiC SGTO simulation of the turn-on delay as a function of gate resistance

VI. Conclusion

The fast *dI/dt* capability of the high-voltage SiC SGTOs was evaluated in a narrow-pulse LRC circuit, and their long-term pulse power reliability was determined using a an automated pulse forming network system that generates a 100 µs pulse-width. The robustness and the fast *dI/dt* handling capability of the devices presented in this research prove that SiC is an excellent candidate for pulsed power applications.

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