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RPPR Final Report
as of 17-Nov-2017

Agency Code:

Proposal Number: 65551EL **Agreement Number: W911NF-14-1-0291**
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Final Report for Period Beginning 01-Jul-2014 and Ending 30-Jun-2017
Title: Compact, Low-Power, and High-Speed Graphene-Based Integrated Photonic Modulator Technology
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Report Term: 0-Other

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STEM Degrees: **STEM Participants:**

Major Goals: This research is focused on the development of the infrastructures for new nanophotonic material and device platforms through integration of single-layer and double-layer graphene structures with CMOS-compatible substrates (primarily silicon (Si) and silicon nitride (SiN) to enable ultra-fast low-power modulators. The goals of this project are achieved through the following tasks:

1) Development of a vertically integrated hybrid material platform that combines CMOS-compatible (i.e., Si-based) substrates with single- and multi-layer graphene and high-k dielectrics to yield high performance (e.g., ultra-fast carrier dynamics, low optical loss, strong free-carrier plasma effect) devices.

2) Development of new miniaturized resonators with moderate Qs and ultra-low mode volumes that break the trade-off among the operation voltage, power dissipation, and operation bandwidth.

3) Optical mode design by vertical integration of dissimilar materials through ultra-thin buffer or slot layers to form horizontal miniaturized resonators with strong light-matter interaction in the material active region (e.g., nonlinear optical polymer in the slot)

4) Enabling reconfiguration (and in especial case, modulation) through carrier accumulation in high carrier density materials (graphene) and strong light-matter interaction in high-quality-factor (or high-Q) resonators to achieve ultra-compact resonance-based modulator designs with high modulation speed, low operation voltage, and low power consumption (at least one order of magnitude better performance compared to state-of-the-art Si-based modulators).

5) The use of a novel interferometric-based structures in a high-Q resonance platform to break the trade-off among the modulation bandwidth (usually varying inversely with Q) and the modulation sensitivity (or the operation voltage; varying directly with Q through light-matter interaction).

Accomplishments: Please see the attached file

Training Opportunities: Nothing to Report

Results Dissemination: The results were presented in several conferences in the form of contributed talks, invited conference talks, and invited seminar talks. The complete list is provided in the attached report.

RPPR Final Report
as of 17-Nov-2017

Honors and Awards: The PI (Ali Adibi) received the institute-level "Advisor of the Outstanding PhD Thesis" Award from Georgia Tech Sigma Xi in all 3 years of this research (2015, 2016, 2017); Adibi has received this award for 7 years in-a-row, which is an all-time record at Georgia Tech.

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Technology Transfer: Nothing to Report

PARTICIPANTS:

Participant Type: PD/PI
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Person Months Worked: 1.00 **Funding Support:**
Project Contribution:
International Collaboration:
International Travel:
National Academy Member: N
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Project Contribution:
International Collaboration:
International Travel:
National Academy Member: N
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Project Contribution:
International Collaboration:
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Other Collaborators:

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Person Months Worked: 6.00 **Funding Support:**
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National Academy Member: N
Other Collaborators:

RPPR Final Report
as of 17-Nov-2017

Final Report to the

Army Research Office (ARO)

Compact, Low-Power, and High-Speed Graphene-Based Integrated Photonic Modulator Technology

Georgia Institute of Technology

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I. Introduction

This final report summarizes achievements in Dr. Adibi's research group at Georgia Institute of Technology in the area of "Compact, Low-Power, and High-Speed Graphene-Based Integrated Photonic Modulator Technology", supported by award grant number W911NF-14-1-0291 since July 1 2014. Major achievements until June 30 2017 with brief descriptions are listed in this report. The focus of this report is on the recent achievements during the last year of the project and the main achievements in the first two years of the program (that are reported in previous annual reports) are briefly included.

This ARO-supported program started on July 1 2014 and was directed toward developing a hybrid integrated photonic platform for realization of high-speed and low-power optical modulators based on integration of graphene with CMOS-compatible substrates.

Optical interconnects are poised to replace metallic wires in short-range communications networks at different levels, including board-to-board communications between different processing units in computer clusters, chip-to-chip communications on electronic board between different processors and memory units, and even intra-chip between different processing cores. With the ever-increasing need for higher computation power and higher data rates, the dissipated heat due to the interconnection network has become one of the main challenges and facing the advancement of the current processing systems. Optical interconnection is the most promising solution that can mitigate this challenge by enabling broadband and low-power communication networks. However, to realize such solution, especially for intra-chip interconnect networks, there is an urgent need for a new optical communication subsystem/device technology to achieve these data rates at very low power consumption to avoid any energy dilemma. One of the main building blocks of such systems is a high-speed and low-power optical modulator. Current modulation technologies such as directly-modulated lasers (e.g. VCSELs) and silicon photonic modulators based on carrier dispersion (e.g., PN-junction-based modulators) face several limitations in delivering the stringent system requirements of next-generation optical interconnects in terms of speed and power consumption. The goal of this ARO-funded research program was to develop the necessary infrastructure to enable a new class of modulators based on the hybrid silicon-graphene (HSG) material platform. Taking advantage of the high carrier mobility and the strong plasma dispersion effect of graphene combined with strong light confinement in compact Si-photonic devices, this program was aimed at developing a novel material and device platform, which can enable modulators with modulation speeds reaching 100 Gb/s and sub-100 fJ/bit energy consumption. These target modulator performance measures surpass the existing on-chip modulating solutions in terms of modulation speed while enabling 5 times less power consumption than the best-reported Si-photonic modulators for similar speeds.

During the three-year period of this research, we developed two major graphene-based integrated nanophotonics material platforms with very high quality based on: 1) integration of single layer graphene with silicon on isolator (SOI) namely graphene-on-Si (GoS), and 2) integration of double-layer graphene on silicon nitride (SiN), namely graphene on SiN (GoN). While the first platform enables to achieve low-power modulator devices with specifications that considerably surpass those of Si-photonic modulators, the second platform enables high-performance modulators in the SiN platform that lacks any modulation

mechanism otherwise. In realization of the proposed high-performance modulators several major challenges in different aspects of the process had to be addressed. At the material layer, an optimal mechanical transfer process was needed for the integration of atomic-thin graphene layer, grown by chemical vapor deposition (CVD), with CMOS-compatible material platforms to achieve a reasonably high-yield process, which preserve the as-grown graphene layer without any tears or wrinkles. In the device fabrication, an optimal process was needed for processing (i.e., patterning and etching) of the monolayer graphene, while preserving its distinctive electrical and optical properties (e.g. carrier mobility) through a complex multi-stage fabrication process. At the design level, the understanding of the roles of the design parameters and utilization of the trade-offs among parameters affecting device speed and power consumption (e.g., the device capacitance, device resistance, and modulation performance) was needed to find the optimal device design by adjusting different device parameters, including different parameters in device geometry, different material layers doping/electric gating, and optical specification of the integrated photonic device (e.g., quality factor). We performed extensive research in addressing these challenges, and the resulting material platforms after this program are at the best quality compared to all existing reports.

In addition to the development of very high-quality material platforms, we have also demonstrated graphene-based modulators based on different alternative modulator architectures in both GOS and GON material platforms. In the GOS platform, we have demonstrated optical modulation based on carrier accumulation in graphene-layer in miniaturized hybrid (graphene/Si) resonators with the possibility of achieving high-speed operation. We have also developed a technique for achieving high carrier mobility in graphene for modulator structures based on sandwiching graphene between a pair of few-layer-thick boron-nitride (BN) films to improve the modulation speed. In the GON platform, we have demonstrated several alternative modulator architectures including Mach-Zehnder interferometer (MZI)-based, resonator-based, and coupling-modulation-based modulators. To maximize the device quality and the yield of the fabrication process, we have demonstrated a new technique to planarize the SiN device after photonic device patterning. Our experimental results show the resulting modulators have the potential to surpass the performance of the more conventional Si-photonic modulators based on carrier accumulation in Si. We have also proven the capability of these platforms for the implementation of the desired high-speed and low-power modulators (which will be pursued in a follow-on program). In addition, the unique capabilities of the demonstrated platforms are not limited to the design of modulators; they enable many other important integrated photonic functionalities that have been conventionally implemented in Si (e.g., reconfigurable nanophotonic devices, tunable filters, ultrafast switches, reconfigurable add/drops and multiplexers/demultiplexers, etc.).

II. Research Accomplishments

In this section we briefly review or research progress in different areas. More details will be available upon request.

II.1. Single layer graphene on silicon modulators

II.1.1. Fabrication of passive SOI devices

We designed micro-disk resonators with radius of 3 µm and 20 µm, and slot structures with radius of 10 µm as our optical devices, all at working frequency of 1550 nm.

The silicon on insulator (SOI) we used in the design and fabrication is 250 nm silicon with 3 µm box oxide beneath on 500µm silicon substrate. First the negative-resist Hydrogen silsesquioxane (HSQ) 6% was spin-coated on SOI substrate. The approximate thickness of HSQ on SOI was about 85 nm. Next, electron beam lithography (EBL) was used to pattern HSQ to form mask on SOI. The chloride etching was used afterwards in an inductively-coupled plasma etching tool (Plasma Thermal ICP). The etching rate was recorded about 108nm/min. Before conducting the etching process, the chamber needed to be cleaned carefully to minimize the effect of particle contamination which would otherwise compromise the sidewall roughness and reduce the quality factor. Finally, after etching 200 nm of Si (leaving a pedestal of 50nm), the passive structure passed the inspection under microscope. We also monitored it under SEM to check the sidewall roughness. Figure 1 shows an optical image of the passive structure and a closely zoomed in SEM image of the fine designed gratings. Owing to the stable DC power and reduced particle contamination during the etching process, the roughness was virtually negligible under SEM.

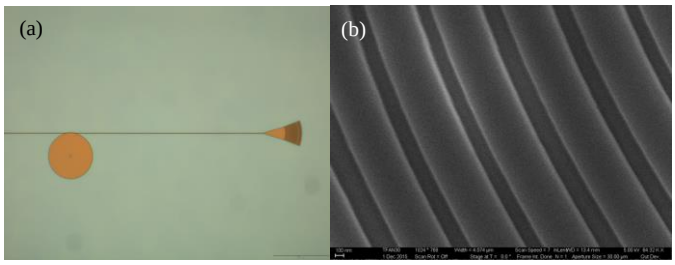

Figure 1. (a) optical image of silicon micro disk resonator, and (b) SEM image of fine designed grating structures

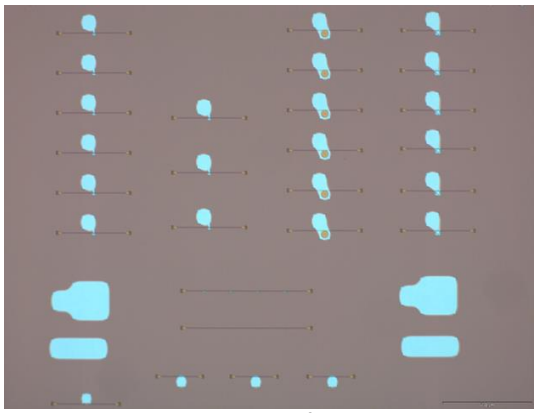
Figure 2. Optical image of devices with 50nm silicon pedestal.

To remove the unwanted area of pedestal which is required for effective capacitance reduction and high-speed operation, negative resist Ma-N 2403 was spin-coated on the substrate with the thickness of about 500 nm. Aligned EBL was performed to pattern the ma-N to cover only the part needed. Chloride etching with Plasma Thermal ICP was performed next to remove the region of unwanted 50 nm pedestal and left reasonable space of silicon to form the back-gate contact. After the etching process, Ma-N was removed with acetone. Figure 2 shows an optical image after etching the pedestal.

To this point, the passive structure was formed. We did measurement of quality factor for the devices we fabricated on our near-infrared (NIR) characterization setup. For the small disks with radius of 3µm, we got the quality factor equals to 10k. For the big disks with radius of 20 µm, we got the quality factor equals to 100k.

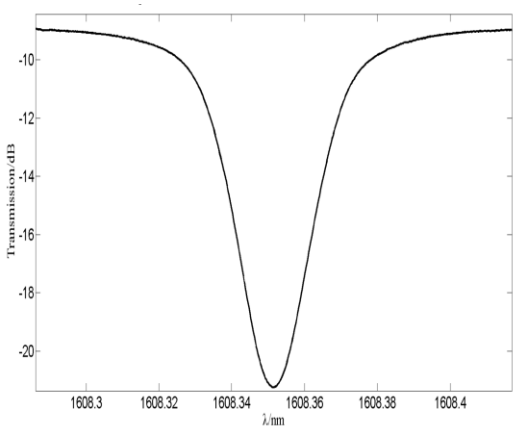

Figure 3. Transmission spectrum of a 3 µm micro disk resonator before annealing.

After the characterization, the next step is ion implantation to reduce the resistance for the sake of speed. Before ion implantation, the HSQ was removed using Buffered Oxide Etchant (BOE), and a thin (30nm) layer of Al2O3 is deposited by Atomic Layer Deposition (ALD) method as the channeling mask during the ion shooting. We did 3 steps of ion (phosphorous) implantation process on the sample including N++ implantation, low-energy N implantation, and high-energy N implantation. For each step of implantation, first we spin-coated thick (1 µm) PMMA A11 and defined the mask by EBL. Then we did ion implantation on the sample. After that, we removed PMMA by acetone and repeated the similar process for next step of ion implantation. After all steps of ion implantation done, we cleaned sample with acetone, removed Al_2O_3 with BOE, and finally did rapid thermal annealing (RTA) at 950 degree for 2 minutes to active the ions.

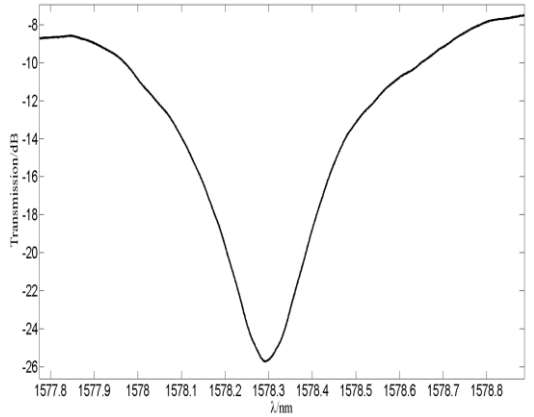

Figure 4. Transmission spectrum of a 3 µm micro disk resonator after annealing.

After annealing, we re-measured the same device to see its quality factor. For the 3um disk, the quality factor did not drop that much (5k) since there was considerable radiation loss due to the curvature. For the 20 µm disk, the Q drops to 20k since ion implantation introduces additional material loss.

Next step is to form metal contact on silicon layer. First we spin-coated PMMA A6 (thickness 500nm) on the sample. Then we defined the mask for our metal contact by EBL. Last step was to deposit metal onto the silicon pedestal. We used aluminum since it delivers good ohmic contact with N-doped silicon. First we deposited 20 nm titanium as the adhesion layer, and next we deposited 200 nm aluminium as the metal pad. The deposition was done by electron beam (e-beam) evaporation.

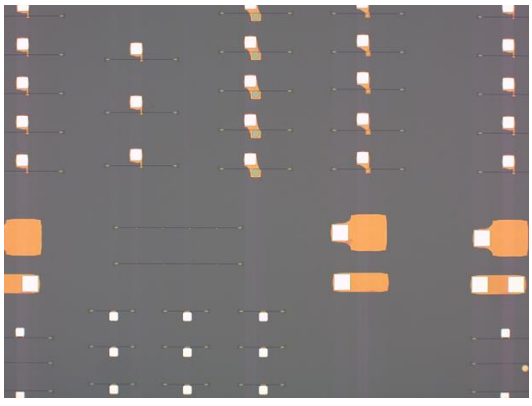
Figure 5. Optical image of devices with contact on back gate.

After making contact on the silicon layer, we deposited 30 nm Al_2O_3 as the gate oxide by ALD. Theoretically, 100 Ω resistance coming from graphene contact resistance and transmission line itself and

100 fF capacitance coming from graphene-silicon capacitor together would give us an operation speed of 30 GHz for 3 µm disks. The electric field induced by 15V voltage applied on 30 nm Al2O3 on graphene could deliver theoretical resonance shift of 400 pm. Also, a breakdown voltage test was performed on the sample, and it turned out voltages between +15V to -15V on 30nm Al2O3 are in compliance range of the device functionality.

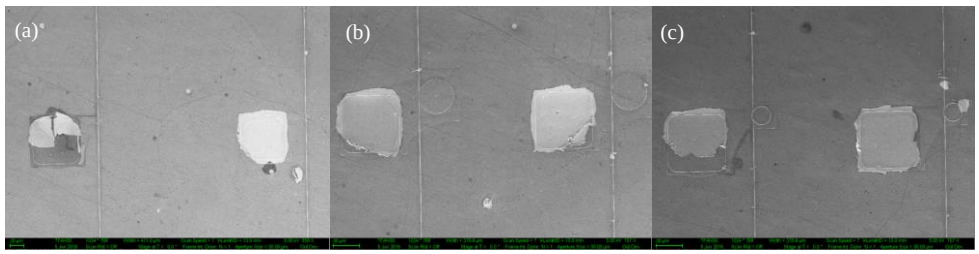

Figure 6. SEM images of (a) 3um micro disk resonator, (b) 20um micro disk resonator, and (c) micro slot ring resonator with graphene transferred on top.

II.1.2. Fabrication of graphene layer for modulation.

After depositing the gate oxide, we transferred single layer graphene on devices through the conventional transfer method using the Marble's reagent (CuSO4/HCl/H2O: 10 g/50 mL/50 mL). After transferring graphene, as shown in Figure 6, we found that it was broken on the Al pads due to height difference, which was desirable since we did not want contact between Al and graphene. Meanwhile the parts left on the disks and rings were complete.

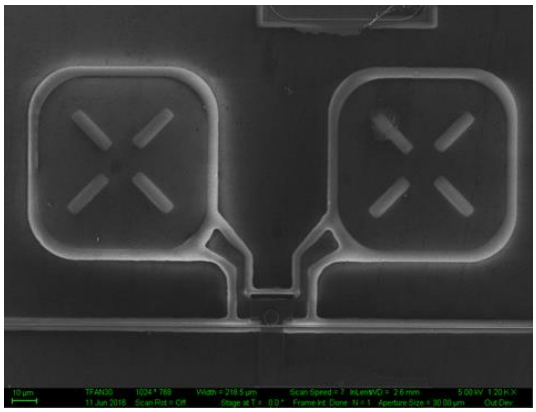
Figure 7. SEM images of devices after removing the unwanted area of graphene.

After transferring graphene on our sample, we did another step of EBL with PMMA A6 to define the mask to remove the region of unwanted graphene. We used Vision RIE to conduct a 5-second Oxygen plasma etching to remove graphene. After etching, we used acetone to remove the PMMA and checked the sample under SEM.

Based on SEM observation, the part of unwanted graphene was totally removed and the box oxide layer was partially etched. Figure 7 shows the SEM image after patterning the graphene. We measured the quality factor after transferring and patterning the graphene. The quality factor dropped to 800 for small disks, due to the absorption of graphene in the near-IR range.

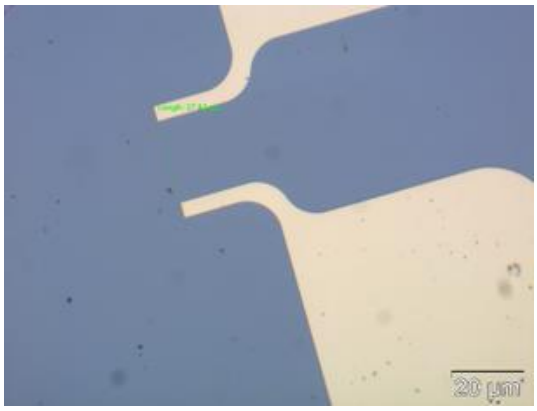

Figure 8. Optical images of the metal contacts on graphene.

The last step was to form metal contact on graphene. In the real experiment, we would add bias on graphene, probably high back gate voltage. Under this condition, the graphene would be biased at a point where its sheet resistance was decreased. The contact resistance played an important role in the RF performance of the device. The resistance management is especially critical

for the performance of devices based on graphene at high-speed applications. Typically metal with high work function compared to graphene was preferred which provides lower resistance such as Pd. [1]

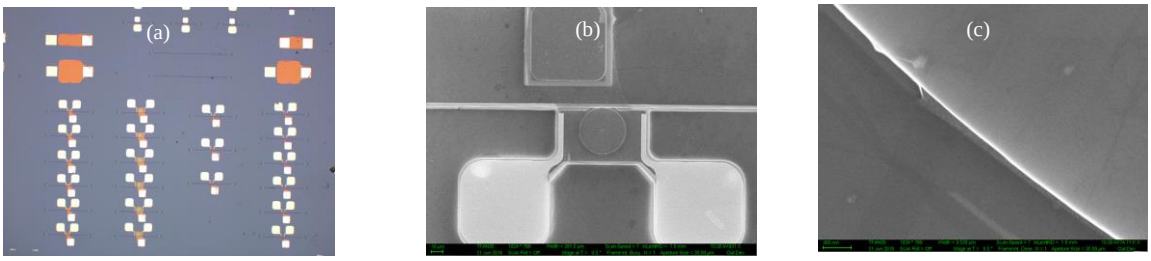

Figure 9. (a) optical image of the completed devices, (b) SEM images of the 20um micro disk resonator, and (c) SEM image of the edge of micro disk.

Before conducting any experiment on the real sample, we made a test sample with two identical contact on top of graphene with 1.5nm Ti/45nm Pd/15nm Au deposited by E-beam evaporation. By measuring the I-V curve, we got the value of resistance (a combination of sheet resistance and contact resistance) at zero bias point as 200Ω.

In the end we chose to deposit 1.5 nm Ti as the adhesion layer, 45nm Pd and 15 nm Au as the pads on graphene by E-beam evaporation. After all the process had been done, we deposited 10nm Al_2O_3 by ALD to passivate the graphene.

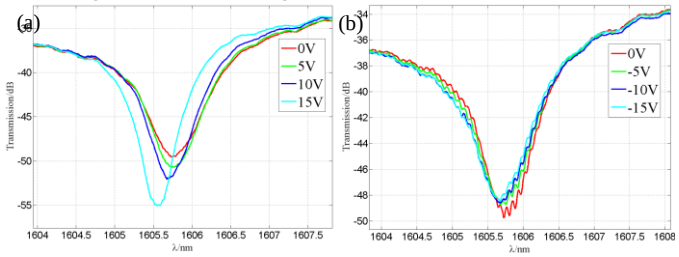

Figure 10. Transmission spectrum of graphene modulator by applying (a) positive back gate voltage, and (b) negative back gate voltage.

II.1.3. Characterization of the final devices.

Finally, after all steps were done, we took a close look at the final device. graphene survived after all the process. It was not broken at the edges of our disks/rings.

We did quality factor measurement of the device on our near IR setup. We applied voltage between graphene and silicon, and got an 8 dB extinction change over 10V change of DC gate voltage. Meanwhile the quality factor increased from 900 at 0V to 1200 at 15V. It showed that we are changing the index of graphene as well as its absorption by injecting free carriers. [2] We got 300pm shift of the resonance peak over 15V range. On the contrary, by applying negative voltage, the resonance did not vary that much.

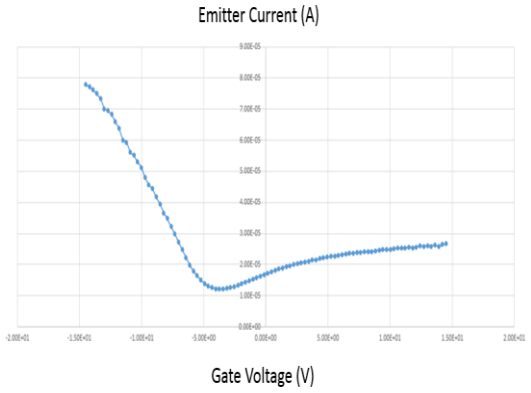

Figure 11. Current going through graphene versus back gate voltage applied on graphene modulator.

Meanwhile, electrical measurement was done on the sample. We applied 0.1V between the two metal contacts on graphene while sweeping the voltage on the back-gate. We read currents between the two metal contacts on graphene.

The shape of the curve indicated that the change of graphene resistance was different between the negative and positive sweep of back gate voltage. It was consistent with the direction of shifts we got in our optical measurement. From the curve, we got the graphene resistance between 2 pads as 8 kΩ at 15V and 1 kΩ at -15V. In the end our resistance was 500 Ω at negative high bias.

II.2. Improved high speed h-BN encapsulated single layer graphene modulators

We wanted to further reduce the resistance of graphene we have got from single layer graphene on silicon structures so that our device could work for even higher speed modulation. We introducde an h-BN-encapsulated graphene structure on our ultra-compact microdisk resonators (3μm radius) in SOI platform to shield graphene from trapped charges and surface phonons.[3] This structure had been proved to maintain the high intrinsic mobility of graphene in order to further reduce the resistance for higher speed.[4]

II.2.1. Fabrication process

We fabricated the waveguide-coupled optical microdisk resonator with 50nm silicon pedestal on a SOI wafer through electron beam lithography (EBL) and an induced coupled plasma (ICP) etching process. We selectively doped the silicon region to n-type through ion implantation- low energy doping for the whole silicon layer, high energy doping for the disk region, and shallow heavy doping for the contact region. 15nm alumina was deposited as the gate dielectric on the doped sample by atomic layer deposition (ALD). Then a 13nm thick multilayer h-BN was transferred onto the sample as both the other half gate dielectric and the bottom shield for graphene through the conventional transferring method using the Marble's reagent ($CuSO_4$/HCl/H_2O: 10g/50mL/50mL). Afterwards, a single layer graphene was transferred onto the bottom h-BN and another layer of multilayer h-BN was transferred on top of graphene as the top shield. The unwanted graphene was patterned by EBL and etched away by oxygen plasma to reduce the resistance as well as capacitance. Only a 2μm wide graphene ribbon was left on the periphery of the disk resonator to cover the part where whispering gallery mode exists. The metal contacts were made by EBL and electron beam evaporation on graphene (1.5nm Ti/45nm Pd/15nm Au) and on silicon (10nm Ti/200nm Al). The schematic of the envisioned device is shown together with optical image and scanning electron microscope (SEM) image of the fabricated sample in in Figure 12.

During the inspection under SEM, we noticed that multilayer h-BN acted as a layer for planarization to reduce the height difference between 250nm thick silicon and the substrate. As can be seen from Figure 13. (a), we happened to found a region with bottom h-BN folded to one side so that on the other side graphene sit on alumina. On the side without bottom h-BN, graphene cracked due to the step height of waveguide while it was safe on the other side. And we could also see from Fig 13. (b) graphene looked ultra-smooth when it sits on h-BN.

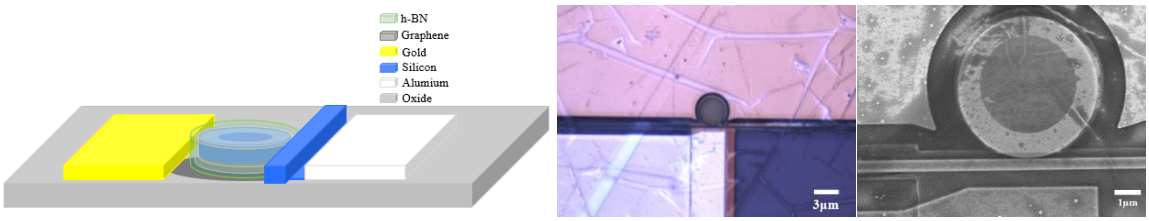

Figure. 12. (a) Schematic of envisioned device, (b) optical image shows the metal contacts, (c) SEM image shows the graphene and h-BN

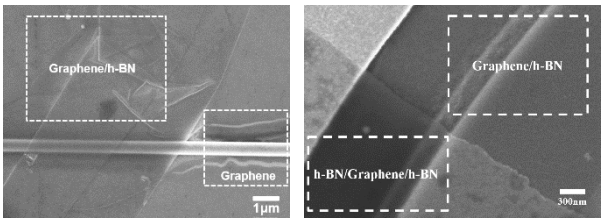

Figure 13. (a) SEM image shows folded h-BN beneath graphene, (b) SEM image shows graphene on h-BN and graphene encapsulated by h-BN

II.2.2 Characterization of the final devices

We conducted an I-V measurement to study the resistance of a sheet of graphene (100μm by 100μm) with/without h-BN encapsulation. We characterized our modulator by inducing and collecting near-infrared laser light through grating couplers on two ends of the waveguide separately. We measured transmission spectrum while applying different voltage from 0V to 20V between graphene and silicon.

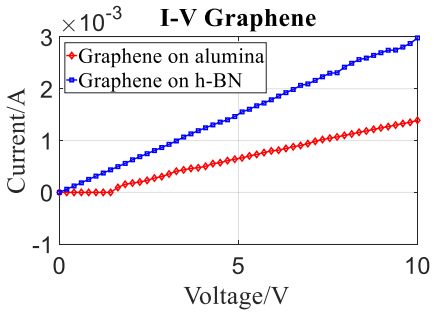

Figure 14. I-V curves of graphene sheet (100μm by 100μm), with Alumina and on h-BN.

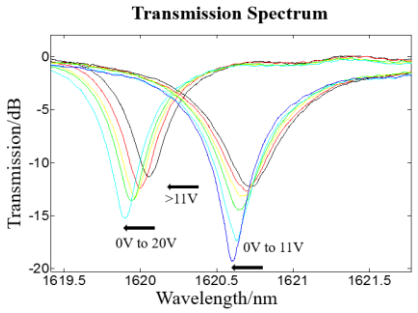

Figure 15. Transmission spectrum of device on voltage bias

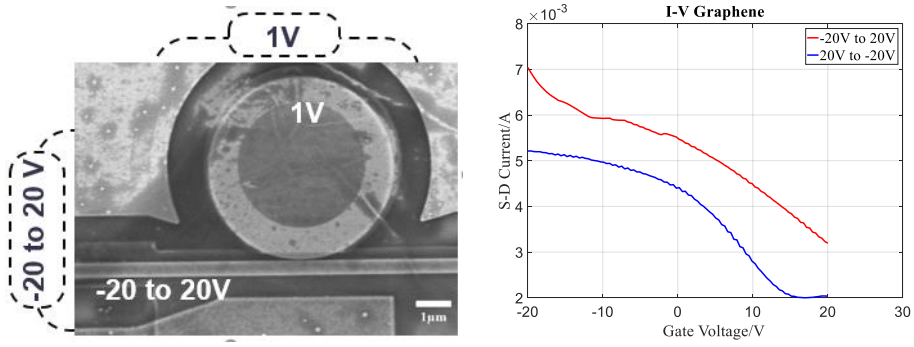

Figure 16. (a) Schematic of the device with voltage applied, (b) current between two contacts (0.1V applied between contacts) on graphene measured with gate voltage applied.

II.2.3 Results and analysis

In figure 14 we compared the I-V curves of the graphene with/without h-BN encapsulation. It is evident that graphene resistance was reduced by a factor of 1/2-1/3 when its intrinsic properties was protected by h-BN. It was explained as the fact that h-BN protects graphene from trapped charges and surface phonons on alumina or oxide substrate.

In figure 15 we find that the resonance blue shifted by 200pm and the loaded quality factor improved from 2.1k to 2.4k while sweeping voltage from 0V to 11V. When the voltage went above 11V, we observed a 700pm large blue shift of the resonance and the quality factor further increases to 2.8k. After the large shift, we could still manipulate the resonance by applying voltage from 0V to 20V to get 200pm blue shift and to further increase the quality factor to 3.1k. We noticed the resonance did not go back after the large shift happened. The large shift could come from charge trapping in multilayer h-BN. Further characterization was being done to confirm the source of the large shift.

In figure 16 we found that total resistance of the graphene side was less than 150 Ω (75 Ω on one side), which was composed of contact resistance less than 50 Ω and sheet resistance less than 25 Ω.

II.2.4 Conclusion

We have successfully integrated h-BN/Graphene/h-BN structure onto ultra-compact silicon microdisk resonators in SOI platform. We demonstrated reduced resistivity of graphene and the active interaction between optical mode and voltage-gated graphene. Our device could be used for high speed modulation and other photonic applications.

Further improvement of the contact resistance is possible. We believe that the contact resistance is even smaller than 50 ohm and sheet resistance may be the major issue here, but have stayed with more conservative estimation.

The measured device capacitance based on the required voltage to compensate for the initial doping of the graphene on Al_2O_3 substrate (~ 0.33 eV) and 20 um^2 area is 10 fF (corresponding to ~70 nm oxide dielectric layer). However, based on the model assuming the 15 nm Al_2O_3 and 12 nm BN the capacitance

should be 36 fF. The measured capacitance of 10 fF matches better with the shift measurements as well (corresponding to a carrier concentration of $5x10^{12}/cm^2$ for an applied voltage of 15 V on the capacitive device). The 10 fF with a resistance of 150 ohm leads to a calculated 3dB frequency response ($1/(2\pi RC)$) of 100 GHz. However the for the calculated capacitance of 36 fF this will reduce to 30 GHz. At 30 GHz 3dB, you can get a baud rate as high as 60 GS/s.

Here we have not included the silicon side resistance, which is expected to be around or less than 75 ohm. Therefore the assumption of 150 ohm total resistance, 75 ohm single side graphene and 75 ohm Si is not a bad estimate and could be improved in both graphene/silicon and double-layer graphene structures.

Over this device a 10 V voltage change on graphene is resulting to ~ 250 pm shift (matches with 10 fF effective capacitance), which for the current device with ~ 1k quality factor results in a modulator with 2 dB insertion loss and 5 dB modulation depth. If the Q of the resonator was 4K that we have in similar devices and should be easily achievable, this could result in an insertion loss of 1 dB and modulation depth of 10 dB.

Design based on 10 fF capacitor assumption and modifying the design should give us 1dB insertion loss, >10 dB modulation depth (equivalently 2dB insertion loss and > 25 dB modulation depth), > 50 GHz 3dB bandwidth (100 G baud rate), ~ 3.3 V modulation voltage, and ~ 75 fJ /bit.

III.1. High-speed double-layer graphene modulators on silicon nitride (SiN)

SiN platform has a wide range of application in integrated optics for its low optical loss at Near IR and visible range. [5,6] A major shortcoming of SiN is its lack of a reliable tuning mechanism. The capability to tune optical devices (e.g., resonance wavelength of resonators) is an important requirement to make reconfigurable devices such as switches, modulators. [7,8] Unfortunately, conventional tuning mechanisms that have widely been used for Si-based devices cannot be used for SiN-based ones. For instance, while reconfigurable devices based on carrier injection and depletion (through relatively strong plasma dispersion effect in silicon) have been demonstrated on SOI platform [9], the same devices cannot be implemented in SiN due to its insulating nature. Another widely used tuning mechanism in silicon is thermal reconfiguration through its relatively strong thermo-optic coefficient (TOC). [10] This approach is technically possible in SiN, but because the TOC in SiN is one order of magnitude lower than in Si, it cannot be used as an effective tuning mechanism in SiN. Moreover, thermal tuning is inherently a slow process; therefore, we need to come up with novel approaches to tune SiN-based optical devices. One example could be to integrate other materials with the SiN platform to enable efficient and fast reconfiguration techniques. [11] One excellent candidate in doing so is graphene. Graphene is a monolayer of carbon atoms in a hexagonal lattice, and has attracted a great deal of attention due to its unique mechanical, electrical, and optical properties. Moreover, graphene interacts remarkably with light across infrared and visible spectrum with ~2.3% absorption of normal incident light, even though it is composed of a single monolayer of atoms. This is due to the unique zero-gap electronic band structure in graphene. Furthermore, the absorption spectrum of graphene can be tuned by electrostatic gating to change the Fermi level through application of voltage. Graphene also exhibits remarkably high carrier mobility (200000 $cm^2V^{-1}s^{-1}$) at room temperature. Therefore, by integrating graphene on SiN, not only tuning

capability will be added to SiN-based devices, but performance of conventional Si-based integrated photonics devices could be surpassed in terms of, for example, modulation speed at much less power consumption. In this new class of modulators based on hybrid graphene-SiN material platform, we take advantage of the high carrier mobility and the strong plasma dispersion effect of graphene combined with high light confinement in compact SiN photonic devices to enable switches and modulators with speeds that could potentially exceed 100 Gb/s. This enables us to meet the stringent requirements for next generation processing and communication platforms for higher communication and processing speed and denser on-chip integration. Therefore, the availability of such a material and device technology will have a major impact on next generation computing and communication systems.

Recently, graphene has been integrated on Si waveguide-based structures, and optical modulation has been demonstrated through electro-absorption effect. [9] Since these structures are waveguide-based, the footprint of the final modulator is large. There has also been reports of graphene integrated onto photonic crystal cavities, which are electrochemically tuned through ion gels. However, due to the low-speed nature of ion gels, they have not been able to demonstrate high speed modulation. Basically, smaller footprint photonic devices such as microring resonators with fast electrostatic gating scheme could result in higher speeds and denser integration.

The proposed graphene-SiN modulator in this work is electronically a simple graphene-based parallel-plate capacitor placed on top of SiN optical devices; therefore, under ideal circumstances, no current flows in DC, and the devices are ultra-low power. The phase shift and absorption change in graphene layers are induced through the change in the real and imaginary parts of the conductivity of graphene by applying voltage between the two graphene layers. Light-matter interaction takes place between carriers on the graphene sheet and the optical field inside the SiN devices. The required voltage/power consumption of the modulator is determined by the strength of the electro-optic effect that is used for modulation. Recently a similar modulator based on hybrid graphene-SiN has been published. Here, we use a much simpler fabrication process, and also use novel devices to show modulation on the hybrid graphene-SiN platform.

We proposed to use the strong free-carrier plasma dispersion effect and ultra-high charge mobility in a hybrid material platform formed by integrating two layers of graphene films on SiN to add tuning capability to SiN. The strong free-carrier plasma dispersion effect in graphene enables ultralow-power modulation of the effective refractive index of waveguides and resonators in the proposed material platform. Figure 17 shows the schematic of the proposed hybrid graphene-SiN platform in which two graphene layers are separated by a thin oxide layer to form a capacitor. The device is a microdisk optical resonator with whispering gallery modes. Free carriers can be accumulated on the two sides of this capacitor (by applying voltage) to change the absorption of graphene and index of refraction based on the free-carrier dispersion effect. This index or absorption

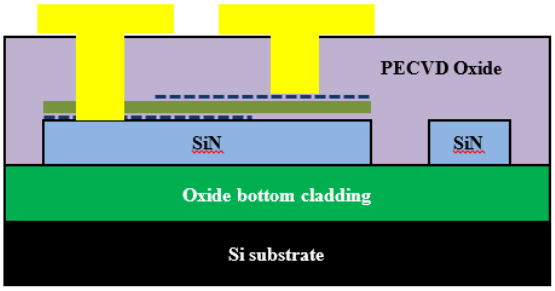

Figure 17. Schematic of the Graphene-SiN hybrid platform.

change results in changing the resonance wavelength or its extinction. Thus, the transmitted optical power through the waveguide is modulated by the application of the voltage.

The main optical devices that is used here to implement the modulation scheme on are microdisk and microring resonators (shown in Figure 18(a) and Figure 18(b), respectively). Microdisk and microring resonators are both subsections of traveling-wave resonators (TWRs). In TWRs optical field travels around the resonator. If the field interferes constructively with itself after one roundtrip, the resonance condition is satisfied and energy is built up inside the resonator. In microdisk resonators the resonant mode "sees" or interacts with only one etched sidewall, and therefore roughness on the sidewalls play a smaller role in the overall Q of the resonators. Such resonators are commonly referred to as "whispering-gallery mode" (WGM) resonators. The WGM effect is present as long as the inner sidewall of the resonator is far enough not to interact with the optical mode. Microring resonators are designed to support only one mode, and that resonant mode "sees" or interacts with both etched sidewalls, and therefore roughness on the sidewalls play a bigger role in the overall Q of the resonators. Because of this microring resonators tend to have lower Q's than micrdisk resonators.

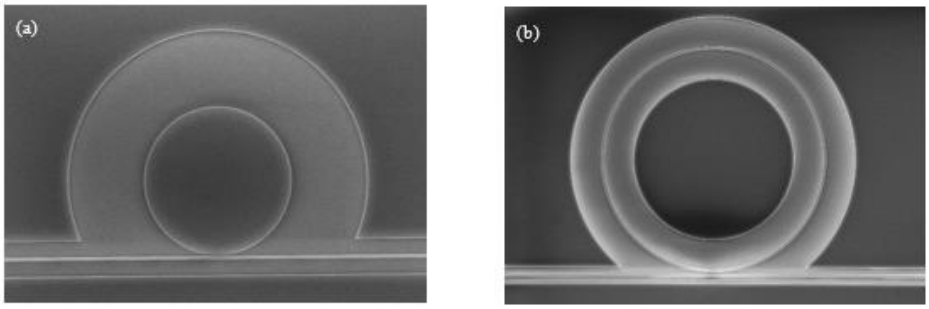

Figure 18. Top view SEM image of (a) microdisk resonator, and (b) a microring resonator.

III.1.1. First Fabrication Trial

Here, we present, in detail, the process for forming double-layer graphene devices on SiN, which is very complicated and requires many fabrication steps. In the double-layer graphene structure, the two graphene layers are separated by a thin oxide layer to form a capacitor in which the application of a voltage between the two graphene layers results in charge accumulation in these layers. When this capacitive structure is integrated with a (passive) SiN or Si resonator, the change in the index of refraction of graphene or its absorption results in a change in the resonance wavelength or extinction. Thus, the transmission through the waveguide can be modulated (or switched on and off) by applying a voltage to the double-layer graphene structure.

Our device fabrication process starts with design, optimization, and fabrication of the underlying passive SiN structure, which in the simplest form includes a waveguide coupled to a microdisk/microring resonator. In this work, the properties of the double-layer graphene structure is considered in designing the passive device and optimized using an in-house code implemented in the COMSOL environment. The most challenging part of the fabrication process was to develop and optimize a reliable transfer process for the two graphene layers. With extensive efforts, this process was optimized, and it can now be used repeatedly with high yield.

III.1.2 Fabrication of Photonic Structures on SiN Substrate

The bottom cladding of my SiN devices is a thick (>3 μm) SiO_2. In order to get minimum scattering from the bottom cladding, we choose high quality thermal oxide. So, the first step of fabrication is to grow thick oxides on prime silicon wafers. This thick oxide layer will prevent the optical modes from leaking into the substrate (silicon). As the dry oxidation rate is very low, the majority of the oxidation process is done via wet oxidation. We either grow the oxide in-house at Georgia Tech cleanroom (at 1100° C for over 30 hours) or purchase Si prime wafers with the thermal oxide already grown on them. The next step would be to deposit high quality stoichiometric LPCVD SiN films on the oxidized wafers. We use LPCVD instead of PECVD to end up with devices with lower optical loss.

As discussed in previously, a 400 nm thick SiN results in high effective index and allows for dense integration of integrated photonics devices. So, 400 nm LPCVD SiN is grown in-house on the oxide wafers at 800° C. We use dichlorosilane (SiH_2Cl_2, or DCS) and ammonia (NH_3) as source gases. The parameters for the stoichiometric LPCVD deposition on a Tystar furnace at Georgia Tech cleanroom are as follows: pressure 165 mTorr, DCS 50 sccm, NH_3 140 sccm, temperature 800° C. This process deposits SiN at a rate of ~4.4 nm/min. After the LPCVD deposition the wafer is cleaved into chips with suitable dimensions before moving on to the next fabrication steps.

After preparing the substrate (SiN on SiO_2) and cleaving it the photonic structures are patterned. We use e-beam lithography (EBL) since the minimum features of my structures are well in the sub-micron region. For the first round of devices, ZEP (ZEP520A by Zeon cooperation) was used as the e-beam resist. ZEP is a positive-tone resist (resist becomes soluble in developer after being exposed to e-beam) and in order to save on EBL write time only the periphery of the devices is written with e-beam to confine light inside the unexposed regions. ZEP is coated on the substrate and it is spun at 1000 rpm (with ramp speed of 500) for 60 seconds, then baked on a hotplate for 2 minutes at 180° C. After the bake step, there is usually around 750 nm ZEP on the sample. After the bake step the resist-covered SiN substrate is patterned using a JEOL JBX-9300FS EBL system. When writing with e-beam on insulating materials such as my current substrate (400 nm SiN on 4μm SiO_2), charge dissipating agents such as ESPACER 300Z (a conducting polymer from Showa Denko K.K.) have to be applied on top of the e-beam resist to avoid pattern deformations and field stitching error due to charge-up effect on the sample. So, after baking ZEP, and before moving on with the EBL process, we spin coat ESPACER 300Z at 2500 rpm (with ramp speed of 2500) for 30 seconds on the sample. ESPACER 300Z is water soluble and will be easily removed right after the EBL step (before developing ZEP) by rinsing it with DI water for just a few seconds. As will be discussed later, for the final round of a devices ZEP was not used as the e-beam resist, and a modified fabrication process based on the alumina hard mask was used.

Next, the pattern is transferred to the SiN layer using reactive ion etching (RIE) in an Oxford RIE system with a CHF_3/O_2 gas mixture. The etching parameters are as follows: pressure 55 mTorr, RF power 175 W, CHF_3 50 sccm, and O_2 5 sccm. The etch rate of SiN and ZEP in this process are around 60 nm/min and 56 nm/min, respectively. So with the selectivity of a little bit over than 1, 400 nm of SiN is easily etched with 750 nm ZEP as mask. Usually a 10-20% extra time is added to the etching step to make sure all the tight openings (for example waveguide-resonator gaps) are fully etched. Integrated photonic devices such are

microdisk and microring resonators with different radii coupled to bus waveguides are fabricated. Input and output grating couplers are used to couple light into and out of bus waveguides. The advantage of using grating couplers is that devices can be optically characterized after each step of fabrication to make sure everything has gone according to plan. Figure 19 shows SEM images of one of the fabricated microdisk resonators, and also SEM of an input grating coupler fabricated on the SiN platform.

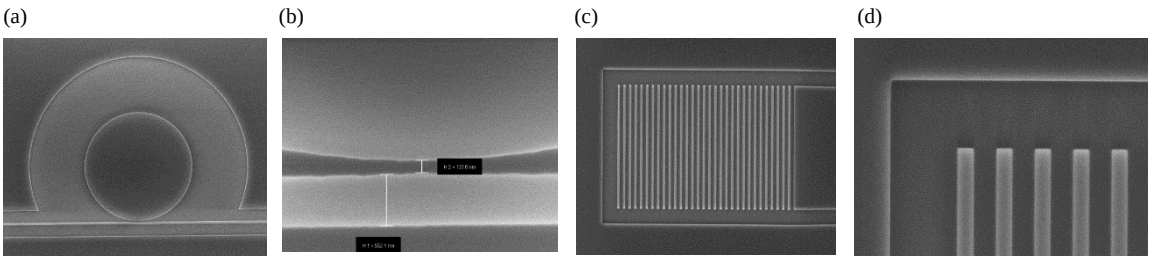

Figure 19 - (a) top-view SEM image of a microdisk resonator fabricated on SiN substrate, (b) zoomed-in SEM image of the gap between the bus waveguide and the microdisk resonator, (c) top-view SEM image of a grating coupler, and (d) zoomed-in SEM of the grating coupler.

III.1.3 Graphene Transfer Process

After discussing the fabrication process of passive SiN devices, here we present the process of transferring graphene to a desired substrate. The graphene we use for my devices is grown using the Chemical Vapor Deposition (CVD) technique on a thin Copper (Cu) film. We do not grow graphene in-house and purchase high quality and mostly single-layer graphene from ACS material. Figure 20 shows an image of a typical single-layer graphene on Copper foil purchased from ACS material.

Figure 20. CVD-grown graphene on Copper foil purchased from ACS material

Depending on the size of the chip onto which we want to transfer graphene, we cut the graphene-on-Copper foil into appropriate pieces using sharp razor blades or scissors. We then follow a similar wet transfer process as discussed in. If not performed carefully, the graphene transfer process will not be very successful. Figure 21 shows the SEM from a sample after unsuccessful graphene transfer. As we can see, the graphene is torn in different places. This is not acceptable for my application. Therefore, we had to carefully optimize the transfer process through several test steps. After cutting graphene/Cu into an appropriate size, we need to get rid of the Copper and etch it away before transferring graphene on the SiN substrate. To do so, we first need to cover the graphene with a protective layer that is hydrophobic to avoid graphene from sinking in the Copper etching solution after the Copper is completely gone. We use PMMA for this task, and it is spun on the graphene/Cu foil. PMMA will provide mechanical support

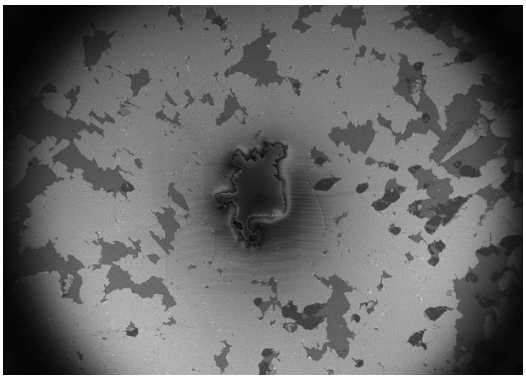

Figure 21. SEM of a sample with failed graphene transfer process.

for the graphene layer after the Cu is etched away. As we mentioned earlier, the Cu foil is very thin; therefore, we need to tape the foil down to a clean glass slide to help with the spin coating process. So, we first place graphene/Cu foil between two clean glass slides and press the slides together to completely flatten out the foil. Then, we tape the foil down on a clean glass slide using Kapton tape on the sides. Using the flat head of a tweezer, we press the tape hard to prevent PMMA going under the gap between graphene/Cu and the glass slide. We then take the sample and spin coat A6 PMMA (from Microchem) on it to get a ~500 nm thick film. We leave the sample for several hours (or overnight) for the PMMA solvent (here anisole) to evaporate.

During the CVD process, graphene is grown on both sides of the Cu film. But, we only need graphene on one side; therefore, we need to remove graphene from the back side of the foil. After the PMMA is dried out, we carefully remove the tape from the sides of the PMMA/graphene/Cu to avoid causing any wrinkles to the film. We then flip it over and put it on a clean glass slide and press it down with another clean slide to make it flat, tape the sides with Kapton tape once more and etch the graphene on the backside using O_2 plasma in an RIE etching machine. The tapes need to be fully pressed over the sides of the graphene to avoid exposing the PMMA-covered side to O_2 plasma.

The PMMA/graphene/Cu is now ready to be transferred to a wet etching solution to remove the Cu. Several different etchants can be used to remove Cu. Here we use Copper Sulfate. The solution is made by adding DI water and HCl to $CuSO_4$ crystals. After preparing the etching solution we remove the Kapton tape from the sides of the film and place it in the etching bath (Copper side down). Due to the hydrophobic nature of PMMA, the sample floats on top of the solution, and Cu gets etched away. After more than 5 hours that Cu is completely etched, we carefully transfer the sample from the etching solution into DI water and change the DI water several times to remove any Cu or acid residues. We use a concave watch glass for transferring graphene from the acid bath to DI water baths, so that the liquid puddle that forms inside the watch glass protects the PMMA/graphene layer from damage during each transfer. Before the Cu is etched, it provides mechanical support for the PMMA/graphene layer. But after it is etched away the thin PMMA/graphene film needs to be handled/carried very carefully from one solution to the other to avoid any tears in the film.

After several steps of DI water cleaning the PMMA/graphene film is ready to be transferred to the desired substrate/chip. As the film floats on the DI water we immerse the chip in the DI water and fish the PMMA/graphene out, and let the DI water to dry out for several minutes. We then place the chip on a hotplate to anneal the PMMA/graphene to get rid of any wrinkles on the sample and enhance the adhesion between graphene and the SiN substrate. We increase the hotplate temperature from 40º C to 220 ºC at the rate of 10º C per minute. Then, leave it at 220 ºC for 5 minutes. Then, remove the substrate from the hotplate and allow it to cool down for several minutes.

The next step would be to get rid of the PMMA as we no longer need it. People usually immerse the sample in an Acetone bath for a few hours to remove the PMMA. However, the wet removal of PMMA in Acetone is not very safe, and we noticed that on several samples the graphene layer gets badly torn after this step. Figure 22 shows the SEM of a microring resonator with graphene transferred on it. The PMMA on the graphene was removed by keeping the sample inside Acetone for 2 hours. As we can see, the

graphene layer is torn on different parts of the sample. Therefore, we modified the process and used Acetone vapor instead to remove PMMA. Basically, the sample is fixed right above the surface of Acetone. The beaker holding the Acetone is placed on a hotplate at 90º C to increase the rate of evaporation of Acetone. PMMA gets removed from the top surface in a couple of hours, and only graphene is left on the sample. This method (vapor Acetone for PMMA removal) has proved to yield excellent results with minimal damage to graphene.

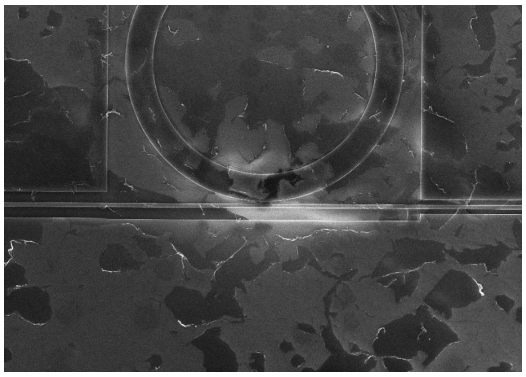

Figure 22. Failed graphene transfer process on SiN a microring resonator. Sample failed due to the damage to the graphene layer during PMMA removal in Acetone bath.

III.1.4 Transferring Bottom-layer Graphene on Photonic Structures

Now that we became familiar with the graphene transfer process in general, we move on to the discussion of successful transfer of graphene on SiN integrated photonic structures. After fabricating passive devices on SiN, we need to transfer the first layer of graphene (bottom-layer-graphene) on top of the chip. This graphene layer serves as the bottom plate of the capacitor to be formed on top of the devices. In transferring graphene on silicon-on-insulator (SOI) substrates, it is required to first deposit a dielectric layer on top of the Si (i.e., between Si and graphene) to avoid current flowing from graphene to Si layer, whereby shorting the capacitor. This extra step is not required for SiN-based structures due to the insulating nature of SiN. Thus, in my process, the bottom layer graphene layer can be transferred directly on top of the SiN layer. This transfer is performed using the process discussed in the previous section. Figure 23 shows a top view SEM image of the bottom-layer graphene transferred on a SiN microdisk resonator. As discussed before, the thickness of the SiN layer in this work is 400 nm, which is needed for designing high-Q devices.

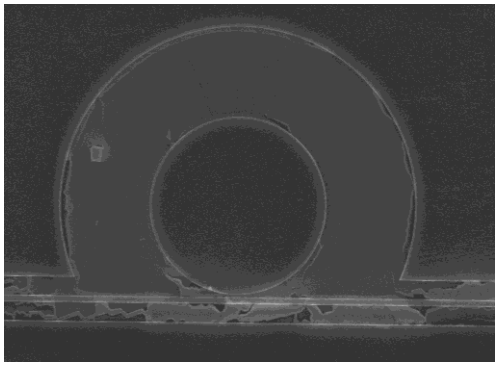

Figure 23. Top view SEM image of the bottom-layer-graphene transferred on a SiN microdisk resonator.

As we can see from the SEM image, the graphene layer completely covers the microdisk and is almost a perfect intact film on top of it. However, as it meets the 400 nm height difference around the periphery of the resonator it cannot withstand the tension caused by this height difference and starts to tear. Fortunately, most of these tears do not cause major issues in the performance of the optical devices, as we mainly need graphene to cover (and be attached to) the microresonator. We actually need to remove the graphene from other parts of the structure including the access waveguides in the following steps. Therefore, as long as the transferred graphene covers the top of the microresonator, the transfer process is considered successful.

Figure 24 shows the result of Raman spectroscopy on the transferred film. The G band appears at approximately 1583 cm^{-1}, and the 2D band is located at approximately 2680 cm^{-1}. The 2D band can be used to determine the number of layers of graphene. This is because in the multi-layer graphene, the shape of 2D band is different from that in the single-layer graphene. As shown in Figure 24, the higher intensity of 2D band as compared to G band proves that the transferred layer of graphene is a high quality single-layer film.

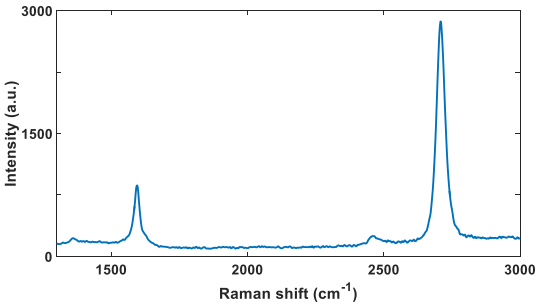

Figure 24. Raman shift of the transferred graphene.

III.1.5 Patterning the Bottom-layer Graphene Over the Optical Devices

After successful transfer of the bottom-layer-graphene on the passive SiN devices, we need to pattern and remove graphene from unwanted areas, both to minimize optical loss caused by graphene and also to avoid short circuiting the bottom and top plates of the capacitor to be formed on the devices. We use the combination of EBL and dry-etching using O_2 plasma to pattern the graphene. The e-beam resist that we use should have some properties including, being easily removable from the substrate after the EBL/etching process without causing tears/damages to the graphene layer. The resist's corresponding solvent should also be compatible with the SiN/SiO_2 substrate so that it does not damage/etch the passive structures already fabricated on the substrate. This is why we selected PMMA as the e-beam resist to pattern graphene. PMMA is the same polymer that was previously used in the graphene transfer process, so there is no compatibility concerns. Therefore, if processed carefully, PMMA does not cause extra damage to the graphene layer.

After successful transfer of graphene on the chip, the patterning step is as follows. We first spin coat A6 PMMA from Microchem on the chip at 3000 rpm (speed ramp of 1500) for 60 seconds. Then bake it at 180º C to remove the excess solvent for 90 seconds. After baking we spin coat ESPACER 300Z at 2500 rpm (ramp speed of 2500) for 30 seconds on the sample to help avoid charge-up issues. We then load the chip in the EBL system and write the desired pattern on the sample. It should be noted that PMMA is a positive-tone e-beam resist meaning that the exposed areas will dissolve in the developer and the unexposed areas remain on the chip. So, In order to remove graphene from the undesired areas on the chip (e.g., access waveguides and the bottom of the trenches around the devices) and also pattern the graphene layer as the bottom plate of the capacitor on top of the photonic structures, we should expose these areas to the e-beam. After the EBL process, we develop the sample in a 1:1 solution of MIBK:IPA for 2 minutes to remove PMMA from the e-beam exposed areas. Now that PMMA is patterned on the sample, we use a mild O_2 plasma in an RIE system to etch/burn away graphene from the exposed areas on the sample. PMMA is easily removed in O_2 plasma, so the power and the duration of the O_2 plasma has to be short enough not to consume the whole PMMA film that is protecting the parts of the sample. After the O_2 RIE etching process, we remove the PMMA (resist) from the unexposed areas using Acetone. Here again we use Acetone vapor instead of immersing the sample in Acetone bath to avoid damaging the graphene in the liquid. Vapor Acetone dries out without leaving any residues on the sample, and there is no need to

use N_2 blow gun to facilitate the drying, as it may cause damage to the graphene layer. Figure 25 shows a top view SEM image of the bottom-layer-graphene (i.e. bottom capacitor plate) on a SiN microdisk resonator after being patterned using PMMA. As we can see, the graphene is successfully removed from the access waveguide, the bottom of the trenches around the microdisk resonator, and some parts of the microdisk resonator without being torn or damaged where it is supposed to stay.

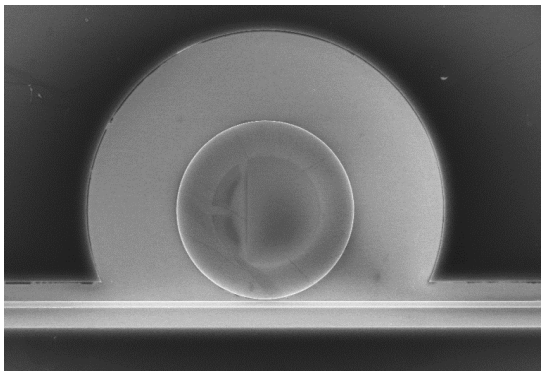

Figure 25 - Top view SEM image of the bottom-layer-graphene on a SiN microdisk resonator after being patterned using EBL and dry etching in O2 plasma.

III.1.6 Making Metal Contact to the Bottom-layer Graphene

After successfully removing graphene from unwanted areas and patterning the graphene layer on top of the passive SiN devices, we proceed to add the metal contact on the bottom-layer graphene to serve as the contact to the bottom plate of the capacitor. The contact should be placed away from the outer-radius, either well inside the resonator or outside of it. The reason behind this is that, as seen in Figure 26, the optical field of the fundamental TE mode (i.e., electric field in the place of the resonator) in a typical microdisk resonator resides close to the periphery (i.e., outer-radius) of the microdisk. Due to the high optical loss of metals, placing the metallic contact where the optical field is strong (i.e., close to the outer-radius) considerably reduces the Q of the microresonator.

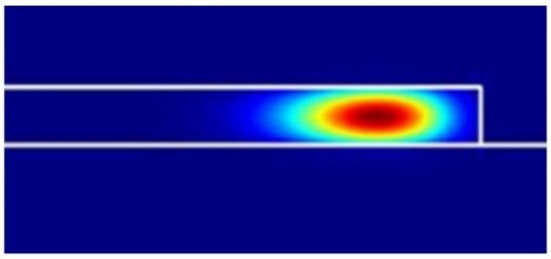

Figure 26. Cross-sectional profile of the Poynting vector for the fundamental TE mode in a typical microdisk resonator.

In addition to the optical loss, we need to consider the contact resistance of the metallic contact to graphene. This seriously affects the modulation speed. Other than the location and the shape of the contact, the choice of metal is an important factor in achieving low contact resistance with graphene. Using all these criteria, we optimized the location, the shape, and the material of the metallic contact to the bottom-layer graphene.

Here we use Ti/Pd/Au 1.5/45/15 nm as the contact to graphene. We use the combination of EBL, e-beam metal evaporation, and lift-off to form the Ti/Pd/Au contact to the bottom-layer graphene. We again use PMMA as the e-beam resist for the lift-off process due to its compatibility with graphene. We first spin coat A6 PMMA from Microchem on the chip at 3000 rpm (ramp speed of 1500) for 60 seconds. Then bake it at 180º C to remove the excess solvent for 90 seconds. After baking we spin coat ESPACER 300Z at 2500 rpm (with ramp speed of 2500) for 30 seconds on the sample to help avoid charge-up issues. We then load the chip in the EBL system and write my desired pattern on the sample. After the EBL process, we develop the sample in a 1:1 solution of MIBK:IPA for two minutes to remove PMMA from the e-beam exposed areas. Now that PMMA is patterned on the sample we load the sample in an e-beam metal evaporator and pump down the chamber to the low 10e-6 Torr range before evaporating 1.5 nm Ti, 45

nm Pd, and 15 nm Au, successively. After the evaporation process, we perform the metal lift-off process as follows. We leave the sample in Acetone for two hours. Then, after most of the large metal pieces have been removed from the sample, we place it in a second (fresh) container of Acetone. This helps to keep floating metal pieces from redepositing onto the sample. We keep the sample immersed in Acetone for another 30 minutes. In the next step, we place the sample in IPA and change the IPA solution a couple of times to completely remove any Acetone left in the solution. We then take the sample out of the IPA solution and leave it to dry by itself under a fume hood. Figure 27 shows a top view SEM image of the bottom-layer graphene on a SiN microresonator with metal contact. As we can see from the figure, the contact is well inside the microdisk and completely away from its periphery (where the optical modes reside). At this stage the bottom plate of the capacitor is completely formed, and we move on to the next step, i.e., depositing the capacitor dielectric before transferring the second (top-layer) graphene.

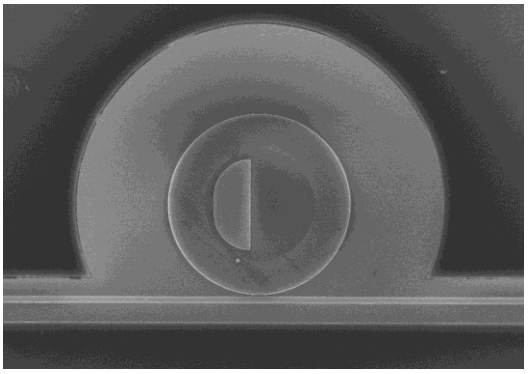

Figure 26. Cross-sectional profile of the Poynting vector for the fundamental TE mode in a typical microdisk resonator.

III.1.7 Depositing Alumina on Graphene

The material we choose as the capacitor dielectric is alumina (Al_2O_3). It is a high-k dielectric material which enables higher charge accumulation in the (graphene) capacitor plates (i.e., more shift in the resonance of the devices). Alumina can be deposited via atomic layer deposition (ALD), which produces conformal, pinhole-free films with atomic level control over the thickness of the film. ALD films are grown on a substrate by exposing its surface to alternate gaseous precursors. For the case of alumina deposition, we use Trimethylaluminum (TMA) and water as the alternating precursors at 250º C.

Unfortunately, ALD of alumina (or other thin films for that matter) on pristine graphene is not trivial, because there are no dangling bonds on the untreated graphene surface, which are needed for chemical reactions with the ALD precursors. As shown in Figure 28, performing 90 ALD cycles of alumina on pristine graphene results in disconnected islands of alumina instead of a uniform film. The alumina film has in fact preferentially formed on graphene edges and defect sites.

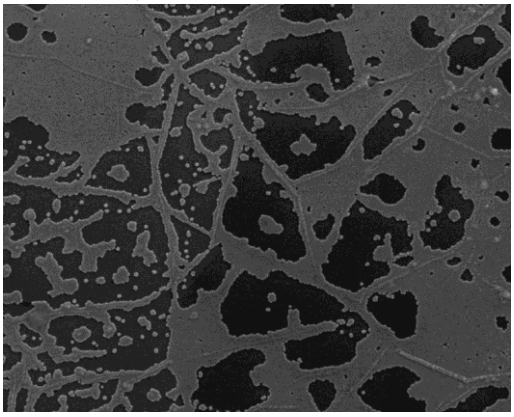

Figure 28. Top view SEM image of a graphene layer after 90 cycles of alumina ALD performed on it without any pretreatment.

The solution to improve the uniformity of the ALD of alumina on graphene is to evaporate a very thin seed layer (~1 nm) of Aluminum (Al) on pristine graphene before performing ALD on it. The Al seed layer will oxidize before the ALD process starts and becomes alumina, which will help increase the uniformity of the

final film (alumina seed layer plus the ALD alumina). Figure 29 shows the SEM image of the sample formed by 90 ALD cycles of alumina on graphene after functionalizing the graphene layer with ~1 nm Al as the seed layer. The dramatic improvement in the quality of the deposited alumina as compared to the case of the ALD growth with no seed layer (Figure 28) is evident from Figure 29.

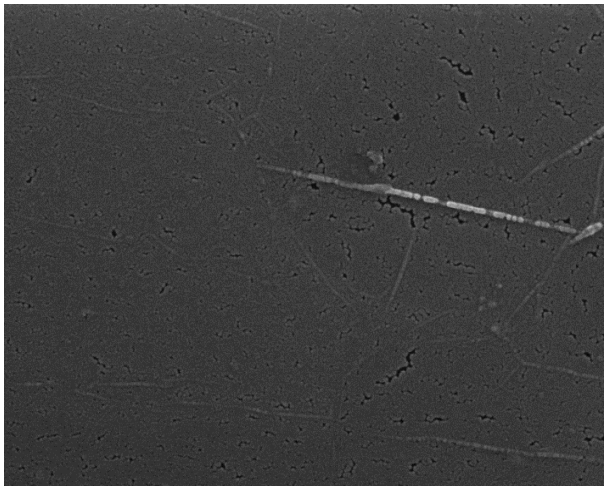

Figure 29. Top view SEM image of a graphene layer after 90 cycles of alumina ALD performed on it (with a ~1 nm Aluminum seed layer).

So, back to the fabrication steps of the graphene-SiN sample. After successful metallization and lift-off on the bottom-layer graphene, the graphene-coated sample is placed inside the metal evaporator chamber. The chamber is then pumped down to the low 10e-6 Torr range, and then 1 nm Al is evaporated on it at the rate of 0.1 Angstroms per second. The final thickness is confirmed with ellipsometry measurement. The sample is then taken to the ALD chamber, and about 14 nm of alumina is coated on it via alternating pulses of water and TMA. Figure 30(a) and Figure 30(b) (higher magnification) show the SEM images of the sample after alumina deposition. The final result is a uniform pinhole-free alumina film grown on bottom-layer graphene (this is evident from Figure 30(b)).

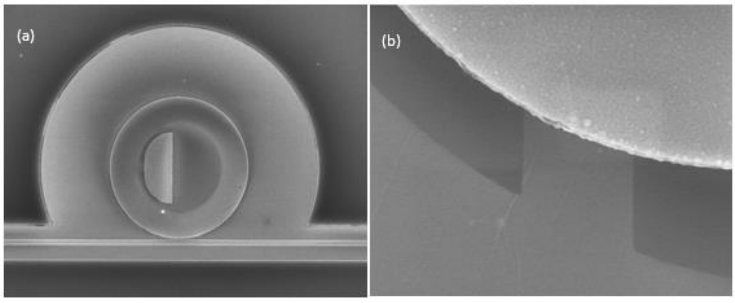

Figure 30. Top view SEM image of a graphene layer after 90 cycles of alumina ALD performed on it (with a ~1 nm Aluminum seed layer).

III.1.8 Transfer of Top-layer Graphene on Optical Devices

After successful deposition of the dielectric material, we proceed to transfer the second layer of graphene (top-layer graphene) on top of the alumina layer using the process described earlier. This graphene layer will serve as the top plate of the capacitor on top of the device. Figure 31 shows the top-view SEM image of the top-layer graphene layer transferred on the alumina layer. As we can see in the figure, the top graphene layer completely covers the microresonator area and is almost a perfect intact film on top of it. As discussed earlier, the tears on the graphene at the periphery of the microdisk resonator do not cause any problems; and the transfer process is considered successful as long

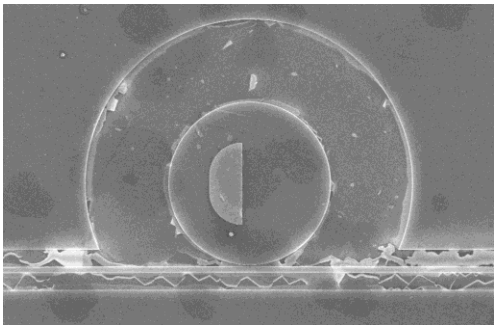

Figure 31 - Top view SEM image of the top-layer-graphene transferred on a SiN microdisk resonator.

as the transferred graphene remains a high-quality layer on top of the optical devices.

III.1.9 Patterning the Top-layer Graphene Over the Optical Devices

After successful transfer of the top-layer graphene, we need to pattern and remove graphene from unwanted areas using a similar process composed of EBL and O_2 dry-etching as explained for case of the bottom-layer graphene. After the RIE etching process, we remove the PMMA from the unexposed areas using vapor Acetone. Figure 32 shows the top-view SEM image of the top-layer graphene (i.e., the top capacitor plate) on a SiN microresonator after being patterned using PMMA. Figure 32 clearly shows that graphene is successfully removed from the access waveguide, the bottom of the trench around the microdisk resonator, and some inner parts of the microresonator.

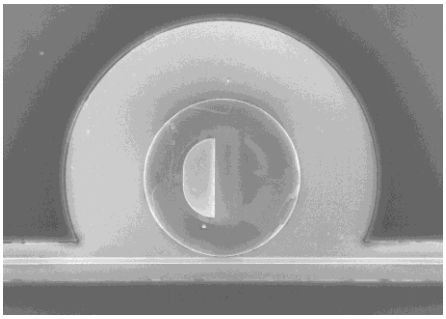

Figure 32. Top view SEM image of the top-layer-graphene on a SiN microdisk resonator after being patterned using PMMA and O2 plasma.

III.1.10 Making Metal Contact to the Top-layer Graphene

To complete the fabrication of the double-layer capacitive graphene structure, we must add the metal contact to the top-layer graphene. Here we use a similar process to the one in case of the bottom-layer graphene (i.e., using the combination of EBL, e-beam metal evaporation, and lift-off) to form the Ti/Pd/Au contact to the top-layer graphene. Figure 33 shows the top-view SEM image of the top-layer graphene on the SiN microdisk resonator with the Ti/Pd/Au metal contact. At this stage, the capacitor is completely formed.

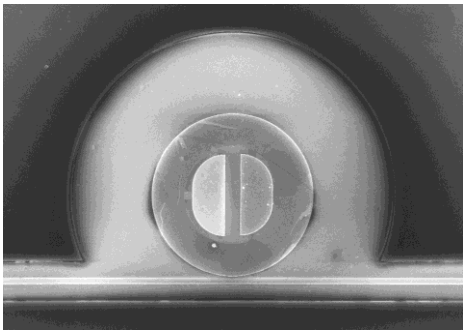

Figure 33. Top view SEM image of the top-layer-graphene on a SiN microdisk resonator with metal contact made to the top-layer-graphene.

III.1.11 Depositing Protective Alumina Layer on Top of Top-layer Graphene

The final fabrication step after forming the double-layer graphene capacitor on top of the SiN microdisk resonator is to deposit another layer of ALD alumina to protect the top-layer graphene from the next fabrication steps on the device. Similar to the case of ALD deposition on the bottom-layer graphene, we first grow a ~1 nm Al seed layer before growing ~14 nm alumina in an ALD chamber. Figure 34 shows the SEM of the sample after top alumina deposition with different magnifications. It is clear from Figure 34 that the final result of my process is a uniform pinhole-free alumina film grown on the top-layer graphene.

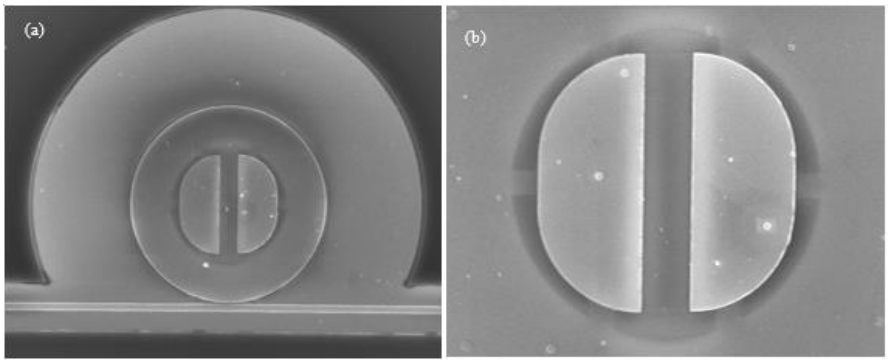

Figure 34. (a) Top view SEM image of the bottom-layer graphene on a SiN microdisk resonator after ALD of alumina; (b) same as (a) at higher magnification

III.1.12 Growing Buffer Oxide on the SiN Devices

Up to now, we showed different steps required to fabricate a double-layer SiN graphene modulator all the way from growing high quality SiN film in a low-pressure chemical vapor deposition (LPCVD) chamber on oxide wafers to transferring two layers of graphene and patterning them and depositing low-resistance metal contacts. After these steps, major fabrication steps of the modulator are basically complete. However, limitations in characterization equipment force me to add one final step. The contacts that are made in the middle of the microresonators are only 2-3 μm in size and only 2-3 μm apart. On the other hand, standard characterization probes are much larger than these contacts. Thus, we need to form much larger pads (on the order of 100 μm by 100 μm) on these smaller contacts to be able to electrically characterize the device. On the other hand, as discussed previously, the high optical absorption coefficient (or optical loss) of metals prevents me to use large pads directly on top of the microresonators (on the same surface as the microresonators). This is why we have to deposit around 2 μm of buffer insulator (PECVD SiO_2) on top of the chip, then, make via openings on top of the contacts by etching back the insulator, and filling the vias up with metals to form the necessary large pads on top of the device for characterization purposes.

Unfortunately, as shown in Figure 35(a) and Figure 35(b), after depositing the 2 μm buffer oxide on top of the chip, poor adhesion of graphene to the substrate in the periphery of the optical devices, and the stress of the thick buffer oxide film caused the buffer oxide to delaminate from the bulk of the chip. However, the oxide directly on top of devices is intact. This has caused a 2 μm bump of oxide on the devices with no oxide covering the rest of the chip. The areas with darker green color are the areas where the buffer oxide is not delaminated. Due to this 2 μm height difference no further processing (e.g., e-beam resists spin coating and e-beam lithography) can be done on this chip. So, basically, this fabrication approach failed; therefore we tried other approaches.

So, how to avoid sample failure for the next round? We need graphene only on top of the resonators and some of the waveguides, i.e., an area a few percent of the whole area of the chip. So a question might be raised why we kept this much graphene in the unwanted areas on the chip in the first place. Well, to answer this we should first review the process that we use to pattern and remove graphene from unwanted areas.

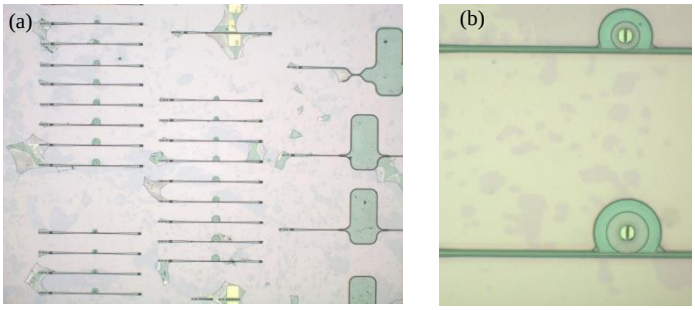

Figure 35. Optical image of the chip after the buffer oxide delamination from the top of it at (a) low magnification, and (b) high magnification.

As discussed previously, we work with PMMA to pattern the graphene and etch it away using O_2 plasma. Since PMMA is a positive-tone resist, areas of graphene that are supposed to be etched away need to be directly exposed with e-beam. So, if we want to remove graphene from all over the chip except on the active regions, it would take very long which is not reasonable. This is why we had chosen to only remove graphene from the areas that had to be removed and left the rest untouched. So why not use a negative-tone resist so that only the wanted areas are exposed, and basically reduce the exposed area to a few percentage of the chip size? Unfortunately, neither of the conventional negative tone e-beam resists are compatible with my structure. HSQ (negative-tone e-beam resist) needs BOE wet etching after O_2 etching process to remove its residues, and BOE will damage the substrate of the chip. On the other hand, for the case of Ma-N (another negative-tone e-beam resist), my experiments showed that graphene tends to stick to Ma-N better than to the substrate which causes poor adhesion to the surface of the chip after removing Ma-N. Since, changing the e-beam resist did not seem to be a viable option, we devised three other approaches to get around the buffer oxide delamination issue. We explain these approaches in the next sections. One of the approaches is based on removing the unwanted graphene using PMMA exposed with Deep UV or higher e-beam currents. The second one is based on wafer bonding approach. The third one is based on planarizing the chip after etching SiN devices to avoid having to deposit thick PECVD buffer oxide followed by making via openings.

III.2 Other Fabrication Trials

III.2.1 Exposing PMMA with Deep UV or Higher E-beam Current

Well, as we discussed in the previous section, it was basically the unwanted graphene in the periphery of the devices that caused the failure. If we remember, the buffer oxide directly on top of the optical devices (where the graphene was partially etched) did not delaminate. This suggests that if we etch some lines in the graphene layer on the periphery of the devices, the buffer oxide will have several direct connections to the bottom substrate whereby increasing its adhesion, to hopefully resist delamination from the chip. This will only add a few more percent of writable area and only incrementally increase the e-beam exposure time. Figure 36(a) shows the AutoCAD drawing of some part of the pattern that will be used to expose the new sample. The red areas are critical areas on top of the active devices. The white lines are the new added patterns that are supposed to make openings in the unwanted areas of graphene so that the buffer oxide (that will be deposited in the following steps) will have direct contact to the substrate to improve its adhesion. Well, a new SiN chip was etched, the bottom-layer graphene was transferred and

exposed using the new pattern (with the adhesion promoting lines added), followed by O_2 plasma etching. The bottom-layer contacts were lifted-off. Then, the dielectric layer was deposited using the combination of Al seed layer evaporation and alumina deposition in an ALD chamber. Then, the top-layer graphene was transferred and exposed using the new pattern (with the adhesion promoting lines added), followed by O_2 plasma etching. The top-layer contacts were then lifted-off. Then, the protective alumina layer was deposited using the combination of Al seed layer evaporation and alumina deposition in an ALD chamber. Then, 2 µm PECVD buffer oxide was deposited on the chip. The new etched lines in graphene layers did in fact improve the adhesion of buffer oxide to the substrate, and it did not delaminate during the PECVD deposition step. So, we continued with making via holes in the buffer oxide to access the metal contact in the center of microdisks. Chromium etch mask was deposited on the sample with Ma-N used as the lift-off resist. Unfortunately, after Cr evaporation and when the sample was in Acetone bath to lift-off the exposed parts, the underlying buffer oxide delaminated again (Figure 36(b)). This shows that, although the adhesion of buffer oxide to the substrate had increased due to the new etched lines in graphene layer, the adhesion was still not strong enough.

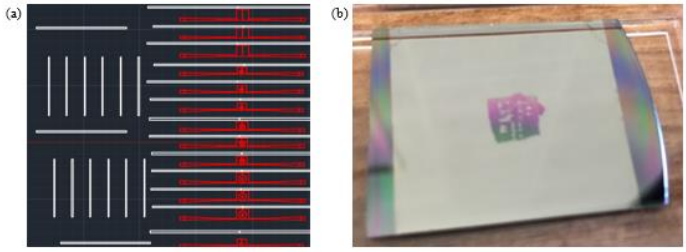

Figure 36 - (a) Snapshot of the new Autocad pattern with added lines to increase adhesion of buffer PECVD oxide. (b) Failed sample after buffer oxide being delaminated from underneath Cr etch mask.

So, we conclude that in order to avoid delamination of buffer oxide from the chip, we need to remove the majority (if not all) of it from the unwanted areas. To fix this issue on the next sample we should try to keep graphene only on the active parts and remove it from unwanted areas. Removing this poorly attached film from bulk of the chip will avoid delamination of the buffer oxide. As we discussed in the previous section, exposing the PMMA from the whole unwanted area on the chip using PMMA at the standard e-beam current (2 nA) takes very long (on the order of days) which is unreasonable. How about only exposing the critical areas (regions with sub-micron dimension on or around microresonators) at the standard (2 nA) current, then changing the current to 20 nA and exposing the less critical areas (which do not need high resolution exposure). This will considerably reduce the e-beam exposure time from close to four days to only several hours.

But, there is another approach to remove graphene from all over the unwanted areas that takes shorter than high current exposure. Other than e-beam, PMMA is also sensitive to deep ultraviolet (UV) spectrum. So, we can first pattern the critical areas (regions with sub-micron dimension on or around microresonators) using PMMA and e-beam lithography, then, without developing or removing the PMMA re-expose the unwanted areas using deep UV lithography. Finally, develop the doubly-exposed (first e-beam then deep UV) PMMA only once and get rid of PMMA from everywhere except only on active devices. Figure 37 shows the AutoCAD patterns of the etching pattern of one of the resonators. In Figure 37(a) the red areas show the areas that will be exposed with e-beam. Figure 37(b) shows a cropped circle,

everything around this cropped circle will be exposed with deep UV, and only the areas inside the cropped circle will be protected. By combining these two patterns for each device we can keep graphene only on the necessary areas and completely remove it from unwanted areas whereby avoiding poor adhesion between buffer oxide and substrate to prevent delamination and failure.

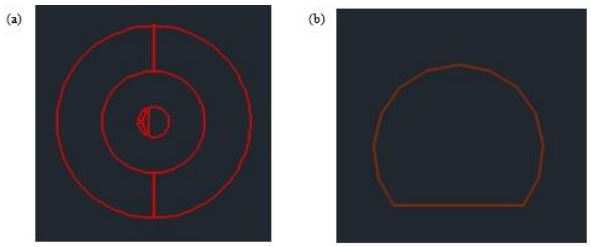

Figure 37 - Snapshot of the Autocad pattern for a microresonator. Part (a) is the pattern that will be exposed in E-beam. Part (b) is the pattern that will be exposed with deep UV lithography.

Before working on this sample we had to optimize the process to expose PMMA with deep UV and develop it afterwards. According to Microchem, PMMA needs dosage of more than 500 mJ/cm^2 in deep UV (248 nm) so that the exposed parts can be dissolved in developer (MIBK:IPA 1:1). However, it was only at dosages above 20000 mJ/cm^2 that we was able to remove the exposed PMMA in developer. This significant difference could be due to the fact that maybe the intensity reader that we use to measure the deep UV intensity is not calibrated, or maybe the optical mask we use is not made with high quality Quartz and in effect has absorption in deep UV. Anyways, we was able to develop and optimize a deep UV process to remove PMMA from the bulk of the sample. The only issue with this process is that after development some few nanometer PMMA residue is left on the sample. However, this is not a big issue for us, as the next step after PMMA development would be O_2 plasma etching of graphene. Basically, the first few seconds of the Oxygen plasma process will get rid of the PMMA residues and then the uncovered graphene will be etched away.

So, with the inclusion of deep UV lithography the process would be modified as follows. After transferring each layer of graphene, we spin coat PMMA on it. We then expose the critical areas (regions with sub-micron dimension on or around microresonators) using e-beam lithography. Then we unload the chip and re-expose the unwanted areas using deep UV lithography, while the areas that were exposed in e-beam lithography are protected/covered using the optical mask. After the second exposure, the chip is developed in MIBK:IPA 1:1 for 2 minutes, followed by O_2 plasma to etch away the uncovered areas.

III.2.2 Inverted Geometry Using Wafer Bonding to Planarize

In the approach that we explain in this section, we will try to use a new device geometry (inverted compared to the initial technique) to avoid having to deposit buffer PECVD oxide and make via openings on it. In this inverted geometry technique, we deposit LPCVD SiN directly on Si (not SiO_2). Then pattern and etch the SiN layer and form optical devices on it. At this stage, the etched devices cannot be optically characterized, because underneath SiN, we have Si which has a higher refractive index than SiN and light will not be confined in the devices fabricated in the SiN film. But there is no need to worry as we will later remove the underlying Si layer and it will only work as a handle/sacrificial layer. As shown in Figure 38(a), the idea is that after etching the optical devices we spin coat flowable oxide (FOx-25) on the wafer and anneal it. Then deposit a couple of microns PECVD oxide on top of it. Then bond an oxide wafer to this

wafer. Later on, we will flip the structure and get rid of the Si handle layer. As seen in Figure 38(b), after removing the Si handle layer from the first wafer, the top surface of the wafer is now planarized and there are no more steps that could tear the graphene layers. So, basically, there is no longer any need to deposit PECVD buffer oxide and making via openings on it. Graphene layers can be easily transferred on the chip and contacts can be made to them. We started making devices using this approach. We deposited 400 nm LPCVD SiN on a Si wafer. Then, etched desired devices on the SiN film. Then we spun FOx-25 on the sample and annealed it, followed by depositing 2 µm PECVD oxide. We then bonded this chip to an oxide wafer using wafer bonding technique. After successful bonding, we flipped the chips and started etching the Si handle wafer using Bosch process. Unfortunately, after the handle layer was thinned down to tens of micron, different layers delaminated from the chip (Figure 38(c)). We believe this sample failed due to the internal built up stress between different layers.

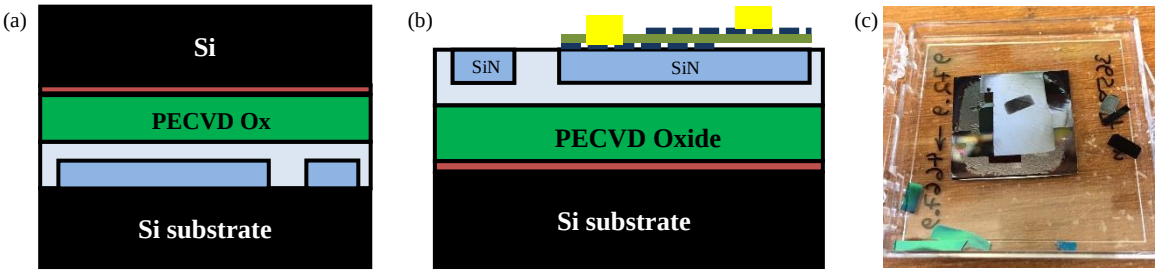

Figure 38 - (a) Schematic showing the concept behind the inverted geometry technique. (b) The final sample after etching the Si handle wafer and transferring graphene and making contacts. (c) Optical image of the bonded chip that failed during back-side etching.

III.3 Final Approach for Fabrication

The final technique that is discussed here is the one that was used for the fabrication of final devices. As shown in Figure 39(a), it is based on avoiding the need for depositing PECVD oxide through planarizing the surface of the chip right after etching the SiN layer using spin-on-glass (here we use FOx-25). By having a planarized surface the graphene layers would be easily transferred onto the surface, and there would be no height difference to cause the graphene layers to tear up at the edges. Therefore, there would not be a need to deposit PECVD buffer oxide and make via openings. However, after spinning a single layer of FOx-25 the surface does not become perfectly flat and planarized. Figure 39(b) shows the SEM of the cross-section of a SiN on Si sample that has been planarized using FOx-25. As we can see there is still some height variations over the waveguides after being partially planarized with FOx-25. Figure 39(c) which is the result of profilometry on the surface (over the waveguides) also confirms this height difference. Basically, after FOx-25 partial planarization, the 400 nm heigth difference is reduced to less than 100 nm. As will be discussed later, using successive steps of FOx-25 spin-coating and etch back, a perfectly planarized surface was achieved.

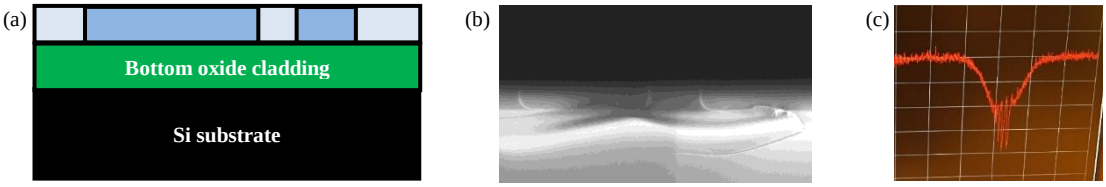

Figure 39- (a) Schematic showing the devices after being planarized with FOx-25. (b) Cross-sectional SEM images of cleaved facet of SiN on Si waveguides after planarization with FOx-25. (c) Snapshot of the result of profilometry on the surface (over the waveguides).

III.3.1 Fox Planarization

In this section, we will discuss the different steps for fabrication of planarized SiN integrated photonic structures using flowable oxide (FOx-25) to enable transfer of graphene layers without tearing up over the steps of the SiN chip. So, as discussed earlier, the thickness of the SiN film in this work is 400 nm. After etching the SiN layer the step height would be at least 450 nm (with some oxide over-etch included in the SiN etching step). The maximum FOx-25 thickness that we can safely spin coat on the sample is around 1 µm which is achieved at a spin speed of 1000 rpm. The reason behind this is that thicker FOx films tend to crack starting from the edges of the chip (Figure 40(a)), or anywhere there are particles on the sample which allow for cracks to originate (Figure 40(b)). We tried spinning a second 1 µm thick FOx-25 on the first layer (after it had already been baked on hotplate). It did not help with crack formation, and the final film (after the second spin coating) cracked as well. So, multiple FOx spin coating and etc-back steps are required to achieve a flat surface.

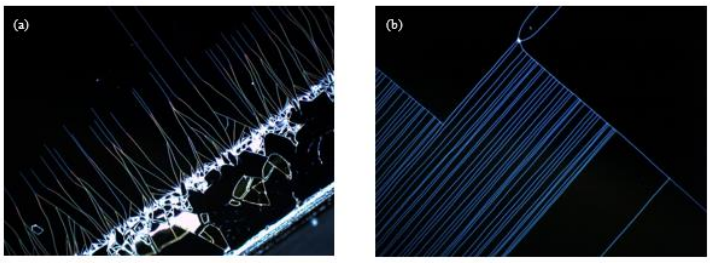

Figure 40 - Dark field optical micrograph of spun FOx with cracks originating from (a) the edges or (b) particles that were on the wafer before spin coating.

So, as discussed earlier, due to the large step height (over 400 nm) on the etched structures, a single step of FOx coating is not enough to completely flatten out the surface, and multiple steps of FOx coating is required. So, every time a 1 µm thick FOx film is spun on the sample, it has to be partially etched back to avoid forming cracks due to excessive stress. In order to protect the passive SiN structures during the etch-back step, he have to protect them with some sort of an etch-stop. Since Fluorine-based plasma is used for the etch-back step, and as discussed previously, we know that alumina has excellent etch resistance in Fluorine based plasma, we use alumina as my etch-stop. So, we could either fabricate my passive structures in SiN, then cover them with alumina as etch-stop. Or using the alumina hard mask process use alumina itself as the mask for etching SiN structures, then use the alumina residue on top of the structures as etch-stop for the planarization step. As will be discussed later, the second approach was chosen. In the following section, we will discuss the details of making the passive SiN structures.

5.3.2 Etching SiN Structures with Alumina as Mask

So, we start with preparing the substrate by growing 4 µm thermal oxide on a prime Si wafer, followed by depositing 400 nm high quality LPCVD stoichiometric SiN on it. Then deposit 50 nm alumina on the wafer using TMA and H_2O as precursors at 250º C in an ALD chamber (Figure 41(a)). About 20 nm of this alumina film will be consumed during etching the SiN passive structures, and the rest will act as etch-stop during the planarization step. Then, 6% HSQ is spun on the wafer at 500 rpm for 60 seconds, and baked at 90º C

for 3 minutes. This low spin speed should give around 250 nm of HSQ after baking which is more than enough to etch the 50 nm alumina hard mask. Instead of HSQ we can also use FOx-25 as the e-beam resist and process it under the same EBL conditions as for HSQ. After baking the HSQ, we spin ESPACER 300Z on the sample to help avoid charge-up issues because my substrate (alumina on SiN on SiO2) is insulating. The sample is then loaded into the EBL system, and is exposed with patterns for passive SiN structures. HSQ is then developed in warm TMAH (40º C) for 30 seconds and rinsed under running DI water for 5 minutes. Patterns on HSQ are then transferred to alumina in a Plasma-Therm ICP system using the recipe which was discussed previously. The process parameters for etching alumina are as follows: coil power 800 W, platen power 150 W, pressure 5 mTorr, BCl3 30 sccm, Cl2 20 sccm. Figure 41(b) shows the schematic of the sample with alumina layer etched using HSQ as mask. The next step would be to use alumina as hard mask and transfer the patterns to SiN in an Oxford RIE system. The process parameters for etching SiN are as follows: RF power 175 W, pressure 55 mTorr, CHF3 50 sccm, O2 5 sccm. Figure 41(c) shows the schematic of the sample with the SiN layer etched using alumina as hard mask. After this etching step around 30 nm of alumina will be left on the sample. Normally, we would remove the alumina hard mask residue from the sample right after etching the SiN layer, however, we keep the alumina residue on this sample because it will serve as etch-stop during the following FOx planarization step.

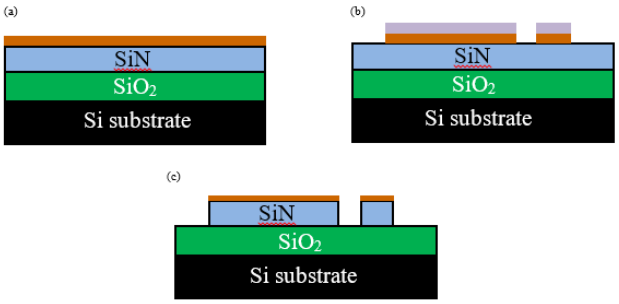

Figure 41. Optical image of the chip after the buffer oxide delamination from the top of it at (a) low magnification, and (b) high magnification.

Figure 42 shows the optical micrograph of the different passive integrated optics structures made on SiN after this step including microring resonators, Mac h-Zehnder interferometers, and coupling modulated rings.

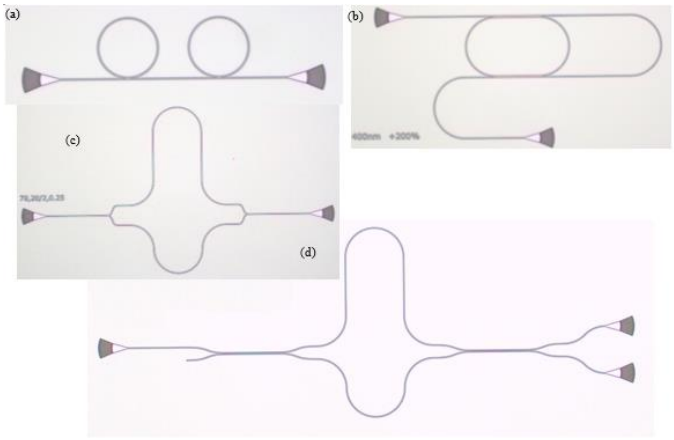

Figure 42. Different passive SiN integrated optics structures fabricated on the substrate before planarization.

III.3.3 Planarizing the Etched SiN Wafer

After successful etching of the passive structures on SiN, we move on to the planarization step. As discussed earlier we use the combination of successive FOx-25 spin coating and etch-back to planarize the sample. We use profilometry to measure the height difference across the sample during different planarization steps.

The first step in the planarization process would be to spin the first FOx-25 layer on the sample. Basically, we spin it at 1000 rpm for 60 seconds then bake it at three different temperatures on hotplate. Starting with 2 minutes at 150º C, followed by 2 minutes at 220º C, and finally 15 minutes at 350º C. Figure 43 shows the result of profilomtery across four waveguides. As we can see from Figure 43(b), the step height after this step is about 50 nm. Although going down from a step height of over 400 nm to 50 nm is a huge improvement, there is still room for improvement through more spin coating steps.

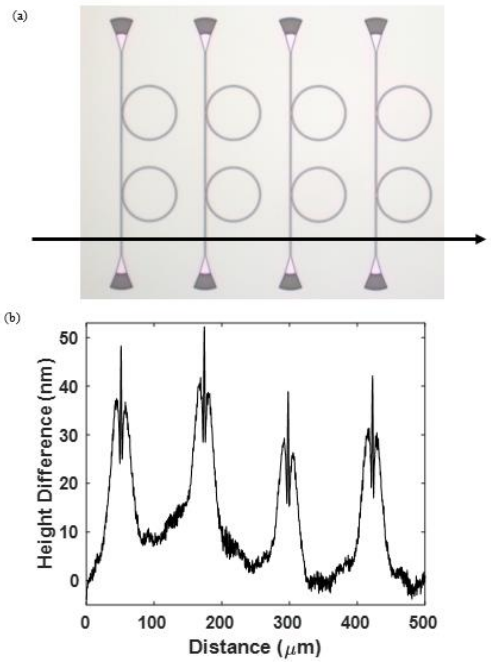

Figure 43. (a) Micrograph of where on the sample profilometry is performed. (b) Result of the profilometry after spin coating the first layer of FOx.

I cannot spin coat a new FOx-25 layer on the sample at this state. Because, as discussed earlier, cracks will generate on the thicker FOx film. To avoid getting cracks on the sample, we need to etch-back some FOx from the top of the sample before spinning a new layer. The residue of alumina on the SiN structures will keep them from getting damaged in plasma during the etch-back step. So, we continue to thin down FOx in an Oxford RIE system using an anisotropic oxide etch recipe as follows: RF power 200 W, pressure 33 mTorr, CHF_3 25 sccm, Ar 25 sccm. We etch 400 nm of FOx from the top of the sample. Before spinning a new FOx layer, we deposit ~100 nm of PECVD SiO2 on the sample to avoid having the second FOx layer directly deposited on top of the previous FOx layer. This will help to avoid crack formation on the sample.

We continue to spin coat a new layer of FOx on top of the PECVD oxide using the same parameters as for the first spin process. Figure 44 shows the result of profilomtery across the same waveguides as for the ones in Figure 43(a). As we can see from the figure, the step height after this step is reduced to less than 20 nm. We could continue with coating another layer of FOx-25 to reduce it even more. But, this 20 nm is more than enough to guarantee successful graphene transfer and avoiding graphene tears over the steps across the sample.

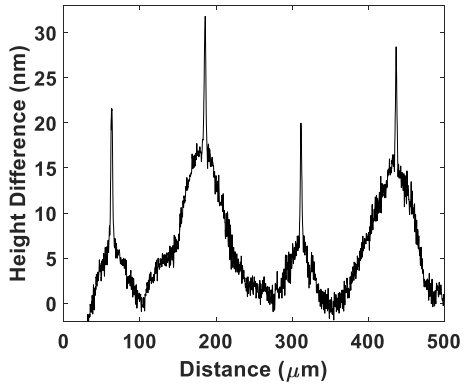

Figure 44. Result of the profilometry after spin coating the second layer of FOx.

After successful planarization we need to perform a final etch-back to uncover the SiN structures, as we want to have the graphene layers as close to passive SiN devices as possible. The alumina on top of the SiN passive structures will once again serve as etch-stop and help to protect them against plasma damage. So, we etch down FOx in an Oxford RIE system using an anisotropic oxide etch recipe as follows: RF power 200 W, pressure 33 mTorr, CHF3 25 sccm, Ar 25 sccm. Once the alumina is uncovered we no longer need it, and remove it from the top of my SiN passive structures using a hot Piranha solution. Piranha clean is safe

for my sample as none of the layers (SiN, baked FOx) get damaged by going through it. Figure 45 shows the schematic of the final planarized structure after removing the residue of alumina from top of the SiN structures.

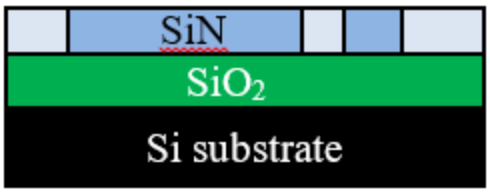

Figure 45. Schematic of the sample after planarization.

III.3.4 Double-layer Graphene on Planarized SiN

Now that the chip is planarized, we continue with the rest of the fabrication steps, which are as follows: transferring the first layer (bottom-layer) graphene on the sample using CVD grown graphene, patterning the bottom-layer graphene using EBL on PMMA and O_2 plasma, making metal contacts (Ti/Pd/Au) to the bottom-layer graphene using EBL and PMMA followed by metal evaporation and lift-off in Acetone, evaporating the Al seed layer on the bottom-layer graphene, depositing 14 nm ALD alumina as the capacitor dielectric, transferring the second-layer (top-layer) graphene on the sample using CVD grown graphene, patterning the top-layer graphene using EBL on PMMA and O_2 plasma, making metal contacts (Ti/Pd/Au) to the top-layer graphene using EBL and PMMA followed by metal evaporation and lift-off in Acetone, evaporating the Al seed layer on the top-layer graphene, depositing 9 nm ALD alumina as a final protective layer. Since, all of these steps were discussed in detail in the previous sections, we will not discuss them here again, and move on to discuss experimental results.

III.4 Experimental Results

Using the fabrication method that was discussed in the last section, double-layer graphene capacitor was integrated with different SiN passive structures. Figure 46 shows optical micrographs of some of the fabricated devices. Figure 46(a) is a SiN microring resonator, Figure 46(b) shows a Mach-Zehnder interferometer, and Figure 46(c) shows a coupling modulated microring resonator. Without the double-layer graphene capacitor integrated with them, they are all just passive structures without any efficient method for tuning or reconfiguration. However, now that a double-layer graphene capacitor is introduced on top of them, we can modify the resonance wavelength or its extinction by applying voltage to the graphene capacitor.

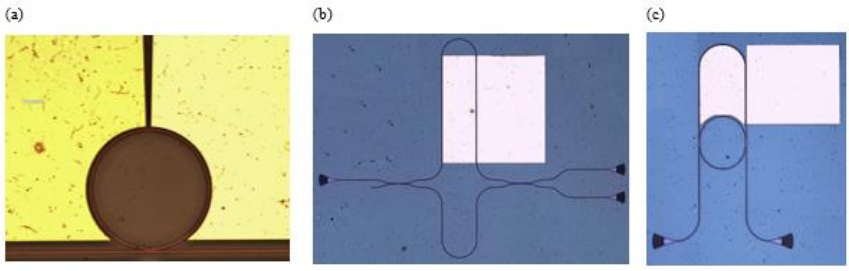

Figure 46. (a) A microring resonator, (b) a Mach-Zehnder interferometer, and a coupling modulated microring resonator. They are all fabricated on planarized SiN platform with double-layer graphene capacitor integrated with each to add tuning capabilities.

Characterization of the fabricated devices is done using a swept-wavelength transmission characterization setup. A fiber polarization controller is used to adjust the input polarization for the characterization. Grating couplers as shown in Figure 46(b) and Figure 46(c) are used to couple light into and out of the bus waveguides. The output light is detected using a variable gain photo-receiver and sent to a computer

through a data acquisition card. Figure 47 shows the TE transmission spectrum of two microring resonators with 20 µm radius coupled to a single bus waveguide. DC voltage is applied only to one of the microring resonators. We can clearly see from Figure 47 that through applying voltage to the graphene capacitor the extinction of only one of the resonators is changed while the extinction of the other one stays the same.

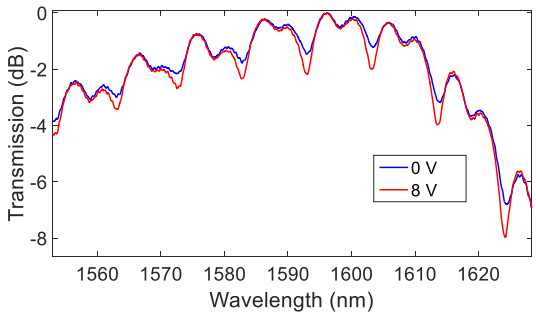

Figure 47. Transmission spectrum for two 20 µm radius microring resonators for the TE polarization. DC voltage is applied to the graphene capacitor on one of the resonators.

Figure 48 and Figure 49 show one of TE resonances of the same microring resonator. Here we can see that under applying both positive and negative DC voltages the extinction of the microring resonator is modified.

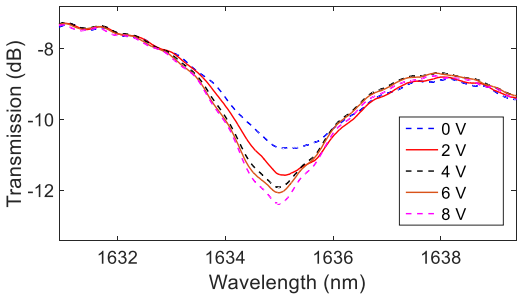

Figure 48 .TE resonance of a 20 µm radius microri[illegible] condit[illegible]

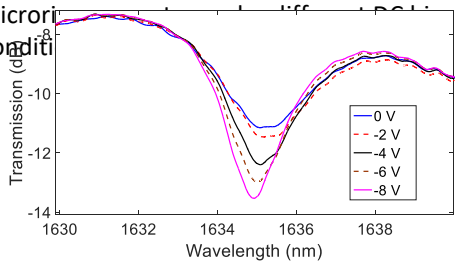

Figure 49. TE resonance of a 20 µm radius microring resonator under different DC bias conditions from -8 to 0 volts.

In summary, we developed a hybrid SiN-graphene material platform for development of functional devices such as high-speed and low-power modulators. The fabrication process for the hybrid SiN-graphene devices were developed. Through this work, we have developed a reliable process for fabrication of the double-layer graphene on SiN structures and have developed a series of SiN-based hybrid devices with relatively high yield and high performance, and modulation based on the developed device platform was demonstrated. The bandwidth of the operation of SiN-graphene hybrid structures could be increased by reducing the sheet resistance of transferred graphene films through exposing the graphene layers to forming gas to remove any residue of PMMA that might have been left on the surface after the transfer and EBL steps. Another approach to increase the bandwidth would be to reduce the capacitance of the double-layer graphene film through depositing a thicker dielectric. Due to the nature of the wet transfer process, both layers of graphene on the double-layer graphene capacitor are p-doped. Because of this similar doping polarities were only able to achieve small shift in the resonance frequency of modulators through electro-refraction effect. By modifying the doping level of one of the graphene layers and making it n-type (e.g., through immersing the transferred graphene into some wet chemical) much higher shift in resonance and more efficient modulation schemes would be possible.

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IV. Publications and Presentations

IV.A Expected journal papers in the near future

[1] H. Moradinejad, T. Fan, A.A. Eftekhar, A. Adibi, "High-speed graphene modulators on passive SiN substrates," To be submitted to Optics. Express (2017).

[2] T. Fan, A.A. Eftekhar, H. Moradinejad, A. Adibi, "High-speed graphene modulators on passive SiN substrates," To be submitted to Optics. Express (2017).

IV.B Conference presentations

[1] T. Fan, A. H. Hosseinnia, H. Moradinejad, A. A. Eftekhar, and A. Adibi, "Hybrid graphene modulator on CMOS platform for integrated photonic applications," accepted for Photonics West 2018, San Francisco, CA, January 2018.

[2] A. H. Hosseinnia, M. Sodagar, S. H. S. Mousavi, A. A. Eftekhar, and A. Adibi, "Hybrid CMOS-compatible material and device platform for integrated nanophotonics," Conference on Lasers and Electro-Optics (CLEO), San Jose, CA, May 2016.

[3] A. H. Hosseinnia, M. Sodagar, H. Moradinejad, T. Fan, A. A. Eftekhar, and A. Adibi, "High-speed active devices integrated in hybrid silicon on silicon nitride platform," CLEO, San Jose, CA May 2017.

IV.C Invited Conference and seminar presentations

[1] H. Moradinejad, M. Sodagar, T. Fan, A. A. Eftekhar, and A. Adibi, "Hybrid integrated photonic modulators based on carrier plasma dispersion effect in graphene," Invited for Presentation in IEEE Summer Topicals, Nassau, Bahamas, July 2015.

[2] M. Sodagar, H. Maoradinejad, A. H. Hosseinnia, A. A. Eftekhar, and A. Adibi "Hybrid material and device platforms for reconfigurable integrated nanophotonics," Integrated Photonic Workshop, IEEE Photonic Society Boston, Boston, MA, September 2015.

[3] A. Adibi, "Hybrid material platforms for reconfigurable integrated photonic structures", Invited for Presentation in Reconfigurable Electronic Workshop, Arlington, VA, May 2016.

[4] A. Adibi "Hybrid material and device platforms for reconfigurable integrated nanophotonics," Invited Seminar Talk, Jet Propulsion Laboratory, Pasadena, CA January 2016.

[5] A. Adibi "Hybrid material and device platforms for reconfigurable integrated nanophotonics," Invited Seminar Talk, University of Washington, Seattle, WA, January 2016.

[6] A. H. Hosseinnia, H. Moradinejad, M. Sodagar, A. A. Eftekhar, and A. Adibi, "Hybrid CMOS-compatible material and device platform for integrated nanophotonics," Invited for Presentation in CLEO: Science and Innovations, San Jose, CA, June 2016.

[7] H. Maoradinejad, A. H. Hosseinnia, T. Fan, M. Sodagar, A. A. Eftekhar, and A. Adibi, "Hybrid multi-layer integrated nanophotonics materials and devices," Invited for Presentation in SPIE Optics and Photonics, San Diego, CA, August 2016.

[8] H. Maoradinejad, T. Fan, A. H. Hosseinnia, M. Sodagar, S. Taghavi, A. A. Eftekhar, and A. Adibi, "Optical modulation in hybrid integrated nanophotonic platforms," Invited for Presentation in IEEE Summer Topicals, San Juan, Puerto Rico, July 2017.