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Ashwani Sharma

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AIR FORCE RESEARCH LABORATORY
Space Vehicles Directorate
3550 Aberdeen Ave SE
AIR FORCE MATERIEL COMMAND
KIRTLAND AIR FORCE BASE, NM 87117-5776

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ASHWANI SHARMA
Program Manager

//SIGNED//
DAVID CARDIMONA
Technical Advisor, Space Based Advanced Sensing and Protection

//SIGNED//
JOHN BEAUCHEMIN
Chief Engineer, Spacecraft Technology Division
Space Vehicles Directorate

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14. ABSTRACT

The Space Electronics Technology Branch (RVSW) is conducting a first time experimental and theoretical investigation focused on evaluating new physical phenomena in the quasi-quantum regime in which the hole mobility tends to exceed the electron mobility, and the electron reaches the group velocity in 2-D materials. These phenomena are due to a dramatic reduction of the hole's effective mass resulting from combined effects of two dimensional confinement coupled with strain/tensile effects, and due to the electron wave function not being able to penetrate the barrier regions in 2D materials.

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Summary

We report the transport characteristics of both electrons and holes through narrow constricted crystalline silicon (Si) long-channels that were surrounded by a thermally grown silicon dioxide (SiO_2) layer. The strained buffering depth inside the Si region (due to Si/SiO_2 interfacial lattice mismatch) is where scattering is seen to enhance some modes of the carrier-lattice interaction, while suppressing others, thereby changing the relative value of the effective masses of both electrons and holes, as compared to bulk Si. In the narrowest wall devices, a considerable increase in conductivity was observed as a result of higher carrier mobilities due to lateral constriction and strain. The strain effects, which include the reversal splitting of light- and heavy-hole bands as well as the decrease of conduction-band effective mass by reduced Si bandgap energy, are formulated in our microscopic model for explaining the experimentally observed enhancements in both conduction- and valence-band mobilities with reduced Si wall thickness. Also, the enhancements of the valence-band and conduction-band mobilities are found to be associated with different aspects of the theoretical model.

Introduction

For over 40 years, the microelectronics market place has driven the very large scale integration industry to make continuous improvements in computational power, bandwidth, and speed. These continued enhancements in performance have come in the form of “cramming” more components onto integrated circuits, as was predicted in 1965 by Moore. The push to increase the speed and density of the transistors on a chip has come in the form of shrinking the transistor size, in particular, the channel length. However, reductions in channel length have come with challenges, i.e., short channel effects. Short channel effects lead to higher leakage currents, poor signal-to-noise ratios, and instability during operation, such as loss of channel gate control. In order to improve the transistor’s gate control and switching speed, the complementary metal oxide semiconductor (CMOS) industry has looked for alternative solutions to the traditional planar transistor designs and substrates. Over the past several years, the CMOS industry has narrowed their focus into multi-gate field effect transistor designs for improving the gate control, and strained substrates to enhance carrier mobilities and ultimately the switching speed and drive currents.

Here we report a comprehensive experimental and theoretical study on the nature of carrier transport, of both electrons and holes, through narrow constricted crystalline Si “wall-like” long-channels that were surrounded by a thermally grown SiO_2 layer. The carrier transport characteristics were evaluated as a function of dimensional scaling of the Si wall widths from 200 nm to 20 nm. The Si wall-widths were reduced by the process of thermal oxidation, where stress naturally accumulates in the channel. Basically, this structure configuration allows us to investigate the effects of strained regions that are “closing-in” from both sides. Additionally, as the wall-widths approach the quasi-quantum regime, the carriers start to become confined and therefore react to the narrow paths, and possibly behave more like waves than particles, thus altering the macroscopic nature of resistance, capacitance, and inductance to a more exotic

microscopic one. However, this transition into the quantum mechanical regime does not come about abruptly. Rather, there is a transition region in which the bulk properties begin to slowly weaken while the quantum effects begin to strengthen.

The effects of quantum confinement on carrier transport properties, however, have been primarily investigated in ternary and quaternary material heterostructures and superlattices, in which scattering is seen to enhance some modes of the electron-lattice interactions while suppressing others, thereby changing the relative value of the carrier's effective masses of electrons and holes, as compared to bulk semiconductors. [1] To date such studies in Si have been very limited. We believe that these wall structures are a useful starting point for a broader study, as these can be configured into novel high density 3-Dimensional very large scale integrated devices, where thermal effects, such as heat buildup, can also be efficiently managed.

Methods, Assumptions, and Procedures

Si-on-Insulator (SOI) wafers with a top active layer of <100> crystal orientation were used to fabricate the wall-like structured devices for this research effort. The initial SOI structure had a 1500 nm active layer on top of a 3000 nm buried oxide. The SOI configuration allowed complete electrical isolation of the Si wall-like structures from the underlying substrate. All samples had identical p-type active layer with a lightly doped concentration of 10^{14} cm^{-3} boron atoms. Intrinsic SOI wafers would have been an ideal choice for the experiment; however, due to the commercial unavailability of 100% intrinsic material, the above choice of dopant type and concentration was adequate enough to minimize the effects of impurity scattering. Boron tends to segregate away from the Si interface and into the thermally grown oxide, thus reducing the impurity concentration near the Si interface with SiO_2. Thus the segregation coefficient, which is defined as the ratio of the dopant concentrations at the interface, is less than one in our case. The thermal oxidation process leads to the formation of an oxide-trapped charge, which contributes to the formation of a depletion region near the Si/ SiO_2 interface. Now, if we combine this oxide-trapped charge with the fixed charge which naturally results from the excess Si atoms not reacted with the oxygen, and the interface trapped charge which results from the mismatch between the number of atomic bonds in the Si crystal surface and the number of available bonds in the SiO_2 layer, these all combine to form a depletion region in the Si that extends several nanometers away from the SiO_2 interface. Thus the effective Si cross-sectional wall widths were considerably narrower than the actual physical widths, due this formation of depletion regions from both sides.

In order to fabricate the wall structures, photoresist nano-scale pattering was required. The precursors to the wall structures were patterned using interferometric lithography and reactive-ion-etching (RIE). The 1D nanoscale patterns were first formed in the photoresist followed by pattern transfer onto the underlying substrate using RIE in a parallel plate reactor using a sulfer-hexafluoride plasma chemistry. Figure 1 shows a scanning electron microscope (SEM) cross-sectional image of an array of nano-wall structures with a remaining layer of patterned photoresist after RIE has been performed. Note at this stage these structures are merely the precursors to the thin Si wall structures that are then reconfigured into metal-semiconductor-

metal (MSM) devices. After the photoresist was removed, the wall structures were thermally oxidized. The oxidation process accomplished two things. First, it consumed the Si, and thus thinned the wall width. Second, the thermally-grown oxide preserved a low defect, clean Si/SiO_2 interface, and at the same time passivated the surfaces of the nanostructures. The Si/SiO2 interface has low defects, and it is important to note that strain is present at the interface and it reduces with distance from the interface.

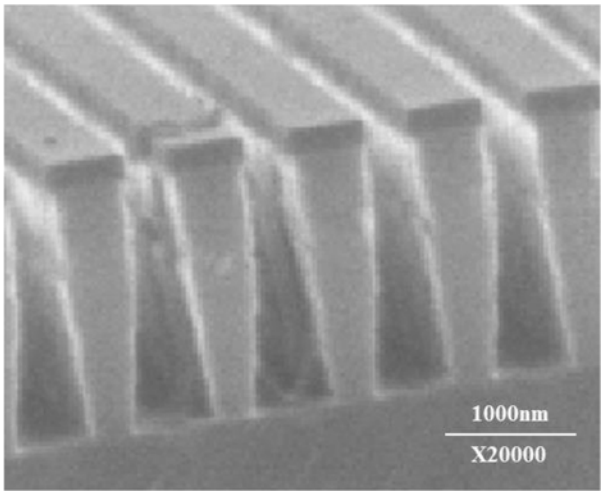


Figure 1. Scanning electron microscope cross-sectional image of an array of wall precursor structures with a remaining layer of patterned photoresist after reactive ion etch.

The modeling of the thermal oxidation parameters needed for the desired thicknesses was complicated due to the fact that in a three dimensional wall structure there are several crystal lattice orientations that have different thermal oxidation rates. As a first order approximation, we used average values of oxidation rates between the various lattice orientations, i.e., oxygen flow rate, pressure, temperature, and time. These parameters were then fine-tuned empirically during the actual thermal oxidation runs. Figures 2(a)-2(c) show SEM images of the cross-sectional views of the wall structures after the respective thermal oxidations. As can be seen from the SEM images, due to the high aspect ratio of these structures the oxidation rate was not fully uniform throughout the height of the walls. The rate was faster at the top part of the walls and slower at the bottom part due to higher availability of oxygen atoms in the upper regions.

The resulting wall-like Si structures surrounded by the thermally grown oxide were then configured into two terminal metal-Si/nanowall-metal (i.e., MSM) devices for optical and electrical characterization. The MSM device configuration was specifically designed so the current would flow within the wall boundaries between the electrodes. This allowed the physical cross-section of the wall structures to dictate the current flow properties. The mesa structures were fabricated to cutoff any stray current paths that could bypass the intended active region (wall) carrier path.

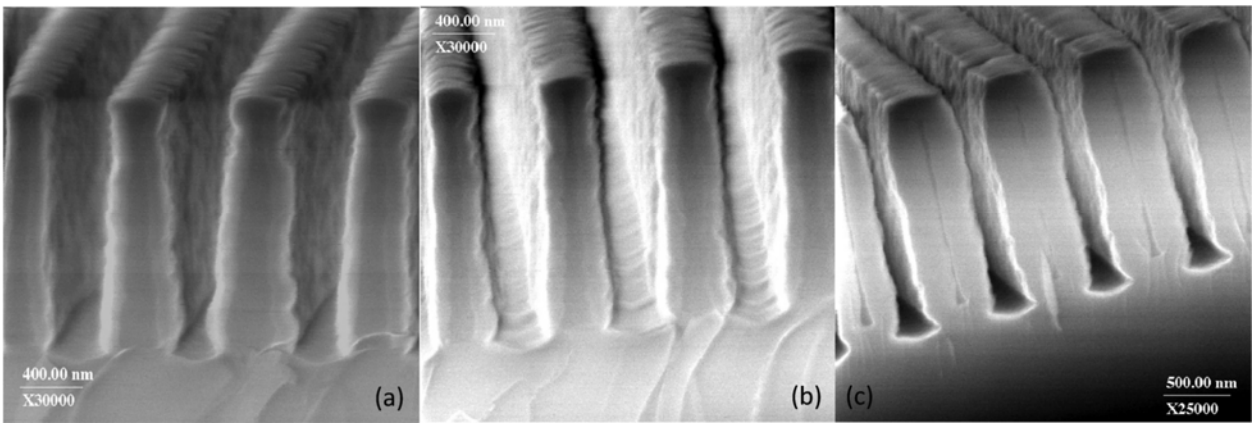


Figure 2. SEM cross-sectional images of an array of wall structures after thermal oxidation: (a) 200nm wall structures; (b) 95 nm wall structures; (c) 40 nm wall structures.

Figure 3(a) shows an SEM image of a typical pre-device mesa structure. After the walls were oxidized to achieve the desired wall width, the thermally grown oxide was selectively removed from the planar un-textured Si pad locations [Figure 3(b)] using an appropriate photo-mask and a chemical buffered-oxide etch. Following resist removal, the samples were cleaned using a sulfuric-acid/hydrogen-peroxide solution, and a deionized (DI) water rinse followed by a nitrogen gas dry step. The samples were then re-patterned using photoresist, and a second mask was used to form the electrode contact regions. Three separate evaporations of 30 nm of nickle (Ni) were performed. The first one was performed at normal incidence to the sample surface and the other two at a 30^{o} tilt angle in order to ensure complete coverage of the mesa step height. After Ni evaporation, liftoff was performed to remove the unwanted metal and resist using acetone. Following a thorough rinse using methanol/DI-water, the samples were again dehydrated and spin-coated with a thick resist layer. The samples were patterned using a final metallization mask. Layers of chromium (Cr) and gold (Au) were evaporated onto the electrode regions in a ratio of 30 nm/200 nm of Cr/Au, and the liftoff process was used to remove the resist and unwanted metal. Figure 3(c) shows an SEM image of a fully fabricated device.

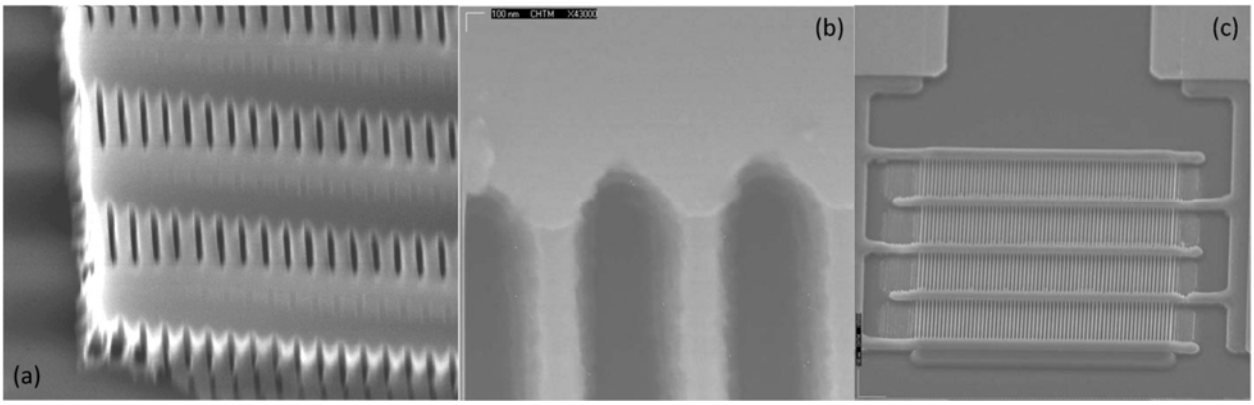


Figure 3. SEM images of (a) pre-oxidized Si mesa configuration with precursors to wall structures in the active region in-between planar un-textured regions where the metal contacts will be deposited; (b) planar un-textured Si where thermally grown oxide was removed for metal contact deposition connecting walls; (c) fully fabricated wall device with interdigitated electrodes.

The schematic of the pulsed carrier transport experiment is shown in Figure 4. This setup is based on a modified version of the Haynes-Schockley [2] experiment. This measurement provides an unambiguous direct measure of the actual transit time of electrons and holes through the channel. When a narrow pulse of light strikes the wall structured active region of the device near the left electrode as shown in Figure 4, equal numbers of electrons and holes are generated, and are then subjected to diffusion and drift forces in the presence of an electric field. Based on the experimental configuration, the electrons will be rapidly collected near the positively biased electrode and the holes will have to travel the entire channel to the negatively biased electrode. From the measured time response signal profile at the opposite electrode, the hole transient time limited carrier velocity can be determined, provided the carrier lifetime is greater than the total transit time. If the optical pulse of light strikes near the opposite electrode, the holes will be rapidly collected and the electrons would have to transit through the channel, thus the measured signal at the opposite electrode would be electron transit time limited. The pulsed response measurements were taken using a 150-fs duration excitation at λ = 400 nm from a cw modelocked Titanium-Sapphire laser (doubled for the short wavelength, 0.2 mW average power at a 77 MHz repetition rate). The wall structured MSM devices were probe tested using an 18 GHz probe and a high-speed digital sampling oscilloscope with an approximately 1 ps resolution capability. The laser spot size was 1 μm in diameter and the electrodegaps were 8 μm. Normal incidence was used for the experiment. The time response measurements were taken for low electric field strengths $3x10^3$ V/cm, (2.5V across 8 μm gap) thus avoiding velocity saturation.

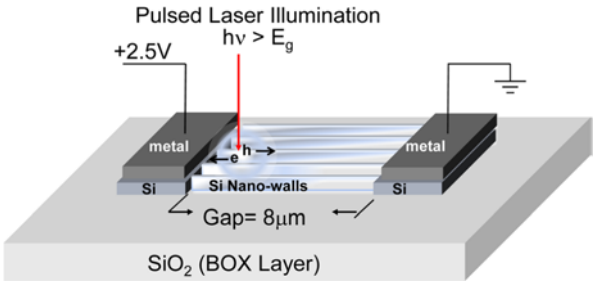


Figure 4. Schematic configuration of a wall structured MSM device used for carrier time response measurements.

Results and Conclusions

At room temperature only a small number of carriers are thermally generated (as dark current) for a Si bandgap of 1.15 eV. At low bias voltages (linear region of operation), the slope of the current versus voltage (I-V) dark current curve is proportional to the device resistance that includes contributions of thermally generated carriers from both the wall channels and the metal/semiconductor contact regions. At higher biases, the current saturates when all thermally-generated carriers are collected. Any further increase in the current can be attributed to leakages across the contact metal-semiconductor barrier and to nonlinear generation of carriers across the barrier. The back interpolation of this leakage current to zero bias (0 V) is a measure of the saturated dark current. Although the photocurrents are a few orders of magnitude larger than the thermally-generated dark currents, the analysis of the photocurrent I-V function is the same as the dark current I-V plots. For direct-current (DC) response analysis, two sets of measurements

were performed. These include: (i) dark currents as a function of wall width thickness, and (ii) photocurrents as a function of wall width thickness.

To study the carrier conduction properties versus dimensionally scaling down the width of the wall structures into the nano-regime, the samples were characterized in batches. Using samples with wall widths of 200 nm, 95 nm, 75 nm, 40 nm, and 20 nm, the room temperature dark currents were measured with a probe station and digital I-V curve tracer. As the physical cross-sectional area of the wall widths were reduced from 200 nm to 20 nm, we know from Ohm's law, for a given length, the resistance should increase linearly as the area decreases, and the resistivity should remain constant. However, as can be seen from Figure 5, the resistivity is not constant but drops significantly as the width of the wall is reduced below 95 nm. This suggests that there is an increase in conductivity as the wall thickness decreases from 95 nm to 20 nm. Since the number of thermally generated carriers is directly proportional to the volume of the active region, any increase in the conductivity, as wall width cross-sectional region decreases from 95 nm to 20 nm, cannot be attributed to the volume of the semiconductor material, but must be the result of a substantial increase in the carrier velocity. Confirmation of this hypothesized mechanism was obtained with the use of transient time analysis.

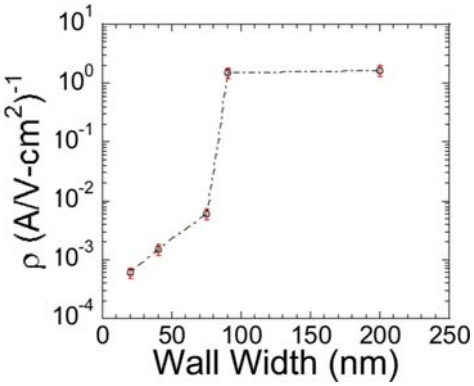
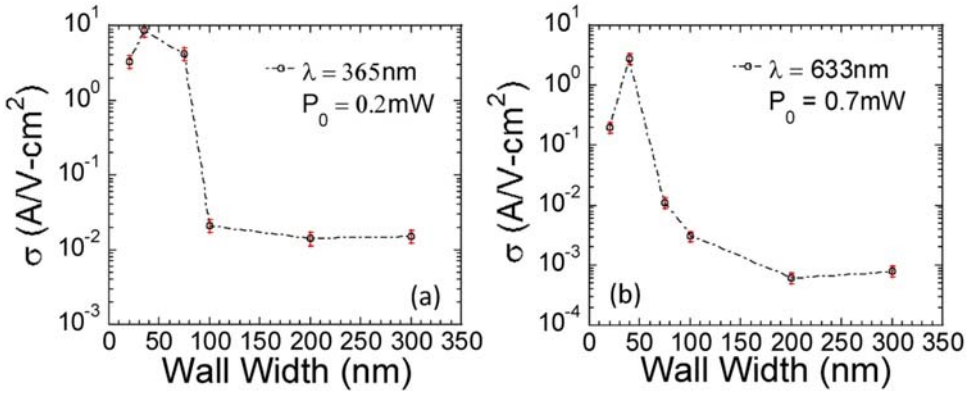


Figure 5. Plot showing resistivity characteristics as a function of down scaling the wall widths.

DC steady state photocurrents were measured using a 365 nm wavelength, 1.132 W/cm^2 argon-ion laser and a 633 nm wavelength, 3.96W/cm^2 helium-neon laser. The laser beam spot diameter was less than 8 μm and was focused within the active region of the electrode spacing covering several wall structures. By using 365 nm and 633 nm wavelengths, a more complete insight into absorption and carrier transport as a function of wall thickness can be achieved. At 365 nm, absorption occurs within the top first 10 nm of the Si wall structures with heights of 1500 nm. For 633 nm the total photon absorption extends through the entire wall height. Figures 6(a) and 6(b) show the conductivity versus wall thickness profiles, respectively. As can be noted from the figures, a peak in the conductivity occurs around the 40 nm (physical wall width) samples followed by a decrease around the 25 nm width samples. The significance of this can be explained through the effects of strain inside the wall structures that affect the carriers mobilities as the dimensions are reduced.



(a) **(b)**

Figure 6. Plots of photoconductivity characteristics as a function of down scaling the wall widths for: (a) λ = 365 nm; (b) λ = 633 nm.

Figure 4 shows the bias polarity of our experiment in which the left electrode polarity is positive and the right electrode is ground. With this bias configuration once a pulse of light with a spot size <1 μm, as in the case of our experiment, strikes within the active region, the holes travel towards the right electrode and the electrons travel in the opposite direction towards the left electrode. Figures 7(a) – 7(d) show the experimental results of the time response measurements for 200 nm, 95 nm, 40 nm, and 20 nm thick wall devices for both electron and hole dominated signals. From a first pass, as can be seen from these plots, as the thickness of the wall-channels is decreased, the time response signal decays faster. In particular, in the case of the 40 nm and 20 nm thick walls, the signal decays over an order of magnitude faster than the 200 nm sample for both electrons and holes. The rise time of the signals is an important parameter, since it directly provides the carrier transit time. The rise time is defined as the time-lapse from the moment when the pulse of light strikes one end of the active region of the MSM, near one electrode, and the moment when the photogenerated carrier signal is detected at the opposite electrode. From the rise time data, provided on Figures 7(a) – 7(d), we can determine the carrier mobilities as a function of wall thickness.

Figure 8 shows a plot of average field dependent electron and hole limited mobility values using the experimental values of rise time and the expression: average mobility = (carrier velocity) times (electrode gap) divided by (external applied bias), as a function of wall thickness. Here, carrier velocity = (electrode gap) divided by (rise time). We know that the carrier transport of electrons and holes in the thickest wall sample (200 nm) is essentially similar to the transport properties in bulk silicon. However, we observe a considerable increase in low field dependent mobility values below 75 nm wall thicknesses. Recall the fact that we actually have much narrower effective cross-sectional regions from which carriers propagate due to the repulsive nature of the boundary at the Si/SiO_2 interface, and the carrier profile tends to peak a certain distance away from the interface close to the center of the wall structures. At these nanoscales, we must account for the strain effects, which include the reversal splitting of light- and heavy-hole bands as well as the decrease of conduction-band effective mass by reduced Si bandgap energy.

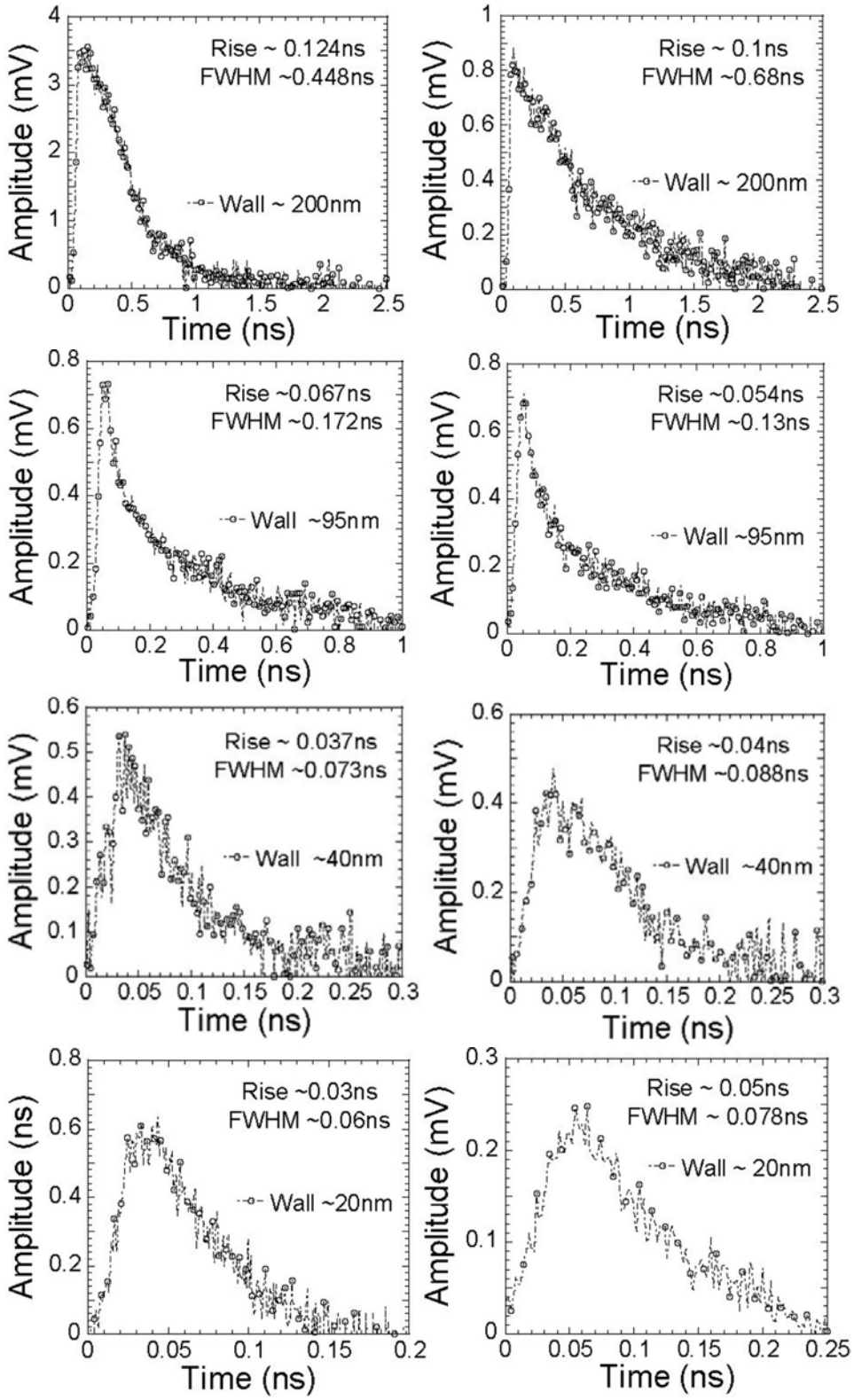


Figure 7. Measured time response signals of 200nm wall (row-1), 95 nm wall (row-2), 40 nm wall (row-3), and 20 nm wall (row-4).

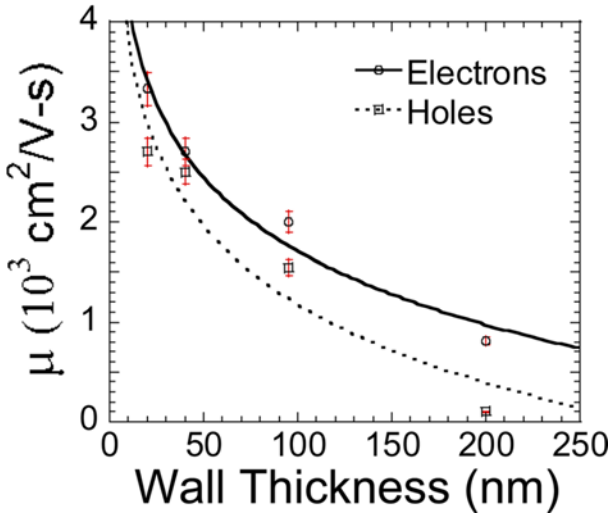


Figure 8. Carrier mobility values calculated from direct measure of rise time values as a function of wall thickness.

In summary, the semiconductor processing, fabrication, and the resulting carrier transport characteristics of MSM devices fabricated as wall like structures in silicon on insulator technology were reported here. MSM device dark current, DC photocurrents, and the time response of carrier transport were investigated. The resulting conducting channels were actually smaller than their physical dimensions, a result of depletion of carriers near the interfaces. As the physical channel widths were reduced by oxidation, strain was produced near the interface and the strained lattice became a significant portion of the conducting channel. The changes in carrier mobilities stemming from the strained silicon resulted in a dramatic increase in mobility for both electrons and holes as the physical channel width was reduced from 200 nm to 20 nm. If these electron and hole mobilities can be retained with the application of gate electrodes, then this technique may yield a much simpler path towards high performance CMOS, both n-channel and p-channel, than current techniques for either planer ultra-thin body or fin-shaped field-effect transistors.

The work on this Advanced Electronics project performed between October 2015 and April 2017 in the Spacecraft Electronics Technology Branch of the Space Vehicles Directorate in the Air Force Research Laboratory has been published in References [3] – [5].

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List of Symbols, Abbreviations, and Acronyms

Si: silicon
SiO_2: silicon dioxide
CMOS: complementary metal oxide semiconductor
SOI: Silicon-on-Insulator
RIE: reactive ion etching
SEM: scanning electron microscope
MSM: metal-semiconductor-metal
DI: deionized
Ni: nickel
Cr: chromium
Au: gold
I-V: current versus voltage
DC: direct-current

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