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DARK CURRENT REDUCTION OF IR DETECTORS

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Trustees of Boston University

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14. ABSTRACT ***(Maximum 200 words)***

This research and development program aims at demonstrating a novel approach to dark current reduction for dense infrared detector arrays. This technique is based on the diffusion control junction (DCJ) concept that has been developed at Boston University. The DCJ concept is material and wavelength agnostic and was applied to the design of dense arrays fabricated with InGaAs and HgCdTe. Modeling and simulation was performed to try to better understand the underlying physics. Through this modeling effort, it was demonstrated that a more symmetric annular control junction provides the highest degree of dark current suppression, but at a greater loss of quantum efficiency. Unfortunately, characterization of the actual arrays did not demonstrate a noticeable degree of dark current suppression when biasing neighboring junctions. The results also indicate problems with the device fabrication process. The isolated diodes, arrays, and variable area diodes all have extremely high dark currents, exhibited increased dark current with the contact anneal, and do not vary with junction area. All of these symptoms are inconsistent with what can be expected for p-n junctions formed in SWIR InGaAs using the double layer planar heterostructure. More work is required to determine the cause of these problems.

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1. Summary

Through the course of the program we have developed a fabrication procedure for SWIR InGaAs photodetectors, and attempted to demonstrate a new pixel architecture that can be used to lower the dark current, and hence, improve the sensitivity of existing devices. To support the fabrication process, a significant number of finite-element simulations were performed to try to better understand the underlying physics. Through this modeling effort, we demonstrated that a more symmetric annular control junction provides the highest degree of dark current suppression, but at a greater loss of quantum efficiency. We also provided evidence that this lost QE can be recovered through the use of microlens arrays, which are already used in photodetecting arrays today. Future work on the modeling will include additional simulations on optimizing the control junction structure in terms of detectivity and crosstalk.

At the time of writing this report, the characterized arrays do not demonstrate a noticeable degree of dark current suppression when biasing neighboring junctions. However, the results also indicate remaining issues with the device fabrication process. The isolated diodes, arrays, and variable area diodes all have extremely high dark currents, exhibited increased dark current with the contact anneal, and do not vary with junction area. All of these symptoms are inconsistent with what can be expected for p-n junctions formed in SWIR InGaAs using the double layer planar heterostructure. More work is required to determine the cause of these problems.

While the devices fabricated at Boston University do not demonstrate the DCJ effect, we are confident that our simulations are accurate, and that the problem lies with the process. In an effort to prove this, we will continue this work outside of this program and update the participating parties (AFRL, DARPA, and ARL) with any new findings.

2. Introduction

This research and development program aims at demonstrating a novel dark current reduction approach for dense infrared detector arrays. This technique is based on the diffusion control junction (DCJ) concept that has been developed at Boston University. Although the DCJ concept is material and wavelength agnostic, during the proposed research program it was applied to the design of dense arrays fabricated with InGaAs and HgCdTe (MCT).

The main goal of the program is to successfully fabricate and test detector arrays with and without DCJs on the same wafer and demonstrate the effectiveness of the DCJ approach in reducing dark current. Preliminary simulation results indicate that for HgCdTe/InGaAs dense arrays, with pixel pitch less than 20μm designed for the extended short wave infrared (E-SWIR) spectral band, we can expect an order of magnitude decrease in dark current when operating in a diffusion-limited regime and at temperatures in excess of 250K. The experimental results will be also used to validate our material and 3D device simulation model to further optimize the array configuration. The team that will carry out the proposed work includes the Army Research Laboratory (Adelphi, MD) and DRS Technologies (Cypress, CA). Both organizations will participate in the development of the DCJ technology with their fabrication and testing capabilities. Furthermore, their participation in this program will provide a technology transfer path that may lead the use of the DCJ concept in commercial infrared FPAs.

2.1 - Motivation

One of the performance limiting factors in the operation of infrared detectors and imaging devices is the dark current. Dark current is due to the contribution of different mechanisms, that are broadly classified into two categories: intrinsic (due to the fundamental material physics) and extrinsic (due to the technology). For example, the latter results from phenomena due to carrier generation/recombination via traps, and tunneling/surface leakage currents. In state of the art InGaAs/HgCdTe focal plane arrays designed for the short-wave spectral band, the dominant current sources are from thermally generated carriers from intrinsic mechanisms (mainly Auger and radiative) that diffuse to the junction from the quasineutral region, and from generation through defect levels within the band gap (Shockley-Read-Hall).

The main approach to reduce the extrinsic contribution is to improve the material quality and fabrication techniques. Unfortunately, reducing the contribution from intrinsic mechanisms is more difficult. It is possible to cool the device, often to cryogenic temperatures, in order to reduce dark current generation, but at the cost of detector versatility. Furthermore, cooling systems require more power, add bulk to the end product, and are expensive.

The new detector architecture we intend to demonstrate is based on a new paradigm for thinking about the pixel sub-architecture. In fact, existing approaches accept bulk radiative or Auger recombination currents as fundamental limits on device performance, and therefore focus on reducing dark current through expensive fabrication or material processing improvements, novel epitaxial structures, power-hungry thermoelectric or cumbersome cryogenic cooling. Our new approach, by contrast, applies insight from fundamental physical models to provide complementary dark current suppression through structural modifications.

Conceptually our new approach, and our ability to push dark current below the radiative or Auger limit, might be compared to noise squeezing, in that we trade higher dark current in some array locations for lower dark current in signal extraction locations. Furthermore, the dark current falls (due to the dense array effect) faster than the photocurrent (which falls as a given diode effective optical volume is reduced by hole collection by intervening diffusion control junctions), resulting in a net benefit. The diffusion control junction is especially valuable since it is immediately compatible with existing detector array technology without including additional processing steps. Moreover, it is also compatible with the current read out integrated circuit (ROIC) technology and consequently it does not require re-design effort.

3. Theory and Simulation

In this section, we describe the fundamental concept behind the DCJ approach and present the simulation approaches used to predict the potential improvement in dark current performance for InP/InGaAs based double heterostructure detectors.

3.1 – DCJ Fundamentals

The DCJ concept has evolved from the analysis of pixel arrays that operate under the so called "dense array" condition [1,2]. This is broadly defined as a detector array in which the pixel pitch and the thickness of the absorber are both smaller than the minority carrier diffusion length $L_{p,n}$. For a p+-on-n planar array with diffused junctions shown in Figure 1, the dense array condition is satisfied if $2L < L_p$ and $W_{epi} < L_p$. In the case of E-SWIR HgCdTe a conservative estimate of the hole lifetime leads to a value of $L_p = 20\mu m$ that is larger than the typical absorber layer thickness and leads operation in the dense array condition for pixel pitch smaller than L_p. A similar situation is encountered in SWIR InGaAs detector arrays, for which arrays with pixel pitch smaller than 10μm have been fabricated.

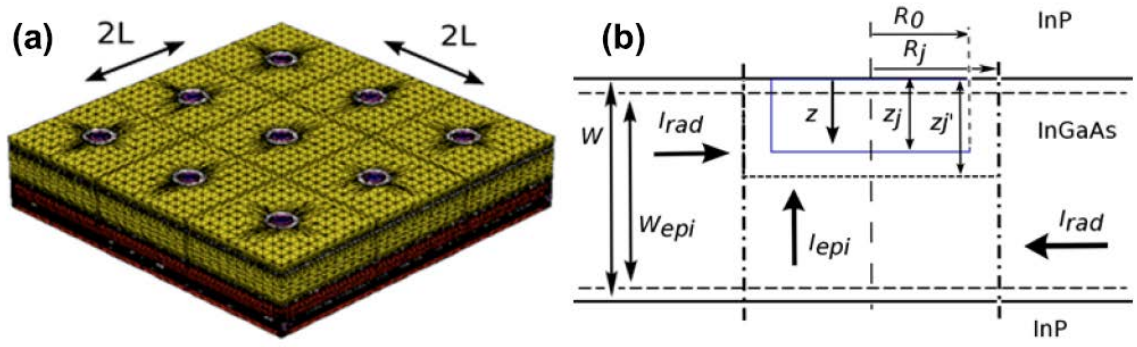

Figure 1: *(a) 3×3 pixel array model. (b) Geometric parameters defining the single pixel structure.*

To understand how the dense array condition affects the array operation we consider first an isolated detector diode. This can be approximated in a conventional P^+n double layer planar heterojunction (DLPH) 3 x 3 pixel array by reverse biasing the center pixel and grounding the neighbors. In such a pixel operated under constant reverse bias, the minority carrier density (holes) reaches a minimum directly underneath the junction. This is shown in Figure 2(a). If one considers a cross section of the device, as in Figure 2 (b), it is possible to see that in an isolated diode (blue top line) that the minority carrier density will return to the unperturbed thermal equilibrium value far from the junction. The dark (reverse bias) current in this pixel diode is proportional to the gradient of the minority carrier density in the region close to the depletion region.

If one considers the case in which all the pixels in the array have equal bias a different situation is found. Figure 2(c) presents the minority carrier density distribution in the pixel array for this case. We can notice that for this operating mode, unlike the case of the pixel diode, the minority

carriers are symmetrically distributed in the array. Further insight can be gained by looking at the minority carrier distribution along the array cross section, as shown in Figure 2(b), represented by the bottom black line. It is immediately possible to make two observations: the overall value of the carrier density is lower and the gradient close to the depletion region boundary is smaller than the previous case.

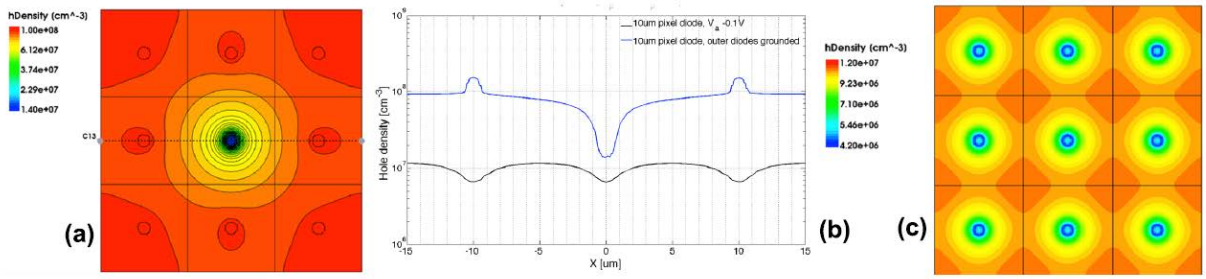

Figure 2: (a) Map of the minority carrier distribution in an isolated pixel diode. (b) Minority carrier density along a cross section of the device: upper (blue) line for pixel diode, lower (black) line pixel array with equal bias. (c) Map of the minority carrier distribution in a pixel array with equal bias.

As a result, one can reach a number of important conclusions that are valid when the dense array condition is fulfilled. Specifically:

1 - The shape of minority carrier distribution in a dense array, unlike in the case of an isolated diode, is determined by the presence of the neighboring pixels.
2 - Due to the symmetry of the system, the gradient, and consequently the lateral diffusion current is zero at the middle point between two pixels.
3 - Due to the lower gradient of the minority carrier distribution close to the depletion region, the dense array presents a lower dark current than an isolated pixel diode with similar geometrical features.

We want to point out that this is not due to different material properties but is a purely geometrical effect. It is also important to understand the fact that if the minority diffusion length is much smaller than the pixel pitch, then the minority carrier density would return to the bulk equilibrium value and the dark current will be larger. Based on these observations, it is clear that in a dense array it is possible to modify the gradient of the minority carrier density, and as a result, the dark current by a suitable choice of bias on the neighboring pixels. In practice, this can be obtained by using a number of DCJs that can actively tune the distribution of the minority carrier density profile in the device.

3.2. Simulation Results for SWIR (DLPH) InGaAs Array

We have investigated the possibility of applying the same concept to SWIR DLPH InGaAs detector arrays. In this case it is also possible to compare the improvement obtained with the state of the art results measured by different organizations. We have considered first device structures similar to what has been reported in literature by a number of manufacturers. The 3×3 miniarray has a pixel pitch of 10μm, r0 = 0.5μm, z j = 0.1μm, Wn = 3μm, ND = 10^{16}cm^{-3}, NA = 5×10^{19}cm^{-3}. To determine the dark current reduction, we bias the center pixel at a fixed voltage

of VA = -0.1V and change the voltage on the outer pixels to a lower value. Figure 3 presents the calculated dark current. In this case it is also possible to appreciate that the DCJ approach becomes much more effective at suppressing the dark current as the temperature increases. Furthermore, if the bias voltage on the DCJs is kept constant and the dark current of the sensing diode evaluated as a function of temperature we can compare the DCJ improvement against the current state-of the art. Figure 4 presents a comparison between six published sets of results [3-8] and the predicted dark current computed using a ring of pixels around a sensing diode to simulate the DCJ effect. Even using such a rudimentary approach, the calculated dark current with the DCJs (downward triangles) is close to an order of magnitude smaller that the state of the art above room temperature and below the fundamental diffusion limit of InGaAs.

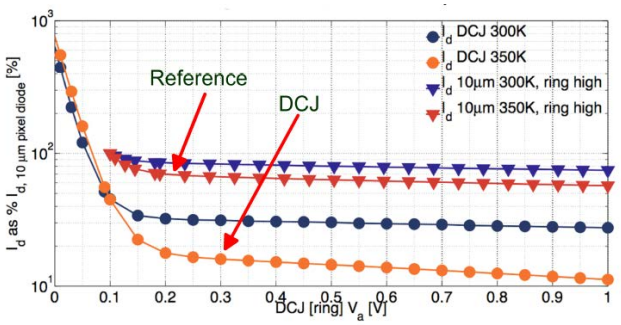

Figure 3: Comparison between calculated dark current with and without DCJs in an InGaAs DLPH detector arrays at T = 300K and T = 350K.

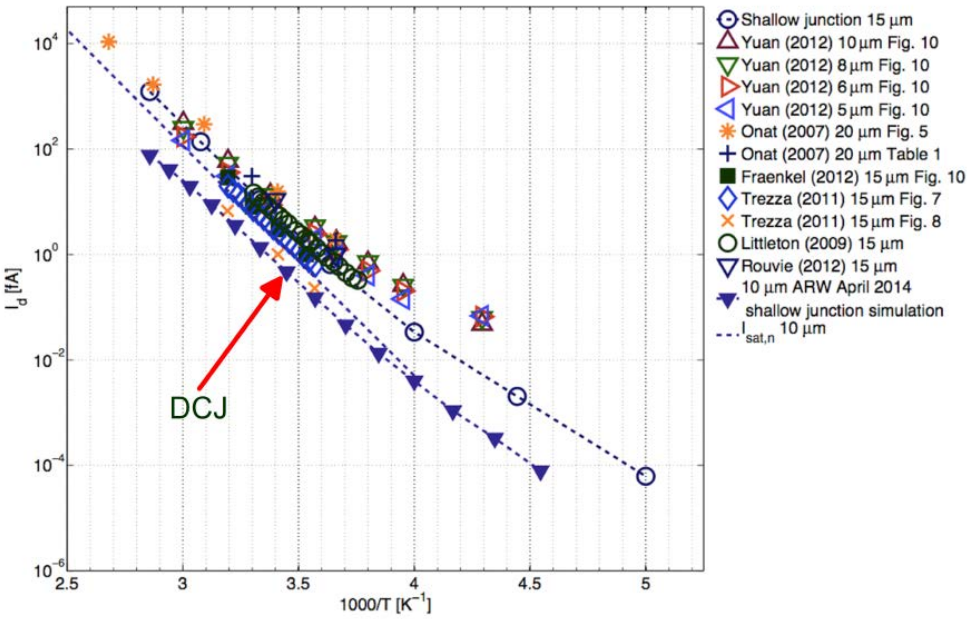

Figure 4: Comparison between six published set of results for SWIR InGaAs arrays and the predicted dark current when using a ring of pixels around a sensing diode to simulate the DCJ effect.

3.3. Quantum Efficiency Modelling of DCJ Structures

While the dark current can be potentially reduced using DCJ structures, this has to be achieved without compromising any other array performance parameters. Photo-generated carriers are indistinguishable from the ones contributing to the dark current, and hence, are also subject to the influence of the diffusion control junctions. To study this, we consider a fully guarded pixel, in which an annular DCJ structure fully surrounds the sensing diode. Figure 5 presents the structure and the relevant geometric and doping parameters. Here, we present results on the quantum efficiency and ratio of photo to dark current. To perform these calculations, we employ an optical excitation constituted by a gaussian beam of variable size, in order to provide evidence that if the optical generation can be localized beneath the sensing junction, the quantum efficiency can be recovered.

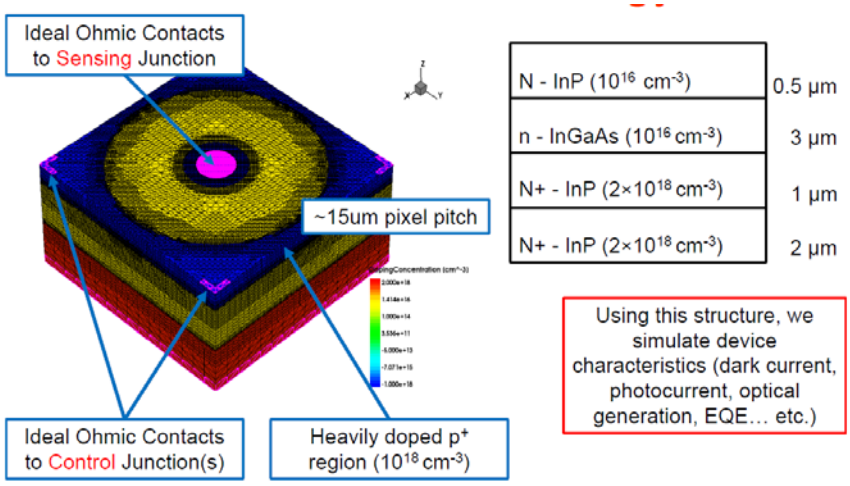

Figure 5: All around DCJ structure used to evaluate the effect of the DCJ on quantum efficiency.

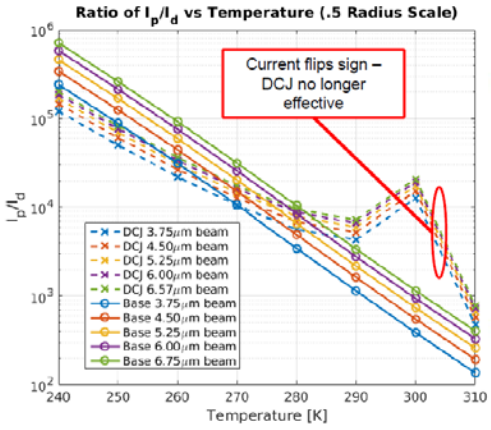

Figure 6: Temperature dependent dark to photocurrent ratio as a function of the size of the illuminating beam for a device with (DCJ) and without (Base) DCJ.

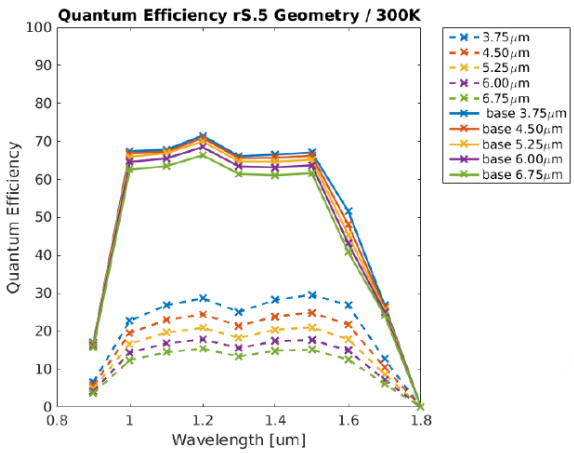

Figure 7: Wavelength dependent quantum efficiency as a function of the size of the illuminating beam for a device with (DCJ) and without (Base) DCJ.

Figure 6 presents the calculated dark to photocurrent ratio as a function of the operating temperature. As the temperature increases the DCJ effect becomes more effective. At an operating temperature of 300K the improvement in the dark to photocurrent ratio can be up to ten times greater than the baseline case. One can also notice that this value decreases slightly when the beam size is reduced. Figure 7 presents the calculated quantum efficiency as a function of the wavelength for different beam radiuses. The calculated quantum efficiency is significantly lower when the DCJ structure is included. This is because the DCJ will collect carriers that will not contribute to the sensed photocurrent. As we decrease the beam size the quantum efficiency marginally increases, but never fully returns to the original value. To mitigate the lost QE, we consider using micro lenses fabricated on the back of the substrate. Figure 8 present the geometrical model of the micro lenses (left) and the optical generation (right) resulting from a uniform illumination of the device. It can be immediately noticed that the optical generation is concentrated very close to the sensing junction. To verify that the use of micro lenses leads to an improvement we have recalculated the dark to photocurrent ratio and the quantum efficiency.

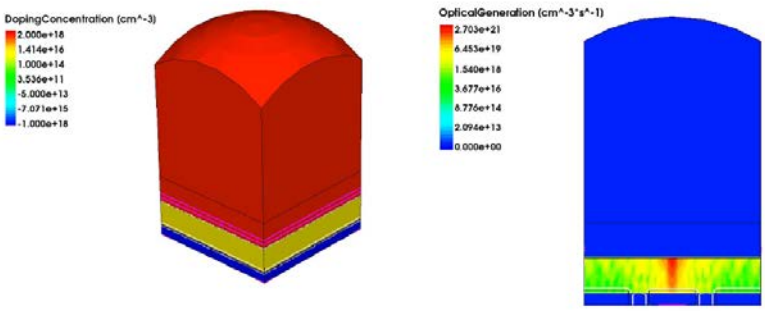

Figure 8: Micro lenses geometrical model (left) and calculated optical generation (right) resulting from a uniform illumination of the device

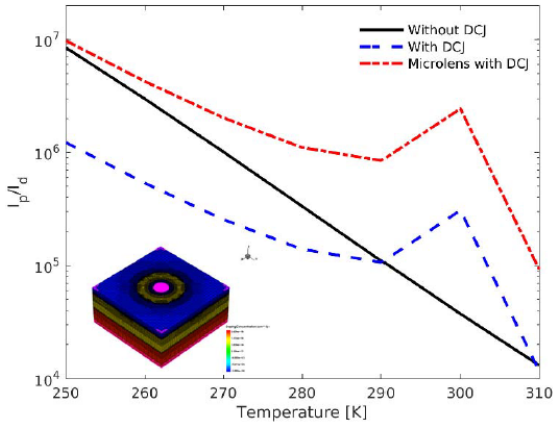

Figure 9: Calculated dark to photocurrent ratio for a DCJ structure without (blue line) and with (red line) micro lenses.

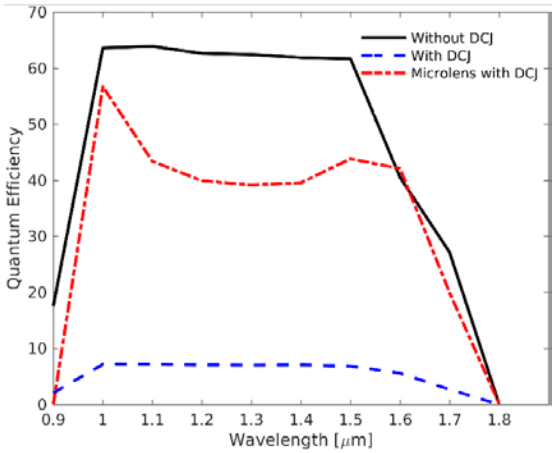

Figure 10: Calculated dark to photocurrent ratio for a DCJ structure without (blue line) and with (red line) micro lenses.

Figure 9 presents the calculated dark to photocurrent ratio for a DCJ structure without (blue line) and with (red line) micro lenses. Because of the micro lenses, more photo-generated carriers are collected by the sensing junction and this lead to a higher dark to photocurrent ratio. This beneficial effect is also present when the quantum efficiency is considered. As it can be seen in Figure 10, the calculated quantum efficiency for a DCJ structure with (red line) micro lenses is significantly higher than in the case when the micro lenses are not employed (blue line). Further optimization of the micro lenses shape and position may lead to an additional performance improvement.

4. Fabrication Process

We have attempted to provide a practical demonstration of the DCJ approach using two different material platforms. At BU an InP/InGaAs double hetero-structure was selected to try to show the DCJ phenomena in the SWIR spectral band. At ARL the same approach was pursued with HgCdTe material tailored for the MW spectral band.

Two 2" InP/InGaAs wafers were purchased from IQE with internal funding from the BU-Ignition program. The only difference between the two wafers is the n-type doping level in the absorber. One wafer is doped 5 x 10^{16} cm^{-3} while the other is 10^{16} cm^{-3}. The two donor concentrations were chosen to show how the efficacy of the DCJ effect changes for a different device structure. Due to the limited amount of material available, we diced one wafer into individual dies of one square centimeter in order develop the fabrication process. Scrap pieces around the sides of the wafer were used for blanket diffusions, contact tests, and other general process steps. The remaining nine square pieces were used for the final devices. Due to time constraints, only one of the wafer was used for this round of fabrication. Figure 11 presents a photograph of the diced wafers. A schematic representation of the pixel detector structure is shown in Figure 12. Both isolated diodes and small pixel arrays, with a 50 x 50 configuration were fabricated. In the case of single diodes, the contact on the n-type layer is nearby the device. In the case of arrays, two common contacts are placed at two opposite corners of the array. As it can be seen in Figure 12, the junction is formed by diffusing zinc into the wafer through a 50nm thick InGaAs contact layer, a 500nm thick InP cap layer thick, and into the InGaAs absorber layer. Controlling the depth of the zinc diffusion is critical in order to minimize the detector's dark current and maintain a high quantum efficiency. The InGaAs contact layer is etched in order to isolate the pixels, to form the p-type contact, and serve as an alignment layer for subsequent processing steps. A deep etch is used to form the common n-type contact on the highly doped InP substrate. The device is passivated with a silicon dioxide or silicon nitride passivation layer. To be able to fabricate the diode and detector arrays a process was developed at BU and implemented both in the BU Optoelectronics Fabrication Facility (BU-OPF) and the Harvard Center for Nanoscale Systems (Harvard-CNS). The main steps of the fabrication recipe are outlined in Table 1. The entire process requires between four to five days to execute, excluding tool downtime. The critical steps were optimized using test pieces and test structures and, when possible, silicon and InP wafers were used instead of the more expensive InP/InGaAs material.

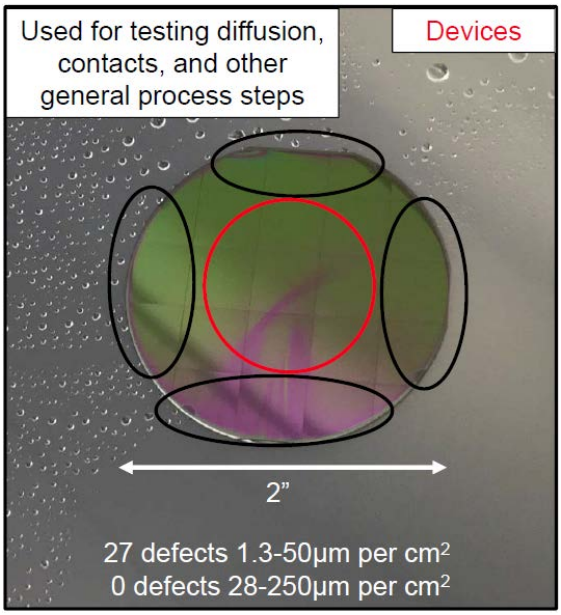

Figure 11: Photograph of the diced InP/InGaAs wafer.

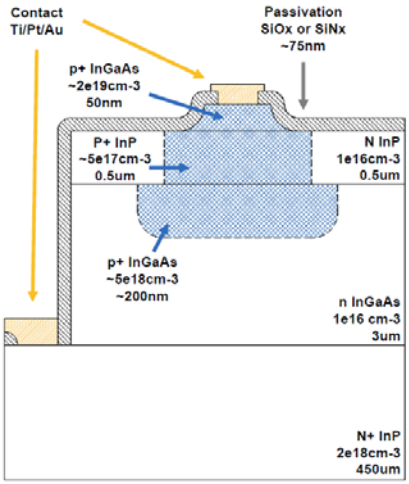

Figure 12: Schematic representation of the detector structure

Table 1 – Processing step for the fabrication of the InP/InGaAs

1	Surface preparation / particle removal (repeated before every step)
2	Etch InGaAs contact mesas, used for ohmic contact and alignment
3	PECVD oxide #1 ~200nm (diffusion blocking layer)
4	Pattern oxide in HF for zinc diffusion
5	Spin on zinc, 250°C hotplate, plasma asher 150 W 40 sccm 10 min
6	PECVD oxide #2 ~200nm (capping layer to prevent substrate sublimation)
7	RTA diffusion 500°C 10 minutes in forming gas
8	Remove oxide and dopant film in with HF dip
9	PECVD oxide #3 ~75nm (passivation)
10	Pattern oxide for metal-semiconductor contacts
11	Final metallization using e-beam evaporation and lift-off

4.1. Lithography and Lift-off Process

We began by conducting a series of lithographic cycles to determine the smallest geometries that we can feasibly fabricate at Boston University. Using a variable transmissivity photomask, we can easily optimize any step involving photolithography, such as a typical positive process or a lift-off technique. For example, Figure 13(a) and Figure 13(b) presents the result of the result of the lift-off for process of 5nm Ti / 200nm Al metal stack on an InP substrate using the well-known ammonium hydroxide image reversal method. It can be seen that features with linewidth as fine as 2μm can be reliably obtained.

(a) (b)

Figure 13: (a) Result of lift-off process for features with linewidth of 2μm; (b) Result of lift-off process for features with linewidth of 4μm.

To guarantee a sufficient margin of error during the mask alignment, a minimum feature size of 4μm was used. This choice limits the minimum pixel geometry that can be implemented with the contact lithography process available at BU.

4.2. Zinc Diffusion Process

The formation of p-n junctions and, as a result, the sensing diode structure, is the most critical step in the fabrication process. There are several problems to overcome when performing the diffusion: controlling the junction depth, removing possible contaminants from the surface (as with all high temperature process steps), and preventing outgassing of the group V element. The typical approach for III-V detectors is to use a gas source for the diffusion, either during the material growth or in a tube furnace with an overpressure of phosphorus or arsenic. At BU, we do not have the required setup to handle the toxic gases involved with a gas source diffusion, so we have opted for a different approach using a spin-on film.

For both gas source or spin on film diffusants, a diffusion blocking layer is required to selectively dope specific regions of the substrate. While, Si_3N_4 is typically used as a diffusion blocking and passivation layer, its removal is challenging and prohibitive for the sample sizes that we are working with. In fact, the etch rate of Si_3N_4 in HF is too long for photoresist to be an effective masking material. An alternative involves an additional deposition of SiO_2 as a hard mask, patterning this layer in HF, and finally etching the Si_3N_4 in boiling phosphoric acid. Due to the increased complexity of this process, we have attempted to solely use SiO_2 as the diffusion blocking layer and passivation. This simplifies patterning/removal and eliminates one PECVD cycle. We have tested this in InP wafers and subsequently transferred the procedure to InGaAs/InP. Above 350°C, the volatile group-V elements (phosphorus, arsenic) can sublimate from the substrate, destroying the surface morphology. As a result the III-V materials require a capping layer of oxide or nitride layer to prevent out-diffusion of this material. An example of process is shown in Figure 14, in which it can clearly be seen the holes left behind as a result of the Outgassing of group-V elements from mask openings during zinc diffusion process.

Figure 14: Outgassing of group-V elements from mask openings during zinc diffusion process

To verify the outcome of the zinc diffusion process we have performed a study using secondary ion mass spectroscopy (SIMS) and determine the zinc diffusion profile. We have performed a number of blanket diffusions on side pieces from the InP/InGaAs wafer at different annealing temperatures and measured the SIMS profiles. Figure 15 presents the measured diffusion profiles

of zinc in InP and InGaAs. The annealing process was performed at a temperature of 500C for 10 minutes. The junction is relatively shallow with a depth approximately of 150-250nm. This value is what it is needed for optimal devices performance. Furthermore, the very high concentration of zinc at the InGaAs contact layer surface, ideal for ohmic contact formation. It should be pointed out that this result is valid for blanket diffusions on non-patterned samples. The situation may be different for diffusions through small openings. We are currently investigating the effects of aperture size on the diffusion profile.

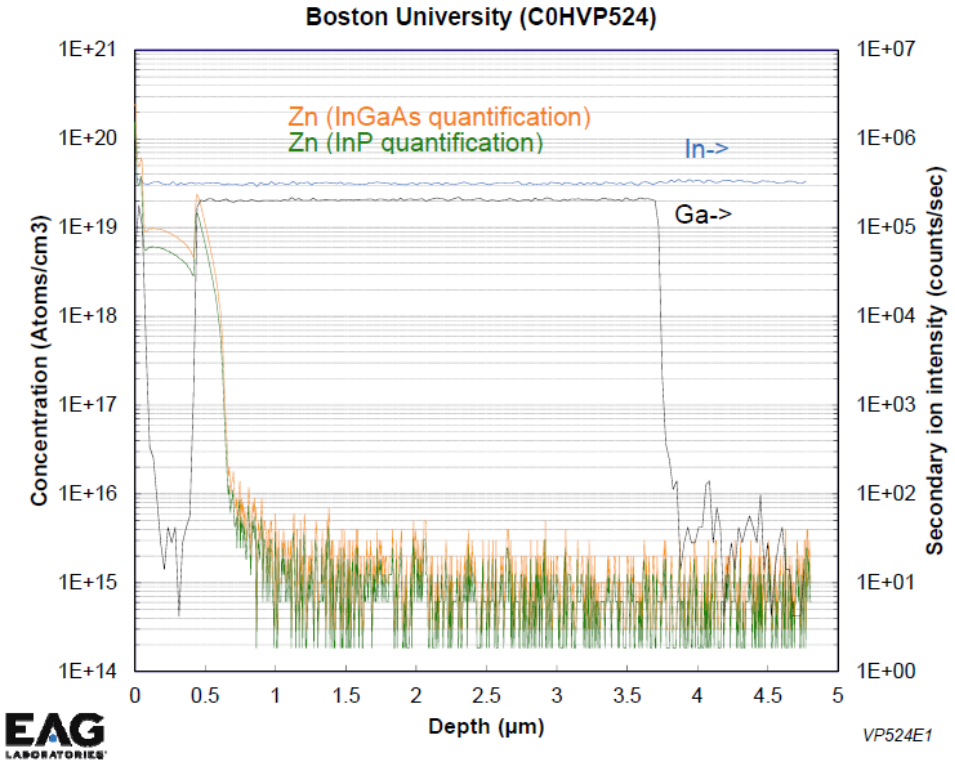

Figure 15: Measured SIMS profile of diffused zinc in InP and InGaAs

4.3. Mask Designs

We have designed three masks to be used within this project. The first designated M1, shown in Figure 16 includes a number of test structures intended to evaluate the contact performance and diffusion properties. The test structures include, guarded and unguarded diodes, CTLMs, minority carriers' diffusion length measurement structures, and alignment keys. The second mask, designated M2, shown in Figure 17 is used to fabricate both passivated and un-passivated diodes and mini arrays. Since the expected dark current of a single diode is expected to be of the order of femto-amperes per pixel, a possible way of testing the operation of the array is to string together a linear array of diodes all connected in parallel so that there summed current is large enough to measure. We have chosen to connect pixels diagonally with interleaved strings that are connected to independent contacts. This makes it possible to treat one string as a set of sensing diodes and the two adjacent ones as the DCJs. The only possible alternative to this arrangement

is to hybridize the mini-array to a ROIC. Strings contain a variable number of detectors, as a results it is possible to determine if the dark current scales with the number of diodes and it is reproducible string by string. It is also important to realize that even if only one of the diode manifests with a large dark current, or is shorted, then the entire string is no longer useful.

Figure 16: Test structures mask M1

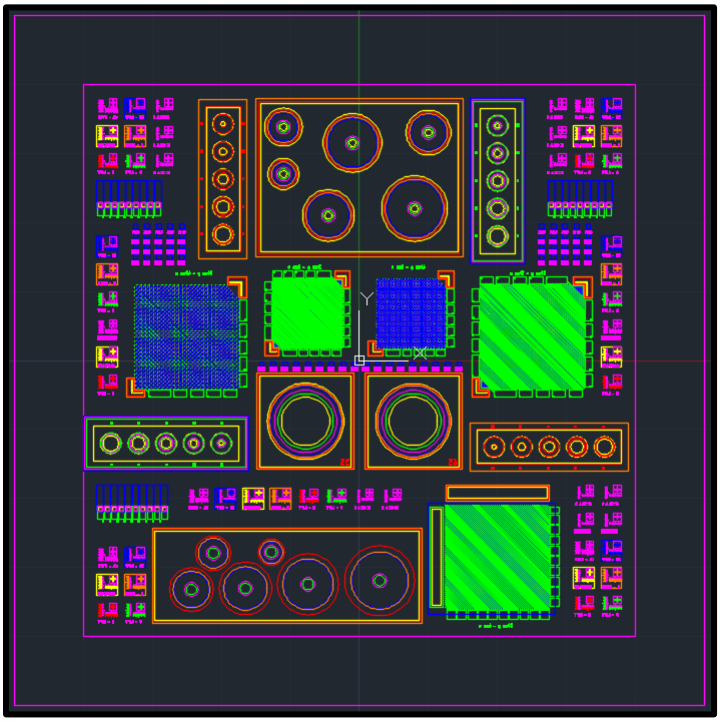

Figure 17: Mask with diodes and mini-arrays M2

As it can be seen in Figure 17, the second mask contains five different arrays. Four are conventional 50 x 50 pixel arrays with variable pitch and diffusion size. The fifth array has an annular DCJ structure as presented in section 2.3 to mimic what was used in simulations. Finally, a third mask set, M3, was also created, and is a variation of the one in Figure 17 in which the positioning of the arrays has been optimized to try to improve the yield.

5. Device Characterization

A total of eight fabrication runs have been performed so far resulting in three operational devices/arrays sets. The fabricated device were: one side piece with incomplete mask M2 that was fully characterized, two successful center pieces with complete mask M2 that have been fully characterized, two center pieces with complete mask M2 that were lost due to failed SiO_2 diffusion barrier removal, one center piece with complete mask M3 that were lost due to failed diffusion process caused by the need to recalibrate the process at Harvard CNS, and one complete center piece was lost due to mechanical failure after it was completed. We are currently completing the fabrication of the last three center pieces of the first wafer. Figure 18 shows one of the completed chip that have been extensively tested. Both standalone diodes and arrays have been characterized using a semiconductor parameter analyzer HP4145B and the I-V characteristics measured. To determine the real dark current values, it is necessary to remove all sources of light from the probe station. Since this is not always possible we will present the measure I-V characteristics in case of illuminated devices and in almost-dark conditions, in which the probe station is covered to eliminate the majority of visible light. While, this cannot be considered a true dark current measurement, the measured I-V characteristics approximate the dark operating condition.

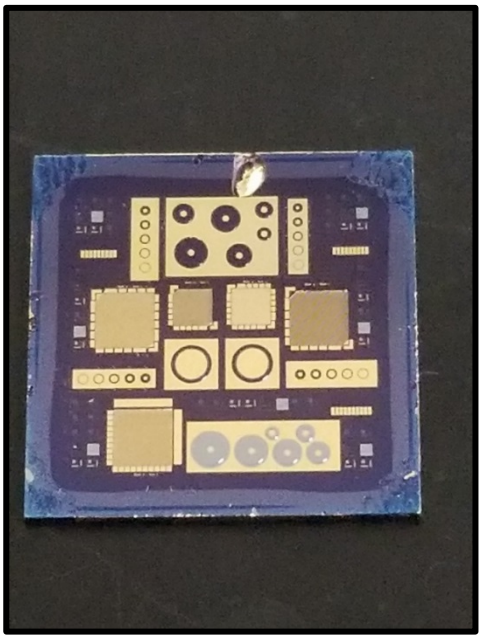

Figure 18: Completed chip ready to be characterized.

5.1. Large Area Diodes

Figure 19 shows where the two large area diodes, with a junction diameter of 1mm, are located on the die. Figure 20 presents the measured illuminated and dark I-V characteristics of large area diodes. The diodes are illuminated simply by using the fluorescent lamp attached to the probe station microscope. The dark measurement is performed by tuning off the lights and covering the probe-station. The diodes exhibit rectifying behavior, indicating successful junction formation.

Furthermore, the behavior of the reverse bias current seems to indicate the presence of a generation-recombination contribution to the dark current. The measured dark current density for these diodes is approximately 25.5µA cm^{-2} that is several order of magnitude higher than the state of the art for this technology.

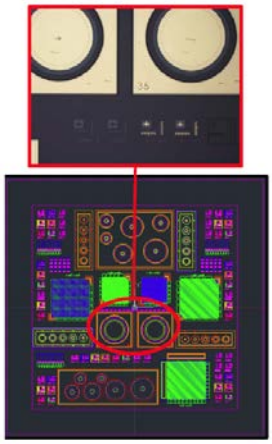

Figure 19: Location of the large area diodes

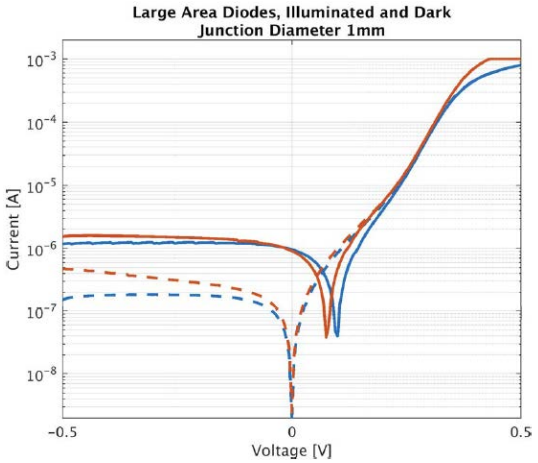

Figure 20: Measured illuminated and dark I-V characteristics of large area diodes.

5.2. Passivated and Un-passivated Variable Area Diodes

Figure 21 shows where the passivated and non-passivate variable area diodes are located on the die. The diodes have junction radii between 150µm and 400µm. The measurement of the I-V characteristics have been performed in dark conditions, for which the microscope lights are turned off and the probe station covered. Nevertheless, some light still reaches the detectors. Figure 19 presents the measured I-V characteristics of the passivated and un-passivated variable area diodes before annealing. It appears that the passivation is effective at suppressing the generation-recombination contribution to the dark current and as a result it may be possible to

resolve the diffusion component. Furthermore, the open-circuit voltage is not centered at zero, indicating that we are not measuring the true dark current. Unfortunately, it appears that the dark current does not have any dependence on junction area. Figure 20 presents the measured I-V characteristics of the passivated and un-passivated variable area diodes post-annealing. It appears that due to the annealing, the dark currents of both set of diodes increases. While for the un-passivated diodes the reverse bias current seems to be diffusion limited, for the passivated diodes, the reverse bias current drastically increases and becomes dominated by a generation-recombination contribution. We are currently working on identifying which process step is the cause for this behavior.

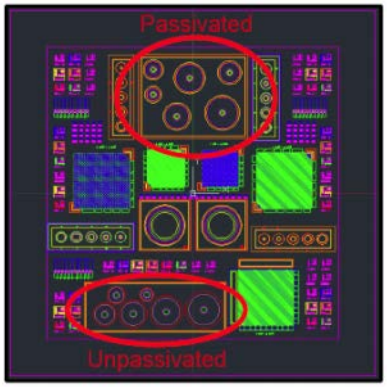

Figure 21: Location of the passivated and un-passivate variable area diodes.

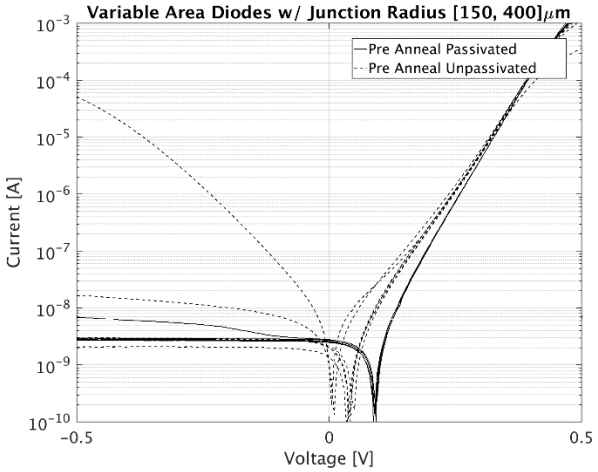

Figure 22: Measured I-V characteristics of the variable area diodes before annealing.

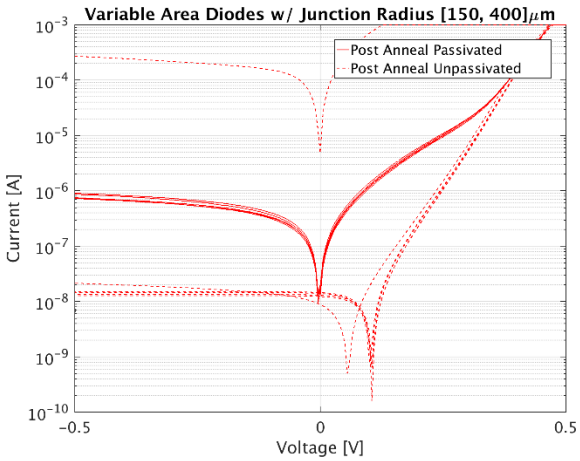

Figure 23: Measured I-V characteristics of the variable area diodes before annealing.

5.3. Array Characterization.

We have measured the I-V characteristics of the mini arrays on the chip that have organized in a square configuration of 50 x 50 pixels, for a total of 2500 diodes. We find that the mini-arrays fabricated on pieces coming from the center of the wafer have a much better yield, resulting in almost full operation of the strings. We have tested each string by connecting the one terminal of the semiconductor parameter analyzer to the corner common contact and one the string pads. Figure 24 presents the location of the arrays hat have been characterized and, in particular the ones for which we analyze the values obtained. Specifically, we have measured the I-V characteristics of four arrays: two a small-pitch arrays and two with large-pitch. Additionally, we compute the average current per pixel for each diode string by diving the total current measured by the number of pixel in the string. In both cases we consider the values measured for a reverse bias voltage of 500mV.

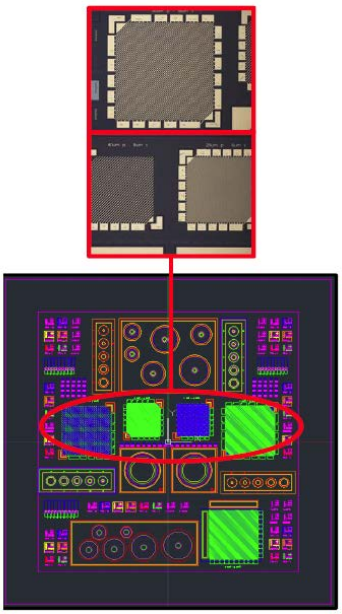

Figure 24: Location of the arrays that have been characterized.

In the case of large pitch array, from the results presented in Figure 25 we observe a significant variance of the dark current per pixel. Furthermore, as observed before, the post-annealing currents are consistently higher than the ones measured before annealing. Post-anneal dark currents increase by about an order of magnitude. This clearly indicates that while some strings may have diodes with equally good performance, other may have uniformity issues, possibly due to edge effects. Assuming a 1nA average dark current, we obtain a dark current density of 111.1 $\mu A / cm^2$ and ~27.8 $\mu A / cm^2$ for arrays with and without DCJs respectively. The current density increases with DCJ since effective pitch decreases without lowering dark current.

In the case of small pitch arrays the situation improves drastically, as shown in Figure 26. The measured currents scale with the number of diodes in the string, indicating an improvement in diode uniformity. As already noted, the post-anneal dark currents increase by about an order of magnitude. With average dark current of 0.5nA per pixel, we obtain a dark current density of ~12.5 μAcm^{-2} and ~3.1 μAcm^{-2} for arrays with and without DCJs respectively. These current are significantly larger than the ones measured for state of the art arrays

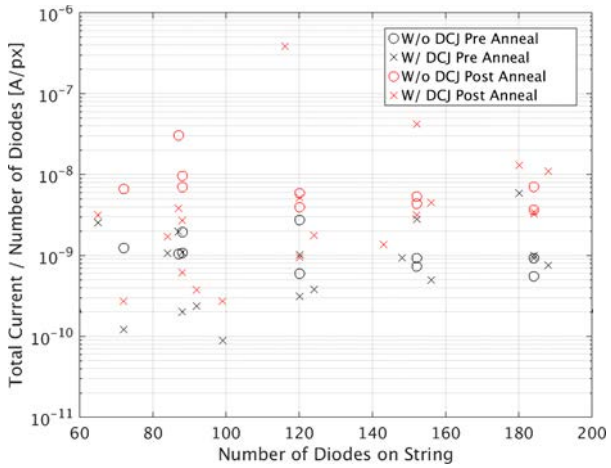

Figure 25: Measured dark current per pixel as a function of the number of pixels in a string for a large pitch array.

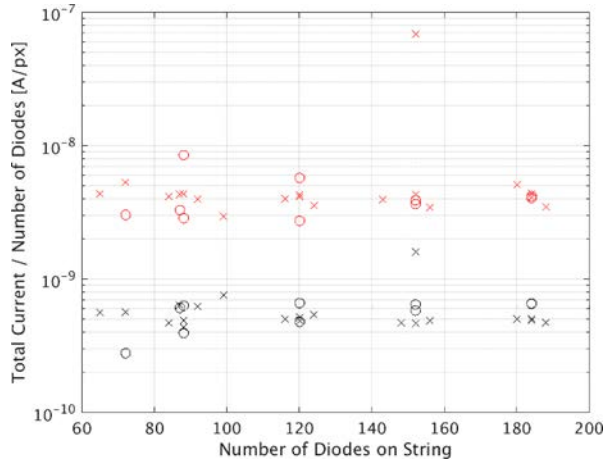

Figure 26: Measured dark current per pixel as a function of the number of pixels in a string for a small pitch array.

Lastly, we have attempted to show the presence of the DCJ effect sweeping the voltage on one string of diodes, and sensing the current out of its neighboring string. This arrangement is presented in presented in Figure 24. To perform this measurement, we apply a constant reverse bias the center string (second from the top in Figure 24) and sweep the reverse bias on the DCJ strings (first and third from the top). In Figure 25 and Figure 26, the red-dashed line represents the base case where the DCJ string is left floating, and we measure a constant current. The black lines are the measured current while sweeping the DCJ array. When forward biased, there is a sharp increase in dark current in the sensing array, as expected. Unfortunately, under reverse bias there is no indication of reduction in dark current

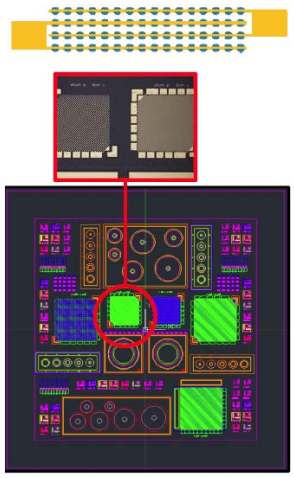

Figure 27: Device configuration used to test if the DCJ effect is present.

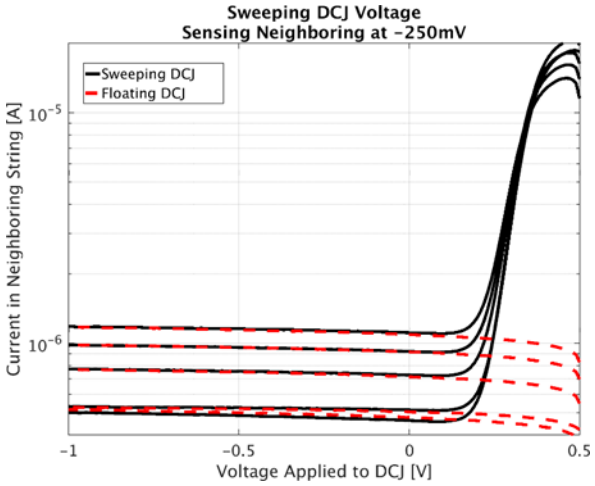

Figure 28: Measured dark current per pixel as a function of applied DCJ bias.

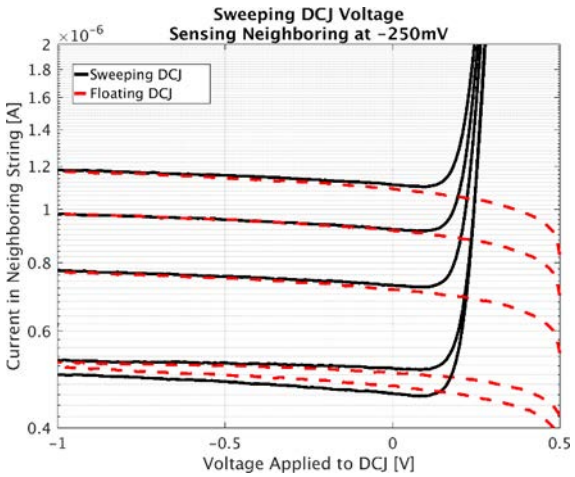

Figure 29: Measured dark current per pixel as a function of the applied DCJ bias.

6. Conclusions

Through the course of the program we have developed a fabrication procedure for SWIR InGaAs photodetectors, and attempted to demonstrate a new pixel architecture that can be used to lower the dark current, and hence, improve the sensitivity of existing devices. To support the fabrication process, a significant number of finite-element simulations were performed to try to better understand the underlying physics. Through this modeling effort, we demonstrated that a more symmetric annular control junction provides the highest degree of dark current suppression, but at a greater loss of quantum efficiency. We also provided evidence that this lost QE can be recovered through the use of microlens arrays, which are already used in photodetecting arrays today. Future work on the modeling will include additional simulations on optimizing the control junction structure in terms of detectivity and crosstalk.

At the time of writing this report, the characterized arrays do not demonstrate a noticeable degree of dark current suppression when biasing neighboring junctions. However, the results also indicate remaining issues with the device fabrication process. The isolated diodes, arrays, and variable area diodes all have extremely high dark currents, exhibited increased dark current with the contact anneal, and do not vary with junction area. All of these symptoms are inconsistent with what can be expected for p-n junctions formed in SWIR InGaAs using the double layer planar heterostructure. More work is required to determine the cause of these problems.

While the devices fabricated at Boston University do not demonstrate the DCJ effect, we are confident that our simulations are accurate, and that the problem lies with the process. In an effort to prove this, we will continue this work outside of this program and update the participating parties (AFRL, DARPA, and ARL) with any new findings.

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List of Symbols, Abbreviations, and Acronyms

AFRL	Air Force Research Laboratory
ARL	Army Research Laboratory
BU	Boston University
BU-OPF	Boston University Optoelectronics Fabrication Facility
DARPA	Defense Advanced Research Projects Agency
DCJ	diffusion control junction
DLPH	double layer planar heterojunction
E-SWIR	extended short wave infrared
FPA	focal plane array
Harvard-CNS	Harvard Center for Nanoscale Systems
HF	hydrofluoric acid
I-V	current-voltage
MCT	HgCdTe
MW	mid-wavelength
QE	quantum efficiency
ROIC	read out integrated circuit
RXAN	Nanoelectronic Materials Branch, Functional Materials Division, Materials and Manufacturing Directorate
SIMS	secondary ion mass spectroscopy
SWIR	Short wavelength infrared