Relating Silicon Carbide Avalanche Breakdown Diode Design to Pulsed-Energy Capability

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Abstract: *Silicon carbide avalanche breakdown diodes (ABDs) were fabricated with different P^+ implant depths, drift layer thicknesses, and doping concentrations. ABDs from 4 different designs, having breakdown voltages near 1 kV, were pulse tested in an inductive load circuit at peak powers of over 110 kW. Total pulsed-energy dissipation was kept nearly the same among the ABDs for a defined pulse subinterval. Results of the pulsed-current tests are presented and conclusions are drawn from comparisons of the ABD clamping voltages about which design provides the highest pulsed-energy capability.*

Keywords: Avalanche; Breakdown; Diode; Silicon Carbide

Introduction

Four avalanche breakdown diode (ABD) designs having different P^+ implant depths, and different drift layer thicknesses and doping concentrations were fabricated in silicon carbide (SiC). The ABDs were designed to have breakdown voltages near 1 kV, to protect 1.2-kV rated transistors during fast turn-off transitions. The repetitive pulsed performance of ABDs from one of these designs was previously reported [1]. A total of 6 ABDs from the 4 different designs were pulsed with avalanche current at peak power levels of over 110-kW in an inductive-load circuit to compare their clamping-voltage responses [2]. The total pulsed energy dissipated in each ABD was kept approximately the same over a selected subinterval of each pulse. Reaching nearly the same energy among the ABDs was complicated by their different breakdown voltages, and was achieved by tuning circuit operating parameters specifically for each ABD. The focus of this paper is to present results from pulsed-current tests of the 4 ABD designs and to draw conclusions from their clamping voltage waveforms about which design provides the highest pulsed-energy capability.

ABD Design Parameters

Figure 1 shows a cross-sectional diagram of the ABD structure. Table 1 shows parameters and resulting nominal breakdown voltages of the 4 SiC ABD designs. N-type epitaxial layers of 5-µm, 5.5-µm, and 6-µm were grown on the Si-face of a 4-degree off-cut, 350-µm thick, N^+ 4H-SiC substrate. The 5-µm layer had a doping concentration of 1.3×10^{16} cm^{-3}, and the 5.5-µm and 6-µm layers had doping concentrations of 1.6×10^{16} cm^{-3}. The P^+ anodes were formed by aluminum implantation. Figure 2 shows doping concentration as a function of depth for the three different implant profiles used. Although the three implants have the same peak doping concentration, they have different depths, characterized as deep, medium, and shallow. The implants were annealed at approximately 1600 °C. Ni-based ohmic contacts were formed on the anode P^+ implants, and on the backside of the N^+ substrate, which serves as the cathode of the ABD. A 4-µm Al layer was deposited and patterned for the top anode electrode, and a Ti/Ni/Au layer was deposited on the backside for the cathode electrode. The die size was 3.4 mm × 3.4 mm, with an active area of approximately 0.09 cm^2.

Each ABD was solder bonded and wire bonded into an open-cavity TO-247 package and encapsulated with dielectric gel. A curve tracer was used to record ABD breakdown voltages at 100 µA, before pulse testing. By heating the ABDs, a positive temperature coefficient of breakdown voltage was measured between 25 and 150 °C. The coefficient was measured to be 176 mV/°C, for all ABDs.

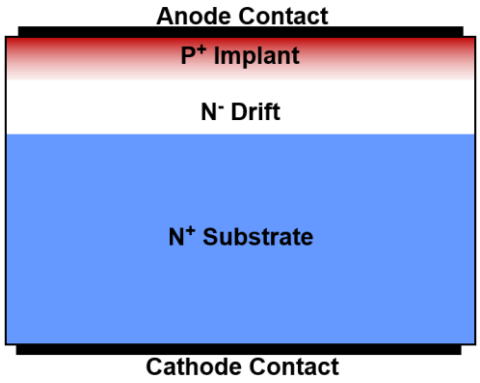

Figure 1. Cross section of the ABD design

Table 1. Design parameters of 4 different SiC ABDs

ABD design split #	Drift thickness (µm)	Drift doping (cm^{-3})	P^+ implant profile	V_{BR} nom. at 100 µA (V)
1	5	1.3×10^{16}	deep	950
2	6	1.6×10^{16}	deep	1050
5	5.5	1.6×10^{16}	medium	1020
8	5.5	1.6×10^{16}	shallow	1040

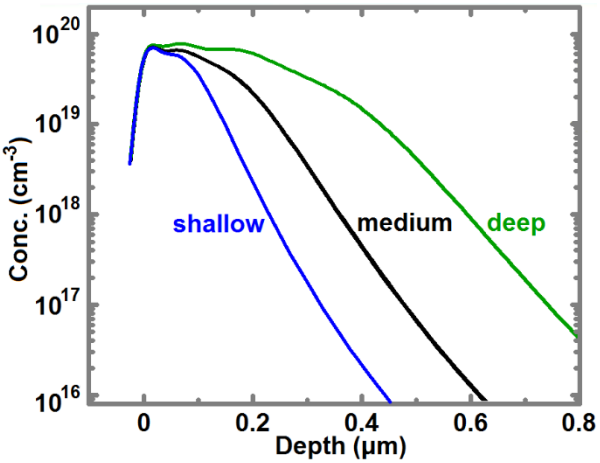

Figure 2. ABD P^+ implant profiles

Pulsed-Current Evaluation

The ABDs were evaluated in a pulsed-inductive-load circuit. The schematic of the circuit is shown in figure 3. Component values of 2 kΩ, 90 μF, and 24 μH were used for *R*, *C*, and *L*, respectively. With the capacitor charged by the DC supply, the IGBT is pulsed to the on-state to ramp up inductor current. The IGBT is then turned off, and the inductor current ramps down through the ABD under avalanche breakdown. The 6 ABDs evaluated consisted of two parts from design 1, two parts from design 2, and one part each from designs 5 and 8. The capacitor voltage and the inductor charging time, were adjusted for each ABD to control the peak avalanche current and its negative slope. These parameters allowed nearly 223 mJ of energy dissipation to be reached in a 2.7-μs subinterval in the ABDs; despite their range of breakdown voltages.

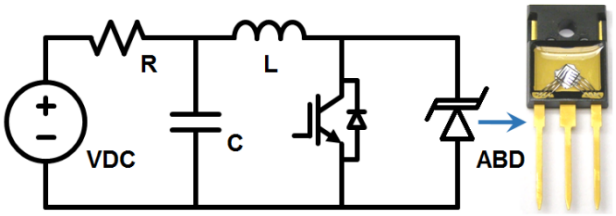

Figure 3. Pulsed-inductive-load circuit and packaged ABD

Figure 4 shows captured pulse waveforms for an ABD from design 1 (1 μs/div.). Channels 2 and 3 show the test-circuit IGBT-emitter current (20 A/div.) and the ABD avalanche current (20 A/div.), respectively. Channel 4 shows the ABD clamping voltage (20 V/div.) with a 900-V offset. Math channel 1 shows the calculated ABD energy dissipation during the pulse (50 mJ/div.). Figures 5(a)-(c) show captured pulse waveforms for an ABD from designs 2, 5, and 8, respectively. Due to their higher avalanche voltages, the offset of channel 4 is 1000 V in each plot, with the same scaling as figure 4. Because pulsing of the second diode from designs 1 and 2 produced nearly identical results for each design, only the four ABD clamping waveforms shown in figures 4 and 5 are analyzed and compared.

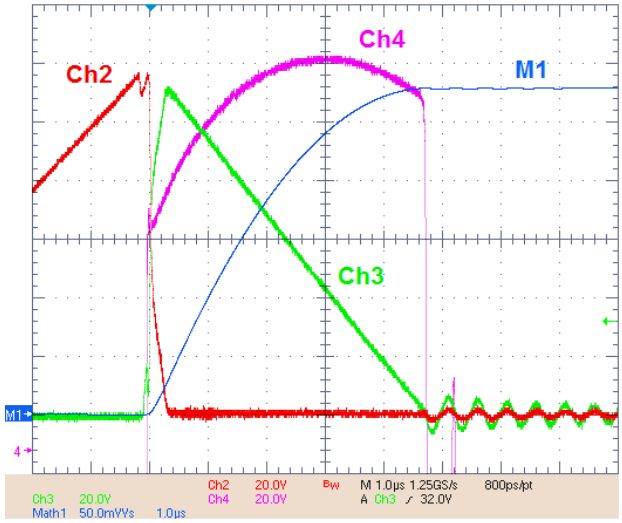

Figure 4. Pulsed response for ABD design 1 (1 μs/div.); Ch2, IGBT current (20 A/div.); Ch3, ABD avalanche current (20 A/div.); Ch4, ABD clamping voltage (20 V/div. with 900-V offset); M1, ABD energy dissipation (50 mJ/div.)

In figure 4, as the avalanche current peaks at 112 A, the clamping voltage reaches 989 V, which is 38 V above the 951-V ABD breakdown voltage (measured at 100 μA). The additional clamping voltage is attributed to the ABD resistance and the resistance of the device package and connections. The clamping voltage rises with the current, and continues to rise following the current peak of 112 A, as energy continues to be dissipated in the ABD, and its temperature rises. The clamping voltage reaches 1033 V, 2.7 μs from the start of the pulse. After 3 μs, the voltage begins to fall as heat diffuses within the ABD. Thermal calculations of heat spreading within the ABD have shown that the temperature rise at the backside of the die, closest to the package heat spreader, is less than 1 °C at 10 μs from the start of the pulse [1]. Because all pulse widths in this evaluation are less than 5 μs, heating is confined to the ABD die during the pulse, with negligible heat spreading into packaging materials.

In figure 5(a), the clamping voltage of the ABD from design 2 rises to 1095 V at its 103-A current peak. This is 46 V above the 1049-V breakdown measured at 100 μA. At 2.7 μs the clamping voltage is at its peak of 1139 V. In figure 5(b), the ABD from design 5 has a clamping voltage of 1081 V at a peak current of 104 A. This is 58 V above its breakdown voltage of 1023 V at 100 μA. At 2.7 μs, the clamping voltage is past its peak value of 1115 V and is 1112 V. Finally, in figure 5(c), the clamping voltage of the design 8 ABD is 1112 V at the 102-A current peak, which is 72 V above its 1040-V breakdown at 100 μA. At 2.7 μs, its clamping voltage is also past its peak value of 1145 V and is 1143 V. Table 2 summarizes the measured clamping voltage values from the ABDs, listed by design number. Also listed are the differential resistances (R_D), calculated from the breakdown voltage to the clamping voltage at peak current as shown in equation 1, the peak clamping voltage up to 2.7 μs (V_{CPK}), and the energy (E) measured 2.7 μs from the start of each pulse.

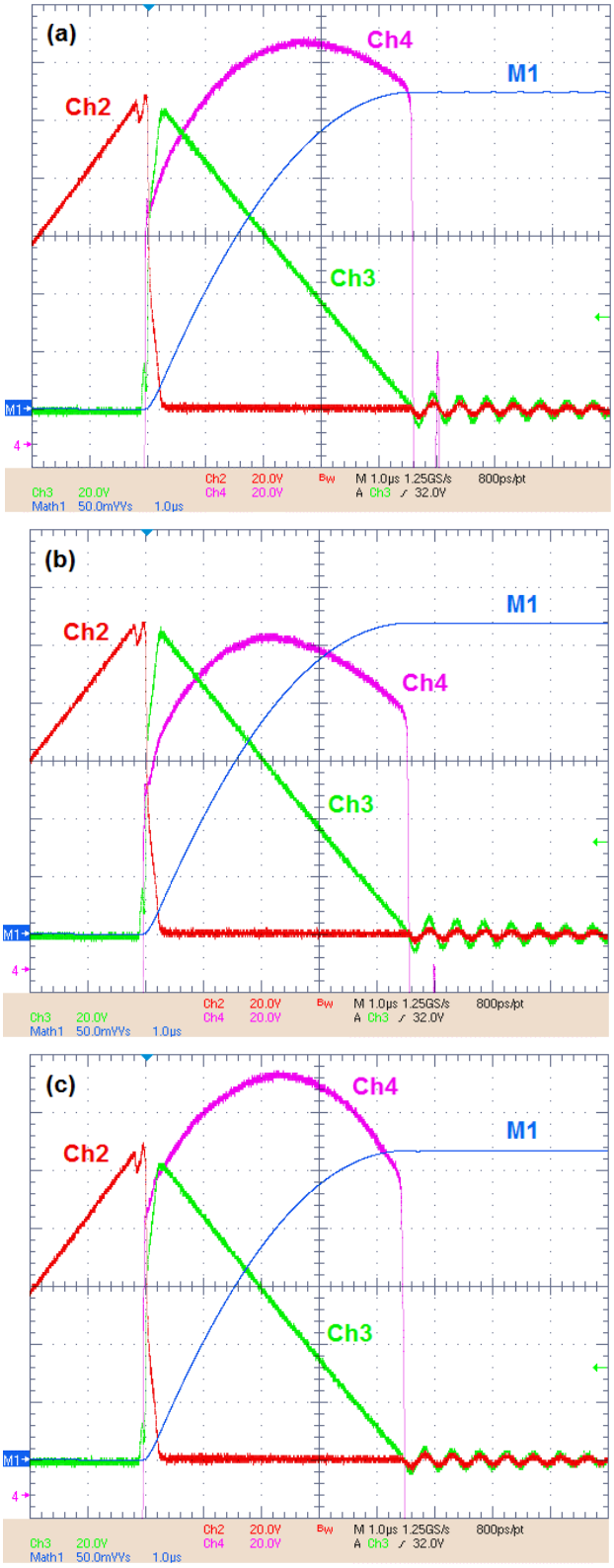

Figure 5(a)-(c). Pulsed responses for (a) design 2, (b) design 5, and (c) design 8 ABDs (1 µs/div.); Ch2, IGBT current (20 A/div.); Ch3, ABD avalanche current (20 A/div.); Ch4, ABD clamping voltage (20 V/div. with 1000-V offset); M1, ABD energy dissipation (50 mJ/div.)

Table 2. Measured and calculated ABD pulse-test data

ABD	V_{BR} (V)	V_C at I_{PK} (V, A)	R_D (Ω)	V_{CPK} to 2.7 µs (V)	E at 2.7 µs (mJ)
1	951	989, 112	0.34	1033	224
2	1049	1095, 103	0.45	1139	225
5	1023	1081, 104	0.56	1115*	223
8	1040	1112, 102	0.71	1145*	223

*Peak clamping voltage occurred before 2.7 µs.

$$R_D = \frac{(V_C \text{ at } I_{PK}) - (V_{BR} \text{ at } 100\ \mu A)}{I_{PK}} \quad (1)$$

Analysis of Results

The increases in clamping voltage during pulsing are attributed to ABD resistance and ABD heating from energy dissipation. Because only a small fraction of the total energy dissipation occurs before the peak avalanche current is reached, the increase in clamping voltage, over the 100-µA breakdown voltage, is mostly due to ABD resistance and resistance associated with packaging. The ABDs with higher design numbers have higher resistances, with ABD 8 having over twice the differential resistance of ABD 1. This is partly because ABD resistance is directly related to drift-layer thickness, and ABD design 1 has the thinnest drift layer of 5 µm. Also, ABD design 1 has a lower drift-layer doping level than the other designs (1.3×10^{16} vs. 1.6×10^{16} cm^{-3}), which may provide marginally lower resistance by reducing the scattering of carriers during avalanche. ABD 2 had the highest breakdown voltage, which can be attributed to its design having the thickest drift layer (6 µm). However, ABD 2 had a lower resistance than ABDs 5 and 8, despite their slightly thinner 5.5-µm drift layer specification.

The pulse data indicate that P^+ implant depth is the most significant driver of ABD resistance in this design comparison, and that resistance is inversely related to implant depth. Designs 1 and 2 had the deepest implants and exhibited the two lowest resistances during pulsing. ABD design 8 had the shallowest implant and showed the highest resistance; and design 5 had an implant depth and resistance between those of ABDs 2 and 8. The higher resistances of ABDs having shallower implants is attributed to higher P-type contact resistances due to lower implant doses.

Thermal modeling has shown that heat is confined to the ABDs during these short pulses. In this evaluation, their clamping voltage waveforms may indicate on a relative basis how heat is distributed in the die. Because energies were kept nearly equal among the ABDs at 2.7 µs from the start of each pulse, and energy dissipation is largely dependent on clamping voltage, clamping-voltage amplitude is not a good discriminator of peak ABD temperature. However, the time intervals to the peaks of the clamping-voltage waveforms may indicate which die have

steeper temperature gradients and have higher peak temperatures. ABDs 1 and 2 reached their peak voltages at or after 2.7 μs, and ABDs 5 and 8 reached their peak voltages before 2.7 μs. This may indicate that ABDs 5 and 8 reached their peak temperatures sooner than ABDs 1 and 2. In turn, this implies that ABDs 5 and 8 had less heat spreading within the 2.7-μs interval, and therefore had higher temperature gradients and higher peak temperatures than ABDs 5 and 8.

Faster heating rates and higher peak temperatures can also be attributed to higher contact resistances. Although approximately the same amount of energy was dissipated in each ABD, greater portions of that energy may have been concentrated near the anode contact for ABDs 5 and 8.

Conclusion

Four SiC ABD designs were fabricated with different combinations of drift layer thickness, drift doping, and P^+ implant depth. The ABDs were pulse tested in an inductive-load circuit at over 100-A peak, resulting in peak power levels of over 110 kW. Clamping-voltage responses of the ABDs were compared to relate resistive and thermal characteristics to the ABD design parameters, and to determine which design parameters may provide the highest pulsed-energy capability.

The differences between clamping voltages at peak pulse currents and at breakdown showed that ABD differential resistances were most significantly inversely related to P^+ implant depth. The higher resistances of the ABDs with shallower implants is attributed to higher anode-contact resistances. By reaching peak clamping voltages earlier in their pulses, ABDs having shallower implants are believed to have higher temperature gradients and higher peak temperatures. This is attributed to a larger concentration of energy dissipation near the anode contact.

The fabrication of SiC ABDs with deep P^+ aluminum implants is believed to improve ABD performance, reliability, and pulsed-energy capability. Lower ABD resistance gives lower clamping voltage at a given avalanche current, improving ABD performance. A lower clamping voltage results in lower ABD energy dissipation, which can reduce ABD peak temperature. Peak temperature is also reduced by distributing energy dissipation more uniformly in the ABD. By reducing peak temperatures, improved ABD reliability can be realized or traded for higher energy-dissipation capability.

References

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