Analog 65/130 nm CMOS 5 GHz Sub-Arrays with ROACH-2 FPGA Beamformers for Hybrid Aperture-Array Receivers

Viduneth Ariyarathna [1], ***Nilan Udayanga*** [1], ***Arjuna Madanayake*** [1], ***Leonid Belostotski*** [2], ***Peyman Ahmadi*** [2], ***Soumyajith Mandal*** [3], ***Ali Nikoofard*** [3]

[2]Department of Electrical and Computer Engineering, University of Akron, Akron, OH.

[1]Department of Electrical and Computer Engineering, University of Calgary, Calgary, AB T2N 1N4, Canada.

[3]Case Western Reserve University, Cleveland, OH, USA.

Abstract: Analog-digital hybrid aperture array receiver is proposed towards reducing the analog-to-digital converters (ADC) power consumption and circuit complexity of a fully digital array. Proposed system consists of a Nyquist sampled analog sub-array (level-1) followed by an undersampled digital beamformer (level-2). Two alternatives for the level-1 analog sub-array are discussed. In the first approach, a voltage-controled all-pass filter is realized using 130 nm CMOS technology and having more than 5 GHz bandwidth, is used as the true-time delay element to obtain electronically steerable analog beams. Prototype radio frequency integrated circuit (RF-IC) implementation of a 4-element wideband analog sub-array, which is based on all-pass filters (APFs) is realized using 130 nm CMOS technology. Approximate-discrete Fourier transform (a-DFT) algorithm based multi-beam architecture is proposed as the second approach for the level-1 analog sub-array. An 8-point a-DFT multi-beam array using 65 nm CMOS technology supports 4GHz of bandwidth. The level-2 digital beamforming occurs in the ROACH-2 FPGA platform. Array factor measurements are provided for several frequency and beam direction combinations.

Introduction

Wideband optimal array processing [1] is an important requirement in wireless communications, radio astronomy, microwave imaging, radar and electronic signal intelligence. Particularly in dense aperture array receivers, the presence of a very large number of antenna elements (hundreds/thousands) requires careful trade-offs between circuit complexity, power consumption, performance, size, weight, reliability and cost. In general, a fully digital array having a dedicated receiver chain and data converter for every element offers the most flexibility. However, such a scheme can be costly, prohibitively complicated and high in power consumption. A purely analog RF-IC solution offers the lowest power consumption but is difficult to implement for large numbers of elements. Interestingly, analog-digital hybrid architectures allow the best of both worlds [2], [3].

This paper presents our progress with the design, implementation and test of a reconfigurable and software-defined wideband array receiver based on analog-digital hybrid array processing [4], [5]. The array processor consists of a wideband front-end, tunable wideband true-time delay and analog beamformers (ABFs), that are realized using CMOS custom integrated circuit designs. Both the analog front-ends as well as the beamformers operate on a sub-array consisting of wideband antenna elements organized in a uniform linear array (ULA) configuration. Each output of the ULA sub-array is digitized and subsequently applied to a array processor implemented using a field-programmable gate array (FPGA) on the open-source reconfigurable open architecture computing hardware-2 (ROACH-2) platform [6].

Proposed Analog-digital Hybrid Beamforming Architecture

Consider an N-element antenna array consisting of M number of L-element analog sub-arrays as shown in Fig. 1(a), where $N = ML$. Inter antenna spacing $\Delta x = \frac{\lambda_{min}}{2}$, where λ_{min} is the wave length corresponds to the maximum frequency that the analog sub-array can handle without grating lobes in the array factor, where c is the wave speed. Proposed two-level hybrid beamforming architecture consists of an analog sub-array at level-1 (L-element analog beamformer) followed by an undersampled M-element digital beamformer at level-2, which is fed by the beamformed outputs of the analog sub-arrays (there are M sub-arrays). The effective inter-element spacing of the digital beamformer is $L\Delta x$. The number of digital receivers and data converters have reduced from N to M as a result of adopting the analog-digital hybrid architecture. This leads to simplified data communication overheads, lower ADC power consumption and lower complexity of the total system, compared to a fully digital array.

We propose two alternatives for the level-1 analog sub-array beamforming stage, as shown in Figs. 1 (b) and 1(c). First approach is to implement the level-1 analog sub-array using tunable wideband analog delays, which leads to a wideband beamformer. Here, an analog APF [7], [8], which has more that 5 GHz of bandwidth, is employed as the true time delay element. Delay of each element is tunable through a control voltage. Second approach is to employ an analog multi-beamformer, where multiple simultaneous fixed beams are directed at known directions [9]. The proposed approximate-discrete Fourier transform (a-DFT) based multi-beamformer [9] yields L independent radio frequency (RF) beams for an L element array. The subsequent level-2 beamforming

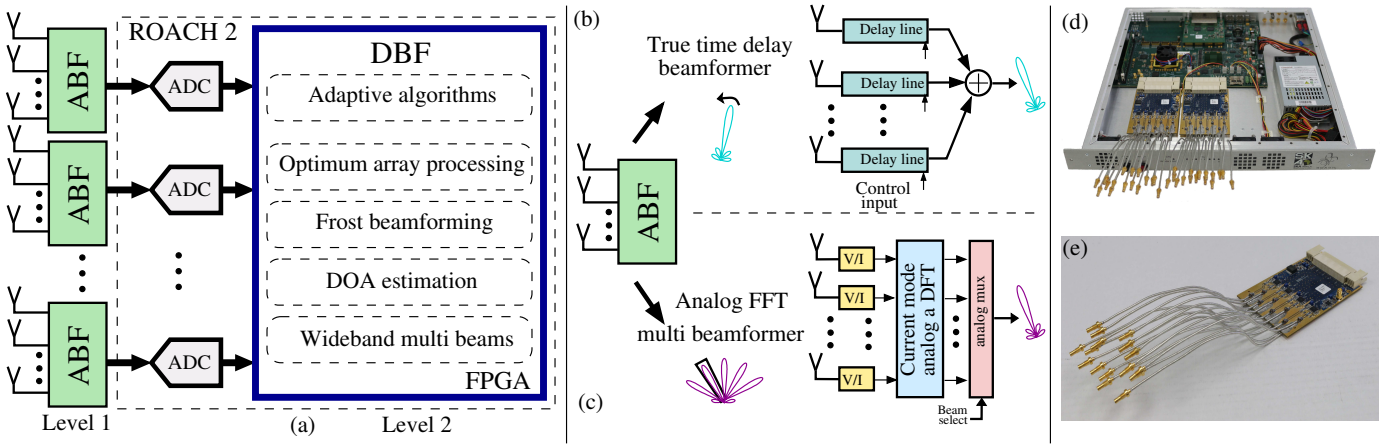

Fig. 1. a) Top level architecture for the proposed system; b true-time delay-sum and/or c) DFT-based multi-beam sub-array based analog beamforming options at level-1; (d) ROACH-2 platform; (e) upto 1 GHz analog to digital conversion daughter board.

occurs in the discrete time domain (in ROACH-2 FPGA platform) following signal digitization (see Figs. 1(d) and 1(e)). Subsequent digital receivers and processing algorithms allow optimal wideband beamforming including adaptive algorithms to be applied to the sub-array signals.

Level-1 Analog Sub-Array Beamformer

Analog Sub-array Approach 1 - Wideband True-time Delay Beamformer: Consider a plane wave impinging on the L-element sub-array from a direction of arrival (DOA) ψ, where the angle is measured in clockwise direction to the array broadside. The time that the plane wave takes to travel from an antenna to its neighboring antenna is given by $\tau = \frac{\Delta x}{c} \sin\psi$. Thus, the steering delay vector $\mathbf{S}$ that requires to enhance signals from the DOA ψ can be expressed as $\mathbf{S} = \left[1, e^{-j\omega\tau}, \ldots, e^{-j(L-2)\omega\tau}, e^{-j(L-1)\omega\tau}\right]$, where ω is the temporal frequency. The analog delay τ can be approximated using an APF which is having an approximate frequency domain representation $e^{-j\omega\tau} \approx \left(\frac{1-j\omega\tau/2M}{1+j\omega_t\tau/2M}\right)^M$, $M \in \mathbb{Z}^+$. In this paper, we propose to use an APF which is realized using 130 nm CMOS technology and capable of tuning the group delay τ up to a range of 82 ps using a control voltage. Voltage controlled group delay leads to an electronically steerable analog beamformer. The group delay $i\tau$, where $i \in \{2, 3, \ldots, L-1\}$, can be approximated by cascading i number of identical all-pass filters.

The proposed tunable analog RF-IC based delay element has a wide bandwith (up to about 5 GHz) and it enables a voltage controlled delay that can be tuned. The APF used in this work is a differential versions of a current-mode first-order APF described in [10]. The circuit diagram and micrograph of the implemented filter are shown in Figs. 2 (a) and 2(b), respectively. The cross-coupled pair (M2) at the top of the filter reduces the node resistance by generating negative resistance R1, which reduces the required input transistor (M1) transconductance, reduces the filter power consumption, and extends the operating frequency range. Tuning is accomplished by varying bias current with Vbias and the feedback resistance R2.

A 4-element electronically steerable array of antennas was implemented in a 130 nm CMOS technology based on the proposed APF. The circuit included a low-noise amplifier (LNA) followed by a voltage-to-current stage and a cascade of 3 all-pass filters in each branch. The outputs of the APFs were added together with current mirrors. The array was mounted on a PCB and measured in an anechoic chamber as shown in Figs. 2(c) and 2(d). Fig. 2(e) shows measured beampatterns at three different frequencies for different direction of arrivals of the signals.

Analog Sub-array Approach 2 - approximate-DFT (a-DFT) Multi-beamformer: The second analog sub-array approach is to realize simultaneous multiple beams at the level-1 using the a-DFT algorithm, which can obtain L number of narrowband beams directed at known fixed directions using a L-element ULA [9]. The 8-point a-DFT fast algorithm proposed in [11] has been used in [9], to propose an analog RF-IC circuit on TSMC 65 nm technology. The small-integer coefficients $\{0, \pm 1, \pm 2\}$ present in the approximate transform allows analog-IC implementation of the 8-point using current mirrors in current mode. In [9], it has been shown that the 8-point a-DFT based multi-beam array using 65 nm CMOS technology can handle exceeding 4GHz of bandwidth. This enables pontential beamforming of sub-millimeter wave signals having couple of GHz bandwidth using analog circuitry (which will be narrowband signals at those frequencies).

Fig. 3 (a) shows a block diagram of such multi-beamformer having L elements, where an L-point a-DFT operation across the downconverted signals is performed in order to achieve L narrowband beams at fixed directions. An example block-diagram realization of the 8-point a-DFT (given in [11]) using current mode CMOS is shown in Fig. 3(b). The real and imaginary components of the approximate DFT matrix have been realized separately. NMOS and PMOS current copiers are used to achieve small-integer coefficients and the addition/substration operations respectively. Fig.

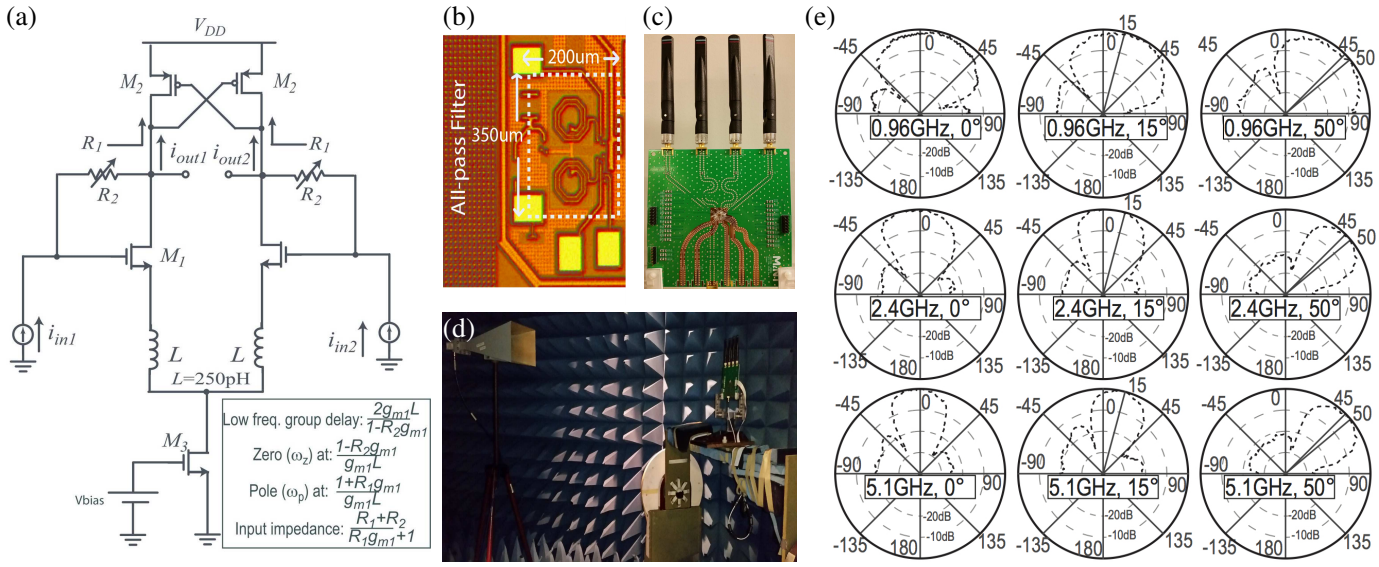

Fig. 2. (a) The circuit diagram of the implemented APF; (b) micrograph of the fabricated filter; the 4-element array and the PCB build using the APFs; (d) setup in an anechoic chamber for obtaining the measurements; (e) measured array factors from the 4-element array.

3 (b-1) shows the low-voltage cascode realization of the NMOS and Fig. 3 (b-2) illustrate an example realization of a PMOS mirror. An example of one row of the 8-point approximate DFT (row 4) is shown in Fig. 3 (b-3). Each fixed analog DFT beam can be connected to the digital beamformer to provide level-2 beamforming. However, instead of tuning a continuously-variable delay, this approach requires an analog switch to connect the required beam that is best suited for a particular scenario. A prototype DFT multi-beam analog realization has been taped-out and submitted for fabrication, and the CMOS layout of the 8-point a-DFT circuit is shown in Fig. 3 (c). The polar patterns obtained from the current mode 8-point DFT approximation circuit on 65nm CMOS using the simulations based on BSIM4 models in Cadence Spectre for input frequencies of 1 GHz and 2 GHz are shown in Fig. 3 (c) and (d), respectively.

Level-2 Digital Beamformer

Second level digital beamforming can be achieved with different methods. Differnt digital filter structures, such as, finite impulse response (FIR) filter approximations, or infinite impulse response (IIR) (e.g. digital realization of the Thiran APF, to approximate the required TTD [12]) filters. The digital beamformer is fed by the beamformed outputs of the analog sub-arrays. Thus, the inputs to the digital beamformer are undersampled by a factor of L, leading to grating lobes in the array factor. Proposed beamformers are realized on the ROACH-2 FPGA platform.

The ROACH-2 is an open source single-FPGA board which was designed for the Square Kilometer Array (SKA) radio telescope project [6] (see Fig. 1 (d)). The platform contains a Xilinx Virtex-6 FPGA that has enough resources to accommodate high complex logic. The PowerPC 440EPx stand-alone processor provides the user to perform control functions with the FPGA registers and facilitate sofware-defined functions. It comprises of 2 multi-gigabit transceivers, to support 4x10Ge links (SFP+) for high-speed communication. ROACH-2 also supports two ZDOk+ interfaces supporting high speed ADCs. The ADC boards can be configured to achieve sampling rates up to 5 GHz using available ADC daughter cards [6].

Narrowband Hybrid Beamforming Example Using Analog a-DFT based Sub-Arrays: To demonstrate the functionality of the hybrid-beamforming architecture, consider a setup having analog 8-point a-DFT sub-array as the level-1 beamforming stage. Thus $L = 8$ and let $N = 4$. If the level-1 sub-array is Nyquist-spaced the individual array-factor of a sub-array will have a beam pattern similar to patterns given in Figs. 3 (c) and (d). The level-1 beamforming stage will have 8 beam outputs and the selected beam from all the sub-arrays are fed to the digital beamforming stage. If the beam number 3 directed at $48.5°$ is fed to level-2, the digital stage is configured with weights to beamform to the same direction and the array factor of the digital stage is shown in Fig. 4 (a). Grating lobes exists due to the equivalent element spacing for the digital beamformer is now $4\Delta x$ if the element spacing of the level-1 sub-array is Δx. Fig. 4 (b) shows the resultant array factor of the two stages obtained using the simulated array pattern at 1 GHz frequency for level-1.

Conclusion

Hybrid beamforming architectures for analog-digital hybrid aperture array receiver have been proposed here for reducing the required number of ADCs in turn reducing the power consumption and the complexity of the beamforming system. Proposed architectures consists of two beamforming stages; an analog sub-array beamforming stage (level-1) and digital beamforming stage (level-2). Two alternative beamforming methods for level-1 analog subarray beamforming methods have been proposed. As the first approach, a TTD beamformer

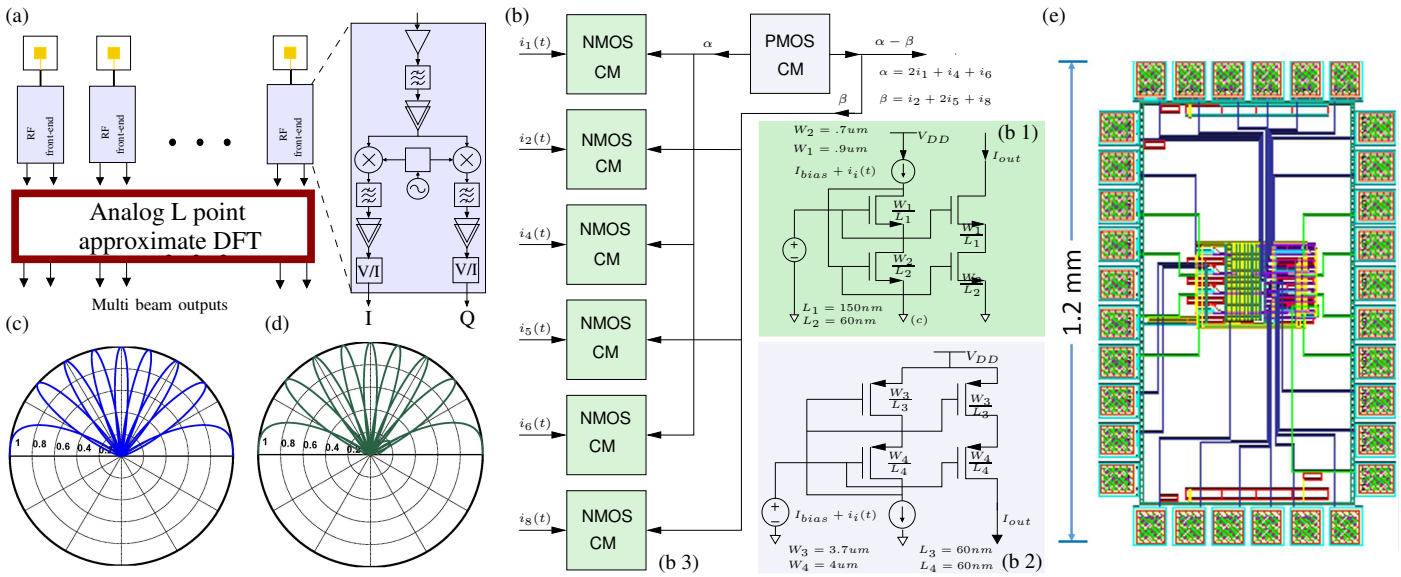

Fig. 3. (a) Beamforming setup using a-DFT to obtain multiple beams in fixed directions; (b) realization of a row of the 8-point a-DFT matrix using current mirrors; polar patterns obtained from the 8-point a-DFT circuit on 65nm CMOS using the BSIM4 models in Cadence Spectre for (c) 1 GHz, (d) 2 GHz signal frequencies; (e) layout of the taped-out analog a-DFT circuit.

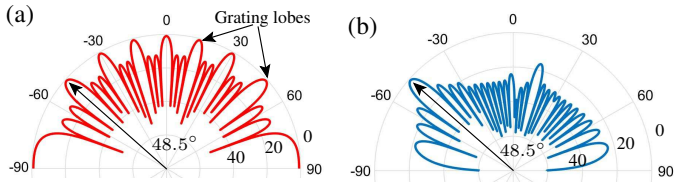

Fig. 4. (a) Individual array factor (in dB) of level-2 beamforming itself for beam number 3 using the 8-point spatial FFT; (b) resultant array factor (in dB) of level-1 and -2 beamforming stages using analog DFT sub-array based method.

using voltage-control all-pass filters which is realized using 130 nm CMOS technology and having more than 5 GHz bandwidth. Measured beam patterns for a 4-element sub-array is presented. For the second approach, approximate discrete Fourier transform based multi-beam analog sub-array architecture is proposed. Analog current-mode implementation of the 8-point a-DFT circuit on 65nm CMOS proves exceeding 4 GHz bandwidth using BSIM4 models in Cadence Spectre. Level-2 digital beamforming is achieved using ROACH-2 FPGA platforms.

Acknowledgements

Arjuna Madanayake thanks NSF ECCS Awards 1408361 and 1509754 for financial support.

References

[1] P. Chevalier, "Optimal array processing for non-stationary signals," in *IEEE International Conference on Acoustics, Speech, and Signal Processing Conference Proceedings*, vol. 5, May 1996, pp. 2868–2871 vol. 5.

[2] S. Han, C. l. I, Z. Xu, and C. Rowell, "Large-scale antenna systems with hybrid analog and digital beamforming for millimeter wave 5G," *IEEE Communications Magazine*, vol. 53, no. 1, pp. 186–194, January 2015.

[3] W. B. Abbas and M. Zorzi, "Towards an appropriate receiver beamforming scheme for millimeter wave communication: A power consumption based comparison," *arXiv preprint arXiv:1604.05151*, 2016.

[4] H. Krishnaswamy and L. Zhang, "Analog and RF interference mitigation for integrated MIMO receiver arrays," *Proceedings of the IEEE*, vol. 104, no. 3, pp. 561–575, March 2016.

[5] T. Hoffmann, C. Fulton, M. Yeary, A. Saunders, D. Thompson, B. Murmann, B. Chen, and A. Guo, "Impact -2014; a common building block to enable next generation radar arrays," in *2016 IEEE Radar Conference (RadarConf)*, May 2016, pp. 1–4.

[6] "ROACH-2 revision 2." [Online]. Available: https://casper.berkeley.edu/wiki/ROACH-2_Revision_2

[7] P. Ahmadi, B. Maundy, A. S. Elwakil, L. Belostotski, and A. Madanayake, "A new second-order all-pass filter in 130-nm CMOS," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 63, no. 3, pp. 249–253, March 2016.

[8] C. Wijenayake, A. Madanayake, L. Belostotski, Y. Xu, and L. T. Bruton, "Linear RF apertures using 2-D analog beam filters," in *2016 IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2016, pp. 293–296.

[9] V. Ariyarathna, S. Kulasekera, A. Madanayake, K. S. Lee, D. Suarez, R. J. Cintra, F. M. Bayer, and L. Belostotski, "Multi-beam 4 GHz microwave apertures using current-mode DFT approximation on 65 nm CMOS," in *IEEE MTT-S International Microwave Symposium*, May 2015, pp. 1–4.

[10] P. Ahmadi, M. H. Taghavi, L. Belostotski, and A. Madanayake, "10-GHz current-mode 1st- and 2nd-order allpass filters on 130nm CMOS," in *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, Aug 2013, pp. 1–4.

[11] D. Suarez, R. J. Cintra, F. M. Bayer, A. Sengupta, S. Kulasekera, and A. Madanayake, "Multi-beam RF aperture using multiplierless FFT approximation," *Electronics Letters*, vol. 50, no. 24, pp. 1788–1790, 2014.

[12] A. Madanayake, N. Udayanga, and V. Ariyarathna, "Wideband delay-sum digital aperture using thiran all-pass fractional delay filters," in *2016 IEEE Radar Conference (RadarConf)*, May 2016, pp. 1–5.