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ANALYSIS THROUGH MODELING OF DESIGN TRADEOFFS AT THE TRANSISTOR LEVEL FOR A B-GA2O3 BASED LATERAL SWITCH (PREPRINT)

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14. ABSTRACT *(Maximum 200 words)*
Thermal transport capability of monolayer 2D materials has been under constant spotlight. However, different definitions of thickness in literature have led to ambiguity towards predicting thermal conductivity values and thus in understanding the heat transfer capability of different monolayer 2D materials. We argue that the same thickness should be used and a 'sheet thermal conductance' should be defined as an intensive 2D material property when characterizing the heat transfer capability of 2D materials. When converting literature thermal conductivity values of monolayer materials to this new property, some new features that were not displayed when using different thicknesses show up.

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Analysis through Modeling of Design Tradeoffs at the Transistor Level for a β-Ga_2O_3 Based Lateral Switch

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Abstract:

β-Ga_2O_3 based devices show great promise for power switching applications based on metrics such as Baliga's Figure of Merit (FOM), exceeding Si by orders of magnitude and even exceeding emerging wide bandgap materials such as GaN and SiC. This and similar FOMs are valuable metrics to assess the promise of a material for an application. They allow materials to be compared to each other under the assumption that the "ideal" device can be fabricated for each material, and additionally that no other limiting factors exist. Here, an electro-thermal device model of lateral devices with realistic layouts and device properties is used to assess a number of non-idealities that will cause a material to fall short of the ideal theoretically best performance stated by the FOM. We use the model to assess the relative importance of various known performance limiters at the device level (access resistance, ohmic contact resistance, etc.), design considerations (centered vs. offset gate, gate recess, gate field plate, dopant profile, etc.), and other limiters not addressed by BFOM (such as thermally limited operation). We quantify the expected improvement due to refinements in material quality, layout, channel and substrate specifications. We find that our modeled device is extremely thermally limited, such that it never really saturates at an open channel steady state bias, and additionally that thinning the backside will not fully alleviate this problem. Because of thermal limits, we find counterintuitively that maximum current is a function more of the low field mobility than the saturation velocity.

Introduction:

Wide bandgap materials such as GaN and SiC have revolutionized the power switching and (for GaN) the RF device markets. Far more power can be handled in a smaller form factor, with greater efficiency and with more operating margin, such as high ambient temperatures. The single biggest factor for this is the wider bandgap of the materials involved, which allow a bigger critical electric fields strength (E_C) to be sustained before the material breaks down. As a concrete example, BFOM for resistive losses [1] scales as bandgap *cubed*, so even wider bandgap materials such as β-Ga_2O_3 are predicted to far surpass GaN and SiC. This scaling comes from an assumption that an ideal device can be constructed, with the entire device area fully field-depleted with the lateral electric field equal to E_C everywhere at the breakdown voltage. This is an ideal way to compare materials for an application, but it is apparent though that no allowance is made at this level for real-world device considerations like

ohmic contact resistance, source access resistance, thermally limited behavior, etc. In short, BFOM indicates that Ga_2O_3 is a promising material for power applications, but gives no guidance on how to make the ideal device. In fact, as a device is more tightly scaled, many of these factors will become more important. For example, a given minimum gate-source gap to accommodate design rules will be a bigger fraction of the total area, or a given cross-section amount of ohmic metal needed for low resistance will be a bigger fraction of the total area, or a given amount of device heating expected at peak power will increase as the power *density* climbs and the gate pitch drops. *The increasing relative importance* of real-world non-idealities and parasitic effects required to fabricate practical devices as a material's innate properties improve has motivated this publication. We start with a baseline hypothetical β-Ga_2O_3 device modeled in ISE Synopsys Sentaurus Device. This model leverages prior work in GaN [2, 3, 4]. Model inputs are the known β-Ga_2O_3 properties (with references) where these are well understood and immutable. Where reasonable improvement can be expected over time from best known values (for example ohmic contact resistance), we reference the best known value but model with reasonable choices for expected values as devices mature.

Baseline Model Construction:

We started with a 2D model of a lateral Ga_2O_3 device using the as-observed geometry (SEM) [5] for the gate. The overall shape of the gate is critical for understanding peak electric field, especially the drain corner of the gate footprint. Dimensions were set for the baseline model to 0.50 µm each from source to gate, gate footprint, and from gate to drain, as shown in Fig. 1 This baseline 200 nm channel with $5*10^{17}$ cm^{-3} active dopant concentration gives a targeted sheet charge density (n_s) of 200 nm * $5*10^{17}$ cm^{-3} = 10^{13} cm^{-3}. A full 3D electro-thermal model of a ring-FET structure on a Ga_2O_3 bulk wafer (0.50 mm thickness unless otherwise noted) is simulated in Synopsys's Sentaurus Device. The bottom of the wafer is assumed held at 300 Kelvins and also is electrically grounded. The entire simulation domain (0.5 mm by 5 mm diameter with the device at center) is modeled with the full physics invoked. This diameter was chosen because the simulation was insensitive to domain size at this point (the domain needs to be large enough to capture all of the relevant effects, but beyond that it only adds to simulation time). This is done through a 2D TCAD model that was swept along an axis of rotation 129.88 um from the center of the gate as seen in Fig. 1, simulating a 0.816 mm periphery FET. Channel donors are assumed to be shallow, and acceptor-like traps in the SI material under the channel are assumed to be slightly above mid-bandgap (0.25 eV above). Trap occupancy was modeled by free-carrier capture and thermal emission processes, with this charge coupled into the Poisson equation. It is critical to consider the properties of the SI region when modeling wide bandgap semiconductors; free carrier concentrations will be negligible for a wide range of Fermi levels in the bandgap causing the electrical problem to be ill-defined if the material is assumed to be intrinsic and with no states in the bandgap. A large-periphery lateral device would probably take the form of many parallel gate fingers, but the ring structure was chosen for this work due to ease of 3D simulation and because it is a simple layout for evaluating transistors in emerging materials.

Electron and hole transport were solved with drift-diffusion carrier transport, assuming a low field mobility of 63.5 * $(T/300)^{-1.55}$ $cm^2/V/s$, saturation velocity of 1.2 * 10^7 cm/s, and following the Sentaurus "extended Canali model" at intermediate fields [6], where T is temperature in degrees K. Ohmic contact resistance is assumed to be 0.5 Ohm*mm for each contact, a value competitive with GaN HEMTs technology. While achieving a low Ohmic contact resistance is a continuing challenge for Ga_2O_3, the intent of this work is to explore the ideal Ga_2O_3 device on the assumption that issues such as this are solved. Temperature coefficient is from reference [7]. Thermal conductivity for Ga2O3 is anisotropic, and somewhat different for a, b, and c directions, forcing a 3D model for exact temperature modeling. For the purposes of this investigation thermal conductivity was assumed to be an effective average of these, 16 * $(T/300)^{-1.135}$ W/m/K, which will invoke a slight error in the absolute accuracy of temperature predictions. However, the relative comparison of the thermal merits of one layout vs. another will not be much affected by this approximation, and the electrical comparison at low power dissipation will not be affected at all. Thermal conductivity for the gate and ohmic metals were set to standard bulk values for the pure metals unless otherwise specified. The gate was 480 nm Au on 20 nm Ti, the ohmics 300 nm Au on 300 nm notional ohmic contact layer assumed here to be 200 W/m/K. As ohmic contacts are still very much in development, this is a notional value that should be updated as processes mature. The static dielectric constant for Ga_2O_3 was 10.0 ε_0 and for the barrier was set to 9.61 ε_0 (representative of Al_2O_3). A fully coupled steady-state solution to the drift-diffusion carrier transport equation, Poisson equation, and thermal diffusivity equation were obtained for all modeled data reported.

Figure 2 shows internal detail for the modeled Baseline device as described and shown in Fig. 1, while Fig. 3 shows basic quasi-static DC electrical properties. It can be seen that at lower bias (top row) the device is roughly symmetrical, with the gate at the center of the hot spot. At higher biases, the hot spot moves to the depletion zone and farther out into the gate-drain region, with this trend increasing at higher biases (not shown). The thermal gradients are large enough that a treatment beyond the current approach, such as one treating optical phonons and hot electrons in a full-band approach would be warranted for a more exact extraction of the temperature profile [8, 9].

Variations Modeled:

Relative to the baseline model, we vary first items in the current path. We improve (1-1) low field mobility and (1-2) high field saturation velocity to understand if the channel material limits device performance and (2) ohmic contact resistance. While items (1-1 and 1-2) might not be attainable with this materials system, as they are adjustments to the fundamental properties of the material; the intent is to understand how much this is a fundamental issue. We then alter the layout of the device, in all cases holding the source-drain spacing constant at 1.5 µm. Variant (3) has a 0.2 µm larger gate footprint (still centered) to adjust the short-channel effects, while (4) has a gate offset 0.2 µm to the source, as compared to the centered baseline. Variant (5) explores addition of a 0.2 µm gate field plate; (5-1) and (5-2) are respectively on top of the baseline centered gate and on top of variant (4). . Last, considerations relating to the choice of starting material for device fabrication are explored. To reduce short channel effects for the baseline device, the channel layer thickness was reduced but with doping

level altered to hold the targeted carrier sheet density constant (6-1, 6-2) and (7) with increased targeted carrier sheet density. Just under the channel, the substrate properties were explored by altering the (8-1, 8-2) substrate SI layer trap density with a few choices for this value, and (9) reduced substrate thickness was explored to improve the thermal resistance of the device.

Table I summarizes parameters of interest for power switches, where the gain in expected performance is quantified for the more complicated device processes. Some of the combinations are instructive, and **Figure 4** shows the value of the peak lateral electric field as a function of the applied drain bias at a set pinch-off condition of $V_{po} = V_{th}$-10V. The breakdown field to expect for a mature real-world lateral device fabricated in Ga_2O_3 bulk material is an open question. We chose 4 MV/cm lateral electric field because it is considerably less than the theoretical breakdown field of ~ 8 MV/cm for bulk Ga_2O_3 [10], to allow for inevitable defects, process variation, etc. As an example, GaN can theoretically reach 3.3 MV/cm [11] yet the highest demonstration we have found for a lateral device is ~2 MV/cm [12]. The location was picked on the assumption that the Ga_2O_3/dielectric interface would be weaker than either the bulk Ga_2O_3 or the bulk dielectric barrier layer, and also because of the proximity to gate and ohmic metal make this a worst case within the Ga_2O_3 (fringing fields near small radius equipotential surfaces will increase electric fields)

Results:

From Table I, we see that (as expected) the low field mobility dominates the on-resistance; variant 1-1 shows that doubling the mobility nearly halves the on-resistance. It also substantially improves the maximum current (I_{max}) although this is nowhere near doubled, as a simple analytical treatment neglecting heating effects might predict. Thermal resistance increases considerably but this is solely because the high power condition at which thermal resistance is extracted is higher power for variant 1-1 than the others, and the thermal conductivities of the material stack degrade with increasing temperature the thereby increase the thermal resistance. As is seen in Fig. 2, I_{max} is greatly influenced by self-heating. This is because as modeled, the low field mobility has a strong temperature dependence. Turning off the temperature dependencies in the model (not shown) causes the IV family curves to were verified to approach a saturation current but not droop with increasing drain bias. The lack of any discernable effect of increasing v_{sat} as seen in variation 1-2 is counterintuitive. Further investigation (not shown) reveal that at I_{max} the peak carrier velocity in the channel is about $3*10^6$ cm/s, still far from saturating. *As designed, the device is thermally limited before it can enter a true saturation*. The local temperature at this location is about 500 K, greatly reducing the low field mobility and increasing the electric field at which carrier velocity saturates to well beyond the value reached at the I_{max} point. While not the subject of this work, v_{sat} is expected to be critical for an RF device.

The biggest improvements are seen optimizing the layout. First, a larger gate length is explored (variant 3), keeping the centered gate. It is clear that the baseline gate of 0.5 µm exhibits significant short-channel effects. We see improvements through both offsetting the gate toward the source (variant 4) and through addition of a gate field plate. By themselves, offsetting the gate 0.2 µm and

adding a 0.2 µm gate field plate improve the breakdown voltage significantly, by 14V (variant 4) and 25V (variant 5-1) respectively. Together, *the improvement in breakdown voltage is far greater than an additive some of the changes* would naively suggest, with 78V improvement (variant 5-2). The FOM contains this term *squared* so shows a more extreme improvement yet. It is critical to observe that the modeled breakdown voltage (V_{br}) is dependent on the criterion that is assumed met at breakdown, here 4 MV/cm lateral electric field reached at the top of the channel. It can be seen in Fig. 4 that variant 5-2 has a fairly uniform lateral depletion field, but could be further optimized with some adjustment to the exact field plate overhang length, gate position, etc., keeping in mind that the ideal values will be a function of the targeted peak allowed electric field.

The channel variations showed that a thinner channel for the target n_s of $1*10^{13}$ cm^{-2} is better, with variants 6-1 and 6-2 showing better breakdown, while an increase in target n_s (variant 7) is very detrimental. While not shown, the 40 V breakdown for variant 7 increases to 160V when the allowed "critical" lateral electric field is increased to 6 MV/cm. As expected, the electrostatic of the problem will favor more highly doped regions if the critical field increases.

The substrate properties are explored last. To effectively pinch off a transistor, the substrate needs to actively confine the channel. In GaN, this is typically done with deep acceptor-like traps and considerable sensitivity for some parameters of interest for designing RF devices is seen to the density of traps under the channel [4]. The baseline device employed a $5*10^{17}$ cm^{-3} density of mid-gap traps to achieve this, of uniform density and abruptly stopping at the bottom of the channel. For 2X variation (8-1, 8-2) around this targeted density, the design is not very sensitive to this item. Last, thinning the substrate was tried to alter the thermal resistance. The substrate was thinned from 500 µm to 30 µm, where in all cases the heat sink at the bottom of the substrate is assumed an ideal sink. Given that common metals such as Cu, Al, Al are >10x the thermal conductivity of Ga_2O_3, and even AuSn eutectic is several times better at 57 W/m/K, this is a reasonable starting point for comparison. A similar periphery part in GaN would have roughly 10 K/W thermal resistance [13]. Here, we are able to reduce thermal resistance from 190 to 100 W/m/K, but this is still far from our target. To reduce the thermal resistance to a GaN-like value, heat will have to be extracted in another fashion such as through the topside metal contacts avoiding Ga_2O_3 as a path for heat transport. Alternatively, the higher thermal resistance is tolerable if the heat dissipated during switching operation can be reduced.

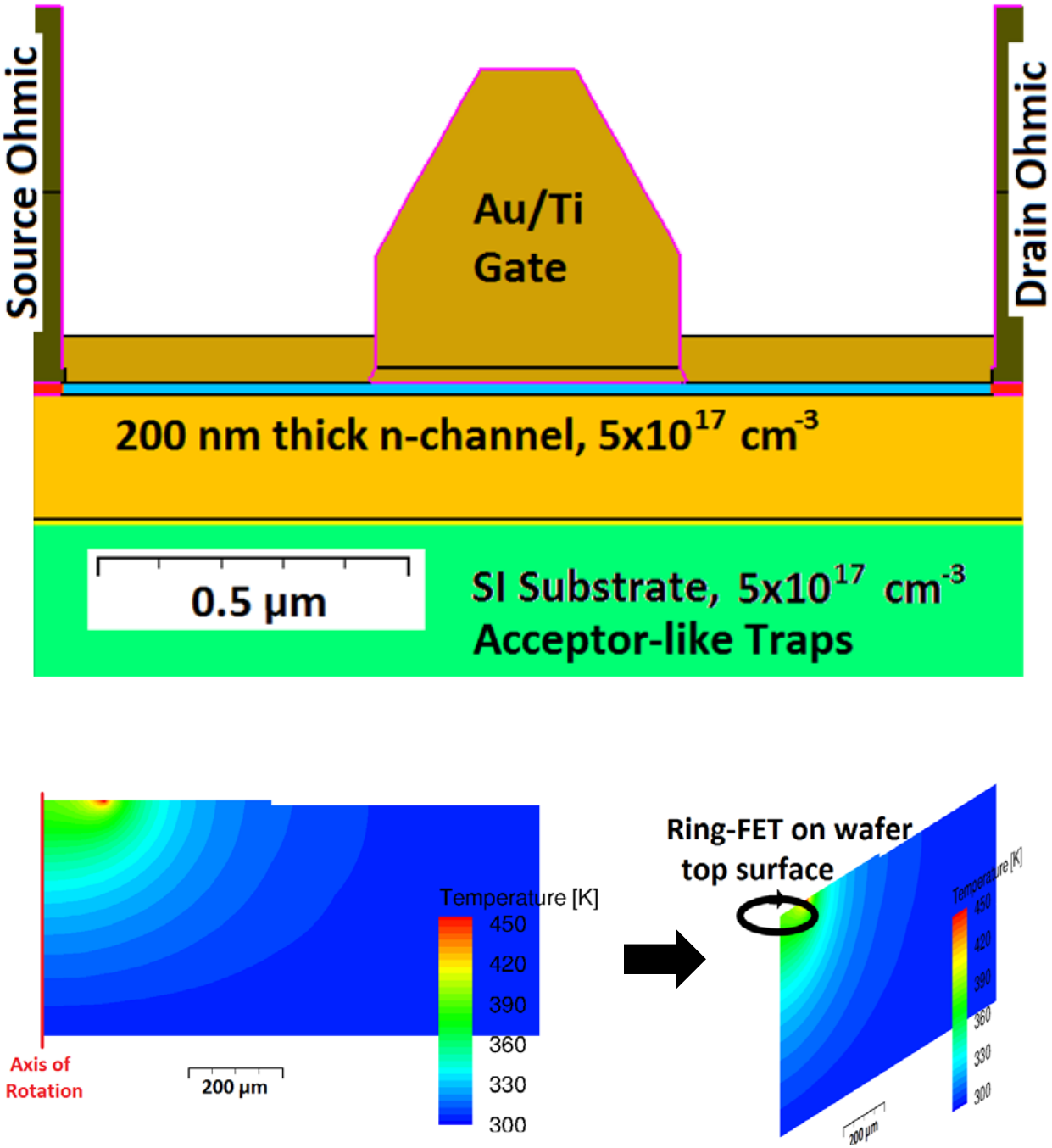


Figure 1: Small scale (top) and large scale (bottom left and right) baseline model construction. Cyan layer is a 25 nm Al_2O_3 dielectric barrier, while brown to the left and right of the gate is 75 nm dielectric passivation (static dielectric constant was 7.5 ε_0).

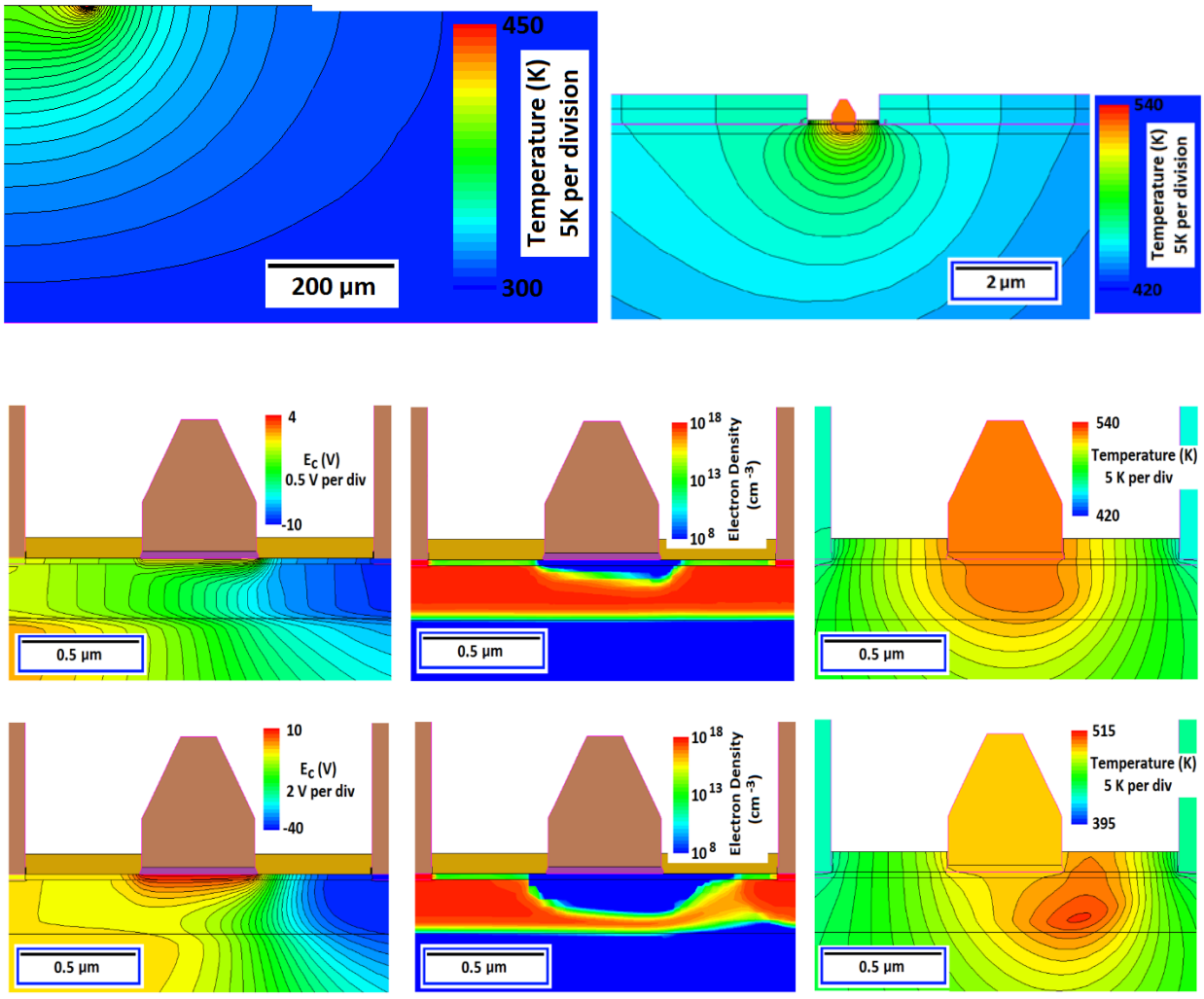


Figure 2: Views of the baseline device.

Top row: (left) a cross-section at a partially-on state (Vg=0, Vd=10V, Id = 1.209e-1 A → 1.209 W) and (right) a zoom-in of the active region at the same bias condition.

Bottom detail rows are:

Middle row: the partially on-state (Vg=0, Vd=10V, Id = 1.209e-1 A → 1.209 W): (left) Conduction band edge, (middle) electron profile, (right) T profile.

Bottom row: the partially on-state (Vg=-12V, Vd=40V, Id=2.689e-2 A → 1.0756 W): (left) Conduction band edge, (middle) electron profile, (right) T profile.

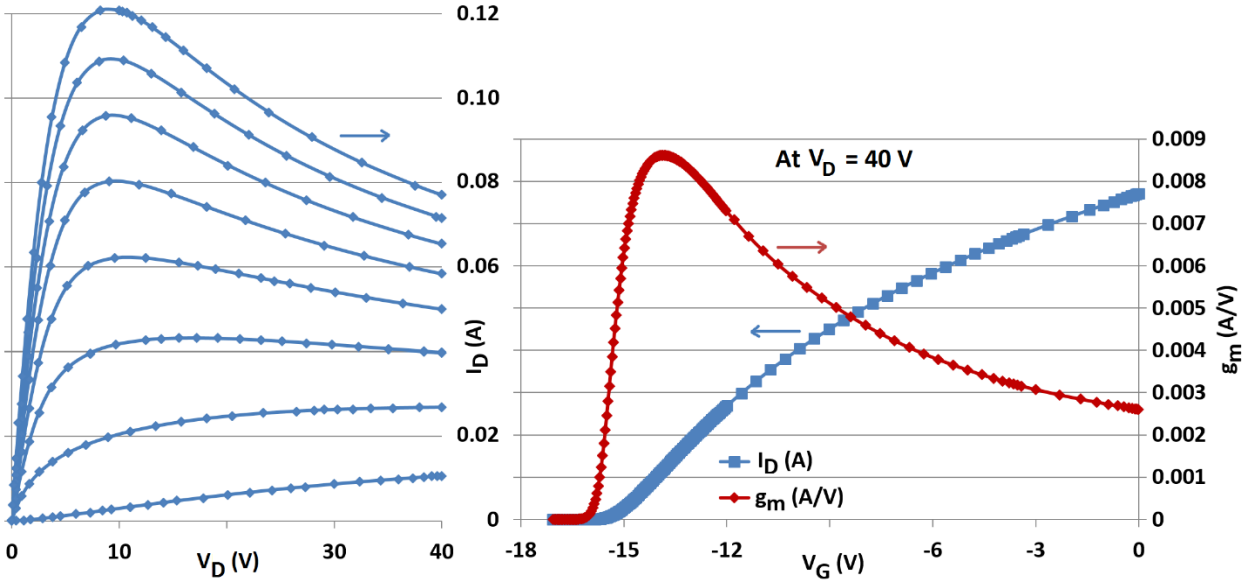


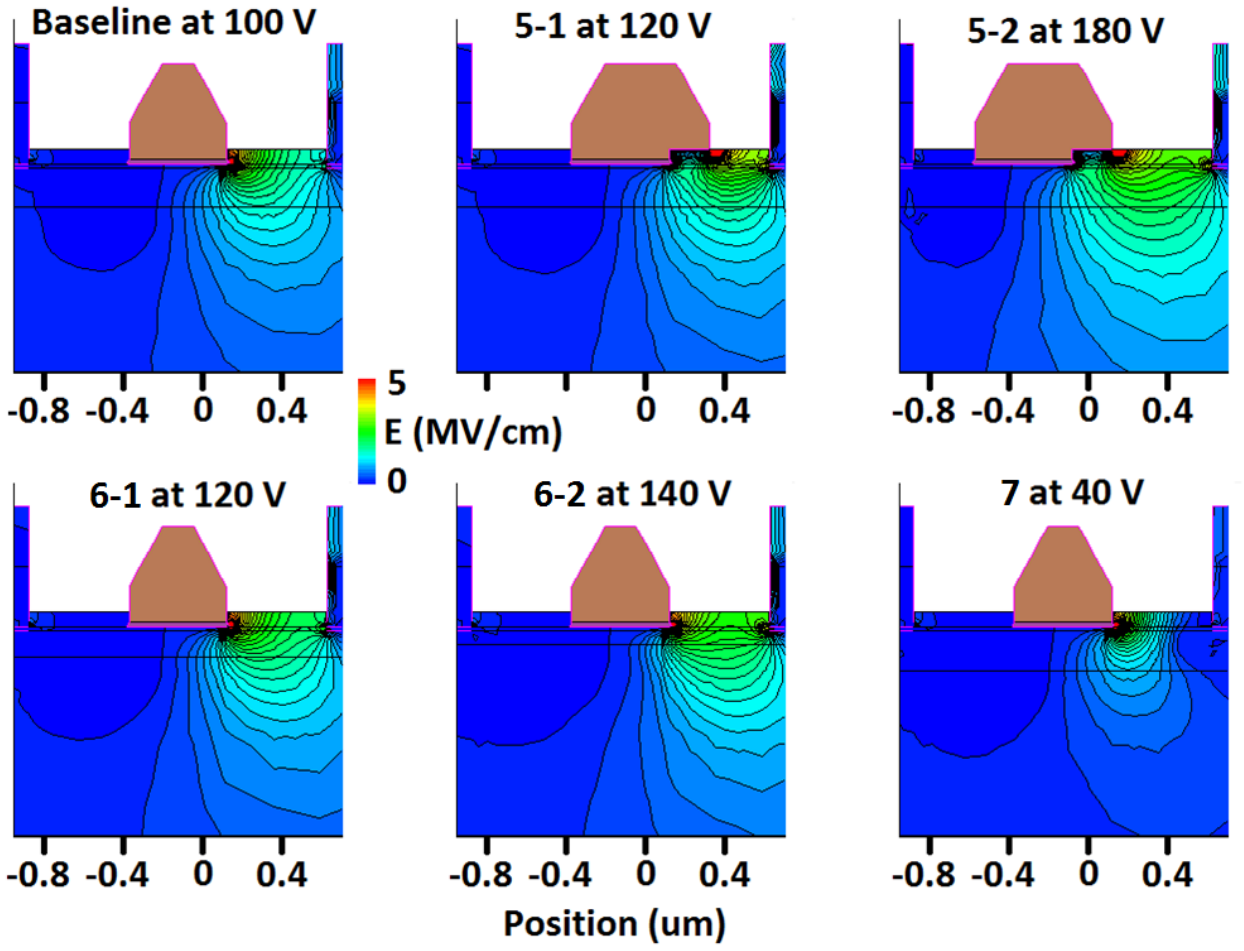
Figure 3: (left) Baseline IV FOC from V_G = 0 V to -14 V in 2 V steps, and (right) I_D-V_G and g_m curves. Thermally limited behavior is seen in FOC at open channel saturation.

	Low bias R_{on} (Ohm) (At V_D = 0.1V, V_G = 0 V)	I_{max} (A) (V_D = 10V, V_G = +4V)	V_{th} (V) (V_D = 40 V)	g_m peak (mA/V) (V_D = 40V) / V_G at g_m peak	Subthreshold Swing (mV/decade) (V_G where I_D =0.1 mA and Vd=40V)	Thermal Resistance (R_{th}) (K/W) (Open Channel) At V_D = 10V, V_G = 0V	Breakdown V_D (V) Defined at 4e6 (V/cm) (lateral) / Location (near gate or drain)	Device FOM** V_{br}^2/R_{on} (W) Relative to Baseline
The Baseline Device								
Baseline	27.6	0.142	-15.2	8.6 / - 13.8	325	190	99 / Gate	1.00
Vary the Basic Electrical Properties								
1-1. Doubled Low field Mobility	**14.4**	**0.200**	-15.3	**13.7**/ -14.4	**300**	216	99 / Gate	**1.91**
1-2. 20% improved saturation velocity	27.6	0.142	-15.2	8.7 / -13.9	325	190	100 / Gate	1.02
2-1. Halved Rc	26.7	0.143	-15.2	8.6 / -13.8	325	191	99 / Gate	1.02
2-2. Doubled Rc	28.8	0.141	-15.2	8.6 / -13.8	325	189	99 / Gate	0.96
Vary the Device Layout (in all cases holding source-drain spacing constant at 1.5 µm)								
3. Increase Gate Length by 0.2 um (gate is still centered)	28.2	0.141	-13.7	7.8 / -12.1	**310**	185	100 / Gate	1.00
4. Gate offset by 0.2 µm toward source	27.6	0.149	-15.2	9.0 / -13.8	325	191	**113** / Gate	**1.30**
5-1. 0.2 µm GFP added to the baseline centered gate	27.6	0.142	-14.7	8.4 / -13.3	315	189	**124** / Drain*	**1.57**
5-2. 0.2 µm GFP added to a gate offset of 0.2 µm	27.6	0.149	-14.6	8.8 / -13.2	315	190	**177** / Drain*	**3.20**
Vary the Channel								
6-1. Epi thickness 2/3 baseline, 1.5x doping	27.5	0.141	-10.1	**10.1**/ -9.1	**235**	192	**117** / Gate	**1.40**
6-2. Epi thickness 1/3 baseline, 3x doping	27.3	0.138	-5.8	**12.4**/ -5.0	**170**	195	**137.5** / Drain*	**1.95**
7. Epi thickness same as baseline, 1.5x doping	**17.3**	**0.183**	-26.3	**9.9** / -25.2	350	209	44.5 / Gate	0.32
Vary the Substrate								

8-1. Halved Substrate SI trap level	26.1	0.147	-17.4	8.0 / -16.0	**305**	192	97 / Gate	1.00
8-2. Doubled Substrate SI trap level	28.7	0.139	-13.9	8.7 / -12.5	320	189	102 / Gate	1.02
9-1. Substrate thickness 100 um	27.6	0.162	-15.2	9.3 / -13.6	325	**140**	98 / Gate	0.98
9-2 Substrate thickness 30 um	27.5	0.185	-15.0	**10.0** / -12.9	320	**100**	98 / Gate	0.98

*** Drain voltage is approximate; this is a function of how the ohmics are formed and is a rough lower limit as-modeled.**
**** FOM is calculated for breakdown voltage where the lateral field 4 MV/cm is first exceeded.**

Table I: Variations on the baseline ring-FET, subdivided by the portion of the device explored, and with significant improvements **bolded** for readability. The "Breakdown" drain voltage (at $V_g = V_{th}$ - 10V) is conservatively defined at which 4.0 MV/cm *lateral* E field component is first reached at *the top of the Ga_2O_3 channel* and the location of that peak (near gate or near drain) is noted. V_{th} is extracted via the transconductance linear extrapolation method (GMLE) [14].



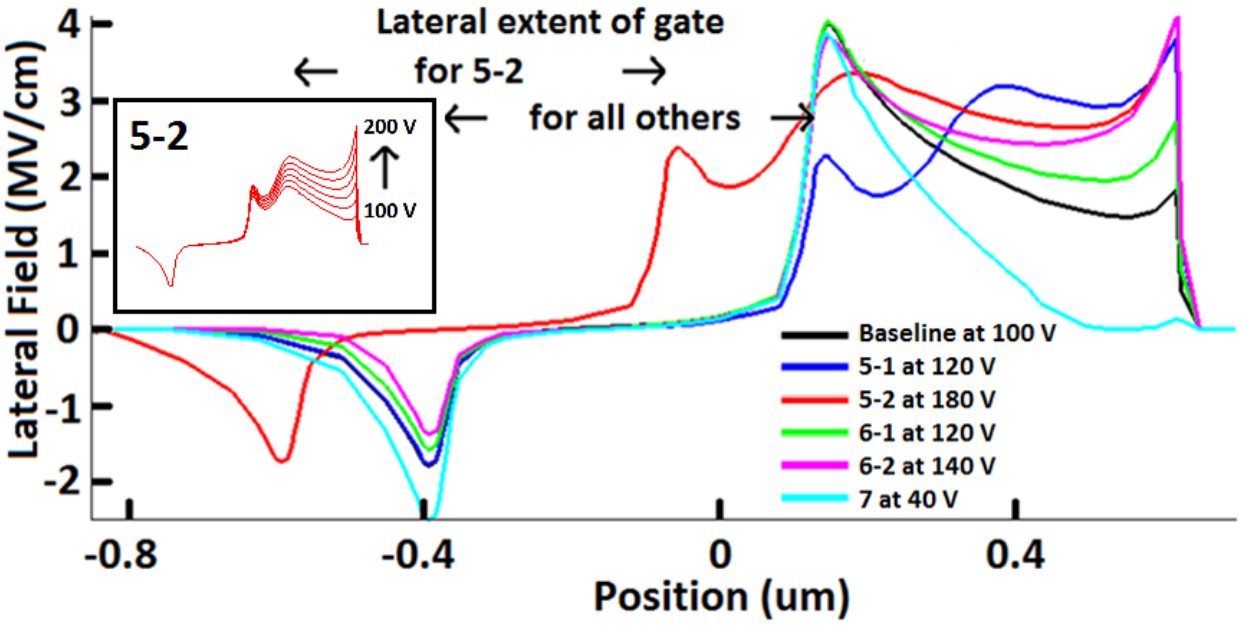


Figure 4: Peak lateral electric field for the baseline device and selected variants (as labeled in Table I) with very different field shaping profiles than the baseline. In all cases plots are of the drain voltage where V_{br} (as defined by 4 MV/cm lateral field component) is first breached at the top of the Ga_2O_3 channel. The boxed inset shows for variant 5-2 how lateral field distribution changes with drain voltage (the second to top curve matches the main plot).

Conclusions:

We quantified the impact of various design trade-offs at the materials and device level on lateral FETs in Ga_2O_3. We find that the modeled device is very limited by channel resistivity and that improvement in the low field mobility achievable in the material will have a big effect. For this modeled device a GaN-like ohmic contact resistance is sufficient. Variant 5-2 (gate offset to the source and a gate field plate) is able to reach higher breakdown voltage for electric field under the selected 4 MV/cm lateral field component criterion because this structure effectively spreads out the electric field over the a large breakdown zone. Yet, for this selected lateral field component criterion, we saw that a thinner and more highly doped channel layer (variations 6-1, 6-2) would perform better than the baseline structure for the selected breakdown field limit, with improved trans-conductance and subthreshold swing, *for no additional processing complexity*.

To further optimize transistor layout requires an understanding of the allowable peak field for the weakest material(s) in the device, after which the elements of the process that are achievable can be adjusted to optimally spread that field such that the highest possible drain bias is reached. We expect further processing complexity (gate recess for example) will further improve device performance and expect to explore additional levels of complexity in future work.

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