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Broadband 0.25- μm Gallium Nitride (GaN) Power Amplifier Designs

by John E Penn

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Sensors and Electron Devices Directorate, ARL

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14. ABSTRACT The US Army Research Laboratory is exploring devices and circuits for RF communications, networking, and sensor systems of interest to Department of Defense applications, particularly for next-generation radar systems. Broadband, efficient, high-power monolithic microwave integrated circuit amplifiers are extremely important in any communication system that must operate reliably and efficiently in continually crowded spectrums, with multiple purposes for communications, networking, and radar. This report describes the design of a broadband class A/B power amplifier using Qorvo's 0.25-μm high-power efficient gallium nitride on a 4-mil silicon carbide process. This design was one of several submitted to a US Air Force Research Laboratory–sponsored wafer fabrication.					
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1. Introduction

The US Army Research Laboratory (ARL) has been evaluating and designing efficient broadband linear high-power amplifiers for future adaptive multimode radar systems. Qorvo has a high-performance 0.25- μm gallium nitride (GaN) fabrication process and a process design kit (PDK) that researchers at ARL used to design broadband amplifiers, power amplifiers, and other circuits for future radar, communications, and sensor systems. These ARL designs are to be submitted for fabrication as part of a US Air Force Research Laboratory–led effort. These designs will demonstrate the performance, bandwidth, and capability of GaN processes for broadband power amplifiers.

2. Broadband Power Amplifier

A broadband power amplifier class A/B for C-band was designed using Qorvo's 0.25- μm GaN fabrication process. To keep the initial design simple, a single 1.75-mm high-electron-mobility transistor (HEMT) was used for a preliminary ideal design of the broadband power amplifier, operating nominally at 28 V. These devices can withstand higher voltages, which could produce higher output powers but with the additional need to dissipate higher power densities at the higher DC supplies. The optimal matching circuit designs will be a tradeoff of output power, efficiency, and bandwidth, optimized to a given DC input, or DC input range up to 40 V. These initial broadband power amplifiers are based on a 10- $\times$ 175- μm HEMT at a bias of 28 V and 180 mA. This size HEMT had an optimal match of about 50 Ω in parallel with -0.54 pF in capacitance at 28 V. Since a negative reactance can only be matched over a limited band, an initial design was performed of an ideal double-tuned Q bandpass match for broadband operation centered around 4 GHz, with a goal of achieving at least an octave of bandwidth (2-way). A schematic of the ideal load as a resistor in parallel with a capacitor and the ideal double-tuned output matching circuit is shown in Fig. 1. The simulation from 2 to 9 GHz of the ideal load (blue S11 trace) and ideal bandpass match (magenta S11 trace) is shown in the Smith Chart plot (Fig. 2).

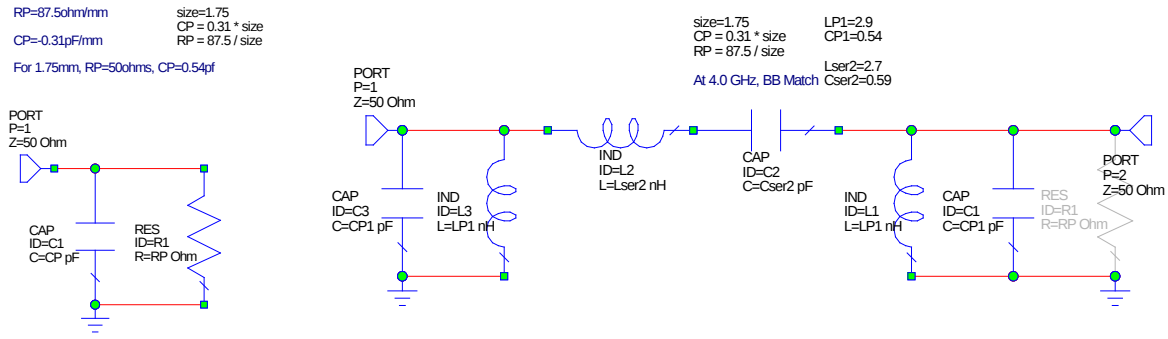


Fig. 1 Microwave Office (MWO) schematic for ideal power load and match (10- × 175- μ m HEMT, 28 V, 100 mA/mm)

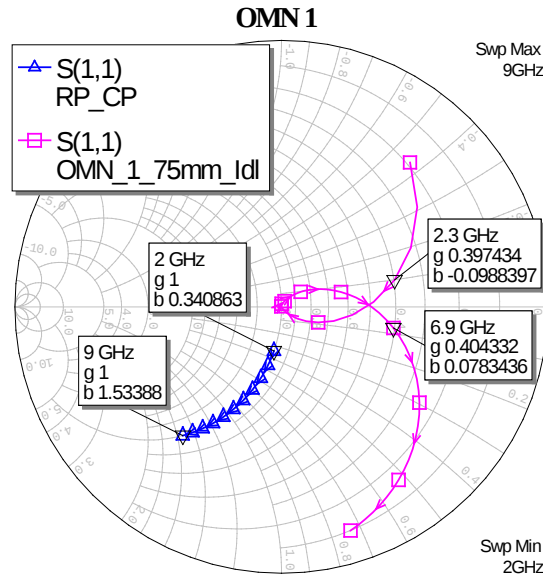


Fig. 2 MWO simulation of ideal power load and match (10- × 175- μ m HEMT, 2 to 9 GHz)

After an ideal lumped element output match was designed, the capacitors and inductors were replaced with monolithic microwave integrated circuit (MMIC) elements from the Qorvo GaN25 design library and returned to achieve a broadband match. Then microstrip bends, tees, and decoupling elements for the DC bias were added to complete a layout of the MMIC output match (Fig. 3). A simulation of the output match (Fig. 4) shows better than 20-dB return loss from 2.7 GHz to above 6.6 GHz (blue trace) versus the ideal lumped element double-tuned match with slightly less bandwidth (magenta trace) but excellent match mid-band. Note the relatively high insertion loss (1.0 dB) at 2.7 GHz versus 0.54 dB of insertion loss at 4.7 GHz for the lossy MMIC output match.

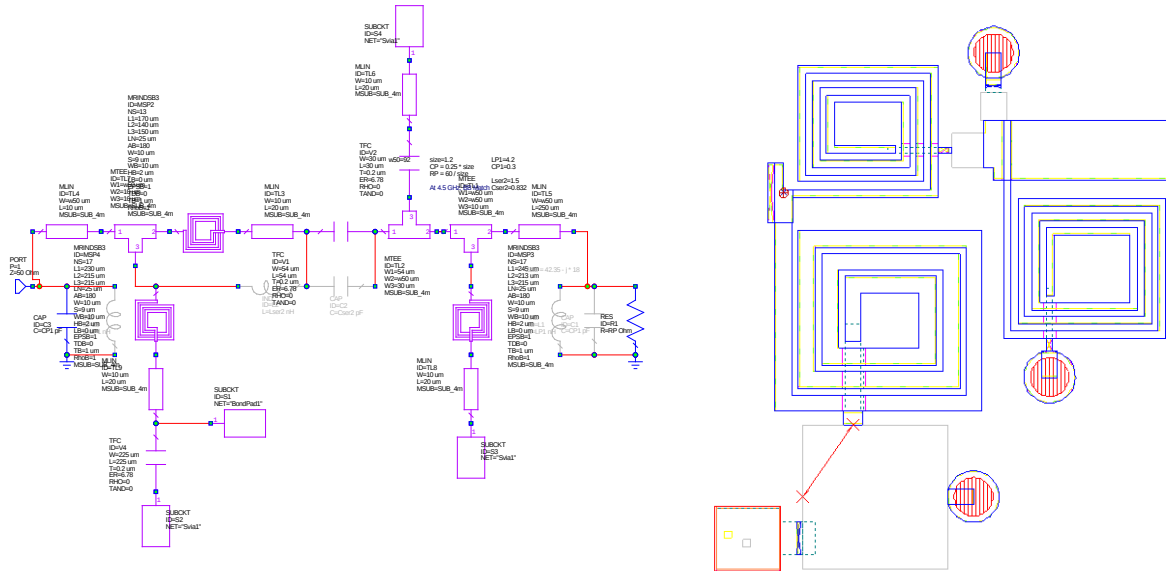


Fig. 3 Schematic and MMIC layout of broadband matching circuit (10- x 175-μm HEMT)

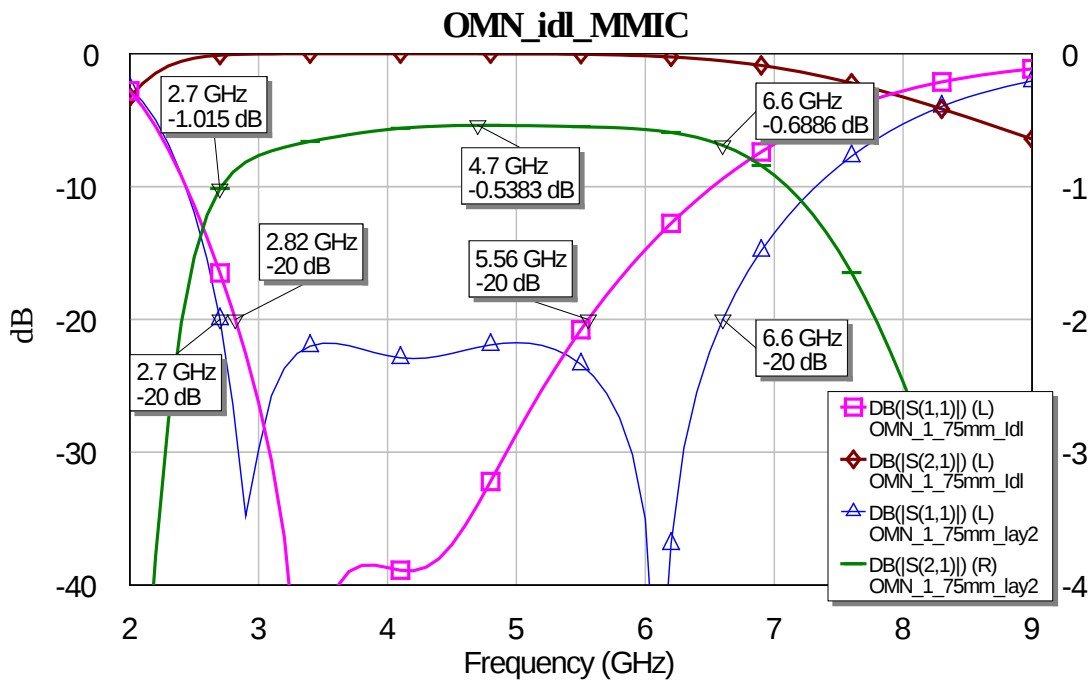


Fig. 4 MWO simulation of ideal (magenta) and MMIC output match (blue)

Comparing the impedance match of the ideal lumped element output match (solid lines) to the lossy MMIC output match (dotted lines) over frequency to the ideal 50-Ω impedance (left axis) and -0.54-pf capacitance (right axis) shows reasonable

broadband performance (Fig. 5). The ideal output match is close to the ideal 50- Ω load line of a 1.2-mm HEMT from 3.2 to 4.8 GHz, while the MMIC output match under-shoots the real part of the impedance and stays close to 43 Ω over a broader range of 3.1 to 5.7 GHz. The compromise of a lower load line impedance to achieve broader band gain will likely skew the output power and efficiency to lower voltages than 28 V, while the original ideal match had good performance from 28 to 35 V. Since an ideal reactance equivalent to a -0.54 -pF capacitance can only be maintained over a finite bandwidth, the output matching circuits can be seen as matching well over the band, diverging at the low and high end of the frequency range (3 and 6 GHz). Resistances (left axis) in the plot are represented by shades of red and magenta, while capacitances (right axis) are represented by shades of blue.

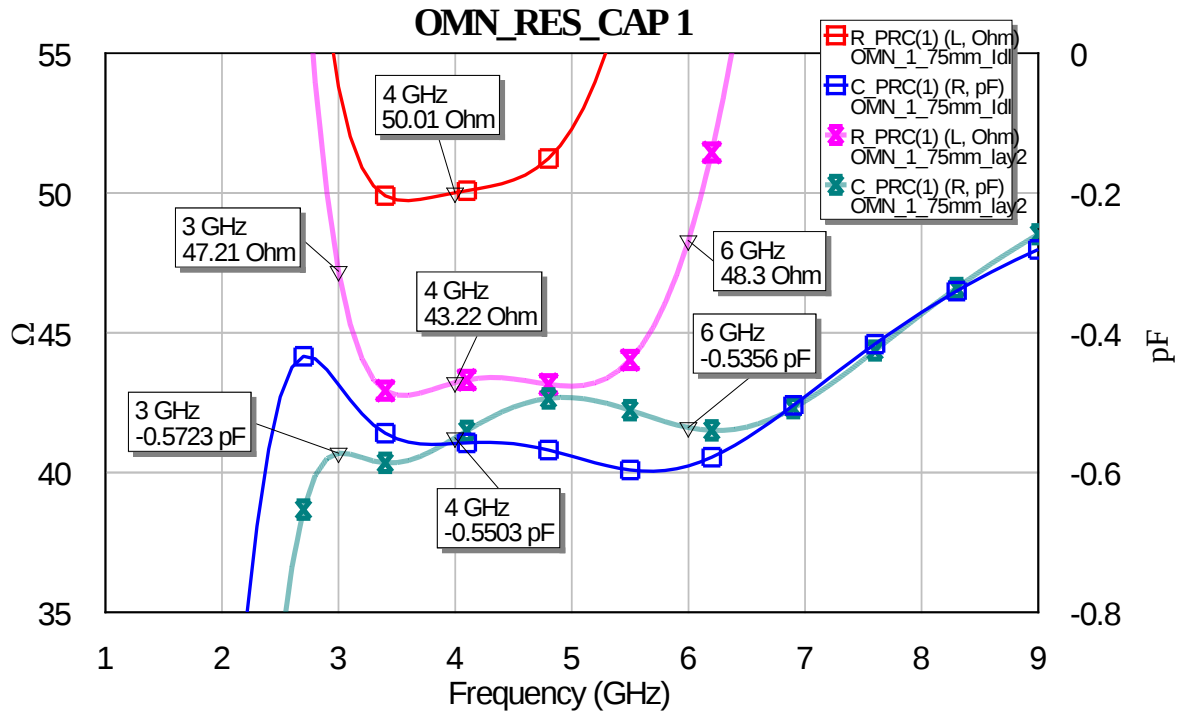


Fig. 5 Broadband impedance of output match ideal (solid) vs. MMIC (dotted) ($50\ \Omega \parallel -0.54\ \text{pF}$)

Further determination of the optimal output impedance was performed using the nonlinear HEMT model biased at 28 and 35 V, with a load pull simulation to generate power and power-added efficiency (PAE) contours at 4 GHz (Figs. 6 and 7). At 35-V DC bias, an ideal output match equivalent to 50 Ω in parallel with $-0.54\ \text{pF}$ simulates as more than 13 W (41.2 dBm) with better than 63% PAE. Even at 28 V, better than 11 W (40.5 dBm) with 66% PAE is shown by a simulation of an ideal output match equivalent to 41 Ω in parallel with $-0.48\ \text{pF}$. A compromise of a conjugate match of 50 Ω in parallel with 0.54 pF of capacitance was chosen as the optimal load for 28- to 35-V operation at C-band (4-GHz center).

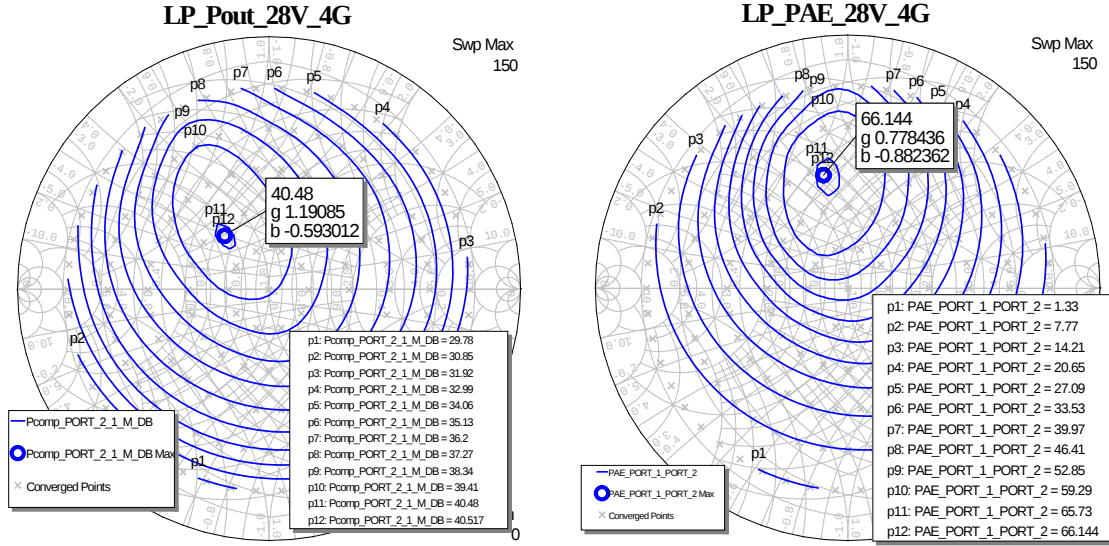


Fig. 6 1.75-mm HEMT load pull simulation 4 GHz, 28 V, 29.5 dBm input max pout 40.5 dBm: ($41 \Omega \parallel -0.48 \text{ pF}$); max PAE 66%: ($64 \Omega \parallel -0.70 \text{ pF}$)

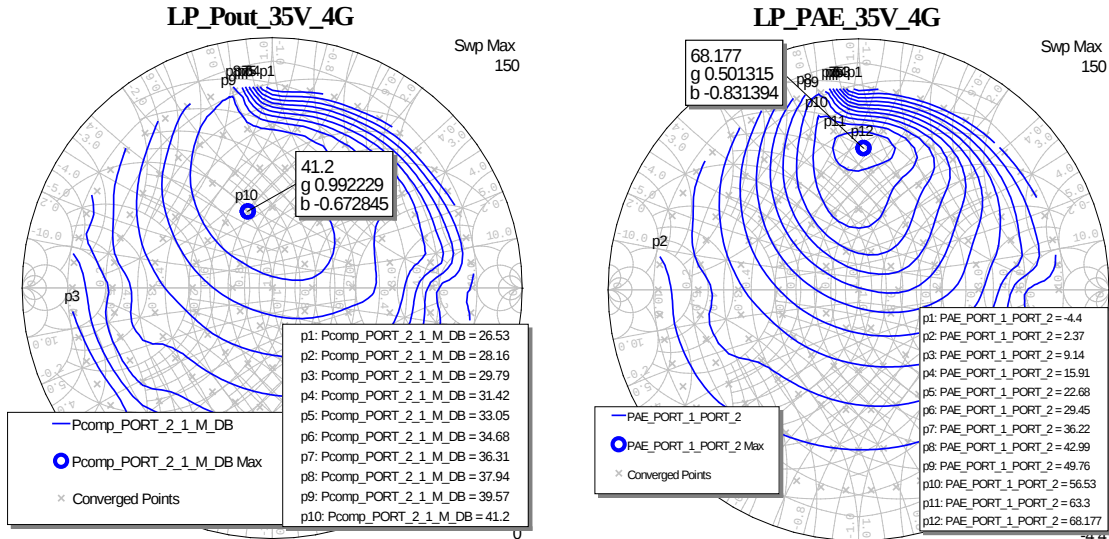


Fig. 7 1.75-mm HEMT load pull simulation 4 GHz, 35 V, 29.5 dBm input max pout 41.2 dBm: ($50 \Omega \parallel -0.54 \text{ pF}$); max PAE 68%: ($100 \Omega \parallel -0.66 \text{ pF}$)

Once the output match for the broadband power amplifier is designed, the s-parameters of the $10 \times 175\text{-}\mu\text{m}$ (1.75-mm) HEMT are generated at the nominal bias of 30 V and 180 mA (100 mA/mm). Small signal stability was analyzed and achieved with a series resistor (2Ω) on the gate of the HEMT (Fig. 8). Figure 9 shows that the source stability circles are all outside the Smith Chart, indicating unconditional stability. After stabilizing the 1.75-mm HEMT, the input impedance at mid-band (4 GHz) was simulated, resulting in a higher Q matching impedance

($Q = 2$) than the output, making it more difficult to broadband match the power amplifier input. An initial ideal input match provided better than 10-dB return loss from 3 to 7 GHz. A preliminary ideal lumped element input matching circuit provided good amplifier performance from 3 to 7 GHz (Fig. 10).

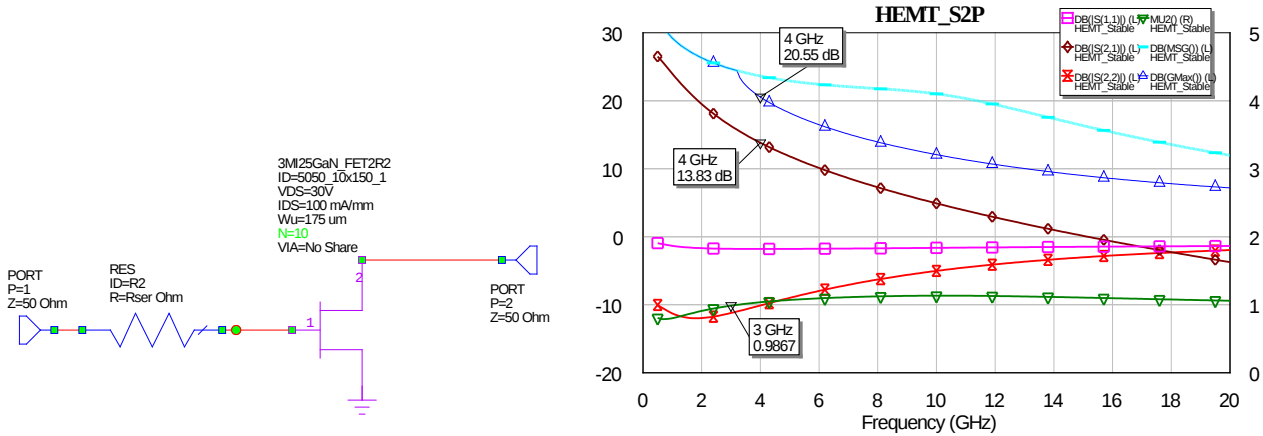


Fig. 8 MWO S-parameter simulation of 10- $\times$ 175- μ m (1.2-mm) GaN HEMT (28 V and 180 mA)

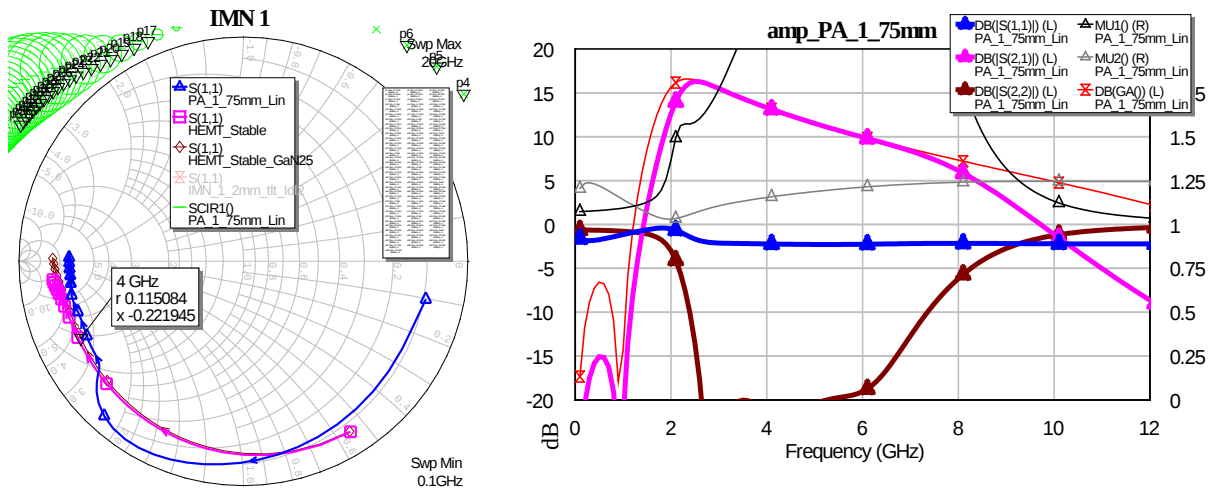


Fig. 9 Stabilizing resistors added to 10- $\times$ 175- μ m GaN HEMT (28 V) plus broadband output match

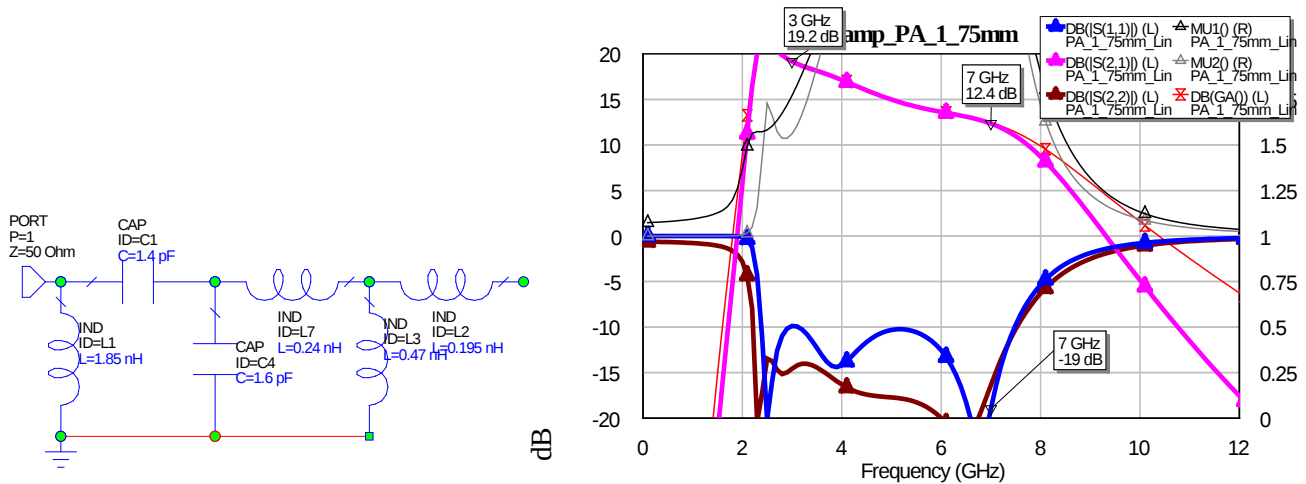


Fig. 10 Ideal input match for 3- to 7-GHz, 1.75-mm GaN HEMT (28 V) power amplifier

A preliminary input match including DC bias input for the gate is shown in Fig. 11. A pseudo layout of the full one-stage 4- to 5-W, 2- to 8-GHz power amplifier is shown in Fig. 12. The resulting single-stage amplifier performance is shown in Fig. 13, with a good gain of 19.1 dB at 3 GHz, dropping to 12.2 dB at 7 GHz.

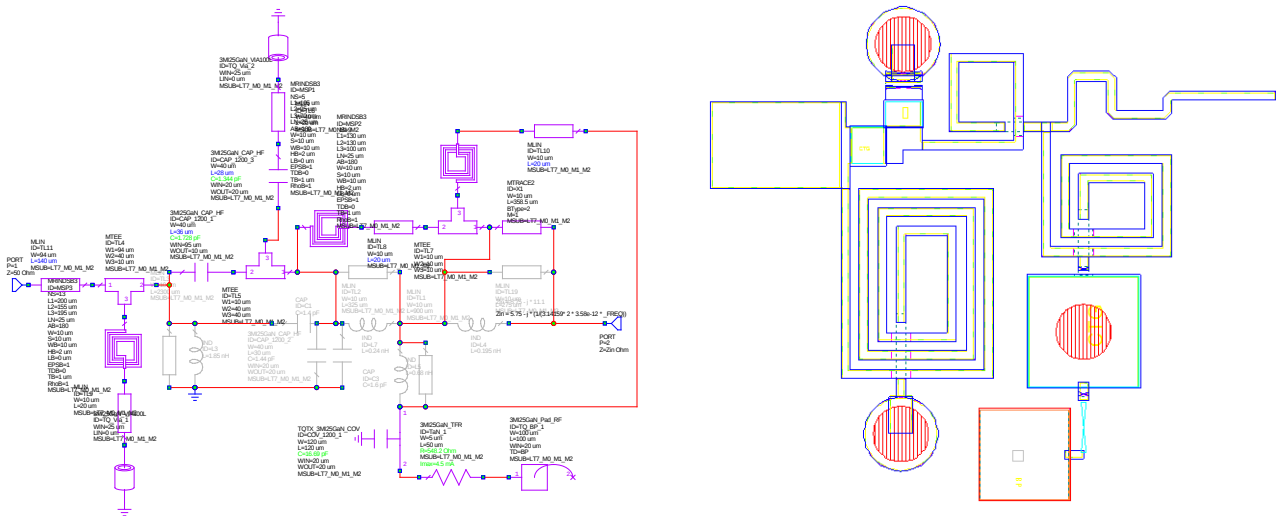


Fig. 11 Broadband MMIC input match for 3- to 7-GHz, 1.75-mm GaN HEMT power amplifier

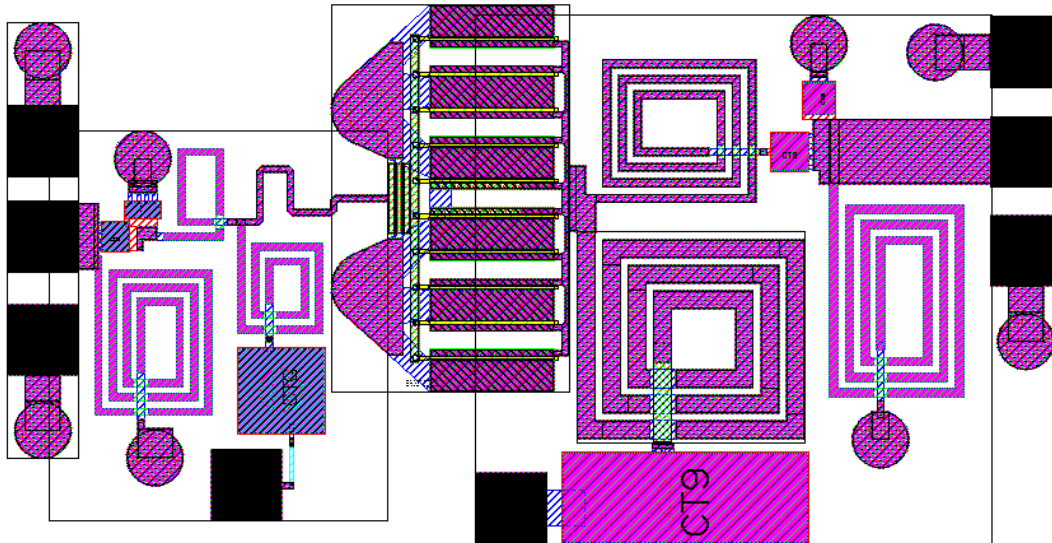


Fig. 12 Preliminary layout of 8- to 10-W broadband (3–7 GHz) 1.75-mm GaN HEMT power amplifier

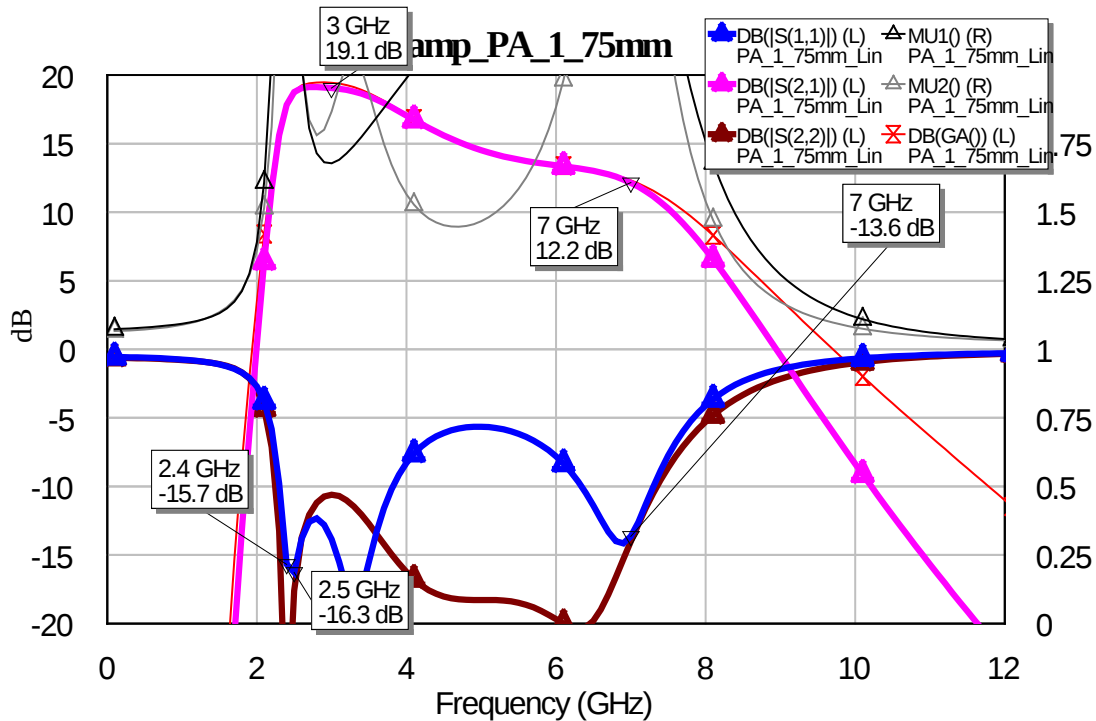


Fig. 13 Small signal simulation of 8- to 10-W broadband (3–7 GHz) 1.75-mm GaN HEMT power amplifier

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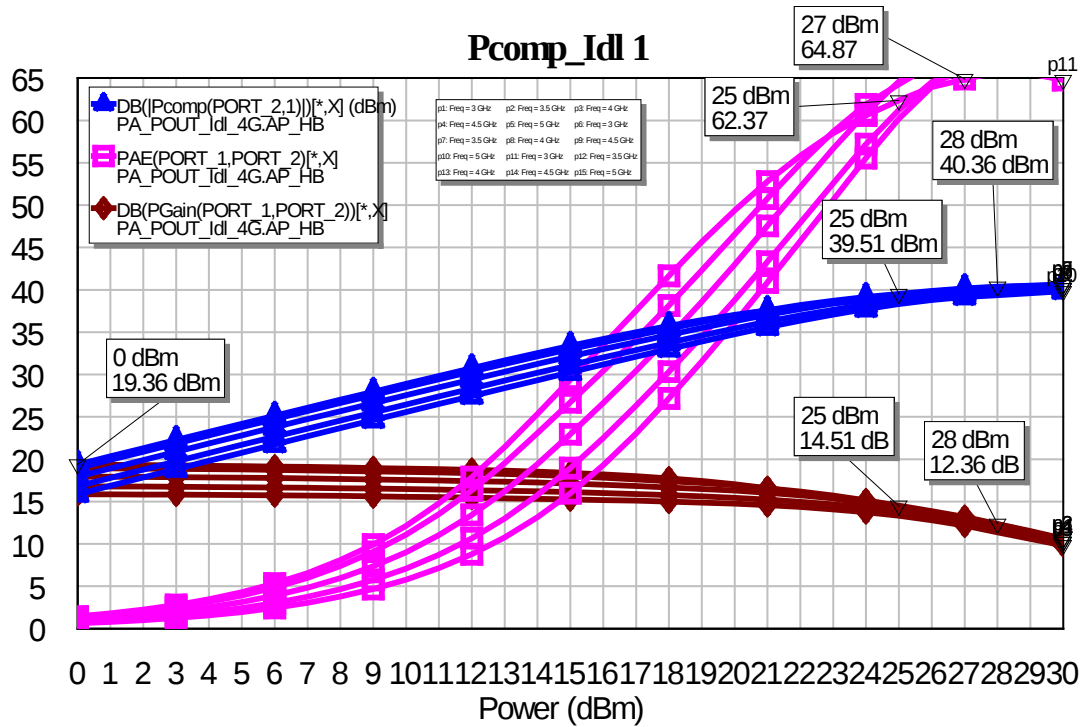


Fig. 15 MWO performance simulation of ideal (3–5 GHz, 28 V/180 mA) 1.75-mm HEMT power amplifier

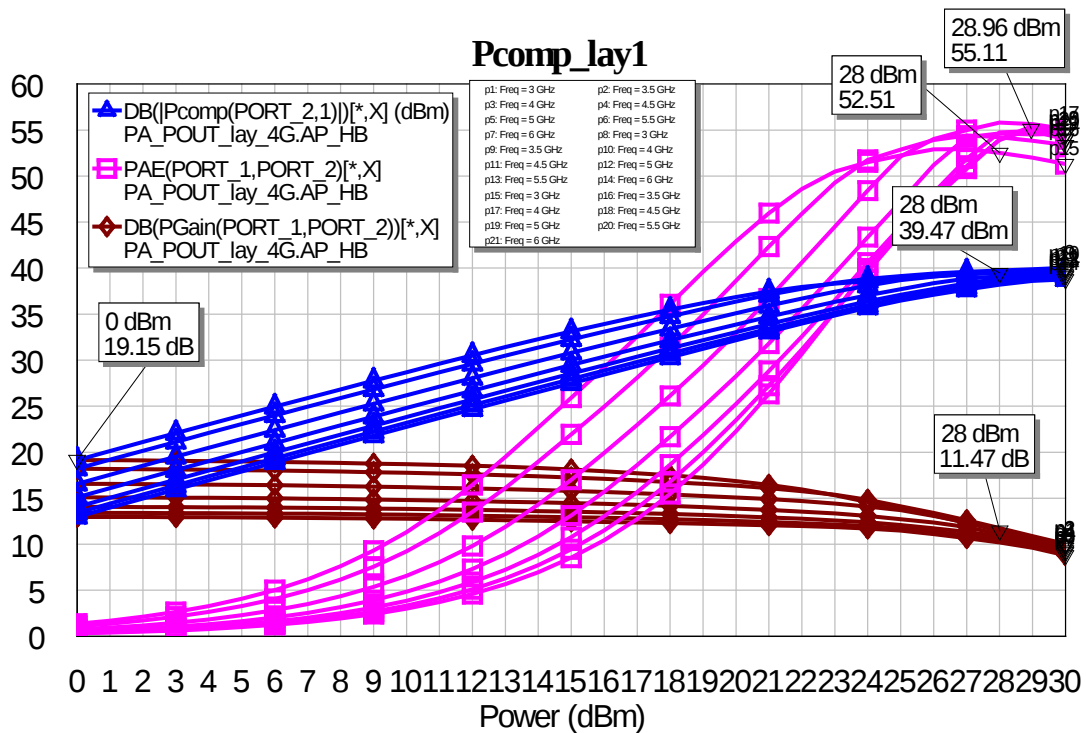


Fig. 16 MWO performance simulations of MMIC (3–6 GHz, 28 V/180 mA) 1.75-mm HEMT power amplifier

3. Axiem Electromagnetic Simulations of Broadband Power Amplifier Layout

Analytical models for MMIC elements were used here for the initial design; however, another time-consuming but very useful simulation and verification of the physical layout uses an electromagnetic (EM) simulator such as AWR's Axiem EM simulator. Descriptions of the process layers, metal thicknesses, dielectric constant, losses, and so on, are included in the Qorvo PDK for the GaN process. Once design rule checks are complete, the layouts of the input and output matching circuits are imported into an Axiem simulation. The EM simulation can model unexpected coupling in the physical layout that was not included in the analytical simulations, and it models the true physical connectivity of the 3-D interconnect potentially locating unintended short or open circuits. The EM simulation provides both a DC and RF verification of the layout. Layout versus schematic checking can often verify DC connectivity but may only identify inductors as a DC connection, possibly missing errors such as a shorted metal overpass and underpass in a spiral inductor. EM simulations are essential at higher frequencies, and even at these lower C-band frequencies the impact on performance indicated by the Axiem EM simulations of the layouts was apparent. While Axiem can simulate DC (zero frequency) to verify proper RF and bias decoupling, an initial schematic (Fig. 17) for simulating the power amplifier used ideal elements for the DC supplies, combined with s-parameters results from the Axiem EM simulations of the input and the output matching circuits (Fig. 18). Performance simulations for PAE and output power using Axiem EM simulations of the matching circuits in place of the original analytical MMIC simulations are shown in Fig. 19 over the frequency range of 3 to 6 GHz. Output power, efficiency (PAE), and gain are slightly less in comparison to the original performance simulation of the layout from Fig. 16.

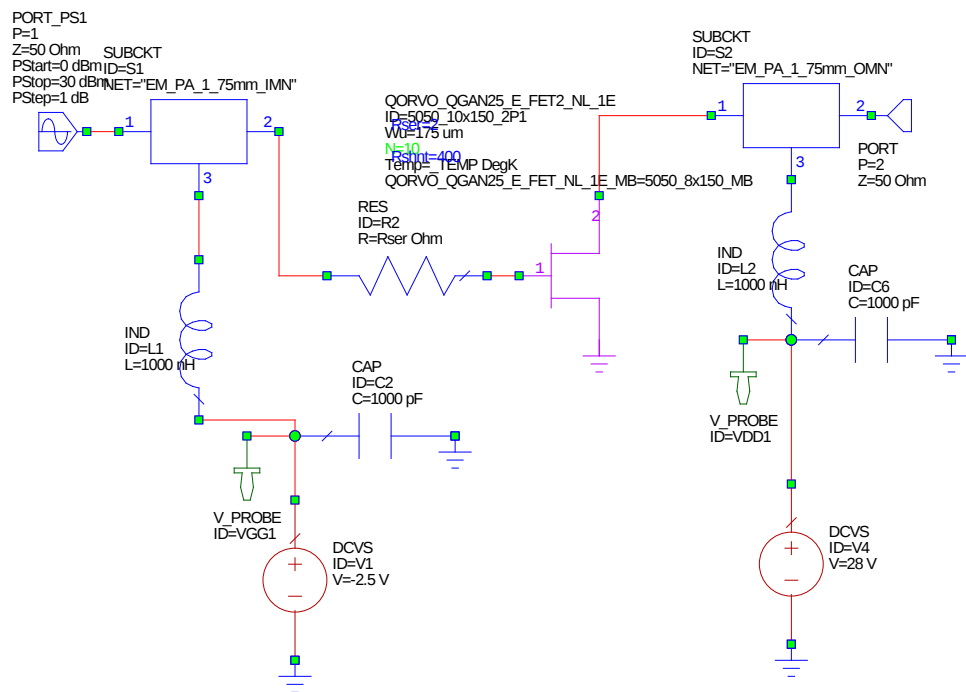


Fig. 17 Schematic of broadband amplifier with Axiem EM matching circuit simulations (ideal DC bias)

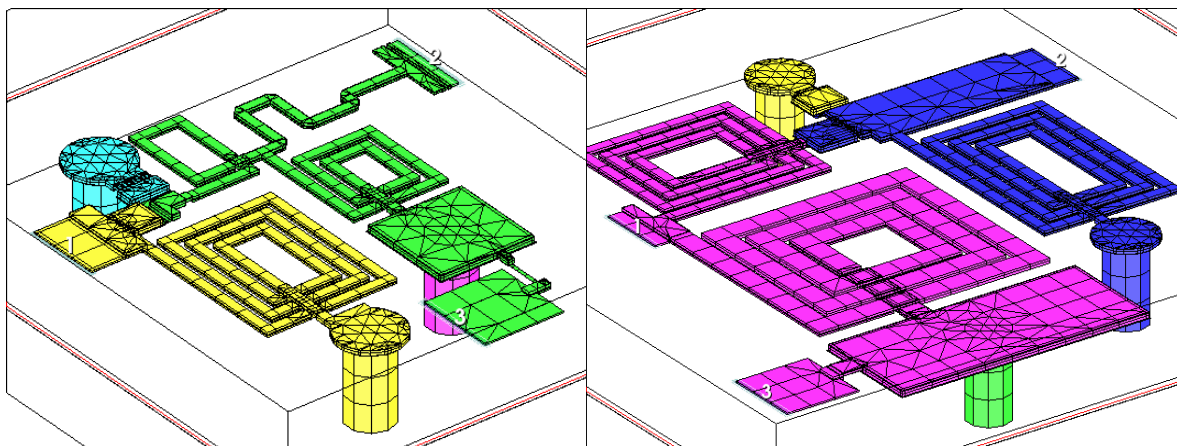


Fig. 18 Axiem 3-D EM node mesh of input (left) and output (right) matching circuits

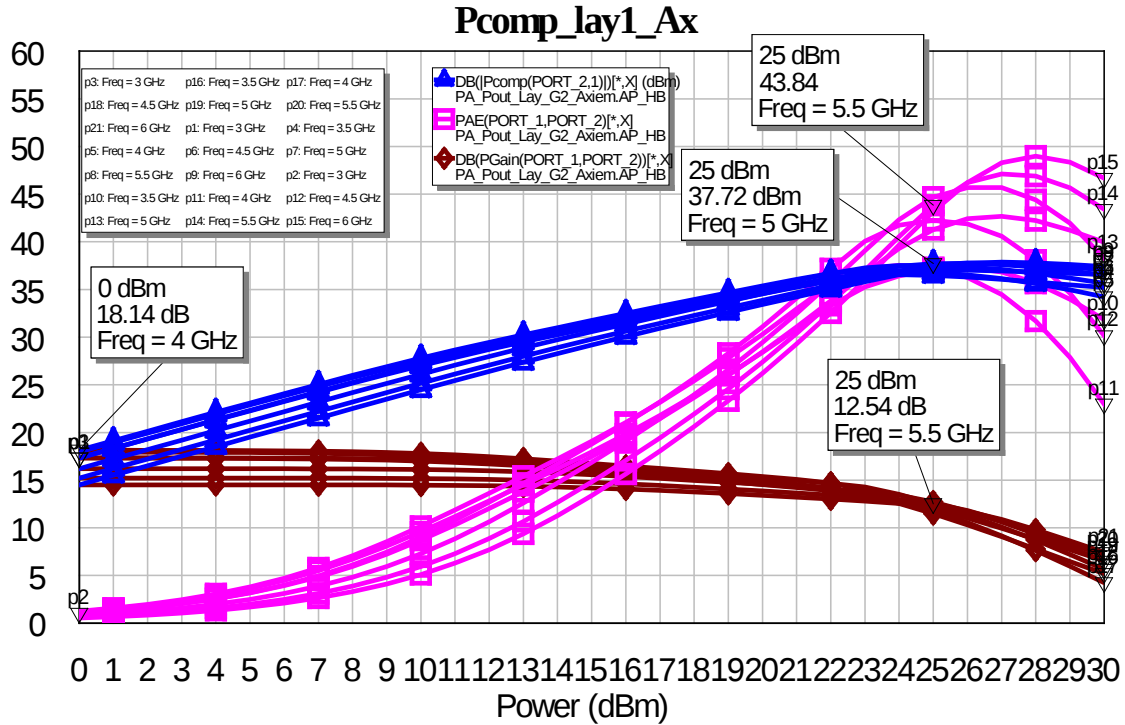


Fig. 19 Axiem (EM) performance simulations of MMIC (3–6 GHz, 28 V/180 mA) 1.75-mm HEMT power amplifier

4. A 2-Stage Broadband Power Amplifier Design

A driver stage for a 2-stage amplifier was needed to increase the overall gain and to flatten the gain slope, which has the typical roll-off of III/V HEMTs. The simplest, quickest design was a feedback amplifier with additional interstage matching elements to flatten the gain slope without sacrificing power and efficiency due to modifying the previously optimized final stage output match. Trying to flatten the gain by modifying the output match to the 1.75-mm HEMT would sacrifice power performance. Given more time, designing a driver stage using an approach similar to the output stage design but with additional margin to ensure that the output stage compresses well before the driver stage may have yielded better efficiency. However, the feedback amplifier was a compact layout and would only increase the overall size of the 2-stage amplifier by a moderate amount. A simple shunt inductor/series capacitor between the feedback amplifier and the original 1-stage power amplifier provided a simple low-pass filter to flatten the overall 2-stage amplifier gain. Since the feedback amplifier was small, it should easily fit on the reticle as a stand-alone test circuit. If there is sufficient room on the reticle, it would be nice to have the 1-stage power amplifier as a stand-alone circuit, but likely there is only room for the 2-stage amplifier.

The simple driver amplifier and 2-element low-pass matching circuit (Fig. 20) provided additional gain while also flattening the gain slope without having to modify the output match, which would compromise power and efficiency. After tuning the feedback amplifier and low-pass output match, the 2-stage amplifier gain is above 23 dB from 3 to 7 GHz, and the gain variation from 4 to 7 GHz is less than 1 dB (Fig. 21). Next, nonlinear simulations were performed to ensure that the driver stage was sufficiently capable of providing enough input power to the output stage to maintain good overall efficiency. Initially, an ideal $4\text{-} \times 125\text{-}\mu\text{m}$ (0.5-mm) HEMT driver amplifier with a $600\text{-}\Omega$ feedback resistor provided good performance for the 2-stage amplifier. Simulations of the feedback resistor and driver-stage amplifier over a range of $4\text{-} \times 75\text{-}\mu\text{m}$ HEMT up to $4 \times 125\text{ }\mu\text{m}$ was performed to try and optimize the overall gain, output power, and efficiency (PAE) of the 2-stage power amplifier. Best efficiencies were achieved with a $4\text{-} \times 110\text{-}\mu\text{m}$ HEMT feedback amplifier ($R = 600\text{ }\Omega$, $L = 2.2\text{ nH}$, $C = 0.35\text{ pF}$) with a saturated power up to 10 W at 28 V Vdd (Fig. 22).

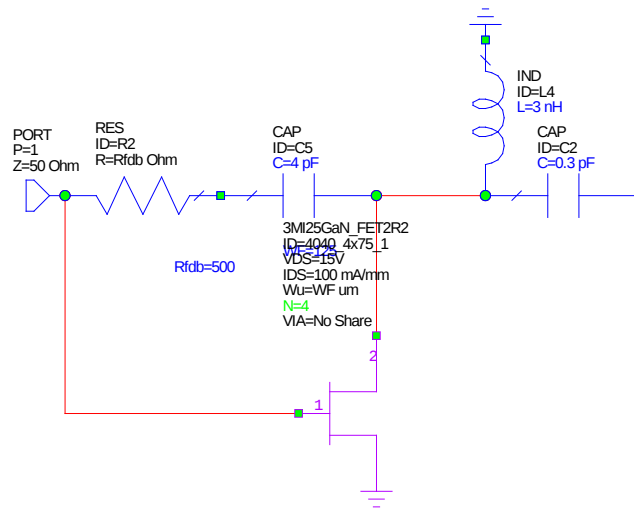


Fig. 20 Simple schematic of broadband driver amplifier with output low-pass circuit

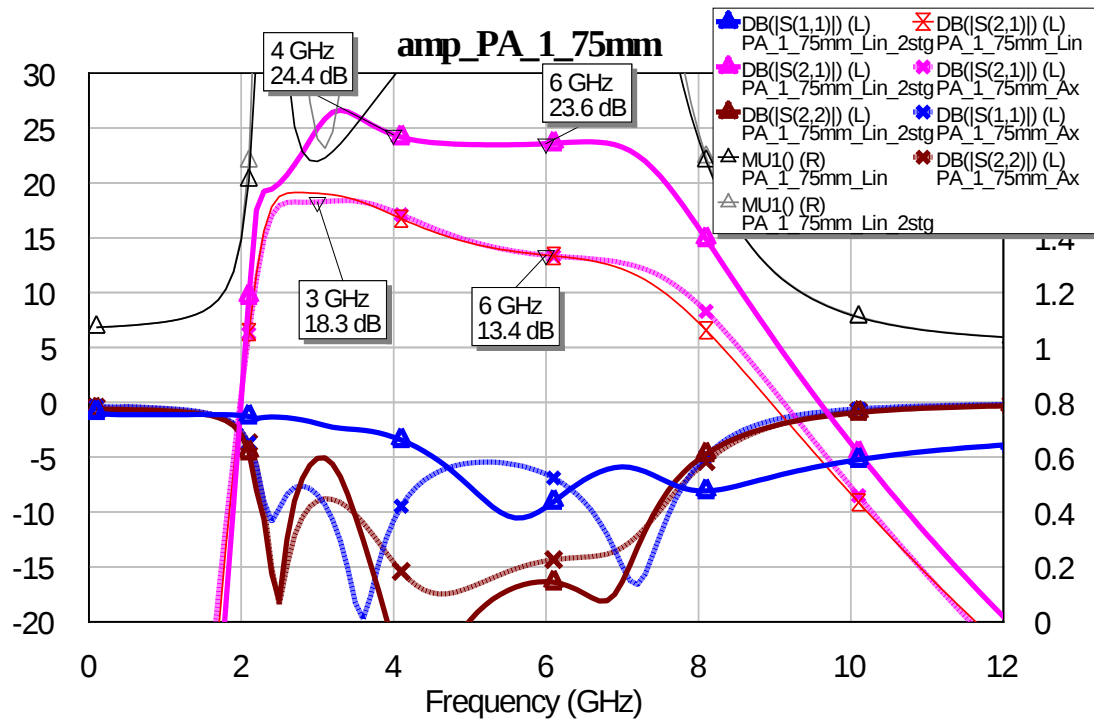


Fig. 21 Initial simulations of 2-stage amplifier (solid) vs. 1-stage power amplifier (dotted)

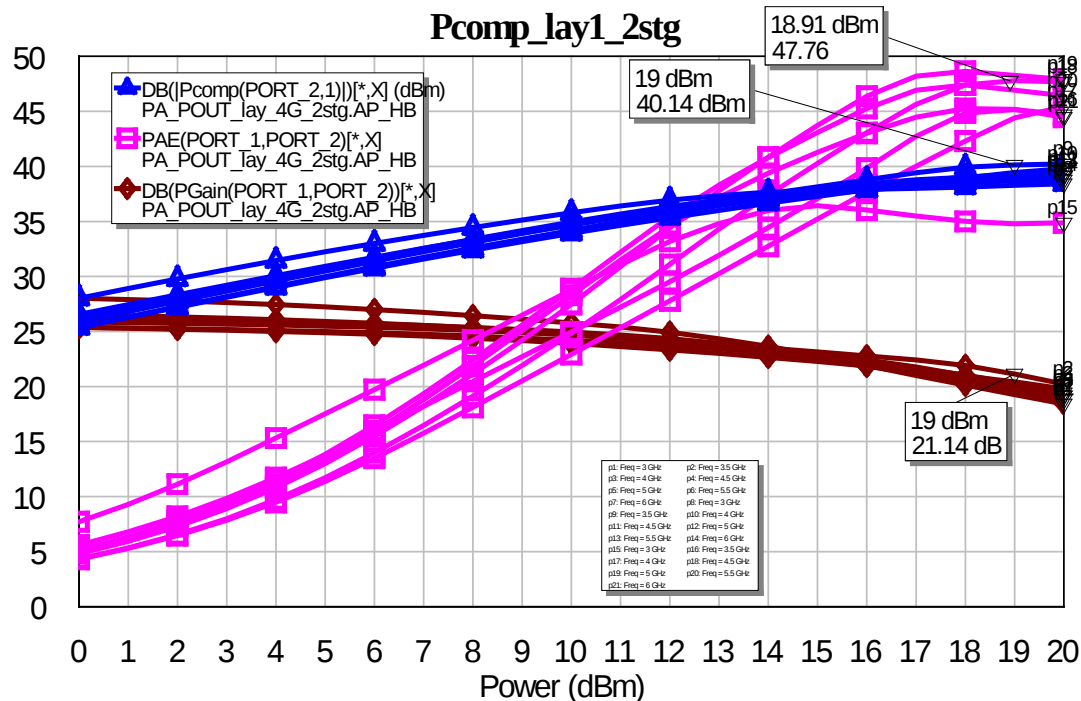


Fig. 22 Ideal feedback driver amplifier ($4 \times 110 \mu\text{m}$, 600Ω , $L = 2.2 \text{ nH}$, $C = 0.35 \text{ pf}$) 2-stage performance (3–6 GHz, 28 V) 1.75-mm HEMT power amplifier

Initially, an attempt was made to absorb the shunt inductor/series capacitor at the output of the driver stage into the shunt inductor/series capacitor at the input match of the 1.75-mm output stage, but there was insufficient impedance transformation ratio without the additional 2 matching elements. Fortunately, these 2 elements added to the new interstage match did not take up much area, and they provided DC access to the drain of the first-stage HEMT.

As a 1-stage amplifier, nonlinear performance simulations verified that a $4 \times 110\text{-}\mu\text{m}$ HEMT should be able to provide sufficient input drive to the output stage without premature compression (Fig. 23). Efficiencies are less than half the output stage, but the 0.44-mm HEMT first-stage driver amplifier is compact, simple, and has an overall efficiency dominated by the larger 1.75-mm second-stage HEMT. The driver stage adds about 25% to the width of the 2-stage layout (Fig. 24) compared to the single-stage layout of Fig. 12.

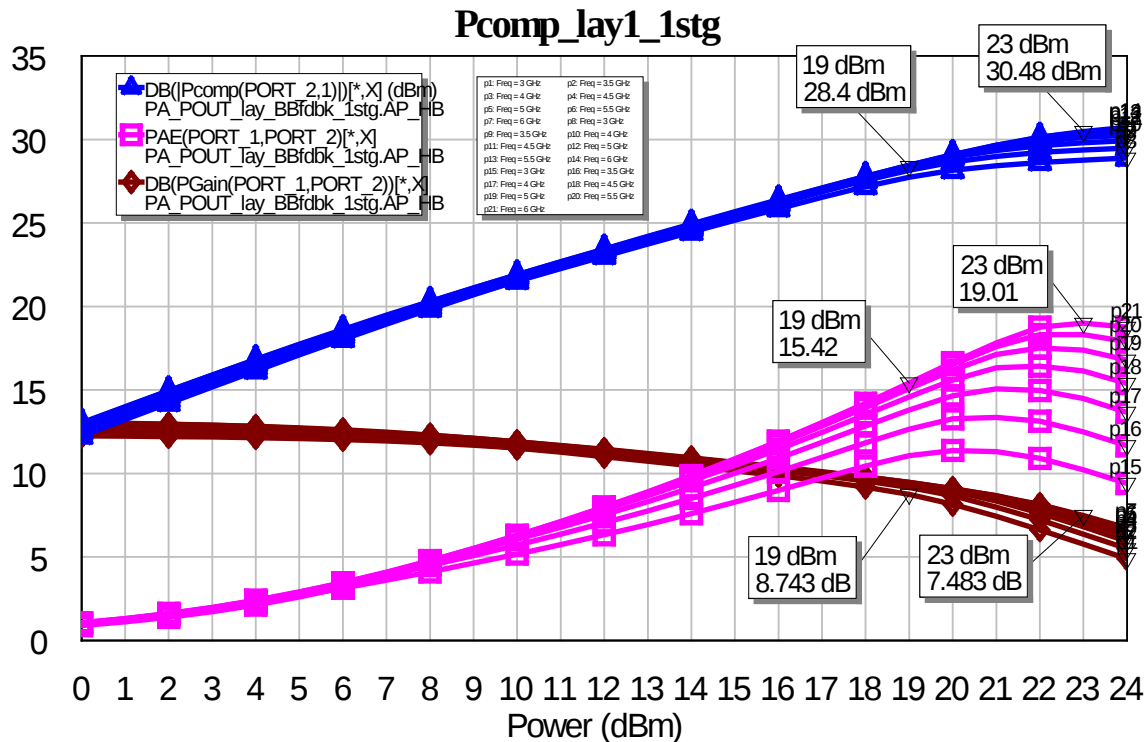


Fig. 23 Feedback driver amplifier ($4 \times 110\text{ }\mu\text{m}$, $525\text{ }\Omega$) single-stage performance (3–6 GHz, 28 V/44 mA)

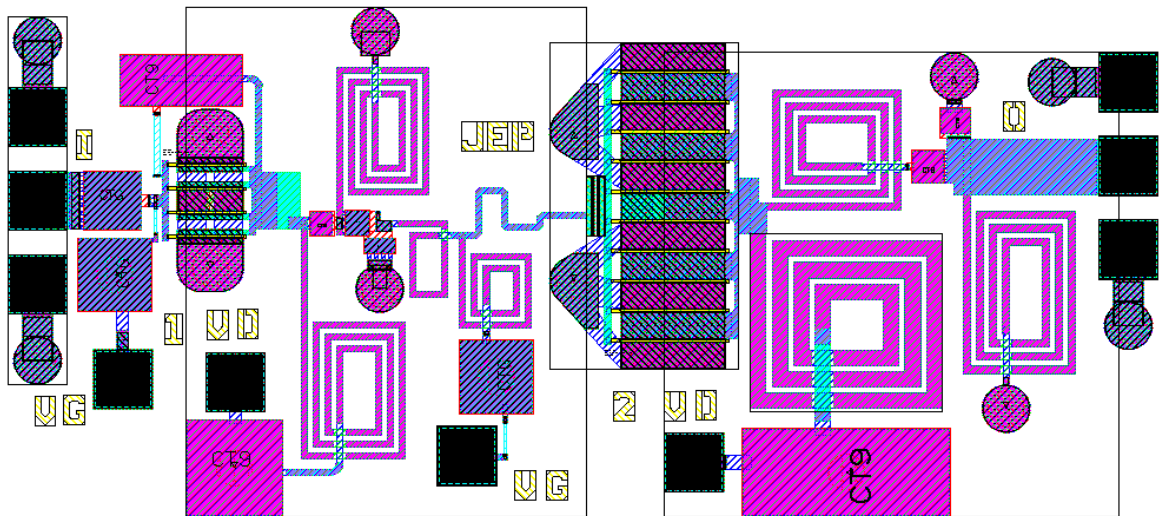


Fig. 24 Initial layout of 8- to 10-W 2-stage (3–7 GHz) 1.75-mm GaN HEMT power amplifier

5. New Models (PDK) and Translation from Gen1 to Gen2

Just as the designs were finalized to pass Gen1 design rule check (DRC), it was decided to switch to the newer Qorvo GaN Gen2 process from the traditional Gen1. It was anticipated that the changes to the device models and layouts would be minor, but translation of the Gen1 designs to Gen2 required more effort than expected. At first, only an Advanced Design System PDK was available for the Gen2 process, while these designs had all been created using MWO. Soon after, a Gen2 PDK was made available for MWO as well, but it required updating to the latest V13 MWO software followed by an additional translation process that was not entirely straightforward. Most, if not all, of the element names and descriptions changed from the Gen1 PDK to Gen2 PDK such that it was no longer as easy to copy schematics from previous MWO design files. While not insurmountable, the layout changes to convert Gen1 layouts to Gen2 were significant. An early hurdle was not having access to the Gen2 DRC checks. Once that hurdle was solved by Qorvo, progress on translating Gen1 layouts to Gen2 accelerated dramatically.

In addition to verifying the DRC rules from the translation, it was equally important to repeat Axiem EM simulations of the new Gen2 layouts to ensure that vertical 3-D circuit connections were not broken in the translation step. A combination of an extended deadline, partly to allow the Gen1 to Gen2 translation, and additional simulations with Axiem and Gen2 HEMT models led to improvements in the power amplifier matching circuits to restore some of the performance losses between the original simulations and the more accurate Axiem EM and Gen2 HEMT model simulations. The biggest change in restoring performance was in adjusting the

lumped elements of the output matching circuit to match the original MWO analytical simulations. The large shunt inductor that provides DC bias to the output HEMT needed to have wide metal traces to reliably handle the DC current. Originally, the space between this inductor and other elements was about twice the width of the traces in the spiral inductor, which was expected to have minimal coupling, but a large improvement toward restoring the desired output match was made by increasing the space to 3 times the trace width. As seen in the final DRC correct Gen2 layout of the 1-stage power amplifier (Fig. 25) and the same matching circuit in the Gen2 2-stage power amplifier layout (Fig. 26), the design is slightly increased in height and stretched about 100 μm in overall length. The rest of the elements in the matching circuits were stretched up or down in size after EM simulations to match the original analytical models of these elements, both individually and as integrated into final matching circuit layouts. As shown in Fig. 27, the impedance of the Axiem EM simulation of the final Gen2 layout versus the original ideal match and versus the original analytical output match is similar but with a slight undershoot of the impedance and a little more capacitance compensation in the final Axiem EM prediction. More time and effort could allow additional explorations to re-optimize the design to a different tradeoff of output power, bandwidth, efficiency, and gain.

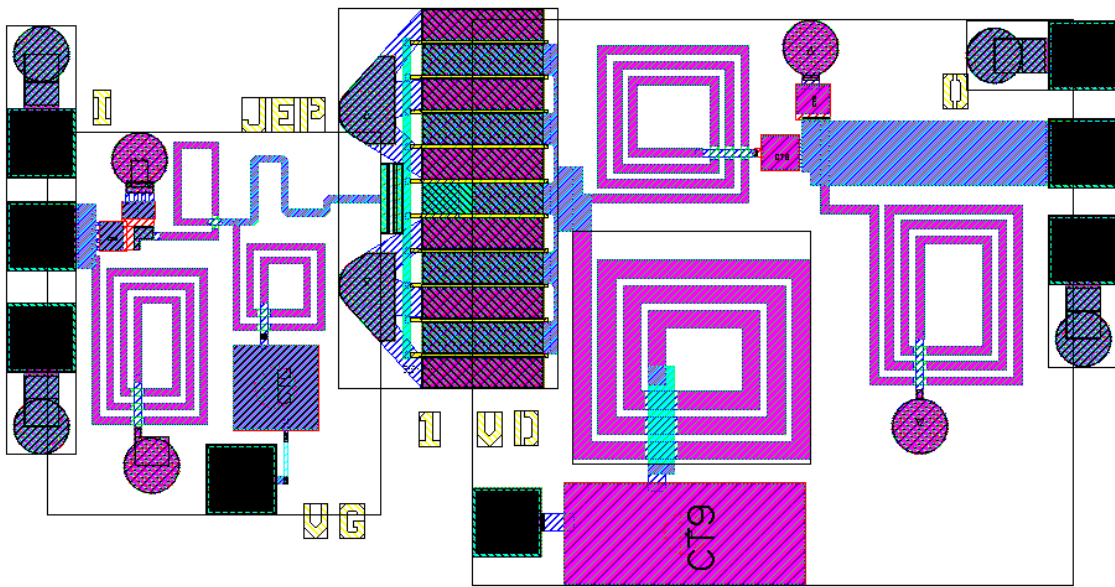


Fig. 25 Final layout of 8- to 10-W Gen2 1-stage (3–7 GHz) 1.75-mm GaN HEMT power amplifier (1.6 × 0.8 mm)

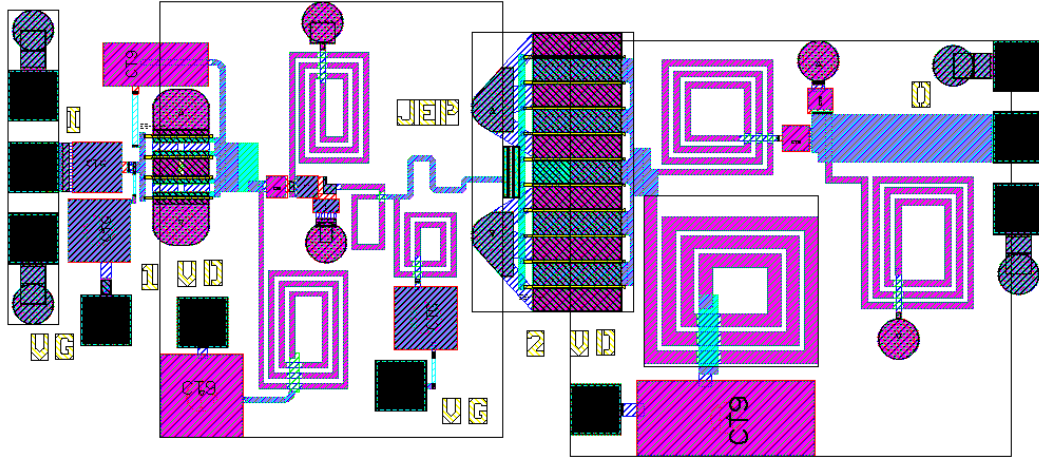


Fig. 26 Final layout of 8- to 10-W Gen2 2-stage (3–7 GHz) 1.75-mm GaN HEMT power amplifier (2.0 × 0.9 mm)

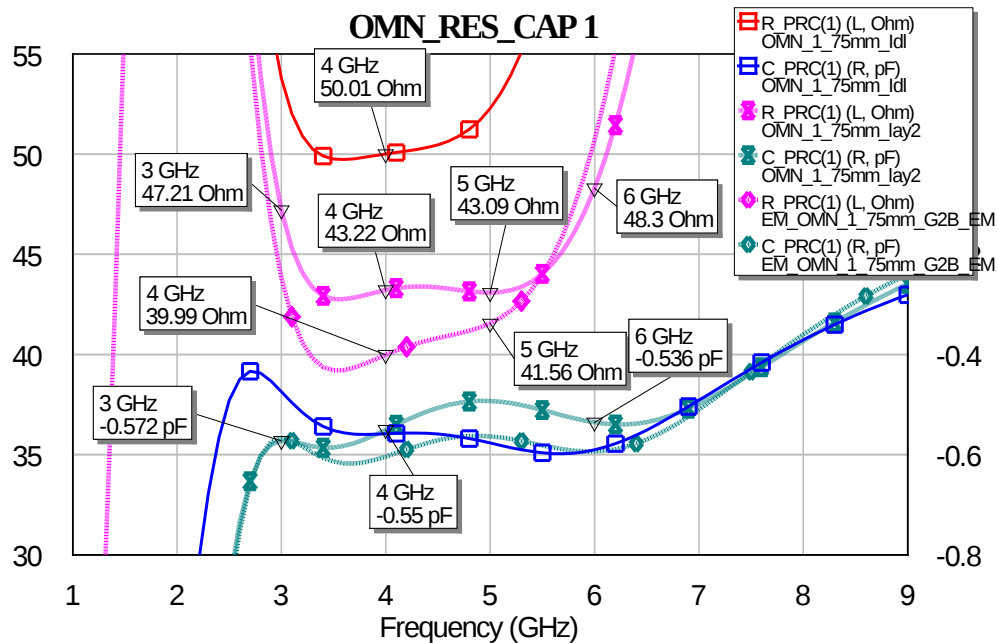


Fig. 27 Broadband impedance of output match ideal (solid) vs. MMIC (dotted) and Axiem EM of final Gen2 layout (dot/dash) (50 Ω || -0.54 pF)

An additional verification using ADS Momentum to EM-simulate the Gen2 layouts with the new PDKs gave extremely similar results to the Axiem EM simulations. Figure 28 shows a comparison of the real and imaginary parts of the admittance for the final Gen2 output match, with the blue solid lines showing the original ideal match (50 Ω || 0.54 pF) versus Axiem (solid magenta) and Momentum (solid brown). Both EM simulations show the output impedance as broader band but lower in impedance (higher conductance) compared to the original ideal lumped element matching circuit.

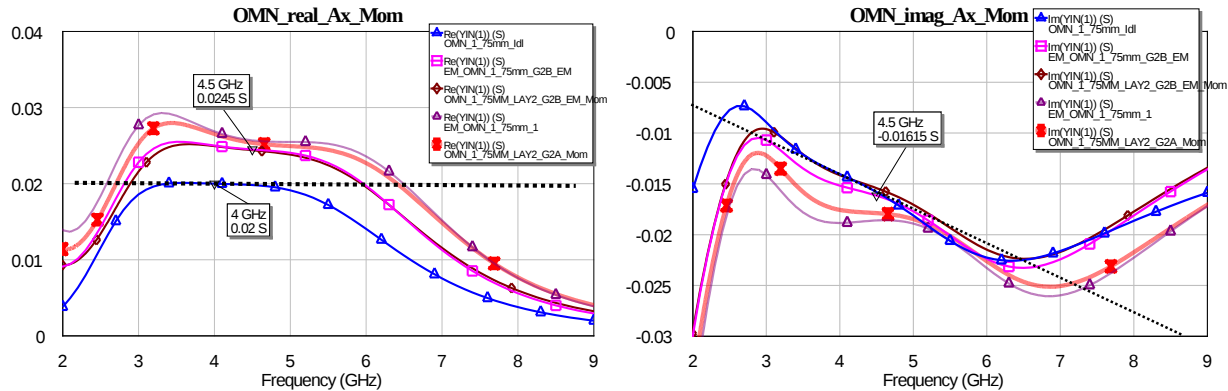


Fig. 28 Admittance of output match ideal (blue solid) vs. Axiem (solid magenta) and momentum (solid brown) ($50\ \Omega \parallel -0.54\ \text{pF}$)

6. Final Gen2 Performance Simulations ADS and MWO with Axiem and Momentum

While the design evolved from an ideal MWO design using a Gen1 0.25- μm GaN process to a DRC correct Gen2 layout with full layout EM simulations using both Axiem and Momentum, the performance was reduced from a 10-W ideal single 1.75-mm HEMT power amplifier biased from 28 to 35 V to about an 8-W MMIC power amplifier with broadband performance at 28 V. Load pull simulations of the 1.75-mm HEMT device showed the potential for 10 W over less than 3- to 6-GHz bandwidth at 35 V, while the additional inherent loss of the physical MMIC layout elements and design tradeoffs resulted in something closer to 7–8 W but over a broader 3- to 7-GHz band from a 28-V supply. Following are simulations from 3 to 6 GHz of the performance prediction using the Gen2 HEMT models in MWO V13 and Gen2 HEMT models using ADS2016.

There were some odd “kinks” in the nonlinear Gen2 simulations under certain conditions. It is not currently clear whether this is a realistic physical effect or just an anomaly. Measurements of the fabricated power amplifiers will show the accuracy of these predictions. There does not appear to be a large difference between Gen1 and Gen2 HEMT models, nor between the presumably more accurate EM simulations of the actual layouts using AWR’s Axiem versus Keysight’s Momentum. Figure 29 shows an MWO Schematic that uses simulations of the matching circuits imported from Keysight’s Momentum. Performance simulations using the Gen2 HEMT models with Axiem EM simulations of the matching circuits are shown in Fig. 30 at 28-V bias from 3 to 6 GHz. For comparison, a similar MWO performance using Momentum EM simulations of the matching circuits is shown in Fig. 31. Small signal performance of the final single-stage power amplifier is shown in Fig. 32, predicting about 19-dB gain at 2.6 GHz, dropping to about 15 dB at 7 GHz (28 V,

180-mA bias). The ADS GAN25_E PDK was used to simulate performance using Gen2 HEMT models and both Axiem and Momentum EM simulations of the final matching circuit layouts. A simple ADS schematic is shown in Fig. 33, which is used to generate the performance simulations with either Axiem EM or Momentum EM simulations of the final circuit layouts. Results using ADS Gen2 HEMT models with Axiem EM at 4.5 GHz (28 V) for the single-stage power amplifier predict 38.5 dBm (7.1 W) and 52% PAE at an input power of 26 dBm as shown in Fig. 34. Results of the nonlinear performance from 3 to 6 GHz of the single-stage power amplifier using ADS Gen2 and Axiem EM are shown in Fig. 35, which is comparable to the MWO Gen2 and Axiem EM performance simulations shown previously in Fig. 30. Similar ADS Gen2 HEMT simulations at 4.5 GHz and over the band 3 to 6 GHz, but with Momentum EM simulations, are shown in Figs. 36 and 37, respectively. The differences between the Axiem and Momentum EM simulations, and between ADS versus MWO with the Gen2 HEMT models, are slight.

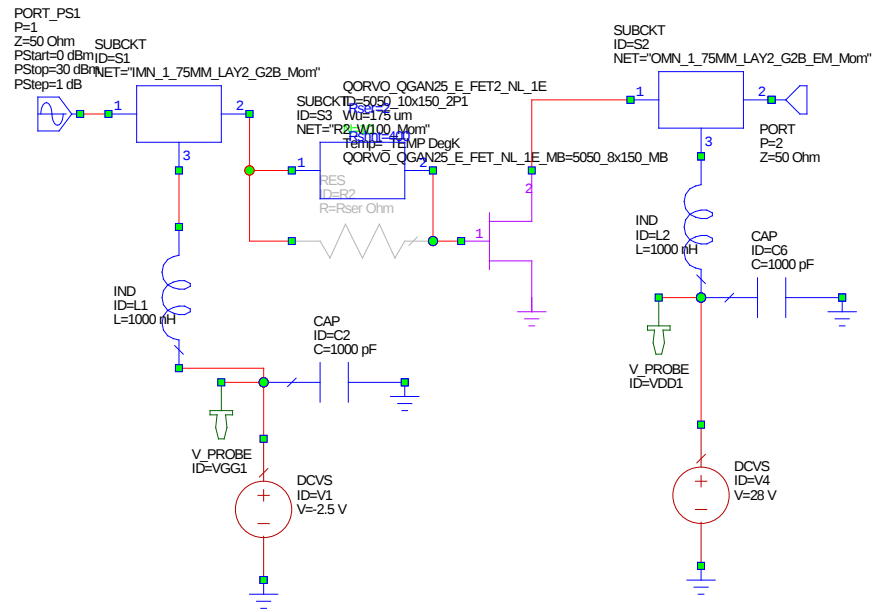


Fig. 29 MWO schematic of broadband amplifier with Momentum EM matching circuit simulations

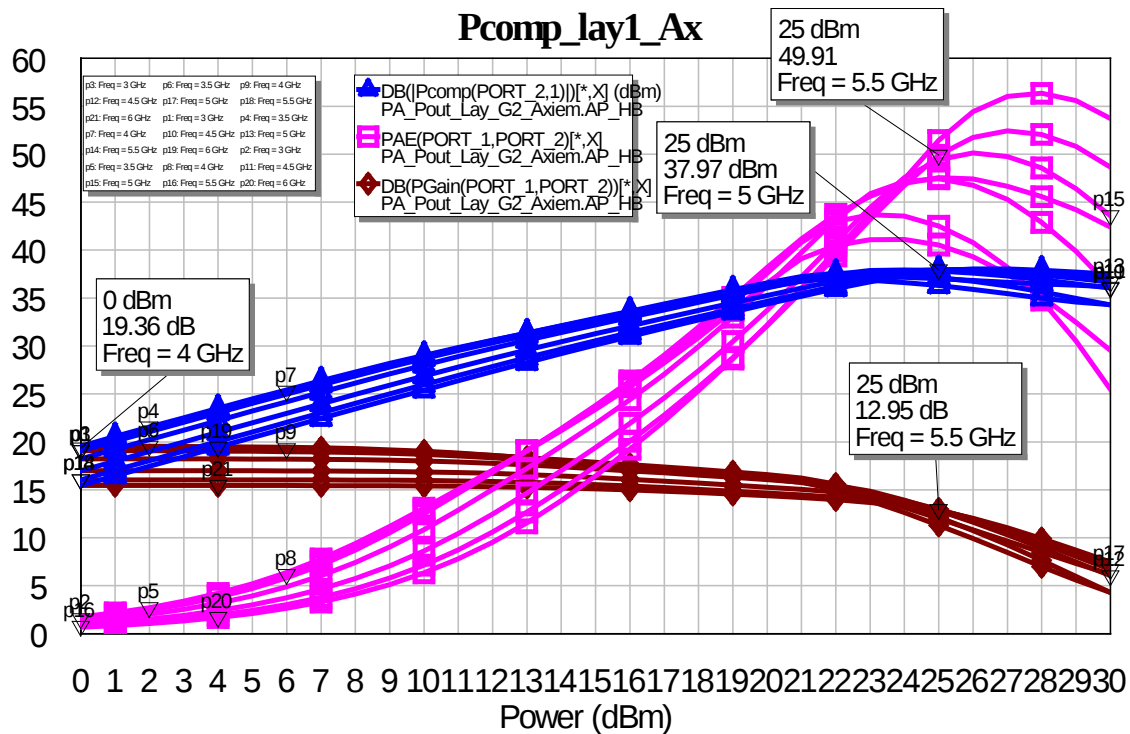


Fig. 30 Axiem (EM) Gen2 final performance simulations (3–6 GHz, 28 V/180 mA) 1.75-mm HEMT power amplifier

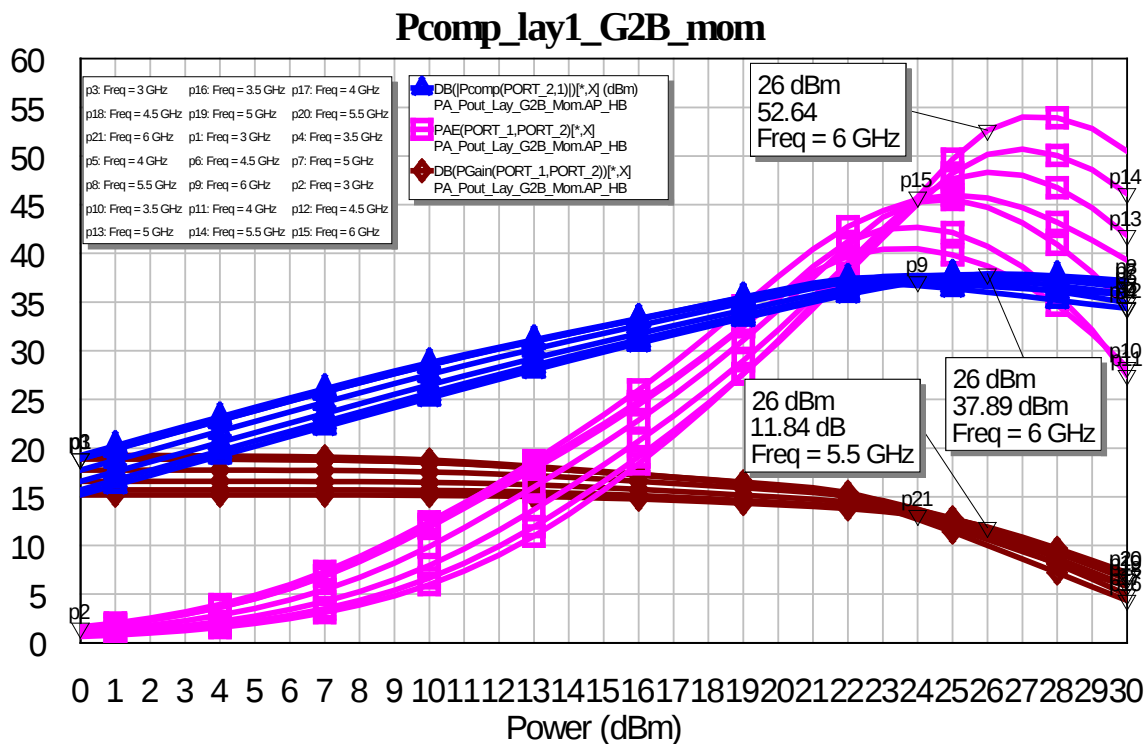


Fig. 31 Momentum (EM) Gen2 final performance simulations (3–6 GHz, 28 V) 1.75-mm HEMT power amplifier

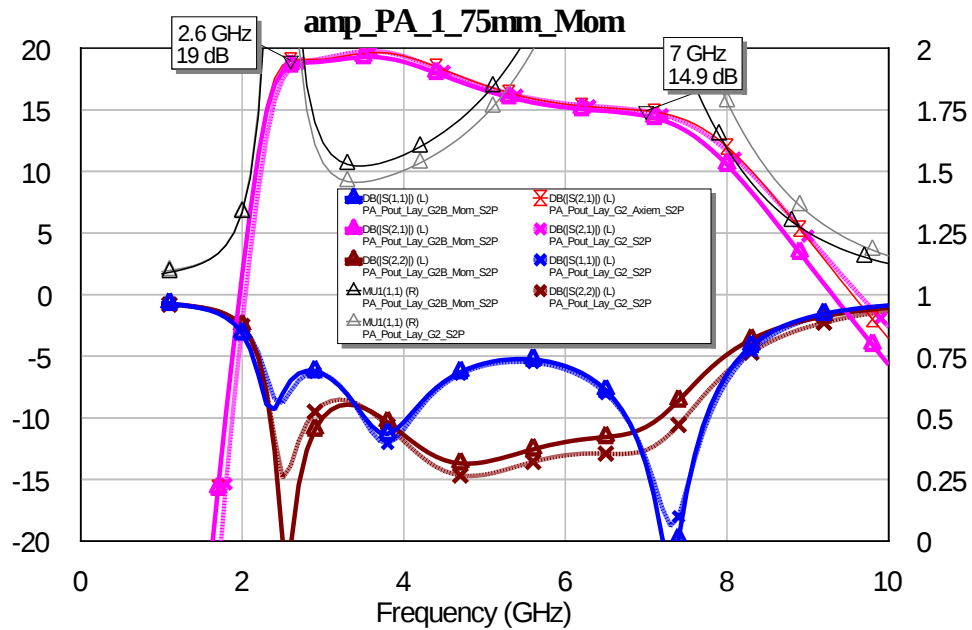


Fig. 32 Small signal EM Gen2 final performance simulations (28 V) 1.75-mm HEMT power amplifier



Fig. 33 ADS schematic of broadband amplifier with Momentum EM matching circuit simulations

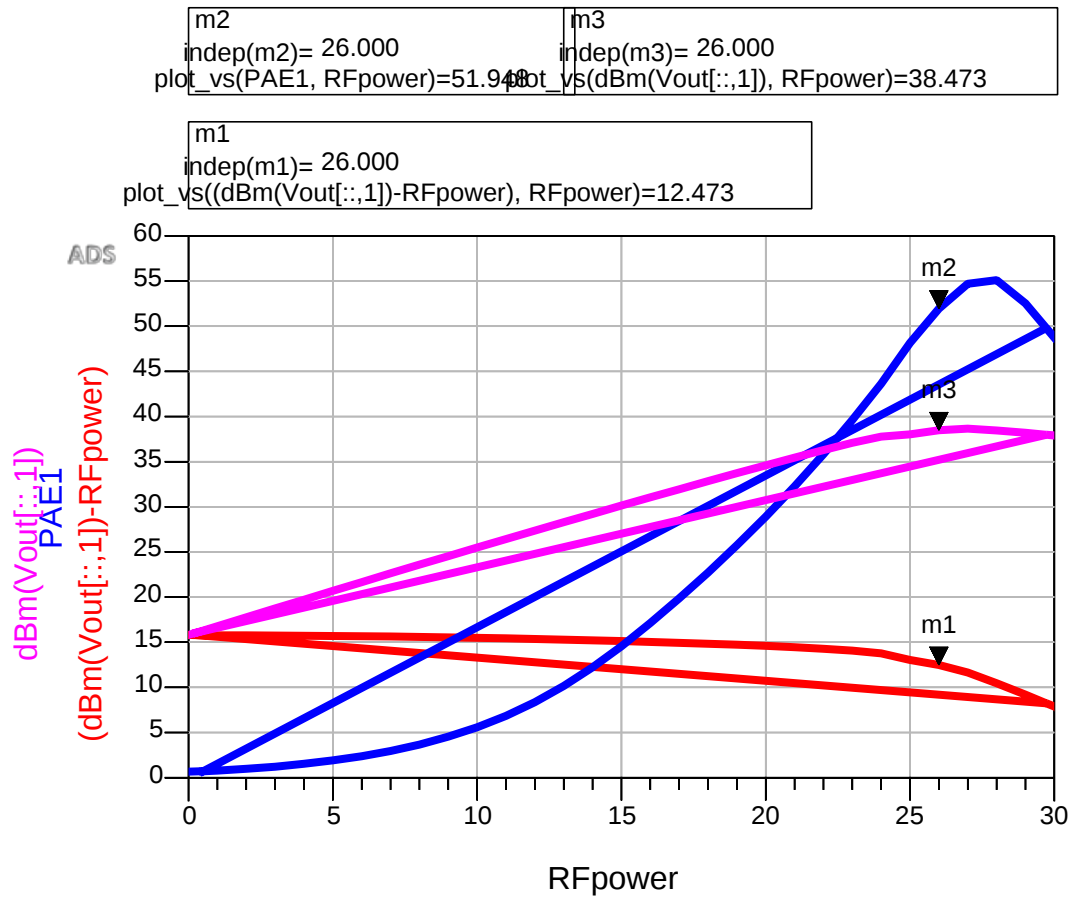


Fig. 34 ADS Gen2 final performance simulations with Axiem (EM) (4.5 GHz, 28 V) 1.75-mm HEMT power amplifier

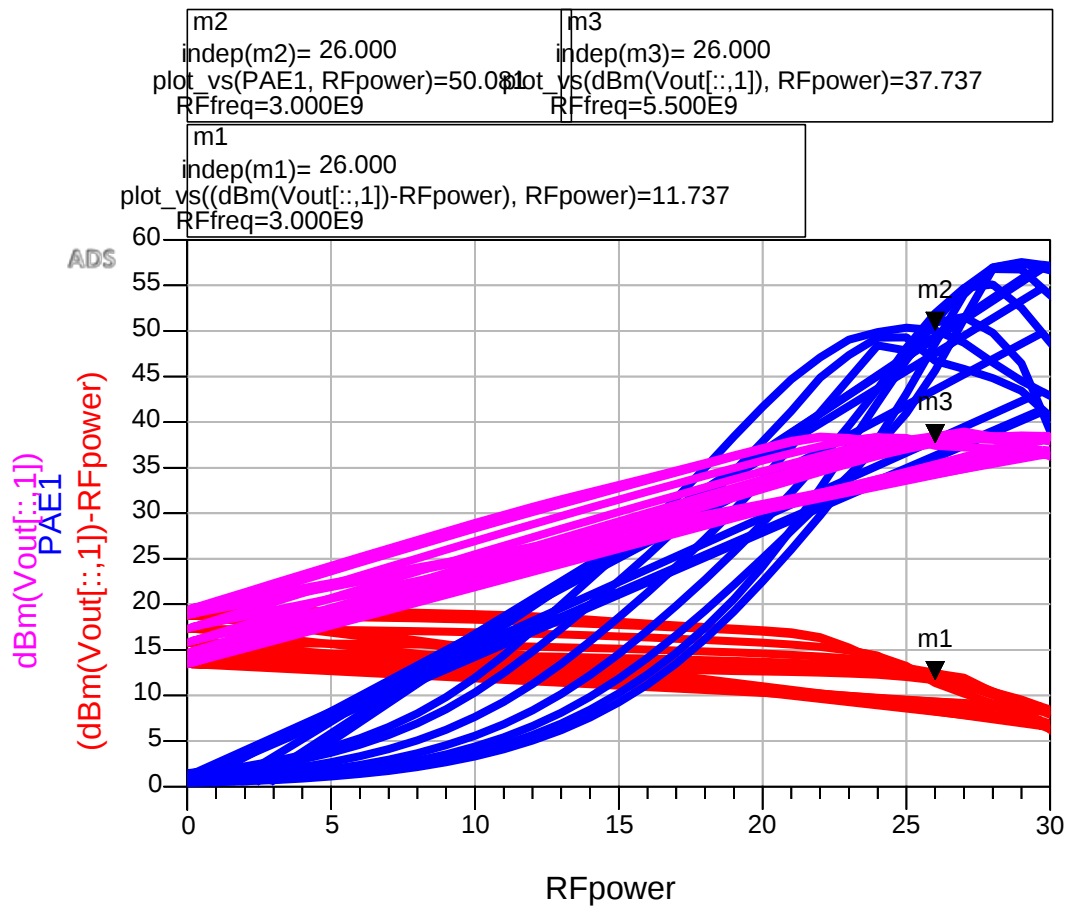


Fig. 35 ADS Gen2 final performance simulations with Axiem (EM) (3–6 GHz, 28 V) 1.75-mm HEMT power amplifier

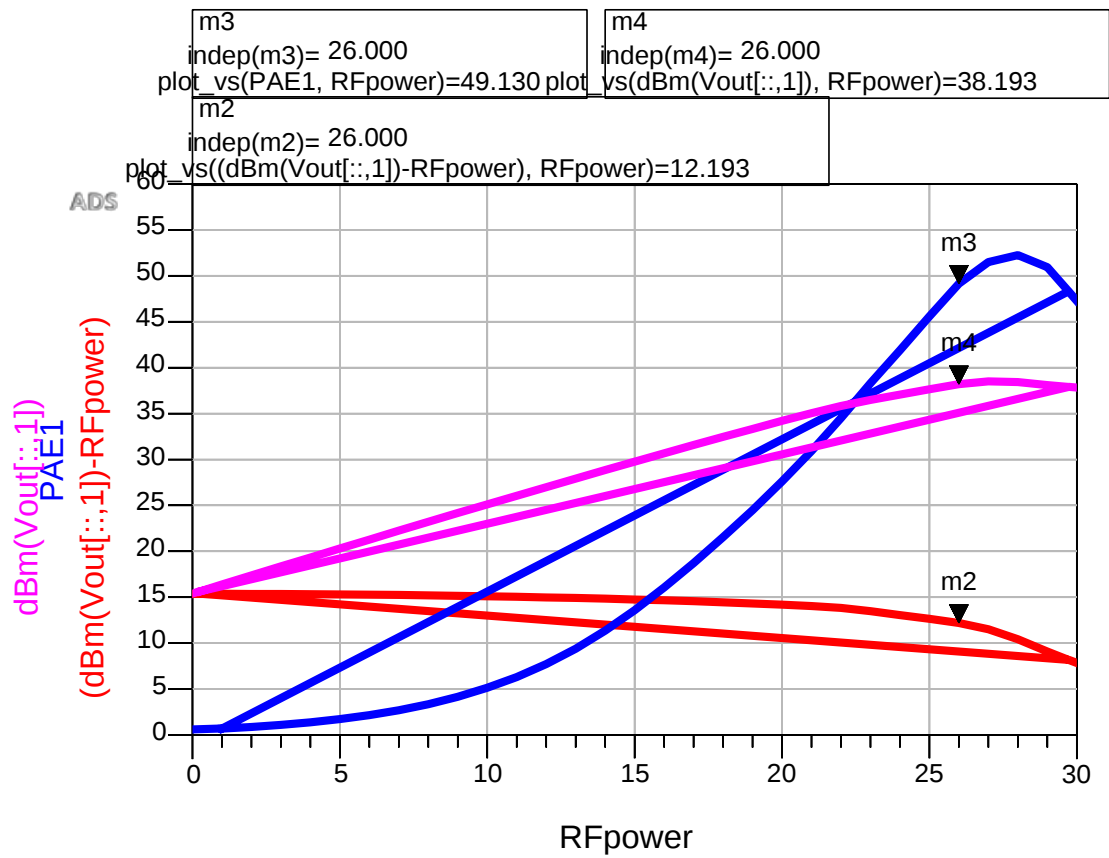


Fig. 36 ADS Gen2 final performance simulations with Momentum (4.5 GHz, 28 V) 1.75-mm HEMT power amplifier

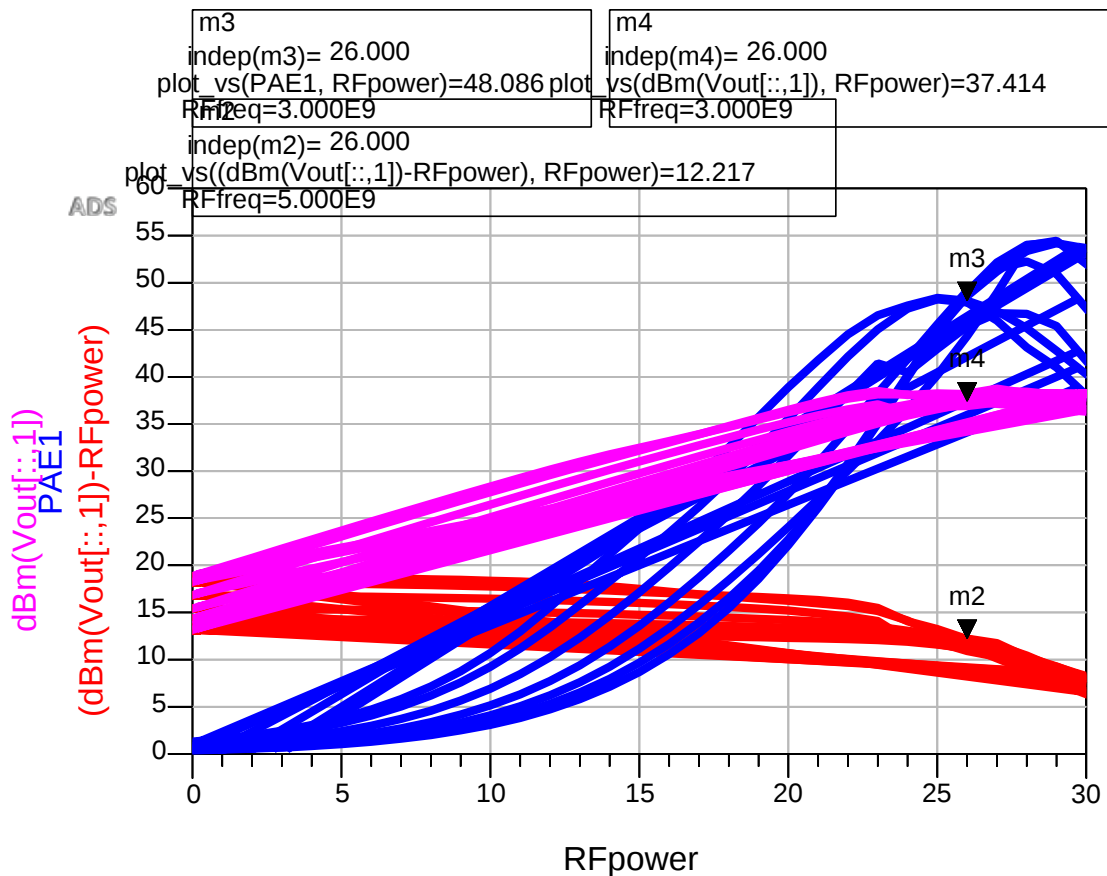


Fig. 37 ADS Gen2 final performance simulations with Momentum (3–6 GHz, 28 V) 1.75-mm HEMT power amplifier

An ADS schematic of the 2-stage amplifier with a feedback driver stage is shown in Fig. 38. Performance simulations of the 2-stage amplifier at 4.5 GHz and over the band 3–6 GHz are shown in Figs. 39 and 40. The output power is comparable to the single-stage amplifier but with less input power required (17 dBm) because of the additional gain of the driver stage. Efficiency is less than the single-stage amplifier because of the DC power consumption of the less efficient compact driver stage but is a very good 45% at 4.5 GHz with 38.85-dBm (7.7-W) output power at 17-dBm input drive (28 V, 225 mA). Small signal gain for the 2-stage amplifier using ADS with Axitem EM shows good flat gain with less than 1 dB slope from 4 to 6 GHz (Fig. 41).

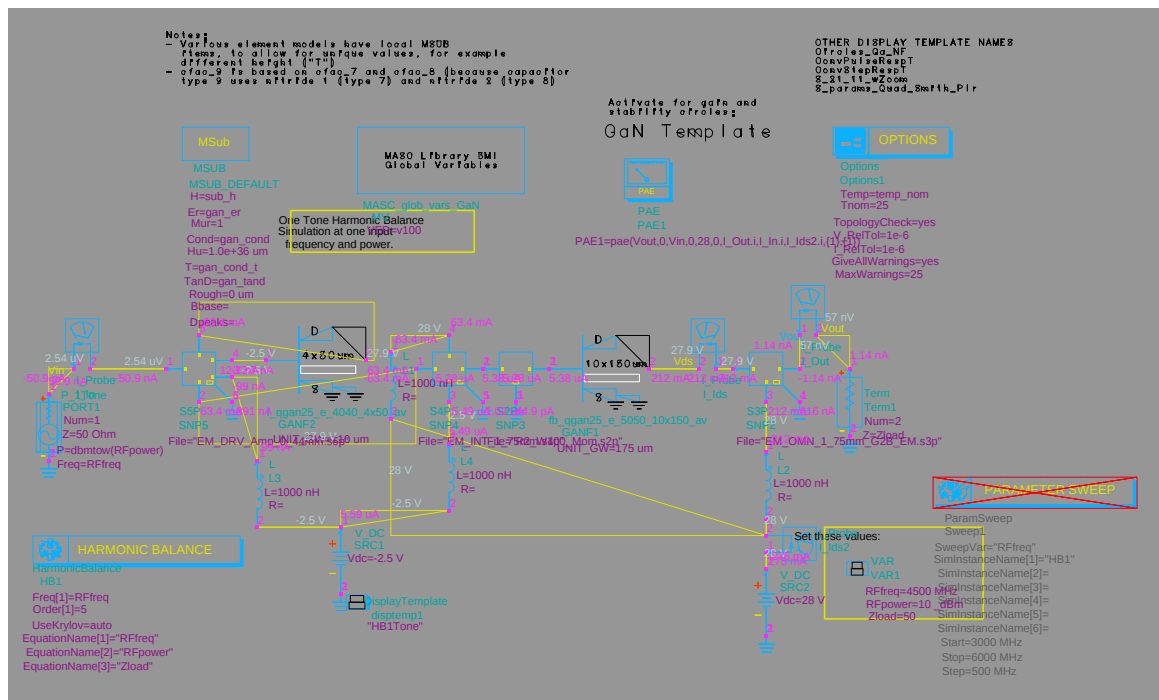


Fig. 38 ADS schematic of 2-stage amplifier with Axiem EM matching circuit simulations

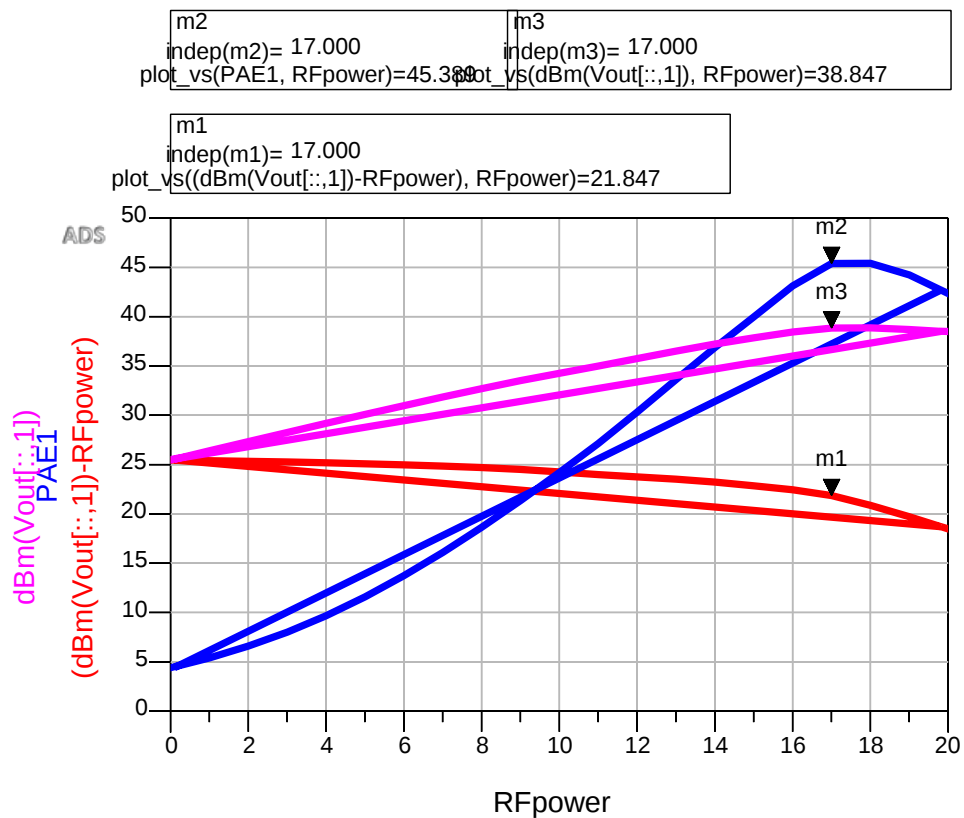


Fig. 39 ADS Gen2 final 2-stage performance simulations with Axiem (4.5 GHz, 28 V) 1.75-mm HEMT

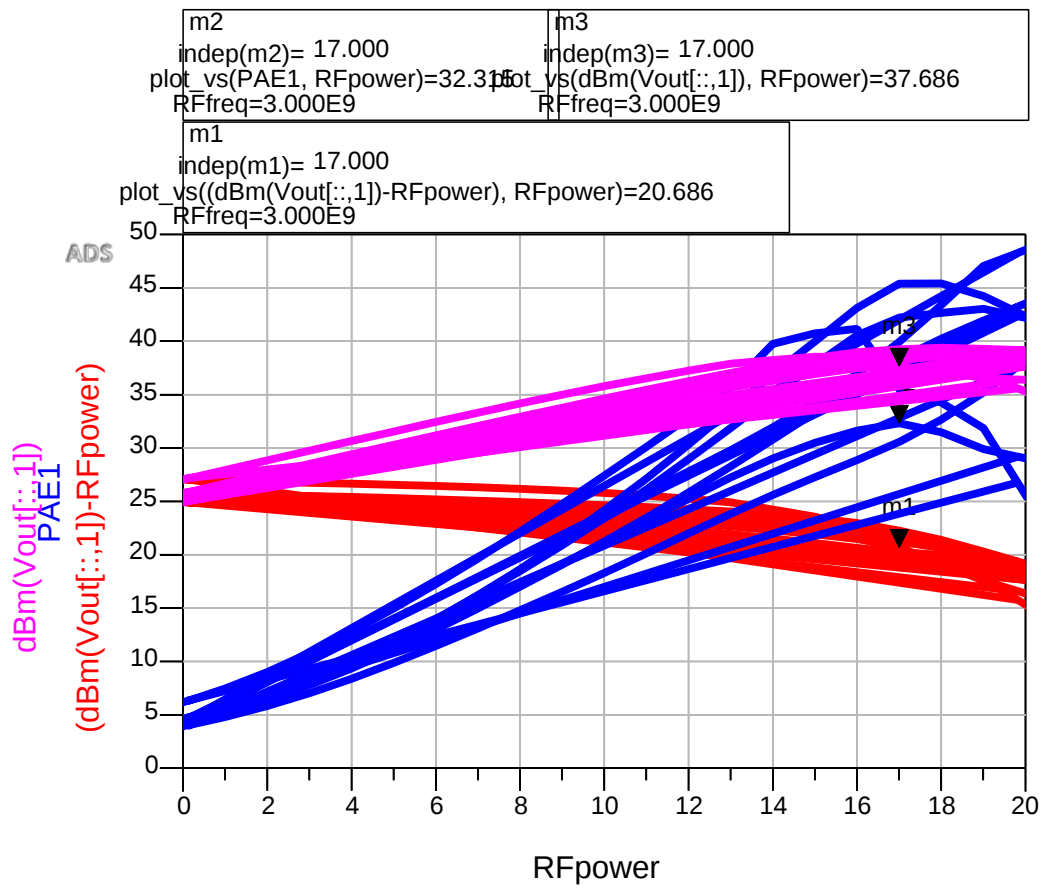


Fig. 40 ADS Gen2 final 2-stage performance simulations with Axiem (3–6 GHz, 28 V) 1.75-mm HEMT

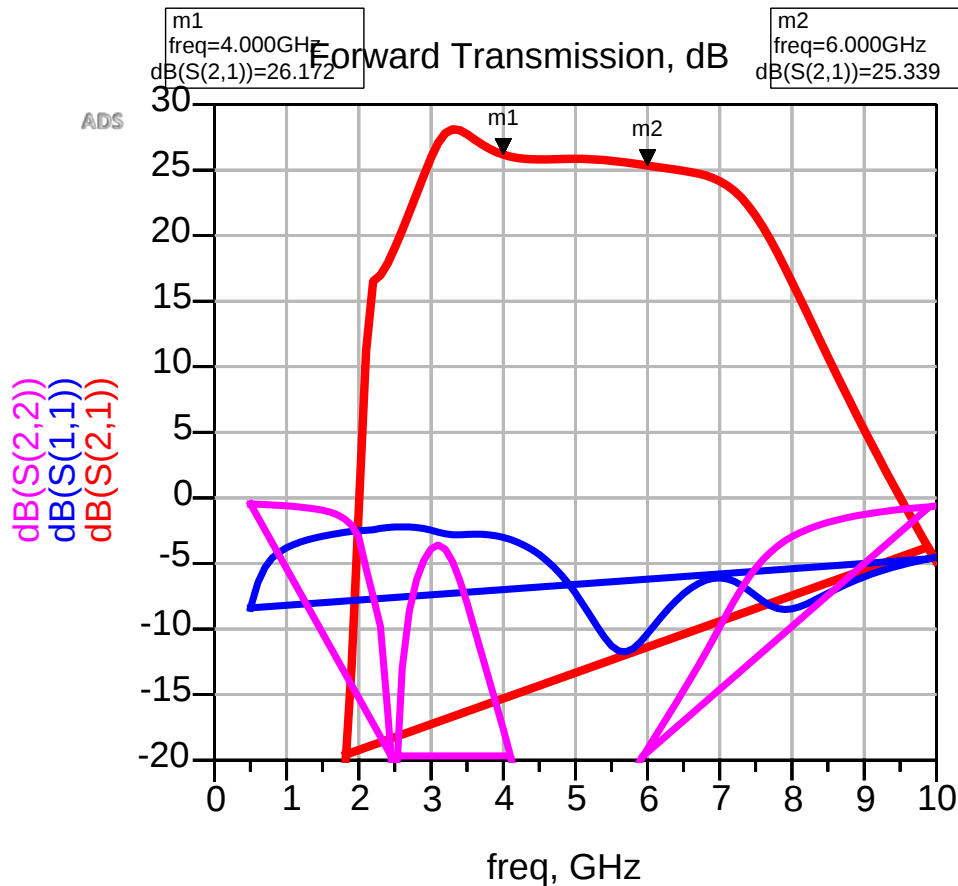


Fig. 41 ADS Gen2 final 2-stage small signal simulations with Axiem (28 V) 1.75-mm HEMT

7. Preliminary Ideal Design for 2 Parallel 1.75-mm HEMT Power Combiner

In addition to the 1.75-mm broadband power amplifier, a 3.5-mm power amplifier was implemented using 2 parallel combined 1.75-mm HEMTs. First, the ideal output match for a single 1.75-mm HEMT was transformed from a 50-Ω output match to 100 Ω so that 2 devices could be easily paralleled into a 50-Ω load. Figure 42 shows the ideal broadband output match from a single 1.75-mm HEMT transformed to a 100-Ω output match, as well as the composite schematic of the 2-way combined output match (Fig. 43). This simple lossless combiner circuit would need to be modified to supply DC bias, which should be relatively easy. The 2-way combiner output matching circuit has the same broadband return loss, with better than 20-dB return loss match to the ideal load from 2.8 to 5.6 GHz (Fig. 44).

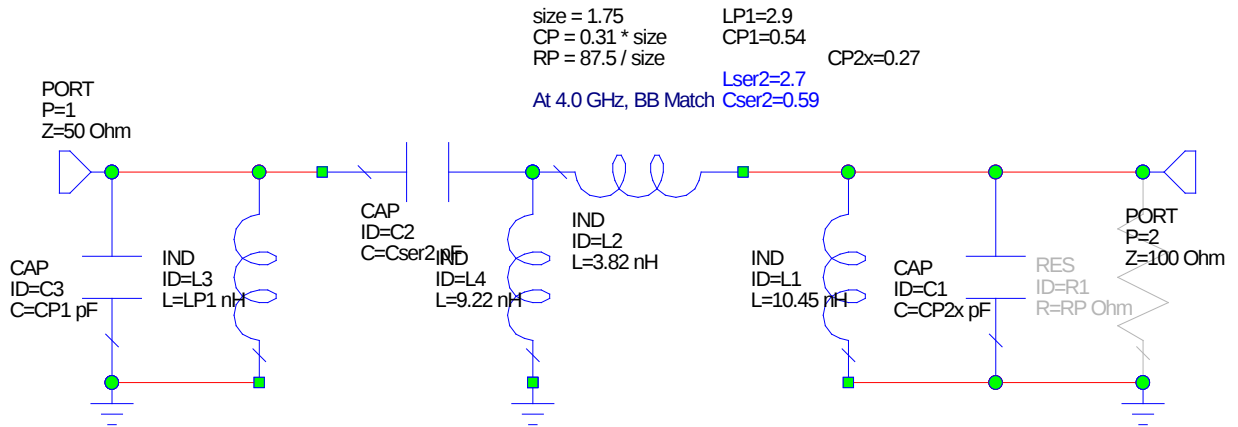


Fig. 42 MWO partial schematic for ideal parallel 2-way combiner circuit (10 × 1.75-μm HEMT)

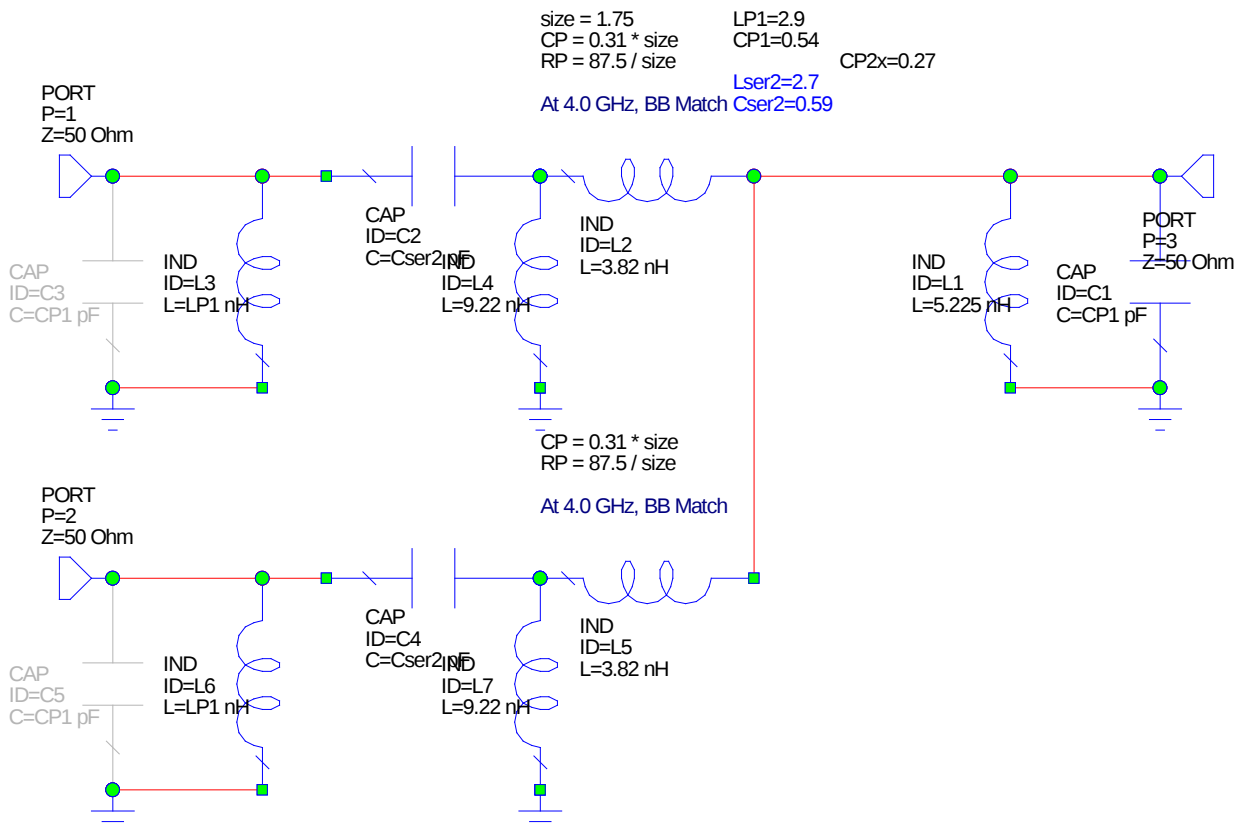


Fig. 43 MWO schematic for ideal parallel 2-way combiner circuit (2–1.75 mm HEMTs)

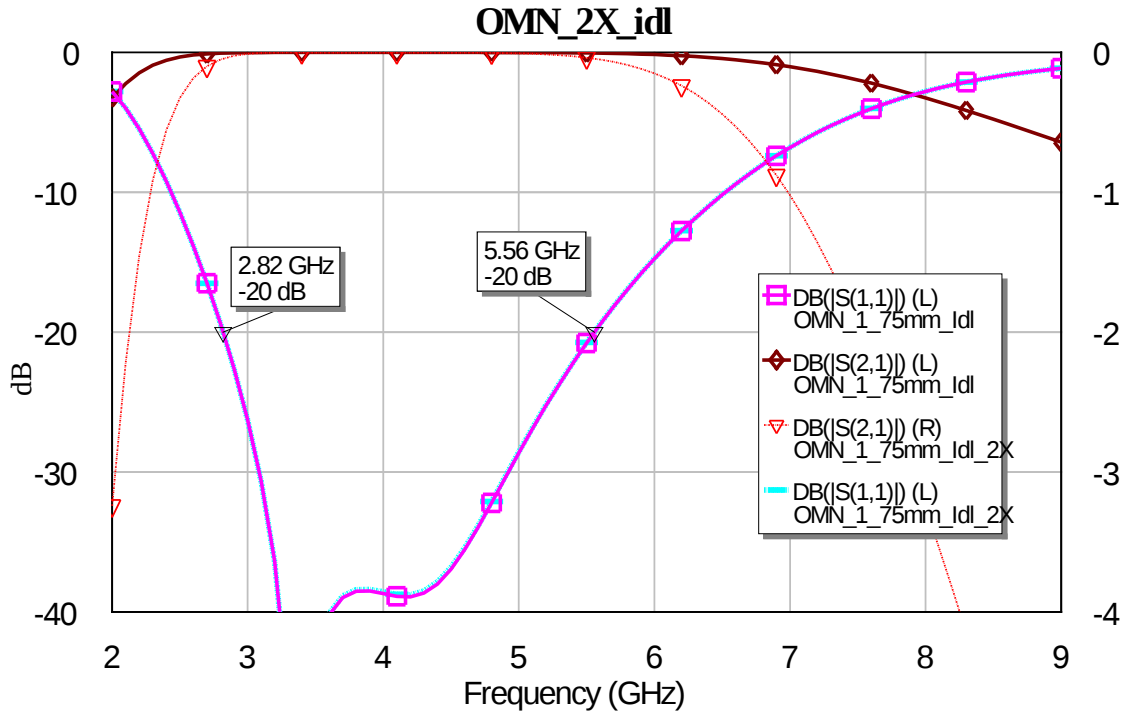


Fig. 44 Double-tuned ideal load match for parallel 2-way combiner circuit vs. single HEMT

MWO was used to simulate the performance of the broadband power amplifier as a 2-way combined (3.5-mm) HEMT power amplifier using the ideal output matching circuit from Fig. 43. The input of the 2-way combined amplifier was simulated as 2 of the coupled line ideal input matching circuits into a 25- Ω source. An input matching circuit into a 50- Ω source would require a redesign but should not change the gain or bandwidth of the 3.5-mm power amplifier. Output power would be expected to double (+3 dB), with similar efficiency and bandwidth compared with the single 1.75-mm HEMT power amplifier. Figure 45 shows the performance simulation from 3 to 5 GHz of a lossless matched broadband 3.5-mm HEMT single-stage power amplifier.

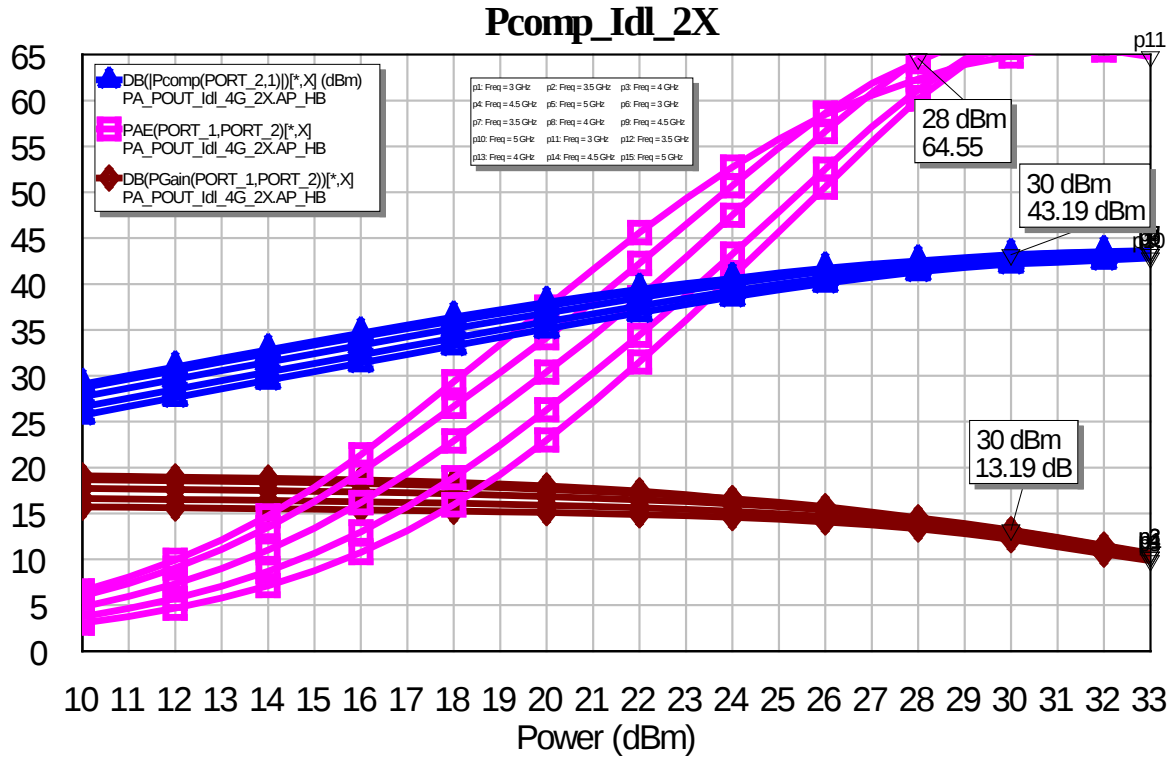


Fig. 45 MWO performance simulation of ideal 2-way combined (3–5 GHz, 28 V/ 360 mA) 3.5-mm HEMT power amplifier

A summary showing performance for the ideal lossless and lossy MMIC 1-stage 1.75-mm HEMT power amplifier at various frequencies, as well as an ideal lossless 2 parallel combined (3.5-mm) HEMT power amplifier, is shown in Table 1. Losses for the MMIC output match were calculated to be about 0.6 dB at mid-band, increasing up to 1 dB loss at the low end of the band (2.7 GHz). Additional losses on the MMIC input match would similarly affect small signal gain and power-added efficiency. Because of the reduced gain with frequency, the input power level at 3 GHz was 24 dBm, at 4 GHz it was 25 dBm, and at 5 GHz it was 27 dBm for the single-stage power amplifiers. This would represent approximately 3- to 4-dB compression for the Class A/B biased power amplifier. For the ideal 3.5-mm power amplifier combining two 1.75-mm HEMTs, the input power level is 3 dB higher, corresponding to 3-dB-higher output power, with the same large signal gain and ideal efficiencies (PAE) as the ideal 1.75-mm power amplifier. Nominal performance for the MMIC 1.75-mm HEMT amplifier is 8.1 W with 54% PAE at 4 GHz with 25 dBm input power. In comparison, the ideal version of the 1.75-mm power amplifier is 8.7 W and 65% PAE with the same 25-dBm input power. As expected, the 2-way combined ideal amplifier has double the output power with similar bandwidth and efficiency, showing 17.4 W and 65% PAE at a comparable 28-dBm input drive level.

Table 1 MWO Gen1 performance simulations of original MMIC, ideal 1.75 mm, and ideal 2-way, 3.5-mm broadband HEMT power amplifiers

Frequency	3 GHz	4 GHz	5 GHz	6 GHz
MMIC MWO	38.3 dBm	39.1 dBm 8.1 W	38.9 dBm	38.2 dBm
Pout PAE	50.5%	54%	54.7%	53.9%
Ideal PA 1.75-mm	38.7 dBm	39.4 dBm 8.7 W	39.2 dBm	...
Pout PAE	60.6%	64.6%	66.7%	...
Ideal 2-way, 3.5-mm	41.7 dBm	42.4 dBm 17.4 W	42.2 dBm	...
Pout PAE	60.6%	64.6%	66.7%	...

Later, Axiem EM and Momentum EM simulations were completed on the original amplifier matching circuits, which predicted a drop in the performance. Adjustments were made to the matching circuit layouts, especially the output matching circuit, which dominates the power performance of the amplifier, and a new layout was created to yield similar performance using Axiem and Momentum EM that were comparable to the original analytical MMIC element simulations. Next, the 0.25- μ m GaN library was changed from the earlier Gen1 to a newer Gen2 process. Most of the changes in the new Gen2 process involved the design rules, particularly affecting the passive MMIC elements, but there were also small changes to the HEMT nonlinear models. Performance simulations with the newer Gen2 HEMT models were completed with MWO V13 using the latest GAN25_E V1.0.0.1 PDK. Some additional simulations were performed with similar results using ADS2016 with the latest GAN25_E V1.1 PDK. A summary table showing updated performance using Axiem EM simulations of the matching circuits with the updated Gen2 layouts, as well as the updated Gen2 HEMT models, is shown in Table 2. In Table 1, the original GAN25 Gen1 HEMT models using MWO PDK GAN25 V1.0.10.4 were used for simulations. For comparison, Table 2 contains updated performance predictions using the Axiem EM simulations of the updated (Gen2) layout but uses Gen1 nonlinear HEMT models, followed by performance predictions using the newer Gen2 nonlinear HEMT models with the Axiem EM simulations of the original Gen1 layout, and with the updated final Gen2 layout.

Table 2 MWO with Axiem EM and Gen2 performance simulations of new layout MMIC (Gen1 + Axiem), original MMIC (Gen2 + Original MWO), and new layout MMIC (Gen2 + Axiem) HEMT power amplifiers

Frequency	3 GHz	4 GHz	5 GHz	6 GHz
Updated MMIC Pout	37.9 dBm	38.9 dBm 7.8 W	38.9 dBm	38.1 dBm
PAE (Gen1/Axiem)	47.8%	53.9%	56.6%	57.1%
Original MMIC Pout	37.7 dBm	38.3 dBm 6.8 W	38.2 dBm	38.4 dBm
PAE (Gen2/MWO)	46.5%	46.7%	49.3%	53.7%
Updated MMIC Pout	37.5 dBm	38.0 dBm 5.8 W	38.2 dBm	38.2 dBm
PAE (Gen2/Axiem)	44.7%	44%	48%	52.6%

Again, to create Table 2, because of the reduced gain with frequency, the input power level for 3 and 4 GHz was 23 dBm, at 5 GHz it was 25 dBm, and at 6 GHz it was 26 dBm for the single-stage power amplifiers (Gen2). This would represent approximately 3- to 4-dB compression for the Class A/B-biased power amplifier. For the updated Gen2 layout, but using the Gen1 nonlinear HEMT model, the single-stage 1.75-mm power amplifier is predicted to have a nominal performance of 7.8 W with 54% PAE at 4 GHz with 26-dBm input power, which is close to the original design performance simulations. Performance using the Gen2 nonlinear model is moderately less, particularly at 4 GHz, but was not much different at 3 and 6 GHz at the band edges compared to the Gen1 HEMT model. It is not clear if the performance change is due to a slight shift in HEMT model parasitics with the Gen2 process or if it is due to a more realistic fit of the nonlinear HEMT model. Using the Gen2 HEMT model with the original analytical MWO models for the matching circuits results in less output power and efficiency at the center frequency of 4 GHz, predicting 6.8 W and 46.7% PAE at an input power of 23 dBm. Adding the Axiem EM simulation of the final updated (Gen2) layout predicts a small loss in performance of 0.3 dB and 3% less PAE at 4 GHz while predicting nearly similar performance between the Axiem EM versus the original analytical MMIC models at 3, 5, and 6 GHz.

8. Gen2 HEMT Re-Simulations

While the original power amplifier designs were based on Gen1 models, the final layouts were to be fabricated in the Gen2 0.25- μm GAN_E process. Some final design re-simulations were performed to evaluate the performance differences with the Gen2 HEMT models. Given additional time, the power amplifier performance could be re-optimized. It appears that, at these frequencies and for this power amplifier design, the differences between the Gen1 and Gen2 simulations are insignificant, probably similar to nominal wafer-to-wafer process variations. Some early ideal simulations indicated powers closer to 10 W, but looking back at the load pull simulations from Figs. 6 and 7, the input power level of 29.5 dBm was probably too high, and the HEMTs were driven well into compression. Also, the initial design was intended as a compromise for a DC bias of 28 to 35 V, where 10 W was possible, ideally at 35 V, but 7.5 W was more realistic for a 28-V dB bias. Load pull simulations were performed with the original Gen1 models using 25 dBm of input power at 4 GHz and 28 V for a more realistic output power of 39.6 dBm (Fig. 46).

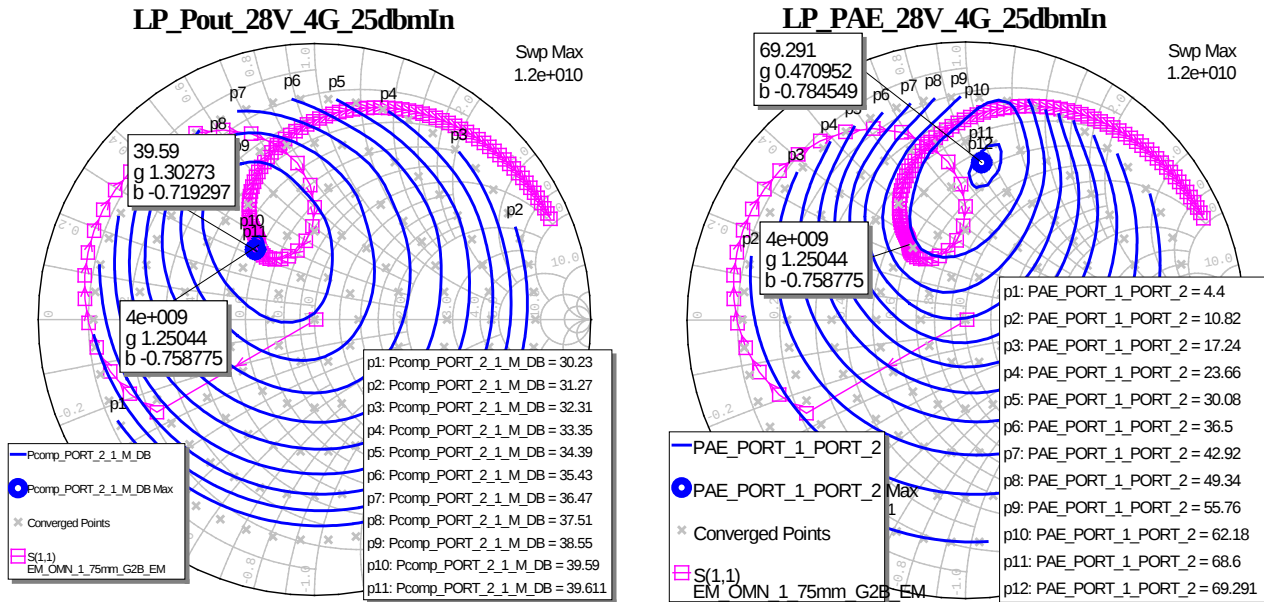


Fig. 46 1.75-mm HEMT load pull re-simulation 4-GHz, 28-V 25-dBm input max pout 39.6 dBm: (38.4 Ω || -0.57 pF); max PAE 69%: (106 Ω || -0.62 pF)

Note the final Axiem EM simulation of the final output match overlaid on the load pull simulation is fairly close to the optimal impedance, and this simulation is in close agreement to the 39.1-dBm value in Table 1 when you factor in about 0.6 dB of loss in the MMIC output matching circuit. A more realistic input drive level with a 3- to 4-dB gain compression in a re-simulation of the power amplifier using the newer design kit with Gen2 HEMT models predicts 38.6 dBm output power for an ideally lossless matching circuit at an input power of 23 dBm (Fig. 47). Note the greater than 10-W output power (40.1 dBm) with 29.5 dBm input power, which is overly gain compressed. This 38.6-dBm output power compares well to the 38.0-dBm value in Table 2 when you factor in the 0.6 dB of matching circuit loss. Looking back at the impedance of the final output matching circuit, the real part of the impedance was lower than the ideal case to increase gain bandwidth. This would likely improve performance at a DC bias of 28 V and lower but would not perform as well at 35 V, which should yield higher output power if the output matching circuit real part (resistance) were increased. A dynamic load line simulation (Fig. 48) showing the DC IV curves of the 1.75-mm Gen2 HEMT overlaid with an ideal design and the final simulations of the MMIC at 28 V and 23 dBm of input power at 4 GHz shows a reasonable output match. A dotted, purely resistive load line of 46 Ω , as shown on Fig. 48, is close to the 50- Ω original target for this design and represents a little less than 6 W (37.6 dBm) of RF power at the HEMT at a 28-V DC bias.

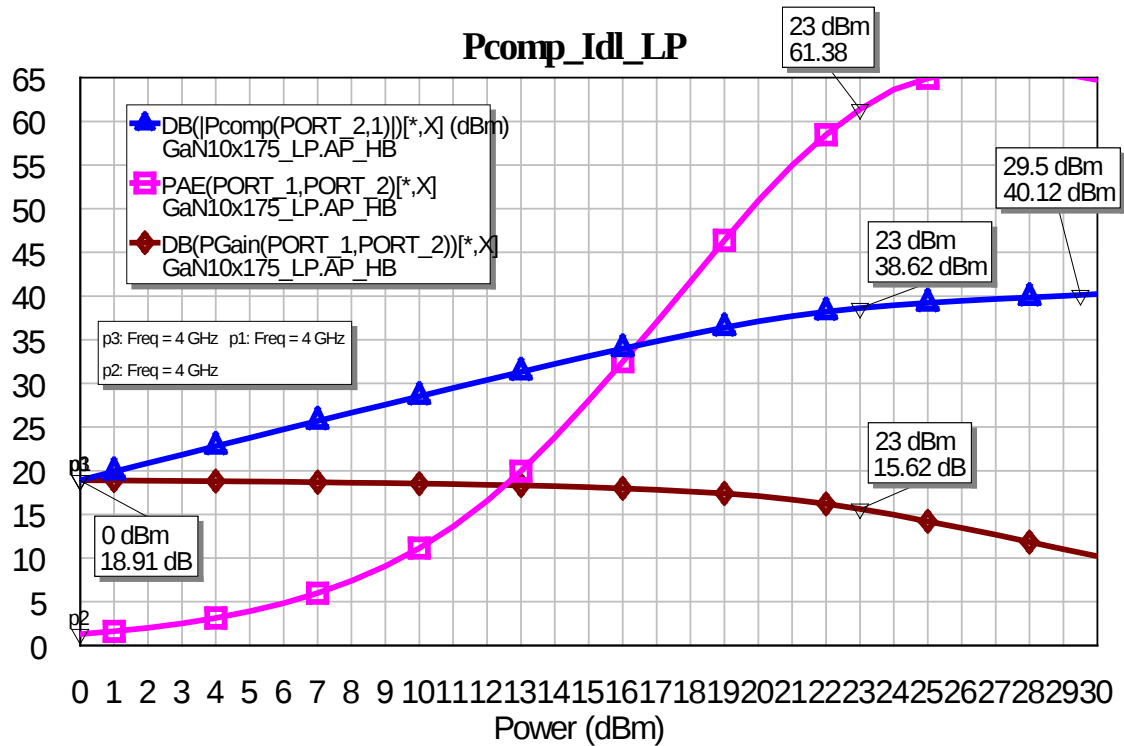


Fig. 47 1.75-mm HEMT ideal Gen2 (load pull) re-simulation 4 GHz, 28 V

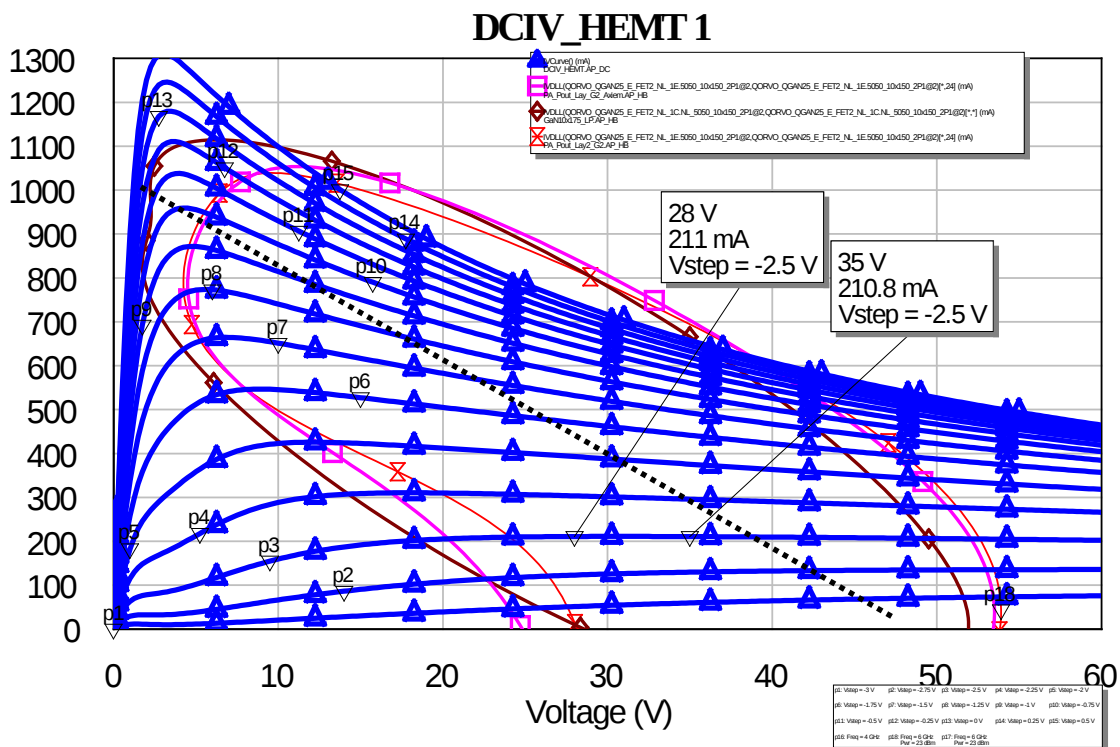


Fig. 48 1.75-mm HEMT Gen2 DC IV curves and dynamic load line 4 GHz, 28 V

9. Compact Broadband Feedback Amplifier

The first-stage driver amplifier of the 2-stage power amplifier was also submitted as a stand-alone probe-testable circuit (Fig. 49). This small circuit does not include the additional gain flattening matching elements on the output, nor the DC drain bias feed. Nominal gate DC bias can be applied to the probe pad shown in the upper left of the layout plot, while the drain DC supply can be fed through the G-S-G probe pads on the right through an external bias tee. Small signal s-parameters for the stand-alone amplifier are shown in Fig. 50 at 28-V, 44-mA bias. Note the noise figure of the feedback amplifier is as low as 2 dB below 3 GHz, so while not intended as a low-noise amplifier, this could be measured for comparison to the model. Large signal performance simulation from 2 to 18 GHz for the feedback amplifier is shown in Fig. 51. This is not the same as the conditions for the driver stage with interstage matching elements that were previously shown in Fig. 23. The input and output impedance are assumed to be 50 Ω for the stand-alone feedback amplifier, yet this does show that it can supply more than enough output power to drive the 1.75-mm output stage of the power amplifier. It is also a much wider band as a stand-alone amplifier than the 1.75-mm power amplifier. It is expected that the compact layout can be added to the tile for later test and analysis of this broadband driver amplifier.

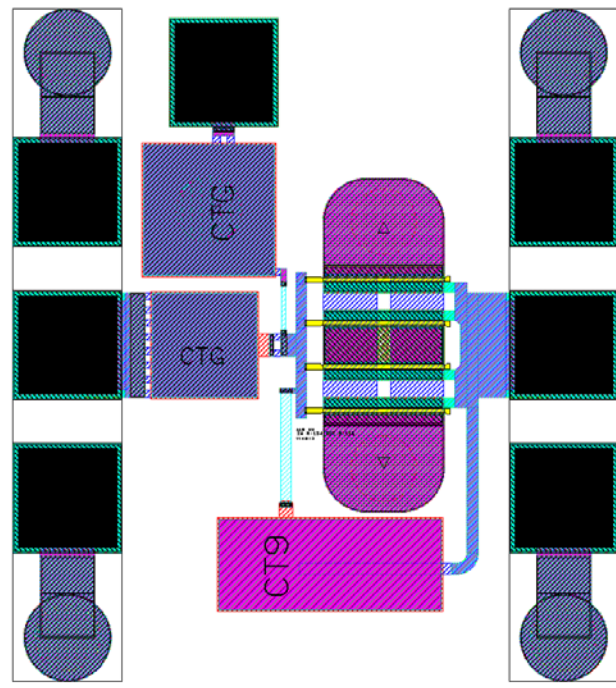


Fig. 49 Layout plot of stand-alone broadband feedback amplifier (0.6×0.6 mm)

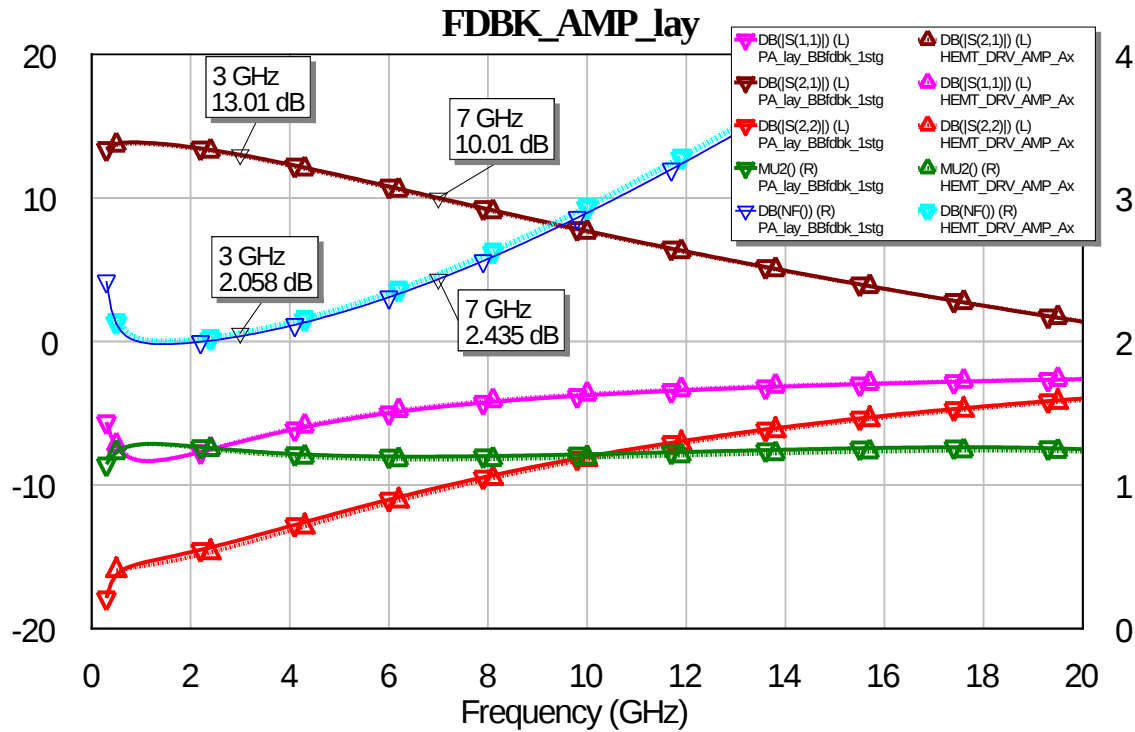


Fig. 50 MWO broadband feedback amplifier S-parameter simulation (0–20 GHz, 28 V)
0.44-mm HEMT

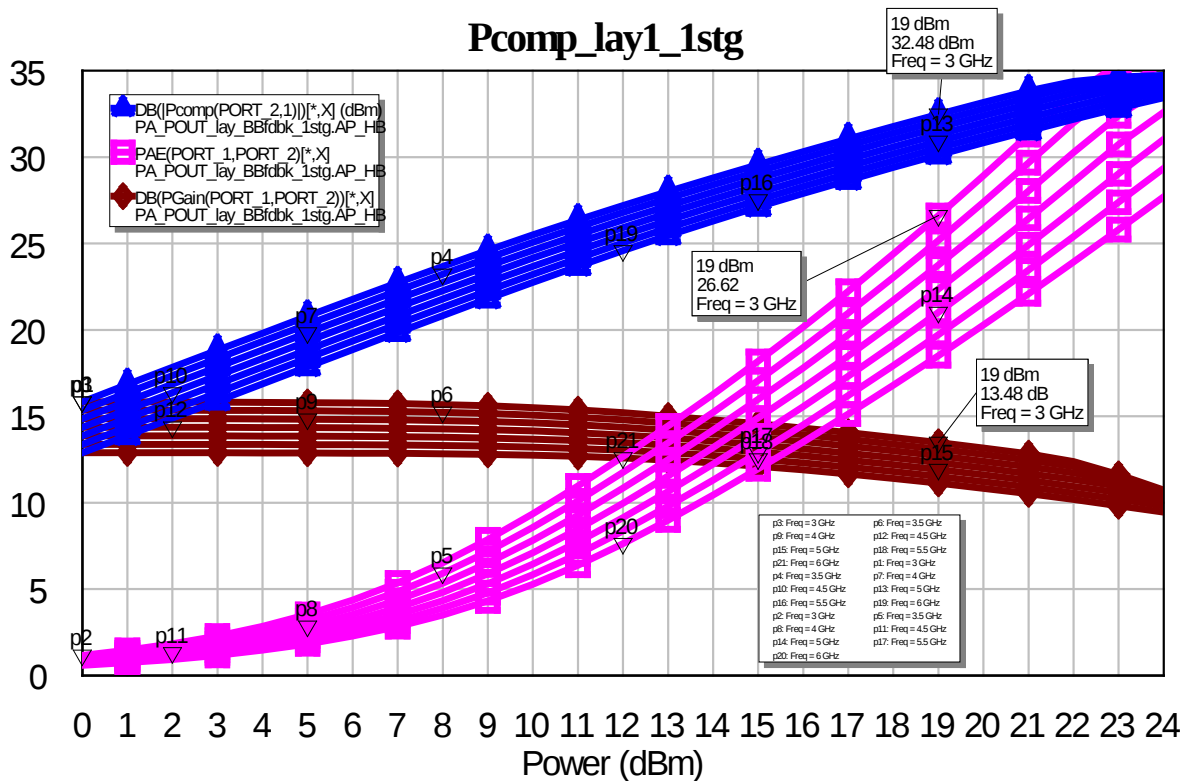


Fig. 51 MWO broadband feedback amplifier performance simulations (2–18 GHz, 28 V)
0.44-mm HEMT

10. Conclusion

A preliminary design of a broadband 8-W (28-V) 1.75-mm HEMT power amplifier was performed. The intent was to explore the bandwidth and performance of a class A/B-biased 1.75-mm HEMT power amplifier designed to maximize bandwidth, output power, and efficiency over the 3- to 7-GHz band. Trying to increase the bandwidth would certainly require more matching losses to extend the bandwidth. A similar 2-way combined 3.5-mm HEMT power amplifier should achieve comparable performance based on a preliminary design using ideal lossless matching elements. For the 1-stage 1.75-mm HEMT design, a preliminary layout was implemented, including EM simulations of the input and output matching circuit layouts. A simple ideal matching circuit design to combine two 1.75-mm HEMTs in parallel was shown. An alternative method to achieve more power is to parallel combine the matched amplifiers with passive couplers such as Wilkinson or Lange couplers. Using external couplers to increase output power can impact size and may increase losses over doing a combiner within the MMIC layout. Additional design work would be needed to complete a 2-way combined 3.5-mm single-stage amplifier with similar performance and bandwidth to the 1.75-mm single-stage amplifier shown.

To achieve a flatter broadband gain, and higher gain, a simple feedback amplifier was added to the power amplifier design to create a 2-stage design with over 20-dB gain in compression (3 to 4 dB) over the desired 3- to 6-GHz band. Hopefully the single-stage feedback amplifier can be squeezed into the tile for fabrication as an additional design to measure and verify. Improvements are expected with the change to Gen2 using the new GAN25_E process from Qorvo. The initial impact to the schedule and rush to get designs translated to the newer PDK should yield a better transition path moving forward and more reliable designs.

These designs are optimized for 28-V DC supplies, which, for a 7-W output on the 1.75-mm single-stage amplifier, corresponds to 4 W/mm, which seems like a reasonable number for this 0.25- μ m GAN process. Higher output power densities can be achieved at higher DC biases, such as 35 V, but this would require a redesign for optimal performance at the higher voltages and power densities. Thermal dissipation would be more challenging at the higher DC biases. All of these performance simulations assume that the HEMT junction temperatures are maintained at normal levels. Applications that require continuous wave operation of these designs would be more thermally challenging to cool than duty cycled or pulsed operation of the power amplifiers. This is typical of the higher power levels achievable, but also higher power densities, of GaN HEMTs.

List of Symbols, Abbreviations, and Acronyms

3-D	3-dimensional
ADS	Advanced Design System (CAD tool)
AFRL	Air Force Research Laboratory
ARL	US Army Research Laboratory
DC	direct current
DRC	design rule check
EM	electromagnetic
GaN	gallium nitride
HEMT	high-electron-mobility transistor
MMIC	monolithic microwave integrated circuit
MWO	Microwave Office (CAD tool)
PAE	power-added efficiency
PDK	process design kit
Pout	power output
RF	radio frequency

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