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University of California, Los Angeles

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14. ABSTRACT
The purpose of this advanced study is to provide an analytic framework for silicon on chip (SoC) technology that is based on numerical, simulation, and experimental analysis, with the aim to realize the radio frequency/analog devices in the Fin Field Effect Transistor (FinFET) platform and to provide the tunneling FinFET feasibility study for future ultra-low power digital applications.

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1. SUMMARY

While tunnel field effect transistors (TFETs) have been extensively examined by many research groups in the past few years, TFETs have not shown significant performance advantages. These devices limitations were carefully analyzed in this project. Based on the understanding of the limitations of previous TFETs, Ge-pocket TFET was proposed for lower power applications with I_{off}=10pA/μm and V_{DD}=0.5V. In this project, the optimized structure shows great potential in both L_g and V_{DD} scaling. The process flow for the proposed Ge-pocket TFET was designed. Vertical structure was adopted to demonstrate the concept of Ge-pocket TFET because of the need for sharp doping/composition gradient.

While fin field effect transistors (FinFETs) have shown great performance advantage over planar metal-oxide-semiconductor field-effect transistors (MOSFETs) for low power/high performance digital complementary metal-oxide-semiconductor (CMOS), their analog and radio frequency (RF) performance have major limitations and need to be enhanced by alternative engineering. FinFET analog performance optimization by graded channel (GC) design is examined. The analyses are carried out using the Sentaurus technology computer-aided design (TCAD) simulations. Doping profile in the source/drain (S/D) extension region is optimized to minimize extension parasitic resistance while avoiding increasing drain-induced barrier lowering (DIBL). SiGe/Si heterojunction leads to a more uniform electron distribution along the channel length direction compared with homojunction (Si) device, and thus improves g_{m_int} and *DIBL*. An improvement of 100% in g_{m_ext} has been achieved by the GC design at I_{DS}=1mA/μm compared with that in experimental 14nm-node FinFET. The redistributed electric field along the channel length direction can result in a 20% better *DIBL* and a 65% larger output resistance compared with experimental data. It has also been demonstrated that a further improvement in transconductance exists when switching channel material from silicon to InGaAs for the latest MOSFET generation.

2. INTRODUCTION

2.1 Group IV Tunnel Field Effect Transistors Optimization

TFET has been studied as an alternative for low power logic device in the past decade. So far, sub-thermal subthreshold swing (SS) and high I_{on} have been demonstrated experimentally on separate platforms. It is essential to combine these two desirable traits and develop a TFET with sub-thermal SS over 5 decades of I_{DS} and I_{on} comparable to International Technology Roadmap for Semiconductors (ITRS) Low Standby Power (LSTP) standards. In order to achieve this goal, the issues of previous TFETs have been pinpointed; Ge-pocket TFET, a very-large-scale integration (VLSI) -compatible solution, has been proposed.

2.2 Analog Performance Optimization for 14nm Node FinFETs

It has been widely accepted that transistor's external transconductance (g_{m_ext}) is affected by parasitic resistance and carrier transport. To the first order, the g_{m_ext} can be predicted by the following equations:

$$g_{m\_ext} = \frac{g_{m\_\mathrm{int}}}{1 + g_{m\_\mathrm{int}} \cdot R_{parasitics}} \tag{1}$$

where g_{m_int} is the intrinsic trans-conductance and $R_{parasitics}$ is the source parasitic resistance. Cut-off frequency (f_T), which is a crucial parameter for analog performance, is related to g_{m_ext} by the equation:

$$f_T = \frac{g_{m\_ext}}{2\pi \cdot C} \tag{2}$$

where C is the total gate capacitance. In 14nm node FinFET, C is dominated by interconnect capacitance, which can only be reduced in the back end process. Consequently, in the front end process, there are two possible ways to improve g_{m_ext} and thus f_T:, improving g_{m_int} and reducing R_S. We demonstrate that both of these goals can be achieved by the GC concept and discuss the possibility of using high mobility InGaAs as channel material to further improve analog performance.

3. METHODS, ASSUMPTIONS, AND PROCEDURES

3.1 Group IV Tunnel Field Effect Transistors Optimization

Limitations of Previous TFETs

To identify the key physics bottlenecks of previously TFETs, the experimental results of three state-of-the-art TFETs were studied (Figure 1).

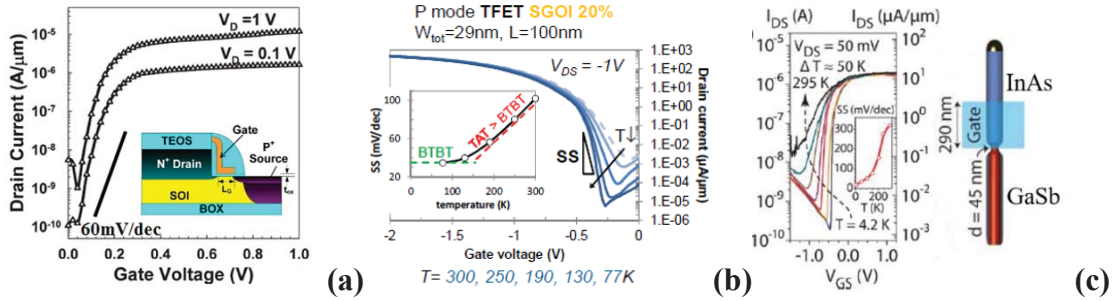


Figure 1: Experimental Results of State-of-the-Art TFETs

(a) SOI (t_{ox}=2nm, L_g=70nm, and t_{soi}=70nm) [1]; (b) tri-gate with SiGe source (equivalent oxide thickness (EOT) =1.25nm, and L_g=100nm) [2]; and (c) nanowire with InAs/GaSb broken-gap (EOT=1.3nm, and d=45nm) [3]

N-TFET with Sub-60mV/dec SS at room temperature was first realized on silicon on insulator (SOI) platform (Figure 1(a)). The device exhibits SS as low as 53mV/dec and I_{on} of 12.1μA/μm with V_{DD}=1V. The small I_{on} is due to the large tunneling resistance at source/channel junction as well as the small tunneling area.

Tri-gate p-TFET with SiGe source has demonstrated I_{on} of 190μA/μm under V_{DD}=-0.9V, which is one order of magnitude higher than the SOI n-TFET thanks to the small bandgap of SiGe and better electrostatic control. However, the average SS is approximately 80mV/dec and the degradation is likely due to the trap-assisted tunneling (TAT) at source/channel junction (Figure 2).

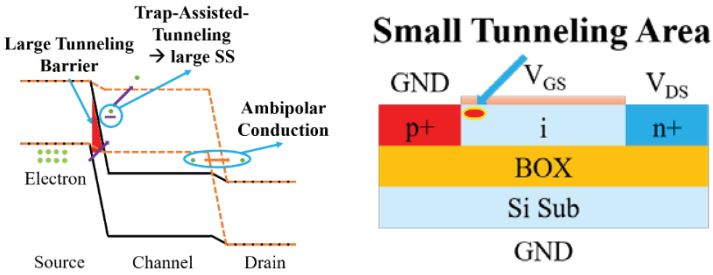


Figure 2: Key Limitations of Previous TFETs

Nanowire n-TFET with InAs/GaSb broken-gap exhibits I_{on}=62 μA/μm with V_{DS}=0.3V and V_{GT}=0.5V thanks to the small tunneling barrier. SS is significantly degraded compared with group IV-based TFET due to material defect from immature material synthesis and fabrication process. Ambipolar conduction is also observed.

Previous TFETs suffer from four major limitations as shown in Figure 2.

Tunneling Model Calibration

Dynamical nonlocal band-to-band tunneling model was adopted for simulation, which calculates the tunneling path dynamically by following the gradient of valence band profile. The tunneling rate is computed by using Kane's model. The model provides a deep physical insight into TFETs operation, and gives good fits to both I_{on} and SS with two fitting parameters, A and B.

A Si/SiGe resonant interband tunneling diode (RITD) [4] was used for calibration (Figure 3).

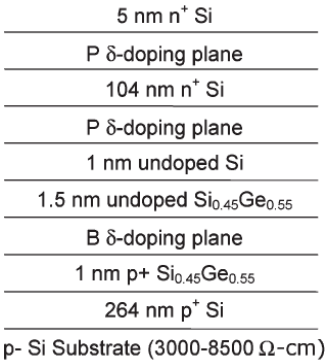


Figure 3: Schematic of Calibrated SiGe/Si RITD

Quantization effect has been incorporated into the simulation by using Poisson Schrodinger solver. The quantization modifies the electrostatic potential profile and gives rise to subband. The formation of subband will modify the tunneling path (Figure 4(a)). The calibrated simulation shows a good agreement with experiment data (Figure 4 (b)).

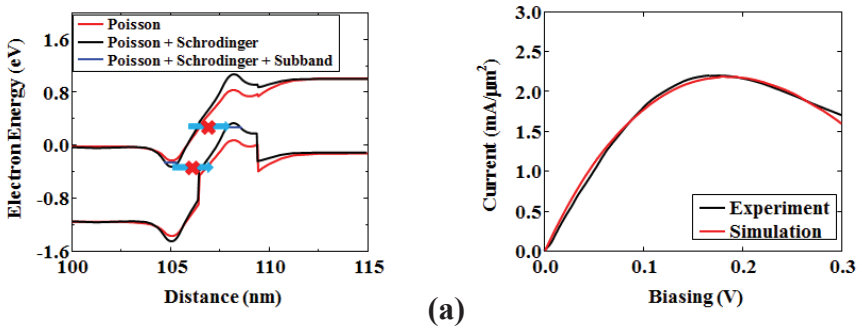
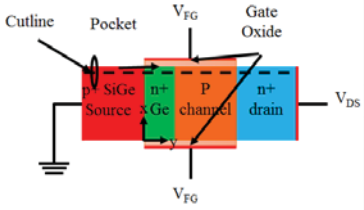


Figure 4: (a) Simulated Band Diagram of SiGe/Si RITD and (b) Calibrated Simulation Compared to Experiment

Proposed Structure

Based on the previous limitations on SiGe-based TFET, Ge-pocket TFET is proposed (Figure 5). Strained-Ge pocket is only adopted at the tunneling junction to enhance the tunneling probability. SiGe is chosen over Ge for source material because of the reduction in the strain, which allows a thicker defect-free SiGe layer. This is essential for steep switching behavior. Ge-pocket TFET is designed for lower power application with I_{off}=10pA/μm and V_{DD}=0.5V.



L_{gate}	20nm
L_{sd}	20nm
T_{ox}	0.8nm
L_{pocket}	4nm
T_{body}	10nm
$N_{S/D}$	1e20cm^{-3}
N_{Pocket}	3e19cm^{-3}
$N_{Channel}$	1e16cm^{-3}

Figure 5: Schematics of Proposed Ge-pocket TFET with Design Parameters

Scalability

In order to study the scalability of the proposed structure, the concept of natural length was adopted. The natural length is given by:

$$\lambda = \sqrt{\frac{1}{2}\frac{\varepsilon_{Si}}{\varepsilon_{ox}} t_{si} t_{ox}}$$

Device with different combinations of t_{si} and t_{ox} were simulated. The I_{on}/I_{off} is plotted against the ratio of L_g/λ (Figure 6). I_{on}/I_{off} increases as the ratio increases, and saturates when the ratio exceeds 8. A minimum ratio of 7 is needed to provide the necessary I_{on}/I_{off} for the proposed structure to be competitive against state-of-the-art FinFET technology. Based on the assumption that L_g/λ=7, the projected device parameters are given in Table 1.

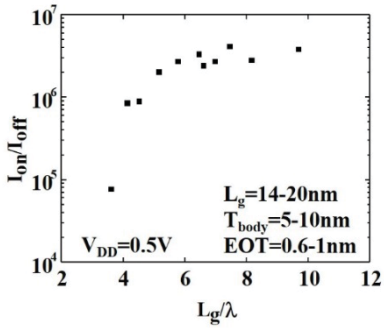


Figure 6: I_{on}/I_{off} Ratio as a Function of L_g/λ

Table 1. Projected Device Parameters Based on $\lambda=L_g/7$

L_g (nm)	20	16	14
EOT (nm)	0.8	0.7	0.6
T_{body} (nm)	8	5	5

Doping Optimization

Tunneling is sensitive to band profile and thus it is essential to investigate the impact of doping concentration on the proposed TFET's performance. Doping concentrations at all four regions, source, pocket, channel, and drain, have been optimized to improve I_{on}.

The impact of increasing Ge-pocket TFET's source doping is twofold. On the one hand, the tunneling probability is enhanced at source/pocket due to a higher electric field across it. On the other hand, the quasi-Fermi level of hole in the source region moves further away from the valence band edge, where electric field peaks. The optimum source doping concentration is determined to be $2x10^{20}cm^{-3}$ (Figure 7).

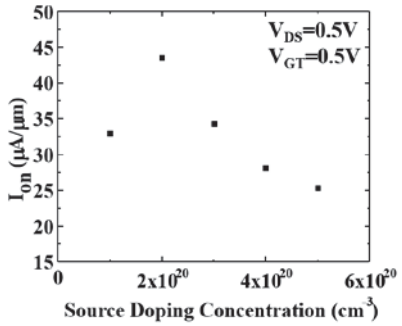


Figure 7: I_{on} for Ge-pocket TFET as a Function of Source Doping
$V_{GT}=V_{GS}-V_{TH}$ and $I_{DS}=10pA/\mu m$ under $V_{DS}=0.5V$ and $V_{GS}=V_{TH}$ for each device

The insertion of counter-doped pocket significantly increases the electric field across the tunneling junction, thus leading to an improvement in I_{on} [5]. However, a tunneling window will open even at off-state when increasing pocket doping beyond $4x10^{19}cm^{-3}$. This leads to a significant increase in leakage current (Figure 8(a)). Taking both effects into consideration, the optimum pocket doping concentration is $4x10^{19}cm^{-3}$ (Figure 8(b)).

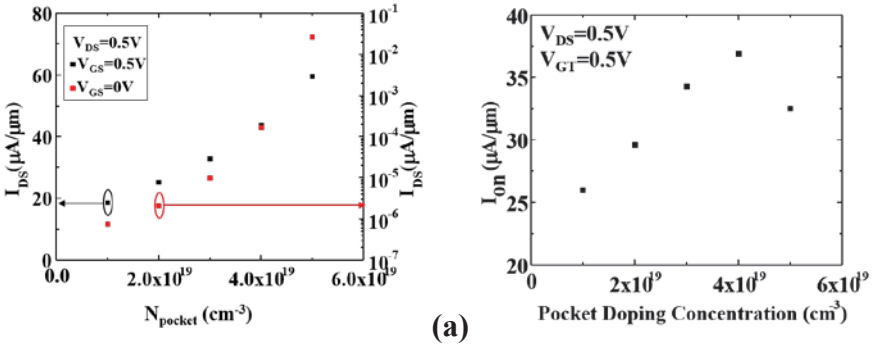


Figure 8: (a) I_{DS} for Ge-pocket TFET with Various Pocket Doping Concentrations under V_{GS}=0V and V_{GS}=0.5V and (b) I_{on} as a Function of Pocket Doping Concentration

Due to the thin body nature of double-gate structure and light channel doping, the channel of Ge-pocket TFET is virtually undoped. The impact of channel doping is negligible (Figure 9).

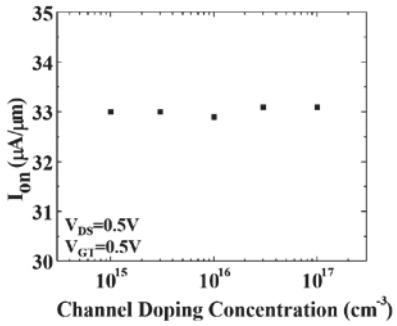


Figure 9: I_{on} of Ge-pocket with Different Channel Doping Concentrations

At off-state, increasing drain doping concentration leads a higher electric field penetrating into the channel region, and it lowers the conduction in the channel, which gives rise to a higher off-state current under a fixed bias (Figure 10(a)). It is desirable to have a lightly doped drain as long as the drain doping concentration is slightly higher than the electron density in the channel. After adjusting gate voltage to match I_{off}, a drain doping concertation of $10^{19}cm^{-3}$ yields the highest I_{on} (Figure 10 (b)).

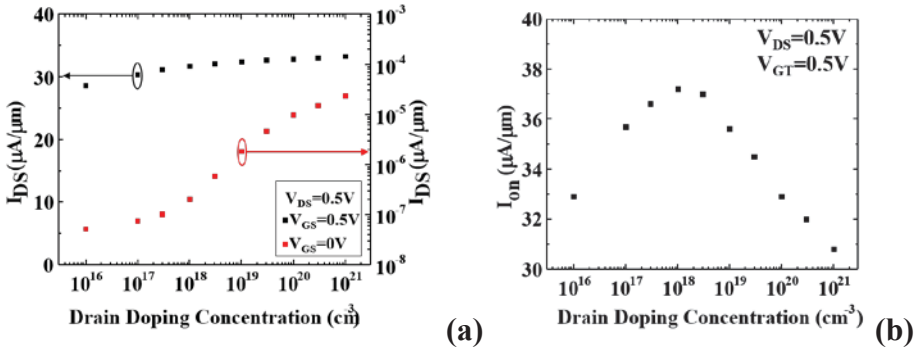


Figure 10: (a) I_{DS} for Ge-pocket TFET with Various Pocket Doping Concentrations under V_{GS}=0V and V_{GS}=0.5V and (b) I_{on} as a Function of Pocket Doping Concentration Optimum Drain Doping Concentration

Benchmark

The proposed structure with the optimized doping profile was benchmarked against state-of-the-art 14nm FinFET. It provides roughly 100% improvement in I_{on} at 14nm node (L_g=20nm) compared with Intel 14nm FinFET, and shows great potential in both L_g and V_{DD} scaling (Figure 11).

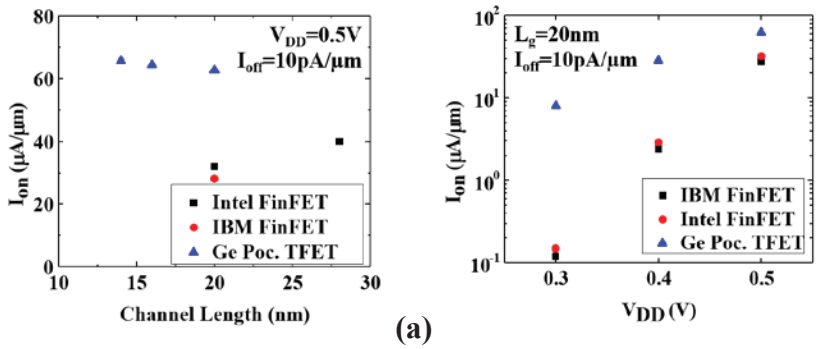


Figure 11: Benchmark of Optimized Ge-pocket TFET against State-of-the-Art FinFETs in Terms of I_{on}

The optimized structure in (a) gate length and (b) supply voltage scaling.

Composition and Doping Gradient

The success of Ge-pocket TFET relies on sharp material composition transition as well as doping profiles. The impact of material composition sharpness and doping gradient on the optimized device has been studied. Both increasing the Ge pocket thickness (t_{pocket}) and reducing the material composition gradient (CG) will result in a reduction in tunneling barrier; consequently, both on-state and off-state current will increase. Figure 12 plots I_{on} for the devices with different pocket length and composition gradient with adjusted V_{GS} to fix I_{off} to 10pA/μm. As the transition of material composition becomes sharper, ~80% I_{on} can be recovered compared to Ge-pocket TFET with abrupt material composition.

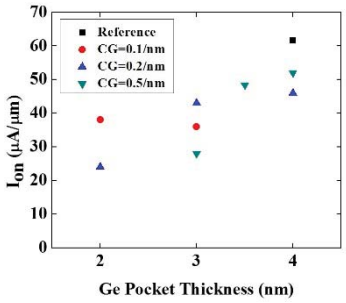


Figure 12: I_{on} for Ge-pocket TFETs with Different t_{pocket} and CG

The impact of doping gradient on TFET performance has been previously examined [6]. By using the doing compensation technique [7], the on-state current can be recovered (Figure 13). Simulations shows that doping gradients of 6nm/dec and 5nm/dec are needed for source and pocket respectively to maintain >70% I_{on} of the device with box-shape doping profile.

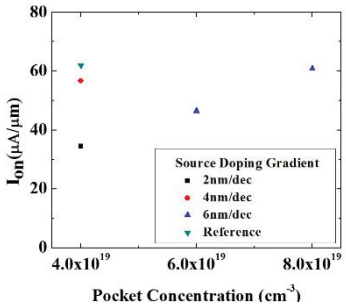
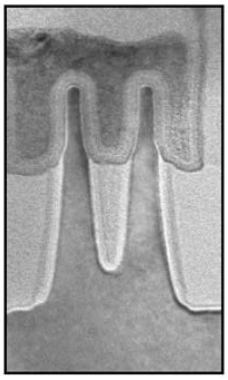


Figure 13: I_{on} for Ge-pocket TFET with Different Source Doping Gradient and Pocket Doping Concentration with Pocket Doping Gradient of 5nm/dec

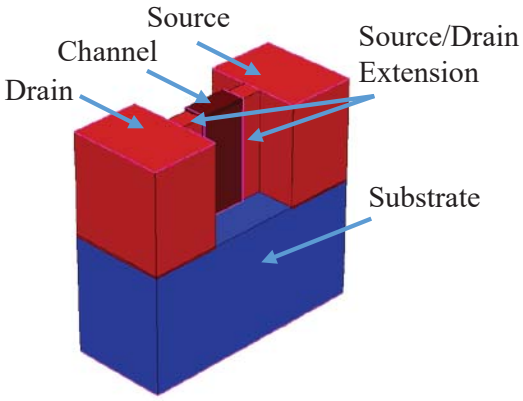
3.2 Analog Performance Optimization for 14nm Node FinFETs

Simulation models and calibrations

Analysis in this project is carried out using the Sentaurus TCAD tools [9]. The design parameters of the simulated FinFET are based on the 14nm node FinFET published by Intel [8]. The device structure is demonstrated in Figure 14.



Device parameters	
Channel length (nm)	20
Fin height (nm)	42
Fin width (nm)	8
Fin pitch (nm)	42
Gate oxide thickness (nm)	0.9



(a) **(b)**

Figure 14: (a) Experimental FinFET Published by Intel [1] and (b) the Simulated Structure

Design parameters are listed in Table 2. A Drift-Diffusion model with modified saturation velocity is used in the simulation to capture the physics of velocity overshoot. Density gradient model and thin layer mobility model are used to simulate carrier quantum confinement as well as mobility degradation in the 8nm wide Fin. $R_{parasitics}$ has also been calibrated by fitting simulated and experimental g_{m_ext}. The total $R_{parasitics}$ is estimated to be 3kΩ/fin. The calibrated I-V curves are shown in Figure 15. The difference between simulated current and experimental data is less than 5%, suggesting that the modified transport parameters and saturation velocity is sufficient to study FinFET alternating current (AC) performance.

Table 2. Design Parameters of 14nm-node FinFET

Design Parameters	Value	Design Parameters	Value
Channel length	20nm	Gate dielectric EOT	0.7nm
Fin height	42nm	S/D extension length	10nm
Fin width	8nm	Fin pitch	42nm
S/D doping concentration	$10^{20}cm^{-3}$	Channel doping concentration	$10^{16}cm^{-3}$

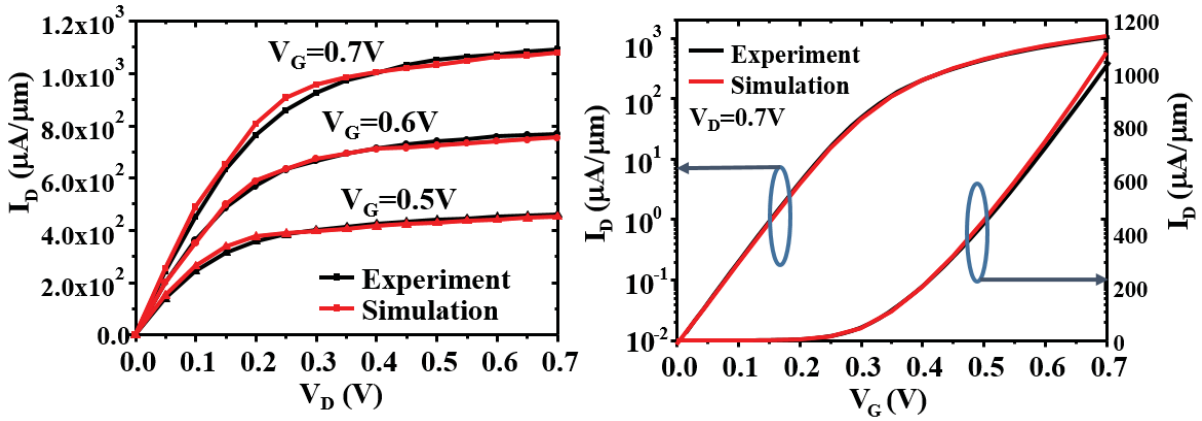


Figure 15: Experimental Data vs. Simulated I-V Curves with Calibrated Mobility Model

Physics of analog performance optimization by GC concept

The GC concept can be demonstrated with a double gate structure shown in Figure 16. An nFET is used as an example. In the proposed structure, GC concept is realized by SiGe/Si heterojunction ($\Delta\chi$=0.16eV along the channel). SiGe with smaller electron affinity (4.05eV) is close to source side and tensile strained silicon with larger electron affinity (4.22eV) is close to drain side. The electron affinity grading can be tuned to achieve uniform electron distribution along channel length direction.

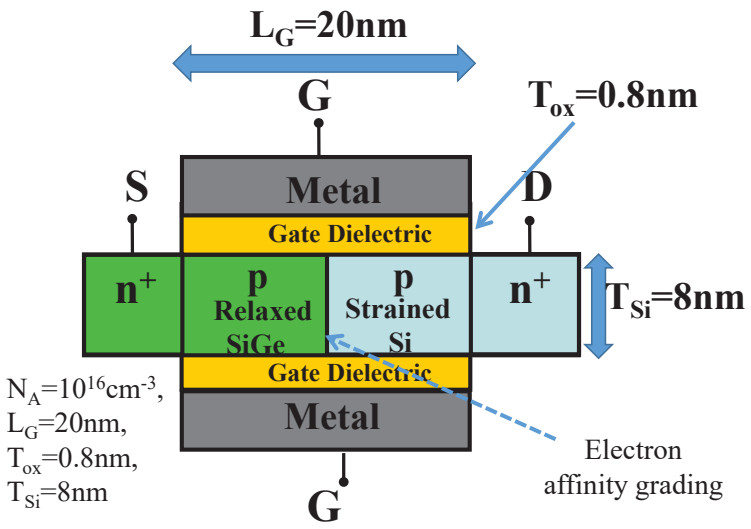


Figure 16: Double Gated FET with Graded Channel

In the proposed design, source and drain extension regions are heavily doped to reduce spacer parasitic resistance. The experimental FinFET $R_{parasitics}$ is extracted to be 3kΩ/Fin. Simulations show that this FinFET $R_{parasitics}$ is dominated by the S/D extension region resistance (~2kΩ/Fin), which is caused by insufficient doping concentration. It will be demonstrated later that the S/D extension resistance can be reduced from ~2000Ω/Fin to 365Ω/Fin, and thus improve g_{m_ext}.

The SiGe/Si heterojunction design can result in more uniform electron density and electron velocity distributions compared to a homojunction device. This uniform electron distribution causes the lateral electric field to redistribute, increasing the electric field at source side and decreasing the electric field at drain side. Higher electric field at the source side results in higher injection velocity, and thus improve g_{m_ext}. Lower electric field at the drain side will reduce the channel length modulation (CLM) and results in better output resistance [10-12].

4. RESULTS AND DISCUSSIONS

4.1 Group IV Tunnel Field Effect Transistors Optimization

Experiment Design

The success of fabricating the proposed structure depends on the quality of SiGe heterojunction. It is logical to use the resonant interband tunneling diode as a test structure to fine tune the growth condition. The process flow is listed in Table 3

Table 3. Process Flow for SiGe RITD

SiGe Resonant Interband Tunneling Diode Process Flow	
1	Thermal oxide growth
2	Patterning for selective area growth
3	Oxide etch
4	Photoresist strip
5	Pre-growth clean
6	SiGe growth
7	Contact hole pattering
8	Oxide etch
9	Photoresist strip
10	Ni deposition
11	Silicidation
12	Excess Ni removal
13	Al deposition
14	Patterning for contact pad
15	Al contact pad etch
16	Photoresist strip

4.2 Analog Performance Optimization for 14nm Node FinFETs

Analog performance optimization by GC design

A quantitative analysis was performed to study g_{m_ext} improvement by GC concept. An nFinFET was used as an example. Optimization of both doping concentration profile in the source/drain extension region and Ge mole fraction profile along the channel direction are required to maximize g_{m_ext}. Both of these profiles are assumed to be uniform along the Fin width and Fin height direction to reduce complexity. For Ge mole fraction profile optimization, the objective is to achieve a uniform electron density along the channel length direction, and thus improve g_{m_ext} and DIBL. For doping profile optimization, the goal is to minimize the extension region resistance while avoiding dopant encroachment into the channel, which can lead to enlarged DIBL.

The optimized device design is demonstrated in Figure 17. Design parameters are listed in Table 4. S/D extension doping profile is assumed to be formed by damage-free dopant implantation followed by laser annealing, resulting in a doping density gradient of 3nm/decade at the extension/channel junction and no mobility degradation [13-15]. Simulation shows that the S/D extension region resistance can be reduced from 2000Ω/Fin [8] to 365 Ω/Fin.

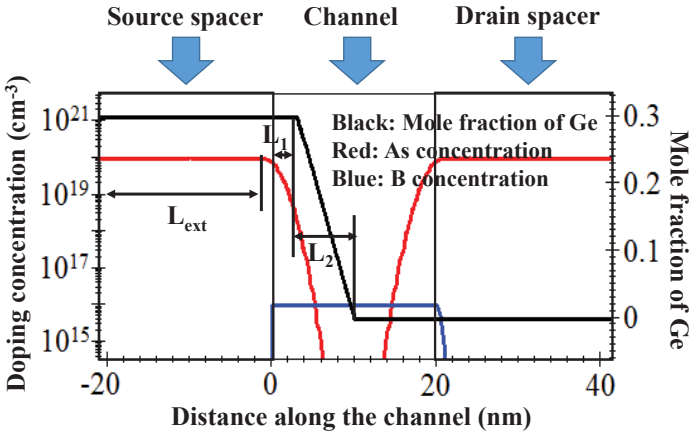
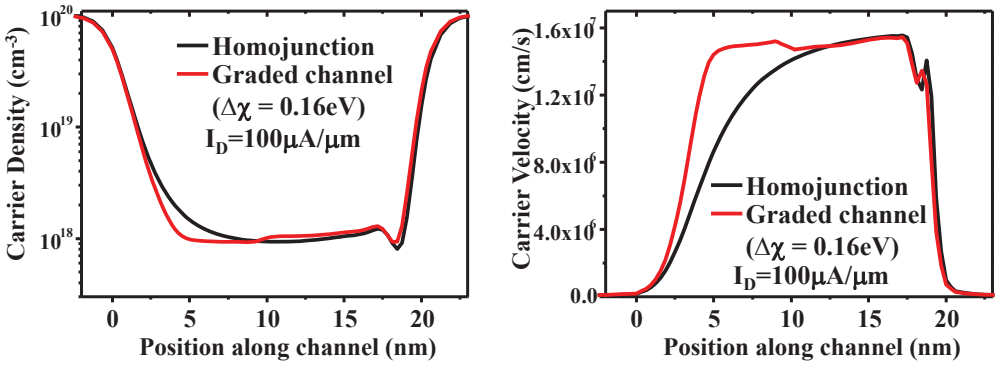


Figure 17: Optimized Doping and Ge Mole Fraction Profile along Channel Length Direction

Table 4. Design Parameters of the Purposed GC FinFET

Design Parameters	Value
L_1	3nm
L_2	7nm
L_{ext}	9nm
Contact resistivity	$2x10^{-9}$ Ω/cm^2
Dopant gradient	3nm/decade

As shown in Figure 18, the optimized SiGe/Si heterojunction leads to a more uniform electron distribution along the channel length direction compared to homojunction (Si) device. The simulated g_{m_ext} of the purposed GC FinFET is shown in Figure 19. An improvement of 100% in g_{m_ext} has been achieved by the GC design at I_{DS}=1mA/μm compared with that in experimental 14nm-node FinFET.



(a) (b)

Figure 18: (a) Electron Density Profile and (b) Velocity Profile in Channel Length Direction at 1nm from Channel Surface

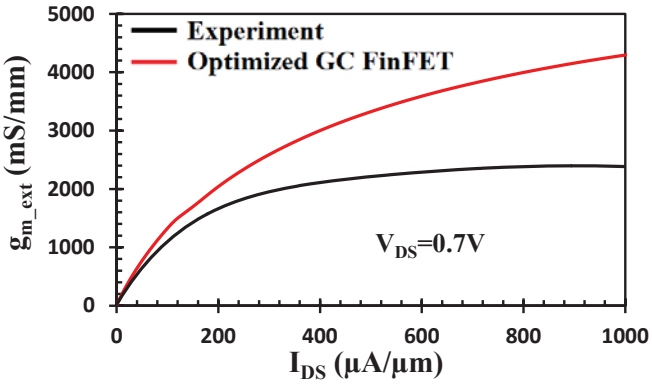


Figure 19: Simulated g_{m_ext} of Optimized GC FinFET vs. 14nm-node FinFET Experimental Data published by Intel

Apart from g_{m_ext} optimization, GC concept can also improve DIBL by screening the electric field from the drain side as shown in Figure 20. TCAD simulations show that DIBL is reduced from 60mV/V to 47.6mV/V. The reduced DIBL results in a 65% larger output resistance than homojunction device as shown in Figure 21.

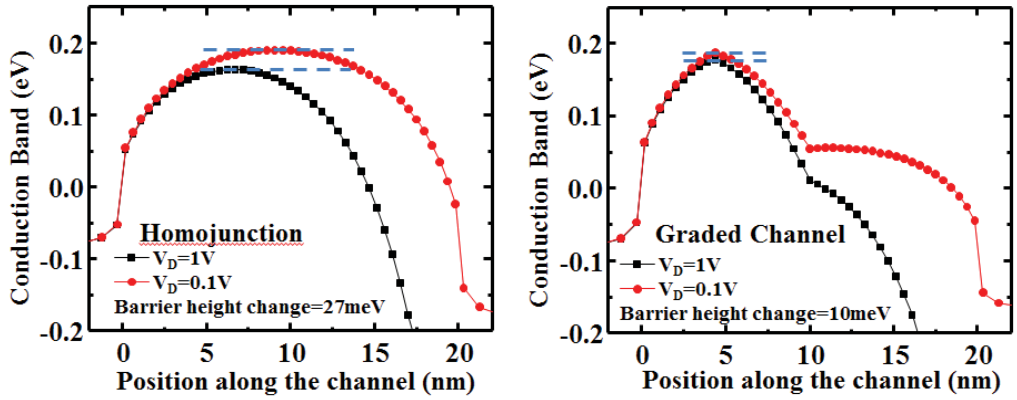


Figure 20: Conduction Band Profiles along the Channel at 1nm from Gate Dielectric for Graded Channel Device and Homojunction Device

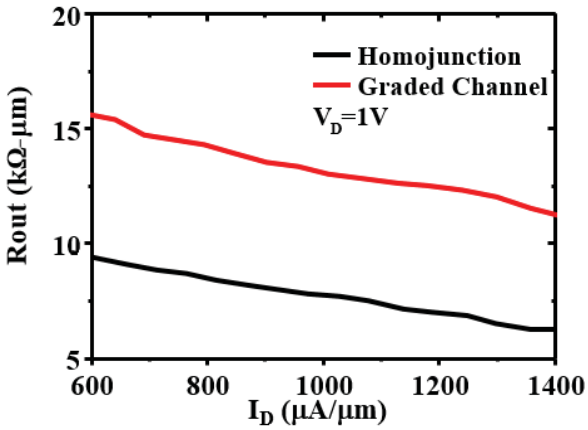


Figure 21: Output Resistance of Graded Channel and Homojunction Devices

Analog performance enhancement by using InGaAs MOSFET

Using high mobility channel material is another potential way to improve the analog/RF performance of MOSFET. Among all the materials, InGaAs has received extra attention due to its high electron mobility and versatile properties when changing composition. In order to study the analog performance of InGaAs MOSFET, we calibrated the simulation platform for InGaAs MOSFET for both short channel and long channel devices (Figure 22). Density Gradient model is used for quantum effect, Lombardi mobility model is used to account for surface mobility degradation, and Drift-Diffusion model with adjusted saturation velocity is used to simulate high field carrier transport.

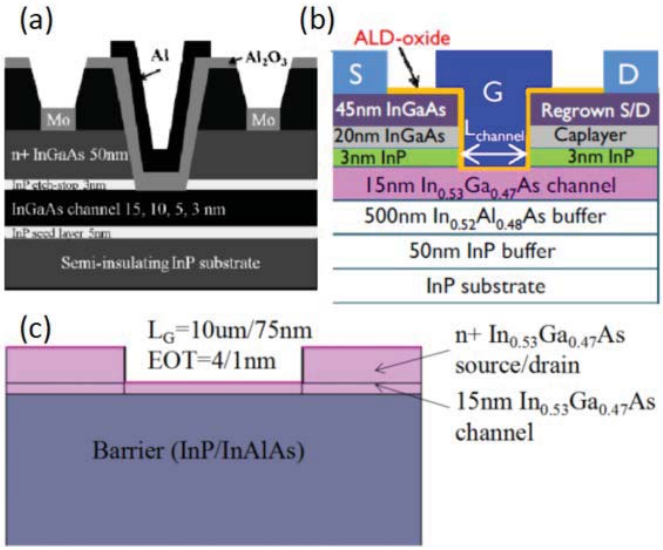


Figure 22: (a) Long Channel MOSFET [9], (b) Short Channel MOSFET [10], and (c) Simulated Structure

The gate capacitance (Figure 23) and peak transconductance (Figure 24) are compared to silicon SOI counterpart with same body thickness. It has been shown that in spite of a gate capacitance degradation introduced by the low density of state compared to silicon, there is still an

improvement of 80% in transconductance when switching channel material from silicon to InGaAs even for with EOT of 0.5nm.

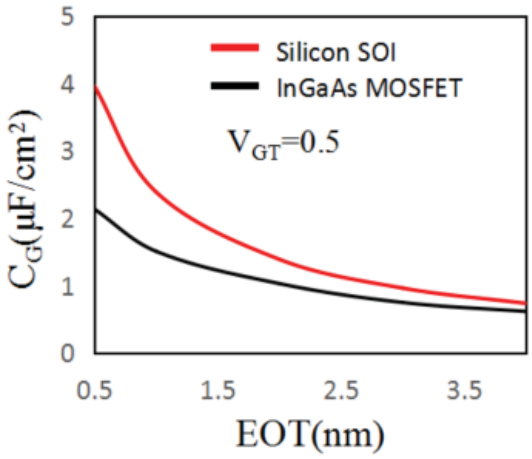


Figure 23: C_G vs EOT for Silicon SOI and InGaAs MOSFET

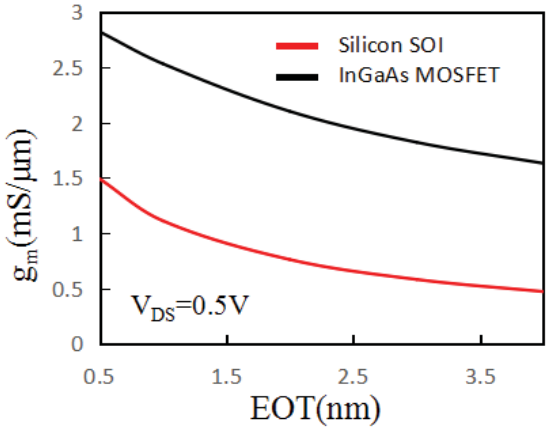


Figure 24: g_m vs EOT for Silicon SOI and InGaAs MOSFET

5. CONCLUSION

Based on the limitations of previous TFETs, Ge-pocket TFET was proposed for lower power applications with I_{off}=10pA/μm and V_{DD}=0.5V. The doping was optimized, and the optimized structure shows great potential in both L_g and V_{DD} scaling. The process flow for the proposed Ge-pocket TFET was designed. Vertical structure was adopted to demonstrate the concept of Ge-pocket TFET because of the need for sharp doping/composition gradient. The impact of growth area on SiGe quality was also investigated by studying SiGe RITD with various dimensions. Ge-pocket TFET was fabricated with optimized SiGe growth condition.

FinFET analog performance optimization by GC design as examined. The analyses were carried out using the Sentaurus TCAD simulations. Doping profile in the S/D extension region was optimized to minimize extension parasitic resistance while avoiding increasing DIBL. SiGe/Si heterojunction led to a more uniform electron distribution along the channel length direction compared to homojunction (Si) device, and thus improved g_{m_int} and DIBL. An improvement of 100% in g_{m_ext} was achieved by the GC design at I_{DS}=1mA/μm compared with that in experimental 14nm-node FinFET. The redistributed electric field along the channel length direction can result in a 20% better DIBL and a 65% larger output resistance compared with experimental data. It was also demonstrated that a further improvement in transconductance exists when switching channel material from silicon to InGaAs for the latest MOSFET generation.

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LIST OF ACRONYMS, ABBREVIATIONS, AND SYMBOLS

ACRONYM	DESCRIPTION
AC	Alternating Current
CG	Composition Gradient
CLM	Channel Length Modulation
CMOS	Complementary Metal-Oxide-Semiconductor
DIBL	Drain-Induced Barrier Lowering
EOT	Equivalent Oxide Thickness
FinFET	Fin Field Effect Transistor
GC	Graded Channel
ITRS	International Technology Roadmap for Semiconductor
LSTP	Low Standby Power
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
RF	Radio Frequency
RITD	Resonant Interband Tunneling Diode
S/D	Source/Drain
SOI	Silicon on Insulator
SS	Subthreshold Swing
TAT	Trap-Assisted Tunneling
TCAD	Technology Computer-Aided Design
TFET	Tunnel Field Effect Transistor
VLSI	Very-Large-Scale Integration