

Design of a CCD Camera for Space Surveillance

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Abstract— This paper describes the CCD camera electronics design for observing satellites in the geo belt. The paper discusses the design overview, tactics for tuning operation of a CCD, and test and integration. The main circuit topology is discussed for operating a CCD. Thermal and structural analysis is described. Results from prototype testing are presented. The prototype design and test are completed and assembly of the engineering unit is underway.

for long integration times which results in good sensitivity and revisit rates.

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1. INTRODUCTION

MIT Lincoln Laboratory is building an operational demonstration of the SensorSat satellite to scan the geosynchronous-orbit belt from low Earth orbit. This mission is technology pathfinder follow-on for the Space Based Space Surveillance satellite currently in operation. The camera is the primary sensor on the satellite which is based on the Lincoln Laboratory fabricated CCID-51M, a 2048x1024 pixel Charge Couple Device (CCD) imager. [1]

The mission objective is to observe and detect satellites in the geo belt from an equatorial orbit. This is done with a novel approach via microsatellite of only 120 Kg. The satellite will scan the belt continuously using the Time Delay Integration (TDI) capabilities of a CCD. TDI allows

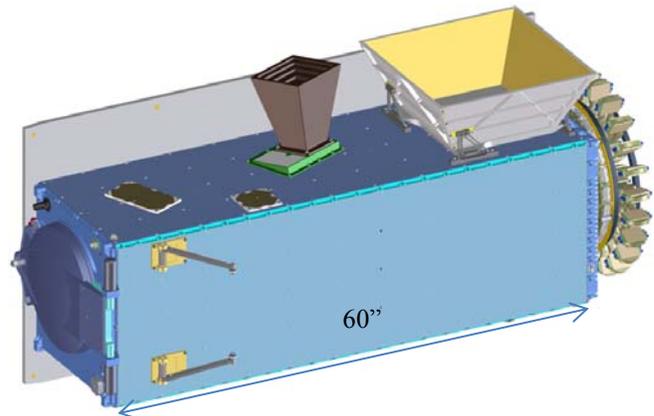


Figure 1 SensorSat Space Vehicle

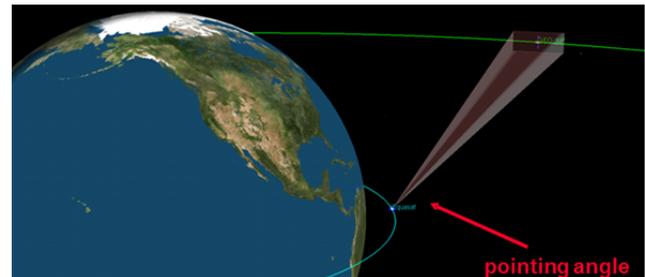


Figure 2 Space Vehicle Orbit

The camera electronics incorporates all the circuitry necessary to operate the CCD. A CCD requires numerous clocks and bias levels to properly function. The analog processing circuitry architecture is two channels of Correlated Double Sampling (CDS) which offers low noise. The CCD output signal is sampled with a 400 kHz analog to digital converter. The camera is controlled with a ProAsic3 FPGA which generates all the timing for reading out the CCD and ingesting the digitized image data. The image data is formatted and transmitted via LVDS (Low Voltage

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Differential Signal) drivers to the satellite's processor. The FPGA also provides the control to the satellite with an LVDS Universal Asynchronous Receive and Transmit (UART) interface.

The bias and clock levels are adjustable with digital to analog converters. This allows flexibility to adjust the levels far into the integration and test cycle as well as on orbit to maximize performance of the sensor.

The camera power input is 3.3 V, +15 V, and -15 V provided by the processor chassis. The CCD requires voltages that exceed +15 V and a charge pump boots the +15 V to +24 V for this. The input power is well filtered to exclude noise from the processor and outside environments from adversely affecting the low noise floor of the sensor

A prototype of the camera electronics is built and undergoing test. The performance of the camera prototype currently meets all requirements of the sensor and satellite. An engineering development unit (EDU) is planned for this summer with the flight unit assembled early 2016.

2. CCD PRIMER

A CCD is a silicon device which collects photoelectrons when exposed to visible light. The photoelectrons are collected in potential wells created by the clock voltages. Once the exposure is complete, the clocks are phased to transfer the charge to the outputs. An electronic shutter is created by having an equal area of pixels covered by an opaque metal mask. The charge in the image area is quickly transferred under the mask, and then the image can be read out slower while the next exposure collects in the image area.

The key element of the design is the CCID51M. The CCD is fabricated a Lincoln Laboratory which is known for low noise CCD's for space and other scientific applications. The CCID51M is a 2048x1024 full frame transfer back illuminated CCD. Back illuminated CCD's have very high quantum efficiencies, >85% across the visible solar spectrum. The output is a single source follower on the CCD which is buffered with a U309 JFET just off the chip. The U309 provides enough drive for a short flex print or cable to the electronics.

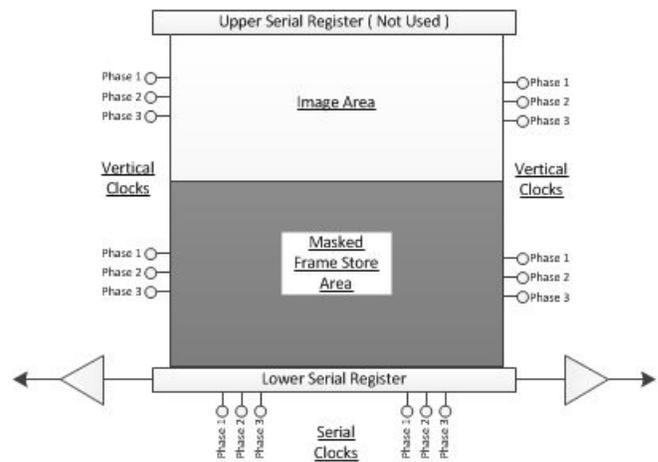


Figure 3 CCID51M Diagram [2]

Time Domain Integration is a technique to clock the image clocks in coordination with the movement of a subject. In this instance it is the stars which are moving in the image and the image clocks are clocked to match the movement. This keeps the stars in the same spot while the satellite moving and using TDI results in significantly longer integration times with increased sensitivity. The nominal operation is 128 steps with a step time of 59 ms. The effective integration time is 7.5 seconds.

4. CORRELATED DOUBLE SAMPLING CIRCUIT (CDS)

The focus of the design is the correlated double sampling circuit. A correlated double sample reduces the correlated noise of the output sampling node of the CCD. The analog signal from the CCD is clamped once across a capacitor during the reset phase of the CCD and then sampled when the CCD video signal is active. The reset voltage across the capacitor is subtracted from the CCD signal, removing the correlated noise. The CDS is also provides bandwidth filtering to reduce random noise.

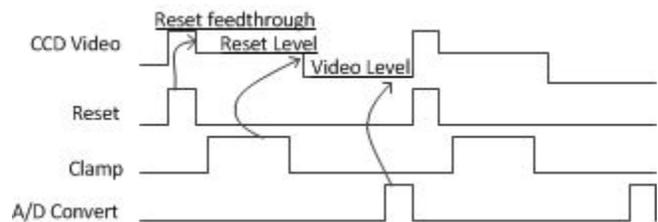


Figure 4 CDS Timing Diagram

By design the CCD readout rate is 400 KHz. This rate was chosen so reading the 2E6 pixels from one output is less than 7.5 seconds. With two outputs only 2.5 seconds is needed to read out the image. In TDI mode the readout needs to be synchronized with the TDI clock edges. The image clock transitions cause large voltage spikes in the CCD video signal. To avoid this discrete lines are read out

in between the transitions. This adds overhead to the readout, particularly when using one output.

Figure 5 shows a block diagram of the CDS circuitry including the output of the CCD. The first opamp stage of the camera electronics provides the load for the U309 and AC couples the CCD output to remove the ~12V DC bias. The first stage is non-inverting to provide high input impedance and a gain of 2.7 V/V. The second stage is an inverting opamp to invert the signal so the CCD signal is positive for the A/D. This stage also drives the CDS capacitor. The CDS capacitor is clamped with a high speed switch to a voltage reference. When the CCD is in the reset phase the switch clamps the capacitor to the reference voltage to provide the Analog to Digital Converter (A/D) a reference above ground. When the actual pixel voltage is clocked through, the reset level is subtracted and the bias voltage added. The last op-amp buffers the CDS capacitor and drives the pixel level to the A/D. The op-amp buffer has high input impedance and low leakage to minimize input current errors.

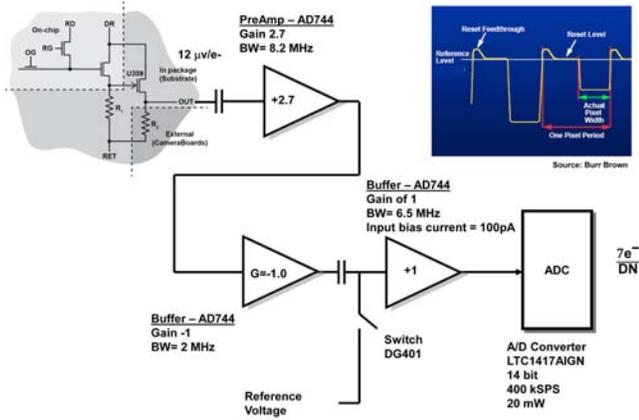
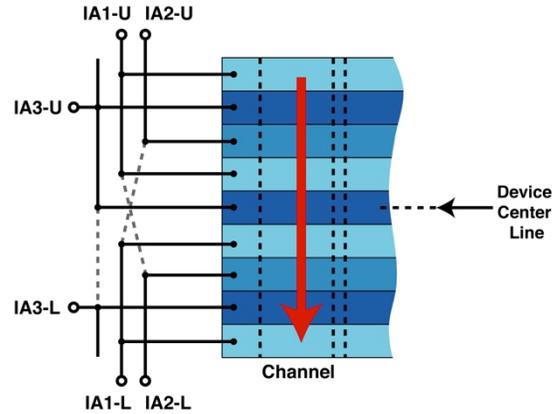


Figure 5 CDS Block Diagram

5. CCD DRIVE CIRCUIT

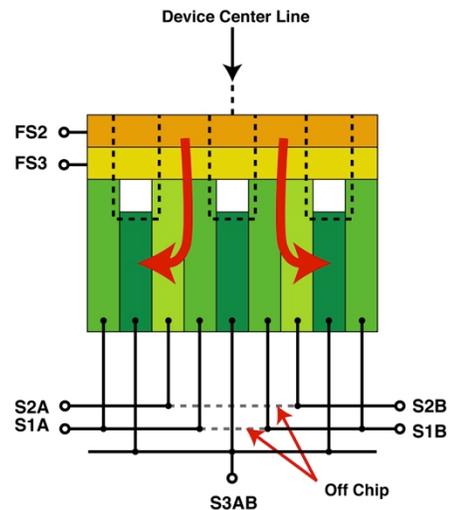
The CCD requires image clocks to move the collected charge in the pixels under the light shield and to the serial registers. The serial clocks move the charge to the output node where the charge is converted to a voltage. The image clocks have to drive the combined capacitance of the all the pixels which can be many nanofarads. This capacitance is distributed across the resistance of the polysilicon of which the CCD pixels are created. This distributed resistance and capacitance of the pixels limits the frequency of operation. Through testing the maximum image shift frequency of the CCID-51M was determined to be 45 kHz. The large capacitance requires a strong current drive and this is

provided by the Micrel 4427 FET driver. The driver can source over an amp of current to the image clocks. The 4427 is a single ended driver which requires level translating. In this design analog switches convert the 3.3 V digital control signals to typical CCD levels of -4V to +6V.



Unidirectional

Figure 6 Image Area Clocking Diagram



Bidirectional

Figure 7 CCD Serial Register Clocking Diagram

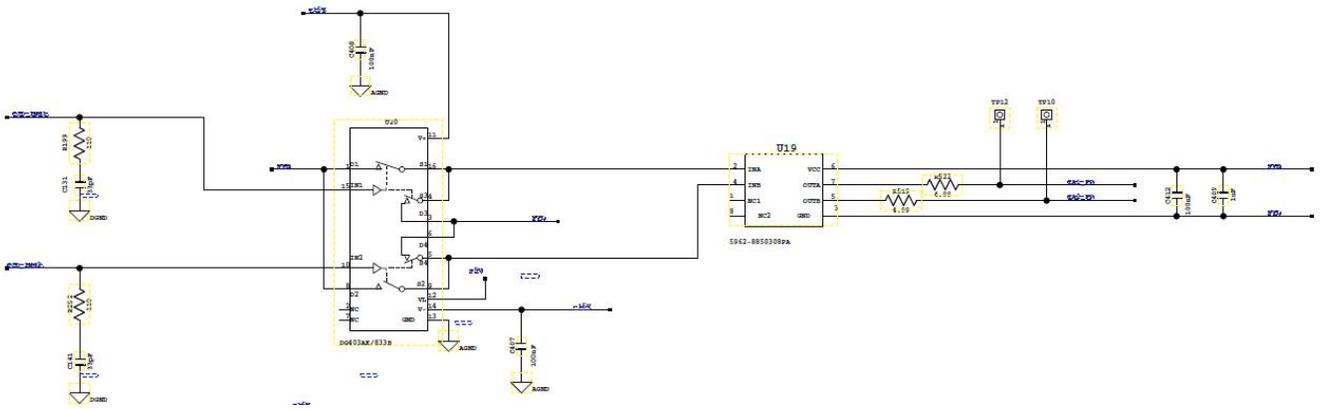


Figure 8 Image Clock Drive Circuit Schematic

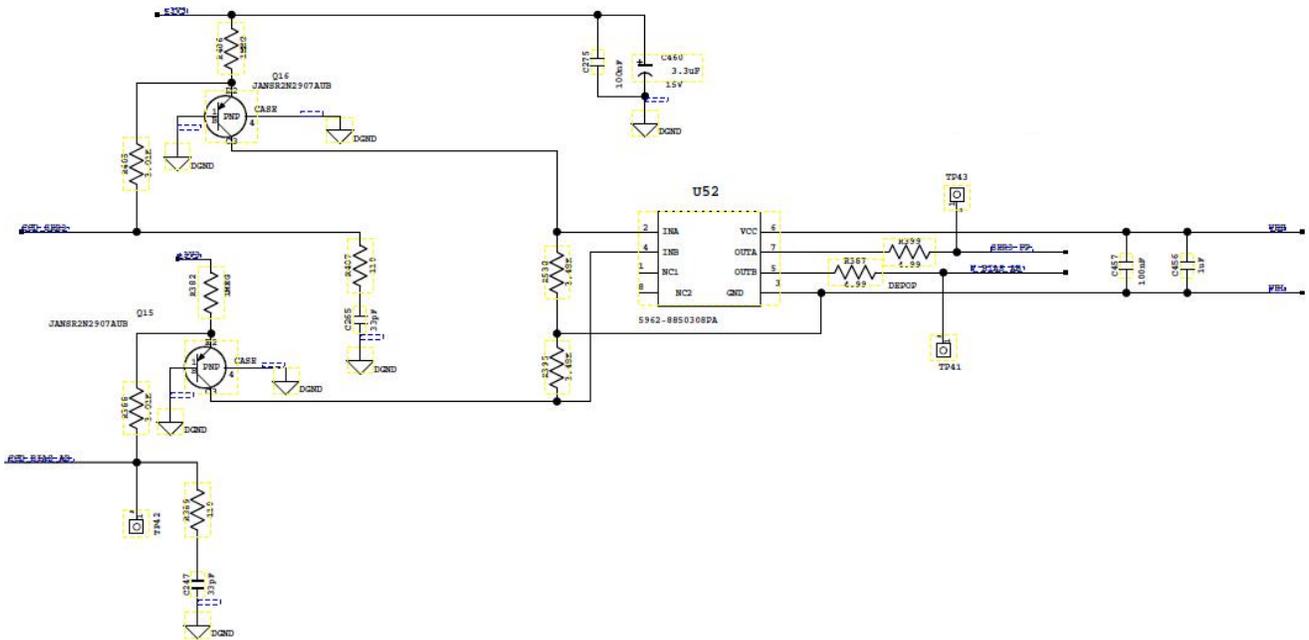


Figure 9 Serial Clock Drive Circuit Schematic

The serial clocks consist of only one row of pixels and are lower in capacitance than the image and storage areas. They are also clocked much faster at a 400 kHz rate. The 4427 is also used to drive the serial clocks but the faster clock precludes the use of the same analog switch. A different circuit using a transistor in a cascade configuration provides level translation shown in Figure 9.

6. CCD BIAS AND CHARGE PUMP

A CCD requires many bias levels to operate. Varying the biases and clock voltages is very useful for testing and optimizing the CCD performance. This design uses two octal Digital to Analog Converter, DAC8800, to provide the flexibility to vary voltages via a serial interface from the FPGA. The voltage outputs of the DAC are buffered with

the AD4096 quad opamp. For the low current biases, the AD4096 drives the voltage directly. Higher current biases require a voltage regulator and the AD4096 drives the adjust pin of the regulator.

A few of the biases are higher than the 15V and a charge pump is used to boost the voltage from 15V to above 25V. The charge pump is a two stage circuit also driven with the MIC4427 FET driver. The FET driver is a convenient switch to charge the capacitors for the charge pump. The driver can source over 1A and operates at 10KHz. The charge pump easily sources ~30 ma.

The charge pump output is linearly regulated to 22V. The drain bias for the CCD (typically 18V) is derived from the 22V with an opamp output drives the adjust pin of a regulator. Other opamp biases are supplied with the 22V.



Figure 12 ProAsic3

The I/O banks of the FPGA are supplied with 3.3V though some of the devices which it interfaces with require 5V level signals. A bi-directional logic level translator is used for this interface, the Aeroflex UT54ACS164646S. Two 16 bit devices are used for all the signals necessary to interface to the A/D's and the clamp in the CDS channels.

The FPGA is clocked with a 40 MHz oscillator. This was selected to support a 20 MHz synchronous serial output data interface. The interface consists of data and clock signals as well as frame, line, and data valid. The signals are converted to LVDS levels with LVDS drivers.

The ProAsic is reprogrammable through JTAG through an external connector. This allows programming throughout the development and test cycle up to final integration of the Space Vehicle without opening the chassis.

A Camera Link IC was included on the prototype to support development but will not be populated on the flight build.

The overall power dissipation for the FPGA is ~55 mW.

8. INPUT POWER

The CEB is supplied with regulated, low noise, 3.3V, +15V, and -15V. These supply voltages are filtered with a common mode choke. The +15V and -15V inputs have additional transistor filters. All three inputs have high side current sense which is buffered with an instrumentation op amp.

Additional voltages are derived from these inputs. A linear regulator generates +5V from the +15V. This is used for the video A/D's, DAC's, the logic level translator, and a few other circuits.

The overall measured power draw is 3.5 W at 20 °C.

9. HOUSEKEEPING

Most of the voltages and all of the input currents are

sampled with four octal input analog to digital converters. The 12 bit A/D used is the ADC128S102 from Texas Instruments. The supply voltage is 3.3V and many of the voltages sampled are attenuated with resistor dividers to match the input range. The A/D conversion is ratiometric. One input on each A/D is a 2.5V reference to correct any errors due to variations in the 3.3V supply.

The board temperature is monitored with a thermistor. An RTD is located next to the CCD measures the CCD temperature. The CEB provides a reference voltage to drive the RTD and sampled with the AD620 instrumentation opamp.

10. THERMAL ANALYSIS

An emphasis was placed on low power which benefits the thermal design. Typical power hungry components such as the FPGA and A/D converter were specifically chosen for low power dissipation. The complete design was analyzed with ICEPAK 15.0.7. modeling only conduction cooling. The board is contained in an aluminum chassis bolted to the spacecraft panel. The panel was held to the hottest expected temperature of 34 °C. The hottest component on the board, with a junction temperature of 63 °C is one of the AD744 opamps in the analog chain. The other hot components were linear regulators with junction temperatures around 60 °C. All junction temperatures were well below the design limit of 100 °C.

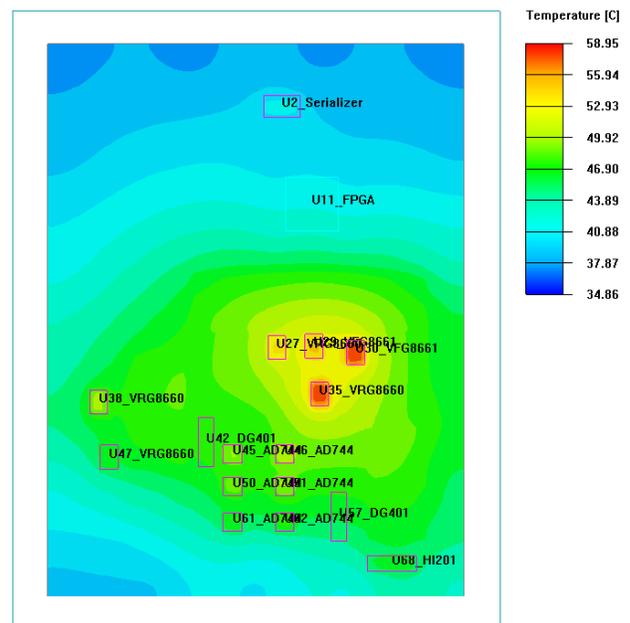


Figure 13 Thermal Analysis

11. VIBRATION ANALYSIS

The printed circuit design was analyzed over the expected

launch loads and quasi-static loads. The lowest frequency harmonic mode was 227 Hz next to a connector. The FPGA package was analyzed for fatigue life and passed and all components passed the Steinburg criteria for maximum displacement.

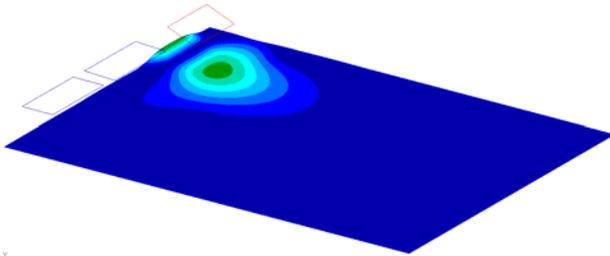


Figure 14 Vibration Mode Analysis

12. TEST RESULTS

A prototype board was completed in February of 2015. Since then it has gone under extensive testing. Several support boards were made to facilitate the testing. A general purpose FPGA board with LVDS I/O and a Camera Link output was used to interface to the avionics. This supported the command and control interface and also converted the SSL data interface to Camera Link interface. This provided a compatible path to collecting data into the test computer from either the Camera Link interface on the board or from the avionics interface.

Another support board was built to simulate the CCD. This board emulated the loading of the CCD clock lines and biases. The CCD video signal is simulated by attenuating the horizontal clock, S3, and buffering it with a U309 JFET biased with the biases, Vdr and Vrd. The circuit also buffers all the clocks and bias and multiplexes them for measurement with an oscilloscope. This facilitates automated testing with Matlab scripts.

A series of Matlab scripts have been written with test the majority of the board functionality and interfaces. The scripts provide a good way to test the CCD interface by measuring all the CCD clock frequencies and levels, all the biases, and the video chain. Other scripts test integration time, test patterns, housekeeping, and the command and control interface. The test patterns include header information which is verified. These scripts will expedite testing during environmental and unit test.

The real verification of the CEB is when the board operates a CCD. The full sensor can be tested with a dark image and test pattern. The read noise is measured with the CCD at the operating temperature of -40 °C. Some of the test results are shown below.

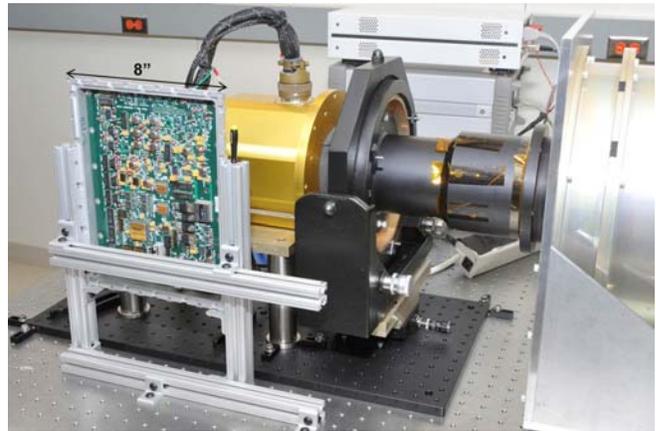


Figure 15 Camera Test Setup with CCD in Dewar

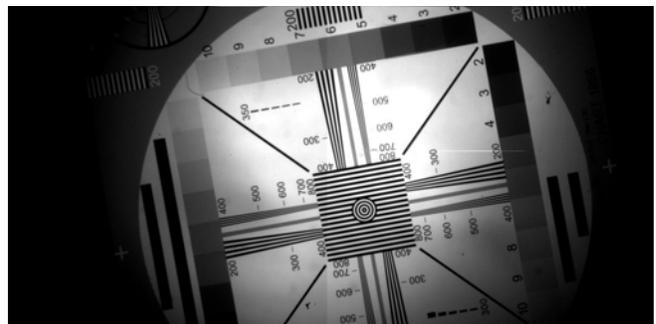


Figure 16 Test Image

System gain is measure with an x-ray source such as Cadmium¹⁰⁹. A Cd¹⁰⁹ K α x-ray generates ~6300 electrons when it interacts in silicon. The histogram below shows the number of digital counts generated by the K α peak. The system gain is the number of electrons in the peak divided by the digital counts, 6300 e-/ 920 DN = 6.8 e-/DN.

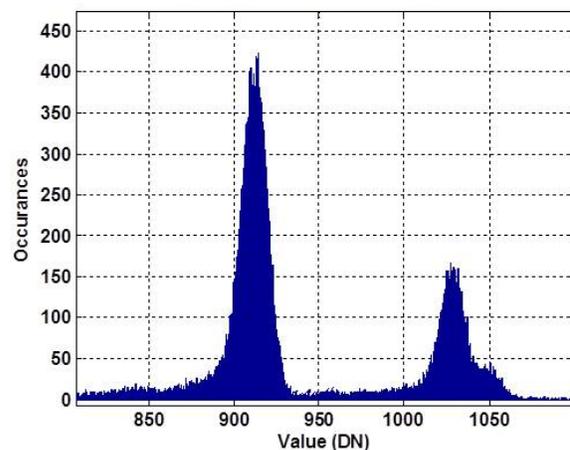
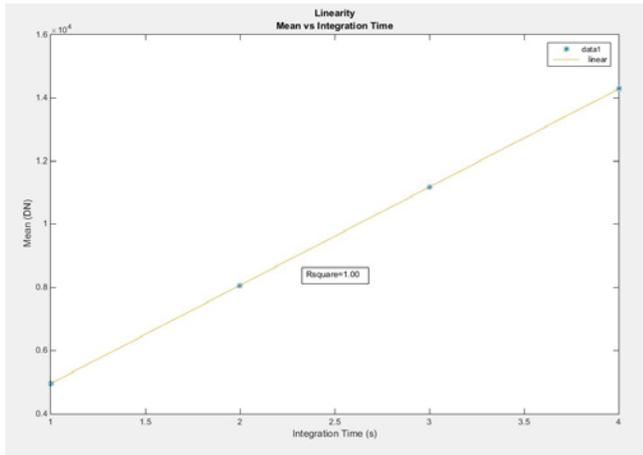


Figure 17 Cadmium¹⁰⁹ Histogram

Linearity is measured by imaging a flat field and calculating the mean while varying the integration time. The measured linearity is excellent as shown in the figure below.



11. CONCLUSION

The paper describes the design of camera electronics for the SensorSat spacecraft. The electronics are low power to accommodate the limited power of a microsatellite and low noise to provide good sensitivity. The circuit design provides all the circuitry to read out the CCD and process and digitize the video signal. The FPGA generates all the timing signals, formats and outputs the video data, and provides the control to the avionics to operate the sensor. A prototype board was built and tested and the results summarized. The prototype board met all the requirements and was operated with a CCD from the same lot as flight. The EDU board is fabricated and awaiting assembly.

ACKNOWLEDGEMENTS

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- [2] CCID51M Users Manual, James Gregory, MITLL

BIOGRAPHY



Andrew Cunningham received a B.S. in Electrical Engineering from University of Michigan, Ann Arbor, MI, and M.S. in Electrical Engineering from Northeastern University, Boston, MA. He has been with MIT Lincoln Laboratory for 11 years. He was a lead engineer on several space imaging projects involving Lincoln CCD's.

Previously he worked at Adaptive Optics Associates for 17 years in Cambridge, MA, and Raytheon Corporation for 3 years.