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CHARACTERIZATION OF CARRIER TRANSPORT PROPERTIES IN STRAINED CRYSTALLINE Si WALL-LIKE STRUCTURES AS A FUNCTION OF SCALING INTO THE QUASI-QUANTUM REGIME

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14. ABSTRACT

This research focused on transport characteristics of electrons and holes through narrow constricted crystalline Si "wall-like" long-channels that were surrounded by a thermally grown SiO_2 layer. The strained buffering depth inside the Si region (due to Si/SiO_2 interfacial lattice mismatch) is where scattering is seen to enhance some modes of the carrier-lattice interaction, while suppressing others, thereby changing the relative value of the carrier's effective masses of both electrons and holes, as compared to bulk Si. Importantly, as a result of the existence of fixed oxide charges in the thermally grown SiO_2 layer and the Si/SiO_2 interface, the effective Si cross-sectional wall widths were considerably narrower than the actual physical widths, due to the formation of depletion regions from both sides. The physical height of the crystalline-Si structures was 1500 nm, and the widths were incrementally scaled down from 200 nm to 20 nm. These nanostructures were configured into a metal-semiconductor-metal device configuration that was isolated from the substrate region. In the narrowest wall devices, a considerable increase in conductivity was observed as a result of higher carrier mobilities due to lateral constriction and strain.

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1 SUMMARY

The University of Missouri at Columbia, MO and the Air Force Research Laboratory, Kirtland AFB NM, collaborated on this research study pertaining to the fabrication, analysis of scaled down semiconductor devices, and theoretical quantum mechanical modeling. The work was carried out under the AFRL Grant No. FA9453-10-1-0001. The semiconductor processing, fabrication and the resulting carrier transport characteristics of Mobile Service Manager (MSM) devices fabricated as wall like structures in silicon on insulator technology were reported. MSM device dark current, direct current (DC) photocurrents, and the time response of carrier transport were investigated. The resulting conducting channels were actually smaller than their physical dimensions, a result of depletion of carrier near the interfaces. As the physical channel widths were reduced by oxidation, strain was produced near the interface and strained lattice became a significant portion of the conducting channel. The increase in mobilities for both holes and electrons stemming from the strained silicon resulted in a dramatic increase in carrier mobility for both electrons and holes as the physical channel width was reduced from 200 nm to 20 nm. The theoretical model incorporating the effects of strain present in these nanoscale MSM devices compared favorably with experimental results, showing that hole mobilities increased with decreasing L. Additionally, if these electron and hole mobilities can be retained with the application of gate electrodes, then this technique may yield a much simpler path towards high performance Complementary Metal Oxide Semiconductor (CMOS), both n-channel and p-channel, than current techniques for either planer ultra-thin body Field Effect Transistor (FET)s or Fin shaped Field Effect Transistor (FinFET)s.

2 INTRODUCTION

In thin film silicon-on-insulator (SOI) technology a buried oxide layer separates the active Si device structure from the parasitic influence of the substrate, thus making the device less susceptible to radiation effects, specifically single event upset. [1] The fabrication of such devices is fully compatible with existing very-large-scale integration (VLSI) fabrication technology. [2] Moreover, it has become possible to develop and study electrically isolated ultra-thin-films and nanostructures for the quantum confinement effects on electrons and other quasi-particles, such as holes and excitons. [3]

The effects of quantum confinement on carrier transport properties, however, have been primarily investigated in ternary and quaternary material heterostructures and superlattices, in which scattering is seen to enhance some modes of electron-lattice interaction while suppressing others, thereby changing the relative value of the carrier's effective masses of electrons and holes, as compared to bulk semiconductors. [4] Such studies in Si have been very limited.

In the nano-scale-regime, electrons start to behave more like waves than particles, yet this transition to quantum mechanical regime does not come about abruptly. Rather, there is a transition region in which bulk properties begin to slowly weaken while the quantum mechanical effects begin to strengthen. [5] Because of the lack of available scientific literature on this subject in Si, it is evident that little attention has been focused in this transition bulk/quantum region of Si. Nevertheless, an understanding of the physics, in particular electron-hole transport properties, including the role of biaxial strain, in the transition region of the semiconductor devices is of great importance due to the increased interest as the VLSI devices are scaled down to the nanometer regime. [6]

Strain is an important aspect of CMOS and has been incorporated into planar CMOS as standard practice since the late 1990s, specifically in the 90 nm technology node, in order to enhance carrier mobilities and ultimately device drive currents. As detailed by S. W. Bedell et. al. [7], biaxial wafer scale tensile strain was accomplished first, achieved by growing silicon epitaxially on relaxed Ge_xSi_{1-x} since the lattice constant of silicon was less than the germanium-silicon alloy. While this silicon germanium wafer scale approach resulted in enhanced nFET drive current, there was no discernable p-type field-effect transistor (pFET) drive current enhancement. By incorporating Ge_xSi_{1-x} layers in the source and drain regions of pFET devices, uniaxial compressive strain was achieved and resulted in 50% enhancement in hole mobilities and subsequently p-type field-effect transistor (pFET) drive currents. The result was a biaxial tensile strained n-type field-effect transistor (nFET) and a uniaxially compressive strained pFET fabricated simultaneously in the CMOS application.

Continued scaling of CMOS in accordance with Moore's Law and the International Technology Roadmap for Semiconductors (ITRS) roadmap required increases in both uniaxial and biaxial strain to achieve necessary drive currents. Uniaxial strain was augmented by increasing the Ge content in the source and drain Ge_xSi_{1-x} layers, closer proximity of the germanium bearing layers to the channel, and with new gate structures designed specifically to transfer strain to the channel. Uniaxial tensile strain was also achieved in the channels of nFET devices as well by incorporating a layered source and drain using carbon rather than germanium to reduce the lattice parameter of silicon.

As device pitch was reduced, localized stressors for pFETs became less effective due to the reduced volume of Ge_xSi_{1-x} material, and the stressor for nFETs, carbon bearing silicon, approached the limits of solubility of carbon in silicon. Ultimately, the practical limit for this type of strain scaling may be reached as a result of severely reduced circuit lifetimes or premature material failure [7].

A scalable approach achieved by utilizing wafer level strain with devices fabricated on mesas providing a virtual local substrate, has proved beneficial for device pitch below 100 nm. Strained virtual substrates are grown on insulator material, germanium-silicon provides compressive strain for pFETs while strained silicon on insulator provides tensile strain for nFETs. Initially strain is biaxial but as mesa widths are reduced below 0.3 μm biaxial strain is converted to beneficial uniaxial strain. While this provides a promising path towards reduced pitch, edge relaxation still poses a problem for device reliability [7].

Regarding three dimensional devices such as new multi-gate or tri-gate architectures, also known as FinFET technology, although these devices have achieved performance enhancement by virtue of increased sub-threshold slope and a reduction in drain induced barrier leakage with the gate geometries, they are operated at relatively high *Ioff* and higher voltage drain supply (VDD) to achieve higher switching speed. At these increased operational parameters, higher channel mobilities becomes desirable. Process induced stressors in the form of embedded silicon germanium layers in the source and drain have been modeled and shown to have a modest performance increase, approximately one-half of the mobility boost for similar size planar FETs [7]. It turns out that process induced strain in FinFETs is most effective directly under the gate but diminishes below the gate and along the sides of the channel, thus reducing average mobility and the effectiveness of stressors. Attempts to increase strain in the channel and along the sides of FinFETs with the choice of gate material and oxides are limited in their selection by the work function, inversion capacitance, fabrication complexity and reliability. Incorporation of wafer level strain using SiGe-on-insulator (SGOI) and Strained Silicon-On-Insulator (sSOI) in small pitched circuits may be possible by converting the tensile strain of sSOI to compressive strain by selective

growth of silicon-germanium. The industry is left at a point where device complexity will have to be increased to provide methods for strain incorporation.

In this report we describe the comprehensive study where the nature of carrier transport properties are evaluated as a function of dimensional scaling wall widths from 200 nm to 20 nm in devices where the width is reduced by thermal oxidation and stress naturally accumulates in the device channel. We believe that these wall structures are a useful starting point for a broader study, as these can be configured into novel high density 3-D devices, where thermal effects, such as heat buildup, can also be efficiently managed. [8]

3. METHODS, ASSUMPTIONS, AND PROCEDURES

3.1 Rationale for substrate material

SOI wafers with < 100 > top active layer crystal orientation were used to fabricate the wall-like structured test devices for this study. The initial SOI structure had a 1500 nm top active layer on a 3000 nm buried oxide. The SOI configuration allowed complete electrical isolation of the top active Si layer from the underlying substrate. All five samples in this study had identical p-type active layer with a lightly doped concentration of 10^{14} cm^{-3} boron atoms. Intrinsic SOI wafers would have been an ideal choice for the experiment, however due to the commercial unavailability of completely 100% intrinsic material, the above choice of dopant type and concentration was carefully made in order to minimize the effects of impurity scattering as a result of redistribution of impurities during the thermal oxidation process. Boron was chosen as dopant because it tends to segregate away from the Si interface and into the thermally grown oxide, thus reducing the impurity concentration near the Si interface with SiO_2. [8] Thus the segregation coefficient, which is defined as the ratio of the dopant concentrations at the interface, is less than one. This process leads to the formation of an oxide trapped charge (Q_{ot}), which contribute to the formation of a depletion region near the Si/SiO_2 interface. [9,10]

This oxide trapped charge (which can be calculated from the doping concentration) coupled with the estimate of fixed charge (Q_f) which results from the excess Si atoms not reacted with the oxygen and the estimate of interface trapped charge (Q_{it}) which results from the mismatch between the number of atomic bonds in the Si crystal surface and the number of available bonds in the SiO_2 layer combined ($Q_{ot} + Q_f + Q_{it}$) significantly reduce the dimensional cross-sectional area of the channel width. 10 Based on the literature, for the given parameters, it is reasonable to expect that the depletion region in Si would extend to a thickness of approximately 40 nm from the Si/SiO_2 interfaces, considering the thermally grown oxide was at least 50 nm thick. [11] Thus a physical Si wall width of approximately 100 nm would have an effective width of 20 nm.

3.2 Crystalline silicon wall nanostructure fabrication

In order to fabricate the wall structures, photoresist nano-scale pattering was required. The precursors to the wall structures were patterned using interferometric lithography (IL) and reactive-ion-etching (RIE). IL is a well-developed technique for inexpensive nano-patterning process. [12] IL, in its simplest form, is interference between two coherent waves resulting in a 1-D periodic pattern defined by $\lambda/2 \sin \theta$ where λ is the optical wavelength and 2θ is the angle between the interfering beams. A typical IL configuration consists of a collimated laser beam incident on a Fresnel mirror (FM) arrangement mounted on a rotation stage for period variation. [13] There is no z-dependence to an IL exposure pattern, which is limited only by the laser

coherence length and beam overlaps. [14] The 1-D nano-scale pat-terns were first formed in the photoresist followed by pattern transfer onto the underlying substrate using RIE in a parallel plate reactor using SF_6 plasma chemistry. Figure 1 shows a scanning electron microscope (SEM) cross-sectional image of an array of nano-wall structures with a remaining layer of patterned photoresist after RIE has been performed.

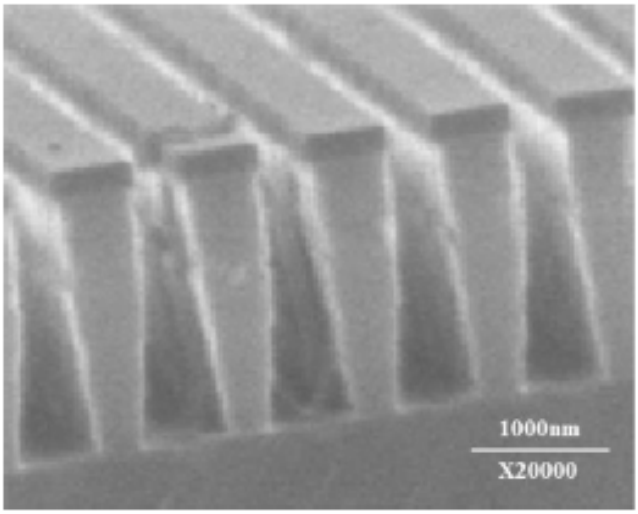

Figure 1. Scanning electron microscope (SEM) cross-sectional image of an array of wall precursor structures with a remaining layer of patterned photo-resist after reactive ion etch process step

Note at this stage these structures are merely the precursors to the thin wall structures that are then reconfigured into MSM devices. After the photoresist was re-moved the wall structures were thermally oxidized, in the absence of H_2, in order to further minimize any effects of dopant (boron) redistribution. The oxidation process accomplished two things. First it consumes the Si thus thins the wall width. Secondly the thermally grown oxide preserves a low defect, clean Si/SiO2 interface and at the same time passivates the surfaces of the nanostructures [15,16]. While the Si/SiO_2 interface is low defect, it is important to note that strain is present at the interface and reduces with distance from the interface. This reduction in strain as a function of depth has been seen experimentally in Si/SiO_2 interfaces using a scanning transmission electron microscope using Z-contrast imaging to produce strain contrast imaging [17]. Using this technique, the 1/e decay length was measured at 0.2 nm. The modeling of the thermal oxidation parameters needed for the desired thicknesses was complicated due to the fact that in a three dimensional wall structure there are several crystal lattice orientations that have different thermal oxidation rates. As a first order approximation, we used average values of oxidation rates between the various lattice orientations i.e. oxygen flow rate, pressure, temperature and time. These parameters were then fine-tuned

empirically during the actual thermal oxidation runs. Figure 2(a)-2(c) show SEM images of the cross-sectional views of the wall structures after the respective thermal oxidations.

As can be seen from the SEM images, due to the high aspect ratio of these structures the oxidation rate was not fully uniform throughout the height of the walls. The rate was faster at the top part of the walls and slower at the bottom part due to higher availability of oxygen atoms in the upper regions. The wall-like structures then formed the active region of the MSM devices as described in the next section.

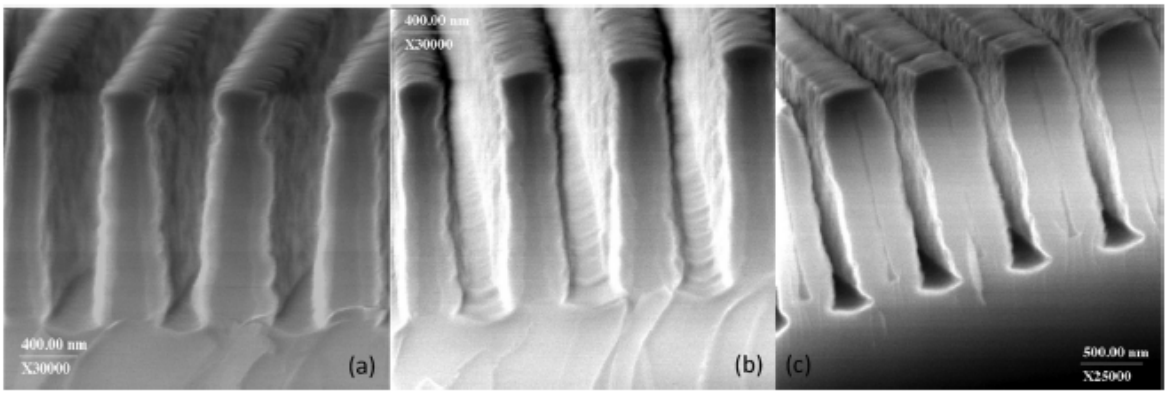

Figure 2. SEM cross-sectional images of any array of wall structures after thermal oxidation; (a) 200nm wall structures (b) 95nm wall structures; (c) 40nm wall structures

3.3 MSM device fabrication

The wall structured samples were then configured into two terminal metal-Si/nanowall-metal (MSM) devices for optical and electrical characterization. The MSM device configuration was specifically designed so the current would flow alongside within the wall boundaries between the electrodes. This allowed the physical cross-section of the wall structures to dictate the current flow properties. The mesa structures were fabricated to cutoff any stray current paths that could bypass the intended active region (wall) carrier path. Figure 3(a) shows a SEM picture of a typical

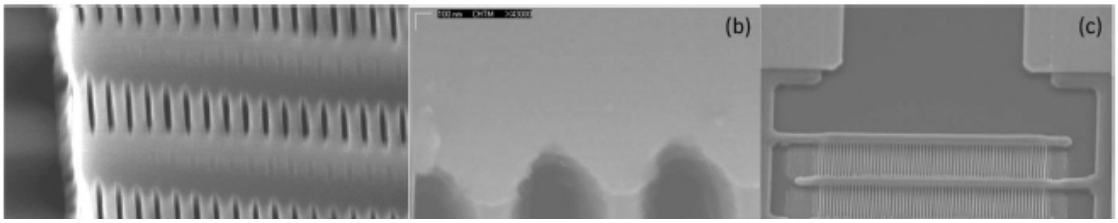

Figure 3. SEM image of (a) pre-oxidized Si mesa configuration with precursors to wall structures in the active region in-between planar un-textured regions where the metal contacts will be deposited; (b) planar un-textured Si where thermally grown oxide was removed from metal contact deposition connection walls; (c) fully fabricated wall device with interdigitated electrodes.

pre-device mesa structure. After the walls were oxidized to achieve the desired wall width, the thermally grown oxide was selectively removed from the planar un-textured Si pad locations [Figure 3(b)] using an appropriate photo-mask and a chemical 1:6 buffered oxide etch (BOE) process.

Following the resist removal the samples were cleaned using a sulfuric-acid:hydrogen-peroxide solution and a DI water rinse followed by a nitrogen gas dry step. The samples were then re-patterned using photoresist and a second mask was used for the process to form the electrode contact regions. Three separate evaporations (30 nm of Ni) were performed. The first one was performed at a normal incidence to the sample surface and the other two at a 30o degree tilt angles in order to ensure complete coverage of the mesa step height. After Ni evaporation, lift-off was performed to remove the unwanted metal and resist using acetone. Following a thorough clean using methanol/DI-water, the samples were again dehydrated and spin-coated with a thick resist layer. The samples were patterned using a final metallization mask set. A layer of Cr and Au was evaporated on the electrode regions. 30 nm/200 nm of Cr/Au were evaporated and liftoff process was used to remove the resist and unwanted metal. Figure 3(c) shows SEM pictures of a fully fabricated wall device.

3.4 DC measurements

At room temperature only a small number of carriers are thermally generated (as dark current) for a Si bandgap of 1.15 eV. At low bias voltages (linear region of operation) the slope of the I-V dark current is proportional to the device resistance that includes contributions of thermally generated carriers from both the wall channels and the metal/semiconductor contact regions. At higher biases the current saturates when all thermally generated carriers are collected. Any further increase in the current can be attributed to leakages across the contact metal-semiconductor barrier and to non-linear generation of carriers across the barrier. [18] The back interpolation of this leakage current to the zero bias (0 V) is a measure of the saturated dark current (Ids). Although the photocurrents are a few orders of magnitude larger than the thermally generated dark currents, the analysis of the photocurrent (Ips) IV function is the same as the dark current (Ids) IV plots. For dc response analysis, three sets of measurements were performed. These include (i) dark currents as a function of wall width thickness, (ii) photocurrents as a function of wall width thickness, and (iii) spectral responses as a function of wall thicknesses. These results are discussed and analyzed below.

3.5 Dark currents versus wall width thickness

To study the carrier conduction properties versus dimensionally scaling down the width of the wall structures into the nano-regime, the samples were characterized in batches. Using samples with wall widths of 200 nm, 95 nm, 75 nm, 40 nm, and 20 nm, the room temperature dark currents were measured with a probe station and digital I-V curve tracer. As the physical cross-sectional area of the wall widths was reduced from 200 nm to 20 nm, we know from Ohm's law, the resistance should increase linearly as a function of area. In other words the resistivity in units of Ω/cm^2 should remain constant.

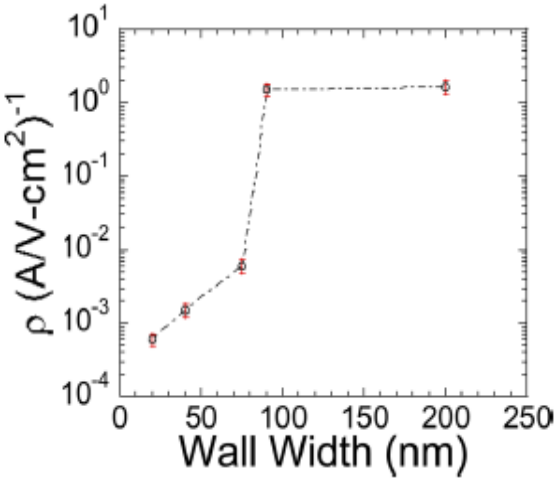

Figure 4. Plot showing resistivity characteristics as a function of down scaling the wall widths.

However, as can be seen from the Figure 4, the resistivity is not constant but drops significantly as the width of the wall is reduced below 95 nm. This suggests that there is an increase in conductivity as the wall thickness decreases from 95 nm to 20 nm. Since the number of thermally generated carriers is directly proportional to the volume of the active region, any increase in the conductivity, as wall width cross-sectional region decreases from 95 nm to 20 nm, cannot be attributed to the volume of the semiconductor material, but must be the result of a substantial increase in the carrier velocity. Confirmation of this hypothesized mechanism was obtained with the use of transient time analysis as discussed in section G. Further verification of this hypothesized mechanism was performed through transient time analysis as discussed in section 3.8.

3.6 Photocurrents versus wall width thickness

DC steady state photocurrents were measured using a 365 nm wavelength, 1.132 W/cm2 argon-ion laser and a 633 nm wavelength, 3.96 W/cm2 HeNe laser. The laser beam spot diameter was less than 8 μm and was focused within the active region of the electrode spacing covering several wall structures. By using 365 nm and 633 nm wavelengths, a more complete insight into absorption and carrier transport as a function of wall thickness can be achieved. At 365 nm,

absorption occurs within the top first 10 nm of the Si wall structures with heights of 1500 nm. For 633 nm the total photon absorption extends through the entire wall height. Figure 5(a) and 5(b) show the conductivity versus wall thickness profiles.

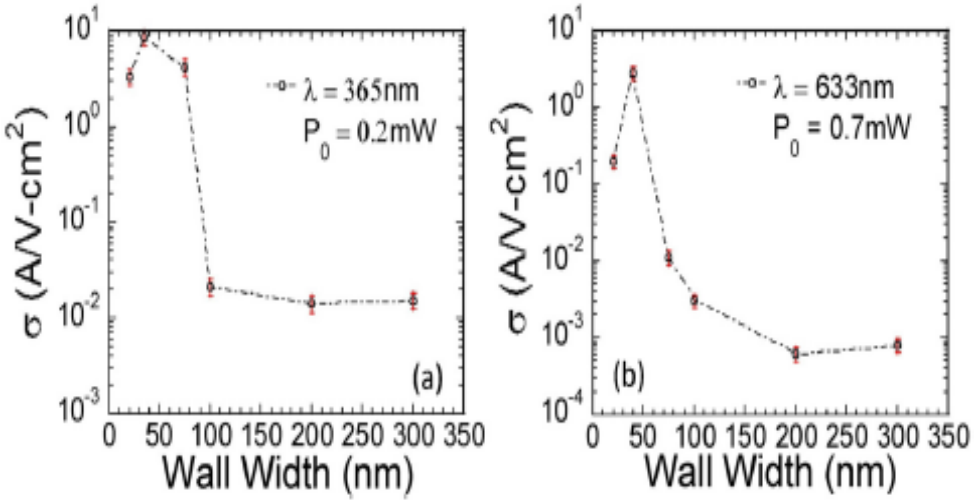

Figure 5. Plots of photoconductivity characteristics as a function of down scaling the wall widths (a) for ƛ=365nm; (b) for ƛ=633nm

As can be noted from the figures, a peak in the conductivity occurs around the 40 nm wall physical width of the samples followed by a decrease in the 25 nm wall width sample. The significance of this can be discussed through the effects of strain on the structure on the mobility of the carriers as the dimensions are reduced in section 3.8.

3.7 Transient time response measurements and analysis

The schematic of the pulsed carrier transport experiment is shown in Figure 6.

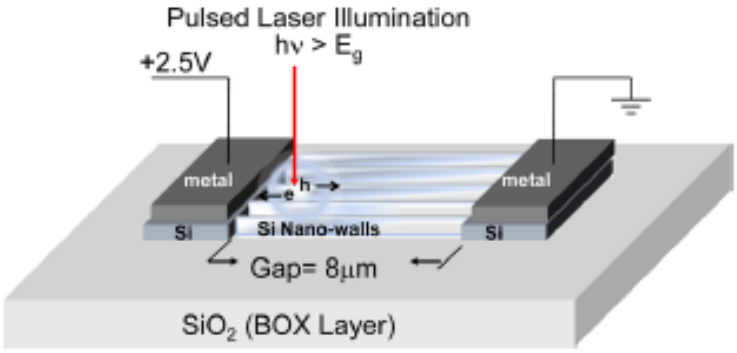

Figure 6. Schematic configuration of a wall structured MSM device used for carrier time response measurements

When a narrow pulse of light strikes the wall structured active region of the device near the left electrode as shown in Figure 6, equal number of electrons and holes are generated and are then subjected to diffusion and drift forces in a presence of an electric field. Based on the experimental configuration the electrons will be rapidly collected near the positively biased electrode and the holes will have to travel the entire active region to the negatively biased electrode. From the measured time response signal profile at the opposite electrode, the hole transient time limited carrier velocity can be determined, provided the carrier lifetime is greater than the total transit time. If the optical pulse of light strikes near the opposite electrode, the holes will be rapidly collected and the electrons would have to transit through the active region, thus the measured signal at the opposite electrode would be electron transit time limited.

The pulsed response measurements were taken using 150-fs duration excitation at $\lambda = 400$ nm from a cw mode-locked Ti:Al_2O_3 laser (doubled for the short wavelength, 0.2 mW average power at a 77 MHz repetition rate). The wall structured MSM devices were probe tested using an 18 GHz probe and a high-speed digital sampling oscilloscope with an approximately 1 ps resolution capability. The laser spot size was 1 μm in diameter and the electrode gaps were 8 μm. Normal incidence was used for the experiment. The time response measurements were taken for low electric field strengths 3×10^3V/cm, (2.5 V across 8 μm gap) thus avoiding velocity saturation.

Before the experimental data and analysis is provided it is useful to review the three primary factors that can impact the carrier transport through a semiconductor region. These factors are:

• Field dependent velocity of carriers through the active region. At high E-fields, the velocities of both electrons and holes in Si saturate at about 1×10^7 cm/s, [19] provided the field within the electrodes exceeds the saturation value for most of its length, we can assume that the carriers move with an average velocity drift. Velocity saturation is not an issue in our experiment since the applied field is much lower than what is required for saturation.

• Diffusion of carriers in the active region. The time it takes for carriers to diffuse a distance d is $\tau_{diff} = d^2/2D$ where D is the carrier diffusion coefficient. The diffusion of carriers becomes a two dimensional process as the thickness of the Si wall-structures is reduced and carriers are physically constricted in movement by the Si/SiO^2 interfaces from all sides.

• Junction and parasitic capacitance effects. A metal-semiconductor junction under reverse bias exhibits a voltage-dependent capacitance caused by the variation in stored charge at the junction represented by the relation $C_j = A/2(2e\varepsilon_s N_d)^{1/2} V^{-1/2}$, where the parameters have their usual meaning. This capacitance is usually quite small for MSM device structures as a result of their planar electrode design. There are also parasitic circuit capacitances associated with the probing and

cabling that usually dominate the electrical response as well as the limiting response of the electronics. For this study all film devices have an identical $\tau_{circuit}$ limitation.

Figure 6 represents the schematic with bias polarity of our experiment in which the left electrode polarity is positive and the right electrode is ground. With this bias configuration once a pulse of light with a spot size *<1* μm, as in the case of our experiment, strikes within the active region, the holes travel towards the right electrode and the electrons travel in the opposite direction towards the left electrode.

Figure 7 shows the experimental results of the time response measurements for *~200* nm, *~95* nm, *~40* nm and *~20* nm thick wall devices for both electron and hole dominated signals. From a first pass, as can be seen from these plots, as the thickness of the film decreased, the time response signal decays faster. In particular in the case of the *~40* nm and *~20* nm thick walls the signal decays over an order of magnitude faster over the *~200* nm sample for both electrons and holes. The rise time is of the signals is important since it gives direct insight to the carrier mobility. The rise time (t_d) is defined as is the time-lapse from moment when the pulse of light strikes one end of the active region of the MSM, near one electrode, and the moment when the photo-generated carrier signal is detected at the opposite electrode. From the rise time data we can now determine the carrier mobilities as a function of thickness as follows:

From the experimental time response measurements we can calculate the average carrier velocities by applying the given relation, $v_{(\text{Carrier-Velocity})}$ = (Electrode gap)/t_d (cm/s) where t_d is the average time it takes for the pulsed carrier signal to cross the electrode gap distance. The pulse travels in the presence of a field and expands from its originating point due to diffusion. In this case we are ignoring the RC time delay that the pulsed signal experiences once it reaches the edge of the depletion region near the electrodes since the widths of the depletion regions are very small in the submicron range compared to the electrode gap which is ~8μm in length.

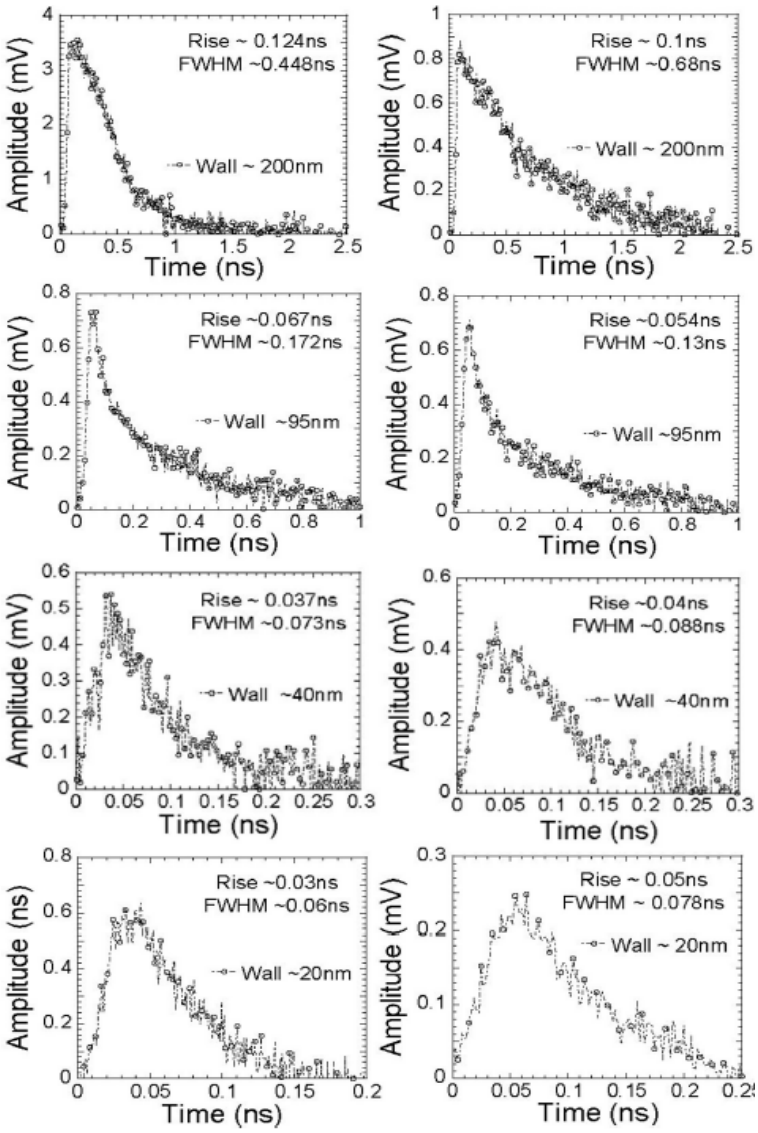

Figure 7. Measured time response signals of 200nm wall (row-1), 95nm wall (row-2), 40nm wall (row-3) and 20nm wall (row-4)

By definition the average carrier mobility can be written as,

$$\mu_{avg} = v_{(\text{Avg Carrier-Velocity})}/[V_{bias}/(\text{Electrode})]$$

where V_{bias} is the external bias applied to the electrodes.

Figure 8 shows a plot of average field dependent electron and hole limited mobility values using experimental values of rise time, t_d, and the above expression as a function of film thickness.

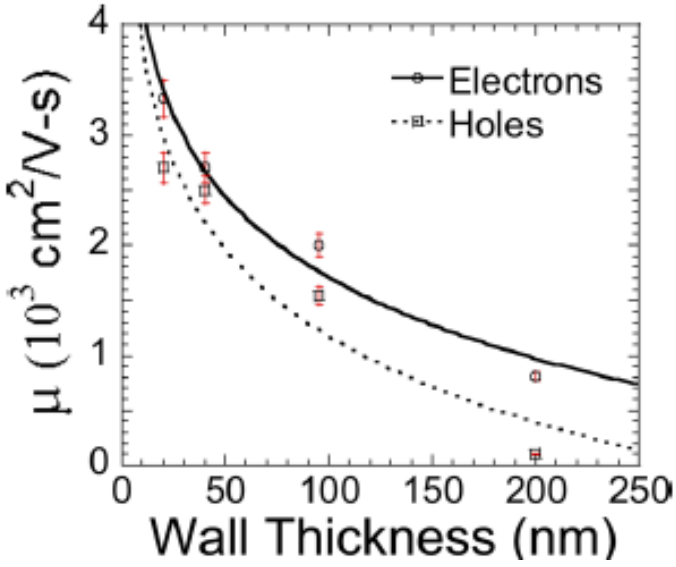

Figure 8. Carrier mobility values calculated from direct measure of rise time values as a function of wall thickness.

We know that the carrier transport of electrons and holes in the thickest wall sample (*~200* nm) is essentially similar to the transport properties in bulk silicon. However we observe a considerable increase in low filed dependent mobility values below *~75* nm wall thicknesses. Recall the fact that we actually have a much narrower effective cross-sectional regions form which carriers propagate due to the repulsive nature of the boundary at the Si/SiO_2 interface, and the carrier profile tends to peak a certain distance away from the interface close to the center of the wall structures. Therefore we believe that quantum confinement effects play a key role in the carrier mobilities of both electrons and holes. A detailed theoretical model is described in the next section which tends to explain our experimental results.

3.8 Theoretical Modeling using strain effects to explain rise in electron and hole mobility

If we consider a total valence-band hole concentration n_v then, the light-hole (n_{LH}) and the heavy-hole (n_{HH}) concentration will satisfy the charge-conservation relation $n_{LH} + n_{HH} = n_v$, where

$$n_\sigma = \frac{g_\Gamma g_s}{V}\sum_{\boldsymbol{k}}\left[1 + exp\left(\frac{E_k^\sigma \mp \eta\Delta E_{str}^v - u_v}{k_B T}\right)\right]^{-1} \approx 2g_\Gamma\left(\frac{m_\sigma^* k_B T}{2\pi\hbar^2}\right)^{3/2} exp\left(\frac{u_v \pm \eta\Delta E_{str}^v}{k_B T}\right),$$

where the subscript σ takes HH or LH and the upper (lower) sign corresponds to HH (LH) state. In the above expressions, the approximations are made for high temperatures, *V* is the volume of the silicon film, *T* is the system temperature, the zero energy is chosen at the middle point between the split pair of light-hole and heavy-hole bands, **k** is the three dimensional wave vector of carriers, $g_\Gamma = 2$ (not *6* due to strain effect) is the Γ-valley degeneracy for holes and $g_s = 2$ is the spin degeneracy for both light-holes and heavy-holes. In addition, u_v, which depends on both *T* and n_V, is the chemical potential to be determined for valence bands, $E_k^{HH} = \hbar^2 k^2 / 2m_{HH}^*$ is the kinetic energy of heavy holes and $E_k^{LH} = \frac{\hbar^2 k^2}{2m_{LH}^*}$ is the kinetic energy of light holes, where $m_{HH}^* = 0.49m_0$ and $m_{LH}^* = 0.16m_0$ ($m_0$is the free-electron mass) are the effective masses for heavy holes and light holes, respectively. Additionally, ΔE_{str}^v introduced in the above expressions stands for the half of the valence-band splitting due to the existence of strain.

From the above two equations and $n_{LH} + n_{HH} = n_v$, we obtain $n_{LH}/n_v = [1 + \gamma^{3/2}\, exp(2\eta\Delta E_{str}^v/k_BT)]^{-1}$ and $n_{HH}/n_v = 1 - n_{LH}/n_v$, where $\gamma \equiv (m_{HH}^*/m_{LH}^*) > 1$. For biaxial and shear strains, [1,2] we have the valence-band splitting, given by $\Delta E_{str}^v = \pm\left\{(b^2/2)\left[\left(\epsilon_{xx} - \epsilon_{yy}\right)^2 + \left(\epsilon_{yy} - \epsilon_{zz}\right)^2 + (\epsilon_{zz} - \epsilon_{xx})^2\right] + d^2\left[\epsilon_{xy}^2 + \epsilon_{yz}^2 + \epsilon_{xz}^2\right]\right\}^{1/2}$, where the upper sign is for the compressive strain while the lower sign for the tensile strain in the direction perpendicular to the interface of silicon and silicon-dioxide materials, *b* and *d* are the optical deformation potentials, and $\epsilon_{jj'}$ represents the strain tensor in the three dimensional space with *j, j'* = *x*, *y*, and *z*, the diagonal matrix elements ϵ_{jj} are associated with biaxial strain, and the off-diagonal matrix elements $\epsilon_{jj'}$with $j \neq j'$ correspond to contributions from the shear strain. For silicon crystals, we have *b*= *-2.33* eV and *d*= *-4.75* eV.

The values of η can be scaled as $\eta = (1/L)\{\min(L, 2D_s)\}$, where *L* is the film thickness and D_s is the strain buffing depth due to lattice mismatch between embedded Si crystal and surrounding amorphous SiO_2 material at their interface, and $L - 2D_s > 0$ represents the film effective thickness free of localized trapping centers [19].

If we choose the *z* direction as the direction perpendicular to the interface for biaxial strain we simply get $\epsilon_{xx} = \epsilon_{yy} = \epsilon_\parallel$, $\epsilon_{zz} = \epsilon_\perp$, and $\epsilon_{ij} = 0$ for $i \neq j$, [19] where$\epsilon_\parallel = \left(a_{\parallel,Si}/a_{Si} - 1\right)$, $\epsilon_\perp = \left(a_{\perp,Si}/a_{Si} - 1\right)$. Moreover, the perpendicular lattice constant $a_{\perp,Si}$ is related to the parallel lattice constant $a_{\parallel,Si} = \overline{a}_{SiO_2}$ by $a_{\perp,Si} = a_{Si}\left[1 - (2c_{12}/c_{11})\left(\overline{a}_{SiO_2}/a_{Si} - 1\right)\right]$, where $c_{11} = 16.75 \times 10^{10}$ N/m^2, and $c_{12} = 6.5 \times 10^{10}$ N/m^2 are the elastic constants of silicon. For silicon and silicon-dioxide, we have $\overline{a}_{SiO_2} = (2 \times 4.914 + 5.405)/3 = 5.078$ Å and $a_{Si} = 5.431$ Å for amorphous silicon-dioxide materials. Therefore, we obtain $a_{\perp,Si}/a_{Si} = 1.050$. This leads to $\epsilon_\parallel = -0.065$ (compressive), $\epsilon_\perp = 0.05$ (tensile), and $2\epsilon_\parallel + \epsilon_\perp = -0.08$.

The total mobility $\mu_{\rm v}$ for holes can be expressed as

$$\mu_{\rm v} = \left(\frac{n_{\rm LH}}{n_{\rm v}}\right)\frac{e\tau_{\rm LH}}{m_0}\left[\frac{m_0}{m^*_{\rm LH}} + \Delta\left(\frac{m_0}{m^*_{\rm LH}}\right)\right] + \left(\frac{n_{\rm HH}}{n_{\rm v}}\right)\frac{e\tau_{\rm HH}}{m_0}\left[\frac{m_0}{m^*_{\rm HH}} + \Delta\left(\frac{m_0}{m^*_{\rm HH}}\right)\right] \approx \left(\frac{n_{\rm LH}}{n_{\rm v}}\right)\frac{e\tau_{\rm LH}}{m^*_{\rm LH}} + \left(\frac{n_{\rm HH}}{n_{\rm v}}\right)\frac{e\tau_{\rm HH}}{m^*_{\rm HH}}$$

$$\approx \left(\frac{e\tau_{\rm LH}}{m^*_{\rm LH}} + \gamma^{3/2}\frac{e\tau_{\rm HH}}{m^*_{\rm HH}}\right)\frac{1}{(1+\gamma^{3/2})} - \gamma^{3/2}\left(\frac{e\tau_{\rm LH}}{m^*_{\rm LH}} - \frac{e\tau_{\rm HH}}{m^*_{\rm HH}}\right)\left[\frac{\exp(2\eta\Delta E^v_{str}/k_BT)-1}{(1+\gamma^{3/2})^2}\right]$$

$$\approx \mu_v^{(0)}\left[1 - \frac{\eta(2\Delta E^v_{str}/k_BT)\gamma^{\frac{1}{2}}(\gamma-1)}{(1+\gamma^{1/2})(1+\gamma^{3/2})}\right] + \mathcal{O}\left[\left(\frac{\Delta E^v_{str}}{k_BT}\right)^2\right],$$

i.e., $\left(\mu_v/\mu_v^{(0)} - 1\right) \propto \eta \propto 1/L$, where $\mu_v^{(0)} = (e\bar{\tau}_{\rm v}/m^*_{\rm LH})(1+\gamma^{1/2})(1+\gamma^{3/2})$ is the valence band mobility for $\eta \to 0$, $1/\bar{\tau}_{\rm v} = (1/2)(1/\tau_{\rm LH} + 1/\tau_{\rm HH})$ (with $\tau_{\rm LH} \approx \tau_{\rm HH} \approx \bar{\tau}_{\rm v}$), $|\Delta E^v_{str}| \ll k_BT$ is assumed, the changes in the hole effective masses by strain have been neglected, $\tau_{\rm LH}$ and $\tau_{\rm HH}$ are the scattering times for light and heavy holes, respectively. It is clear that μ_v increases with $1/L$ for the tensile strain ($\Delta E^v_{str} < 0$) in the direction perpendicular to the interface of silicon and silicon-dioxide materials, as observed by us in Figure 9.

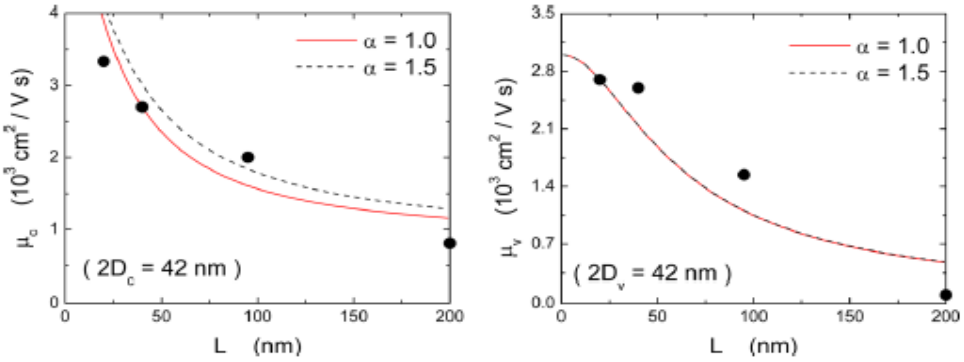

Figure 9. Theoretical modeling for electron (left panel) and hole (right panel) mobilities ias functions of wall thinckness L with α= 1.0 (red solid curves) and 1.5 (black dashed curves) and their comparisons with experimental data (black dots in both panels

d electron concentration n_c, the electron chemical potential u_c, which depends on both T and n_c, is decided from

$$n_c = \sum_{\xi=X,L} n_\xi = \frac{g_s}{V}\sum_{\xi=X,L} g_\xi \sum_k \left[1 + exp\left(\frac{E^\xi_k + E^\xi_G - u_c}{k_BT}\right)\right]^{-1}$$

$$\approx 2\sum_{\xi=X,L} g_\xi \left(\frac{m^*_\xi k_BT}{2\pi\hbar^2}\right)^{3/2} exp\left(\frac{u_c - E^\xi_G}{k_BT}\right) \quad ,$$

where the high-temperature approximation is made in the above expression, $E_{\rm G}^{\xi} = \varepsilon_{\rm G}^{\xi}(T) + \eta' \Delta E_{\rm G}^{\xi}$ is the bandgap energy of strained silicon crystals, which depends on T and the hydrostatic part of the strain, $\varepsilon_{\rm G}^{\xi}$ stands for the bandgap energy of unstrained silicon crystals, $g_{X,L} = 2$ (not 6 due to strain effect) represents the X (in <100> direction) and L (in <111> direction) valley degeneracy for electroncs at the two minima of conduction band, $E_{\rm G}^{\xi} = \hbar^2 k^2 / 2m_{\xi}^*$ is the kinetic energy of electrons and m_{ξ}^* is the transverse effective mass of conduction-band electrons with $m_X^* = 0.19 m_0$ and $m_L^* = 0.1 m_0$. The T dependence of $\varepsilon_{\rm G}^{\xi}(T)$ (based on the Bose-Einstein phonon model) is given by $\varepsilon_{\rm G}^{\xi}(T) = \varepsilon_{\rm G}^{\xi}(0) - 2\alpha_B \Theta_B [coth(\Theta_B/2T) - 1]$, where $\alpha_B = 2.82 \times 10^{-4}$ eV/K is a coupling constant, $k_B \Theta_B$ is a typical phonon energy with $\Theta_B = 351$ K, $\varepsilon_{\rm G}^{\rm X}(T) = 1.12$ eV and $\varepsilon_{\rm G}^{\rm L}(T) = 2.4$ eV at $T = 300$ K for the X and L valleys. Moreover, the strain part [2] of the bandgap energy $\Delta E_{\rm G}^{\xi}$ is calculated as $\Delta E_{\rm G}^{\xi} = \Xi_d^{(\xi)} Tr(\overleftrightarrow{\epsilon}) + \Xi_u^{(\xi)} \vec{e}_{\xi} \cdot \overleftrightarrow{\epsilon} \cdot \vec{e}_{\xi} + a Tr(\overleftrightarrow{\epsilon})$, where $\Xi_d^{(\rm X,L)}$ and $\Xi_u^{(\rm X,L)}$ are the deformation potentials of the conduction band for an indirect-gap silicon crystal ($\Xi_d^{(\rm X)} =$ 1.1 eV, $\Xi_u^{(\rm X)} = 10.5$ eV for the X valley and $\Xi_d^{(\rm L)} = -7.0$ eV, $\Xi_u^{(\rm L)} = 18.0$ eV for the L valley), $a = 2.1$ eV is the difference of the deformation potentials of conduction and valence bands at two different valleys due to hydrostatic component of the strain for the silicon crystal, and $\vec{e}_{\xi}$ is the unit vector pointing to the specific X or L valley. It is clear from the above equation that $\Delta E_{\rm G}^{\xi} < 0$ for the tensile strain and $\xi = X$ or L .

The change in the bandgap energy by strain also affects the effective mass of conduction band, given by [20] also see [21-33].

$$\Delta\left(\frac{m_0}{m_{\xi}^*}\right) \approx -\frac{E_P(2\epsilon_{\parallel}+\epsilon_{\perp})\eta'}{\varepsilon_{\rm G}^{\xi}(T)+\Delta_0/3}\left[2 + \frac{3a+3\Xi_d^{(\xi)}+\Xi_u^{(\xi)}}{\varepsilon_{\rm G}^{\xi}(T)+\Delta_0/3}\right] + \mathcal{O}[(2\epsilon_{\parallel}+\epsilon_{\perp})^2] ,$$

where we have neglected the shear strain and assumed a weak strain with $|2\epsilon_{\parallel} + \epsilon_{\perp}| \ll 1$, $\Delta_0 =$ 44 meV is the spin-orbit splitting and $E_P = 21.6$ eV is the Kane energy parameter.

The total mobility μ_c of conduction-band electrons is obtained as

$$\mu_c = \left(\frac{n_X}{n_c}\right)\frac{e\tau_X}{m_0}\left[\frac{m_0}{m_X^*} + \Delta\left(\frac{m_0}{m_X^*}\right)\right] + \left(\frac{n_L}{n_c}\right)\frac{e\tau_L}{m_0}\left[\frac{m_0}{m_L^*} + \Delta\left(\frac{m_0}{m_L^*}\right)\right] \approx \frac{e\tau_X^0}{m_0}\left[\frac{m_0}{m_X^*} + \Delta\left(\frac{m_0}{m_X^*}\right)\right]^{1+\alpha}$$

$$= \frac{e\tau_X^0}{m_X^*}\left\{1 + (1+\alpha)\left(\frac{m_X^*}{m_0}\right)\Delta\left(\frac{m_0}{m_X^*}\right) + \frac{\alpha}{2}(1+\alpha)\left(\frac{m_X^*}{m_0}\right)^2\left[\Delta\left(\frac{m_0}{m_X^*}\right)\right]^2 + \cdots\right\}$$

$$= \frac{e\tau_{\rm X}}{m_X^*} - \eta'(1+\alpha)\left(\frac{e\tau_{\rm X}}{m_0}\right)\frac{E_P(2\epsilon_{\parallel}+\epsilon_{\perp})}{\varepsilon_{\rm G}^{\rm X}(T)+\Delta_0/3}\left[2 + \frac{3a+3\Xi_d^{(X)}+\Xi_u^{(X)}}{\varepsilon_G^{\rm X}(T)+\Delta_0/3}\right] + \mathcal{O}[(2\epsilon_{\parallel}+\epsilon_{\perp})^2]$$

$$= \mu_c^{(0)}\left\{1 - \eta'(1+\alpha)\left(\frac{m_{\rm X}^*}{m_0}\right)\frac{E_P(2\epsilon_{\parallel}+\epsilon_{\perp})}{\varepsilon_{\rm G}^{\rm X}(T)+\Delta_0/3}\left[2 + \frac{3a+3\Xi_d^{(X)}+\Xi_u^{(X)}}{\varepsilon_G^{\rm X}(T)+\Delta_0/3}\right]\right\} + \mathcal{O}[(2\epsilon_{\parallel}+\epsilon_{\perp})^2] ,$$

i.e., $(\mu_c/\mu_c^0 - 1) \propto \eta' + \mathcal{O}(\eta'^2) \propto 1/L + \mathcal{O}(1/L^2)$ (using $\eta' \sim \eta$), where we assume $\tau_\xi = \tau_\xi^0 (m_0 m_\xi^*)^\alpha$ with α labelling the mass dependence in the scattering rate, $\mu_c^{(0)} \approx e\tau_X/m_X^*$ is the conduction-band mobility for $\eta' \to 0, \tau_{X,L}$ represents the scattering times of conduction-band electrons at two different valleys and the high-energy L valley has been assumed depopulated. It is clear that the electron mobility increases with $1/L^2$ in our system with $(2\epsilon_\parallel + \epsilon_\perp) = -0.08$, as observed by us in Figure 9.

4 RESULTS AND DISCUSSION

Table 1 and 2 below show the results of the theoretical calculations. As was previously shown in Figure 9, the comparisons between experiment and theory are within 10% which is a very good.

Table 1. Model parameters used in calculating mobility of electrons in strained Si WALL Structures.

μ_c^{max} ($cm^2/V \cdot s$)	$\mu_c^{(0)}$ ($cm^2/V \cdot s$)	λ_c (nm)	$2D_c$ (nm)
5500	806	15	42

Table 2. Model parameters used in calculating mobility of holes in strained Si wall structures.

μ_v^{max} ($cm^2/V \cdot s$)	$\mu_v^{(0)}$ ($cm^2/V \cdot s$)	λ_v (nm)	$2D_v$ (nm)
3000	100	143	42

As can be noticed from both the experiment and theory, the carrier concentration includes both the doping and photo-excitation contributions. If the sample is undoped, we can simply neglect the impurity scattering and have $n_c = n_v$. The optical-phonon scattering and the inter-valley scattering are only important at high temperatures, while the acoustic-phonon scattering becomes more significant at low temperatures. The surface-roughness scattering, on the other hand, is largely independent of temperature. In the narrowest wall devices, a considerable increase in conductivity was observed as a result of higher carrier mobilities due to lateral constriction. The strain effects, which include the reversal splitting of light- and heavy- hole bands as well as the decrease of conduction-band effective mass by reduced Si bandgap energy, are formulated in our microscopic model for explaining the experimentally observed enhancements in both conduction- and valence-band mobilities with reduced Si wall thickness. Specifically, the enhancements of the valence-band and conduction-band mobilities are found to be associated with different aspects of physical mechanisms. The role of the biaxial strain buffering depth is elucidated and its importance to the scaling relations of wall-thickness is reproduced theoretically, i.e., $1/L^2$ for electrons and $1/L$ for holes.

5 CONCLUSION

The semiconductor processing, fabrication and the resulting carrier transport characteristics of MSM devices fabricated as wall like structures in silicon on insulator technology were reported. MSM device dark current, DC photocurrents, and the time response of car-rier transport were investigated. The resulting conducting channels were actually smaller than their physical dimensions, a result of depletion of carrier near the interfaces. As the physical channel widths were reduced by oxidation, strain was produced near the interface and strained lattice became a significant portion of the conducting channel. The increase in mobilities for both holes and electrons stemming from the strained silicon resulted in a dramatic increase in carrier mobility for both electrons and holes as the physical channel width was reduced from 200 nm to 20 nm. The theoretical model incorporating the effects of strain present in these nanoscale MSM devices compared favorably with experimental results, showing that hole mobilities increased with decreasing L. Additionally, if these elec-tron and hole mobilities can be retained with the application of gate electrodes, then this technique may yield a much simpler path towards high performance CMOS, both n-channel and p-channel, than current techniques for either planer ultra-thin body FETs or FinFETs.

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LIST OF ACRONYMS

BOE	Buffered oxide etch
CMOS	Complementary Metal Oxide Semiconductor
DC	Direct current
FET	Field Effect Transistor
FinFET	Fin shaped Field Effect Transistor
FM	Fresnal Mirror
HH	Heavy hole
Ids	Dark current
IL	Interferometric Lithorgraphy
Ips	Photocurrent
ITRS	International Technology Roadmap for Semiconductors
LH	Light hole
MSM	Mobile Service Manager
MSM	Metal Si/nanowall Metal
nFET	n-type FET
pFET	p-type FET
Q_f	Fixed Charge
Q_{it}	Interface Trapped Charge
Q_{oT}	Oxide Trapped Charge
RIE	Reactive ion-etching
SEM	Scanning Electron Microscope

SGOI	SiGe on-insulator
SOI	Silicon-on-Insulator
sSOI	Strained Silicon-on-Insulator
VDD	Voltage Drain Supply
VLSI	Very Large Scal Integration

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