A Scalable Fabrication Process for Liquid Crystal-Based Uncooled Thermal Imagers

Shaun Berry, Carl Bozler, Robert Reich, Harry Clark Jr., Phillip Bos, Valerie Finnemeyer, Colin McGinty and Douglas Bryant

***Abstract*—A novel sensor is being developed for a new uncooled imager technology that is scalable to large formats (tens of megapixels) which is greater than what is achieved by commercial microbolometer arrays. In this novel sensor, a liquid-crystal transducer is used to change a long-wavelength infrared scene into a visible image that can be detected using a conventional visible imager. This approach has the potential for making a more flexible thermal sensor that can be optimized for a variety of applications. In this paper, we describe the microfabrication processes required to create an array of sealed, thermally isolated micro-cavities filled with liquid crystals to be used for an uncooled thermal imager. Experimental results from the fabricated arrays will also be discussed.**

***Index Terms*—Alignment layer, birefringence, liquid crystals, long-wavelength infrared, microbolometers, thermal imagers, uncooled thermal imagers.**

I. Introduction

Uncooled thermal detectors have become an indispensable sensor technology in long-wavelength infrared (LWIR) imaging applications. The devices have progressed to where the sensitivity and resolution are sufficient to replace cooled detectors in many applications [1, 2]. However, the state-of-the-art uncooled sensor technology, namely microbolometers based on thermistors, has progressed slowly over the past few years. Some of the challenges with these arrays include: difficulties in scaling to larger formats, increasing noise with decreasing pixel size, and high fabrication cost. A promising technology for thermal detection is liquid crystals. Liquid crystals are extremely sensitive to small changes in temperature [3] and, when configured as an IR-to-visible transducer, have the potential for efficiently converting an IR scene into visible image.

A novel sensor concept has been developed that separates the IR-to-optical conversion process [4-6] from the electronic readout. The decoupling simplifies the sensor architecture and enables independent optimization of the electronic readout. The transducer uses liquid crystals to detect small changes in temperature created by an infrared image. The small changes in temperature result in relatively large changes in the birefringence of the liquid crystals, which results in a variation in visible intensity when processed through other optical components. The visible light is then remotely detected by a solid-state imager which could be a charge-coupled device (CCD) or CMOS active pixel sensor (APS) that changes the signal into a usable digital electronic output. Greater detail about the transducer design and sensor concept can be found in [7].

Benefits of this approach include a simple and flexible sensor design with a scalable architecture for tens of megapixel formats and the potential for improved noise equivalent temperature difference (NETD) compared to what is achieved by commercial microbolometers. The liquid crystal transducer can be created with fewer than 10 photolithography steps, compared to perhaps greater than 40 photolithography steps for microbolometers that require a custom CMOS readout. This technology opens up applications where size, weight, and power (SWaP) constrained cooled thermal sensors, which can have megapixel formats, are not feasible. In addition, by decoupling the optical-to-electronic readout with a solid-state imager, it enables capabilities like; time delay and integrate, plus jitter compensation for example.

We have previously demonstrated that liquid crystals have the required performance (sensitivity, dynamic range, speed, etc.) to make state-of-the-art uncooled imagers [7]. This paper focuses on the fabrication processes required to create thermally isolated liquid crystal pixels (transducers) with scalability to large array formats (tens of megapixels). We have developed several novel fabrication techniques that include an *in-situ* alignment layer method compatible with CMOS microfabrication, and methods to fill and seal small cavities with liquid crystals. The fabrication processes described can also be used for other liquid crystal, cavity-based, photonic devices.

II. Liquid crystal transducer design

The liquid-crystal transducer described herein is a proof-of-concept design and some of the constraints such as fill factor, are relaxed for easier fabrication. In addition, the thermal legs

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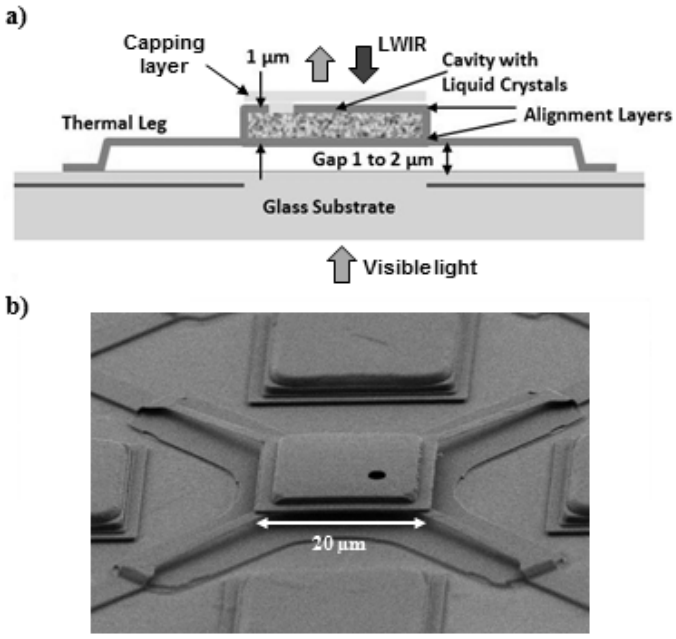

Fig. 1. Liquid-crystal transducer design. a) Cross section of transducer. b) SEM image of thermal imager transducer released from the substrate but not filled with liquid crystals or sealed.

have not been optimized for maximum thermal resistance.

The liquid-crystal transducer concept is shown in Fig. 1. The transducer consists of a liquid crystal cavity that is 20 µm × 20 µm × 1 µm, which is elevated approximately 1 µm above a transparent substrate by four silicon nitride legs (2 µm wide × 300 nm thick). The nitride legs provide the thermal isolation for the transducer. The top surface of the cavity is also a 300-nm-thick nitride layer. The transducers are arrayed forming a sensor.

Details of the sensor operation can be found in [7], but are briefly described here to provide the reader context. As shown in Fig. 1a, a LWIR image is focused onto the liquid-crystal transducer array. This creates a temperature change in the liquid crystals proportional to the thermal resistance of the leg structure. The temperature change induces a relatively large change the liquid crystals birefringence [3] which results in a measureable variation in intensity. This pixel birefringence change is sensed by polarized visible light passing through the transducer as shown in Fig. 1a. This completes the IR-to-visible conversion. To create an electronic image, the visible light then passes through a second polarizer and is focused onto a CCD or CMOS imager that forms a visible intensity image. The electronic image is readout from the solid state imager.

III. Microfabrication

The liquid-crystal transducer is fabricated on a monolithic substrate. The microfabrication is divided in two major process flows. Wafer-scale fabrication, in which large arrays of the transducer design are created using standard CMOS planar-microfabrication techniques, and die-level fabrication where processes such as the liquid crystal cavity fill and pixel releasing from the substrate are performed.

A. Wafer-scale Processing

Transducers arrays as large as 256 × 256 incorporating a die area of 25 mm × 25 mm were stepped-out over a 200-mm fused silica wafer. Figure 2 highlights the major wafer-scale fabrication steps. First, 200 nm of aluminum was deposited to form a light blocking layer. Openings in the blocking layer were created by a dry-etch process to pass visible light where the liquid crystal cavities will be located. A 1-µm thick PECVD silicon dioxide layer was then deposited and planarized by a chemical mechanical polish (CMP) to a thickness of 500nm (Fig. 2a).

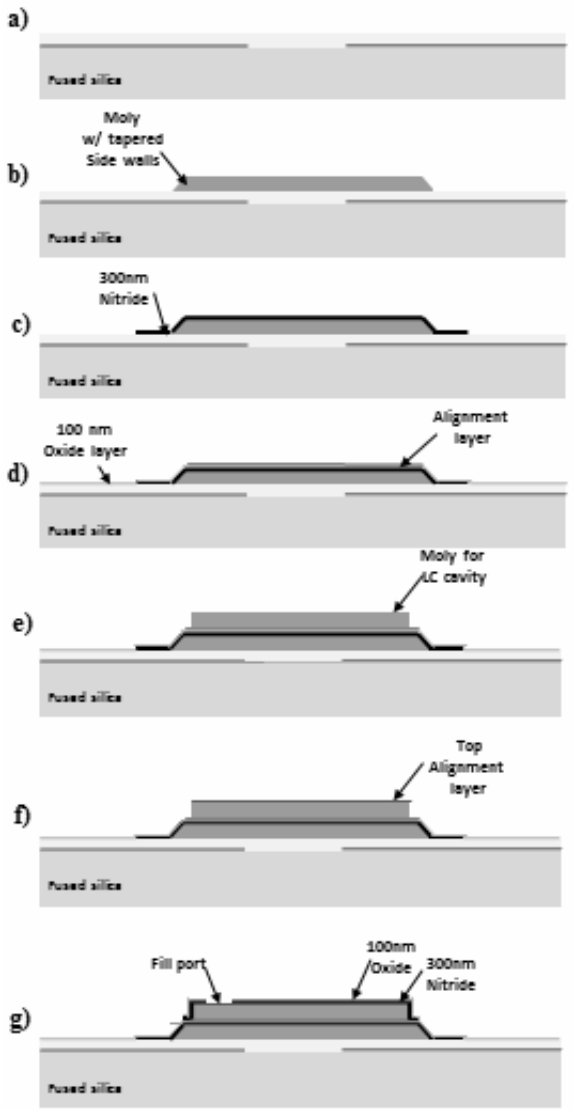

Fig. 2. Major wafer-scale fabrication processing steps on a 200-mm fused silica wafer. a) 200 nm thick aluminum blocking layer added. b) 1 µm of sacrificial molybdenum is deposited to form bottom support. c) 300 nm of silicon nitride (Si_3N_4) deposited to form the thermal legs and cavity bottom. d) Protective SiO_2 layer deposited and 1st alignment layer added. e) 1 µm of molybdenum deposited and the liquid crystal cavity formed. f) 2nd alignment layer added. g) 300 nm of Si_3N_4 added to form capping layer of liquid crystal cavity with a 2-µm diameter fill port added as the last processing step.

Next, a 1-µm thick molybdenum sacrificial layer was deposited over the oxide and dry-etched to form the bottom support for the cavity and thermal legs (Fig 2b). Once the

bottom sacrificial molybdenum has been etched, a 300-nm-thick PECVD silicon nitride layer was deposited and dry-etched with reactive ion etching (RIE) to form the thermal legs and the bottom of the liquid crystal cavity (Fig 2c). Next 100 nm of PECVD oxide was deposited to act as a protective layer for the bottom molybdenum and silicon nitride. The oxide was then diamond lapped using a 500 nm diamond grit lapping film creating the first alignment layer (Fig. 2d). Details about the alignment layer process are discussed in the Alignment Layer Development section. A second 1-µm thick molybdenum sacrificial layer was deposited and buffed smooth with CMP prior to the second alignment layer being added. After the molybdenum was buffed, it was dry-etched to define the cavity interior (Fig 2e). A second diamond lapping was done on the patterned molybdenum to create the top alignment layer in the cavity (Fig 2f). Finally, a 300-nm thick silicon nitride layer was then deposited and dry-etched to form the top surface and sides of the cavity. During this etch a 2-µm diameter hole for filling the cavity with liquid crystals was also created in the silicon nitride on top of the cavity (Fig 2g). The alignment layer grooves made in the top cavity molybdenum were transferred to the silicon nitride layer during the deposition. Figure 3, shows a full 200-mm wafer after the wafer-scale fabrication and Fig. 4 shows the thermal imager transducer pixel after wafer-scale fabrication is completed. The wafer-scale fabrication process required only 5 photolithographic steps to create the transducer.

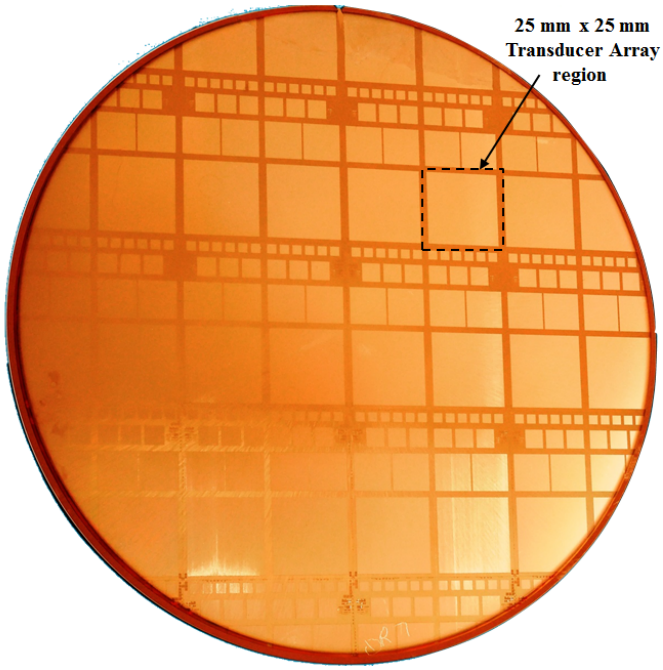

Fig. 3. 200-mm fused silica wafer after wafer-scale fabrication. The wafer contains 16, 25 mm × 25 mm full die containing arrays of 256 × 256 transducer pixels.

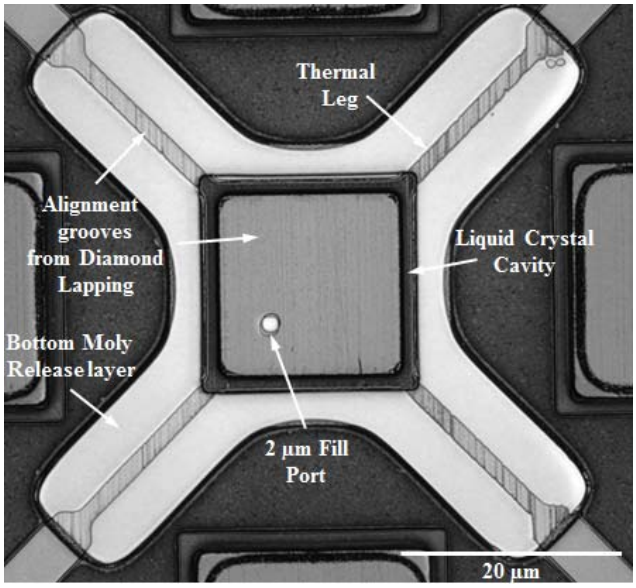

Fig. 4. Top-down microscope image of a single thermal imager transducer pixel after wafer-scale fabrication. The image clearly shows alignment layer grooves from the diamond lapping on the thermal legs and cavity.

B. Alignment Layer Development

To be useful for sensitive temperature measurements required in a thermal imager, the liquid crystals must have a determined alignment. This requires an alignment layer that seeds the orientation of the liquid crystal molecules. The alignment layer has an anchoring energy which determines how much energy is required to change the orientation of the surface contacting liquid crystal director. Several alignment methods have been considered such as rubbed polyimide [8], ionic milling [9], lapped inorganics [10], glancing angle deposition [11], and photo-alignment [12]. Most displays use polyimide alignment layers [8] that are coated and mechanically rubbed to elongate the polymer chains to create an anisotropic van der Waals interaction that aligns the liquid crystal director with a relatively large anchoring energy. In practice, the polyimide is deposited on two relatively large flat glass pieces and then the pieces are brought together within a few microns, the gap being set by glass ball spacers. In the thermal imager application where isolated cavities with lateral dimensions on the order of microns are desired, it was found that the polyimide alignment technique was not compatible with the down-stream microfabrication steps (e.g. solvent cleaning and high temperature processes). Therefore, an alternative alignment technique had to be developed.

To provide alignment for cavity-based liquid crystal devices a mechanical diamond lapping process was developed that was compatible with CMOS microfabrication. Figure 5 shows photographs of the jig specially fabricated for this process. This was an *in-situ,* wafer-scale process where surfaces were lapped using 500-nm grit diamond lapping film from 3M (668X Diamond Lapping Film PSA) to create parallel "troughs" with dimension of several nanometers in height and width on the surface.

A 200-mm wafer was held in place on a lapping jig and was submerged in deionized (DI) water (Fig. 5a). Since the

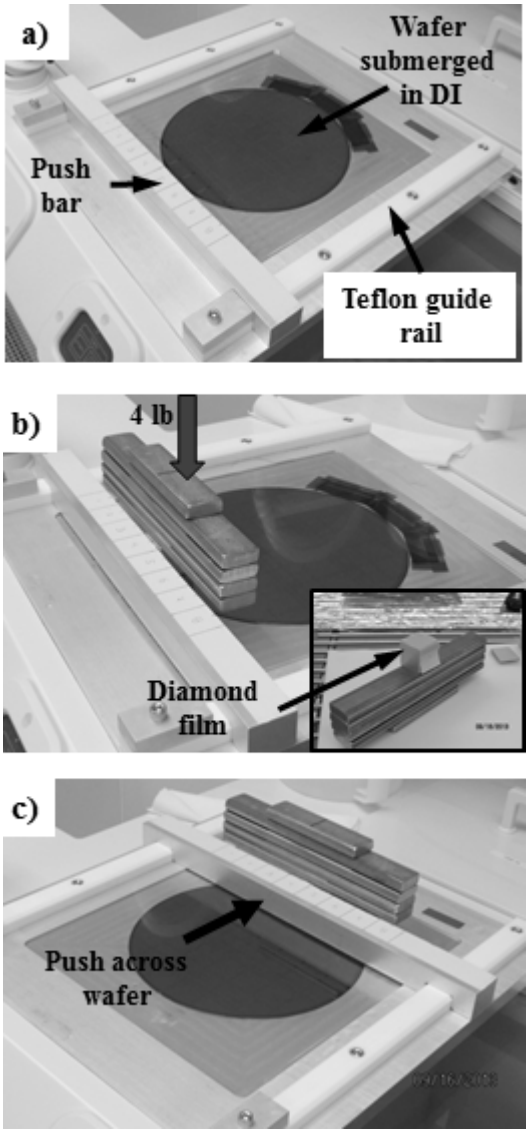

Fig. 5. Alignment lapping jig for mechanical diamond lapping process. a) 200-mm wafer held in jig, submerged in DI. b) 500-nm grit diamond lapping film mounted to 25mm sq. block (insert). Film positioned on wafer and stainless bars added to provide weigh. C) Using the push bar, the film is pushed (rubbed) across the wafer in a constant motion. The process is repeated several times to create parallel grooves on the wafer surface.

transducer array die size was 25 mm, the diamond lapping film was cut to that size and attached to a 25 mm × 25 mm square aluminum block. The block with the film attached was aligned to the die features on the wafer with appropriate weight added (Fig. 5b). We used stainless steel bars to apply the weight to the block. Two different loads were evaluated, 2lb and 4lb. This equates to approximately 2 psi or 4 psi of pressure, respectively. The weight(s) and grit was found to be adequate to form grooves on the nanometer scale for hard materials like silicon dioxide. The film with weight added was then pushed (rubbed) across the wafer with a constant motion over a 25 mm wide strip (Fig. 5c). The jig had guide rails which allowed for a push-bar to slide the weight repeatedly in the same direction and over the same location on the wafer. Multiple rub passes were made per-25 mm wide locations. This process was stepped and repeated over the wafer. A new diamond lapping film was applied for each new wafer location. After the entire wafer was diamond lapped it was rinsed with DI, followed by a quick-dump rinse. To remove the finer lapping debris, a megasonic clean with DI was performed.

For the transducer design, the first alignment layer (bottom layer) was done on the silicon dioxide film after the fabrication step shown in Fig. 2d. The second alignment layer (top layer) was done on the top cavity molybdenum film after the fabrication step shown in Fig. 2e. The top and bottom alignment layers were lapped parallel for these devices. This process also can be used for perpendicular alignment as well. Figure 6 shows an atomic force microscope (AFM) scan image of the first alignment layer after diamond lapping on the silicon dioxide film. The lapping condition was: 4 rub passes using a weight of 4lb. A 5µm × 5µm. The AFM scan was taken at the center of a transducer pixel. As the image shows, there are distinct, parallel grooves in the oxide. The typical roughness was found to be ~2nm RMS and the maximum peak-to-peak height ~±7 nm. AFM scans were also made after the second alignment layer was created on the molybdenum and similar results were obtained, both in the pitch and depth of the grooves formed, as was seen with the first alignment layer.

The azimuthal anchoring energy of the diamond lapped substrates was also measured. In order to perform this measurement, 90° twist cells (on the order of inches) were fabricated from fused silica substrates coated with silicon dioxide or silicon nitride that were diamond lapped using the same conditions that were used for

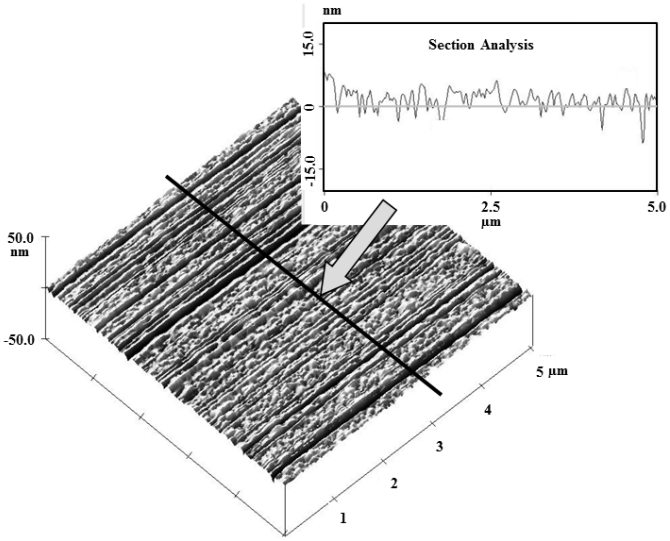

Fig. 6. AFM scan after diamond lapping of the silicon dioxide film using 500nm grit diamond lapping film and a weight of 4lb and 4 rub passes.

the thermal pixel transducer. The twist of the liquid crystal director throughout both of these cell types was measured to determine the energy [13]. The azimuthal anchoring energy of the silicon dioxide coated substrates was measured to be between $0.78 - 1.3 \times 10^{-5}$ J/m^2. The anchoring energy of the silicon nitride coated substrates was measured to be between $2.4 - 5.9 \times 10^{-6}$ J/m^2. The Berreman model of a nematic liquid crystal at a grooved interface predicts that the azimuthal

anchoring energy depends on the amplitude and period of the grooves as well as the elastic constants of the liquid crystal [10]. The pitch of the grooves was determined to be ~100 nm and the amplitude was determined to be ~3.5 nm from the AFM scans of the lapped substrates. Based on this, the Berreman model predicts an azimuthal anchoring strength of ~$4x10^{-6}$ J/m^2 which agrees nicely with the results for the silicon nitride coated substrates. These surfaces exhibit much weaker anchoring energy than that of rubbed polyimide which has been reported to be as high as 10^{-4} J/m^2 [14]. Measured results done on the thermal pixels verified that the diamond lapping was sufficient for the parallel alignment of the liquid crystals.

Even though we developed the diamond lapping alignment process to support the proof-of-concept transducer design, we also have been working on a photoalignment alignment technique that will be more VLSI-compatible. Our recent work with photoalignment for cavity-based liquid crystal photonic devices can be found in [15].

C. Die-level Processing

After the wafer-scale processing was completed the wafer was diced into 25 mm × 25 mm die containing transducer arrays. The die-level processes described here could have been performed at the wafer-scale however we chose to process at the die-level to maximize the number devices we had to work with in order to develop several of the challenging fabrication steps, such as liquid crystal filling, sealing the liquid crystals in the cavities and releasing the transducer cavity from the substrate.

a) Liquid Crystal Fill Process

The first step was to remove the top molybdenum sacrificial layer inside the cavity. The top molybdenum was etched in hydrogen peroxide at 40°C for 45 min. A long etch time is required as a result of the diffusion time associated with completely removing molybdenum in a 20-µm square, 1-µm high cavity through only a 2-µm diameter port in the cavity. During this step the bottom molybdenum is protected by the 100-nm thick silicon dioxide layer that was added after the first silicon nitride film was deposited. At this step, it is critical that the bottom molybdenum is not etched. A layer of photoresist is patterned to expose the cavity fill hole. Figure 7 shows the time progressions of the top molybdenum etch.

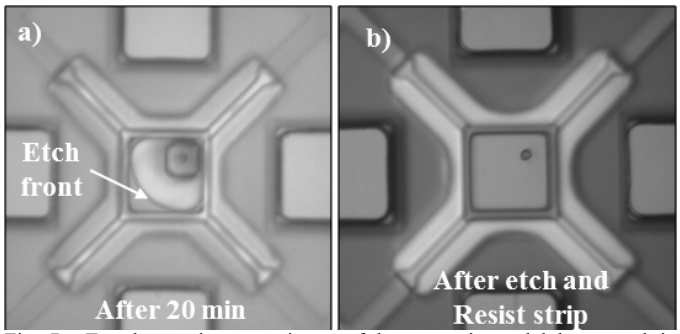

Fig. 7. Top-down microscope image of the top cavity molybdenum etch in hydrogen peroxide. a) Etch after 20 min. molybdenum not completely removed from the cavity. b) After 45 min in hydrogen peroxide molybdenum is completely removed from the cavity.

Once the molybdenum had been etched from the cavities and the protective resist removed, the cavities were filled with liquid crystals. A commercial nematic liquid crystal, 4′-pentyl-4-biphenylcarbonitrile (5CB) was used which has an isotropic transition temperature at 35°C and birefringence of ~0.17. It should be noted that any nematic liquid crystal can be used; but higher birefringence results in better temperature sensitivity. To help ensure good alignment and minimize defects, the liquid crystals were filled at a temperature above the isotropic transition temperature.

Prior to filling, the die and liquid crystals were placed on a hot plate at 50°C. Once the liquid crystals changed to the isotropic phase, a small amount was poured over the die. The liquid crystals wet the silicon nitride surface and spontaneously wick through the 2-µm diameter hole into the cavity. Next, as much of the bulk liquid crystal on top of the die surface was removed by placing the die face down on a silicon wafer and sliding the two surfaces across each other. This leaves behind most of the liquid crystal on the wafer. The remaining thin film of liquid crystal on the die surface was removed by gently rinsing under DI water for 30 s. If this rinse was done to aggressively the liquid crystal in the cavity would be washed out.

We have perfected the overall filling process and typically achieve >90% of the transducers filled over the entire die. Figure 8 shows microscope images of the thermal imager transducer pixel after the liquid crystal fill as viewed between linear polarizers. As can be seen from the image in Fig. 8, the liquid crystals have filled the cavities entirely and the alignment looks good, since there are no Schlieren patterns, which would be caused by the polarized light being distorted by liquid crystal defects.

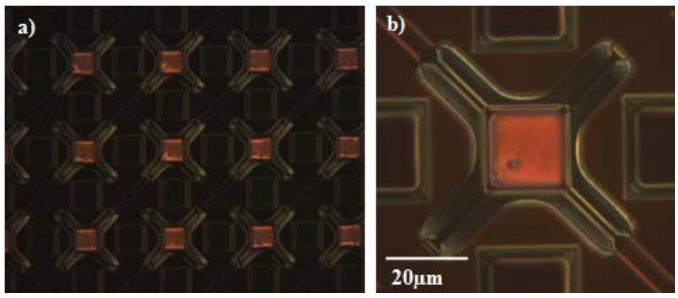

Fig. 8. Top-down microscope image of the transducers viewed between linear polarized light after liquid crystal fill. a) Array of transducers. b) Single transducer pixel. Note the good alignment of the liquid crystals in the cavity as noted by the absence of any liquid crystal defects.

b) Sealing the Cavity

After the liquid crystals are filled, the next step was sealing the fill port on the cavity. The challenge was finding a suitable material that not only was immiscible with liquid crystals but robust enough to survive additional microfabrication processes.

Liquid crystals are soluble in most solvents and our initial attempts of using photoresists, and epoxies, including SU-8 and even PDMS, all of which contain numerous solvents, for the fill port sealing layer did not work. The liquid crystals would immediately be dissolved out of the cavities when

brought into contact with any of these materials. Liquid crystals, however, were immiscible and did not dissolve in perfluorinated hydrocarbons, (e.g. FC-40 (3M) and CT-SOLV180 from Asahi Glass). The cavity sealing material was CYTOP CLT-809M (Asahi Glass) which is an amorphous fluorocarbon that is suspended at 9% by weight in a perfluorinated solvent.

The 9% CYTOP was spun on the liquid crystal filled die, at 1000 RPM for 30 s. For these conditions, all the cavities were filled on most die. Typically, CYTOP needs to be cured at temperatures >120°C in order to form a robust adhesion to the surface. Unfortunately, the curing at high temperatures caused the liquid crystals in the cavity to expand out of the fill port before the CYTOP film could solidify. After spinning CYTOP, the die was placed on a hot plate at 105°C for 30 min which hardened the CYTOP enough to form a robust seal over the fill port. At these process conditions a 1.5-µm thick CYTOP film is achieved. In future designs, smaller fill ports can be used, which will enable a thinner sealing film to also be used.

Once the CYTOP film was cured, 100 nm of aluminum was electron beam evaporated over the die surface and patterned and wet-etched to form a square about the size of the liquid crystal pixel cavity (20 µm × 20 µm). The aluminum served two purposes, to act as a hard mask for the CYTOP etch and to be used a barrier to protect the liquid crystals during the long oxygen plasma etch of the CYTOP. The CYTOP was etched by oxygen plasma using a Gasonics 9102 plasma asher. The RF power was 300 W and O_2 flow rate was 600 sccm. The etch time to clear the CYTOP from thermal legs and bottom molybdenum was ~60min. To avoid over heating of the die (goal to keep <105°C), the etch was broken into six, 10 min etch steps and the die was cooled between etch steps. After the CYTOP was cleared from the thermal legs and bottom molybdenum, the aluminum hard mask was removed by a wet etch process. A 1.5-µm CYTOP plug was left on top of the transducer cavity.

c) Releasing the Transducer from the Substrate

The last fabrication step was releasing the transducer pixel from the substrate. Several different techniques were evaluated including using a critical point dryer, which is often used in MEMS fabrication [16] and various plasma dry-etch techniques. Unfortunately, these techniques did not yield a high number of elevated pixels. The CO_2 used in the critical point dryer caused the CYTOP to plasticize and the liquid crystals were dissolved out of the cavities. Plasma dry-etch processes, like RIE and ion-milling created a charge on the cavity surface which attracted the cavity toward the substrate, pinning it, once the bottom molybdenum was removed. The technique that worked the best was to use xenon difluoride (XeF_2) to etch the bottom molybdenum. XeF_2 is used as an etchant gas for a plasmaless dry-etch technique for silicon [17]. In recent years, XeF_2 has been used to etch other semiconductors and metals, including molybdenum, used in MEMS device fabrication [18].

Once the CYTOP plug is formed, the 100-nm thick protective oxide over the thermal legs and bottom molybdenum is removed. For this step, the CYTOP plug on top of the cavity acts as a mask, protecting the pixel cavity. The oxide is removed by an RIE process using CF_4 etchant. The selectivity between the oxide and silicon nitride is nearly 1:1 for this etch chemistry, thus the oxide etch is timed so that the oxide just clears over the nitride legs. After the RIE of the oxide, a 10-min argon sputter etch is done to remove any residual oxide as well as to remove the thin molybdenum oxide layer that has formed. If there is any oxide remaining over the molybdenum, especially molybdenum-oxide, it will not etch in the XeF_2. After the argon sputter etch, the XeF_2 etch of molybdenum is done in an isotropic etcher, SE Tech ES-2000XM. The XeF_2 is pulsed for 60 s then off for 60 s a total of 5 times. This time was enough to remove the bottom molybdenum, including under the transducer pixel cavity. Figure 9 shows a microscope image using backlighting of an array of liquid-crystal transducer pixels after the bottom molybdenum has been etched in XeF_2. The light passing through the opening for the pixels indicates the bottom molybdenum has been completely etched.

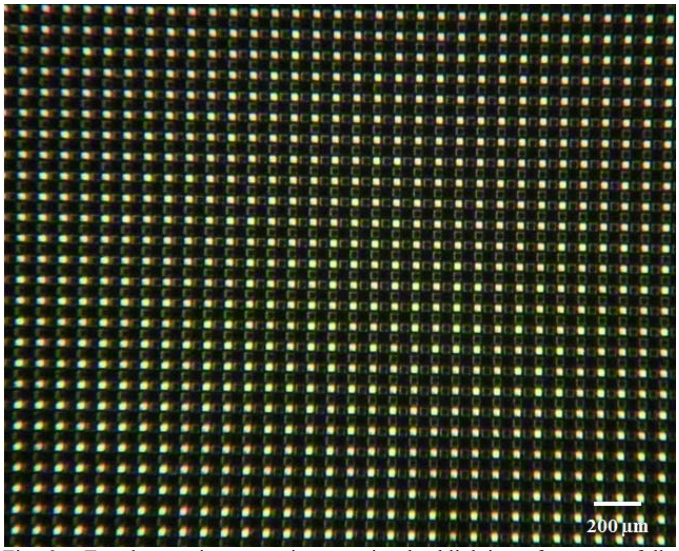

Fig. 9. Top-down microscope image using backlighting of an array fully processed, elevated thermal transducer pixels after the bottom molybdenum has been etched in XeF_2. Bright areas indicate the bottom molybdenum has been completely etched from underneath the pixel cavities.

Figure 10, shows a top-down microscope image of single transducer after the XeF_2 etch, elevated off the substrate and filled with liquid crystal, viewed between cross polarizers.

The critical individual process steps have shown good transducer cavity yield (>90%). The final devices through fabrication have shown thousands of pixels working. Future work would be to refine the fabrication steps and improve uniformity.

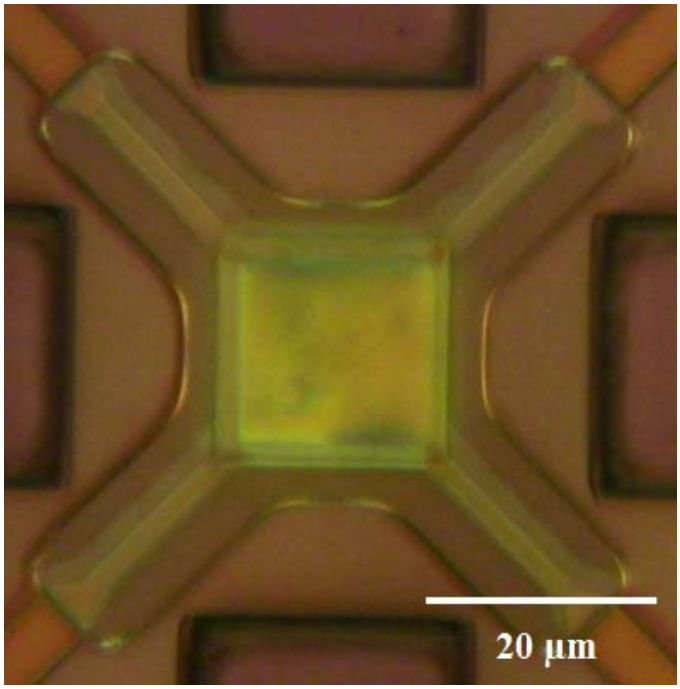

Fig. 10. Top-down microscope image of the fully processed, elevated thermal transducer pixel after the bottom molybdenum has been etched in XeF_2,viewed between cross polarizers.

IV. Measurement Results

The breadboard-camera test setup used to measure the performance of the fabricated transducer arrays is shown in Fig. 11. A dewar is used to keep the thermal imager transducer array under vacuum (< few mtorr) and is needed to reduce the conduction through air to the surroundings. A blackbody source (SR 20) or an IR collimated emitter (EK8520) is used to generate LWIR light. The LWIR light passes through an 8- to 12-µm filter. It is then focused by a ZnSe lens (~f/3) and reflected by a dichroic optic into the dewar and onto the liquid-crystal transducer array. As determined through measurements of individual layers and modeling, the average LWIR absorption is about 40% in the thermal pixel for the 8- to 12-µm band. The Senarmont method [19] is used to detect the liquid crystal birefringence change due to heating of the thermal pixel by the LWIR. The visible light source is an LED with a wavelength selected somewhere in the visible to

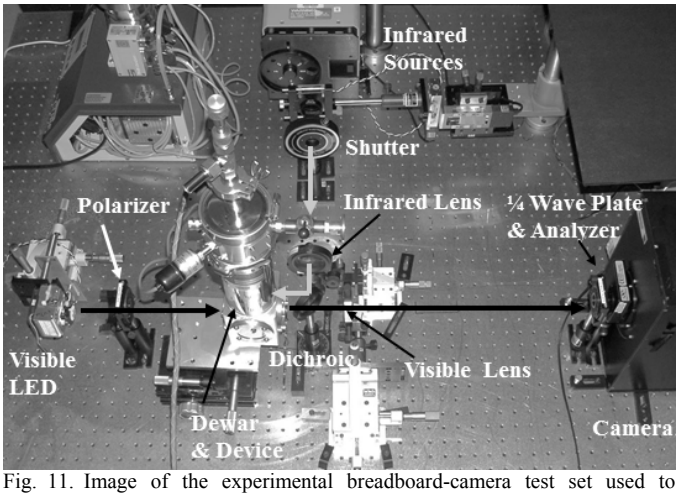

Fig. 11. Image of the experimental breadboard-camera test set used to evaluate liquid-crystal thermal imager transducer arrays.

optimize the signal and to match the quarter wave plate of the Senarmont system. The light bandwidth is reduced to about 10 nm by a filter and linearly polarized. The polarized light is transmitted through the liquid crystal device in the dewar. After passing through the dichroic, the visible light is focused onto the CCD imager in the camera. In front of the camera is a quarter wave plate and analyzer. The quarter wave plate changes elliptically polarized light back to linear. The analyzer is used to evaluate the visible light signal versus polarization angle.

Using the f/3 lens and a binned 5 × 5 array of transducer pixels (equivalent pixel size of 100 µm × 100 µm), a temperature change of a few degrees has been sensed in the transmission mode. This is in the range of sensitivity expected based on the thermal resistance of the legs and absorption of infrared light. The temperature sensitivity is expected to be in the tens of mK range with the integration of higher resistance legs and addition of a good LWIR absorber. All the temperature sensitivity results were taken with the operating parameters of a thermal pixel integration time: tens of milliseconds, lens f/# of: f/3, wavelength range of 8 µm to 14 µm, pixel area of 100 µm × 100 µm. An example of the temperature response is shown in Fig. 12. Each measured point is a two-frame average taken about every 0.5 s (frame grabber acquisition time). The average background was subtracted by closing the shutter in front of the IR source and accumulating 10 image frames before collecting the data in the plot. A temperature change of 9°C is clearly discernable in Fig. 12 between the shutter open and closed conditions. The response time and dynamic range of the liquid crystals has been measured on other test structures and is compatible with video rate operation (~10 ms response and 12-bit dynamic range).

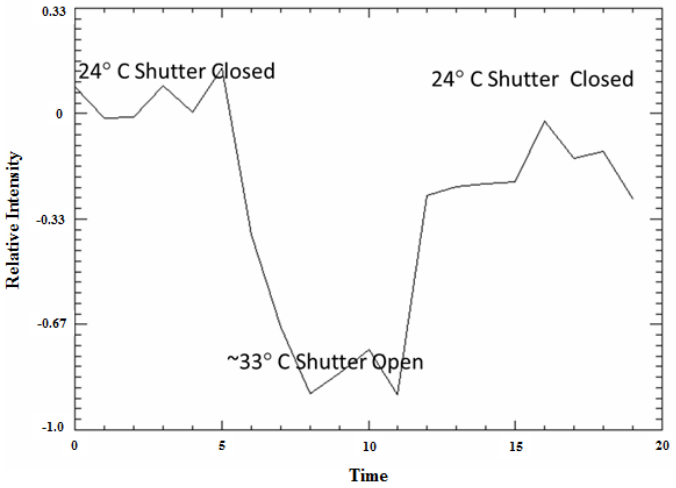

Fig. 12. Temperature response from opening and closing a shutter in front of IR source of a 5 × 5 thermal pixel transducer array (equivalent pixel size 100 µm × 100 µm).

Finally, a visible image was collected demonstrating the IR-to-visible thermal imager concept. Figure 13 shows the converted visible image of the IR collimated emitter. To create the image, the IR emitter source is stepped in 100 µm increments spatially in a raster scan. The active liquid crystal pixel size is 20 µm and is imaged on to an approximately 4 × 4-pixel region in the CCD image array of the camera. The temperature of the coil is approximately 950 °C. For each position, the intensity from the background temperature is subtracted from the source intensity using a shutter that is located in front of the coil.

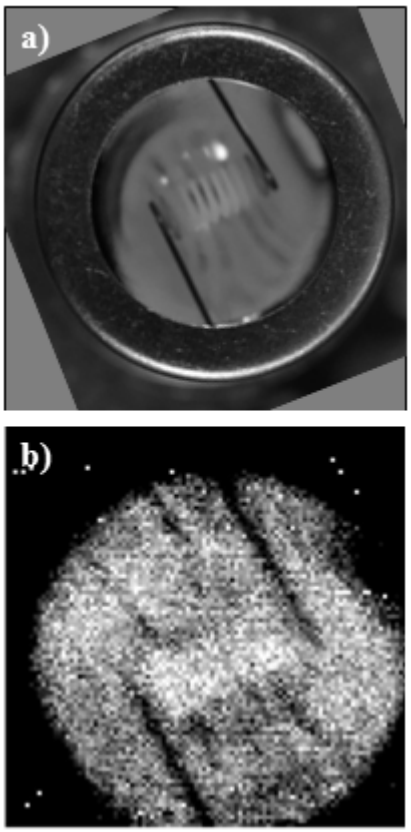

Fig. 13. Infrared-to-visible image of a hot IR emitter captured from the liquid crystal thermal imager breadboard camera setup. a) Actual visible image of the heated coil. b) Infrared-to-visible image from scanning a single liquid crystal pixel on the transducer array.

V. Conclusions

In this paper we have presented a fabrication process to create thermally isolated liquid crystal pixels (transducers) to be used in a novel uncooled thermal imager. We developed several novel fabrication techniques, such as an *in-situ* alignment layer method compatible with CMOS microfabrication, plus methods to fill and seal small cavities with liquid crystal. Arrays have been fabricated that demonstrate that the liquid crystals can be integrated into a MEMS pixel structure while retaining sensitivity and other performance characteristics comparable to the bulk liquid crystals. The fabrication process developed is scalable to large array formats (tens of megapixels).

Future work will include fabricating high-fill-factor devices with larger array formats. The MEMS isolation structure will be designed to increase the thermal resistance for better sensitivity. A better absorber will be integrated into the pixel that is resonant in the LWIR while passing the visible light.

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