Scalable Testing Platform for CMOS Read-In Integrated Circuits

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Abstract: *The read-in integrated circuit (RIIC) is an integrated circuit that drives an array of infrared emitters inside of an infrared scene projector (IRSP) system. We have designed different RIICs for four future IRSP systems that are being built by our research group. This paper describes a single scalable testing platform (STP) capable of testing all of our RIICs. This approach reduces the design time and risk associated with RIIC testing. On the hardware side, our platform consists of several custom printed circuit boards. On the software side, our platform consists of a single code base.*

Keywords: RIIC; IRSP; Wafer Testing; Scalable System; CMOS; infrared: scene; projector;

Introduction

The read-in integrated circuit (RIIC) drives an array of infrared emitters inside of an infrared scene projector (IRSP) system. We have designed different RIICs for four future IRSP systems that are being built by our research group [1, 2]. This paper describes a single scalable testing platform capable of testing all of our RIICs. The hardware that has been designed consists of several custom printed circuit boards (PCB) that have specific functionality and can be modified to add additional features. Figure 1 shows the typical testing setup including the direction of communication between all of the test system components.

The test system is controlled by Python software. The computer communicates the control signals necessary to operate the RIIC over a serial line with an Arduino microcontroller. The Arduino microcontroller then formats the control signals from the computer into the appropriate RIIC commands and transmits the control signals over a serial-peripheral-interface (SPI) to the bare RIIC testing board (BRT). The BRT is a custom board that attaches to the Arduino and routes the signals to the correct pins on the test RIIC and delivers power to the test RIIC. The critical feature of the BRT board is a zero insertion force (ZIF) DIP socket that sits in the middle, which allows us to modify where the control signals are routed. The BRT connects to another PCB, the adapter board, which is a simple interface that changes the connector type to connect another one of our boards, the modular RIIC testing platform (MRTP). The MRTP board is used to test the RIIC in its pin grid array (PGA) package because it has a PGA socket that breaks out all of the necessary RIIC signals. This allows the control signals from the computer to be routed through the system and to the RIIC. The MRTP also has the ability to run up to four RIICs simultaneously allowing us to simulate a bigger system and test that RIICs work in harmony with each other. Another feature of the MRTP is that it can communicate directly to the Arduino bypassing the BRT. The purpose of this is to have the ability to do quick simple tests of the RIIC. Finally, we use two programmable Keithley source meters. One is programmed to do voltage sweeps of the pixel circuits in the RIIC (7 in Figure 1), and the other Keithley measures the output super-lattice-light-emitting-diode (SLED) current on a monitor out (MOUT) pin. The MOUT pin can produce voltage or current readings, depending on the test case. The measured data is sent to the computer (8 in Figure 1). Figure 2 illustrates the RIIC wafer testing setup. When running tests on wafers we replace the MRTP with a probe card specially made to match the bond pads on the wafers. Everything else remains the same including the software that runs the system.

Testing phases

The testing procedure for a RIIC occurs in two phases. The first phase is a development phase. All the tests that the RIIC will be subject to on the next phase are developed in the first phase using a 16x16 RIIC in a PGA package. The first phase is also the time to find possible flaws in the circuit design of the RIIC. If a design flaw is found it gets fixed prior to fabricating the real full size RIIC on a wafer. Phase two of testing is when several full sized RIICs are fabricated on an eight-inch wafer. Then all of the tests prepared in phase one are run on the full size RIICs in a clean room facility. The second phase is more of a selection process where all the best performing RIICs are chosen for hybridization, a process in which the optical emitters are mated with the RIIC using flip chip bonding or post-foundry growth processes [3].

Scalability

When designing a system dedicated to testing a component that will evolve rapidly such as the RIICs, it is very important to keep in mind that such system must be able to handle all the possible changes with minimum or no change to the architecture. So far there has been four different versions of the SLED RIICs that have been subject to testing using this system. These versions include the two color SLEDs array (TCSA) version one and version two, night-glow SLED (NSLED) and currently the high definition infrared LED (HDILED). Because all RIICs have small

differences in the signals required to operate, place holders were incorporated into the design of the hardware, and software. On the hardware side, the place holders are located on the BRT board, this board has extra pins that can be easily open or closed using jumpers. In addition, custom boards can be created to add, remove, or change signals depending on the situation. This method has proven to be very effective during wafer testing because it is very difficult to create a custom probe card that will accurately probe a 512x512 RIIC. Instead, the RIIC is probed in quadrants where the probe card only needs to contact a quarter of the pads. Furthermore, the contact points were place around the corners of the RIIC facilitating the alignment process. For each quadrant a custom signal routing PCB was created. This board plugs into the PGA socket located in the center or the BRT board. Whenever a different quadrant is probed the matching signal routing board is inserted into the socket.

In a similar way, the software architecture is also designed to have place holders in anticipation of the addition or removal of features on future RIIC designs. When a user wants to program the RIIC, all the data is put into a packet of a fixed format. This packet contains information about the version of the RIIC to be tested, header fields that hold different commands to be performed by the receiving end, and finally a payload that gets written to the memory in the RIIC using SPI. The SPI circuitry in all the RIICs is the same, thus it does not require place holders in the software. The expandable fields are part of the header of the packet as some versions of RIICs require input signals to be programmed differently than others. When a new field is needed it replaces an empty slot on the header, then it gets programmed on the python code running on the computer, and the code on the Arduino microcontroller.

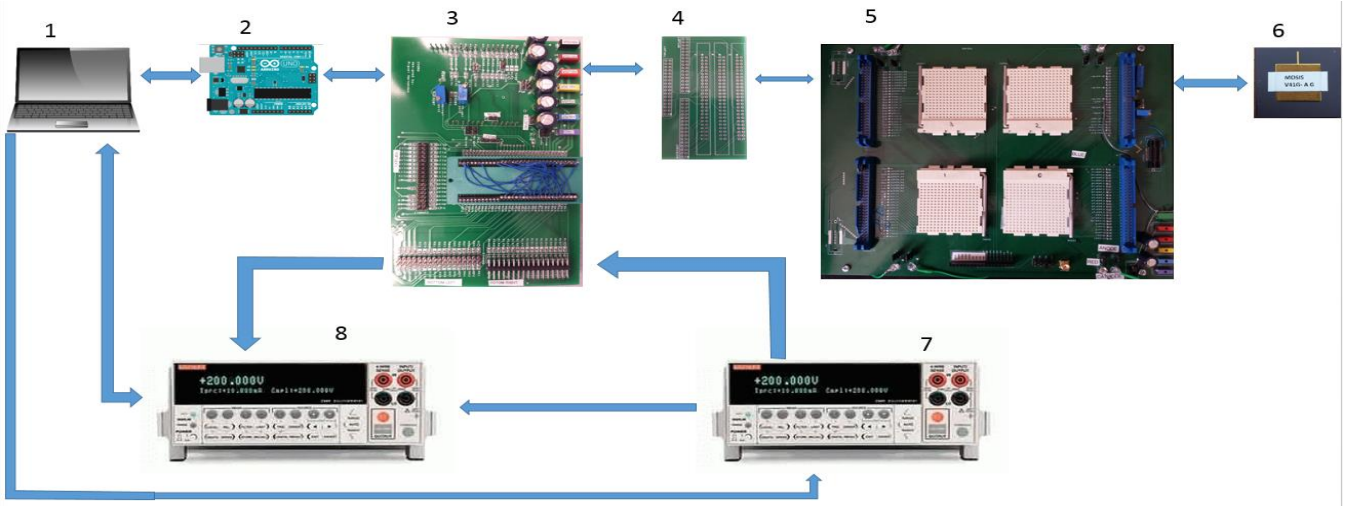

Figure 1. (1) User interface computer, (2) arduino Microcontroller,(3) BRT board,(4) adapter board, (5) MRTP,(6) RIIC PGA package, (7) Keithley meter programmed to do voltage sweeps,(8) Keithley meter programmed to measure the output of the RIIC.

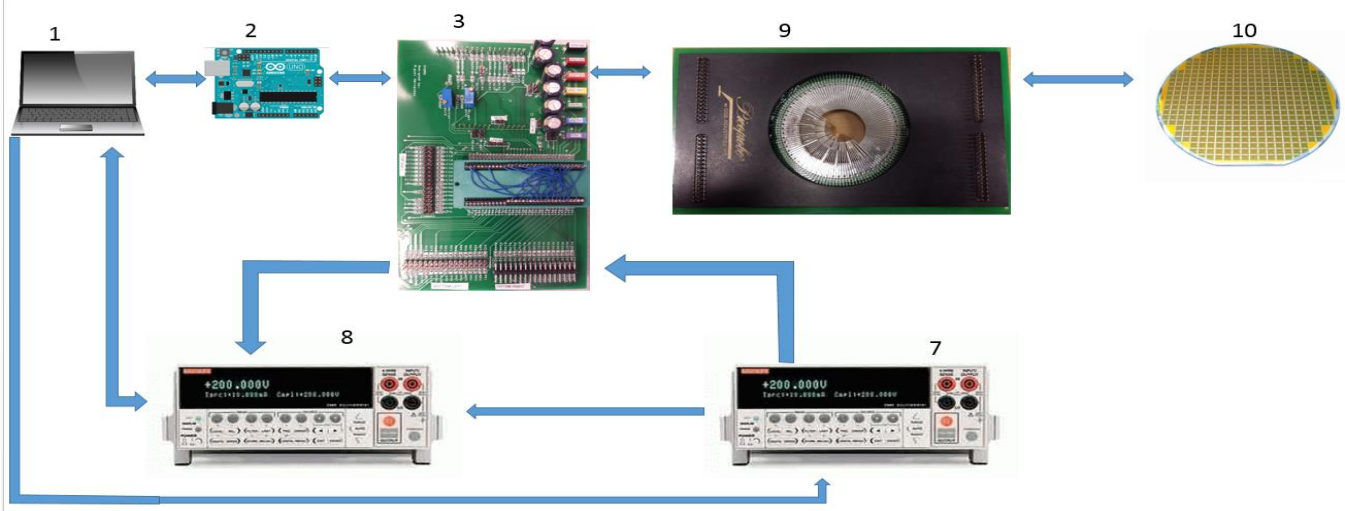

Figure 2. When testing the (10)RIIC in its wafer form, (9) a custom probe card is added. Everything else is the same.

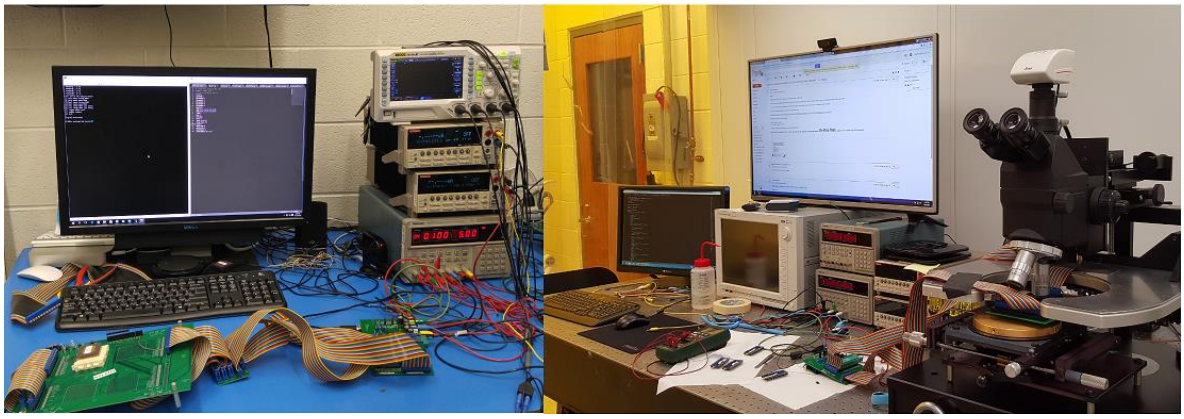

Figure 3. (Left) system setup used to test RIICs in PGA packages. (Right) system setup used inside the clean room to test RIICs on a wafer

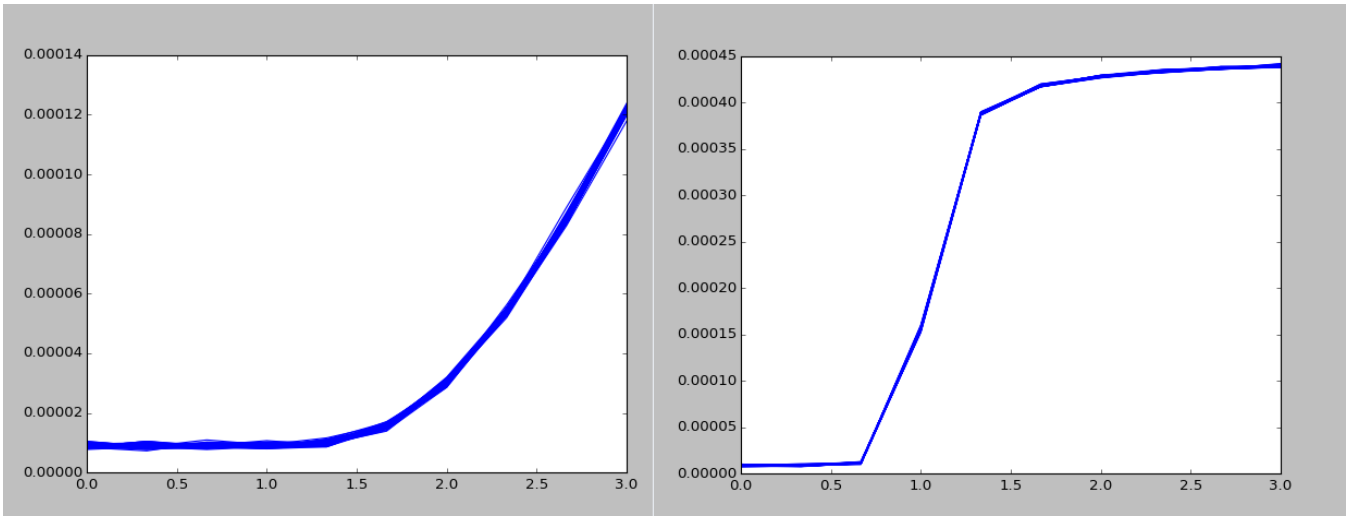

Figure 4. this is data collected from a RIIC. These are hundreds curves stacked on top of each other. (left) curves of the weak drive transistor that drives pixels. (right) curves of the strong drive transistor that drives pixels. On both sets curves the y axis is in Amps and the x axis is in Volts

Tests done on the RIICs

Testing different versions of RIICs requires having two categories of tests: general tests and specific tests. Most of the tests fall under the general tests category. This category includes all of the tests that are the same regardless of the RIIC version being tested. These tests include the following:

Power rails tests: Before applying power to the RIICs it is very important to make sure that none of the power rails are shorted to ground or with each other. This is done by checking the impedance between all the rails.

Communication test: The RIIC is programmed using SPI. Thus in order to make sure that it is getting programmed correctly a specific series of bytes is written to fill its memory, then a second set of bytes with the same size is written to the same memory location. The second set of bytes pushes the first set out of memory to a serial output pin. If the values that come out are the same as those that went in it means the SPI communication works correctly.

Lighting up LEDs: All the RIICs have the corner pixels brought out to output pins. Thus external LEDs can be connected to pins in order to test the behavior of the pixel drive circuitry. Lighting up LEDs is a great visual representation that shows the driving circuits work correctly. There are different methods to run this test, the most helpful method is to program the RIIC to operate in DAC mode. This way the two Keithleys will function as the DAC input voltages to the RIIC, and can do sweeps to change the

brightness on the LEDs. Other tests include blinking the LEDs at different frequencies, and testing the memory of the chip by writing to the corner pixel and then to a random pixel. Also it is possible to visualize how long the charge in the NMOS logic inside the RIIC is held by timing how long the LED stays lit.

Monitor out (mout) tests: The RIIC has a pin dedicated to monitoring certain internal circuitry. This pin can be programmed to monitor different internal circuits. The monitor out tests are the most meaningful set of tests because the mout pin is capable of monitoring all the pixels in the RIIC individually. Different RIICs have different mout tests that can be done on them, however, the most common and important tests are sweeps of all the drive transistors inside every pixel circuit. All RIICs have two drive transistors per optical emitter, a weak and a strong. Sweeps of both the weak and strong NMOS drive transistors are shown in Figure 4. When a RIIC produces a set of curves that look very thin it means it is a good RIIC where all the driving transistors tested behave properly. On the other hand if the line looks thicker or has random spikes it means the pixels might be dead or have an unwanted behavior. In addition, by analyzing the numerical data obtained during testing it is possible to produce statistics that further help deduce which RIICs are best for hybridization. In order to do a sweep the RIIC gets programmed to look at one driving transistor, weak or strong, and monitor its current as function of voltage. At the same time one Keithley meter is programmed to do a voltage sweep of a range and steps specified by the user. The second Keithley is programmed to act as a meter that records current readings on the mout pin.

Some tests that are specific to different RIICs include:

Mout tests on PMOS drive transistors: TCSA RIICs are designed to produce two colors per pixel in the infrared spectrum. Thus PMOS transistors are used to drive the second color. The same procedure is used as the mout tests on the NMOS transistors with the exception that the mout pin has to be pulled up to ten volts dc.

Time multiplexer: The NSLEDS RIIC has twice as many drive transistors per pixel than the TCSA versions. However only half of those can be accessed at any time. For this reason there is a time multiplexing signal that selects which half of the driving transistors gets instructed. The tests consist of programming both sets of drivers by using the multiplexing method. Then resetting or changing one or the other and observing that changes to one do not affect the other.

Conclusion

As of the writing of this paper the TCSA and NSLEDS RIICs have been tested, and through those tests it was possible to find the optimum RIICs for the hybridization process. The HDILED RIIC is the next version getting tested. This RIIC has twice the number of pixels than the previous versions. For this reason the PGA package is bigger and requires a larger socket to plug into. As a result another board was created to serve as an interface between the bigger socket and the MRTP. This small addition ensures that the same test system can be used for larger RIICs. In addition the size of the HDILED RIIC does not matter when testing a full size sample on a wafer using a probe card. Thus no changes will be needed for the set up used in the clean room facility.

Acknowledgments

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