Novel Si-Ge-C Superlattices for "More than Moore" CMOS

Lynn Forester, Carlos J. Augusto, Pedro C. Diniz
Quantum Semiconductor LLC
4340 Stevens Creek Blvd. Suite 284
San Jose, CA 95129
Contact author: Lynn.Forester@Quantumsemi.com

Abstract: *The search for Silicon-based direct band-gap semiconductors is more relevant than ever for "More than Moore" CMOS. Monolithically-integrated novel crystalline materials are key to enabling increased performance and new functionalities, such as efficient light absorption and emission. Si-Ge-C SuperLattices [1] are highly ordered synthetic crystals having direct band-gaps and large oscillator strengths. This paper will present ongoing research in simulation and epitaxial growth.*

Keywords: Silicon; Germanium; Carbon; Superlattices; Direct Band-Gaps; Silicon-Photonics; Image Sensors.

Introduction

Materials with direct band-gaps and large oscillator strengths are necessary to enable efficient light absorption and/or light-emission. The ongoing search for direct band-gap materials with large oscillator strengths that can be monolithically integrated with CMOS has been pursued through multiple approaches. Group-IV materials are still generally perceived as offering the easiest integration with CMOS technology. Engineering of strain, composition, dimensionality, structural order and symmetry, are all being employed to discover and generate modified band structures and optoelectronic properties.

Recent examples include Ge tensile-strained to relaxed Ge buffer layers, which demonstrate lasing action [2]; GeSn alloys grown on Ge buffer layers [3]; Si-Ge superlattices strained to SiGe relaxed buffer layers [4]; and compound semiconductors such as InP [5] and InGaAs [6] grown in silicon nano-trenches. The drawback of many schemes is the use of thick buffer layers. Typical buffer layers (e.g. SiGe), grown on Si(100) surfaces, have a high intrinsic defectivity (> 1E5/cm2) and thicknesses greater than 1µm, which is much larger than the thickness of the gate stack in current and future CMOS generations (<0.2µm), thereby introducing yield and planarization challenges, respectively. The difficulty of incorporating III-V materials into a CMOS process leads to laborious and expensive processes which are not well-suited to high volume production.

An alternative to these schemes is provided by Si-Ge-C SuperLattices (SLs). Since 2011 we have been working with INESC MN [7] to develop ab-initio codes in order to explore the various properties of these materials and to pick the best ones for development. Si-Ge-C SLs strained to silicon surfaces are highly ordered synthetic crystals made by alternating layers of $(Si_{1-y}C_y)_m$ and $(Ge)_n$, in which "m" and "n" are the numbers of atomic planes. The simulations show important variations in band-gap type (direct versus indirect) and magnitude. These properties change as a function of surface orientation of the substrate on which the epitaxial growth is performed, as well as the amount of Carbon and periodicity of the SL.

Compared to the incorporation of III-V materials in CMOS, the use of Si-Ge-C SLs strained to Silicon in future CMOS devices is expected to be relatively straightforward since these new materials are epitaxially grown directly on Silicon surfaces and do not require SiGe or GeSn relaxed buffer layers and do not incorporate new elements, since Si-Ge-C random alloys are widely used in BiCMOS processes. The Si-Ge-C SLs will likely be grown by either blanket or selective epitaxy, and etched to create the layer configuration as required by the specific device.

Simulation Results

Ab-initio studies have shown that it is possible to have band-gaps, including direct ones, that are much smaller than that of Germanium, and also to have negative band-gaps, i.e., semimetals. Figure 1, shows a schematic depiction of a $(Si_4C)_3$-$(Ge)_2$ SL (E_G=0.53eV).

Figure 2 shows the atomistic structure, highlighting the atomic-plane by atomic-plane construction of the cell, in which the Ge, Si and C atoms, are presented by grey, blue and brown spheres, respectively. The ab-initio codes we employ are unique in their ability to represent any combination of atoms plane by plane.

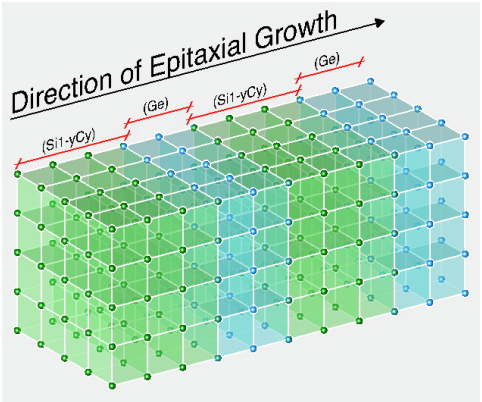

Figure 1. Schematic depiction of a $(Si_{1-y}C)_3$-$(Ge)_2$ SL.

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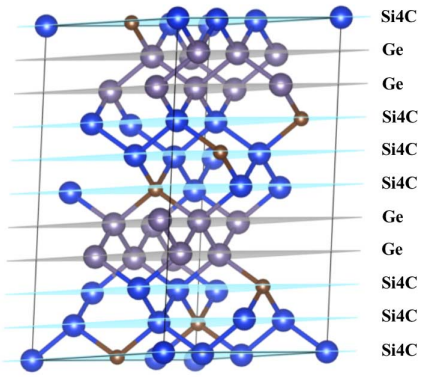

Figure 2. Atomistic representation of a $(Si_4C)_3$-$(Ge)_2$ SL strained to a Si(100) surface.

Figure 3 shows the band structure and the dipole momentum elements (μx, μy, μz) for light absorption/emission across the fundamental gap, for the three polarizations (μx and μy are for light propagating along the z-direction, i.e., the direction of the SL axis).

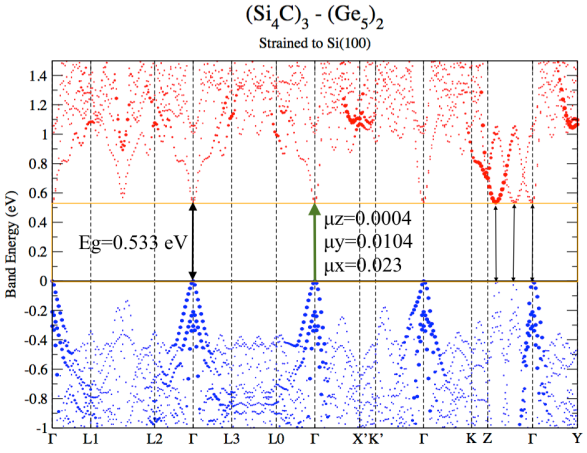

Figure 3. Band structure of a $(Si_4C)_3$-$(Ge)_2$ SL strained to a Si(100) surface.

It is important to note that the same Si-Ge-C SL composition will have significantly different band structures when strained to different surface orientations, such as <100>, <101>, <111>, etc. This is because the conduction bands of different materials have energy minima along the different directions of the Brillouin Zone (BZ), such as the X-direction for Si, $Si_{1-y}C_y$, and the L-directions for Ge. The pseudomorphic growth of the SLs on different surface orientations leads to different alignments between the direction of strain and the directions of symmetry in the BZ. Given that it is possible to have CMOS wafers with active areas with multiple surface orientations [8,9], it becomes possible to have a wide range of different band structures in epitaxial layers that can be grown on adjacent active areas. This opens up a new and vast parameter space to be explored for band-gap and device engineering.

Fabrication of Si-Ge-C Superlattices

The development of fabrication techniques to produce thin films with atomic-layer control has been the focus of several research groups in recent years. A recent major advancement [10] in the self-limiting epitaxial growth of $Si_{1-y}C_y$ mono-layers, with y=50%, provides evidence that such layers are possible to grow in a controlled manner both in composition and thickness (the simulations presented in this paper were done for y=20%).

Furthermore, similar techniques have been applied successfully to the self-limiting growth of several other group-IV elements and dopants [11]. In both cases, commercial epitaxial production equipment was used, which is typically employed to grow random alloy SiGeC layers, for the Base of HBTs in BiCMOS and in leading edge CMOS for strain engineering. These epitaxial growth methodologies enable the consistent fabrication of precisely-defined atomic layer compositions and thicknesses. In addition to the standard process parameters of temperature, pressure and time, novel chemical precursors can be employed to increase the Carbon content of the resulting material or to build-in a particular ratio of elements. We are currently working to develop a CVD process technology to grow these Si-Ge-C SLs.

To ensure that the composition is well-defined, the substrate on which the epitaxial growth occurs should also be atomically flat [12-15], thereby avoiding surface roughness, fluctuations in composition, and in potential. Complementary to the atomic-plane control of epitaxial pseudomorphic growth processes, is the atomic-plane control of etching of silicon and other materials [16]. Atomic-plane control on atomically–flat surfaces of both growth and etching, enables unprecedented precision in manufacturing of materials and devices, and in particular short-period superlattices, along with superlattice nanowires and dots. Consequently, the SL materials represented in the ab-initio simulations, can indeed be realized and manufactured on a commercial scale.

Applications of Si-Ge-C Superlattices

A key application for future Si-Ge-C SLs are high-quantum efficiency photo-diodes in CMOS pixels, for the visible range, as well as for the Short-Wavelength Infra-Red (SWIR), Mid-Wavelength Infra-Red (MWIR), and Long Wavelength Infra-Red (LWIR), which can all be monolithically integrated side-by-side. Because the photo-diodes can be entirely formed by epitaxial growth, CMOS Active Pixel Sensors can be made with Fully-Depleted SOI CMOS. One important advantage of FD-SOI CMOS is its superior radiation hardness, which makes it ideally suited for a number of aerospace and military applications.

Figure 4 shows a schematic cross-section of a Si-Ge-C CMOS pixel, in which the photo-diode comprises a Si-Ge-C SL photo-absorption region, surrounded by a pinning layer, thus making it a Pinned Photo-Diode (PPD). Both the

Si-Ge-C SL and the pinning layer are epitaxially grown on the source/drain region of a NMOS Transfer Gate (TG), which could be part of a 4T pixel APS. PPDs are preferred in CMOS image sensors for the ability of the pinning layer to suppress the surface-related leakage (dark) currents.

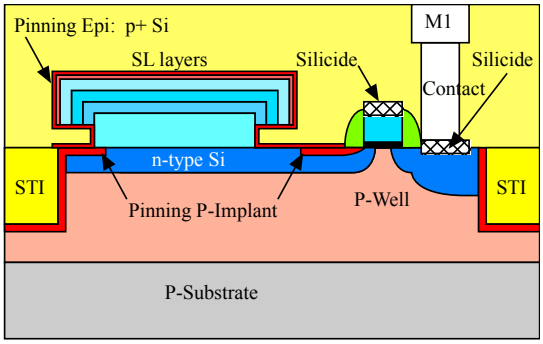

Figure 4. Schematic cross section of a CMOS pixel with a PPD comprising a Si-Ge-C SL absorption region.

The composition of the SL in the photo-absorption region is chosen according to the desired wavelength range of the sensor. Several Si-Ge-C SLs have direct band-gaps across a wide range of energies, i.e., a wide interval of wavelength cutoffs, ranging from E_G=0.53eV (λ_C=2.3µm) for $(Si_4C)_3$-$(Ge)_2$ strained to Si(100) in Figure 3; E_G=0.21eV (λ_C=5.9µm) for $(Si_4C)_5$-$(Ge)_5$ strained to Si(111) in Figure 5; and E_G=0.16eV (λ_C=7.75µm) for $(Si_4C)_5$-$(Ge)_5$ strained to Si(100) in Figure 6.

Another application of Si-Ge-C SLs, shown in Figure 7, is the replacement of the SiGeC random alloy in the base of Heterojunction Bipolar Transistors (HBTs), part of a BiCMOS process, by a Si-Ge-C SL. The large variety of Si-Ge-C SL band-gaps and band offsets, enables the fabrication of HBTs in which not only the Base layer is a SL, but also the Emitter and the Collector may be SLs. This enables the fabrication of high-performance Complementary SL HBTs, which can be useful for analog applications [17].

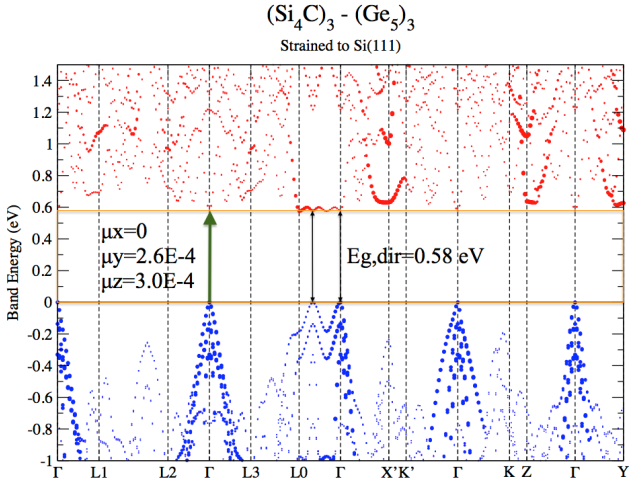

Figure 5. Band structure of a $(Si_4C)_5$-$(Ge)_5$ SL strained to a Si(111) surface.

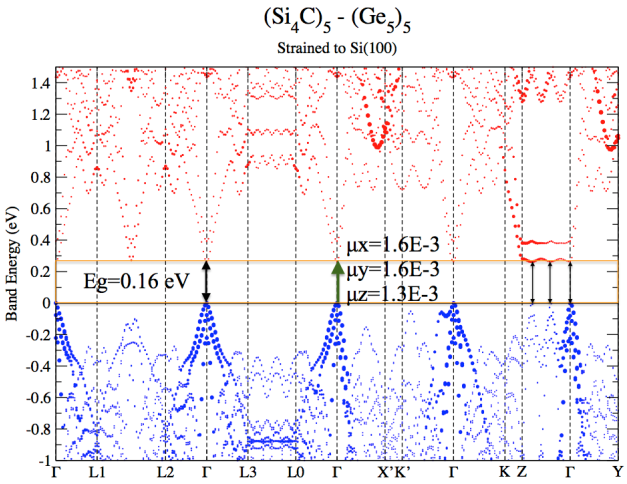

Figure 6. Band structure of a $(Si_4C)_5$-$(Ge)_5$ SL strained to a Si(100) surface.

Si-Ge-C SLs with direct band-gaps may also be used to emit light in certain device configurations, such as LEDs/LASERs, as schematically depicted in Figure 8 for a Vertical Cavity Surface Emitting Laser (VCSEL) monolithically integrated with CMOS devices. HBT-LASERs [18], will also be possible when using a direct band-gap Si-Ge-C SL for the Base layer, which can be monolithically integrated with CMOS circuitry.

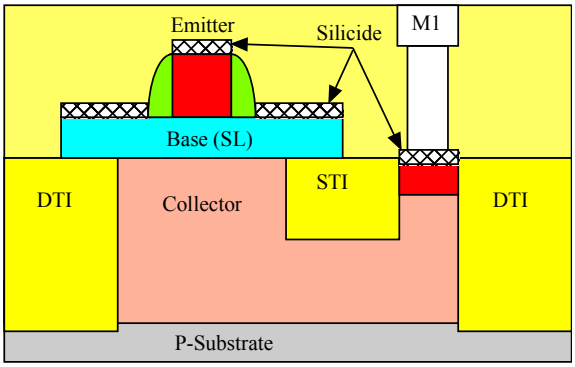

Figure 7. Schematic cross section of a HBT in a BiCMOS technology, with Si-Ge-C SL Base layer.

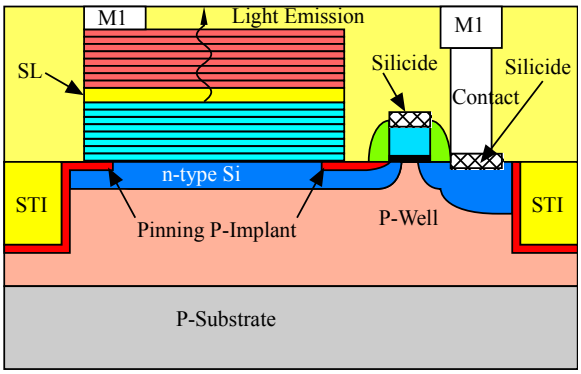

Figure 8. Schematic cross section of a possible monolithic integration of a Si-Ge-C SL VCSEL with CMOS.

An additional device well suited for improvement with SLs is the Avalanche Photo-diode (APD). We are currently using a commercial foundry to develop Separate Absorption & Multiplication (SAM) APD 2D arrays, in which the absorption region is a Si-Ge-C SL.

Conclusions

Si-Ge-C SLs present an exciting opportunity to vastly expand the functionality of silicon-based devices and circuits, enabling "More than Moore" with the creation of active photonic devices monolithically integrated with CMOS. Applications include Multispectral CMOS Image Sensors, higher performance HBTs in BiCMOS, and CMOS-based LED and LASER 2D arrays.

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References

1. Augusto C.J., L. Forester, "Novel Si-Ge-C Superlattices and Their Applications", SSE vol. 110, p1-9, August 2015, (ISTDM 2014). http://dx.doi.org/10.1016/j.sse.2015.01.019.
2. Liu J., X. Sun, R. Camacho-Aguilera, "Ge-on-Si laser operating at room temperature", Opt Lett. 2010; 35(5):679–81. http://dx.doi.org/10.1364/OL.35.000679.
3. Wirths S., R. Geiger, C. Schulte-Braucks, et al., "Direct Bandgap GeSn Microdisk Lasers at 2.5µm for Monolithic Integration on Si-Platform", IEDM Techn. Digest 2.6.1-2.6.4 (IEEE, 2015).
4. d'Avezac M., J.-W. Luo, T. Chanier, et al., "Genetic-algorithm discovery of a direct-gap and optically allowed superstructure from indirect-gap Si and Ge semiconductors", Phys. Rev. Lett. 2012;108:027401. http://dx.doi.org/10.1103/PhysRevLett.108.027401.
5. Wang Z., B. Tian, M. Pantouvaki, et al., "Room-temperature InP distributed feedback laser array directly grown on silicon", Nature Photonics **9**, 2015:837-842. http://dx.doi.org/10.1038/nphoton.2015.199.
6. Waldron N., C. Merckling, L. Teugels, P. Ong, S.A.U. Ibrahim, F. Sebaai, et al., "InGaAs Gate-All-Around Nanowire Devices on 300mm Si Substrates", IEEE Elect. Dev. Lett., VOL. 35, No. 11, Nov. 2014. http://dx.doi.org/10.1109/LED.2014.2359579.
7. INESC-MN, Group of Prof. José Luís Martins. http://bohr.inesc-mn.pt/~jlm/
8. Yang M, M. Ieong, L. Shi, et al., "High performance CMOS fabricated on hybrid substrate with different crystal orientations", IEDM Techn Digest 2003:453–6. http://dx.doi.org/10.1109/IEDM.2003.1269320.
9. Yang M., V.W.C. Chan, K.K. Chan, et al., "Hybrid-orientation technology (HOT): opportunities and challenges", IEEE Trans. Electro. Dev. 2006;53(5):965. http://dx.doi.org/10.1109/TED.2006.872693.
10. Yamamoto Y., J. Murota, B. Tillack, "C and Si delta doping in Ge by CH_3SiH_3 using RPCVD", The 9th International Conference on Silicon Epitaxy and Heterostructures (ICSI-9), p. 147, 2015. http://www.polymtl.ca/nhl/en/nouveautes/index.php.
11. Murota J., M. Sakuraba, B. Tillack, "Atomically controlled CVD processing of group IV semiconductors for ultra-large-scale integrations", Adv. Nat. Sci. Nanosci. Nanotechnol. 2012; 023002(3):4. http://dx.doi.org/10.1088/2043-6262/3/2/023002.
12. Tanaka S., G.C. Umbach, J.M. Blakely, et al., "Fabrication of arrays of large step-free regions on Si (0 0 1)". Appl. Phys. Lett. Aug. 1996; 69(9):1235–7. http://dx.doi.org/10.1063/1.117422.
13. Li X., A. Teramoto, T. Suwa, et al., "Formation speed of atomically flat surface on Si (1 0 0) in ultra-pure argon", Microelectron. Eng. 2011; 88:3133–9. http://dx.doi.org/10.1016/j.mee.2011.06.014.
14. Kuroda R., T. Suwa, A. Teramoto, et al., "Atomically flat silicon surface and silicon/insulator interface formation technologies for (1 0 0) surface orientation large-diameter wafers introducing high performance and low-noise metal-insulator-silicon FETs", IEEE Trans. Elect. Dev. Feb. 2009; 56(2):291–8. http://dx.doi.org/10.1109/TED.2008.2010591.
15. S. Sugawa, Presentation at PIXEL 2012, Inawashiro, September 4, 2012. http://indico.cern.ch/event/137337/session/5/contribution/106
16. Kanarik K.J., T. Lill, E.A. Hudson, et al., "Overview of atomic layer etching in the semiconductor industry", J. Vac. Sci. & Tech. A 33, 020802 (2015); http://dx/doi.org/10.1116/1.4913379.
17. Chakraborty P.S., K.A. Moen, J.D. Cressler, "An Investigation on the Optimization and Scaling of Complementary SiGe HBTs", IEEE Trans. Elect. Dev., Vol. 60, No. 1, Jan. 2013. http://dx.doi.org/10.1109/TED.2012.2225838.
18. Feng M., N. Jr. Holonyak, G. Walter, R. Chan, "Room temperature continuous wave operation of a heterojunction bipolar transistor laser", Appl. Phys. Lett. **87**, 131103, 2005. http://dx.doi.org/10.1063/1.2058213.