Megawatt-Scale Power Hardware-in-the-Loop Simulation Testing of a Power Conversion Module for Naval Applications

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Abstract— **In June through October of 2014, power-hardware-in-the-loop (PHIL) simulation testing of a 1.2 MW, 4.16 kV AC / 1 kV DC power conversion module for naval applications was conducted. In these tests, the device-under-test (DUT) was interfaced to a virtual surrounding system that was generally representative of the power system of a future surface combatant. Tests were focused on demonstration of operation and performance of the DUT through dynamic conditions in a realistic environment, collection of data for characterization and validation of models of the DUT, and collection of data for assessment of the accuracy and suitability of the approach for testing future power conversion modules. These tests were the culmination of numerous coordinated efforts over preceding months to identify, implement, and verify the necessary surrounding systems and supporting models, define meaningful test procedures, and develop, implement, and test appropriate controls and protection systems. The tests successfully concluded with a large amount of data of the behavior of the DUT under a wide range of expected system conditions. Moreover, this project identified the need to further develop PHIL interface algorithms such as the damped impedance method to improve accuracy and stability of future PHIL experiments at the megawatt scale.**

I. INTRODUCTION

Power hardware-in-the-Loop (PHIL) simulation offers solutions to a number of challenges encountered in the development and deployment of new technologies for naval applications. For systems comprised of components from multiple vendors, each of which may have a different development schedule, testing of a power component within an emulated environment often provides one of the only opportunities for assessing and addressing potential system integration issues at an early stage. The approach also can be used to test the device-under-test (DUT) in extreme or dangerous conditions, which might not be attempted in fully hardware experiments. The flexibility afforded by the approach allows the surrounding systems to be quickly and easily changed, allowing a large range of tests to be conducted within a relatively short time and with minimal changes to the test setup. While PHIL simulation offers solutions to a number of challenges, the approach is not without its own challenges. The accuracy of a PHIL experiment is constrained by the accuracy of the surrounding system models, and both accuracy and stability are affected by the non-ideal aspects of the PHIL interfaces. Thus, it is important to properly consider the limitations of a PHIL experiment and to consider the accuracy of the results in the context of the noted points [1].

This paper describes efforts to establish PHIL test capabilities for AC/DC converters to be employed for future advanced sensor and weapons systems, including a description of PHIL testing of a 1.2 MW, 4.16 kV AC/1 kV DC power conversion module (PCM). Section II provides an overview of the preparatory efforts for the testing, including development of the test plan and the surrounding system models. Section 0 describes the test setup, including a description of the DUT

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and the PHIL test bed. An overview of the PHIL testing is given in Section IV, along with selected results from the tests, with concluding comments given in Section V. It is anticipated that the DUT will be tested in a fully hardware test bed, and these results are expected to provide significant information for assessment of the accuracy of the PHIL experiments. However, at the time of writing, these results were not yet available for comparison.

II. PLANNING AND PREPARATION

Efforts to prepare for PHIL testing of the DUT included defining the surrounding systems to be emulated and the component models of which these systems were to be comprised, developing the test scenarios and procedures to be executed, and implementing the necessary models, PHIL interfaces, and control and protection systems for the digital real-time simulator (DRTS). To begin the process, a test concept document was first developed and refined over several revisions. The purpose of this document was to identify, at a high level, the test scenarios to be executed and the surrounding systems needed to support these scenarios. The document identified the component modules that were needed for the surrounding systems and the necessary interfaces, capabilities, and parameters needed to be supported by the modules, but did not specify the particular models to be employed for the modules. Similarly, the scenario descriptions generally described the tests to be conducted and the test parameters to be varied, but did not include specific procedures or the specific sets of parameter values for which the tests were to be executed. This document provided a convenient way to formulate and refine the tests to be conducted and the components that would be necessary for the tests from a high level, functional viewpoint. This step potentially saved substantial effort in defining specific procedures and developing models, as the tests and systems evolved over several iterations of discussions and revisions of the test concept document. Detailed procedures, including specification of models and PHIL interface algorithms to be used, values of sets of parameters, and protection settings were included in the test plan that was subsequently developed.

The identified test scenarios were intended for characterization of the behavior of the DUT, verification of capabilities of the DUT, and to probe for potential interactions between the DUT and the system into which it could potentially be integrated. Tests primarily intended for characterization and verification of capabilities included exposing the DUT to a range of steady state and transient conditions at the AC terminals spanning the space of conditions allowed by MIL STD 1399 [2] and characterization of impedance at the AC and DC terminals. Other tests included exposing the DUT to a range of loading conditions, including ramps of varying magnitude, rate, and characteristic, as well as including superimposed oscillations in load of varying magnitude and frequency. Some of the tests were intended to assess the DUT operating as the sole supplier of the DC load, while other tests were intended to assess the DUT operating in parallel with a simulated PCM.

The process of defining the surrounding systems to be employed focused on assessing the minimum components needed to suitably represent the salient characteristics of a shipboard power system from the perspective of the DUT and in the context of the identified test scenarios. While it is certainly possible to represent a large number of components and a high degree of detail with current DRTS systems, the benefit of additional details in the simulated surrounding system must be weighed against the added complexity in managing, controlling, and maintaining stability in the PHIL experiment. After several iterations of the surrounding systems and test scenarios, the system illustrated by Figure 1 was settled upon, as a single surrounding system which could accommodate the full range of test scenarios identified.

The system includes two AC source modules with aggregate AC load modules at the terminals, along with a simulated PCM (for parallel operation with the DUT) and two DC load modules. The AC source modules were intended to support both emulation of a representative gas turbine generator set, as well as a flexible, controllable voltage source model to be used to create specific conditions at the terminals of the DUT. The controllable voltage source was intended to allow independent control of voltage magnitude, frequency, unbalance, and harmonic distortion, in order to accommodate recreation of conditions spanning the limits of [2]. One of the models to be used as a DC load was required to represent a mix of constant power, current, and impedance characteristics, and support ramps in load power, as well as supporting the superposition of current oscillations. Another model to be used as a DC load was intended to represent the characteristics of a DC/DC converter supplying a sensitive DC load. The AC load modules were intended to represent an aggregate mix of constant power, current, and impedance loads, as well as induction machines, in order to represent typical low-voltage ship service loads. The two AC load modules are connected through primary and backup (dashed lines in Figure 1) supplies to allow vital loads to be transferred to the alternative feed if the primary connection is lost. In addition to affecting the voltage on the AC buses, these load modules are also included to allow observation of the voltage at the load buses. The PCM model was intended to support testing parallel operation, and was intended to represent, as closely as possible, a PCM equivalent to the DUT. Thus, the test concept document generally specified the types of tests to be conducted and the characteristics of the models needed to support these tests.

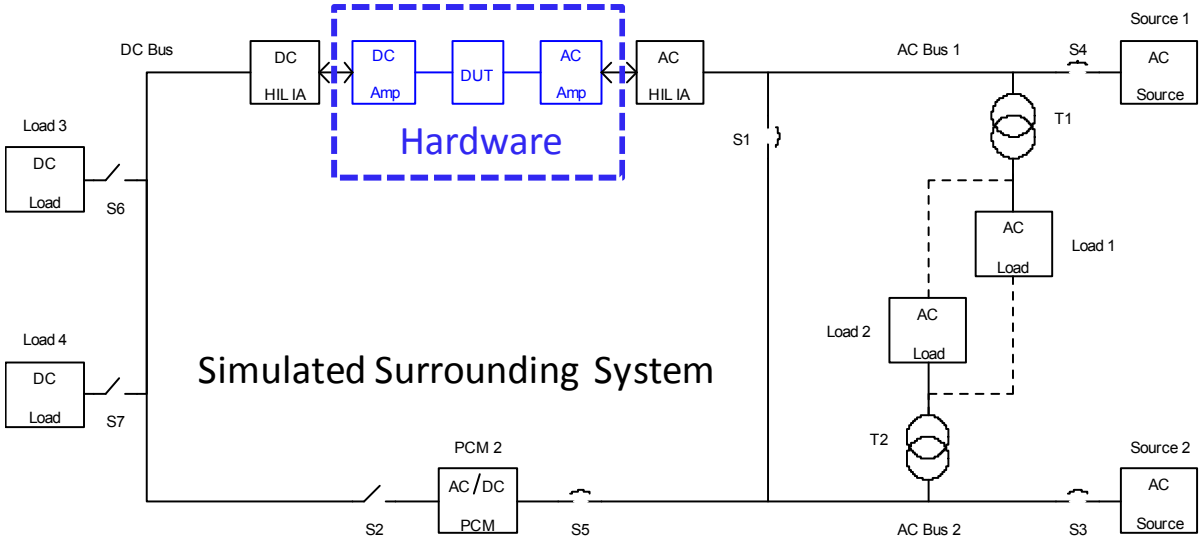

Figure 1 Simulated Surrounding System

For each of the models implemented for the DRTS, a model design document (MDD) was produced, along with verification and validation (V&V) plans and reports. Some of the models were based on actual hardware, such as the generator set, which was based on the Rolls-Royce 4500. For these models, V&V could include validation against physical measurements with the device. For other models, such as the controllable voltage source model, the V&V exercises primarily focused on assessment of the accuracy with which the model reproduced the reference conditions. Other models, such as the large DC load model, which modeled a DC/DC converter and various load characteristics, were developed by the government to be representative of a range of equipment, though not based on a specific device. For these, V&V of the DRTS implementation primarily consisted of assessing the accuracy when compared with the reference implementation that was provided. Prior to testing, these models and the results of the V&V activities were reviewed for suitability of the models for use in the PHIL testing.

III. Test Setup

The test setup, which included the DUT, AC amplifier, DC amplifier, current and voltage probes, and DRTS system is illustrated by Figure 2. The DUT was a bi-directional 1.2 MW, 4.16 kV AC / 1.0 kV DC PCM developed by DRS Technologies as part of the Office of Naval Research (ONR) sponsored Compact Power program.. The PCM provided isolated 1.0 kV DC power via two stages of power conversion. The first stage of power conversion was performed by a neutral-point-clamped, three-level, active-front-end. The second stage of power conversion was performed by a neutral-point-clamped, three-level buck converter. The AC and DC amplifiers and DRTS are part of the 5 MW PHIL test bed at the Florida State University (FSU) Center for Advanced Power Systems (CAPS). The AC and DC amplifiers are parts of a 5 MW, nominally 4.16 kV amplifier developed by ABB. The amplifier can be split into two 2.5 MW amplifiers, as in the configuration used for these experiments, and one of the amplifiers can be configured for DC operation at up to 1.15 kV. The units are each bi-directional with an effective bandwidth of approximately 1.2 kHz. In the configuration used for these experiments, the AC amplifier received instantaneous voltage references from the DRTS, and the DC amplifier was configured to accept a DC current reference, with a small resistive load bank connected in parallel to the amplifier.

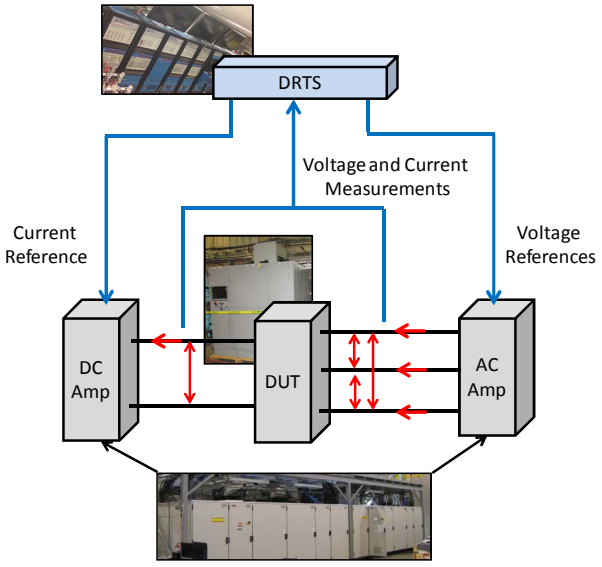

Figure 2 Test Setup

The DRTS system is a 14-rack RTDS system [3] developed by RTDS Technologies. The system executes electromagnetic transient simulations in real-time, with time-step sizes on the order of 50 µs, although small subsystems can be represented with time-step sizes on the order of 2 µs.

The voltages and currents at the AC and DC interfaces of the DUT was measured and supplied to the DRTS for purposes of monitoring, control, and protection. While the DRTS can be used for data acquisition, its time resolution is limited to the time-step size of the simulation, which, in this case, was 50 µs. In order to facilitate higher time-resolution captures, the voltage and current measurements were also supplied to a dedicated National Instruments data acquisition system (DAQ). With this setup, the DUT is able to interact with the emulated surrounding system through the power amplifiers, and power is circulated from the AC amplifier to the DC amplifier such that only system losses are dissipated (i.e. the entire load power is not dissipated).

The DRTS served a number of roles in the experiments, including monitoring, emulation of the surrounding system, and protection. Computation of RMS voltages and currents, real and reactive power, voltage unbalance, and harmonic distortion was included as part of the DRTS case, and displayed to the operators in real time for monitoring purposes. The DRTS is also used for simulation of the surrounding system and control of the PHIL interfaces. Initially, the ideal transformer model (ITM) algorithm [4] was employed for both the AC and DC PHIL interfaces. However, as testing progressed, instabilities with interfaces were encountered, and voltage-type and current-type damping impedance method (DIM) algorithms [4], [5], [6] were substituted for the AC and DC interfaces, respectively. For some of the tests, a DQ-axis implementation of the DIM algorithm was employed. For the phase-locked loops of the interface, the decoupled double synchronous reference frame (DDSRF) PLL was employed, using the double second-order generalized integrator (DSOGI) frequency locked-loop [7]. Further, while the amplifiers and the DUT all implement protection systems, protection functions were implemented as part of the DRTS case to serve as primary protection to gracefully shut down the experiment in the event that a problem was detected. Protection elements were implemented to trigger on over-voltage, over-current, over/under-frequency, and zero-sequence voltage or current (to detect loss of a sensor), as well as detection of external trip signals (both manual and from the DUT) and detection of an issue with one of the simulated component models. A number of protection actions were implemented, ranging from ramping AC voltage magnitude, phase, and frequency to nominal conditions to ramping voltage and current references to zero and tripping the amplifiers. A mode of operation of the DRTS case was also implemented in which the test bed and the DUT are simulated. In this way, the actual controls and protection systems to be used for the PHIL tests, along with the PHIL experiments themselves, could be first tested in simulation.

IV. PHIL TESTING

PHIL testing was conducted from June through October 2014, over which time a large volume of data was collected for the purposes of verifying and characterizing the performance of the DUT, for model development and validation, and for exploring possible interactions with the surrounding systems. Load ramp tests, in which the load type, ramp rate, and ramp magnitude were varied, allowed characterization of the ability of the DUT to regulate the DC voltage under dynamic conditions. Tests were conducted in which the voltage magnitude, frequency, unbalance, and harmonic distortion were simultaneously varied, as in Figure 3, to characterize the behavior of the DUT under these conditions. Tests in which ripple components of varying frequency were superimposed on the DC load current provided insight into how these oscillations might be shared between multiple PCMs and how they would propagate through the DUT and interact with the generator controls or affect other shipboard loads. The flexibility of the PHIL setup was also demonstrated in superimposing different types of current ripples (not only single frequency sinusoidal) that may be more representative of those presented by actual loads, as illustrated by Figure 4. Similarly, pulsating loads approaching 30% of system generation power were applied, and the effects on the system voltage magnitude and frequency were studied, as illustrated by Figure 5 and Figure 6. In other tests, a randomized pulsating load was applied as the profile for the large load model, as illustrated by Figure 7 and Figure 8. The randomized load profile is illustrated by the "Load" curve in Figure 8 (zoom view), but the DC/DC converter of the large load model provides filtering, such that the load current applied to the DUT is as shown by the "DUT" curve. The AC input power and DC output power from the DUT are illustrated by Figure 7. The majority of the tests described were repeated with a simulated PCM operating in parallel with the DUT, to assess the characteristics of operation in this configuration.

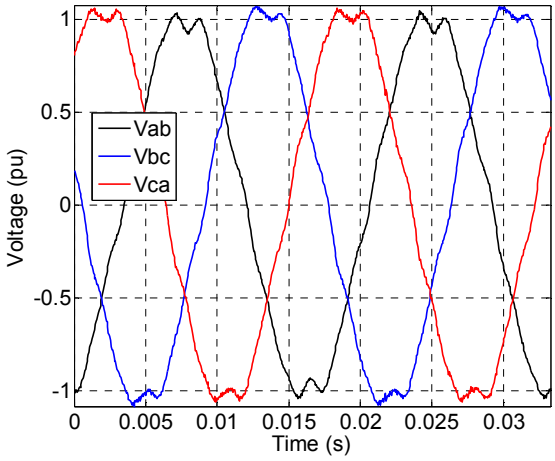

Figure 3 AC Voltage Waveforms Applied During Steady State Characterization Tests

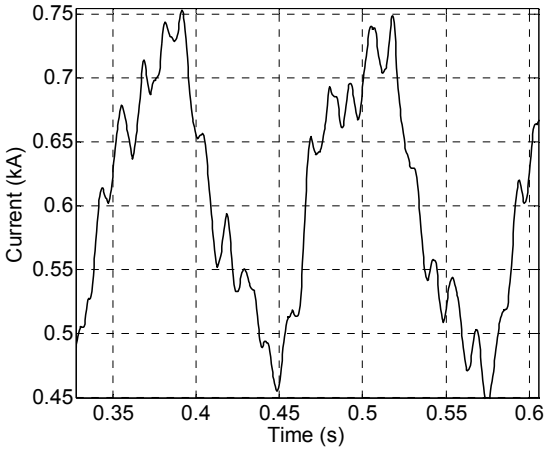

Figure 4 DC Load Current with Multiple Ripple Components Superimposed

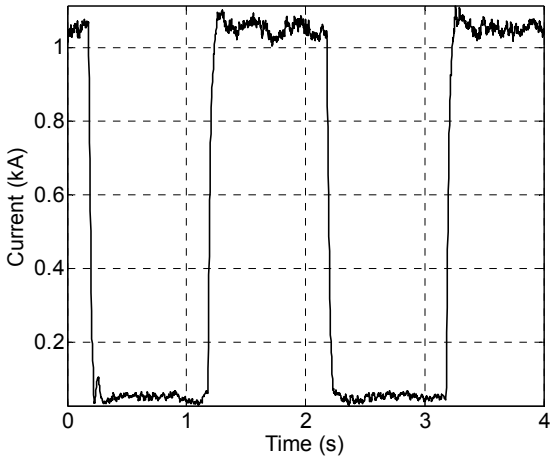

Figure 5 Pulsed Load Current Applied to the DUT

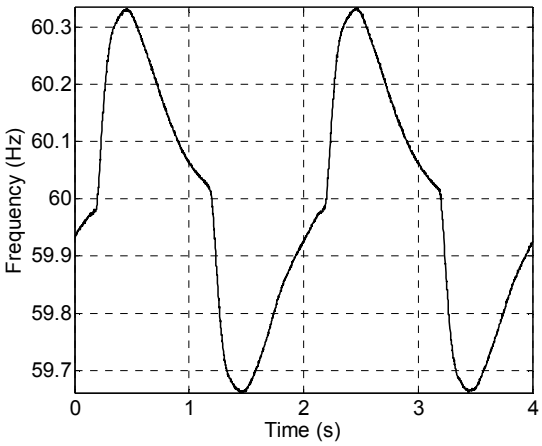

Figure 6 Frequency of Emulated Generator in Response to Pulsed Loading of DUT

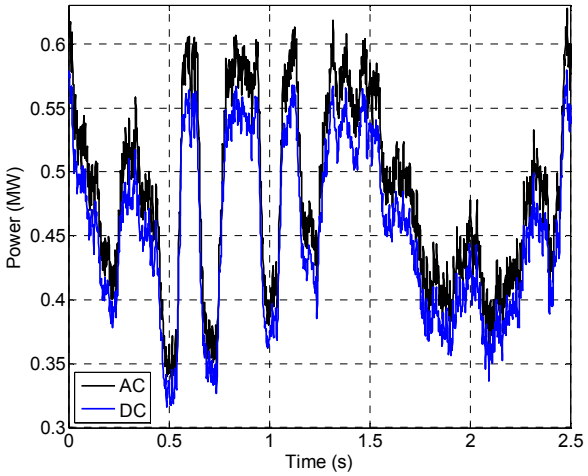

Figure 7 AC and DC Power at the Terminals of the DUT for Randomized Pulse Load

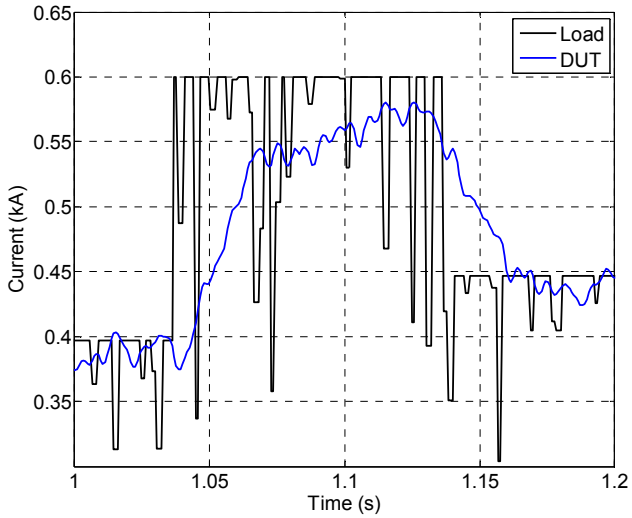

Figure 8 Currents on Primary and Secondary Sides of Large Load Model DC /DC Converter for Randomized Pulsed Load

However, although the testing yielded a large volume of useful results, the progression was not without challenges. One of the notable challenges encountered early in the testing was an instability issue when employing the large DC load model, representative of a load with a DC/DC converter. While the DC PHIL interface had been fully engaged for tests with the constant power, current, and impedance load models, oscillations were noted when engaging the voltage feedback of the current-type ITM interface with the large load model. The large load model is a simulated converter with its own controller bandwidth and input impedance, while the other load models directly interface these load characteristics to the 1 kV DC bus. The oscillations encountered with the large load model are illustrated by Figure 9, which shows the current at the DC terminals of the DUT at 400 kW constant loading and

75% voltage feedback. The magnitude of these oscillations increased with increasing voltage feedback, and would likely have resulted in tripping of the experiment at full voltage feedback. Subsequent simulations showed that this instability arose from the combination of the PHIL interface (including the delays in the amplifier) with the large load model.The oscillations were not observed when simulating the large load model directly connected to the simulated PCM, but these were observed when the model of the PHIL interface was included in the simulation. In order to achieve stability, the ITM interface algorithm (IA) was replaced with a current-type implementation of the DIM IA [5], [6]. The DIM IA is a generalization of the ITM IA, employing both voltage and current feedback, along with a damping impedance (in this case a resistance). As the current-type DIM IA approaches the ITM IA as the damping impedance approaches zero, an attempt was made to reduce the damping impedance as much as possible, while keeping the value large enough to avoid oscillations. Results for the same test with the DIM IA with full voltage and current feedback are illustrated by Figure 10, in which the oscillations have been mitigated. This allowed testing to proceed with the large DC load model.

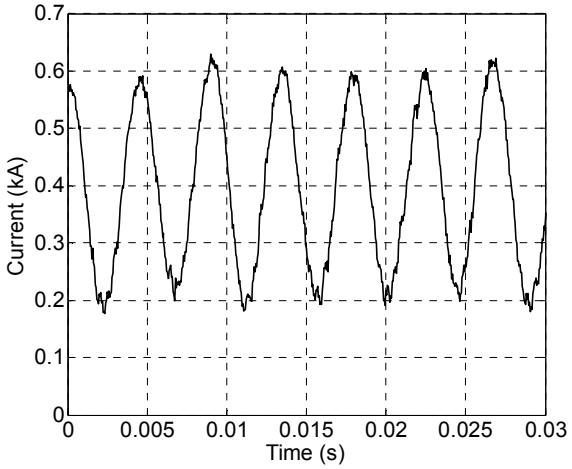

Figure 9 Oscillations in DC Current with 75% Voltage Feedback with ITM IA and Large Load Model

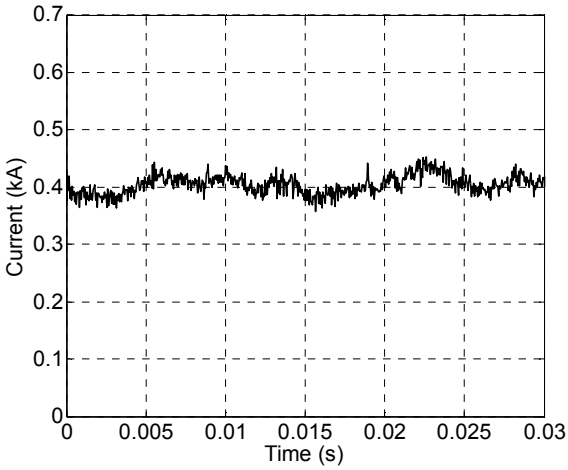

Figure 10 DC Current with Feedback Fully Engaged with DIM IA and Large Load Model

Instability issues were also encountered with the AC PHIL interface when testing at low load using the generator set model as the AC source. This is illustrated by the sustained oscillations that appear in the AC currents following a step load rejection, as illustrated by Figure 11. Although the ITM algorithm generally exhibits high accuracy, it is susceptible to stability problems [4]. As a solution, the voltage-type DIM IA was employed as a substitute for the ITM IA in order to stabilize the case. For this variant, the DIM IA includes, in parallel to the current injection at the terminals of the surrounding system, a voltage source with series resistance (the damping impedance). Thus, this approaches the ITM IA as the damping impedance approaches an open circuit. Ideally, very little current should flow into the branch with the voltage source, and the total simulated current into the interface should closely match the current measured into the DUT. Initially, an overly conservative value was chosen for the damping impedance, and, while stable, comparison of the currents on the hardware and simulated sides of the interface showed large discrepancies following the load rejection event, as illustrated by Figure 12. However, increasing the damping impedance value substantially reduced the deviations between the actual and simulated currents while avoiding the oscillations, as illustrated by Figure 13. This represented a tradeoff between stability and accuracy, but again allowed PHIL testing to proceed in regions that exhibited unstable behavior with the ITM IA. Other techniques, such as the modified DIM IA [4], [8], [9], for which the damping impedance is continually adjusted based on the measured impedance of the DUT, could possibly be used to further improve the accuracy. While this approach was not employed in these tests, this is a method of consideration for improvement of the approach for potential future tests of PCM units.

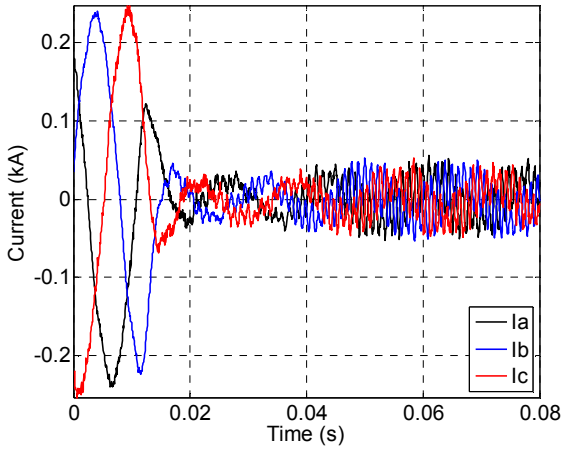

Figure 11 Oscillations in AC Current Following a Step Load Rejection with the Generator Model Using DQ-Based ITM IA

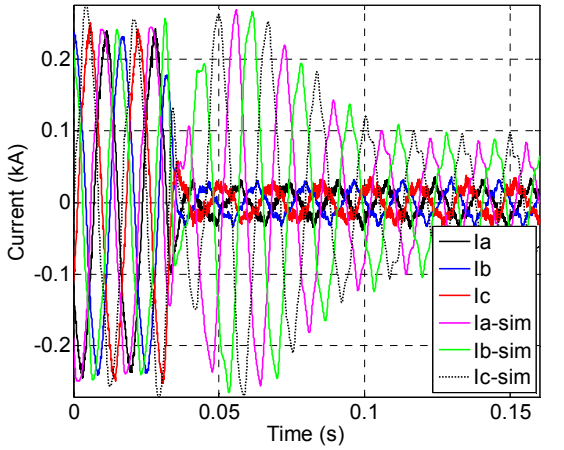

Figure 12 Poor Agreement Between Simulated and Measured AC Current Following a Step Load Rejection with the Generator Model Using DQ-Based DIM IA

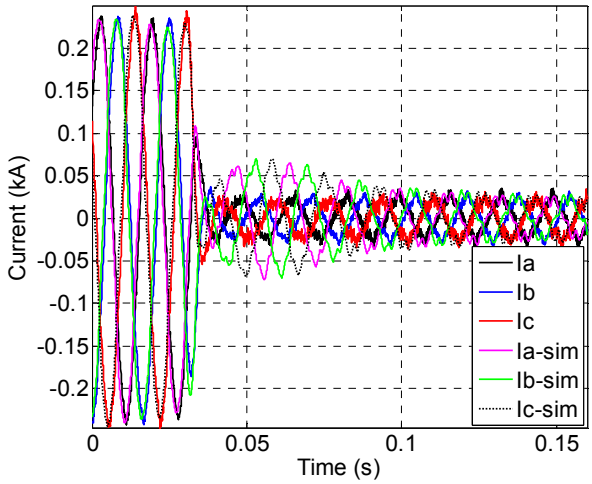

Figure 13 Improved Agreement Between Simulated and Measured AC Current Following a Step Load Rejection with the Generator Model Using DQ-Based DIM IA with Increased Damping Impedance

Another issue that arose in testing was the persistence of a low frequency (≈ 0.5 Hz) oscillation in the load current of approximately 50 A magnitude when operating with the simulated PCM in parallel with the DUT. This is illustrated by Figure 14, showing the current from the actual DUT swinging against the current from the simulated PCM. In this situation, the power through each of the PCM units oscillates, but the net load on the simulated generator, which supplies both PCMs, remains approximately constant. A number of tests were conducted to attempt to isolate the cause of the oscillation, and determine if it was an actual current sharing issue or simply an artifact of the PHIL interface. Although the root cause of the oscillation was not ultimately determined, the magnitude of the oscillation did not seem to be dependent on operating conditions. Because the oscillation was of low frequency and the magnitude of the oscillation did not change appreciably with power level, the planned tests were carried out with the oscillation present.

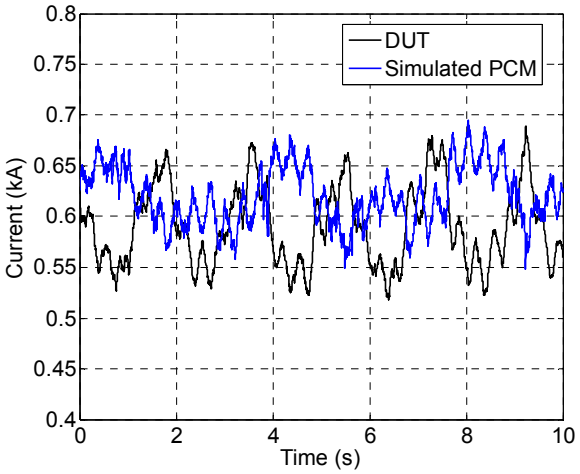

Figure 14 Oscillations in DC Current when Operating with Simulated Parallel PCM

V. CONCLUSION

Herein, the planning and execution of PHIL testing of a megawatt-scale AC/DC power conversion module has been described. This testing was very successful in providing a large volume of data for characterization of the DUT, demonstrating and exploring the performance of the DUT, and exploring a range of potential issues that may surface in integrating the PCM with a shipboard power system. However, through this testing process, a number of challenges were encountered, including instability issues with the ITM IA in some regions of operation. The DIM IA was employed as a method to stabilize the system, but the importance of scrutinizing accuracy was noted. The potential to improve results for future tests using variants of the DIM IA was also noted. A significant portion of the large volume of results from these tests is still being analyzed at the time of writing. Further, as noted in the introduction, it is anticipated that some of the PHIL experiments will be repeated with the DUT in a hardware-only test bed to provide additional information for evaluation of the accuracy of the PHIL experiments. The availability of data from consistent experiments in both PHIL simulation and hardware-only environments at such power levels is truly rare, making the outcome of this test program of particularly high value in the context of assessment of the PHIL simulation approach.

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