



A 21st Century Approach to Electronic Device Reliability

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A 21st Century Approach to Electronic Device Reliability
AFOSR MURI PROGRAM FA9550-08-1-0264

University of Florida, Mark E. Law, PI

Abstract

Lifetime prediction for device operation has usually relied on accelerated testing at elevated temperature and then extrapolation back to room temperature operation. This technique frequently fails for scaled, high current density devices found in modern technologies. Device failure is driven by electric field or current mechanisms or low activation energy processes that are masked by other mechanisms at high temperature. Device degradation can be driven by failure in either active structures or passivation layers. We have seen that many issues have an affect on compound semiconductor performance and reliability, including the material quality, strain state, surface cleaning process, and the actual voltage and current conditions during aging.

We have conducted comprehensive plan of reliability engineering for III-V device structures. This includes materials and electrical characterization and reliability testing. These techniques were utilized to develop new simulation technologies for device operation and reliability. This allows accurate prediction not only of reliability, but the ability to design structures specifically for improved reliability of operation. Our intensely integrated approach of utilizing new characterization methods, device simulations and realistic device stressing and aging provided new insights into device failure mechanisms.

1. Reliability Test Station

In order to accomplish the goal of creating new methods for optically and electrically characterizing and stressing semiconductor devices, an in-house design from readily available, off-the-shelf parts such as power supplies and data-acquisition and control equipment was created. The system was designed for maximum flexibility in order to provide long term voltage/current/temperature stress testing, characteristic IV plots, gate pulse testing and also incorporated laser and shutter control for optical pumping from different laser sources. DC-stress test measurements are taken every second and stored at a user-defined interval (minimum of a second) in a SQL database for future analysis, whereas characterization tests require data points to be measured and stored. An intuitive and accessible user interface is necessary for any level of flexibility. I-V plots, shown in Figure 1, and DC stress results, shown in Figure 2, are displayed graphically and in real-time. Details of this system design can be found in [Cheney 2012] (available on-line at <http://ufdc.ufl.edu/UFE0044885/00001>).

High-speed, high-voltage configuration

The high-speed, high-voltage variation shown in Figure 3 displays the hardware, comprised of two power supplies, a pico-ammeter, and a USB oscilloscope. This combination of the different commercially available off-the-shelf instruments creates a robust system with accurate measurement, large bias-voltages, and high-speed measurement.

All voltage measurements are made directly by the USB oscilloscope and can handle voltages as high as ± 80 volts. During long term DC stress tests, the system samples every second so it takes advantage of the higher precision 16-bit sampling. This wider sampling precision is also applied during characterization measurements since the sample speed is dependent on how quickly the power supplies can sweep voltages and not on sample-rate of the measurement. When performing gate-lag tests with a narrow gate pulse (1 μ s), the USB scope samples at the maximum speed (up to 50MHz) using the reduced sample precision to 12 bits. The 50MHz sample rate enables the gate pulse widths to decrease by orders of magnitude into the nanosecond pulse width range.

Long-term test configuration

The long-term test set can stress four devices at a time. This setup does not have all the capabilities of the high-speed, high-voltage set, lacking high-voltage gate control with a ± 10 volt range and also the data acquisition is limited to 50k samples per second. Figure 4 shows the hardware, comprised of an Instek DC power supply for the drain bias, a National Instruments (NI) analog output module serving as the gate bias supply, an NI high-voltage input module (± 60 volt) that measures the drain voltage, and an NI input module to read gate voltages, gate current and the drain current measurement.

Optical pumping configuration

The optical pumping station, shown in Figure 5, has a unique requirement to stream continuously at high speeds. This requirement precludes the data acquisition equipment in the long-term station because the TDM sampling is too slow. The USB oscilloscope in the high-speed, high-voltage station is not able to stream continuously and sacrifices too much precision to sample fast enough. The compromise is the NI USB-6366 that has 16-bit simultaneous

sampling up to 2 MHz. It uses the Instek power supply as the drain bias source. The NI USB-6366 has digital output controls that are used to switch shutters on the different lasers.

Probe station configuration

The probe station, Figure 6, is a version of the high-speed, high-voltage configuration without the gate pulsing capabilities, using a USB oscilloscope for data acquisition. The voltage inputs V_D and V_G are connected to probes on a probe station, allowing unpackaged parts to be tested on the system.

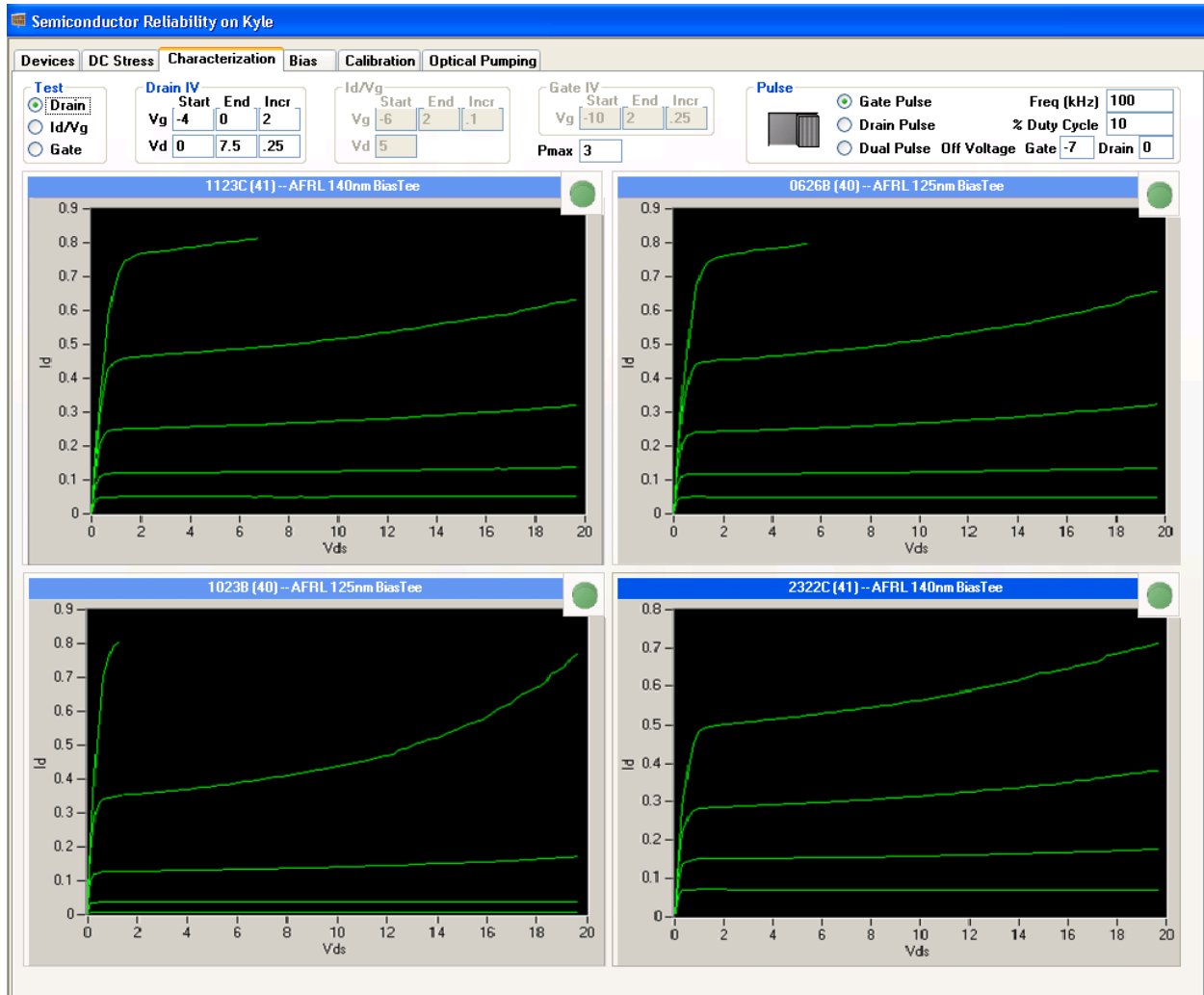


Figure 1 Software user interface showing I-V plots

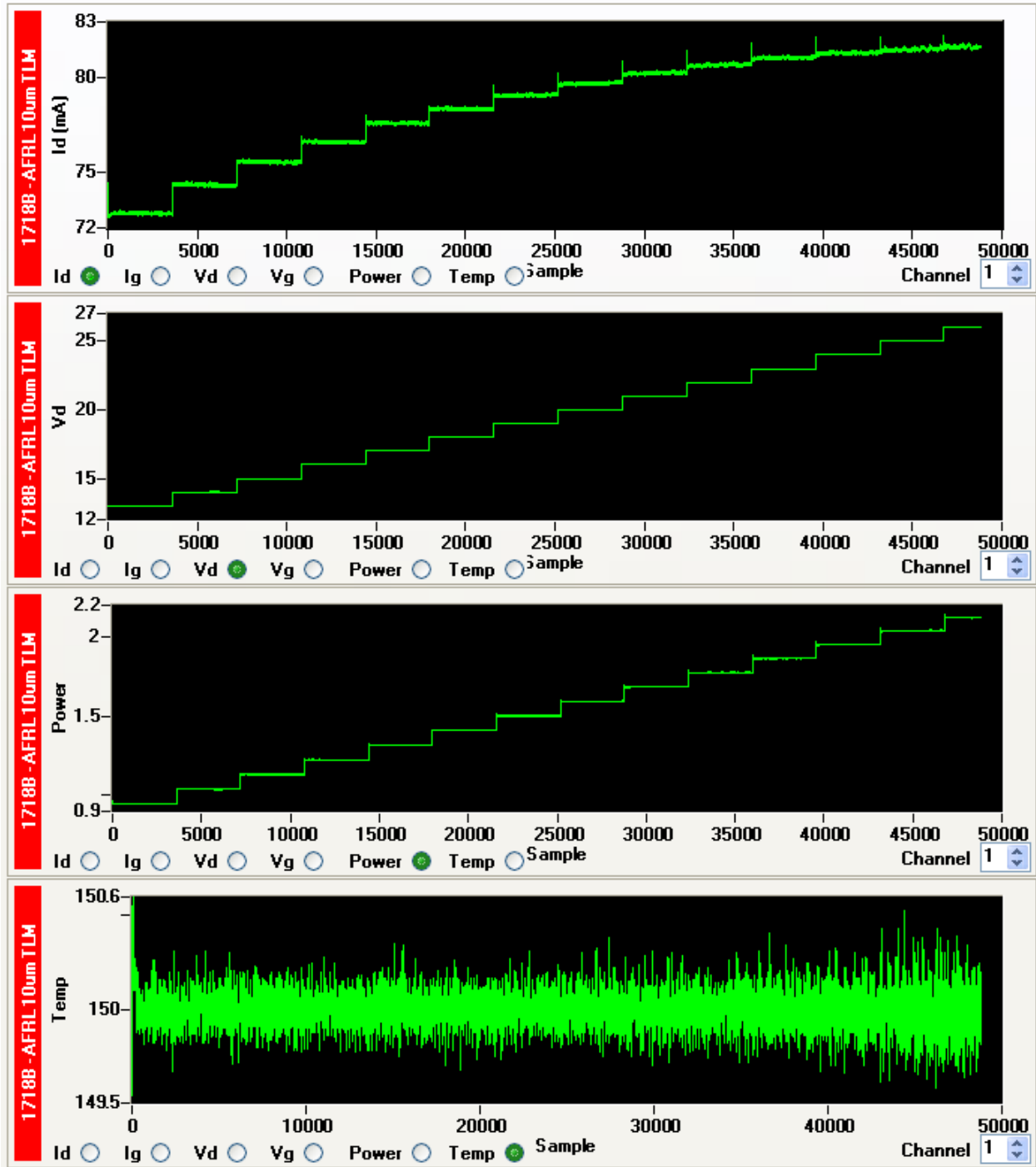


Figure 2. Software GUI showing DC stress

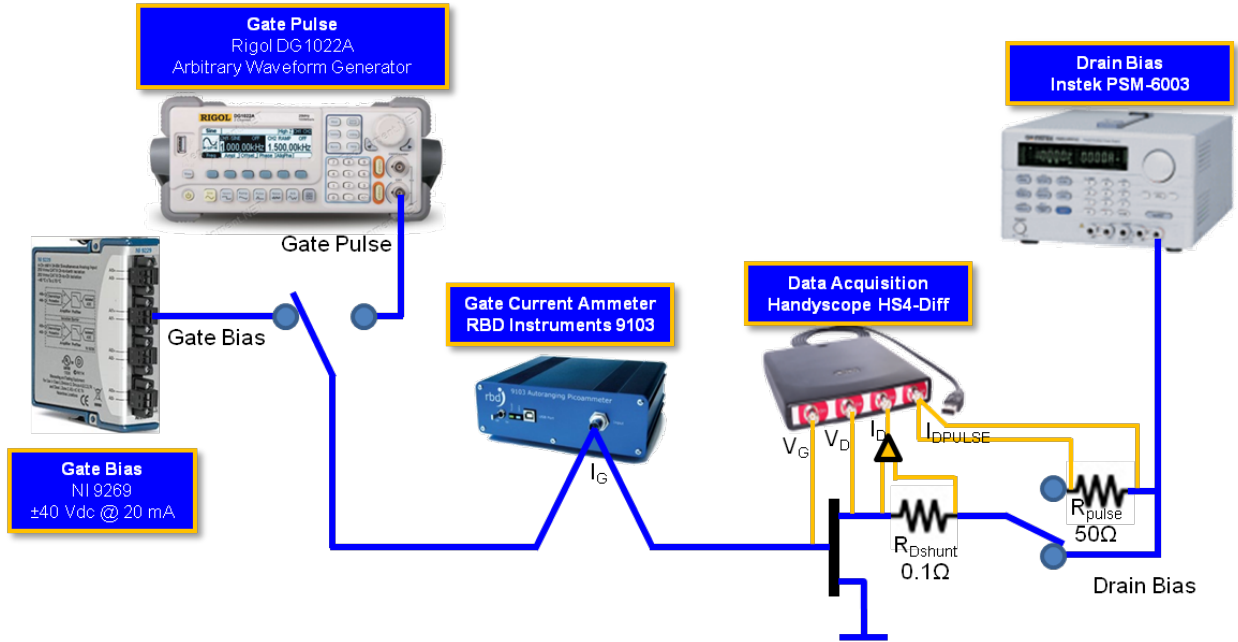


Figure 3. High-speed, high-voltage test station

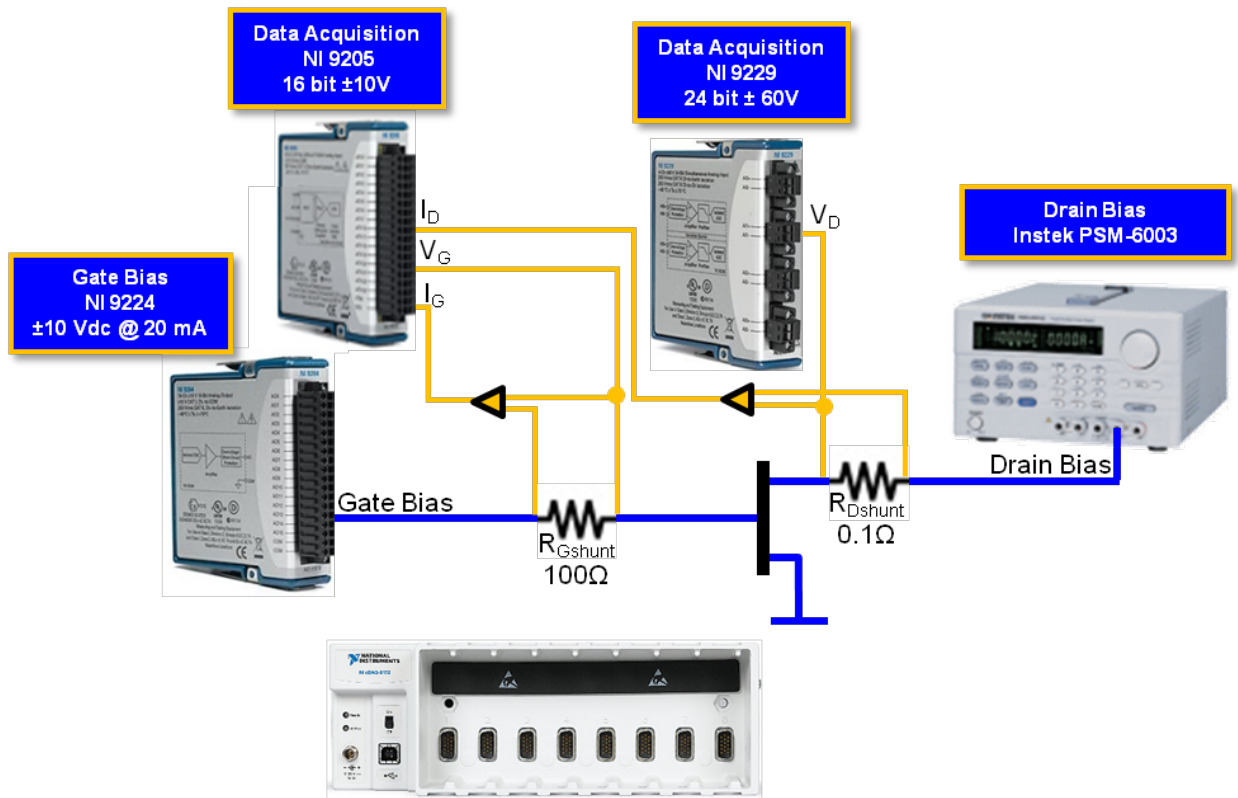


Figure 4. Long term test station

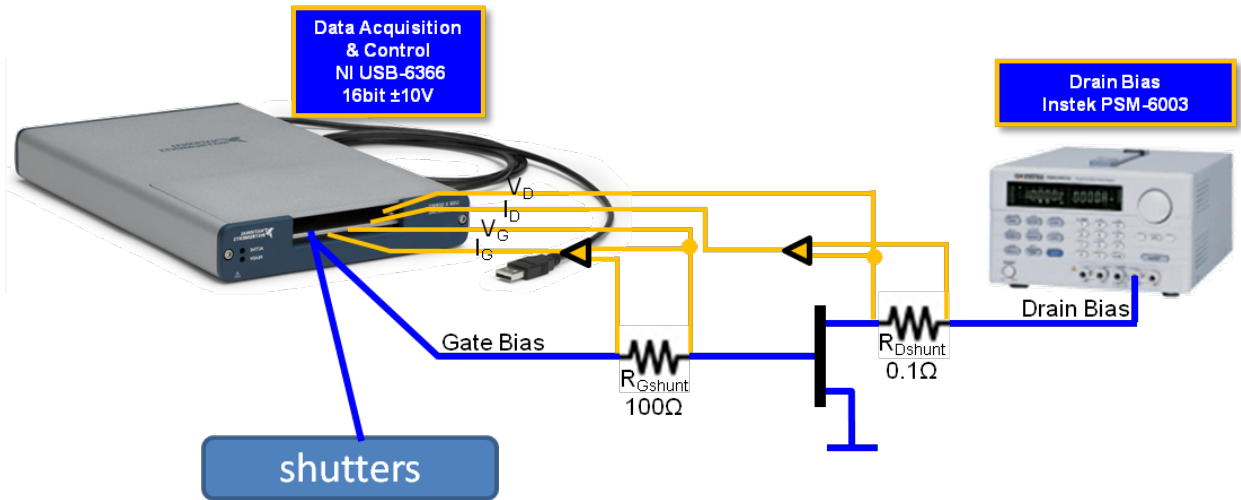


Figure 5. Optical pumping configuration

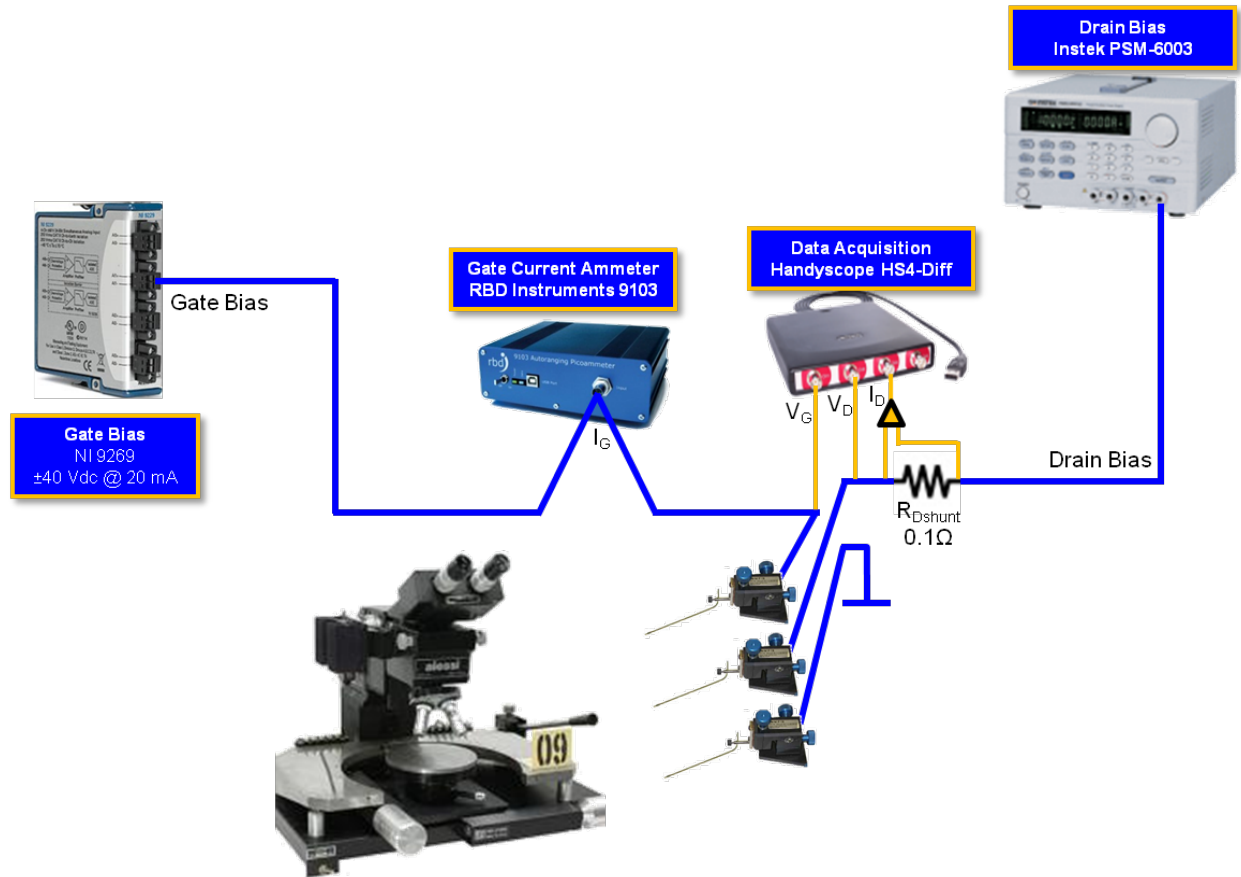


Figure 6. Probe station configuration

Section 2. Device Testing – bias and temperature stressing

Devices from two different vendors were used in this study. Eighteen HEMTs and six transmission line modules (TLM) from the Air Force Research Labs (AFRL) underwent accelerated aging. In addition, there were two devices from an undisclosed vendor, called vendor A.

AFRL Devices

The HEMT layer structures used in these experiments were grown by metal-organic chemical vapor deposition (MOCVD) on 6H SiC semi-insulating substrates with an unintentionally doped 3nm GaN cap, 15nm Al_{0.28}Ga_{0.72}N barrier and 2.25μm Fe-doped GaN buffer. Plasma enhanced chemically vapor deposited SiN was used for device passivation. The HEMTs had dual submicron Ni/Au gates with dimensions of 0.125, 0.14 or 0.17 x 150 μm. The HEMTs employed a Ti/Al/Ni/Au Ohmic metallization with a gate periphery of 300 μm, source-to-gate and gate-to-drain distances of 2 μm with SiN_x passivation. The devices were packaged and wire-bonded for testing. The initial quality of the devices varied widely, with less than 20% actually being suitable for stressing post-packaging. Pre-stress device screening removed parts whose gate leakage was above 0.5 μA or with drain leakage more than 500 μA.

The devices underwent accelerated aging by DC-stressing at 150°C at three different bias points along the one-watt load curve, shown in Figure 7: $V_G = 0$ (on-state), $V_G = -2$ (semi-on), $V_G < V_{TH}$ (off-state). The bias points were chosen with the expectation of devices stressed in the on-state mostly experiencing stress on the channel, while gate defects would manifest themselves as V_G approaches pinch-off and V_{DG} approaches the device's critical voltage [del Alamo 2009]. Devices that are biased between the on-state and off-state experience stress on both the channel and the gate. Since a gate bias of $V_G = -2$ is closer to the operating point of a transistor in a circuit, and because this bias point has the potential to show more interesting results, most of the devices are stressed under this bias condition. To maintain a constant power-dissipation of one watt in the channel, V_D was adjusted based on the measured I_D , except in the off-state case, where V_D was set to constant voltage. The stress tests were interrupted when either a 10% change in the drain current or an order of magnitude change in gate current were observed.

The devices tended to fail in one of two ways, either an abrupt sharp drop in drain current ($\Delta I_D > 10\%$) or a gradual decline in this current. Figure 8 is representative of both types of degradation over time.

Abrupt failures

Table 1 lists the devices that failed abruptly. Figure 9 shows the typical characteristic results of a device that failed abruptly. The dc characteristics show little to no change as a result of the DC-stress test. This suggests the degradation observed was possibly due to contact degradation. Since contact failure has been shown to be temperature dependent [Meneghesso 2008] [Douglas 2011] and to further support the hypothesis that this is contact failure, the fluctuations in current reduced dramatically as the test base-plate temperature was lowered. At a lower base-plate temperature, the devices appear to behave normally, however, they do experience a second abrupt drop in channel current once stress continues.

Gradual failures

Table 2 lists the conditions and devices that displayed a gradual failure mechanism. Most all of the devices that did not exhibit the abrupt drop in current drop, tended to have a similar degradation pattern to that shown in Figure 8-B, with an initial drop in drain current for the first 10 minutes. This has been suggested as resulting from the device reaching a new steady-state as trapping and de-trapping reach equilibrium [del Alamo 2009]. In several of the devices, the current increased before gradually declining to the 10% threshold where the test stopped. Figure 10 shows the typical pre and post electrical characteristic I-V plots, which are indicative of permanent degradation. It is interesting to note that the gate pulse transconductance plot shows no change in the delta between pre and post stress. Only slight changes in reverse gate current were measured, thus there is no trap-assisted tunneling leading to leakage paths as a result of newly created traps in the AlGaN [del Alamo 2009] [Bouya 2008] [Kim 2009] [Zanoni 2012] [Douglas 2011-2].

Off-state tests

Table 3 lists the results of the off-state tests. These devices degraded similarly to the semi on-state devices with the exception of a substantial increase in the gate leakage current as the characterization data in Figure 11 shows.

Transmission line modules

Four different spacings were tested, as listed in Table 4. The TLM's showed no degradation until they reached a catastrophic bias voltage, completely destroying the structure. Three different 10 μ m TLMs were tested. The first structure underwent a step stress, increasing the voltage by one volt every hour. At 40V, the part was destroyed. To investigate time-dependencies, a second device was stressed at 38 V, two volts below the destructive level of the previously tested device. After 26 hours this structure failed catastrophically. There was no observed noisy Id data as seen in some of the HELT devices, leading to the conclusion that the gate metal structure is responsible for the abrupt failure mode for the HEMTs.

Discussion

When the gate has a bias voltage, the devices tended to degrade much more quickly than the devices stressed under on-state tests, which did not degrade as much but exhibited more obvious current fluctuations.

Because the HEMT's were tested while maintaining constant power dissipation in the channel, the drain voltage increased as the device degraded and the drain current decreased. The drain voltage continued to rise as the device degraded reaching a voltage between gate and drain as high as 17 volts ($V_{GS}=-2$ and $V_{DS} = 15$). The voltage did not exceed the critical voltage for these devices under reverse gate bias step-stress conditions previously determined [Douglas 2010]. Consistent with findings, the gate leakage current did not change. This is also consistent in other findings [del Alamo 2009] under on-state conditions where V_{DG} did exceed the devices off-state V_{CRIT} levels.

From these tests, it is also appears evident that the power dissipated in the channel does affect reliability, since both the devices tested under the on-state and the semi-on-state were tested at the same level of $P_{CH} = 1W$ and degraded very differently.

Vendor A Devices

A small population of devices were made available from an industrial vendor. Only a total of eight devices were available for testing and of those eight only one met the criteria of low gate and drain leakage currents. A second device was also tested although its initial gate leakage was considered high, 52 μA versus 1.9 on the first device.

Very little information was provided with the parts in terms of epi structure and growth method. The devices were AlGaIn/GaN with a similar structure as the AFRL parts: dual-finger gate whose width of 167 microns (gate width is unknown).

As a result of the lack of information the parts were stressed under on-state conditions ($V_G = 0$), where the drain voltage was increased by half volt per hour steps until the drain current decreased by 10% of the initial drain current or if the gate current increased by an order of magnitude.

Unlike the AFRL HEMTs which showed little current collapse while tested in the on-state, both vendor A devices showed substantial degradation as the drain voltage increased as outlined in Table 5. These parts experienced a minimal shift in the threshold voltage of nearly a quarter volt in the positive direction as shown in the I-V plots in Figure 12. Interestingly, the gate leakage current improved on both devices with a substantial reduction of 44 μA on device 2 and a micro-amp reduction on device 1.

Table 1. Summary of results for AFRL devices that failed the DC-stress test with an abrupt change in drain current. The values are the difference between the pre and post DC-stress test.

Device	Test State	Test Hours	ΔI_D (mA) $V_G = 0, V_D = 5$	$\Delta G_{m_{max}}$ (mS)	ΔV_{TH}	ΔI_G (μA) $V_G = -6$	Comment
2218C	On	68	-3	-3	-0.26	-0.12	Noise throughout the test
2318C	On	12	-4.5	1	0.05	-0.22	Noise begins after 7 hours
1330D	Semi-on	9	-11	-5	-0.14	-0.06	Noise T > 75°C
		6	-6	1	-0.19	3.5	
1622D	Semi-on	14	2	38	-0.11	25	I_D abrupt failure
2124C	Semi-on	23	-32	-4	0.09	0.2	I_D 8% decrease then abrupt failure
2218B	Semi-on	23.6	-15	0	0.01	0.07	I_D 7.5% decrease then abrupt failure Fully recovers in 3 days.
1131C	Semi-on	2.5	1	4	-0.04	0.06	I_D abrupt failure

Table 2. Summary of results for AFRL devices that did not fail or failed the DC-stress test with a gradual change in drain current. All devices were stressed in the semi-On state ($V_G = -2$). The values are the difference between the pre and post DC-stress test.

Device	Test Hours	ΔI_D (mA) $V_G = 0, V_D = 5$	ΔGm_{max} (mS)	ΔV_{TH}	ΔI_G (μA) $V_G = -6$	Comment
1330D	19.3	-24	-1	-0.03	0.13	Noise T $\leq 75^\circ C$
	10	NA	NA	NA	NA	Minimal
2224C	14.7	-84	-24	0.35	0.36	I_D 10% decrease
2126D	13	-21	-20	0.27	0.61	I_D 25% decrease
	3	-67	-18	0.13	0.05	I_D 30% decrease
	8	-53	-17	0.23	0	I_D 40% decrease
2419C	3.2	-64	-11	0.62	0.46	I_D 10% decrease
1623C	65	-7	-1	0.01	1.8	Minimal
2220C	46.6	-35	-8	-0.02	0.09	I_D 10% decrease
2220B	46	-29	-5	0.15	0.003	I_D 10% decrease
2124C	23	-32	-4	0.09	0.2	I_D 8% decrease then abrupt failure
2218B	23.6	-15	0	0.01	0.07	I_D gradual 7.5% decrease then abrupt failure Fully recovers in 3 days.
1125C	3.67	-46	-13	0.08	0	I_D 10% decrease
1126C	13.3	-39	-8	0.11	0.06	I_D 10% decrease

Table 3. Summary of results from off-state ($V_G < V_{TH}$) DC-stress tests of AFRL devices. The values show the change as a result of the DC-stress test.

Device	Test Hours	ΔI_D (mA) $V_G = 0, V_D = 5$	ΔGm_{max} (mS)	ΔV_{TH}	ΔI_G (μA) $V_G = -6$	Comment
2320D	15.75	-18	-4	0.17	1	I_G doubles in 6.75 hours
1930C	4.4	-58	-11	0.46	-725.9	Very high gate leakage
1128C	10.2	-20	-6	0.02	48.25	$V_G = -7$, $V_{D \text{ step } 1hr} = 15 \text{ to } 16$

Table 4. DC-stress bias conditions for AlGaIn/GaN TLMs supplied by the Air Force Research Labs. All devices failed catastrophically.

Device	T _{BASEPLATE} (°C)	Spacing (μm)	TTF (hours)	V _{FAILURE} (V)	E _{@FAILURE} (kV/mm)
2213B	Room	5	8.25	15	3
1718B	150	10	33	40	4
0629B	150	10	26.6	38	3.8
1627B	150	10	9.8	38	3.8
2211B	Room	15	2.4	30	2
2219C	Room	20	6.5	45	2.25

Table 5. Summary of results from on-state (V_G = 0) DC step-stress tests of vendor A devices. The values show the change as a result of the DC-stress test.

Device	Test Hours	ΔI _D (mA) V _G = 0, V _D = 5	ΔGm _{max} (mS)	ΔV _{TH}	ΔI _G (μA) V _G = -6	Comment
1	41.2	-34	-7	0.25	-1.47	I _D gradual 15% decrease
2	34.4	-55	-16	0.31	-44.2	I _D gradual 10% decrease

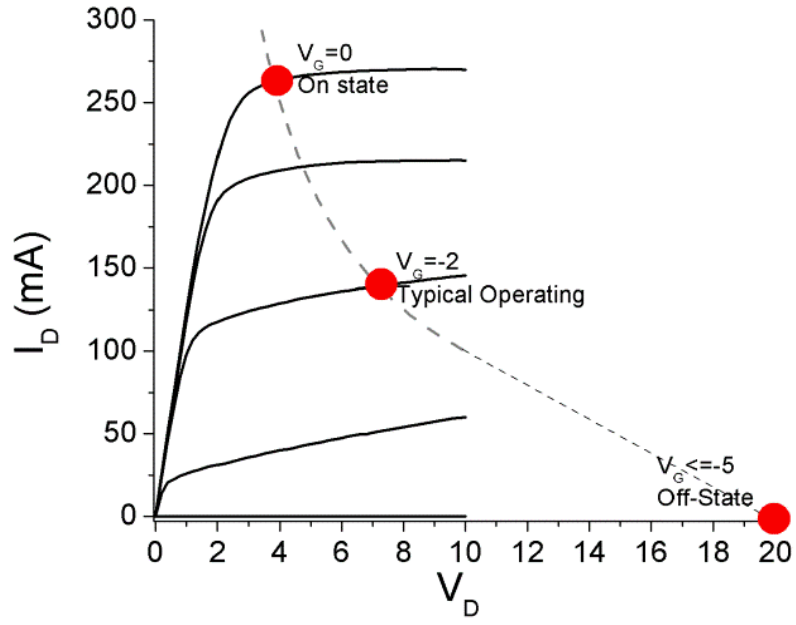


Figure 7. Load line test conditions for AlGaIn/GaN HEMTs.

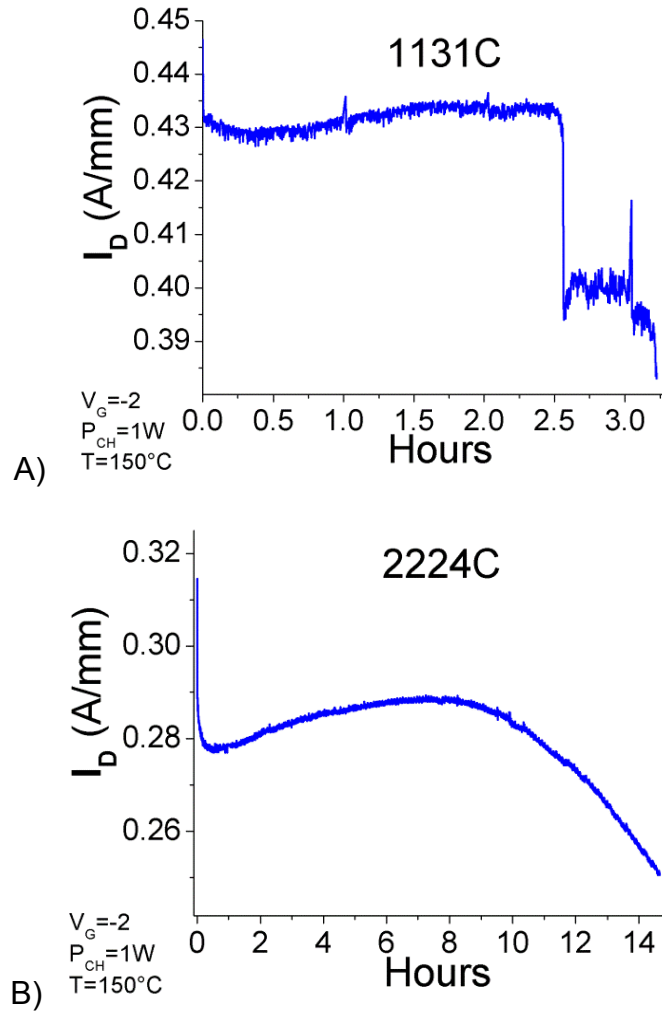


Figure 8. Typical degradation patterns for stressed devices. A) A device that has an abrupt drop in drain current. B) The gradual device degradation over several hours.

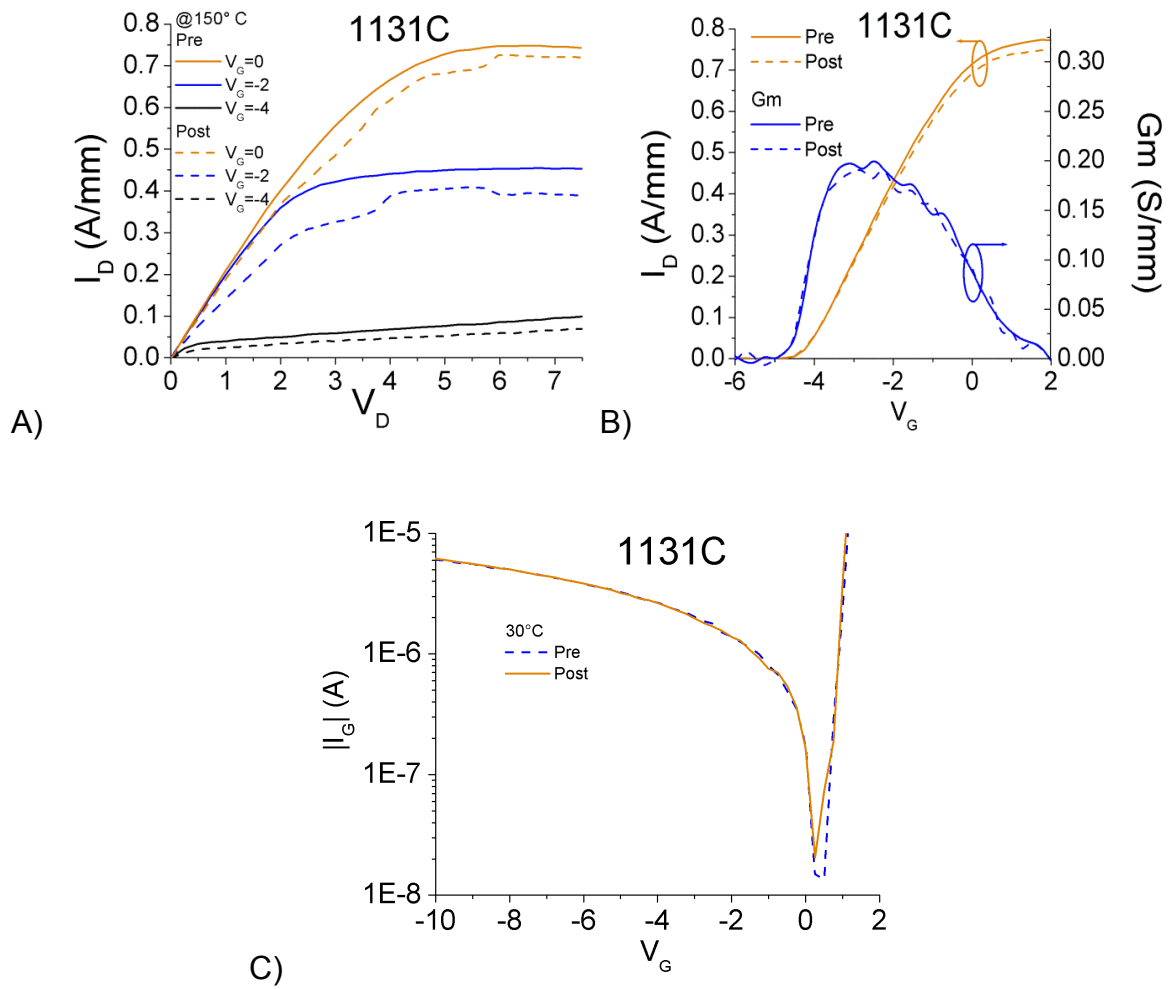


Figure 9. Typical pre and post characteristic curves for devices that fail abruptly. A) The drain I-V plot. B) The transconductance plot. C) Gate I-V plot.

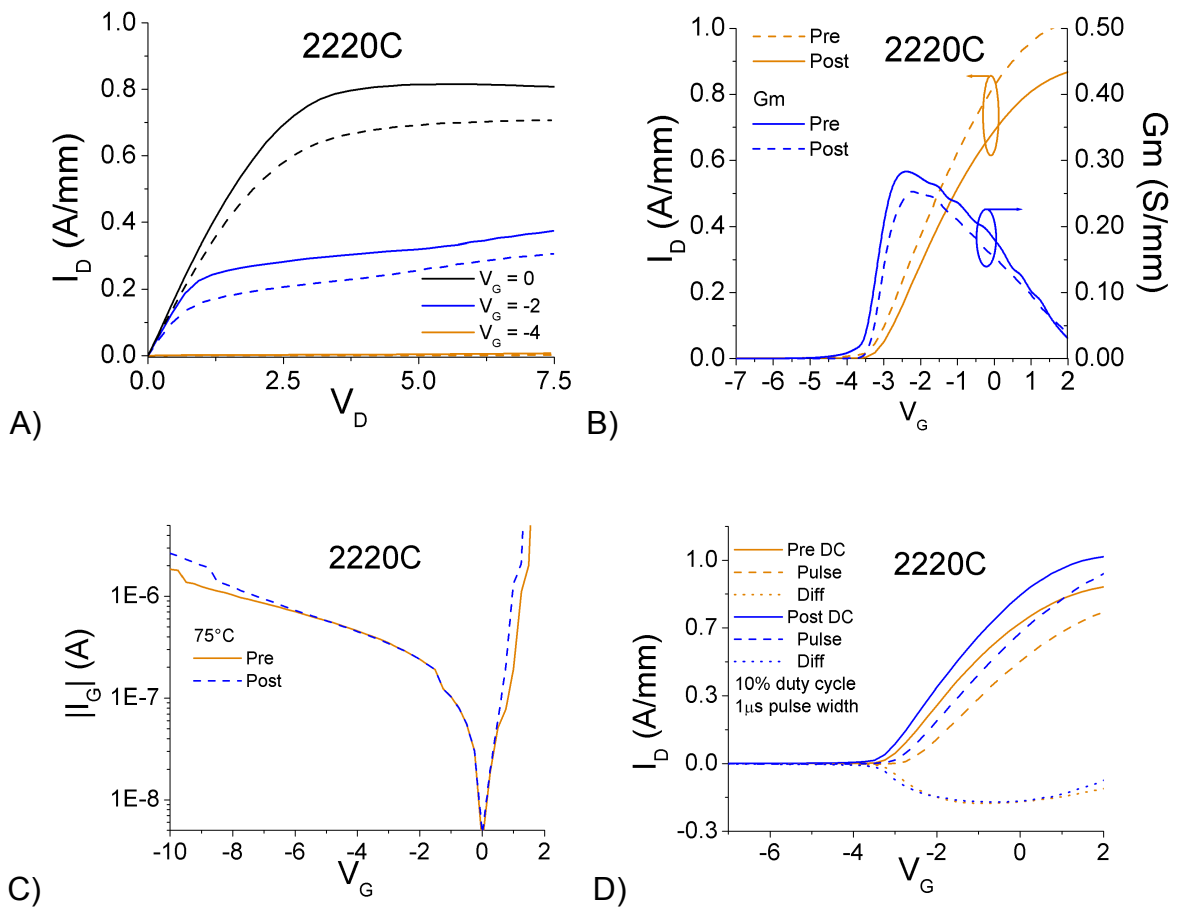


Figure 10. Typical pre and post characteristic curves for devices that fail gradually. A) Drain I-V plot. B) Transconductance plot. C) Gate I-V plot. D) Pulse Transconductance plot

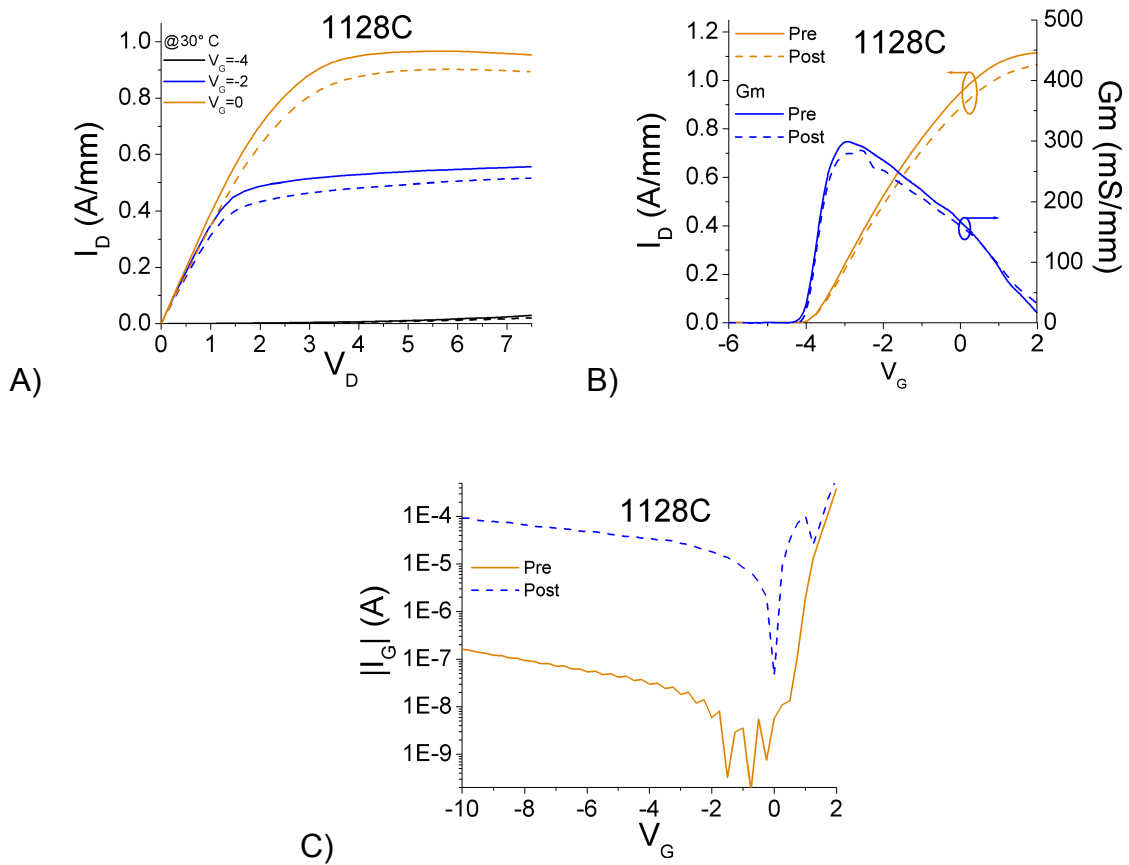


Figure 11. Typical pre and post characteristic curves for devices that underwent DC-stress in the off-state ($V_G < V_{TH}$). A) Drain I-V plot. B) Transconductance plot. C) Gate I-V plot.

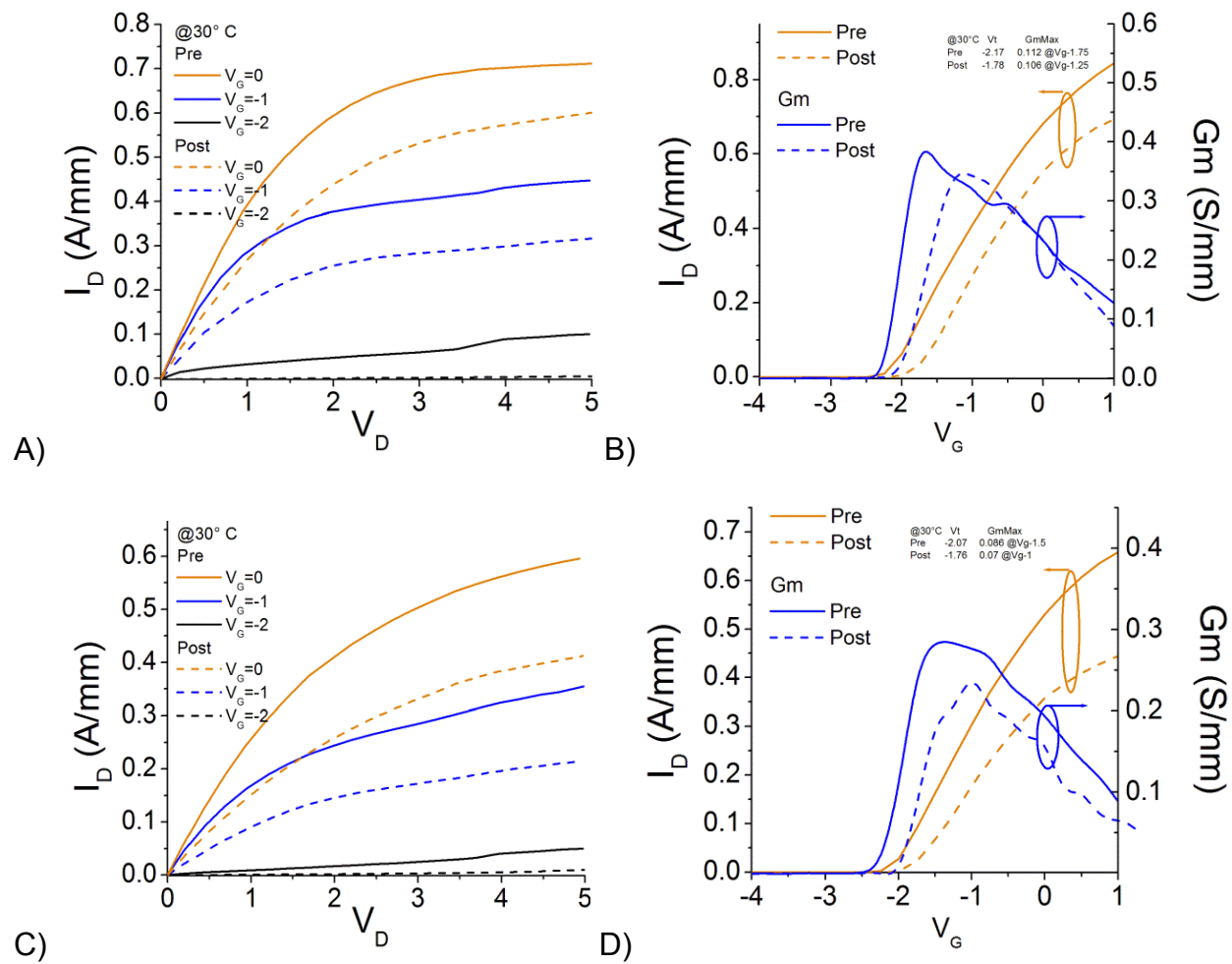


Figure 12. Pre and post characteristic curves for Vendor A devices. A) Device 1 drain I-V plot. B) Device 1 transconductance plot. C) Device 2 drain I-V plot. D) Device 1 transconductance plot.

Section 3 - Degradation Mechanisms in GaN HEMTs

Gallium Nitride based high electron mobility transistors (HEMTs) have become attractive for use in high power and high frequency applications. GaN transistors offer both higher breakdown voltages as well as 2DEG density compared to their GaAs counterparts [meneghesso 2008]. As AlGaIn/GaN HEMTs are introduced in commercial and military applications, it has become critical for reliability studies to extend beyond the normal temperature-accelerated life tests. It is common to determine the failure rate at operating temperatures by extrapolating from the failure rate under thermally accelerated stress conditions through the Arrhenius equation but this does not capture failure mechanisms that are not accelerated by elevated temperatures. Employment of GaN HEMTs for high power radar systems requires devices to be subjected to large-signal RF while being driven into saturation, resulting in devices experiencing high electric fields and high current densities. Impressive mean-time-to-failure values of greater than 10^7 hours have been reported at operating temperatures below 200 °C, with activation energies ranging from 0.18 eV to 2 eV [sozza 2005, zanoni 2009]. However, these studies neglect the effect of high electric field and current on device lifetime. As the device design and material processing technology for AlGaIn/GaN HEMTs has matured over the years, several failure mechanisms that limited device lifetime have been addressed and improved. However, there are still numerous degradation mechanisms that have been reported to plague AlGaIn/GaN HEMTs. These mechanisms can be grouped together into three main categories that affect lifetime: contact degradation, hot electron effect, and inverse piezoelectric effect. Both Schottky and Ohmic contacts have shown excellent stability below 300 °C. Piazza et al. have reported an increase in contact resistance and passivation cracking due to Ga out-diffusion and Au inter-diffusion after a 100 h thermal storage test stress at 340 °C [piazza 2009]. Nickel based Schottky contacts have been shown to form nickel nitrides on GaN at annealing temperatures as low as 200 °C, resulting in a significant decrease in Schottky barrier height [chowdhury 2008]. The observed current collapse and gate lag under high voltage and high current operation have been attributed to hot electrons. Hot electrons are electrons that have been accelerated in a large electric field, resulting in high kinetic energy, which can result in trap formation. Creation of traps can occur in both the AlGaIn layer and the buffer, leading to reversible degradation of transconductance and saturated drain current [del Alamo 2009, Faqir 2008]. GaN is a piezoelectric material and under high bias conditions, the electric field induces additional tensile stress to the already strained AlGaIn layer. Upon reaching a “critical voltage,” irreversible damage to the device occurs resulting in defect formation through which electron leakage can occur [del alamo 2009].

(i) Hot-carriers and trap generation

Permanent device degradation after high V_{DG} stress under on-state conditions has been attributed to the presence of hot electrons. In GaAs- based devices, hot electrons generate holes which are accumulated by the gate and result in a negative shift in V_T [sarua 2006]. Typically, I_G is used to derive the field-acceleration laws for failure. Impact ionization in GaN HEMTs has been reported by some groups although high gate current can hamper its observation [vitusevich 2008]. The hot electrons likely lead to trap generation at the AlGaIn/GaN interface or at the passivation/GaN cap interface, leading to an increase in the depletion region between the gate and the drain and resulting in an increase in drain resistance and a decrease in I_{DSS} . Under off-state conditions, the degradation is greatly reduced due to the reduction of electrons present in

the channel. Sozza et al. showed that AlGaIn/GaN HEMTs that underwent a 3000 hour on-state stress resulted in an increase in surface traps with an activation energy of about 0.55 eV [sozza 2005]. Devices stressed under off-state conditions showed only a very small increase in traps density.

Meneghesso et al. employed electroluminescence (EL) to study the effect of hot-carriers and the dependence on stress conditions [meneghesso 2008]. Uniform EL emission due to hot electrons was observed along the channel for devices stressed at $V_{GS} = 0$ V and $V_{DS} = 20$ V, with no hot spots or current crowding. Under off-state conditions of $V_{GS} = -6$ V and $V_{DS} = 20$ V (resulting in a $V_{GD} = -26$ V), the EL emission from the channel was not uniform. These hot spots may be due to injection of electrons from the gate into the channel. Due to the high bias conditions, the electrons acquire enough energy to give rise to photon emission. This is a clear correlation between the gate leakage current degradation and the hot spots intensity.

(ii) Contact degradation

Contact degradation and gate sinking are significant degradation mechanisms at elevated temperatures in GaAs and InP based HEMTs. This has not yet proven to be a significant issue with AlGaIn/GaN HEMTs at temperatures below 400°C for Pt/Au Schottky contacts and Ti/Al/Pt/Au annealed Ohmic contacts. An increase in Schottky barrier height was observed for Ni/Au Schottky contacts after dc stress at elevated junction temperatures (200°C) [chang 2011]. This was due to a consumption of an interfacial layer between the Schottky contact and the AlGaIn layer, causing a positive shift in Schottky barrier height and pinch-off voltage but a decrease in I_{DSS} . Unstressed devices were subjected to annealing after the Schottky contact was deposited in to decrease the interfacial layer between the gate and semiconductor. Devices that underwent this gate anneal showed 50% less degradation during a 24 hour stress test as opposed to devices that did not receive a gate anneal. Thermal storage tests up to 2000 hours on Ti/Al/Ni/Au Ohmic contacts at and above 290°C showed an increase in contact resistance as well as surface roughness due to growth of Au-rich grains that ultimately led to cracks in passivation. The two primary degradation mechanisms were Au inter-diffusion within the metal layers and Ga out-diffusion from the semiconductor into the metallic compounds. Similar degradation was observed after dc stress tests that resulted in junction temperatures equivalent to the thermal storage tests. Due to the high power capability of AlGaIn/GaN HEMTs, proper temperature management is crucial in order to optimize device performance under high current and high voltage operation. Self heating of devices can ultimately result in poor device performance through contact degradation.

(iii) Inverse piezoelectric effect

Several groups have shown that high reverse bias on the gate results in a defect-generated path of gate current leakage [del Alamo 2009, meneghini 2012]. This defect formation mechanism has been ascribed to at four different mechanisms, including (i) inverse piezoelectric effect (ii) oxidation of the surface, with subsequent generation of pits [marko 2012] (iii) defect generation/percolation in the AlGaIn [lo 2011] and (iv) generation of point defects within the AlGaIn [douglas 2011, gao 2011]. Since GaN and AlGaIn are piezoelectric, the presence of high electric fields results in an increase in stress within these layers. AlGaIn is lattice mismatched to GaN, resulting in significant tensile strain, even in the absence of an electric field. If under electric stress the elastic energy within the AlGaIn/GaN layers surpasses a critical value, the strained layer will relax through crystallographic defect formation and these defects can be

electrically active and result in device degradation. The role of oxygen has been implicated by observing slower degradation rates under vacuum conditions. Negative charge creation in the AlGa_N and positive charge at the AlGa_N/Ga_N interface due to defects has been reported during reverse-biasing of HEMTs [chini 2009]. Permanent degradation occurred with generation of parasitic leakage paths due to a defect percolation process. These were observed during long stress times, where degradation can occur even below the critical voltage. There was an onset of noise in the gate current prior to the permanent degradation, which is consistent with defect creation and also the time to breakdown strongly depended on the initial defect density in the HEMT layers. Similarly, current deep level transient spectroscopy has observed creation of trap states with thermal activation energies of 0.5 eV from the conduction band in devices subjected to high reverse biases.

Joh et. al. [joh2011] have established that I_D and I_G degradation under high reverse gate bias occurs at a critical voltage, typically above 20 V on V_{DG} . This is also correlated with a sharp rise in both source and drain resistance and a positive shift in V_T . However, the critical voltage for devices can deviate substantially within one wafer [Johnson et al 2012, Tapajna et al 2011]. The density of hot electrons increases exponentially as the field increases and only linearly with current. Though stress experiments in the high power state have shown that increasing $I_{Dstress}$ does not significantly accelerate degradation, the critical voltage for reverse bias stress in which I_{Goff} dramatically increases is dependent upon the $I_{Dstress}$, as V_{crit} increases with increasing $I_{Dstress}$ [Douglas 2012]. The hot electrons are not the driving degradation mechanism for this stress condition. TEM cross sections after stressing with $V_{DS} = 40$ V and $I_{D0} = 250$ mA/mm at various base-plate temperatures corresponding to a junction temperature of 250 °C, 285 °C, and 320 °C showed that all stressed devices showed evidence of pit-like defects on the drain side of the gate. The depth of the pit was about 10nm, and remained within the AlGa_N layer. Crack-like defects were observed in a few of the stressed devices, and originated at the bottom of the pit defect, extending to the heterointerface of the AlGa_N/Ga_N layer and occasionally into the Ga_N buffer. As the junction temperature increased, the time after which the crack appeared decreased, developing within 6 hours at a temperature of 320°C. Gate metal was also observed to diffuse ~2nm into the defect crack. The formation of the crack was hypothesized by to originate in the deepest points in the defect pit and spread along the gate width, thus explaining the presence of cracks in very shallow defect pits [Jung 2009, Holzworth 2011, lui 2011].

Joh et al.[joh2011] have postulated that the converse piezoelectric effect is solely an electric field driven degradation mechanism due to the fact that it is the induced mechanical stress that results in the relaxation of the AlGa_N layer. The current should not drive this mechanism, except for indirect self heating that would accelerate degradation of the device. Device design that affects the profile of the electric field on the drain side of the gate will also, in turn, impact the critical voltage.

Sarua [sarua 2006] investigated the effect of piezoelectric strain in AlGa_N/Ga_N FETs under bias with micro-Raman spectroscopy. 2D finite element simulations showed that a pinched-off device at $V_{DS} = 20$ V resulted in a peak electric field on the drain side of the gate within the AlGa_N layer. However, the z component of the electric field extended down into the Ga_N layer. Fe doped Ga_N buffers layers raise the acceptor concentration and decreases the depletion width in the Ga_N buffer, confining the z component of the electric field to the AlGa_N/Ga_N interface. Self-heating will occur under high power stress conditions, which results in a compressive thermal strain/stress. It is possible that due to the mitigation of the piezoelectric stress by the

thermal stress, slower device degradation was seen in devices stressed under the high power state as opposed to off-state condition. This is in contrast to the hypothesis of del Alamo et al that higher temperatures will result in an acceleration of device degradation.

Other issues can lead to additional compressive and tensile strains on the underlying epitaxial layers, including SiN passivation, which is used extensively to minimize surface traps on the AlGaN surface. Mastro et al. reported the simulated effects of non-uniform strain due to SiN passivation [mastro2006]. Typically, SiN has a relatively small magnitude of stress as compared to the tensile strain present in the AlGaN layer due to lattice mismatch. The strain in SiN is highly dependent on processing conditions. When deposited on the device, variations and discontinuities can increase the stress fields. For instance, the opening at the edge of the gate metal will result in a force on the AlGaN which will be perpendicular to the gate edge and parallel to the surface of the AlGaN. It was predicted that as the gate length decreases, the magnitude of the strain fields increases. The reported mechanism for degradation of HEMTs include reactions of the gate or source/drain contacts with the underlying semiconductor, trap formation through hot electron injection and cracking or pitting at the gate edge due to the inverse piezoelectric effect. These give rise to various signatures, including additional noise, current changes and transients due to trap formation and pitting or other metal reactions.

DC Stress Testing

There are four basic stress conditions for HEMTs, as shown in Figure 13 (a). For each of these four conditions (on-state, off-state, high power and $V_{DS}=0$ state), the voltage or current can be increased in stepped fashion, a step-stress recovery cycle or step-recovery cycle, as shown in Figure 13(b). These protocols are used in place of increasing temperature to provide a more realistic estimate of the reliability under various operating conditions. The recovery cycle protocols are especially relevant if deep traps are created by the stressing, since that will lead to current transients. This can be manifested as exponential recovery waveforms and increased noise and gate leakage. To study the effect of high electric field on GaN HEMTs, off-state step-stresses were performed in the dark at room temperature with the gate biased up to -100 V reverse gate voltage at various source-drain biases. The effect of gate length, gate to source and gate to drain distance, as well as the effect of applied drain bias on breakdown was investigated on structure A. As the gate voltage is stepped in 1 V increments for 1 minute per step from -10 V to -42 V, gate leakage current in AlGaN/GaN HEMTs with Ni/Au-based gate metallization increased until the critical voltage (V_{CRI}) is reached, resulting in a permanent increase in gate leakage current of several orders of magnitude as well as a reduction in drain current (Figure 14). This sharp rise in current has been attributed to the inverse piezoelectric effect. Even though a large relative increase in gate current is observed after stress, this is accompanied by a small relative decrease (~20 %) in the drain current, due to an increase in on-state resistance. However, the change of the drain current in absolute value is larger than that of the gate leakage. Similarly, the transfer characteristics typically show a reduction in maximum transconductance of as a result of the gate bias stress cycle and a shift in threshold voltage.

Devices with sub-micron gate lengths ranging from 0.1 to 0.17 μm were step stressed from -10 V to -42 V in the same manner. The bias at which the sudden onset of high gate current was observed was strongly dependent on the gate length, as shown in Figure 15. While a linear dependence of gate length on V_{CRI} is observed, ATLAS/Blaze simulations confirm that degradation occurs at a critical maximum electric field in the channel, ~2.5MV/cm (Figure 16). This is consistent with previously published results indicating that failure is due to electric field

induced tensile strain. Photoluminescence (PL) of an ungated, open area of an unstressed HEMT showed that both the GaN peak centered at 366nm and the AlGaN peak centered at 352nm decreased in intensity after stressing. This degradation is indicative of the formation of non-radiative centers in both the GaN and AlGaN layers.

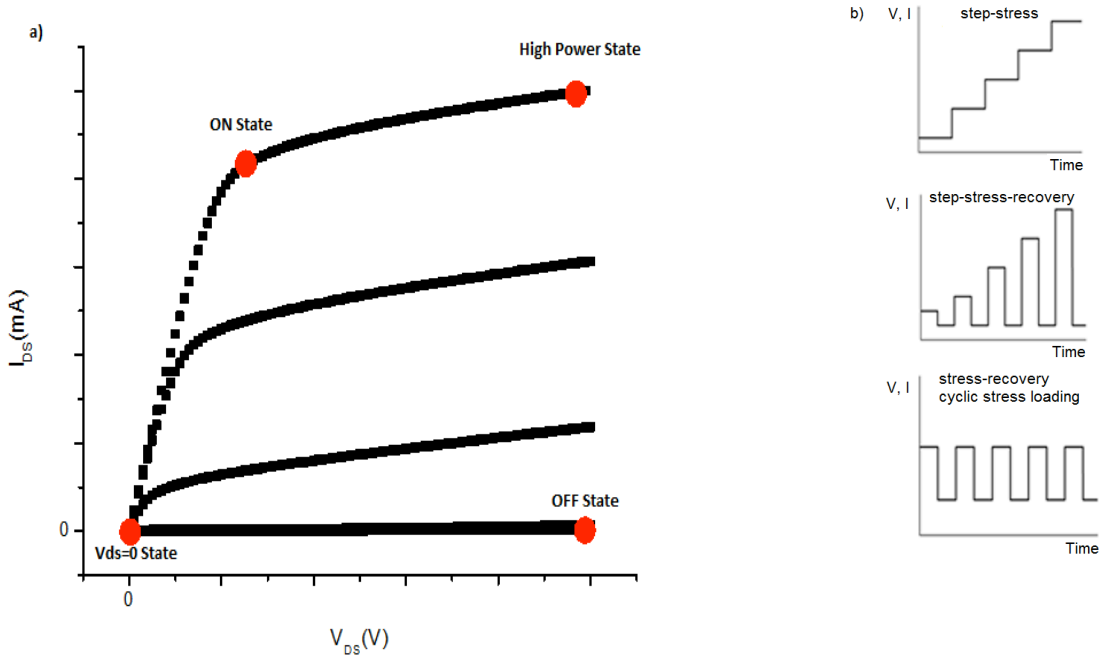


Figure 13. Schematic of (a) different biasing conditions for AlGaN/GaN HEMTs and (b) bias-stress protocols.

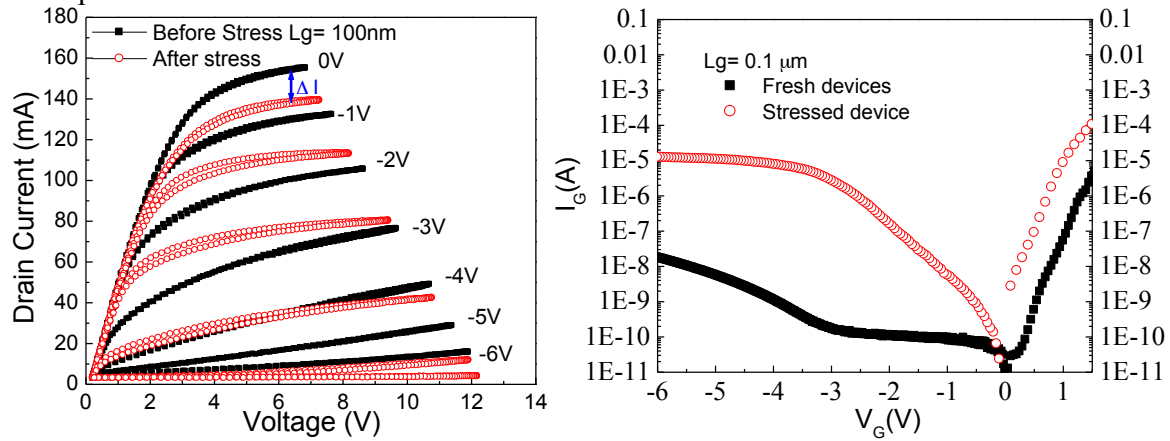


Figure 14. Drain current (top) and gate current (bottom)- voltage characteristics before and after high reverse gate bias step stress

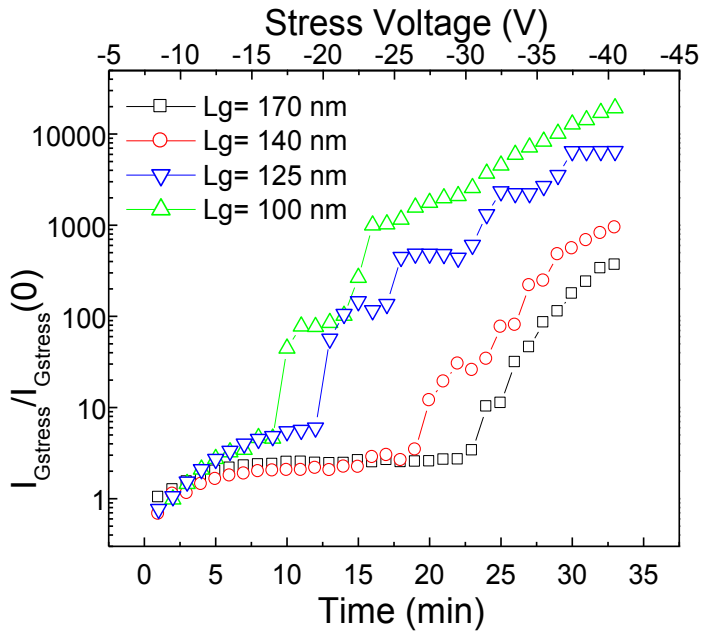


Figure 15. Gate stress current and stress voltage as a function of time for various gate lengths.

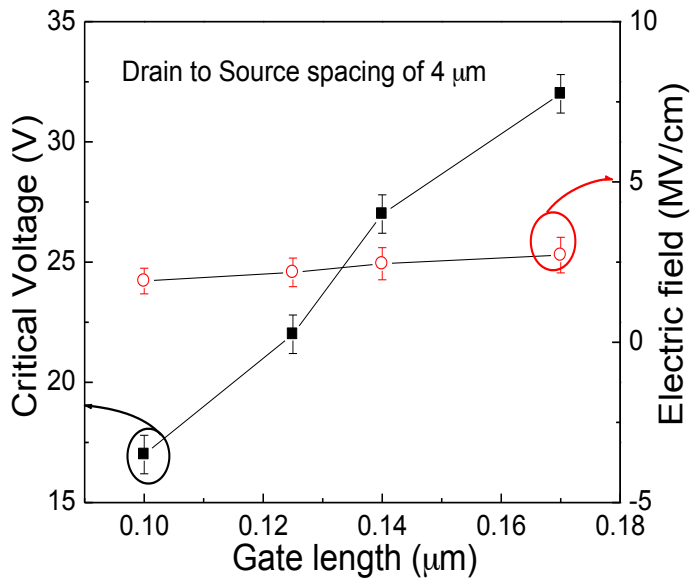


Figure 16. Dependence of critical voltage and electric field on gate length for AlGaN/GaN HEMTs

Field Plate

A source field plate over the gate electrode can increase device breakdown voltage by reducing the peak electric field at the drain side of the gate edge. This resulted in a significant increase in V_{CRI} from -40V to -65V [Iui 2011]. Figure 17 shows the typical step-stress results of more than 30 HEMTs with and without the source field plate; the gate current, I_g , has been plotted as a function of the stressed gate voltage. The devices were step stressed in -1 V increments for 1 min at each increment, while grounding the source electrode and maintaining +5 V to the drain. TEM images indicated the presence of Ni from the gate metal stack interacting with the underlying nitride layer in close proximity to a threading dislocation (Figure 18, top), while simulations using the Florida Object-Oriented Process Simulator (FLOOPS) showed that such metal diffusion can lead to a drop in I_D of at least 40% (Figure 18, bottom). A one-to-one correlation between the characteristics of I-V and gate leakage curves of electrically step-stressed AlGaIn/GaN HEMTs and the presence of specific microstructural defects in the gate region of each device could not be established for all devices studied. Inverse piezoelectric effects are often cited as the driving force for the evolution of gate-edge “pit” or V-shaped defects which are associated with dramatically increased leakage current but it is possible that gate metal diffusion into the barrier layer, which was observed in all samples, may also have some effect. The possible role of the thin and irregular oxide layer beneath the gate metal contact also remains to be determined. In addition, the threading dislocation density has been found to have a strong influence on the early degradation of HEMTs, with much more significant effects for high dislocation density.

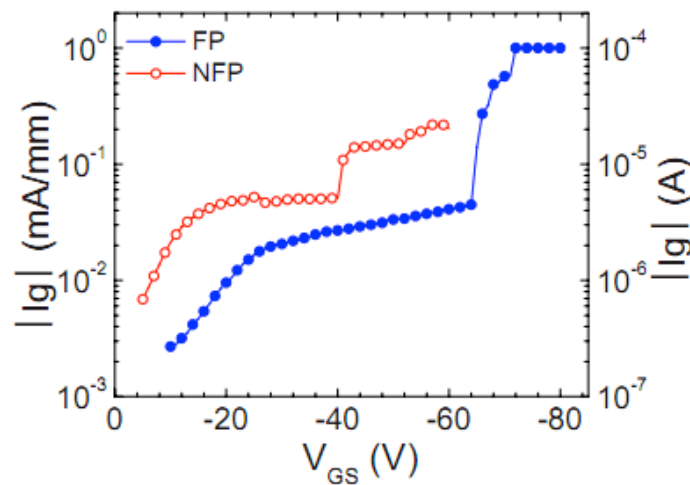


Figure 17. Off-state gate currents as a function of V_{GS} for HEMT with (FP) and without source field plate

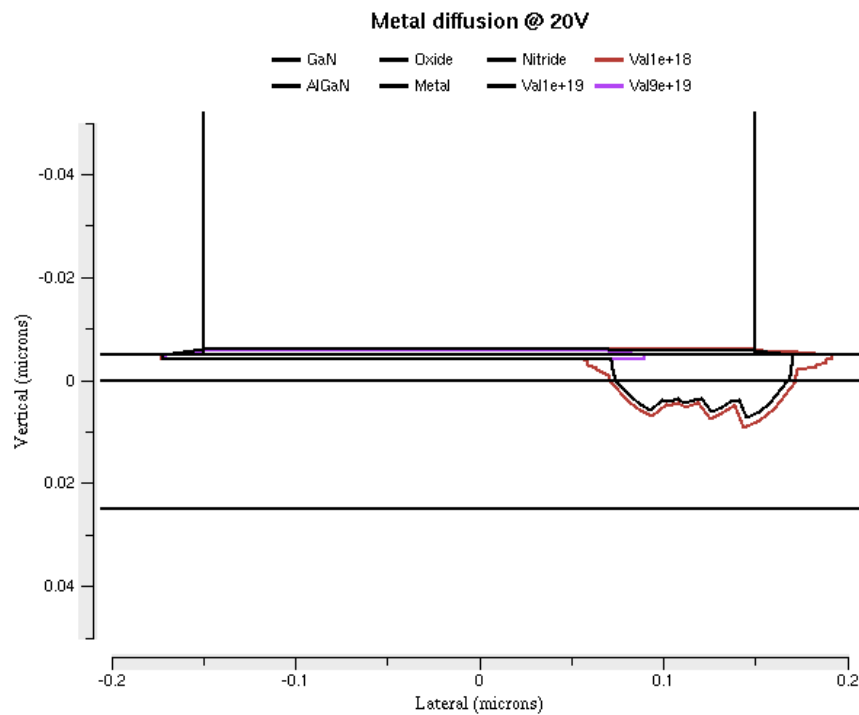
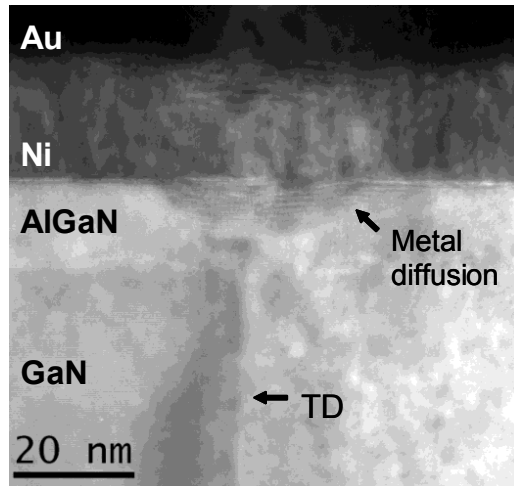


Figure 18. Cross-sectional TEM of drain edge of gate contact. The arrows indicate regions of Ni and oxygen diffusion with an associated threading dislocation. The bottom shows the simulated evolution of field profiles with metal diffusion.

Temperature Dependence

The interacting effects of temperature and electric field during off-state stress HEMTs with a gate length of $0.14 \mu\text{m}$ were stepped stressed from -10 V to -42 V in the dark at various temperatures ranging from room temperature to 150°C , regulated by a heated chuck. Both source and drain were held at ground in order to symmetrically stress the gate contact. The voltage at which irreversible degradation occurred was a strong function of temperature, as shown in Figure 19 [douglas2011]. V_{CRI} , followed a log relationship of the form, $V_{CRI} = V_0 e^{-E_a/kT}$, where the activation energy is 38 meV . The abrupt and permanent gate degradation at elevated temperatures was observed to occur at similar gate leakage currents regardless of critical voltage

and stress temperature ($\sim 10^{-7}$ A). Gate leakage currents immediately after critical voltage was reached also displayed similar values at all stress temperatures ($\sim 10^{-6}$ A).

The critical voltage of these devices at 24 °C was -30 V. As the temperature was increased to 150 °C, the critical voltage was observed to decrease. Due to the fact that V_{CRI} occurs at lower voltages as the temperature increases, the maximum electric field present at the edge of the gate at V_{CRI} also decreases. ATLAS/Blaze electrical simulations indicate that the peak electric field decreases from 3.3 MV/cm at a critical voltage of -28 V with a stress temperature of 28 °C to 2.6 MV/cm at a critical voltage of -18 V at 150 °C. The gate leakage current measured during the step stress of four different devices stressed at four different temperatures ranging from 24 °C to 150 °C further illustrate the negative temperature dependence. This result reveals that the breakdown which results in a sharp increase in gate leakage current does not occur at the same electric field, and therefore does not occur at the same piezoelectric induced stress. In addition, the gate leakage current was independent of critical voltage, indicating similar leakage paths for all stress temperatures. Devices stressed at room temperature have been reported to display a significant dependence on gate voltage / electric field. Ni/Au metallization schemes for Schottky contacts on GaN have been determined to be thermally unstable above 400 °C, with numerous nickel nitrides reported being formed at temperatures as low as 200 °C [43-46]. Additionally, thermal instabilities in Ni/Au based Ohmic contacts have been reported due to Ga out-diffusion and Au inter-diffusion at elevated temperatures.

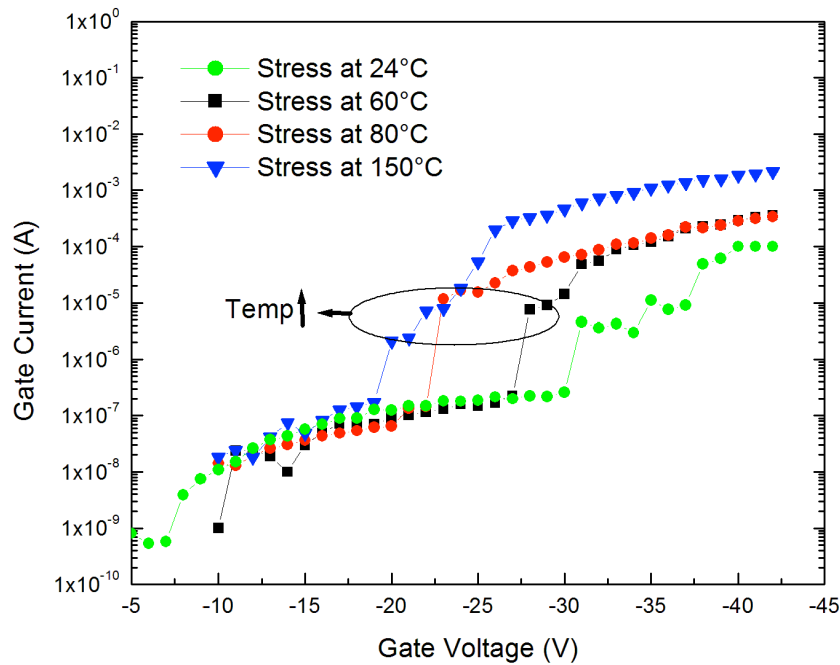


Figure 19. Gate current of four AlGaIn/GaN HEMTs step stressed from -10 V to -42 V at 24°C, 60 °C, 80 °C, and 150 °C.

Gate Metal

HEMTs that have been dc step stressed in the off-state beyond the critical voltage will occasionally show strong reactions of the gate metal with the underlying nitride semiconductor. A typical example is shown in Figure 20, which shows metal reaction regions that have punched

through the GaN cap and into the AlGaN layer. A more extreme example is shown in the TEM images of Figure 21, where the top image is from a device stressed with $V_G = -10$ to -42 V with -1 V step and grounded source and drain, while the lower image is from a device stressed with $V_G = -10$ to -42 V with -1 V step with grounded source and applied $V_{DS} = 10$ V. This shows that the gate metal reaction is still a major issue with HEMT reliability and the choice of metal contact scheme might make a significant difference in the stability of the devices.

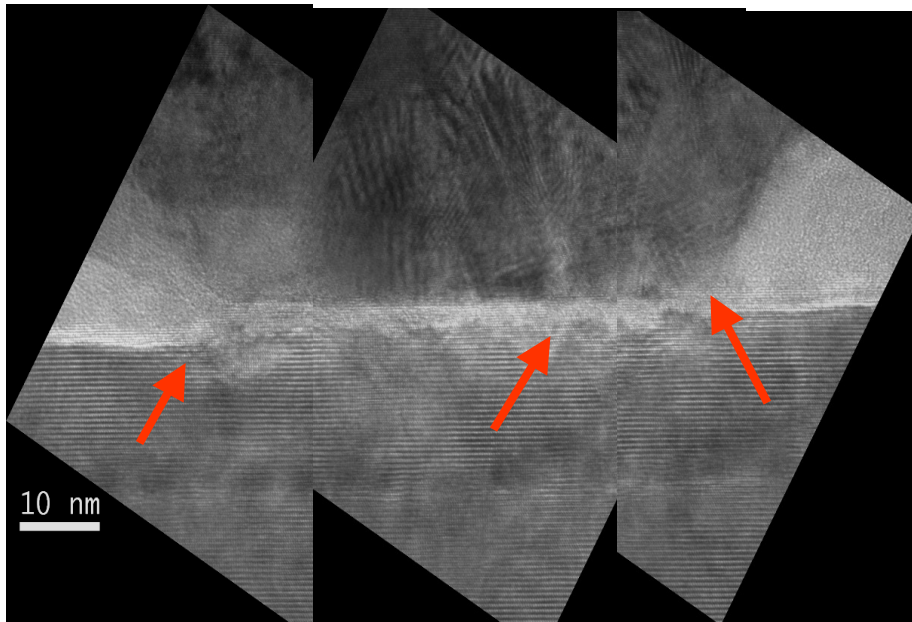


Figure 20. High resolution cross section TEM image of HEMT structure dc stressed in the off-state, showing metal reaction regions that have punched through the GaN cap and into the AlGaN layer.

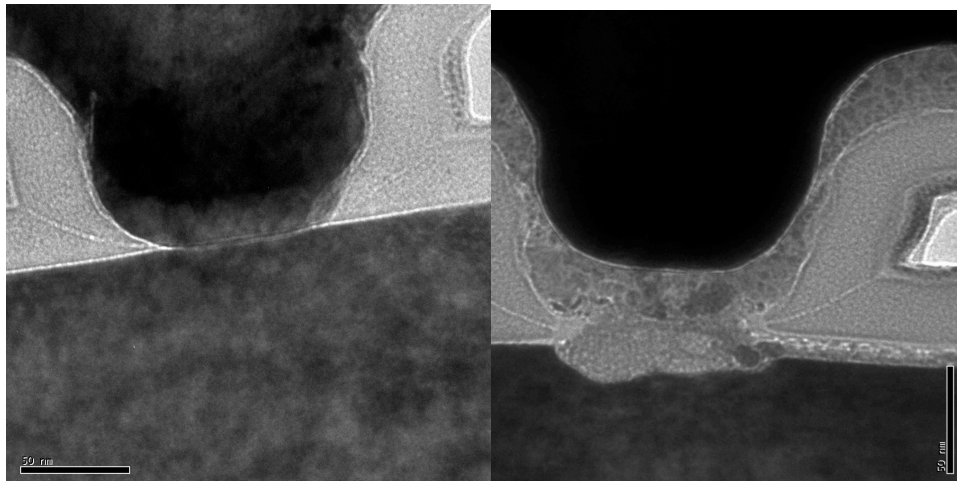


Figure 21. TEM images of the gate regions of HEMTs (top) stressed with $V_G = -10$ to -42 V with -1 V step and grounded source and drain and (b) HEMT stressed with $V_G = -10$ to -42 V with -1 V step with grounded source and applied $V_{DS} = 10$ V.

As shown in Figure 22, HEMTs with Ni/Au gate metallization exhibited a critical voltage around -55 V. However, there was no critical voltage observed for the HEMT with the Pt/Ti/Au gate metallization up to -100 V, limited by the instrument. This suggests that the use of Pt based gate metallization could extend the operating bias conditions and improve the device reliability. The Schottky barrier height and ideality of the Pt/Ti/Au were 1.23 and 1.2 V, respectively, which did not change as a result of stressing. By contrast, HEMTs with Ni/Au gate metallization showed significantly higher gate reverse bias leakage current and much lower breakdown voltage. The forward gate characteristics of the Ni/Au gate contact appeared very leaky after the stress and the Schottky height reduced from 1.09 to 0.66 V after stress.

The interface between Ni/Au gate metal stack and the underlying semiconductor layer showed an oxide layer present prior to performing off-state stress. Laser-assisted APT data showed an O peak at the interface between the Ni and AlGaIn layers and AlO_x and NiO_x present at the interface [holzworth2011]. Consumption of this oxide layer, and even diffusion of oxygen, has been observed after off-state stress. The stability of Pt as a gate metal is due in part to its low reactivity with oxygen.

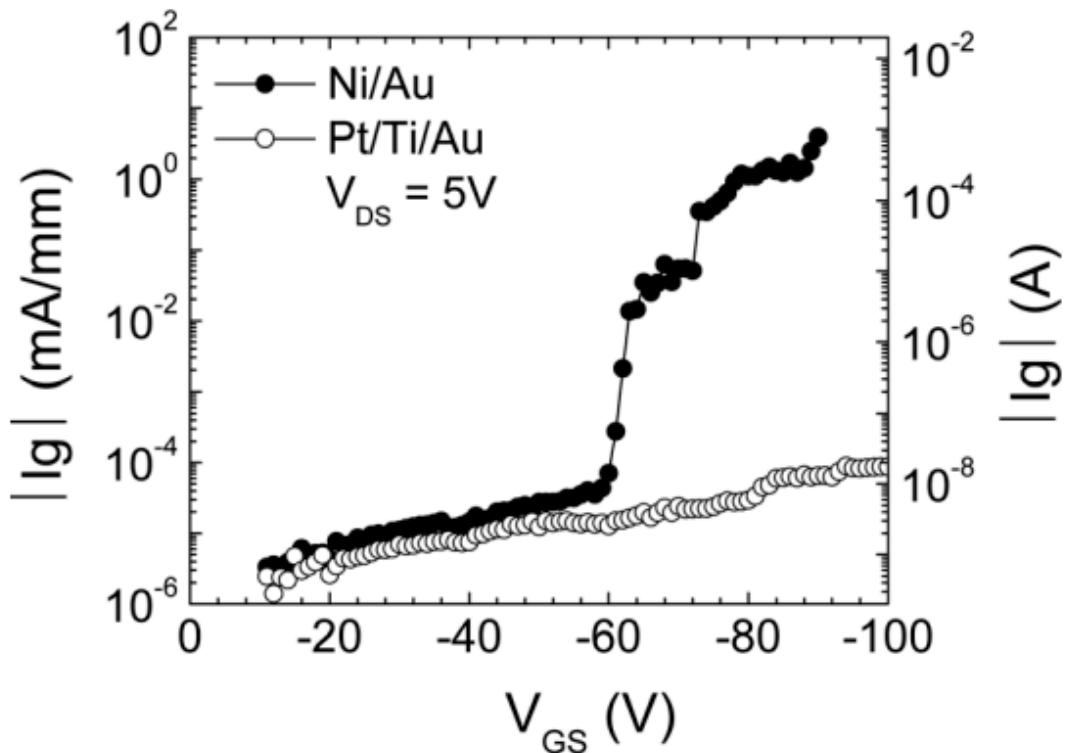


Figure 22. Off-state gate currents as a function of gate for the HEMTs fabricated with Ni/Au or Pt/Ti/Au gate metallization

RF Stress Tests

Devices with a 0.125 μm gate length were biased under Class AB conditions with a quiescent drain current (I_{DQ}) of 200 mA/mm at drain bias (V_{DS}) of 10 V, 20 V, and 25 V. RF stressing for

up to 350 hours was performed at 10 GHz, driven into 3dB compression and a baseplate temperature of 30 °C [douglas2012]. Both P_{OUT} and I_{DS} showed little to no degradation for drain bias of 20 V, but rapid permanent degradation occurred at a drain bias of 25V, as shown in Figure 23. A small recovery in both P_{OUT} and I_{DS} is present after pausing at ~25 hours to obtain mid-stress device characteristics. Operating at a drain bias of 25 V is above the threshold necessary for the onset of degradation and is consistent with the observed critical voltage during dc stress. Small degradation in saturated drain current (I_{DSS}), less than 10%, occurred for all conditions after stress and is consistent with prior reports on RF reliability [joh2012]. For the lowest drain bias of 10 V, a small increase (~3%) in PAE and I_{DS} (~1 mA) was observed during RF stressing for 350 hours, and may indicate that device burn-in is necessary in order to stabilize and improve RF device performance at lower bias conditions. Similarly, minimal degradation in PAE, P_{OUT} , gain, and transconductance occurred for a drain bias of 20 V. An increase in V_{TH} was observed for all stress conditions, with the largest ΔV_{TH} of 0.37 V at a drain bias of 25 V, indicating significant degradation of the Schottky contact. The Schottky barrier height reduced from 673 mV to 602 mV after stress at $V_{DS} = 25$ V. Even though device characteristics for drain bias at or below 20 V do not show significant RF degradation, the gate current-voltage sweeps with $V_{DS} = 0$ V indicate that the Schottky contact suffered degradation, with almost a 2 order of magnitude increase in gate leakage current. Even though the stress at a drain bias of 25 V was performed for a shorter duration, only ~85 hours, gate leakage current shows the largest increase with almost a 3 order of magnitude rise in current.

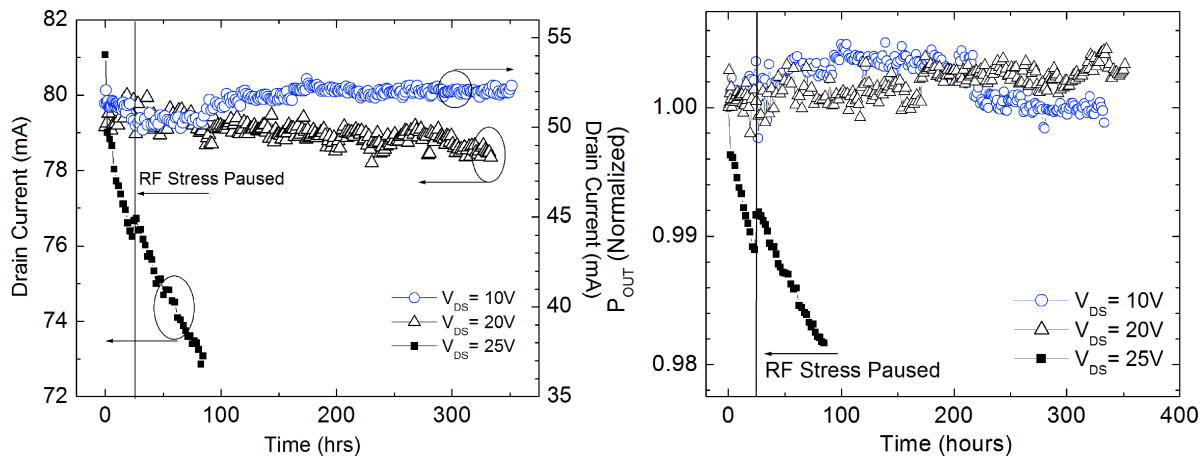


Figure 23. (top) Drain current and (bottom) output power during RF stress at 10 GHz under 3 dB compression of 0.125 μm gate length AlGaIn/GaN HEMT

Prior to stress, devices exhibited uniform EL emission under forward bias. However, points of gate leakage appeared with gate bias of -10 V. After RF stress, gate leakage paths were not present on the same channel as present prior to stress. It appears from EL emission that degradation due to RF stress may be localized along the channel on the right.

Summary

AlGaIn/GaN HEMTs show severe degradation after reverse bias step-stressing of drain voltage whereas TLM structures, in which there is no Schottky contact, exhibited excellent stability.

Increased baseplate and channel temperatures decreased the voltage at which catastrophic failure occurred. The combination of the Schottky gate material itself and the processing steps preceding the gate deposition is the likely cause for permanent degradation. There are a number of mechanisms theories to explain the reverse degradation of HEMTs, including oxidation of the surface, with subsequent generation of pits, defect generation/percolation in the AlGa_N, generation of point defects within the AlGa_N and the inverse piezoelectric effect. Off-state stress showed a linear relationship between critical degradation voltage and gate length. Device degradation is not a threshold process, and may occur even below the so-called critical voltage given enough time under stress. In this view, degradation is supposed to be related to a defect percolation process (activated by the high electric field and/or by the injection of hot carriers), and not unequivocally to the inverse piezoelectric effect.

An oxide layer is present between gate and GaN cap layer before stressing, but consumed after DC stress. Gate leakage current also increases after DC stress. Simulations show constant electric field for breakdown at various critical voltages. Interfacial oxide layers are reactive with the Ni from the Ni/Au gate metal stack after high reverse gate bias stress. In some instances, oxygen was observed diffusing into the underlying AlGa_N layer and further through threading dislocations that terminated below the Schottky contact. Both dc and RF high electric field stress indicated a decrease in Schottky barrier height and large increases in gate leakage current. However, a small decrease in saturate drain current was observed in all instances. Devices with Pt/Ti/Au gate metal scheme showed superior stability up to gate voltages of -100 V. These studies indicate that the reliability of AlGa_N/Ga_N HEMTs can be significantly improved for high electric field applications through the use of much more stable gate metals, such as Pt.

Sub-micron gate length HEMTs stressed under Class AB RF conditions with drain bias of 10, 20 and 25 V. AlGa_N/Ga_N HEMTs show excellent reliability up to a drain bias of 20 V, however the Schottky contact properties show substantial degradation in terms of threshold voltage shift, gate leakage current, and Schottky barrier height increase. This indicates the gate contact is the cause for device failure. RF stressing at a drain bias of 25 V is above the threshold necessary for the onset of degradation and resulted in rapid, permanent degradation in P_{OUT} and I_{DS} .

Section 4 Materials Characterization

Chemical and Structural Characterization of Ni-Gate AlGaN/GaN HEMTs

The work presented in this portion involves the chemical and structural characterization of unstressed, electrically stressed, and thermally stressed Ni-gate AlGaN/GaN HEMTs. The experimental equipment, set up, and procedures are first described, and are followed by a comprehensive summary of significant results.

Device Processing

(a) Electrical Measurements

All electrical measurements and stressing for the AlGaN/GaN HEMTs were completed using a HP 4156C semiconductor parameter analyzer except for C-V measurements which were measured using an Agilent E4980A precision LCR meter. The HEMTs were unpackaged and electrical measurements and applied electrical stresses were completed using probe tips. Conducting metal needles were lowered onto the contact pads of the devices, then voltages were applied to the needles in order to generate electric fields and current flow.

(b) Thermal Annealing

In order to isolate only the effect of thermal stress on AlGaN/GaN HEMTs, transistors were placed in a standard tube furnace to undergo thermal anneal. All anneals used a 36" long quartz tube and the temperature was regulated by a heating coil wrapped around its perimeter as shown below in Figure 24.

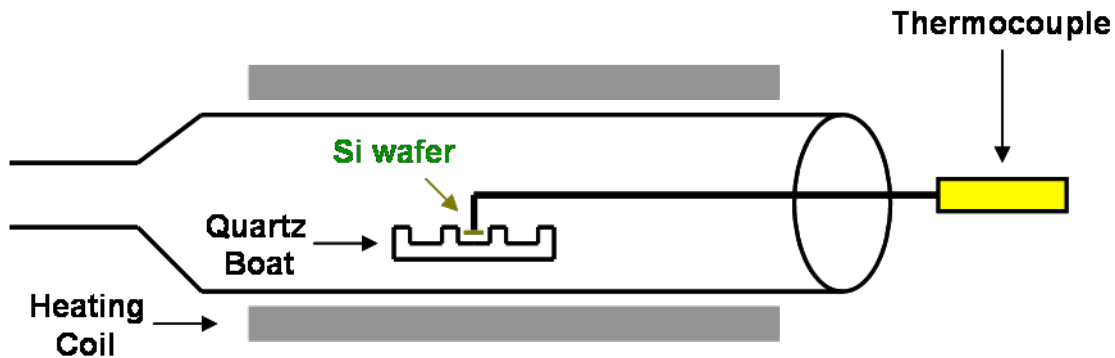


Figure 24 - Schematic of the tube furnace set up used for thermal annealing.

Due to the miniature size of the reticule that contained the transistors (~ 7mm by 3mm), transistors were placed on a cleaved piece of Si(100) wafer that was wedged into a slot on a preheated quartz boat. This setup prevented the transistors from moving during the insertion and extraction of the boat from the furnace and allowed accurate measurement of the temperature. The boat was always placed in the same exact spot for each anneal near the center of the furnace using a system of rods and markings. Because of the size of the samples, the temperature was not measured directly on the sample. Instead a thermocouple was positioned on the Si(100) wafer holding the transistors without touching the transistors, the quartz boat, or any part of the

quartz tube. Furthermore, the temperature was measured both at the start and at the finish of each anneal. Additionally, the thermocouple measurement error is estimated to be $\pm 1^\circ\text{C}$ as per the accuracy of the device. It is noted that one end of quartz tube had a gas inlet and the other end was capped to permit the application of different ambients. For this work, the anneal temperature was varied from 100°C - 850°C and for durations from 0.25 h - 1000 h. Generally, this method is considered to be slow for sample temperature ramp up and cool down (< 5 min) compared to a rapid thermal anneal. However, since the ramp up and cool down time was much smaller than the anneal duration, this possible error is minimized and the measured anneal times are taken to be accurate.

(c) Transistor Etching

In order to observe any large areas (dimensions greater than $20\text{ nm} \times 20\text{ nm}$) of physical degradation on top of the AlGaIn surface, the passivation and gate metal of the HEMTs were removed by wet chemical etching. The first step of the etch process is the removal of the SiNx passivation layer covering the AlGaIn/GaN HEMTs by submerging them in a buffered oxide etch solution of HF for 15 min. Next, the HEMTs were cleaned with water in order to remove any residual solution. After the cleaning step, the metallization was removed by submerging the HEMTs in a solution of FeCN and KI for 0.75 - 5 days. Following the removal of the metal, the top surface of the AlGaIn epilayer was exposed to ambient. This surface was cleaned of any build up of reaction products from the etching steps by ultrasonication in solution of acetone and n-heptane for 1 h, then methanol for 1 h, and lastly in water for 1 h. It has previously been shown that using the FeCN and KI solution to remove the metallization doesn't etch the AlGaIn epilayer of the HEMTs for periods up to at least 18 h [Whiting2012].

Analytical chemical and structural characterization of the AlGaIn/GaN HEMTs was performed using a scanning electron microscope (SEM), transmission electron microscope (TEM) and atom probe tomography (APT) system. However, the sample preparation for these techniques ranges from simple to complex and is described in the following sections.

Device Sample Preparation

(a) SEM

SEM requires electrically conductive samples which is a simple process involving the thermal deposition of thin layers of C over the sample surface.

(b) Cross sectional TEM (XTEM)

TEM requires electron transparent samples. However in order to achieve electron transparency, TEM foils typically must be $< 300\text{ nm}$ thick and preferably $< 100\text{ nm}$ thick if any chemical characterization is desired or if the sample is composed of high Z elements. A thinner foil is advantageous because as thickness increases the number of scattering events (both elastic and inelastic) increases making analysis more difficult. In this work, a FIB system was used to prepare site-specific cross sectional TEM (XTEM) foils due to the required site-specificity involving regions of interest (ROI) $< 100\text{ nm}$ wide.

In this work, the FIB system used for XTEM sample preparation is a FEI DB 235 dual beam machine with both an SEM and an ion beam which are off-set 52° from each other. This orientation permits SEM micrographs to be gathered during the milling progress without damaging the sample. For FIB preparation, the HEMTs were placed on Al stubs using C adhesive tape. Once the samples are placed in the FIB system and the vacuum reaches $< 7 \times 10^{-5}$ mBar, then a focused beam of Ga^+ ions is accelerated at 30 keV towards an ROI. A gas injection system is used to deposit an organo-Pt layer $\sim 8 \mu\text{m}$ wide $\times 2 \mu\text{m}$ long and $1.8 \mu\text{m}$ thick over the ROI using a 300 pA beam current. This Pt layer protects the ROI from further ion beam damage as the sample is milled thinner later in the process. After Pt deposition, large, deep trenches $\sim 10 \mu\text{m}$ wide $\times 7 \mu\text{m}$ long $\times 3.5 \mu\text{m}$ deep were milled above and below the Pt using a 5000 pA beam current which exposed the cross section of the HEMT as shown in Figure 25 A – B. The Pt covered ROI is then progressively thinned using a 1000 pA beam current mill until its thickness reaches $\sim 1 \mu\text{m}$ causing the sample to resemble a wish bone shape. This is followed by an undercut $\sim 2 \mu\text{m}$ below the surface of the ROI which separates the ROI from the substrate using a 1000 pA beam current. Then another 1000 pA beam current mill is used to release one side of the sample from substrate as shown in Figure 25 C. A micromanipulator actuating a W needle is brought close to the surface of this free side and is attached using organo-Pt deposition as shown in Figure 25 D. Once the sample is attached to the W needle, the other end is milled to release the sample from the substrate as shown in Figure 25 E.

With the sample attached to the W needle, it is vertically moved away from the surface of the HEMT and moved to a Cu grid with fingers. The W needle positions the sample so that it touches the grid and the W at the same time, but without overlapping the Cu grid and the ROI as shown in Figure 25 F. Then the sample is adhered to the Cu grid using the organo-Pt deposition and is milled free from the W needle as shown in Figure 25 G. At this point, the sample's sides are progressively thinned again using a 50 pA beam current until the thickness < 300 nm as shown in Figure 25 H. Then the sample is tilted 2° on each side and milled which reduces the thickness < 100 nm. For the final thinning step, the sample is rotated 3° and milled so that it forms a wedge with the ROI positioned slightly before the edge of the sample achieving a thickness < 100 nm as shown from a top view of Figure 25 I. At this point, the XTEM foil is complete is ready for imaging and analysis.

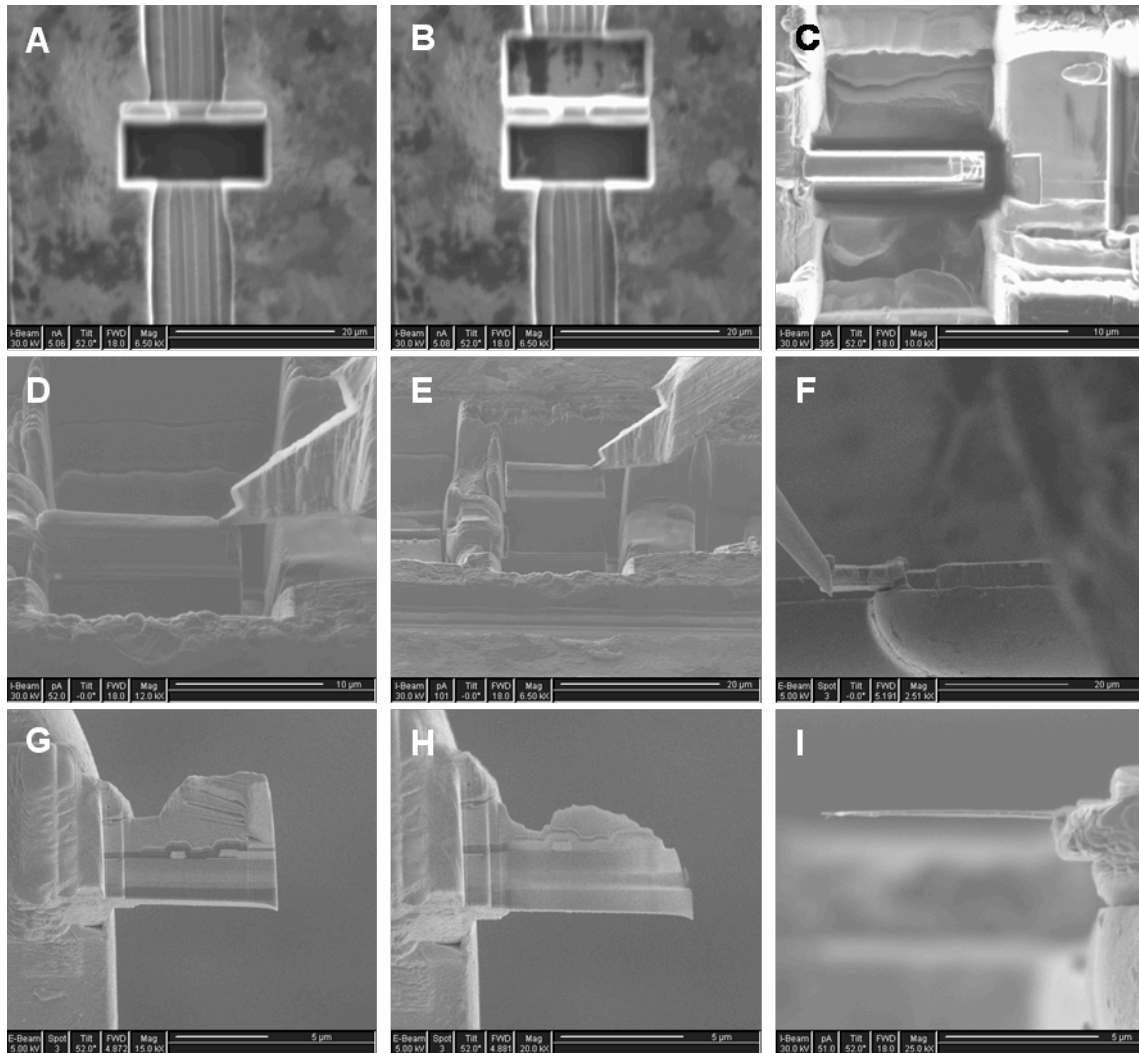


Figure 25 - SEM and ion beam micrographs showing the FIB procedures to lift-out a XTEM sample of an AlGaIn/GaN HEMT.

(c) APT

Similar to TEM sample preparation, APT sample preparation requires the fabrication of samples on the nm-scale. Here, the samples were fabricated by FIB method to form sharp needle-like tips ~ 100 nm in diameter, 100 nm above the ROI, and possessing a half shank angle between $5^\circ - 7^\circ$. The steps to mount a ROI onto a Si post are the same as the steps for XTEM sample preparation described previously until the sample is extracted from the substrate and attached to the W needle as shown in Figure 25 E. Following sample extraction, Figure 26 A – B shows the ROI is centered on top of a Si post where it is bonded to the post using organo-Pt in Figure 26 C. Then $2 \mu\text{m}$ wide sample of the ROI is cut free from the rest of the ROI and the backside of the ROI is bonded to the Si post again using organo-Pt as shown in Figure 26 D. The Si post is then tilted to 52° so that the ROI is parallel to the ion beam as shown from top view in Figure 26 E and from 52° in Figure 26 F. An annular mill at 5000 pA with an inner radius of $4 \mu\text{m}$ and an outer radius of $8 \mu\text{m}$ centered around the ROI is used to mill the Si pillar as shown in Figure 26 G. A second annular mill at 1000 pA with an inner radius of $1 \mu\text{m}$ and an outer radius of $4 \mu\text{m}$

centered around the ROI is used to mill the Si pillar as shown in Figure 26 H. This is followed by a third annular mill at 300 pA with an inner radius of 0.3 μm and an outer radius of 4 μm centered around the ROI to mill the Si pillar. This mill is continued until the tip apex is ~ 500 nm from the ROI. By this time the Si post and ROI should be needle-like in shape. Finally, the FIB accelerating voltage is reduced to 8 kV and a continuous low voltage mill is used to clean up the tip surface from damage caused by higher voltage milling. This mill is continued until the tip apex is $\sim 100 - 300$ nm from the ROI as shown in Figure 26 I.

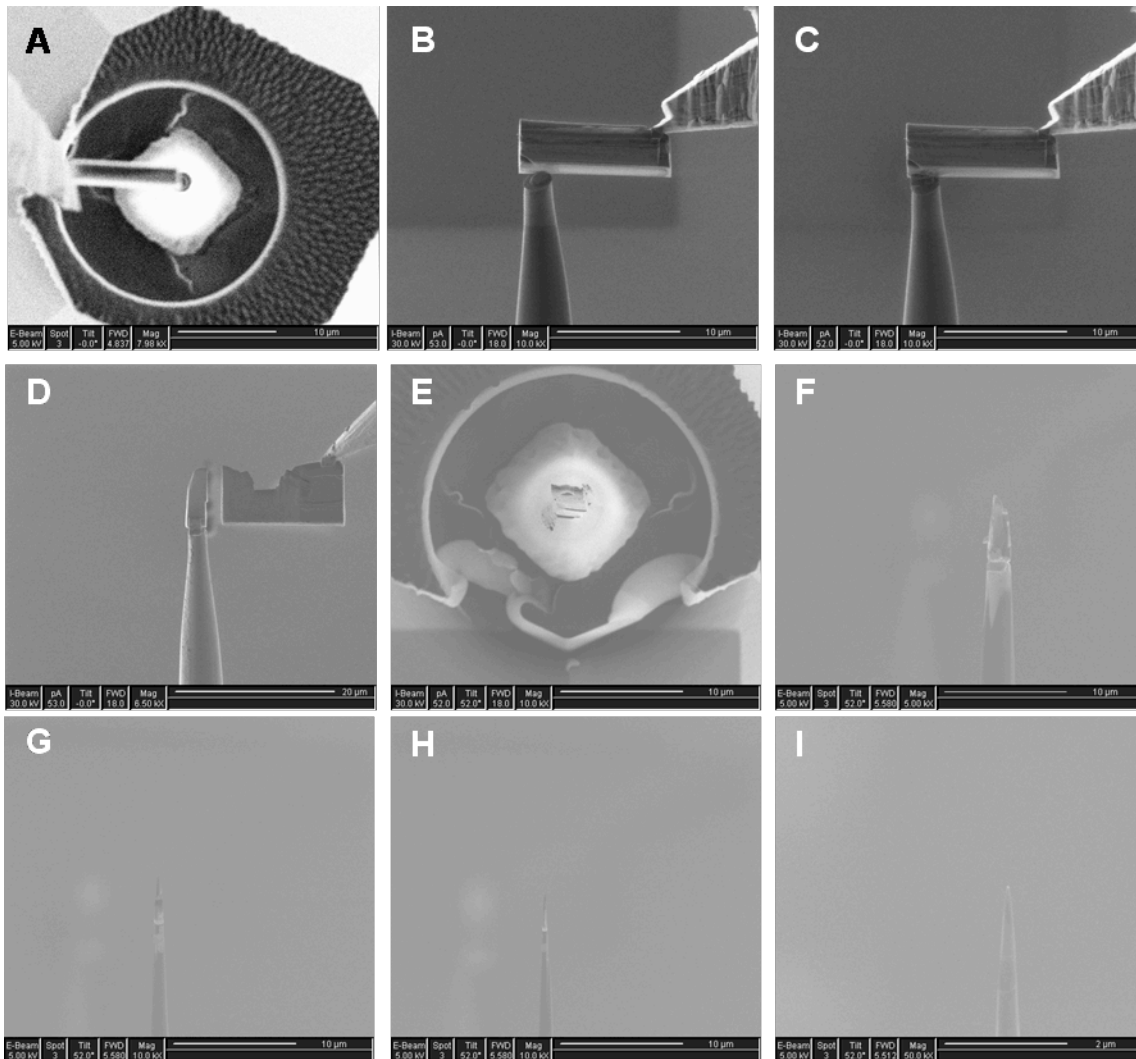


Figure 26 - SEM and ion beam micrographs showing the FIB procedures to fabricate an APT tip of an AlGaN/GaN HEMT.

Significant Results

(a) Interfacial Layer Characterization

The interfacial layer between the gate contact and AlGaN epilayer of commercial and AFRL produced Ni-gate AlGaN/GaN HEMTs was characterized. For the commercial HEMTs, Local Electrode Atom Probe (LEAP) tomography was used to identify the chemistry of the interfacial layer which was revealed to consist of a bi-layer of NiO_x and AlO_x with no GaO_x detected. The

interfacial layer was shown to be approximately 5\AA thick by TEM. These results are shown in detail in the literature [Holzworth2011].

A typical device structure for the gate region of the AFRL HEMTs is shown in the high-angle annular dark-field scanning TEM (HAADF-STEM) image of Figure 27 A. However, for the AFRL HEMTs, the interfacial layer could not be successfully field evaporated using LEAP or APT. This is shown in the LEAP reconstruction in Figure 27 B where the AlGa_N layer is almost completely missing from the analysis. Therefore, high resolution aberration corrected TEM was used to characterize the interfacial layer for these devices. Figure 28 A shows a high magnification HAADF-STEM image of the gate region and semiconductor interface of an unstressed AFRL HEMT. The distinct layers of the device are labeled: Au, Ni, AlGa_N, and GaN, and the interfacial layer is shown to be 15\AA thick. Additionally, a highlighted box indicates the region where electron energy-loss spectroscopy (EELS) maps were acquired for chemical analysis. EELS maps of Ni, Ga, N, and O are presented from the highlighted region of Figure 28 A in Figure 28 B, C, D, and E, respectively. The Ni EELS map in Figure 28 B shows the Ni layer of the gate and that it is flat and uniform. The Ga and N EELS maps shown in Figure 28 C and D show the AlGa_N layer below the gate. Comparing the Ni and Ga maps it is seen that there is a small gap between them. This is explained by analyzing the O EELS map in Figure 28 E which indicates that presence of an O layer between the Ni gate and AlGa_N. This is comparable to the results from the LEAP data from the commercial Ni-gate HEMTs discussed earlier which indicated the interfacial layer between the gate and AlGa_N was composed of an oxide. Thus, similarly to the commercial Ni-gate HEMTs, it is shown that the interfacial layer between the gate and AlGa_N in the Ni-gate AFRL HEMTs is also composed of an oxide layer.

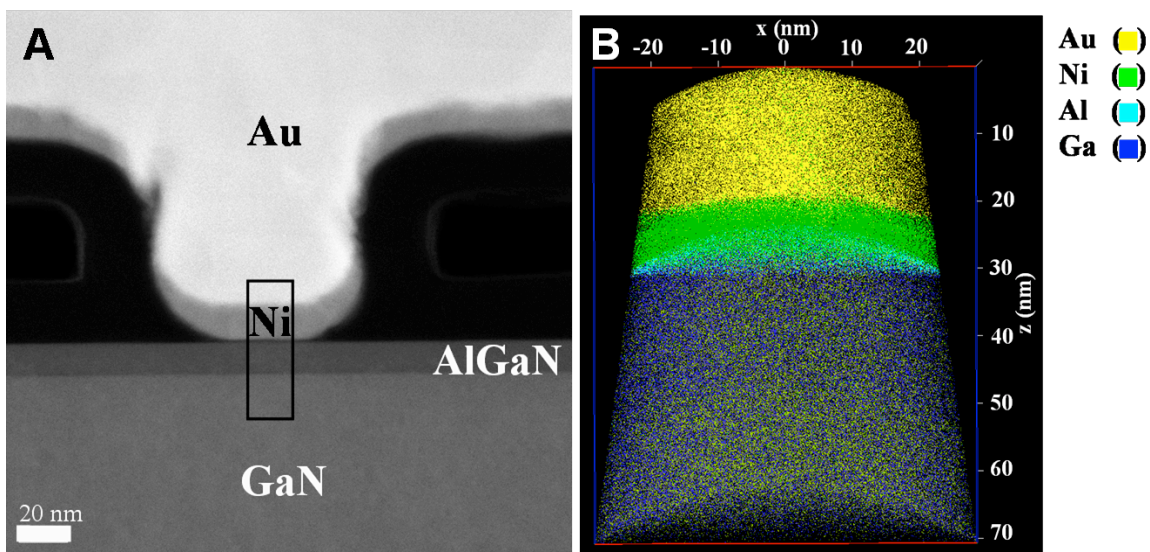


Figure 27 - HAADF-STEM image of the gate region of an AFRL Ni-gate HEMT and an Imago LEAP reconstruction of the gate/AlGa_N interface with the AlGa_N missing.

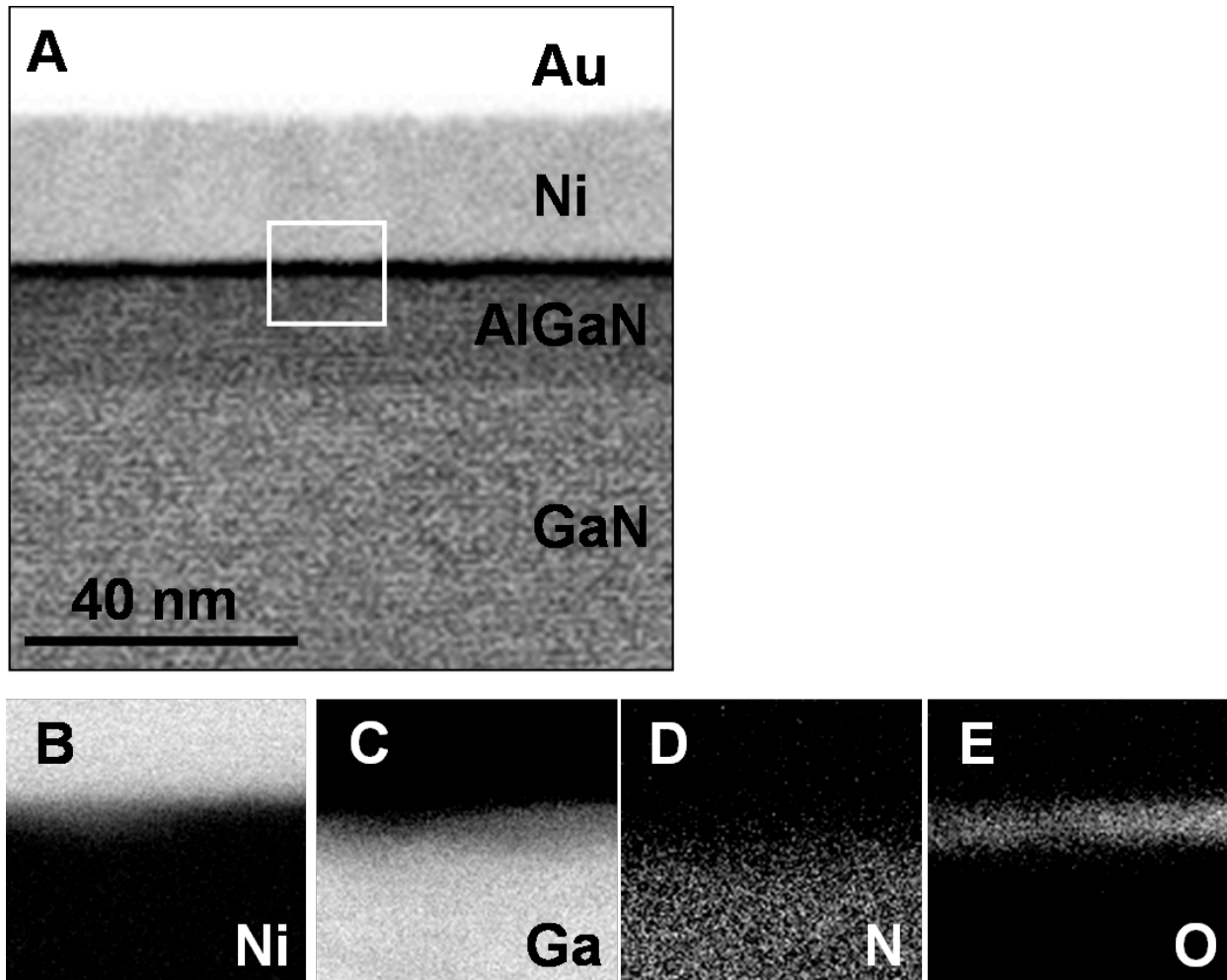


Figure 28 - XTEM image and EELS chemical maps of the gate/AlGaN interface region from an AFRL Ni-gate HEMT.

(b) Electrically Induced Physical Degradation

For the application of electrical stress, only <100 nm gate length Ni-gate AFRL HEMTs on SiC were stressed. Additionally, off-state high reverse gate bias conditions were used to electrically stress the HEMTs. During the applied stress, a constant drain-source voltage $V_{DS} = 5$ V was applied to the majority of the samples. Additionally, for some samples a $V_{DS} = 0, 10,$ or 15 V was applied. However, the gate-source voltage (V_{GS}) was varied for each sample during stressing and started at either -5 or -10 V and ended at -42 V with the gate voltage stepped at -1 V/min. Electrical parameters of each HEMT were measured between each unit decrease in V_{GS} at $V_{DS} = 5$ V and $V_{GS} = 0$ V. All stressing occurred at 25 °C and in air.

The majority of HEMTs underwent an electrical stress with $V_{DS} = 5$ V and these results have been discussed in detail elsewhere in the literature [Holzworth2013]. However, a quick review will be given here. After application of the electrical stress with $V_{DS} = 5$ V, two different behaviors, ‘slow’ and a ‘rapid’ degradation, were recorded for the change in normalized maximum drain current ($I_{D\ max}$) of the HEMTs. On average, devices that exhibit this ‘slow’

degradation behavior show a minimal decrease of $\sim 3.5\%$ in normalized $I_{D\ max}$ by $V_{GS} = -22\text{V}$. Furthermore, by the end of stressing at $V_{GS} = -42\text{V}$, normalized $I_{D\ max}$ has decreased on average by $\sim 13 \pm 4\%$. This behavior is in contrast to the second behavior characterized as a ‘rapid’ degradation process. For these HEMTs, normalized $I_{D\ max}$ has decreased by $\sim 16\%$ by $V_{GS} = -22\text{V}$, which is more than a 350% larger decrease in normalized $I_{D\ max}$ compared to the ‘slow’ degradation process. Additionally, by $V_{GS} = -42\text{V}$, normalized $I_{D\ max}$ has decreased by $\sim 26\%$, which is a decrease in normalized $I_{D\ max}$ of 160% compared to the ‘slow’ degradation process. Also, it is important to note that for the ‘slow’ HEMTs only after the jump in I_G at $V_{GS} = -14\text{V}$ does the normalized $I_{D\ max}$ begin to degrade. Before the jump in I_G , $I_{D\ max}$ had degraded by $< 1\%$ over the first 10 V of applied gate stress; however, after the I_G jump, $I_{D\ max}$ begins to degrade slowly and constantly at $\sim 0.5\%/V$ until the end of stressing. In contrast, for the HEMTs that experience ‘rapid’ degradation, $I_{D\ max}$ begins to decrease as soon as stressing initiates. This contrast between the characteristic $I_{D\ max}$ and I_G curves of the sets of devices indicates that different degradation modes are occurring.

XTEM samples of the ‘slow’ degradation HEMTs showed no obvious physical degradation, and no defects were ever observed in any of the ‘slow’ degradation samples. However, the gate region of a ‘rapid’ degradation HEMTs exhibited a markedly different morphology with an ‘arch’-shaped defect under the gate, which penetrates into the AlGaN epilayer at two points. Chemical analysis of these defects indicates that it is an intermixing of the Ni, Al, and Ga from the gate and AlGaN, and that the defect is an oxide as the nitrogen originally present in the AlGaN is deficient after the reaction.

In addition to HEMTs stressed using a $V_{DS} = 5\text{V}$, other HEMTs were stressed with V_{DS} varying from 0 V to 15 V in increments of 5 V. The change in normalized $I_{D\ max}$ against V_{DS} for representative devices from these stress conditions are shown in Figure 29. Again, it can be seen that from the ~ 30 devices stressed in total, that two behaviors occur, a ‘slow’ and ‘rapid’ degradation of $I_{D\ max}$. Again, for the ‘rapid’ degradation cases shown with $V_{DS} = 5$ and 10 V, the decreases immediately from the start of electrical stressing. Additionally, it is shown again that for the ‘slow’ degradation cases shown with $V_{DS} = 0, 5,$ and 15 V that the $I_{D\ max}$ doesn’t decrease immediately. It is important to note that the slopes of the $I_{D\ max}$ degradation from the ‘slow’ HEMTs are all approximately the same after their respective I_G jump, $\sim 0.5\%/V$. It is noted that even during sections of greatest $I_{D\ max}$ degradation in ‘slow’ HEMTs that the average decrease is still $\sim 0.5\%/V$. This may indicate that these devices degrade by similar and constant mechanisms after the I_G jump possibly due to the creation of traps from the off-state electrical stressing. This is in contrast to the ‘rapid’ HEMTs where the slopes of their overall $I_{D\ max}$ degradation are $\sim 0.8 - 1\%/V$, and during sections of greatest $I_{D\ max}$ degradation range from $\sim 1 - 2\%/V$.

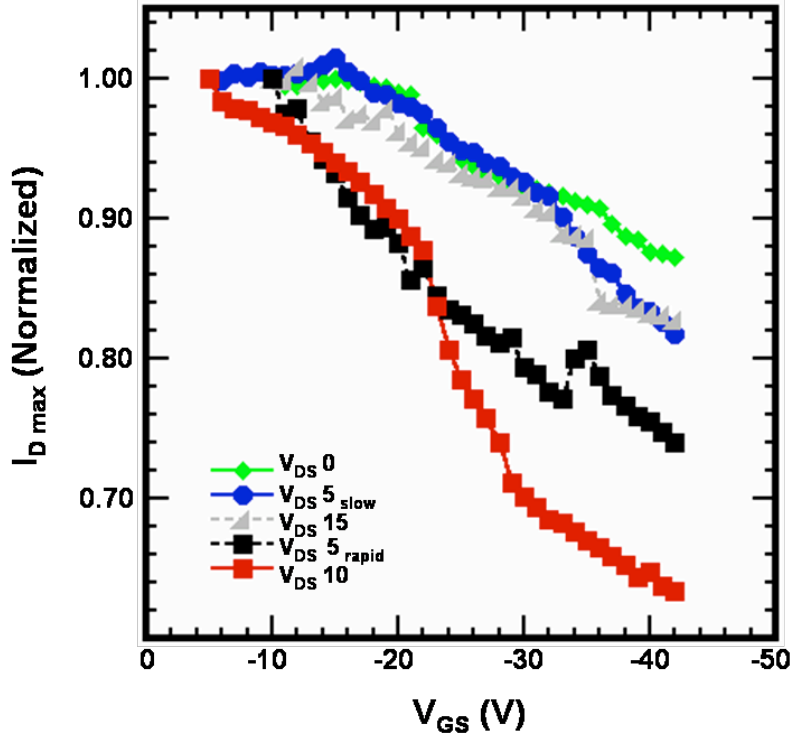


Figure 29 - Measured normalized $I_{D \max}$ representative curves of 'slow' and 'rapid' degradation HEMTs.

Typically XTEMs of the 'slow' degradation samples at $V_{DS} = 0$ and 15 V and the rapid degradation same at $V_{DS} = 10$ V are presented in Figure 30 A-C, respectively. Again, the 'slow' degradation HEMTs, shown in Figure 30 A and B, show no obvious physical degradation, and furthermore, no defects were ever observed in any of these 'slow' degradation samples. However, the gate region of a 'rapid' degradation HEMT at $V_{DS} = 10$ V exhibits a markedly different morphology as shown in Figure 30 C. This image indicates the presence of a 'wave'-shaped defect under the gate, which penetrates into the AlGa_N epilayer.

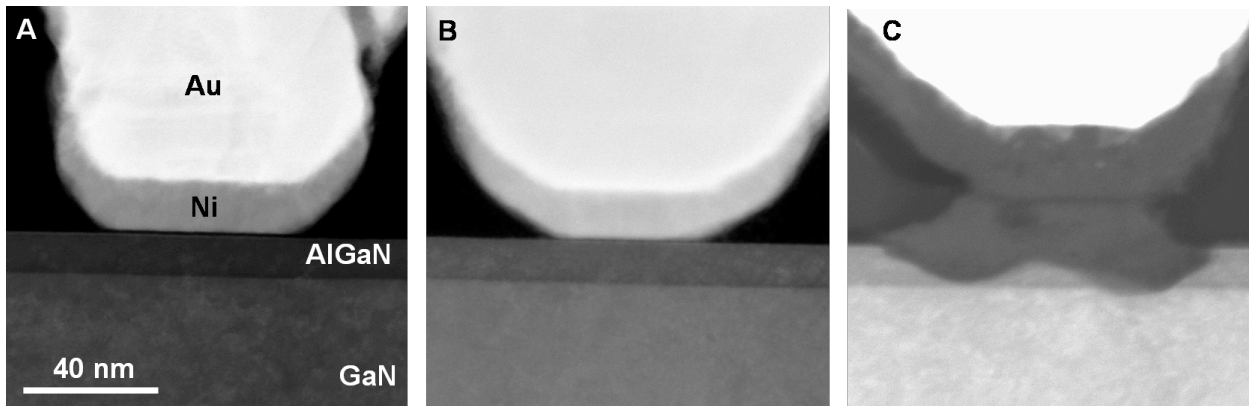


Figure 30. High magnification HAADF-STEM images of the gate region of AlGa_N/Ga_N HEMTs.

Energy dispersive X-ray spectroscopy (EDS) and EELS were also performed on the ‘wave’-shaped defects from the $V_{DS} = 10$ V stress condition. Here chemical maps of the EDS and EELS analysis are presented in Figure 31.

These maps are overlaid on the same image from the defect in order to better show the change in composition. For the ‘wave’ defect, Figure 31 A shows a HAADF-STEM image of the ‘wave’ defect which will be the background template used for comparison to the EDS and EELS maps for this defect. The EDS map of Ni is shown in Figure 31 B and indicates that Ni is present just below the Au region of the gate where the original Ni layer of the gate was and extends down into the top half of the defect. The EDS Ga map is shown in Figure 31 C and it is clear that Ga has diffused upward into the defect from the AlGaN. Next, the O EELS map is shown in Figure 31 D. It is clear that O is present in the original Ni layer of the gate, and there is an increase in O signal in the defect itself particularly in the original AlGaN region as the O signal mimics the shape of the defect. Lastly, the N EELS map is shown in Figure 31 E and shows the defect at both the original Ni layer of the gate and where the defect penetrates into the AlGaN. Therefore, these elemental maps indicate there is some measured diffusion of Ni into the defect and that the defect is shown to contain O and lack N where it penetrates the AlGaN epilayer indicating that an oxidation reaction has occurred. Additionally, it appears from both the EDS and EELS analysis that both the ‘arch’ and ‘wave’ defects exhibit this Ni, Ga, and Al mixing in the defect with O and the lack of N. Therefore, it is shown that the composition of the ‘arch’ and ‘wave’ defects is similar consisting of a Ni-Al-Ga-oxide.

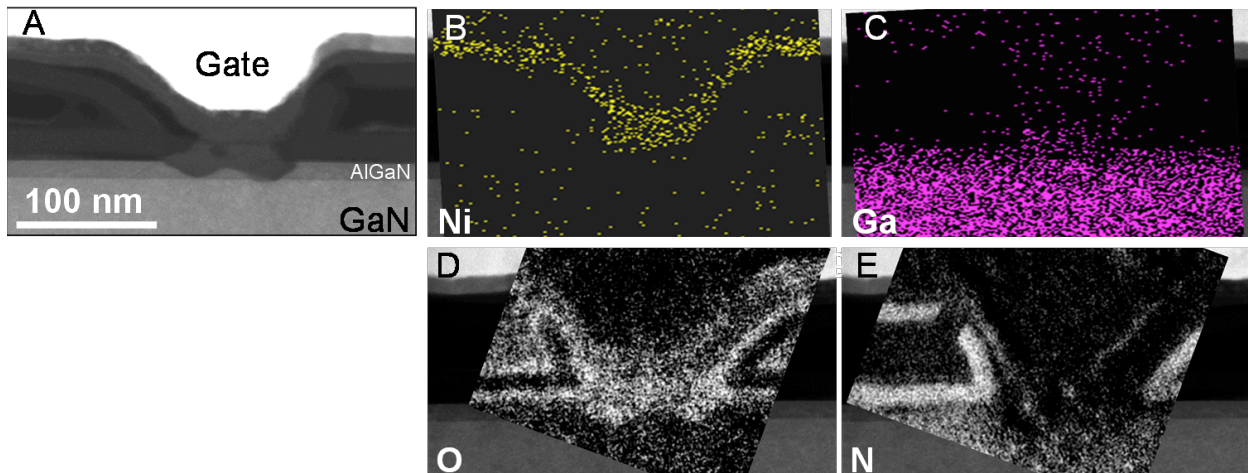


Figure 31 – TEM and chemical characterization of the under gate ‘wave’ defect.

(c) Thermally Induced Physical Degradation

For the application of thermal stress, 1 μm gate length Ni-gate AFRL HEMTs on Si(111) were stressed. For these samples, no electrical or mechanical stress were applied only thermal stress using anneals ranging from 300°C to 850°C for durations of 0.5 h to 400 h in order to isolate the effects of temperature on HEMT degradation.

There are two types of thermal anneal studies presented in this work. First, there are so-thermal anneals which are anneals at the same temperature but for varying duration. In this case, the temperature was maintained at 300°C for up to 400 h in order to determine the kinetics of the diffusion process. Second, there are iso-thermal anneals which are anneals at the same temperature but for varying duration. Here, the anneal duration was 0.5 h with a temperature range from 300°C to 500°C in order to determine the activation energy of the degradation process.

It was found that annealing between 300°C and 550°C resulted in gate metal entering into threading dislocations in the AlGa_N epilayer. This is demonstrated in the low magnification HAADF-STEM image Figure 32 A where gate metal can be observed penetrating into the dislocations. This penetration is more easily observed in the high magnification HAADF-STEM image Figure 32 B. Additionally, it was observed that for moderate temperature anneals (>550°C) even for a short anneal time of 0.5 h that delamination of the gate metal occurred as observed in Figure 32 C. While delamination of the gate metal is a serious reliability issue that needs to be avoided, it prevented the metal from penetrating into the threading dislocation in the HEMT. This was due to the metal now elevated above the surface of the AlGa_N and not in connection with it or the dislocations anymore. Thus, metal penetration into dislocations was not observed using XTEM for temperatures > 550°C.

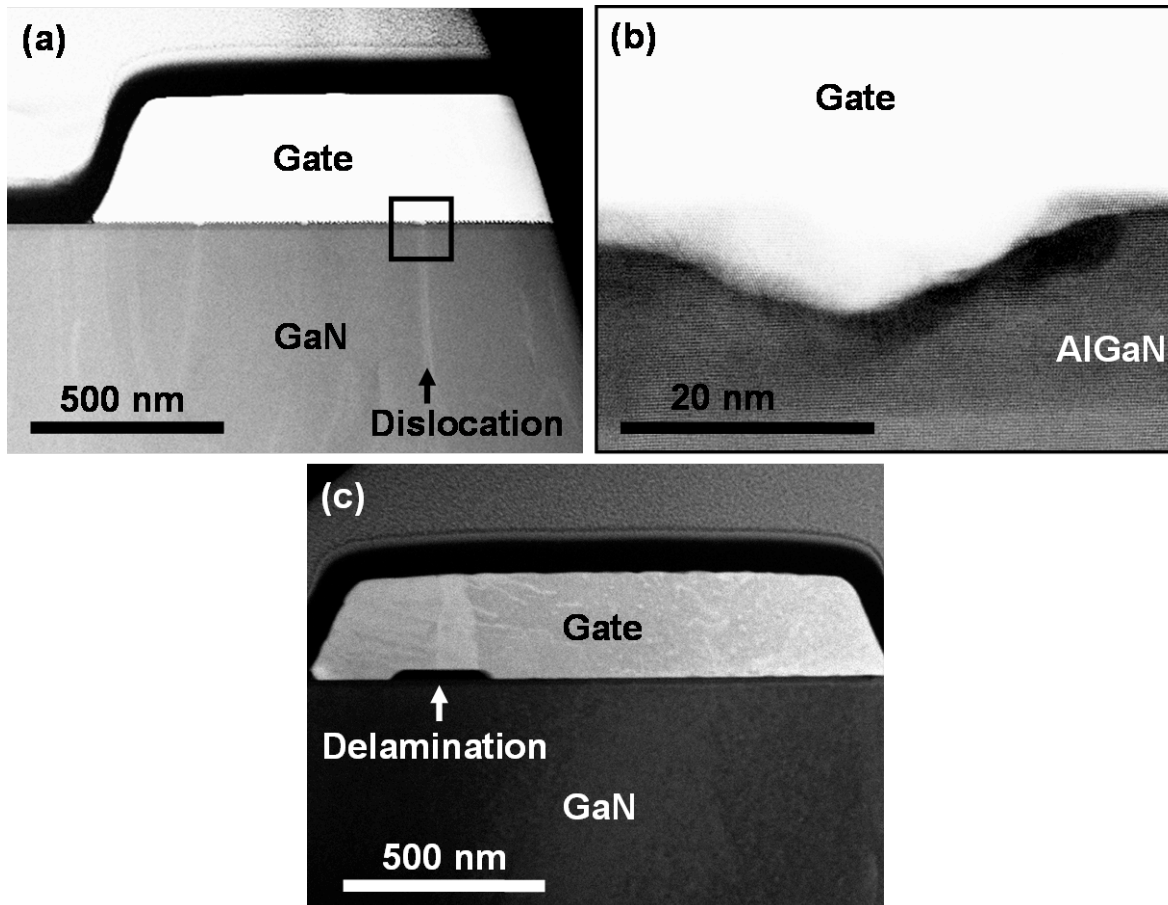


Figure 32 - HAADF-STEM images of the gate region of thermally annealed AFRL HEMTs.

From the iso-thermal anneal study, XTEM samples from the gate region of the HEMTs were made and analyzed. HAADF-STEM imaging was used to image the progressive metal penetration as anneal time increased in the samples. The metal penetration depth increased as the anneal duration is increased. This relationship between the penetration depth and time is plotted in Figure 33. From Figure KJ 10, it appears that the data follow an approximately $(DT)^{1/2}$ fit as shown by the regression equation on the plot. The power of the regression equation shows a fit of ~ 0.59 which is close to 0.5, a $(DT)^{1/2}$. Due to this closeness of fit, it is acceptable to conclude that the metal penetration is diffusion limited and that an Arrhenius behavior can be used to calculate the activation energy from the iso-chronal anneal sequence.

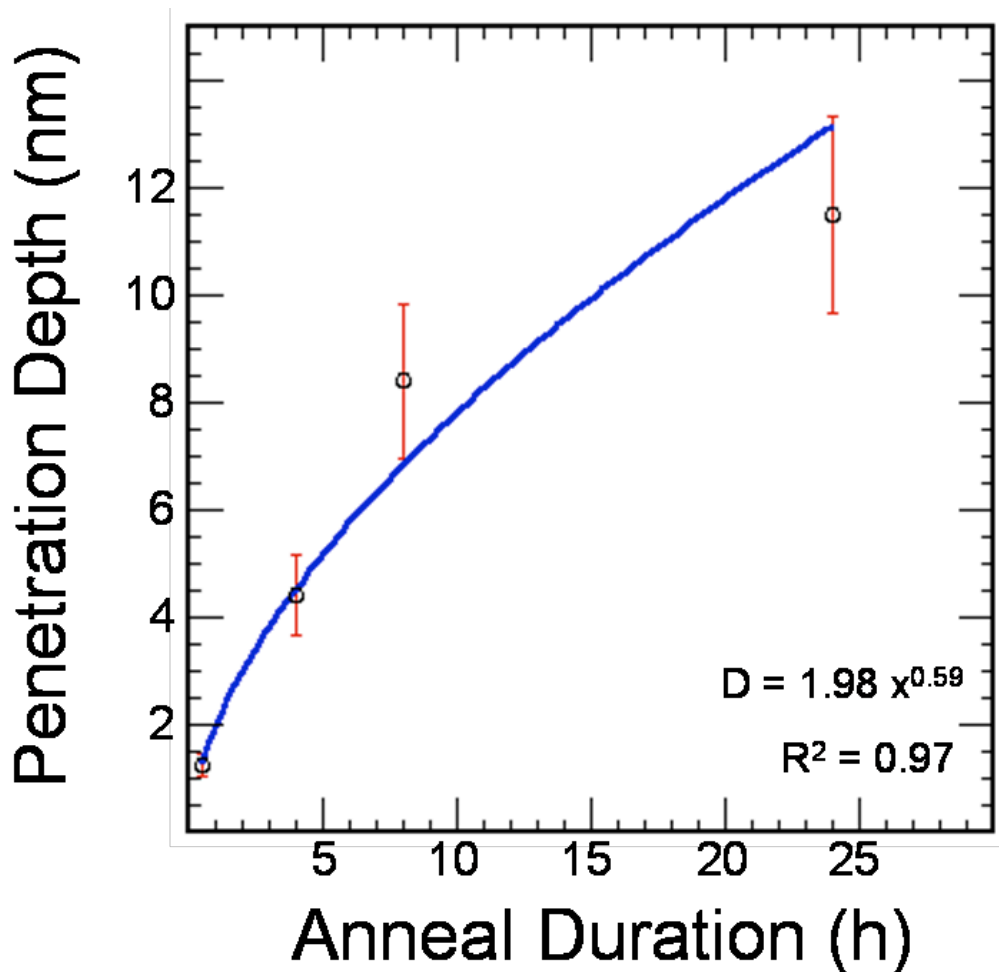


Figure 33 - Plot of the gate metal penetration distance vs. duration of anneal at 300°C.

In order to avoid interdiffusion effects on gate metal dislocation penetration, the anneal times were limited to short durations of 0.5 h. From the iso-chronal anneal study, XTEM samples from the gate region of the HEMTs were made and analyzed. HAADF-STEM imaging was used to image the progressive metal penetration as anneal temperature increased. The rate of penetration of the gate metal into the dislocations was calculated by measuring the penetration distance of the metal and dividing the penetration distance by the anneal time, 0.5 h. Using this

method, it is clear that with increasing anneal temperature penetration depth increased. Since the metal penetration is a diffusion based process as shown by the iso-thermal anneal sequence, then using the Arrhenius equation to plot the logarithm of the penetration rate against the anneal temperature would yield a linear fit whose slope is the activation energy. Indeed, this is the case. When these metal penetration rates are plotted on a semi-log graph as shown in Figure 34, the data appears approximately linear. Upon fitting a curve to the plot of the data, the activation energy for metal penetration was extracted, ~ 0.31 eV.

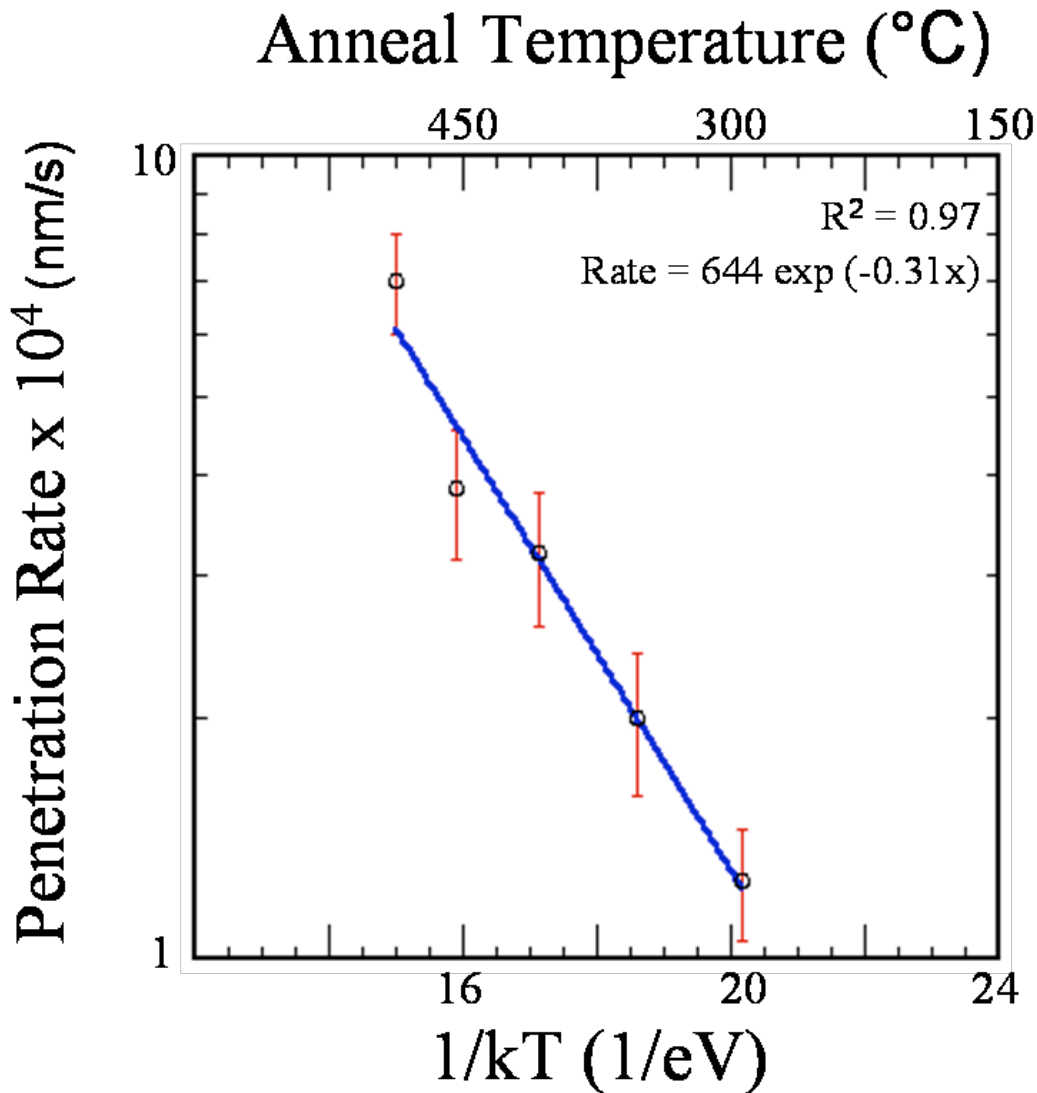


Figure 34 - Plot of the rate of metal penetration vs. temperature for 0.5 h iso-chronal anneals.

In addition to the structural imaging, pre-annealed and post-annealed devices were also characterized electrically in order to develop relationships between the change in structural properties (metal penetration and interdiffusion) to electrical changes. From the iso-chronal anneal study, HEMTs stressed for 0.5 h at 300°C, 400 °C, 450°C, and 500°C.

Changes to the V_T , I_D , and ohmic contact resistance, Ω , change due to thermal stressing are shown in Table 6. Here, the V_T shift is the relative change in V_T between the stressed and unstressed HEMTs. For example in the 400°C anneal, the $V_T = -0.96$ V before stress and $V_T = -1.22$ V after stress which resulted in the reported shift of -0.26 V. For the thermal anneals, it is shown that at 300°C there is almost no V_T shift; however, by 400°C the V_T shift is large but decreases in magnitude as the anneal temperature is increased to 500°C.

Table 6. Electrical data from 0.5 h anneals on Si(111) AlGaIn/GaN HEMTs

Temperature (°C)	300	400	450	500
V_T shift (V)	-0.03	-0.26	-0.16	-0.10
$I_D / I_D(0)$	0.98	1.33	0.79	1.19
$\Omega / \Omega(0)$	3.8	2.0	4.2	0.29
V_T shift (V) [Simulation]	~0	~0	~0	0.015
V_{FB} shift (V) [C-V]	-0.06	-0.15	-0.13	-0.12

For the normalized I_D change, the measured I_D during saturation at $V_{GS} = 0$ V after stress was divided by the measured I_D during saturation at $V_{GS} = 0$ V before stress. Thus, if the I_D is larger post stress, the normalized $I_D > 1$, and if the I_D is smaller post stress, the normalized $I_D < 1$. Additionally, all stress temperature $> 300^\circ\text{C}$ resulted in a larger I_D except the 450°C annealed sample. Furthermore, as the temperature increased, the change in I_{DS} decreases. This is mostly likely due to the shift in V_T discussed earlier and not the change in Ω . As the V_T shifts more positive with temperature, the gates will be more depleted at $V_{GS} = 0$ V which will lower the I_D . For the HEMTs, Ω change is equal to Ω (stress)/ Ω (unstressed). Ω increased when thermal

stress was $< 500^\circ\text{C}$ and decreased when $> 500^\circ\text{C}$. This might explain the outlier at 450°C as Ω doubles which would halve the I_D . However, Ω in general does not follow the change in I_D .

In order to better understand the effect the gate metal penetration had on the V_T and I_D alone without the effects from interdiffusion, a simulation was performed using the Florida Object Oriented Device Simulator [Liang1994, Law1998]. Here, the gate was modified so that a small piece penetrated the AlGaIn epilayer. Due to system restrictions, the penetration was approximated to be rectangular instead of triangular as would be observed in a XTEM image due to the defects hexagonal pyramid shape. Also, the 3D features of the gate were normalized to the 2D simulation grid. The derivation of these 2D features from the 3D HEMTs is shown in Appendix B. Lastly, measured electrical data was used to calibrate the simulated results to actual device performance.

An image of the simulated gate design for no gate metal penetration, 5 nm wide x 2.4 nm of penetration, and 5 nm wide x 3.5 nm of penetration are shown in Figure 35 A – C, respectively. Figure 35 B corresponds to the penetration from the 500°C for 0.5 h anneal, and Figure 35 C corresponds to the penetration from the 300°C for 24 h. For these penetration depths, the simulated shifts in the V_T are 0.015 V and 0.042 V, respectively. Since the 500°C for 0.5 h had the deepest penetration in the anneals for 0.5 h and simulation shows only a 0.015 V change in V_T , it can be concluded that the negative shift in V_T from the 0.5 h anneals is not from the metal penetration. However, this shift could be due to the Ni-Au interdiffusion, a change in the charge distribution in the interfacial layer, a change in the surface or buffer states due to annealing, or a possible change in the Fermi level pinning of the gate contact. These results indicate that the gate metal penetration causes very little change in the V_T and is not the primary factor for the shift.

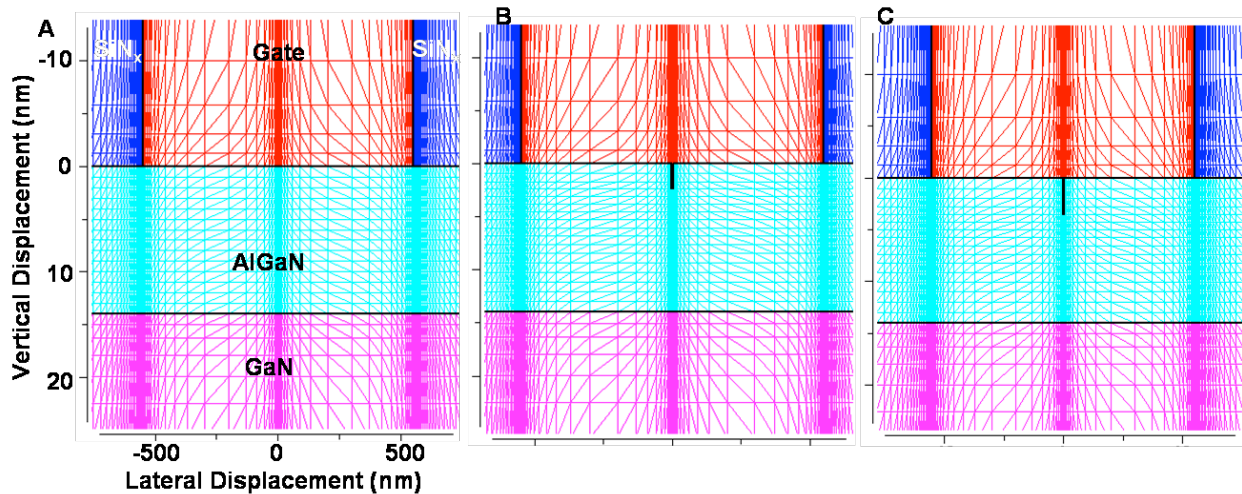


Figure 35 - Gate structures used in simulations to determine the effect of gate metal penetration on HEMTs.

Because the simulations could not explain the shift in V_T for the HEMTs, C-V measurements were performed to measure the change in V_T and effective E_F . From the C-V measurements, the change in flat-band voltage, V_{FB} , was measured. The V_{FB} is defined as:

$$V_{FB} = \Phi_{MS} - Q_f C^{-1} - \epsilon^{-1} \int_0^t \rho(x) x dx$$

where Φ_{MS} is the difference in work function between the metal and semiconductor, Q_f is charge in the interface and the layer, C is the capacitance of the layer, ϵ is the permittivity of the layer, t is the thickness of the layer, and $\rho(x)$ is the charge density within the layer. However, Φ_{MS} can vary due to Fermi level pinning; therefore, the specific change in Φ_{MS} from these measurements cannot be ascertained as they may vary due to pinning. Additionally, the change in trap charges in the interface and the layer cannot be separated from the possible change in Fermi level pinning or the change in the metal work function due to Ni-Au interdiffusion. Thus, the ΔV_{FB} could be due to multiple factors. Additionally, V_T depends upon the V_{FB} . Thus,

$$\Delta V_T \sim \Delta V_{FB} \text{ (C-V measured)} + \Delta V_T \text{ (simulation)}$$

C-V measurements were completed before and after thermal anneals of 0.5 h at 300°C, 400°C, 450°C, and 500°C at 1 MHz. The shift in the V_{FB} was calculated for each anneal and is listed in Table 6. Interestingly, the shifts in the V_{FB} match the trend shown by the shift in the V_T between 400°C and 500°C. Both show a large negative spike in the voltages at 400°C and continue to shift more positive towards zero net change as the temperature increases to 500°C. This indicates that the shift in V_{FB} and therefore ‘effective E_F ’ is responsible for the shift in V_T , as the only change in V_T shown by the gate metal penetration from the simulations was only slightly positive. Thus, continued work into isolating the effects of thermal anneals on the change in ‘effective E_F ’ need to be completed to further explain this mechanism.

Nanocracks Formed at the Ohmic Contacts

Analysis of the ohmic contacts of as-fabricated and electrostatically stressed AlGaIn/GaN HEMTs indicates the presence of nanocracks oriented along the [11-20] directions, which nucleate at metal inclusions present under the alloyed ohmic contact metal. These cracks nucleate as a result of a tensile hoop stress which accompanies the biaxial compressive stress induced in the AlGaIn of the ohmic contact regions when metal inclusions form as a result of the ohmic contact annealing process. (Figure 36) Cracks which form at the edges of these contact regions can extend into the channel region. The maximum of the crack length distribution was used to calculate that a 780 MPa residual tensile stress exists due to pseudomorphic mismatch between the AlGaIn layer and the relaxed GaN. Electrostatic stressing appears to induce additional growth in the longest cracks present within the channel regions of these devices and it seems feasible that cracks which extend under the gate electrode of the device may undermine the rectifying nature of this contact. (Figure 37)

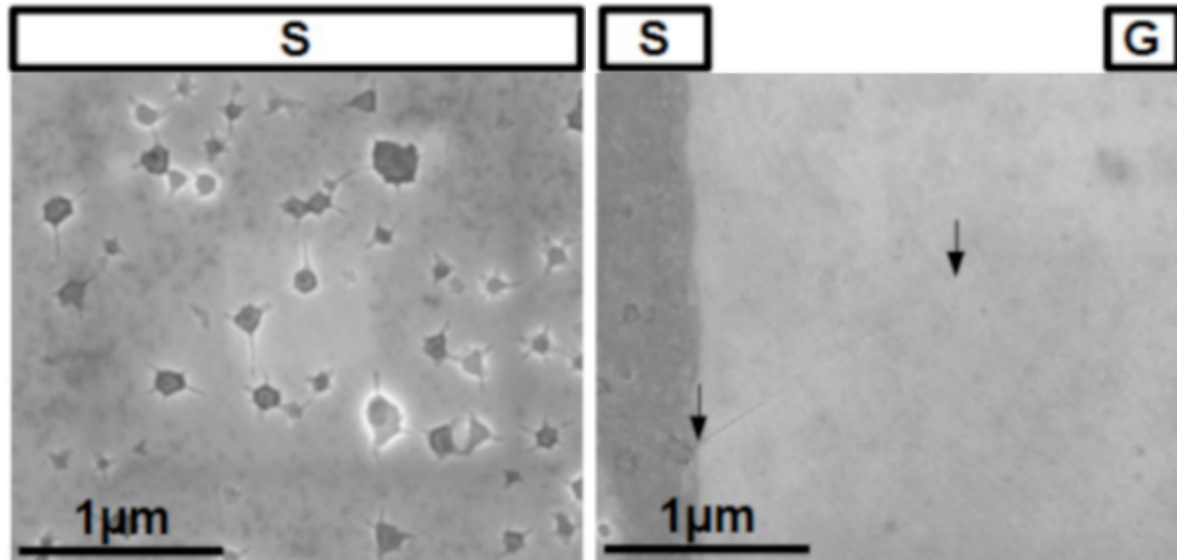


Figure 36 Top-down SEM analysis of the ohmic contact regions of an AlGaIn/GaN HEMT. These ohmic contacts were formed via an anneal at 850°C for 30s (left) The wholesale formation of metal inclusions throughout the contacted surface. Cracks can be seen nucleating on the faceted corners of the metal inclusions. (right) Cracks which nucleate at the edges of the ohmic contact regions can extend into the channel for much longer distances.

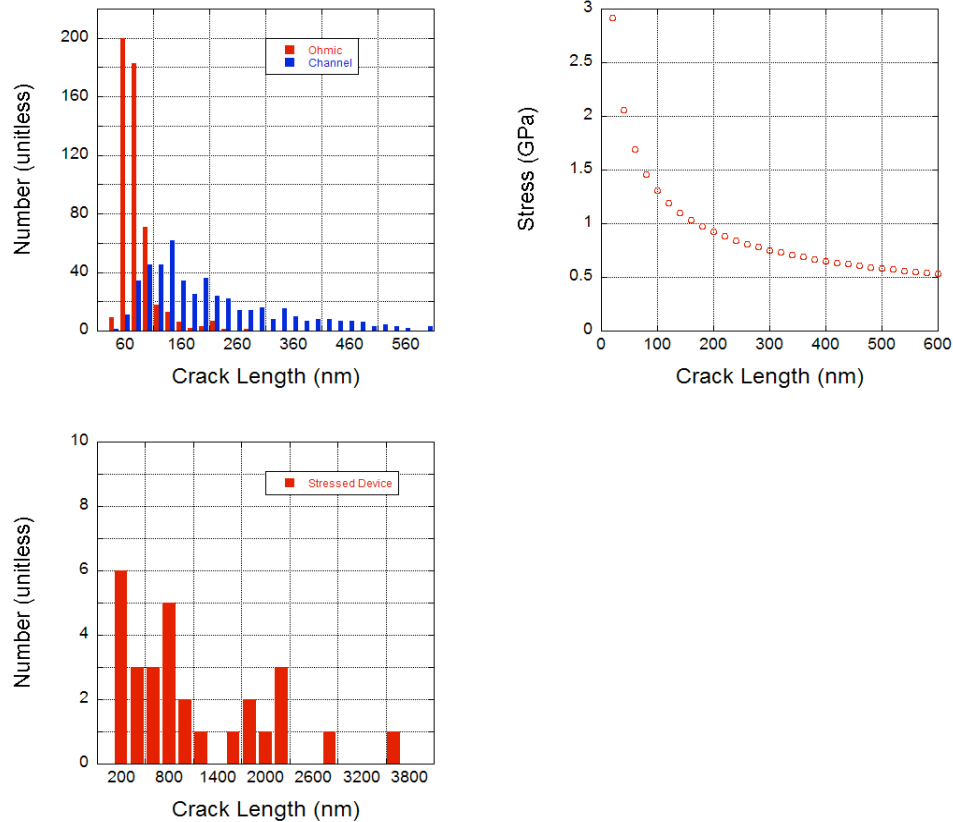


Figure 37 Histograms of crack lengths observed in 20 HEMT devices. (top) The crack length distributions associated with cracks found under the ohmic contacts as well as in the channel of the device are shown. (middle) The tensile stress required to induce additional crack growth for given crack lengths is also shown. (bottom) A histogram of crack lengths observed in a HEMT device which was electrostatically stressed at $V_{DS} = 15V$ from $V_{GS} = -10V$ to $V_{GS} = -42V$ at $-1V/min$.

(b) Banding Defect Formation

Analysis of Ni-gated AlGaIn/GaN HEMTs which were electrostatically stressed at potentials below, equal to, and above V_{CRIT} , while at $V_{DS} = 5V$, indicates the activity of two separate defect formation mechanisms. At potentials well above the critical voltage, a pitting defect is observed. This pitting defect is associated with electrochemical reactions between the AlGaIn underlying the gate metal with the Ni of the gate and oxygen present in the ambient.

At potentials approaching the critical voltage, a new defect, termed "banding", is observed at the interface between the AlGaIn and the Ni gate. This banding defect is a region of dark contrast in SEM corresponding to regions associated with the footprint of the gate contact and can be attributed to the formation of a thin insulating layer which is impervious to etching with BOE or TFAC. (Figure 38) It can be formed as a result of electrostatic stressing or as a result of thermal annealing at $500^{\circ}C$ for 30 minutes. Subtle differences in the morphology of bands formed from stressing and bands formed from thermal annealing suggest that temperature and electric field are both required for band formation.

The thickness of the band observed in SEM after electrostatic stressing and after thermal annealing is approximately equal to the thickness of the interfacial oxynitride present between the gate electrode and the AlGaN surface. While the physical dimensions of the insulating layer are similar to the oxide layer formed as a result of processing of the HEMT, its chemistry differs dramatically from this interfacial layer. EELS (Figure 39) and EDS (Figure 40) indicate a conversion of the interfacial layer separating the AlGaN from the Ni gate from an oxynitride containing intermixed Ga and Al to an Al-based oxide. The structure of this interfacial layer remains amorphous both before and after its conversion to an aluminum oxide.

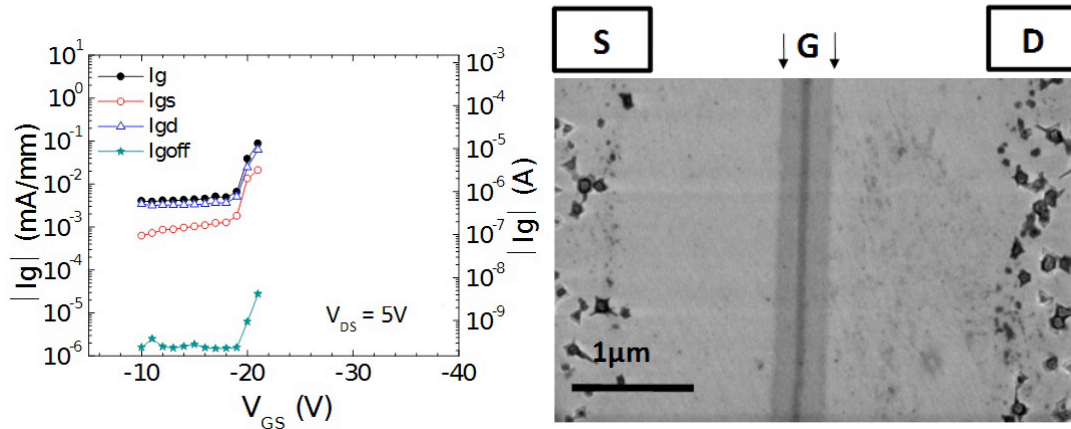
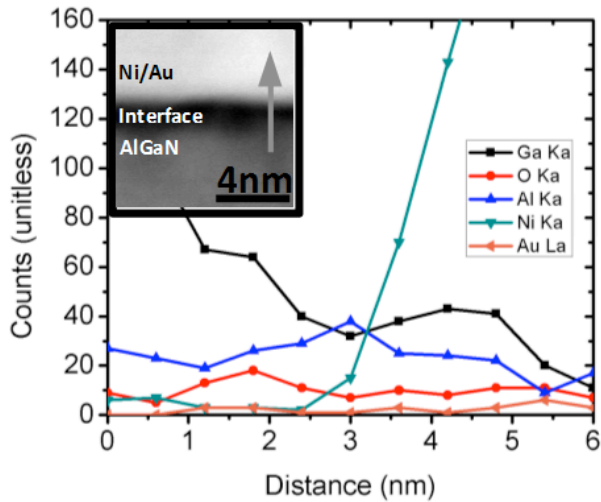
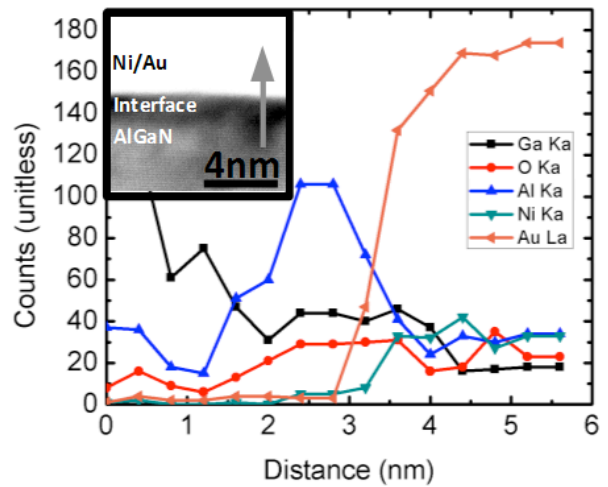


Figure 38 A plot of the gate degradation up to a voltage approximating V_{CRIT} . (left) At V_{CRIT} , the leakage current through the gate electrode both during stressing and in off-mode, increases by two orders of magnitude. (right) An exemplary scanning electron micrograph of the deprocessed surface of this stressed device. A pair of inset dark bands in the same aerial position as the t-gate are observed.



Control Sample



Anneal: 500°C for 30 min

Figure 39 An EDS linescan of the Ni/AlGaN interface before and after annealing. (left) Analysis of the linescan from a sample as-fabricated indicates that the EDS signals arising from Al and Ga are constant up through the interfacial region until they hit the Ni of the gate electrode. (right) An EDS linescan of this same interfacial region, after annealing at 500°C for 30s and deprocessing in an etch solution, indicates a segregation of aluminum into this interfacial layer. The EDS signal arising from the O K α line also appears to be enhanced.

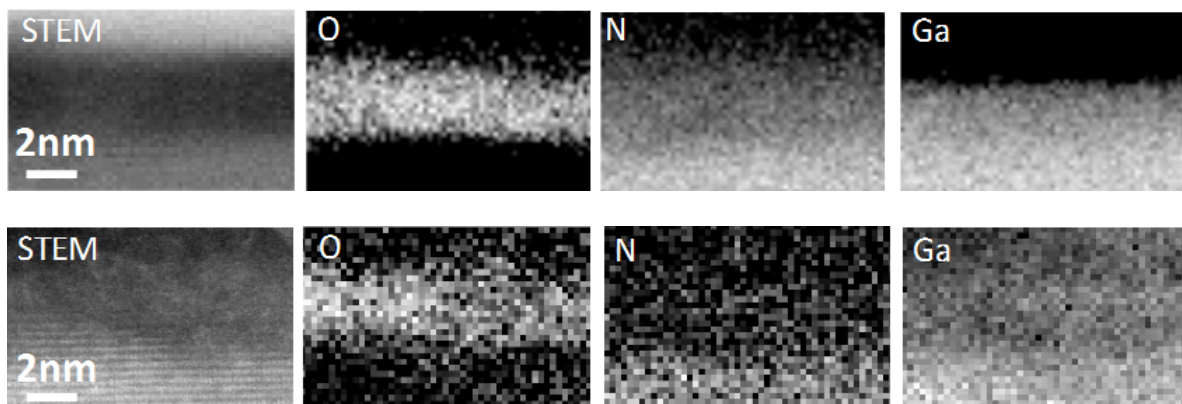


Figure 40 HAADF-STEM and EELS of the Ni/AlGaN interface before and after annealing. (top) Analysis of a lamella formed from an as-received sample indicates that the thin interfacial region separating the AlGaN and Ni gate is comprised of oxygen, indicating that a native oxide may have formed. (bottom) Cross-sectional DF-STEM, in conjunction with EELS, of a lamella formed from a sample annealed at 500°C for 30min and deprocessed, indicates that this layer remains oxygen rich, if somewhat more diffuse, after annealing.

Section 5 - Device Testing - Optical Pumping Characterization

Trap Determination with Current Transients

Two groups have recently employed current transient spectroscopy methods to determine trap activation energies [Joh 2008][Joh 2011][Joh 2008-2] [Tapajna 2010] in GaN HEMTs. Joh presented a methodology to analyze the trapping and detrapping behavior in GaN HEMTs that is amenable to integration with long-term stress experiments. The technique determines the layer location, energy level, and trapping/detrapping time constants of the dominant traps. In the trapping experiments, a bias voltage is applied, and the drain and/or gate currents are sampled at certain points in a logarithmic time scale to monitor the carrier trapping. Different bias points are used in order to induce different modes of trapping and at different locations in the device. These bias points include the ON-state (high I_D and relatively high V_{DS}) and $V_{DS} = 0$ state (relatively high negative V_{GS} with $V_{DS} = 0$). In the detrapping experiments, a trapping pulse in which both the drain and gate voltages are synchronously pulsed is first applied in order to induce carrier trapping. Immediately after removing the trapping pulse, the recovery transient of the current is captured and is analyzed through a curve-fitting procedure that extracts the dominant time constants.

Tapajna employed a similar method using a curve-fitting procedure that extracts the dominant time constants, but has a different process of trapping and detrapping. Drain current transients were measured at $V_{GS}=1$ V and $V_{DS}=0.5$ V after a one second filling pulse of $V_{GS}=-10$ V and $V_{DS}=0$ V. Before any measurements were made the device under test was illuminated with above band-gap light as trap clearing technique.

Optical Pumping

When a device is exposed to sub band-gap light, traps in the lower half of the band-gap are filled while traps in the upper half are emptied. Figure 41 illustrates how the photon energy of blue-light (2.7 eV) illumination affects traps within the band-gap of GaN. When illuminated, traps in the upper half of the band-gap, between the conduction band (3.4 eV in GaN) and the dotted line (0.7 eV) in Figure 41 have enough energy from the light to de-trap the carrier into the conduction band. At the same time traps between the valence band and the solid line (2.7 eV) are filled with carriers from the valence band.

Figure 42 illustrates the impact on traps in the band-gap with four different wavelengths of light: red (650nm, 1.91eV), green (532nm, 2.33eV), blue (445nm, 2.79eV), and violet (408nm, 3.04eV). When GaN is illuminated with red light, traps below 1.91eV are filled with electrons from the valence band, while traps with activation energies above 1.91eV empty trapped electrons into the conduction band. When the GaN device is subsequently exposed to green light, only traps between 1.91eV and 2.33 eV are affected. Under these excitation conditions, they will be filled instead of emptied. The same effect occurs for green to blue wavelengths, with traps between 2.33eV to 2.79eV no longer emptied but filled, and likewise for illumination from blue to violet, affecting traps between 2.79eV and 3.04eV. By recording the change in drain current between illuminations, the effects of traps filled to by each wavelength is measured.

For example, if the post-stress drain current response to red and green light decreased, but blue and violet increased, then the trap creation occurred in the blue range. The red and green illumination would have an emptying effect on the newly created traps, making them electrically

active and decreasing the drain current, while blue and violet would fill the newly created traps, thus removing their effect on the channel and increasing the drain current.

By evaluating the device's response as described in the previous example, the active energy of newly created traps can be determined. Throughout the literature, several different types of line and point defects have been observed with a range of mid-gap energies [Reshchikov 2005] [Diaz-Guerra 2006] [Liu 2005] [Neugebauer 1994] [Wu 2008] [Albrecht 2008] [Yamamoto 2003] [Limpijumnong 2004]. By using light sources of different wavelengths and recording the drain current response to their illuminations, mid-gap traps are populated and identified. Not only are energies of mid-gap energies determined but an understanding of the trap type may be identified.

Trap Detection Experiments

The devices are biased in the on-state while the device is in saturation. The typical bias point is $V_G=0$ and $V_D=5$ at 30°C . Recordings in these experiments included ten seconds of data prior to exposure, one minute of illumination of the device's top-side, and several minutes of post-exposure to capture the decay to the steady state values. The device temperature is regulated using Peltier modules and a PID controller, since temperature stability is critical to minimize thermal effects.

After recording a device's baseline, i.e., the initial trap densities, the devices are then electrically stressed. Post-stressed measurements are compared to the baseline to determine if new traps have formed, along with their activation energies, derived from the photon energy of the pump wavelength. Since many trap activation energies have been studied and identified, the different trap types such as point defects (vacancies, interstitials, substitutional defects and complexes thereof), stacking faults, and edge dislocations can be identified based-on the photon energy applied.

Results

AFRL Devices.

The bias stress results fall into three categories – no degradation, gradual degradation, and abrupt failure. The devices that showed degradation as a result of electrical stressing had two different responses to subsequent optical pumping. As expected, devices that did not degrade (see Table 7) showed no differences between the baseline optical pumping results and the post-stress tests. Devices that failed abruptly had minimal changes between the baseline and post-stress test optical pumping response (see Table 8), which supports the hypothesis the failure mechanism in these devices is contact-related, whereas devices that gradually degraded had remarkable responses to the optical pumping characterization (see Table 9).

In order to get a sense of how traps affect carriers in the channel, Tables 7-9 include the number of carriers affected by the change in traps. The number of carriers can be determined by calculating the resistivity of the channel from R_{ON} , which in this case is the drain voltage divided by the drain current.

$$\rho_{ch} = R_{ON} \frac{A}{l} = \frac{V_D A}{I_D l}$$

The area, A , is the channel width ($300 \mu\text{m}$) and the channel height (3 nm). The length, l , is the source-drain spacing of $4 \mu\text{m}$. Once the resistivity is known, then n , the number of carriers can be calculated, assuming the mobility, μ , is the same and using the average value for these

devices, $1907 \text{ cm}^2/\text{Vs}$. The mobility of a device is expected to change as the device degrades with the addition of newly formed scattering points. Although this change in mobility affects the calculation, its effect is minimal with respect to the order of magnitude.

$$n = \frac{1}{\rho_{ch}\mu q}$$

The shaded area of the optical pumping plots in Figure 43 and Figure 44 delineates the response of the drain current when the device was illuminated with a specific wavelength of light. The figures show the superposition of all the responses to the individual wavelength exposures.

The plots in Figure 43 compare the optical pumping response of a typical device that failed abruptly, where the drain current remains relatively stable for a couple of hours and then declines in a short period of time. The corresponding response to the optical pumping is unremarkable, with the pre-test and post-tests almost identical. Some of the devices that failed in this fashion showed a gradual decline before the abrupt change and the optical pumping also reflected minimal changes.

The typical response of a device that gradually is shown in Figure 44, the drain current response to the optical pumping shows a remarkable change when illuminated with blue and violet light, showing the creation of new trap states.

Generally, the most dramatic changes during optical pumping occurred when the devices were illuminated with blue, violet, and UV light. In these cases, the drain current response to green and red illumination actually decreased after the DC-stress. This indicates the creation of new traps in the blue or violet energy ranges, since red and green illumination would empty the newly created traps, thus making them active and lowering the drain current response.

Vendor A Devices.

The two devices stressed from Vendor A also underwent optical pumping characterization. The responses from these two devices were distinctly different than that of the AFRL devices as shown in Figure 45. Both devices responded nearly identically in that the only change occurred during UV illumination. This result suggests the device did not degrade as a result of the creation of new traps but from other mechanisms. Notice also the reduction in drain current under red and green illumination. This is the opposite response to the AFRL devices that demonstrated an increase in drain current under red and green illumination. This decrease in current is the result of emptying hole traps causing an decrease in band bending near the 2DEG and thus a reduction in carrier concentration.

Discussion of optical pumping characterization

The optical pumping technique shows trap changes in the HEMTs as a result of DC-stressing. The devices that degrade slowly have remarkable changes in the response to optical pumping between the baseline test and the post-stress test. This suggests these devices have existing traps in the as-grown layer structure or created during processing and the density of these is increased by the electrical stressing until they affect the channel carrier density. A trap free material should exhibit no change in channel current when exposed to below bandgap illumination since the material should not absorb such light. For devices that showed little or no increases during green illumination, traps above the energy of green light 2.33eV , have increased

suggesting traps that have activation energies between the energy levels of green and blue light have increased and affect the device's performance.

Reshchikov and Morkoç [Reshchikov 2005] report that point defects with formation energies in the energy range between blue and green light include Ga_N substitutional and N_{Ga} substitutional defects, as well as Ga interstitial point defects. The optical pumping technique indicates these defects increase as a result of electrical stressing and are deleterious to device performance. It is interesting to note that there was no discernible change in the cathodoluminescence imaging or spectra from these samples post stress. This would indicate that the defects responsible for the increase in drain current response are non radiative defects (not light emitting). Typical non-radiative defects in GaN tend to be line defects like threading dislocation and stacking faults. These defects are abundant in GaN and tend to be high density at the GaN substrate interface. Under the device stress conditions, these line defects could become extended into the near 2DEG region or into the 2DEG (as several TEM micrographs published suggest) and result in the optical response observed.

Activation energies of evolved defects

Figure 46 shows ten minutes of trap emissions from an AFRL HEMT device after the device was illuminated by blue laser light. Since the decay is exponential in nature, we used a similar technique as in [Joh 2011] to fit the curve.

$$I_{decay} = \sum_{i=1}^n a_i e^{-t/\tau_i} + I_{ss}$$

I_{ss} is the steady-state current. τ is the individual time-constants of each trap and a is the amplitude of the individual exponent for the time-constant τ . By assigning an equally-spaced arithmetically number of τ 's and recessively solve for a to minimize the error as compared to the measured waveform. The curve is fitted and time-constants determined, the process is repeated for several temperatures to determine activation energies from an Arrhenius plot. This process is repeated for different wavelengths of light allowing different traps to manifest themselves based on the different energy stimulation. Because the decay is believed to be a result of trap emissions and as a form of current transient spectroscopy, the activation energies derived from this process are relative to the conduction band [Mitrofanov 2003].

Figure 47 show the amplitudes solved from the curve fitting algorithm. By inspection, the same peak appears at the different temperatures. By extracting the amplitudes for the time-constants at each temperature and plotting them on an Arrhenius plot, the slope of the data is the activation energy. Figure 48 shows the results of the analysis determining a trap with a time-constant of 260 seconds at 30°C and an activation energy 0.14eV, based on the curve fitting of the waveform decay in Figure 47. Published activation energy of 0.14eV corresponds to a carbon on a gallium site (C_{Ga}) [Levinshtein 2001], which is a common impurity point defect in MOCVD grown GaN.

The above process was repeated for green laser illumination resulting in two distinct time-constants of 35 and 162 seconds at 30°C with activation energies of 0.92eV and 0.96eV respectively. Researchers have estimated the energy levels of the main point defects in GaN through first-principles total-energy calculations based on density-functional theory relevant to nitrides [Van de Walle 2004] [Neugebauer 1994] [Limpijumnong 2004]. From their work, possible point defects in this energy range include antisite Nitrogen and Gallium (N_{Ga}) and antisite Nitrogen and Gallium (Ga_N). The high formation energy of the Ga_N antisite in n-type

GaN is energetically unfavorable, suggesting these defects at 0.92eV and 0.96eV are antisite N_{Ga} .

Table 7. Optical pumping results of AFRL devices that did not show electrical degradation.

Device	DC-stress Condition	ΔI_D (mA)					Comment
		carriers affected (10^{16} cm^{-3})					
		R	G	B	V	UV	
2218C	On State	0	-1.38	-2.04	-0.94	NA	Pre-stress noisy
	$V_G = 0, P_{CH} = 1W$	0	-8.04	-11.9	-5.48		
2318C	On State	0.01	0.44	1.24	-0.03	NA	
	$V_G = 0, P_{CH} = 1W$	0.06	2.56	7.22	-5.74		
2320D	Off State	-0.1	0.86	1.3	1.36	NA	Green traps created
	$V_G = -5, V_D = 20$	-0.6	5.01	7.57	7.92		
1330D	Semi-on State	-0.7	0.54	-0.56	-0.02	NA	
	$V_G = -2, P_{CH} = 1W$	-4.08	3.15	-3.26	-0.12		
1623C	Semi-on State	-0.15	1.68	1.93	0.88	3.74	Green traps created
	$V_G = -2, P_{CH} = 1W$	-0.87	9.79	11.24	5.13	21.8	

Table 8. Optical pumping results of AFRL devices that failed abruptly.

Device	DC-stress Condition	ΔI_D (mA)					Comment
		carriers affected (10^{16} cm^{-3})					
		R	G	B	V	UV	
1622D	On State	0.85	-1.67	0.87	1.32	NA	
	$V_G = 0, P_{CH} = 1W$	4.95	-9.73	5.07	7.69		
2124C	On State	-1.12	-2.87	0.34	1.76	NA	Both gradual and abrupt failure
	$V_G = 0, P_{CH} = 1W$	-6.53	-16.7	1.98	10.3		
2218B	Off State	-0.38	-1.89	-1.76	1.17	0.24	Both gradual and abrupt failure
	$V_G = -5, V_D = 20$	-2.21	-11.0	-10.3	6.82	1.40	
1330D	Semi-on State	-0.3	-1.18	-1.74	-0.79	NA	
	$V_G = -2, P_{CH} = 1W$	-1.75	-6.87	-10.1	-4.6		
1131C	Semi-on State	-0.15	1.68	1.93	0.88	3.74	Green traps created
	$V_G = -2, P_{CH} = 1W$	-0.87	9.79	11.24	5.13	21.8	

Table 9. Optical pumping results of AFRL devices that degraded gradually.

Device	DC-stress Condition	ΔI_D (mA)					Comments
		carriers affected (10^{16} cm^{-3})					
		R	G	B	V	UV	
1930C	Off State	-3.32	-5.8	-0.8	2.84	NA	violet traps created
	$V_G = -5, V_D = 20$	-19.3	-33.8	-4.66	16.6		
1128C	Off State: $V_G = -7,$	-0.87	-0.22	0.65	2.82	NA	blue, violet traps created
	$V_{D \text{ step } 1\text{hr}} = 15 \text{ to } 16$	-5.07	-1.28	3.79	16.4		
2224C	Semi-on State	-0.3	2.69	8.74	6.41	NA	green, blue, violet traps created
	$V_G = -2, P_{CH} = 1W$	-1.75	15.7	50.9	37.4		
2126D	Semi-on State	0.59	2.14	6.62	5.4	NA	traps of many energies created
	$V_G = -2, P_{CH} = 1W$	3.44	12.47	38.6	31.5		
1330D	Semi-on State	-1.2	-1.14	2.66	3.29	NA	blue, violet traps created
	$V_G = -2, P_{CH} = 1W$	-7.0	-6.64	15.5	19.2		
2220C	Semi-on State	0.48	2.28	3.74	4.46	NA	traps of many energies created
	$V_G = -2, P_{CH} = 1W$	2.8	13.28	21.8	26.0		
2220B	Semi-on State	-0.52	-1.29	-1.37	2.86	7.64	violet traps created
	$V_G = -2, P_{CH} = 1W$	-3.03	-7.52	-7.98	16.7	44.5	
1125C	Semi-on State	0.88	2.95	4.29	6.1	18.0	traps of many energies created
	$V_G = -2, P_{CH} = 1W$	5.13	17.2	25.0	35.5	105	
1126C	Semi-on State	-1.12	-1.86	-0.25	2.35	13.1	violet traps created
	$V_G = -2, P_{CH} = 1W$	-6.53	-10.8	-1.46	13.7	76.4	
2419C	Semi-on State	1.5	1.7	5.8	4.8	NA	traps of many energies created
	$V_G = -2, P_{CH} = 1W$	8.74	9.9	33.8	28.0		

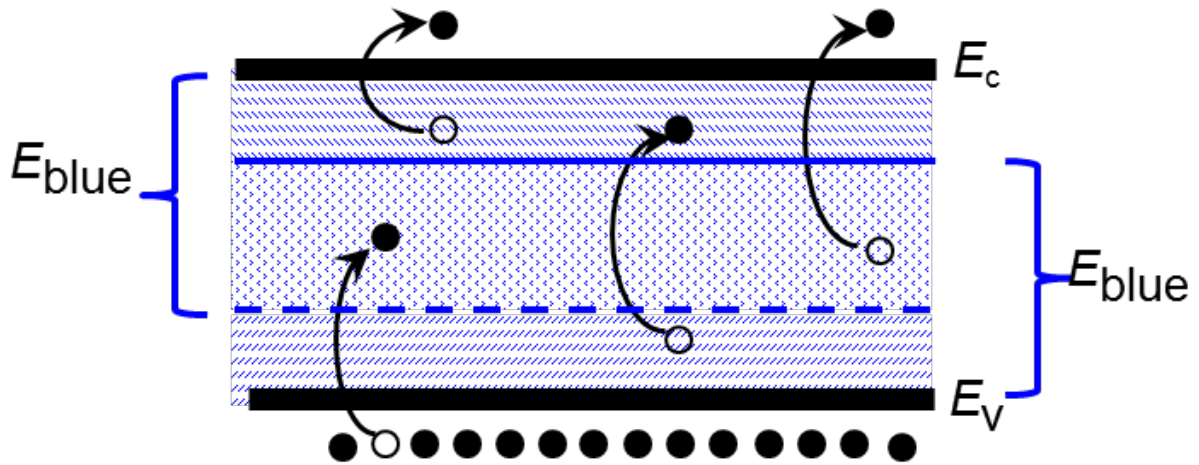


Figure 41. Schematic of the effect that blue light has on traps in the band-gap of GaN

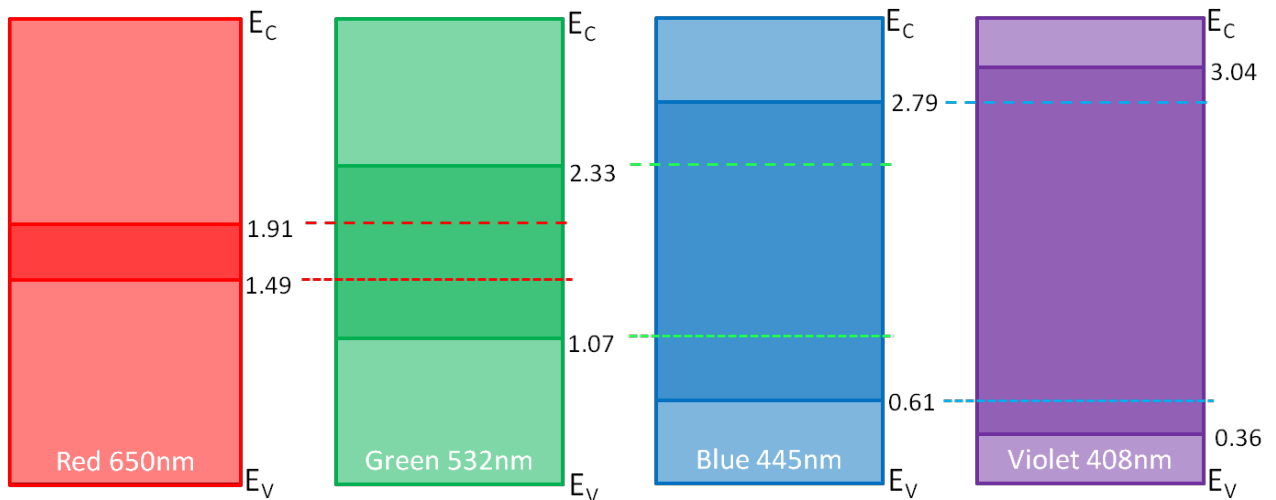


Figure 42. Effect on traps in the GaN bandgap when exposed by different wavelengths of light.

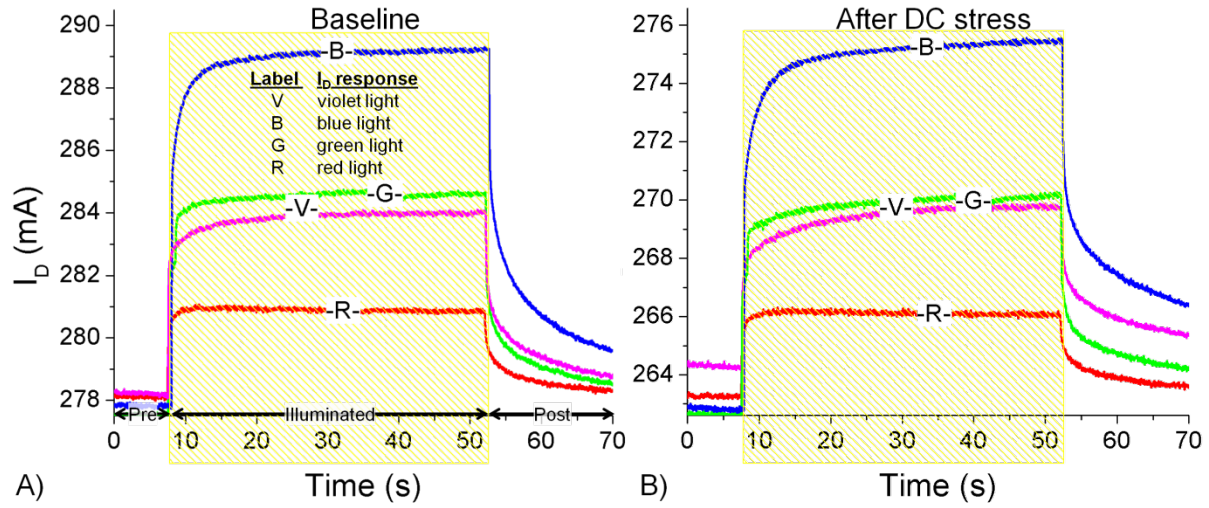


Figure 43. Typical response of a AFRL device exhibiting abrupt degradation. The shaded areas indicate the response when the device was exposed to light. A) The pre-test response. B) The post-test response.

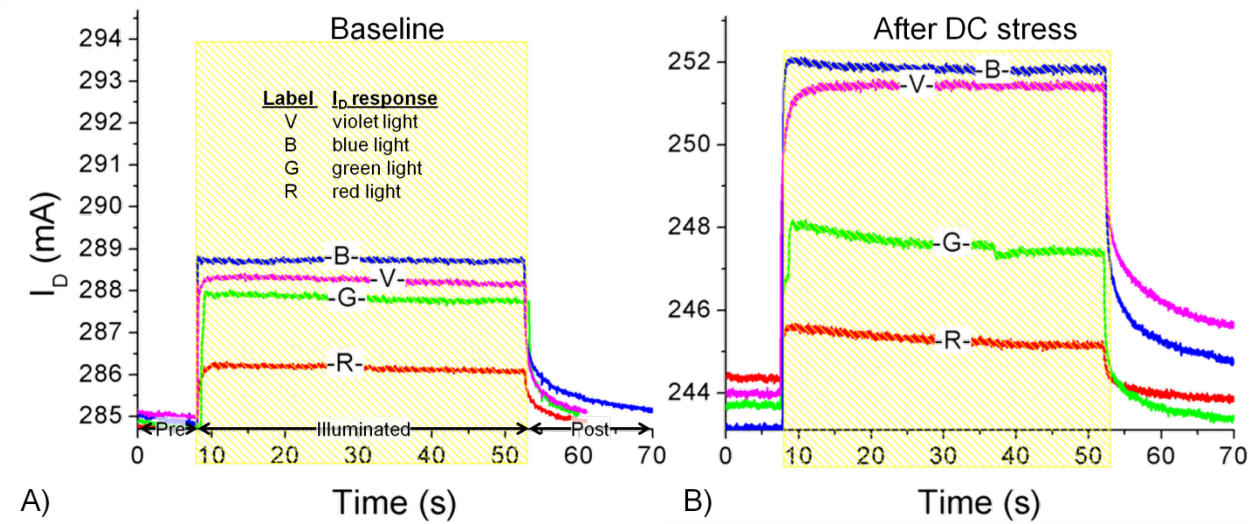


Figure 44. Typical response of an AFRL device exhibiting gradual degradation. The shaded areas indicate the response when the device was exposed to light. A) The pre-test response. B) The post-test response.

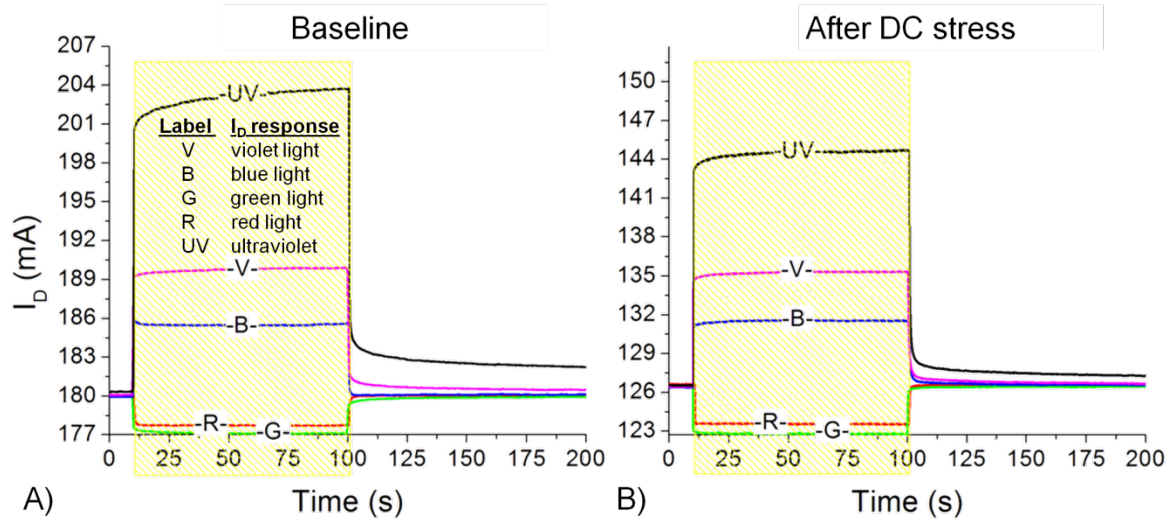


Figure 45. Typical response of a vendor A device. The shaded areas indicate the response when the device is exposed to light. A) The pre-test response. B) The post-test response.

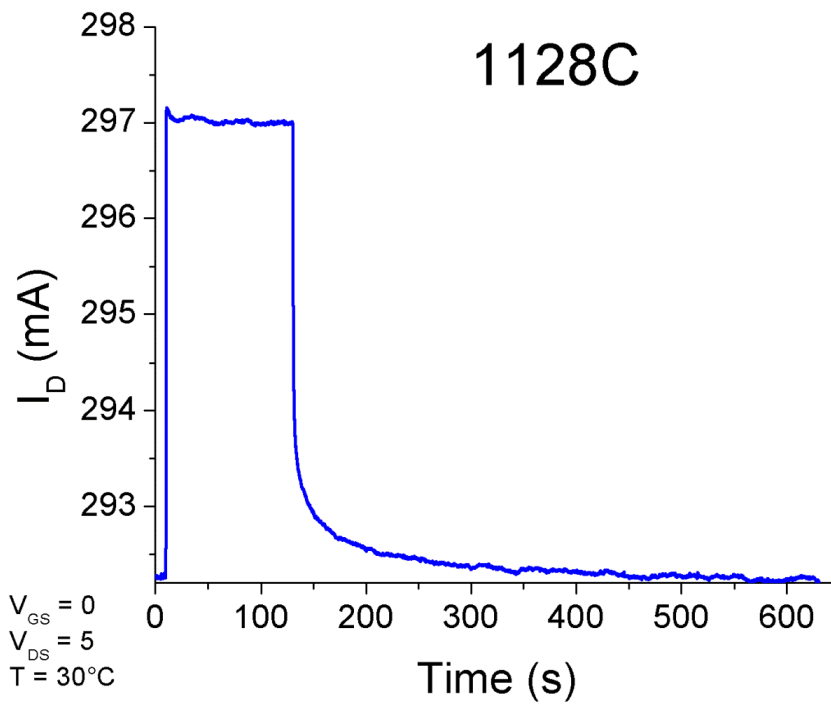


Figure 46. Decay of drain current after device was exposed to blue light.

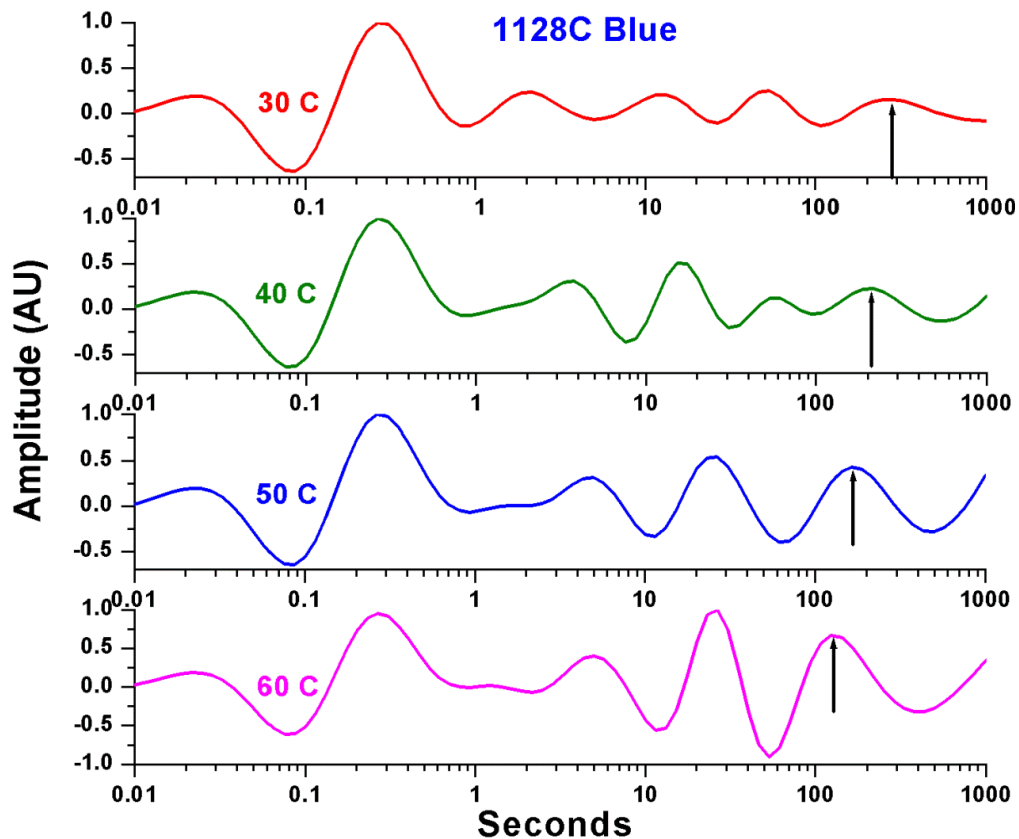


Figure 47. Amplitudes of exponential determined from the waveform decay shown in Figure 46 at four of the ten temperatures measured.

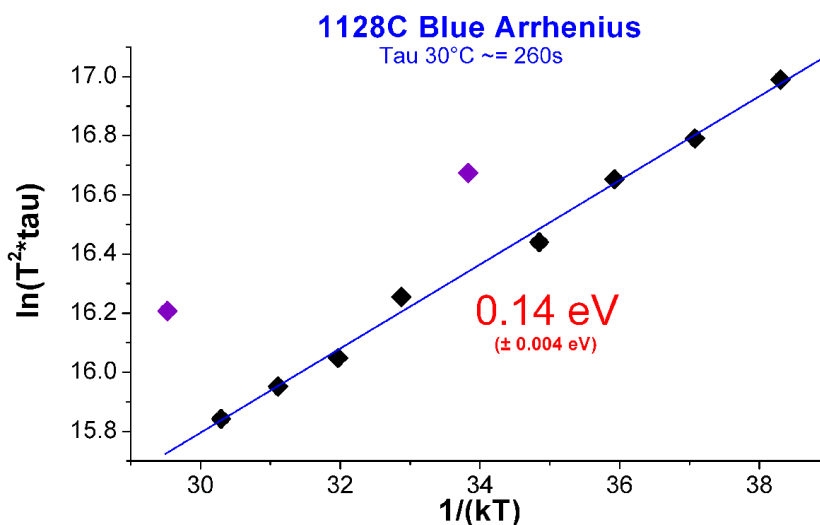


Figure 48. Arrhenius plot of the time constants shown in Figure 47. The resultant activation energy was 0.14eV.

Section 6 - Electrical Noise Characterization

The objective of this study was to understand the nature of defects which negatively impact the reliability of GaN HEMTs using low and microwave frequency noise measurements. A defect map of location, density and activation energy of defects is a powerful instrument for increasing device reliability via device geometry and material choice optimization.

In part 1 of our study fundamental noise sources were identified in AlGaIn/GaN HEMTs using simultaneous drain and gate current low frequency noise measurements. It was found that there is an extremely weak correlation between gate and drain current noise [Rao2009]. Drain current mainly stems from the gated channel region and shows a stable $1/f'$ noise without distinct GR noise components. A low value of Hooge parameter 10^{-4} is determined for it. On the other hand, gate current noise also exhibits a $1/f'$ noise with $S_{IG} \propto I_G^2$ dependence but shows in addition distinct unstable Lorentzian components. It was proposed that the Schottky contact is of high quality and does not degrade under device operation but factors like high electric fields, low defect migration barriers, high mechanical strain via inverse piezo-electric effect in the AlGaIn/GaN system create a possibility whereby, defect centers in AlGaIn barrier diffuse, evolve spatially or change their energy locations at room temperature.

In part 2 of our study the gate was stressed by applying reverse bias voltage. Temporary and permanent degradation of device characteristics were identified in stressed AlGaIn/GaN HEMTs. It was found that existing traps in the AlGaIn barrier layer contribute to the threshold voltage instability and change the drain current noise. The DC characteristics of the device fully recovered after several days. On the other hand gate current noise showed a permanent change which does not recover once the stress is removed. It was proposed that new defect states were created at gate edges via inverse-piezoelectric effect below the so called "critical voltage". The activation of mobile defects pointed to a defect movement or diffusion related mechanism at these early stages of degradation [Rao2010-1, Rao 2010-2].

In part 3 of our study the failure mechanisms in the channel were probed in more detail. It was found that hot carrier injection combined with self-heating was a dominant cause of degradation in the channel for ON-state stress conditions by increasing the trap density at the AlGaIn/GaN interface. Also the kinetics of the hot-carriers in GaN HEMTs was studied in detail by performing microwave noise spectroscopy. It was found that hot-electrons which exist in the channel are confined in the channel but have enough energies to generate new interface defects responsible for the observed degradation in ON-state stress. [Rao2011]

In part 4 RF failure mechanisms were probed by large signal AC stress. It was found that higher gate compression levels led to large forward gate biasing current which degraded the gate stack. New trap states are created right under the gate which degrade both the leakage current and output RF power. A point defect located at 4.5 nm under the gate and activation energy (EC-ET) of 0.9 eV was extracted from gate RTS noise measurements. These defects have been often reported to be related to the core of the dislocations or point defects loosely bound to dislocations [Rao 2012, Rao 2013].

Finally, room temperature gate leakage current and low frequency noise measurements as a function of gate bias voltage were carried out for different AlGaIn/GaN High Electron Mobility Transistors and interpreted in terms of space charge limited flow in the presence of shallow traps through very small area conductive leakage paths already present or formed under electrical stress in the gate stack device area [Xu2012, Xu2013]. This is not to say that tunneling assisted transport through other sections of the gate stack does not take place. However, the scattering

and space charge limited flow dominates the DC and noise characteristics. Transport parameters for electrons following these paths were extracted, and the observation of gate electron velocity saturation in stressed devices indicates that newly created leakage paths form predominantly in high electric field gate edge regions. It has been shown that leakage paths already exist in as made, virgin devices but that electrical stress applied to the gate stack leads to the formation of new gate leakage paths in high field regions of the gate stack as figure 49 below illustrates.

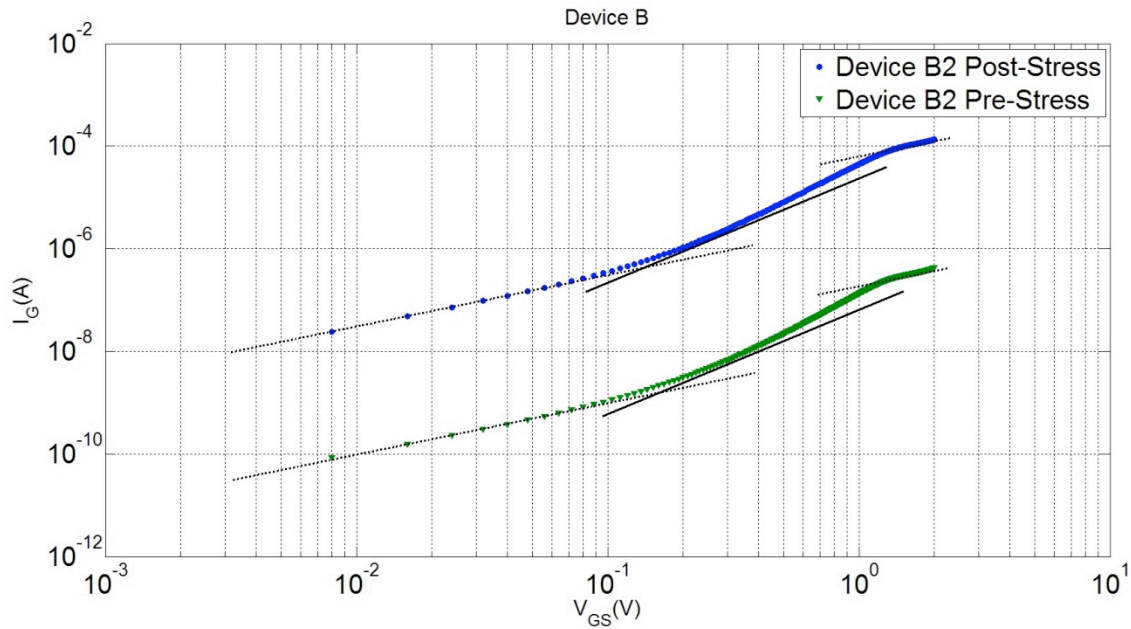


Figure 49: Measured gate current as a function of the magnitude of the gate voltage for device B2 before and after stress. Dotted lines represents fitting lines with slope 1 and solid lines have slope 2 characteristic for space charge limited flow.

Section 7 - Electrical Characterization

Electromechanical Characterization

7.1 Introduction

Mechanical strain resulting from lattice mismatch between the AlGa_N and GaN layers induces piezoelectric polarization. This polarization increases the two-dimensional electron gas (2DEG) sheet carrier density (n_s). Benefitting from mechanical strain, AlGa_N/GaN HEMTs are capable of achieving n_s greater than 10^{13} cm⁻², without intentional doping. This is significantly higher than other III-V systems due to strong piezoelectric polarization in the wurtzite GaN and AlN.

One of the most widely accepted theories explaining AlGa_N/GaN HEMT degradation is based on the inverse piezoelectric effect [Joh2006, Jungwoo2008]. During operation, the large vertical field under the gate creates strain in the AlGa_N barrier, adding to the existing strain from lattice mismatch. Once the strain surpasses the material's critical limit (at the critical voltage), relaxation will occur through crystallographic defect formation. These generated defects act as trapping centers for electrons, degrading performance and reliability. Large amounts of mechanical strain can certainly cause cracks and defects to form, however even nondestructive amounts of strain also can impact performance and reliability of the device. Strain reduces crystal symmetry, reorienting the energy band structure resulting in lifting of band degeneracies, shifting band energies, warping bands [Sun2007], and even altering trap energy levels [Son2008]. This can affect carrier mobility by changing conductivity effective mass, density of states, and scattering, as well as impacting reliability, by increasing gate current, and increasing hot-carrier effects [Dey2006].

Since stress is a major factor in the operation, performance, and reliability in AlGa_N/GaN HEMT devices, a thorough understanding of the impact of stress on performance and reliability can lead to improvements in device design. The effects of strain in Si MOSFETs are well understood and used to improve the devices. Mechanical wafer bending is a cost-effective method to study the effects of stress on semiconductor devices which has been extensively used to isolate and study the effect of stress in Si MOSFETs. In this MURI project, a systematic study of the effects of externally applied mechanical stress on the AlGa_N/GaN HEMT channel resistance and gate current was undertaken to provide insights into the physical mechanisms responsible for stress-related performance and reliability issues.

7.2 Strain and Stress

To obtain insight into the reliability of strained HEMT devices, it is necessary to consider the stress in HEMTs. First, built-in stress is discussed followed by an examination of the effect and use of externally applied mechanical stress as a HEMT performance and reliability probe.

7.2.1 Built-in Stress in HEMTs

Stress is an integral part of AlGa_N/GaN HEMT devices. Large mechanical stress profiles are created during fabrication and are generated during device operation. These stresses can impact device performance and reliability.

Lattice mismatch stress

In order for AlGa_N/GaN HEMTs to be commercially competitive with Si alternatives, low-cost, large-scale production must be achieved. Si (111) substrates offer advantages of low-cost, large size, and high quality over sapphire and SiC alternatives. However, large differences in lattice

constants (~17%) and thermal expansion coefficients (TEC) (~56%) between GaN and the Si (111) produce large strains, resulting in the formation of crystallographic defects [Rajagopal2003]. High quality GaN layers on Si, free of cracks and dislocations, have been fabricated through implementation of stress mitigation using transition layers [Rajagopal2003]. It is hypothesized that the lattice mismatch stress is primarily absorbed by the Al/Si interface, while the (Al, Ga) N transition layer absorbs the TEC mismatch stress, which occurs during processing [Rajagopal2003].

Another type of stress induced during fabrication is biaxial tensile stress in the AlGaN barrier layer. The thin AlGaN barrier is pseudomorphically grown on the relaxed GaN channel/buffer. Lattice mismatch between AlGaN and GaN induces a biaxial tensile stress in the AlGaN barrier. For an Al concentration of 26%, the AlGaN barrier has ~3 GPa of biaxial tensile stress induced. This stress is advantageous since wurtzite GaN and AlN grown in the (0001) orientation are both strongly piezoelectric [Ambacher1999]. The piezoelectric effect results in a polarization fixed charge at the AlGaN/GaN interface, inducing a mobile sheet charge layer which is termed a two-dimensional electron gas (2DEG). In addition, SiO₂ or Si₃N₄ passivation layers possess residual stress which also has been shown to induce stress, adding to the lattice mismatch stress and increasing the 2DEG density [Gregusova2005].

Inverse-piezoelectric stress

During operation, the vertical electric field under the gate contact induces additional stress in the AlGaN barrier through the inverse piezoelectric effect. This vertical field is the largest at the gate edges, where significant amounts of stress (500 MPa) can be generated in the AlGaN barrier during normal operation ($V_{GS} = 30$ V). This stress in addition to the lattice mismatch stress may vary the HEMT performance and reliability, and therefore has attracted researchers' attention in the past decade. It has been proposed that stress generated from the inverse piezoelectric effect can initiate defect formation leading to irreversible degradation [Jungwoo2008].

7.2.2 Wafer Bending Stress

Mechanical wafer bending is a simple and cost effective way to investigate the underlying physics of strain in semiconductors. Fabricating several wafers with varying amounts of process-induced stress is expensive. Furthermore, it can be difficult to accurately quantify the amount of stress present in the device. Also, modifying the process flow to alter the internal stresses can impact other characteristics of the device. Therefore, mechanical wafer bending is fundamental in performing controlled stress experiments. The external mechanical bending stress in this work is applied by using a flexure based four-point wafer bending system [Suthram2007], which achieves significantly improved uniformity of stress in the region between the inner load points.

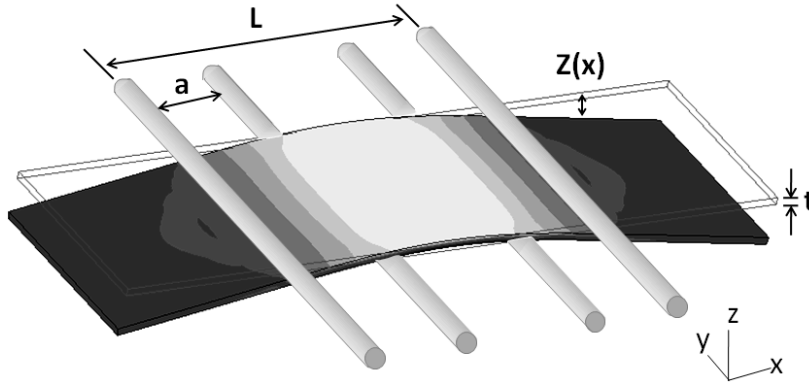


Figure 50. Illustrations of the four-point wafer bending setup for applying uniaxial stress. © [2008] American Institute of Physics, [reprinted with permission from M.Chu et al., “Comparison between high-field piezoresistance coefficients of Si metal-oxide-semiconductor field-effect transistors and bulk Si under uniaxial and biaxial stress”, J. Appl. Phys., vol. 103, pp. 113704, Fig. 3 and Fig. 5, June 2008]

In the four-point bending system, a beam is supported by two anchored points while being deformed by two driving loads as shown in Figure 50. Between the center two rods, the sample is bent with a constant radius of curvature resulting in uniform stress. Therefore, unlike cantilevers and three-point bending, variation of device position does not affect the accuracy of the measurements. The magnitude of uniaxial stress on the top surface of a homogenous material sample between the center two rods can be calculated by [Timoshenko1976],

$$\sigma = \frac{EZt}{2a \left(\frac{L}{2} - \frac{2a}{3} \right)}$$

where E is Young’s modulus along the stress direction, Z is the sample vertical displacement, t is the thickness of the sample, a is the distance between the inner and outer rods, and L is the distance between the two outer rods.

In this work, AlGaIn/GaN HEMT samples were diced into $\sim 1 \text{ cm}^2$ size to maximize the number of measureable samples. However, the samples are smaller than the minimum size that can be directly bent in the four-point wafer bending setup. To apply stress to these small samples, we developed a technique to bend small wafer samples in the standard flexure based wafer bending setup.

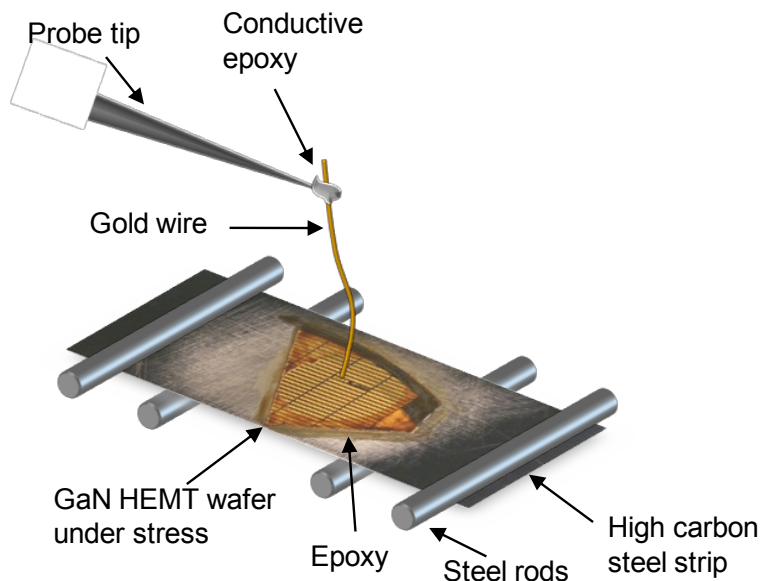


Figure 51. GaN wafer sample attached to heat treated high carbon stainless steel inserted in a four-point bending setup.

This technique of applying mechanical stress to a small AlGaN/GaN HEMT wafer sample starts by attaching the wafer sample to a heat treated high carbon stainless steel plate (Figure 51). First, the steel strip was sanded with fine grit sand paper to remove oxidation and to provide a rough surface for adhesion. A thin layer of Epoxy Technology H74 two part epoxy was then applied to the middle of the steel strip. The wafer sample was placed on top of the epoxy and pressed down, and excess epoxy was wiped away. To eliminate air pocket formation during curing of the epoxy, a metal washer was placed on top of the wafer sample, and the sample was clamped with a metal binder clip. Then, the sample was inserted into a 100°C oven for 5 minutes. The washer and metal binder were removed and the sample was placed on a 150°C hotplate for 5 minutes to complete the curing process. The sample attached to the steel plate was then inserted into the wafer bending setup. Under the amount of stress applied (360 MPa) in the experiments, the stainless steel plate does not permanently deform. A strain gauge is mounted on the top of the device with epoxy to calibrate the stress.

To characterize the impact of mechanical stress on the AlGaN/GaN HEMT devices, electrical measurements need to be taken while simultaneously varying the amount of applied stress. In order to achieve this, wires were attached to the device bond pads. Standard ball and wedge wire-bonding techniques resulted in delamination of bond pads destroying the device. Therefore, a technique was developed to attach wires to the bond pads without the use of heat or ultrasonic energy. First, a ball was formed on the end of a 1 mil Au wire in a ball bonding machine. Then, the wire was cut to approximately 1 cm length and removed from the ball bonder. A small amount of electrically conductive Epoxy Technology EE129-4 two part epoxy, was placed on the end of a probe tip. The probe tip was brought into contact with the end of the wire without the ball and cured for 24 hours at room temperature. The ball end of the wire was dipped in conductive epoxy and the probe tip was inserted into the micropositioner. Using the micropositioner, the ball end of the wire with conductive epoxy was landed on the device's bond pad and left to cure for another 24 hours at room temperature. After the epoxy cured, the

micropositioner was lowered to allow slack on the wire for displacement of the wafer while applying stress.

7.2.3 Gauge Factor

The gauge factor gives straightforward experimental information about strain-enhanced carrier mobility in semiconductors. This coefficient is defined as the normalized change in resistivity per unit strain,

$$GF = \frac{\Delta\rho}{\rho \cdot \varepsilon}$$
$$\rho = \frac{1}{q\mu_n n + q\mu_p p}$$

where ε is the strain and ρ is the resistivity, which can be calculated by the above equations.

For Si MOSFET under steady state, the electron and hole densities are approximately constant, thus its GF is determined by the change in carrier mobility with stress. For GaN HEMT, however, the 2DEG density may vary under mechanical stress, due to a change in polarization. As a result, its GF is determined by both the change in carrier mobility and carrier density. The gauge factor is a measure of the drive current enhancement under a particular stress, and therefore has been widely used to estimate strained device performance [Thompson2004].

7.3 Strain Effects on GaN HEMT Drain Current

7.3.1 Background

The effect of stress on channel resistance has been studied, due to its relevance for reliability issues such as hot electron injection as well as for strain sensors [Meneghesso2008]. Gaska et al. [Gaska1998] applied biaxial compressive stress to study its effect on channel electron density. Their work observed a decreasing electron density with compressive stress. Eichhoff et al. [Eickoff2001], Kang et al. [Kang2003,Kang2004], Zimmermann et al. [Zimmermann2006], and Yilmazoglu et al. [Yilmazoglu2006] applied mechanical stress to investigate the piezoresistive property of GaN HEMTs. A large variation in gauge factors has been reported in the literature, ranging from -4 to -40,000 [Gaska1998, Eickoff2001, Kang2004, Zimmermann2006, Yilmazoglu2006, Chang2009, Kang2005]. This large disagreement likely results from inaccuracies in resolving the applied stress and changes in the trapped charge density over the time elapsed during measurement. These past studies used three-point bending cantilevers [Zimmermann2006, Kang2005], complex lever mass system [Yilmazoglu2006], and circular membranes [Kang2004] to apply stress, which can be difficult to accurately quantify the amount of stress applied.

In our experiment, we use four-point bending, while mitigating the effects of trap charging/discharging to experimentally characterize the effect of stress on AlGaIn/GaN HEMTs. To better understand the stress effect on HEMT device channel resistance and accurately model the gauge factor, we also developed a simulation model by considering the stress-altered two-dimensional electron gas (2DEG) sheet carrier density and electron mobility. For the first time, uniaxial stress is incorporated into a sp^3d^5 empirical tight-binding model to investigate the stress effect on electron effective mass in wurtzite GaN.

Wafer samples were attached to heat-treated high-carbon steel plates with epoxy and stressed in a four-point wafer bending setup. Compressive and tensile uniaxial stress up to 360 MPa was applied longitudinal to the channel direction. To obtain an accurate measurement of the AlGaIn/GaN HEMT gauge factor, parasitic charge trapping transients and external resistances were addressed. After the effects of charge trapping were eliminated, and external resistances were accounted for, an accurate gauge factor measurement was performed [Koehler2010].

Experiment setup for stabilized measurements

To combat the instability issue associated with trapped charges, the HEMT device was exposed to light with photon energy near, but below, the band-gap of GaN (~3.4 eV or 365 nm wavelength) to photoionize all trapped electrons influencing the resistance measurement without band-to-band generation of electron-hole pairs. Initially, a mercury arc ultraviolet (UV) spotlight with peak wavelength of 377.7 nm or 3.284 eV was chosen to illuminate the device under test. A sweep of I_D - V_G under UV spotlight illumination compared to dark (Figure 52a) showed a large increase in off-state drain current and a decrease in subthreshold slope. The spectral intensity of the light source was measured in a spectrometer. A significant portion of the photon energy was above the band-gap of GaN (3.39eV ~ 365 nm) as shown in Figure 52b. Under illumination of above bandgap light, mobile electron-hole pairs are photogenerated. An increase in off-state current and a decrease in subthreshold slope are consistent with carrier photogeneration. A 380 nm band-pass filter was then applied to filter out wavelengths below 365 nm (Figure 53b). A horizontal shift in subthreshold slope and similar off-state leakage current (Figure 53a) verified a decrease in the effect of trapped charge without photogeneration of electron-hole pairs.

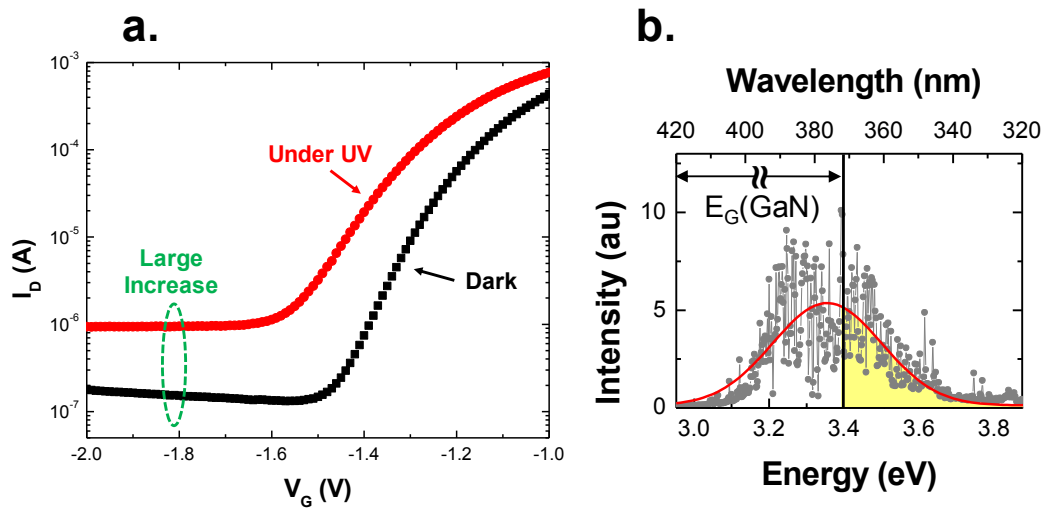


Figure 52. Unfiltered UV measurement (a) I_D - V_G measurements in dark and under unfiltered UV light with a large increase in off-state current and a decrease in subthreshold slope. (b) The spectral output of the unfiltered UV light.

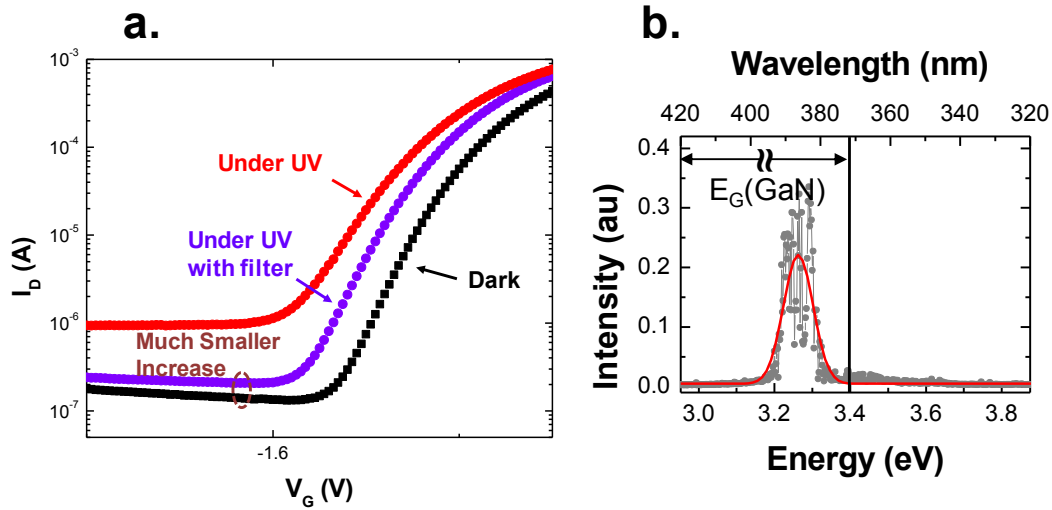


Figure 53. Filtered UV measurement (a) ID-VG measurements in dark and UV light filtered by a 380 nm bandpass filter with a much smaller increase in off-state current and no subthreshold slope change. (b) The spectral output of UV light with 380 nm bandpass filter.

A schematic of the experimental setup is shown in Figure 54. The standard wafer bending setup is illuminated by the UV light source. The band-pass filter is mounted in a 4 inch thick polystyrene heat shield to block ambient heat from the mercury arc lamp and block nonfiltered light from illuminating the device. As shown in Figure 55, over 1500 seconds, the change of the measured channel resistance is less than 0.02%. After the resistance measurement is stabilized, stress is applied to the HEMT device in order to extract the gauge factor.

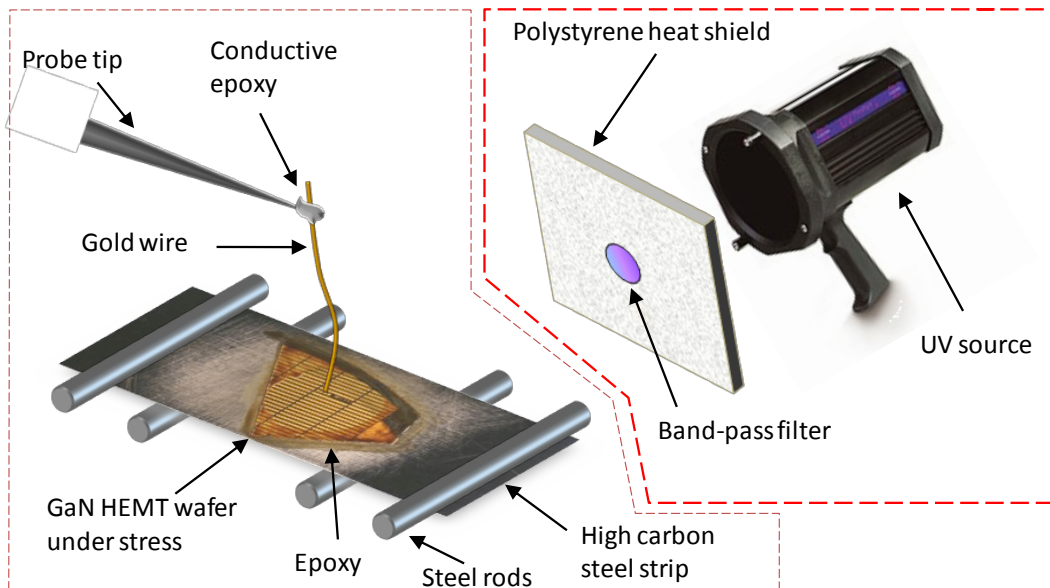


Figure 54. Experimental setup for photoionizing trapped charge to measure the gauge factor.

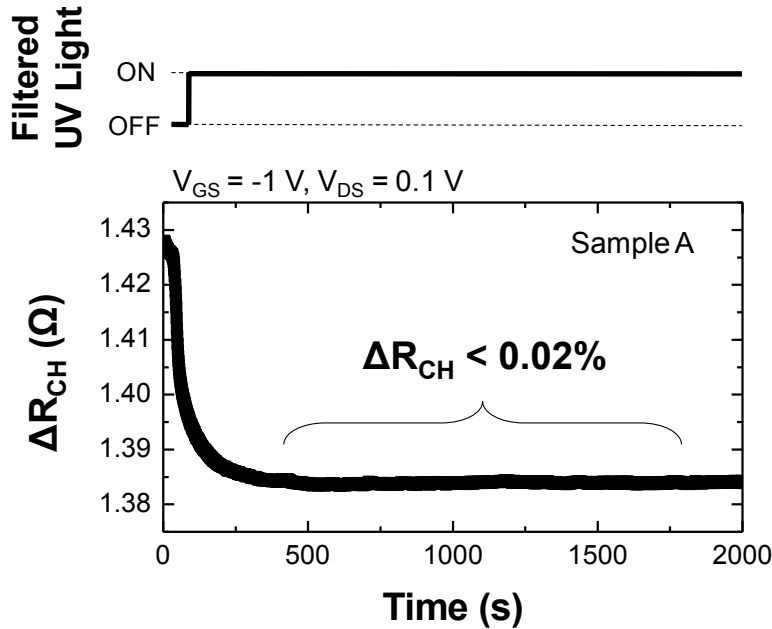


Figure 55. Illuminating the device under test with UV light stabilized RCH to less than 0.02% variation for 1200 seconds of measurement.

External resistance consideration

The stress dependence of the channel resistance (R_{CH}) is measured at $V_{GS} = -1V$ and $V_{DS} = 0.1V$, by excluding source/drain contact resistances. The high conductivity of GaN 2DEG results in a small channel resistance, especially for devices characterized with W/L ratio of 25. The measured resistance (R_{meas}) is the sum of the channel resistance (R_{CH}), source contact resistance (R_S), drain contact resistance (R_D), and external parasitic resistances (R_{ext}) and was on the order of 100 Ω .

$$R_{meas} = R_{CH} + R_S + R_D + R_{ext}$$

The source and drain contact resistances ($R_S = R_D = 5 \Omega$), measured by transmission line measurements, are subtracted from the measured resistance and are assumed to have a negligible stress dependence. A four-point Kelvin measurement is used to eliminate the effect of external resistances. Two wires were bonded to both the source and drain pad and one to the gate. One pair of source and drain contacts are used to supply a dc current via the force connections on the semiconductor parameter analyzer. The other pair of connections are used to sense the voltage drop across the source and drain pads.

Experimentally obtained gauge factor

Longitudinal uniaxial stress was varied in 60 MPa increments and held for 100 seconds at each interval. The normalized change in R_{CH} was measured for incrementally applied compressive and tensile stress up to 360 MPa, which was then released incrementally to zero as shown by the dotted lines of Figure 56. Tensile stress decreases R_{CH} , while compressive stress increases R_{CH} are seen by the solid experimental lines of Figure 57. At the maximum applied

stress (360 MPa), the normalized resistance change was $\sim 0.83\%/100$ MPa, which is much smaller than what is observed in (001)/ $\langle 110 \rangle$ silicon nMOSFETs of $3.2\%/100$ MPa [Min2008]. The resistance returned to the initial unstressed value after increasing and decreasing the compressive and tensile stress. This demonstrates that the change in resistance observed is due to a reversible strain effect, opposed to charge trapping/detrapping transients.

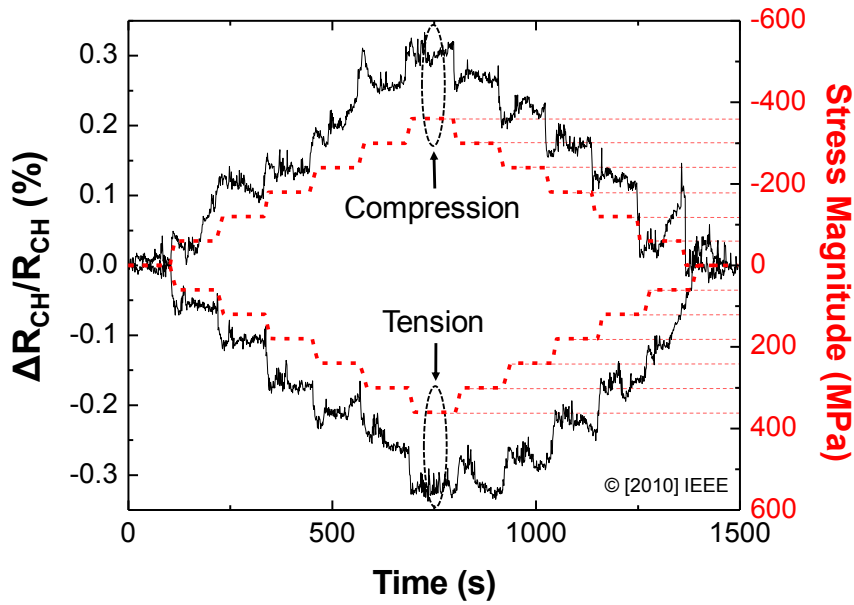


Figure 56. Normalized change in channel resistance with incrementally increasing and decreasing uniaxial stress. [Reprinted, with permission, from A.D. Koehler, et al., Extraction of AlGaN/GaN HEMT Gauge Factor in the Presence of Traps, IEEE Elec. Dev. Lett., vol. 31, pp 665-667, Figure 2, May 2010]

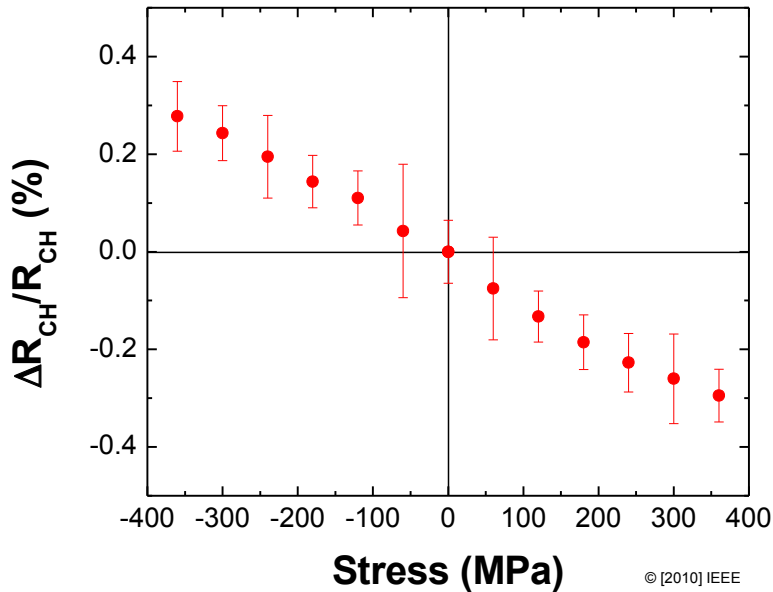


Figure 57. R_{CH} measurements at each time interval stress was held constant. Error bars represent a three standard deviation confidence interval for the measurement. [Reprinted, with permission, from A.D. Koehler, et al., Extraction of AlGaIn/GaN HEMT Gauge Factor in the Presence of Traps, IEEE Elec. Dev. Lett., vol. 31, pp 665-667, Figure 4, May 2010]

The gauge factor was determined by averaging the R_{CH} measurements over each time interval during which the stress was held constant (Figure 57) [Koehler2010]. Error bars represent a three standard deviation confidence interval for the measurement. The slope of a total least squares linear fit of the averaged R_{CH} versus strain curve was obtained to determine a gauge factor of -2.5 ± 0.4 [Koehler2010]. Total least squares analysis included uncertainty of the measurements. The determined gauge factor (-2.5 ± 0.4) is small relative to values in literature ranging from -4 to -40,000.

7.3.2 Theory and Modeling

The channel resistance of the AlGaIn/GaN HEMT device is inversely proportional to the 2DEG sheet carrier density (n_s) and channel electron mobility (μ_e) [Chu2010].

Stress dependence of 2DEG sheet carrier density

The 2DEG forms at the interface of the AlGaIn and GaN layers, arising from the total polarization difference between them [Ambacher1999]. There are two types of polarization: spontaneous polarization (P^{SP}) and piezoelectric polarization (P^{PE}). Spontaneous polarization exists in both AlGaIn and GaN layers, since their $\sqrt{c/a}$ ratio differs from the ideal

wurtzite crystal value ($\sqrt{8/3}$). Piezoelectric polarization arises from the piezoelectric

effect, which is proportional to the strain. In the “as-fabricated” AlGaIn/GaN HEMT structure, a

thin layer of strained AlGa_N due to lattice mismatch is on top of a thick layer of relaxed Ga_N. As a result, piezoelectric polarization exists only in the AlGa_N layer without external stress. Figure 58a schematically shows the total polarizations in the “as-fabricated” device. From the total polarization difference between the AlGa_N and Ga_N layers, $\sigma = P(\text{AlGa}_N) - P(\text{Ga}_N)$, the 2DEG sheet carrier density can be calculated using Equation (54) [Ambacher1999],

$$n_s(x) = \frac{+\sigma(x)}{q} - \left(\frac{\epsilon_0 \epsilon(x)}{dq^2} \right) [q\phi_b(x) + E_F(x) - \Delta E_C(x)]$$

where x is the Al content, σ is the total polarization difference between AlGa_N and Ga_N layers, ϵ is the dielectric constant, d is the depth of the AlGa_N layer, $q\phi_b$ is the Schottky-Barrier of a gate contact, E_F is the Fermi level with respect to the Ga_N conduction-band-edge energy, and ΔE_C is the conduction band offset at the AlGa_N/Ga_N interface. This work uses an Al-content of 0.26.

External mechanical stress affects the 2DEG density by generating additional piezoelectric polarization along the [0001] direction. Spontaneous polarization remains constant since it is an intrinsic material quality. When external stress is applied, additional piezoelectric polarization arises in both layers as shown in Figure 58b. The amount is proportional to the strain and piezoelectric coefficients ($P^{PE, mech} = e_{ij} \cdot \epsilon$). In this work, the AlGa_N and Ga_N layers are assumed to have the same level of strain, due to the fact that in most mechanical-bending experiment both layers of the AlGa_N/Ga_N HEMT are significantly thinner than the substrate and therefore are located near the top surface of the wafer. In addition, the piezoelectric coefficients of AlGa_N and Ga_N are similar. As a result, the difference between the strain-induced piezoelectric polarizations of these two layers is close to zero. Therefore, we expect that external stress has little effect on the 2DEG sheet carrier density.

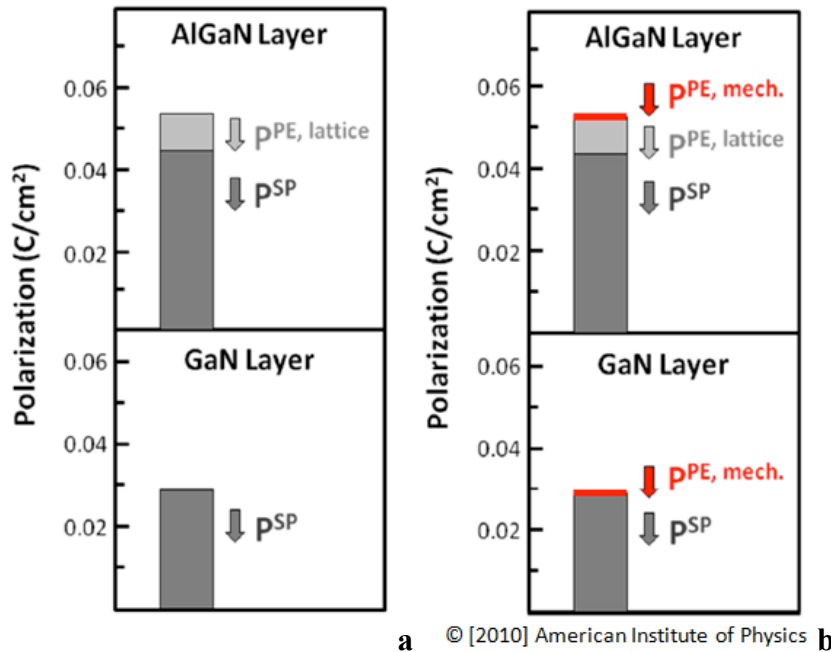


Figure 58. Illustrations of polarizations in the AlGa_N and Ga_N layers. A) For the as-fabricated Ga_N HEMTs. B) For the Ga_N HEMTs under mechanical bending stress. The mechanically applied stress generates additional piezoelectric polarization of similar magnitude in both the

AlGa_N and Ga_N layers. © [2010] American Institute of Physics, reprint with permission from [M.Chu et al., “Simulation of AlGa_N/Ga_N high-electron-mobility transistor gauge factor based on two-dimensional electron gas density and electron mobility”, J. Appl. Phys., vol.108, pp.104502, Fig.3, November 2010].

In this work, the simulation uncertainty is investigated by considering various elastic stiffness constants and piezoelectric coefficients of Ga_N and AlN listed in literature [Chu2010]. The uncertainty arising from the tight-binding parameters is neglected, since these parameters are achieved from an empirical tight-binding method that is considered to be accurate. The percentage change of 2DEG sheet carrier density is computed as a function of $[1\bar{1}20]$ tensile stress. An increase in n_s ranging from 0.09% to 1.4% for 500MPa is calculated depending on the coefficients' value used in the simulation. This small enhancement matches our expectation due to the fact that the additional piezoelectric polarization in AlGa_N and Ga_N layers mostly cancel each other out.

Stress dependence of channel electron mobility

Similar to the strained-Si analysis, the band structure of wurtzite Ga_N is the starting point of investigating strain related Ga_N HEMT behavior. Nido [Nido1995] and Jogai [Jogai1998] incorporated external stress into an empirical sp^3d^5 tight-binding model [Yang1995] to study the consequence of strain effects on the Ga_N band structure. Their work, however, considered only biaxial stress and focused mainly on the bandgap and valance band structure. Since the electron is the majority carrier in the Ga_N HEMT channel, it is essential to study the strain altered conduction band. In addition, uniaxial stress, which is the most beneficial stress for Si devices, is worth considering in Ga_N.

Electron mobility enhancement for bulk Ga_N can result from the average conductivity effective mass reduction and a suppression of intravalley scattering. Stress affects electron effective mass through two factors: band-splitting induced electron repopulation and band warping. Unlike Si, which has six degenerate conduction bands, or GaAs which has energetically adjacent conduction bands, Ga_N is a direct band-gap material with only one conduction band. As a result, no electron repopulation occurs under stress, and thus band warping is the only mechanism responsible for effective mass change. The absence of conduction band splitting also results in negligible change of the acoustic phonon scattering. The polar optical phonon scattering also has negligible dependence on stress, due to the fact that the mechanical stress does not induce polarization change along the longitudinal direction. Therefore, the change in effective mass through band warping is the dominant mechanism for stress-dependent bulk Ga_N electron mobility variation.

In a conventional Ga_N HEMT structure, the 2DEG is confined at the AlGa_N/Ga_N interface and electron energy is quantized. However, there will not be confinement induced sub-band splitting in Ga_N HEMT since Ga_N has only one single conduction band. Therefore similar to bulk Ga_N, the scattering rate change in strained-Ga_N HEMT remains negligible and the band warping induced effective mass variation should dominate its stress behavior.

We used an sp^3d^5 empirical tight-binding method developed in [Yang1995] to calculate the Ga_N band structure and electron effective mass. All nearest-neighbor s, p, and d interactions, as well as second-nearest-neighbor s and p interactions are included using two-center approximation [Slater1954], which results in a 26×26 Hamiltonian matrix. The tight-binding

parameters used in this work, including five on-site, one-center, eight nearest-neighbor two-center, and eight second-nearest-neighbor two-center integrals, are listed in Table IV of [Yang1995]. The GaN band structure is obtained by solving the eigenvalue of the Hamiltonian matrix. The electron effective mass is then calculated along the Γ -M, Γ -K, and Γ -A directions in the reciprocal lattice.

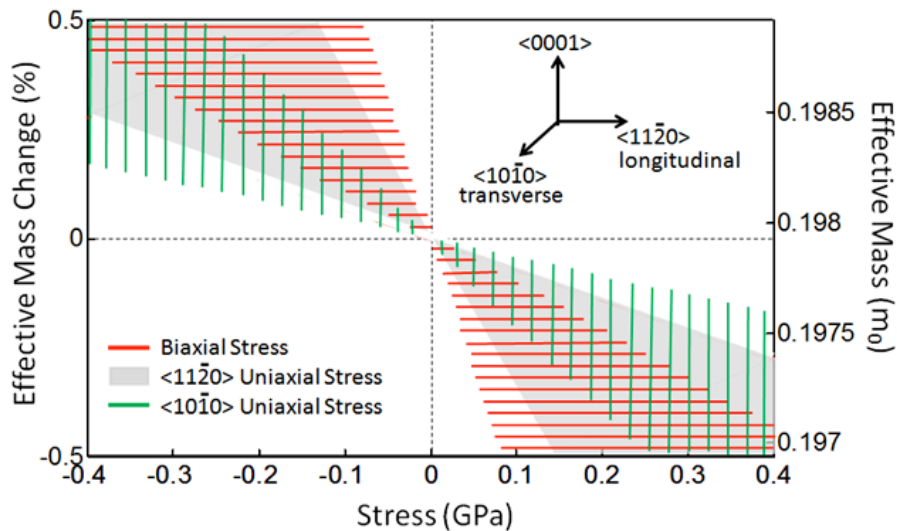
The effect of mechanical stress is incorporated into the tight-binding model by considering the strain-induced change in atom location, which results in varied bond length, bond angle, and reciprocal lattice. In this work, in-plane biaxial stress and uniaxial stress along the x and y axis are considered.

The stress effect on the electron effective mass along the longitudinal, transverse, and out-of-plane directions are calculated and the results are plotted in Figures x-10a-c, respectively.

Here we consider the $[1\bar{1}\bar{2}0]$ $[11\bar{2}0]$ direction to be the channel direction. Therefore, the

longitudinal, transverse and out-of-plane directions refer to the $[1\bar{1}\bar{2}0]$, $[10\bar{1}0]$, and $[0001]$

direction, respectively. The shaded areas in the plots include all possible simulation results considering simulation uncertainties. Without stress, the longitudinal, transverse, and out-of-plane effective masses are $0.198m_0$, $0.197m_0$, and $0.189m_0$, respectively, which agree with the results in [Yang1995]. For longitudinal effective mass, biaxial stress has a slightly larger effect than uniaxial stress ($\sim 3\%/500\text{MPa}$ under biaxial stress comparing to $\sim 1.5\%/500\text{MPa}$ under longitudinal stress). Similarly, transverse and out-of-plane effective mass also have a larger change under biaxial stress. For all types of stress, however, the changes in electron effective mass of GaN are much smaller than those of Si ($\sim 15\%/500\text{MPa}$ under $\langle 110 \rangle$ uniaxial stress [Chu2009]). This is because the subband splitting, which is an important factor affecting electron effective mass in Si, does not exist in GaN. The absence of band splitting and carrier repopulation in GaN causes the electron effective mass and thus mobility to only depend on conduction band warping, which is proved to be small through tight-binding calculations.



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a

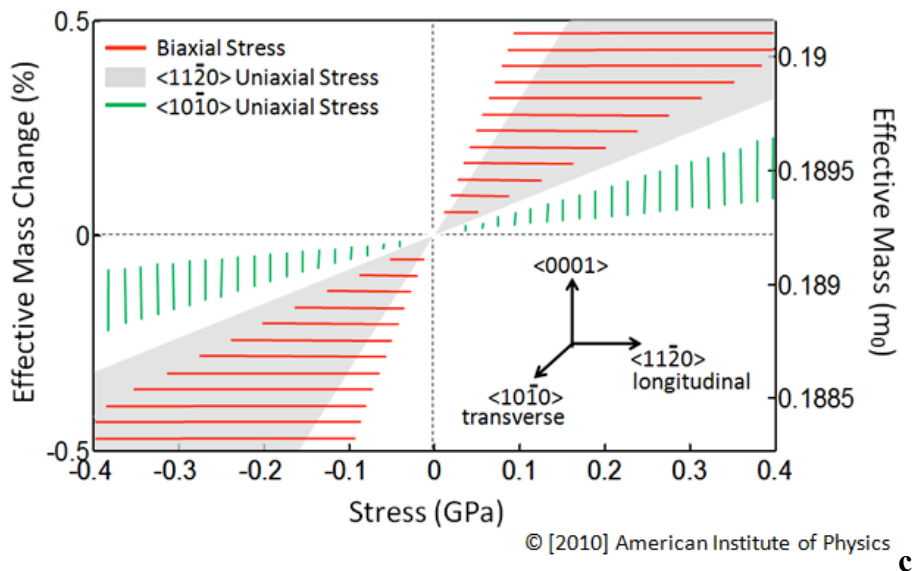
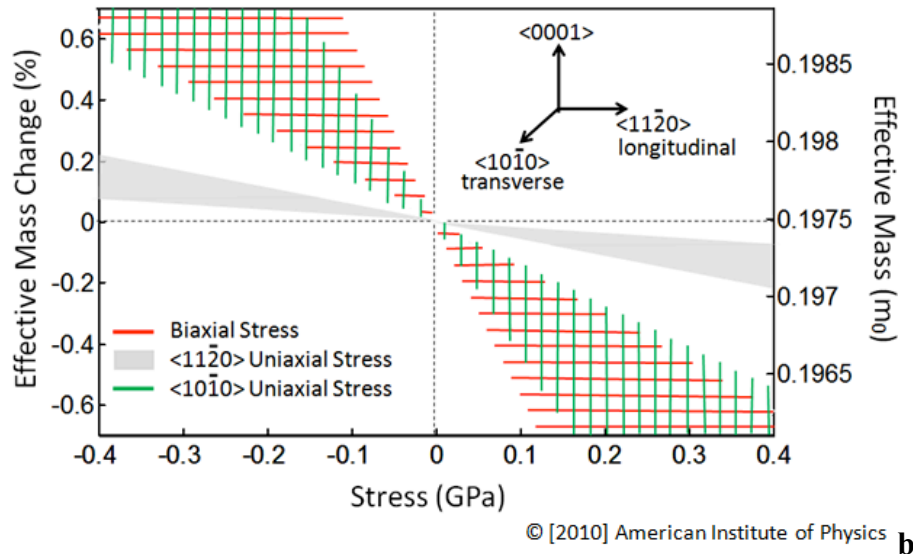


Figure 59. Change of electron effective mass under externally applied mechanical stress. (a) Longitudinal stress. (b) Transverse stress. (c) Biaxial stress. © [2010] American Institute of Physics, reprint with permission from [M.Chu et al., “Simulation of AlGaIn/GaN high-electron-mobility transistor gauge factor based on two-dimensional electron gas density and electron mobility”, J. Appl. Phys., vol.108, pp.104502, Fig.7 (a), November 2010].

Modeling results for gauge factor

Combining the variation of 2DEG sheet carrier density and electron mobility, the stress-induced change in channel resistance of an AlGaIn/GaN HEMT is plotted in Figure 60. Simulation uncertainties are included. The simulation result is compared to our previous experimental result [Koehler2010], in which repeatable gauge factors were obtained after eliminating parasitic charge trapping effects. The simulated gauge factor is determined to be -7.9 ± 5.2 , compared to -2.5 ± 0.4 in experiment [Koehler2010] which is good agreement considering the range of published piezoelectric and elastic parameters for GaN and AlN. The

wide range of gauge factors listed in literature may be a result of the charge trapping/detrapping occurring over the elapsed time of measurements. Our result also agrees with the gauge factors of bulk GaN reported in [Eickoff2001, Bykhovski1996, Mingiacchi2002] with little variation (-1 to -3.6) that indicates negligible trapping effect.

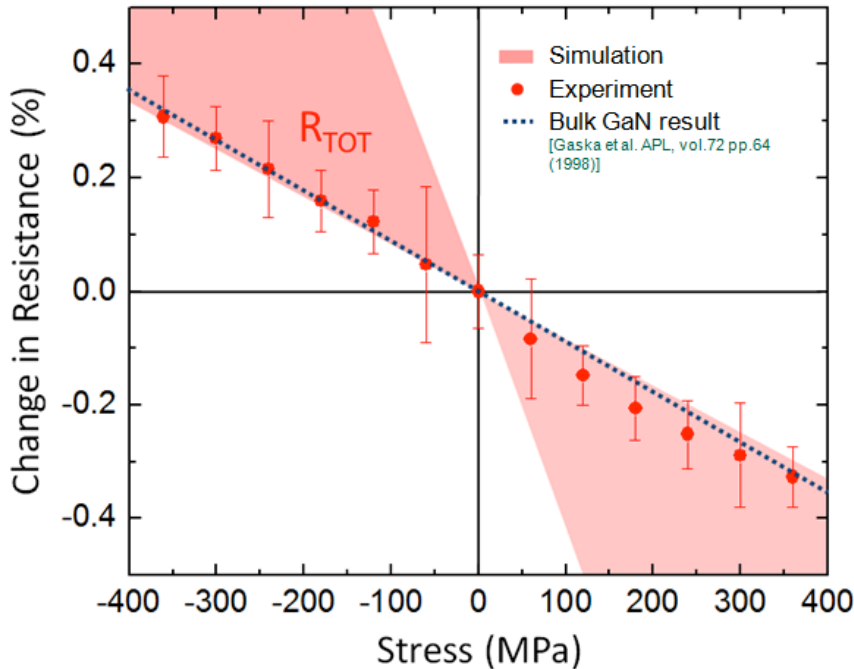


Figure 60. Change of GaN HEMT resistance (R_{TOT}) under longitudinal stress. Symbols represent experimental change in R_{TOT} [38] with uniaxial stress. © [2010] American Institute of Physics, reprint with permission from [M.Chu et al., “Simulation of AlGaIn/GaN high-electron-mobility transistor gauge factor based on two-dimensional electron gas density and electron mobility”, J. Appl. Phys., vol.108, pp.104502, Fig.8, November 2010].

7.4 Strain Effects on GaN HEMT Gate Current

7.4.1 Background

The physical breakdown of the AlGaIn barrier has been shown to occur at voltages beyond the critical voltage (V_{crit}), creating an irreversible increase in J_G [Jungwoo2008]. This type of degradation has been hypothesized to be related to the generation of crystallographic defects via the inverse piezoelectric effect [Jungwoo2008]. This creates additional tensile stress in the AlGaIn barrier, which adds to the pre-existing built-in tensile stress resulting from lattice mismatch between the AlGaIn barrier and the GaN layer. It has been suggested that when stress reaches the material critical limit, defects form in order to relax the internal elastic energy [Jungwoo2008]. These defects cause a low resistance leakage path through the AlGaIn barrier resulting in a sudden increase in J_G . A mechanical wafer bending experiment in literature showed a reduction of V_{crit} with applied tensile mechanical stress, however, only five pairs of devices were investigated in this study and a more comprehensive study is required [Jungwoo2007].

Several leakage mechanisms have been proposed in the literature to explain the GaN HEMT gate current at various temperature and field strength conditions. Zhang et al. [Zhang2006] noted that direct tunneling of electrons from the metal gate into the GaN bulk dominates the gate current measured at low temperature ($<130\text{K}$), while the gate current measured at room temperature or above follows the Poole-Frenkel Emission (PFE) trend. Mitrofanov et al. [Mitrofanov2004] also brought up a similar conclusion that PFE dominates the room temperature gate leakage. Yan et al. [Yan2010] proposed a defect band induced gate leakage mechanism which has similar form as the Poole-Frenkel Emission expression. Karmalkar et al. [Karmalkar2003] developed a bulk defect-assisted tunneling gate leakage model. In their model, the electrons undergo two thermal-assisted direct tunneling processes: from the gate to the trap and from the trap to the bulk GaN. They were able to reproduce their experimental results on various devices by using different sets of parameters including the defect level, defect density, and the Schottky barrier height. Sathaiya et al. [Sathaiya2006] proposed a similar two-step thermal-assisted tunneling model to be the dominant leakage mechanism in the GaN HEMT. Since stress is inherent in AlGaIn/GaN HEMTs, understanding the role of stress on J_G is essential to improve reliability. However, there are discrepancies in the published literature explaining the gate leakage mechanism of unstressed devices.

7.4.2 Measurement

Experiment setup

Wafer samples were attached to heat-treated high-carbon steel plates with epoxy and stressed in a four-point wafer bending setup. Compressive and tensile uniaxial stress up to 360 MPa was applied longitudinal to the channel direction. The stress dependence of the AlGaIn/GaN HEMT J_G was characterized at the $V_{DS} = 0$ state, isolating the effect of electric field induced by the gate. Various reverse biases (-0.1 V to -4 V) were applied to the gate and held constant until J_G reached steady-state to eliminate transient trapping effects before each measurement. At each bias, mechanical stress was incrementally applied then released, while simultaneously measuring J_G . High-temperature measurements were taken on a temperature-controlled probe station using sample stage heaters.

Experimental observations

Longitudinal stress, up to 360 MPa, was incrementally applied to the AlGaIn/GaN HEMT device while J_G was simultaneously measured over a period of 1800 seconds. Averaging J_G over 1800 seconds was done to account for random fluctuations in the measured current. It was found that a time duration of 1800 seconds while the stress was held constant was adequate to obtain a reasonable statistical confidence in the measured J_G . The normalized change in J_G due to applied stress ($\Delta J_G(\sigma)/J_G(0)$) was measured for several constant applied gate biases ($V_G = -0.1, -0.25, -0.5, -1, -2, \text{ and } -4\text{ V}$) using the above mentioned procedure. Figure 61 shows results of $\Delta J_G(\sigma)/J_G(0)$ for $V_G = -0.25\text{ V}$ and -4 V . The stress dependence of J_G was weaker at $V_G = -4\text{ V}$ than at $V_G = -0.25\text{ V}$. Tensile (compressive) stress increased (decreased) J_G for all applied gate biases. At each bias, after the compressive or tensile stress was applied to its maximum magnitude of 360 MPa, then the stress was incrementally released. Upon releasing the stress to zero, J_G returned to its initial, unstressed value. This demonstrates that the measured change in J_G is purely a reversible consequence of the applied stress, and not a transient effect. Also, it

demonstrates that the applied mechanical stress (up to 360 MPa) does not induce permanent damage to the device.

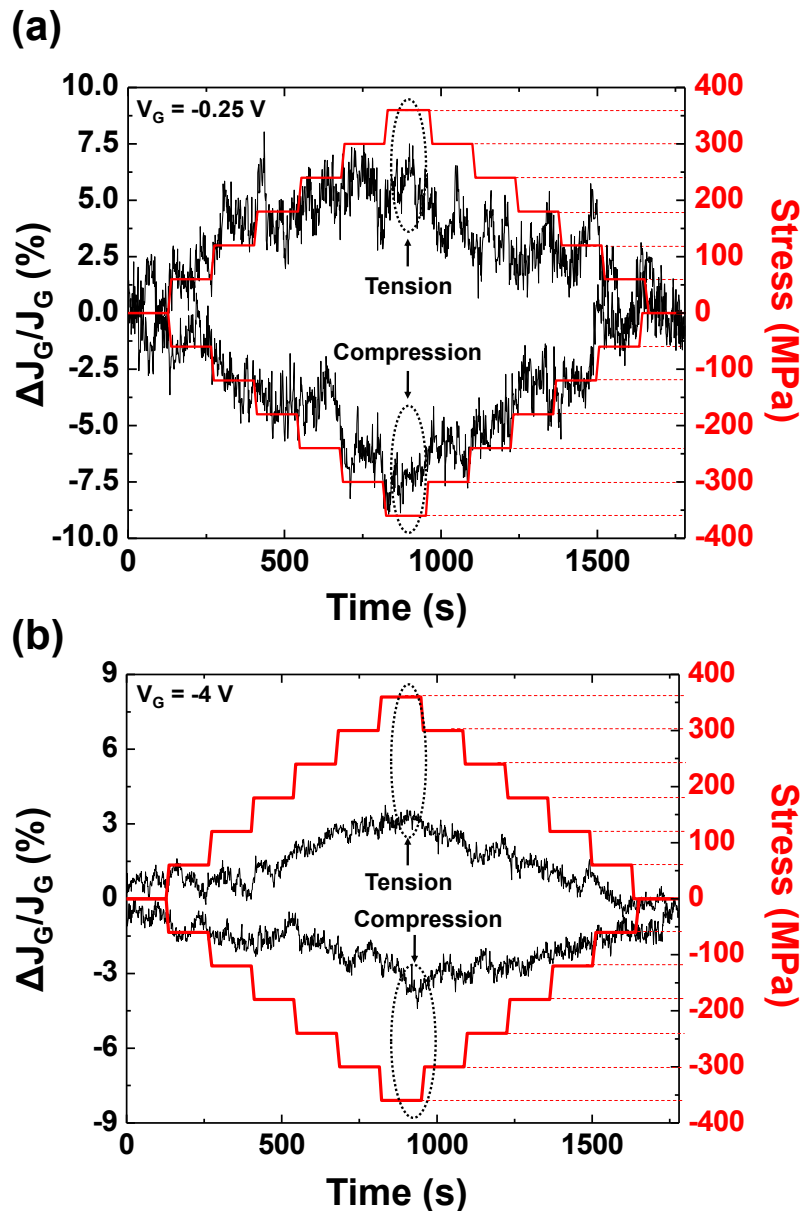


Figure 61. Normalized change in JG for incrementally increasing and decreasing uniaxial stress for (a) $V_G = -0.25$ V and (b) $V_G = -4$ V.

To quantify the magnitude of the normalized change in gate current density, $\Delta J_G(\sigma)/J_G(0)$, for each applied gate bias and stress level, J_G is averaged over the duration of time the stress was held constant. Figure 62 shows $\Delta J_G(\sigma)/J_G(0)$ averaged for all levels of compressive and tensile stress at $V_G = -0.25$ V and -4 V. Error bars representing the uncertainty in the measurement of $\Delta J_G(\sigma)/J_G(0)$ are three times the standard deviation of the J_G measurements over the duration when the stress was held constant.

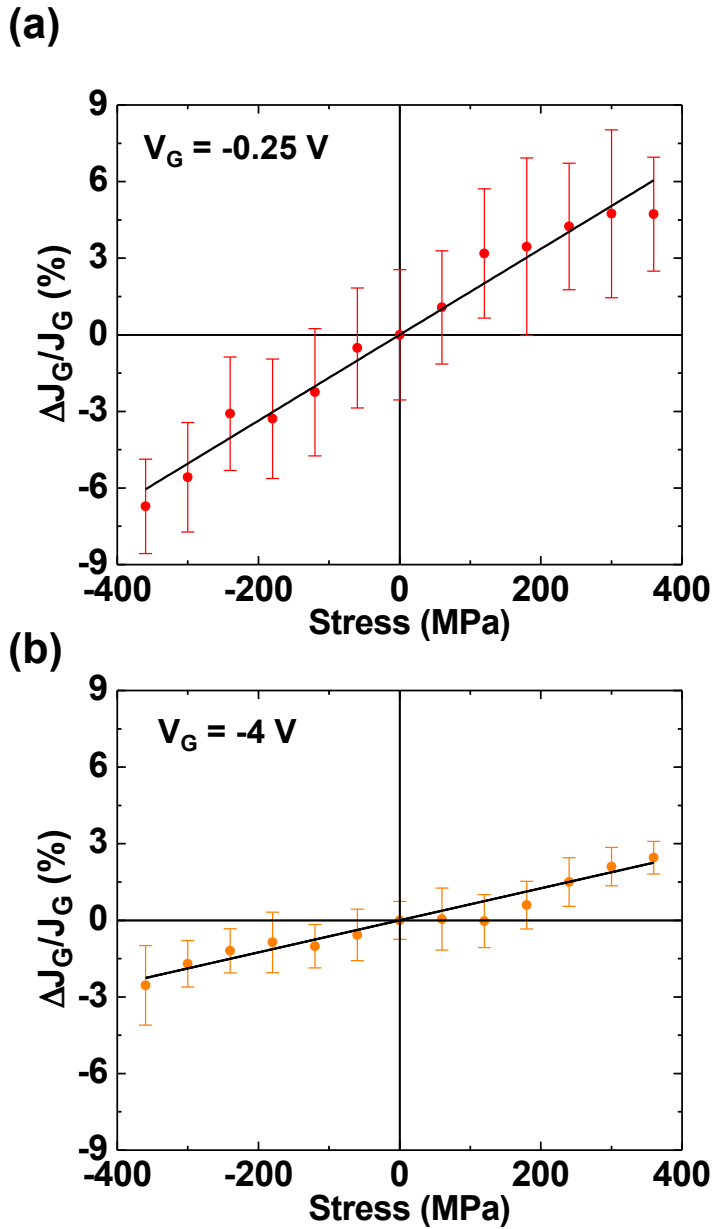


Figure 62. $\Delta J_G(\sigma)/J_G(0)$ averaged for all levels of compressive and tensile stress at (a) $V_G = -0.25 \text{ V}$ and (b) -4 V . Uncertainty comes from three standard deviation from the measurement of $\Delta J_G(\sigma)/J_G(0)$ over the duration stress was held constant.

The sensitivity of J_G to stress defined as the normalized change in J_G per stress, $[\Delta J_G(\sigma)/J_G(0)]/\sigma$, is calculated from the slope of the weighted total least squares linear fit of $\Delta J_G(\sigma)/J_G(0)$ versus stress, including uncertainty in J_G at each stress increment. The stress sensitivity of J_G is plotted as a function of reverse gate bias in Figure 63. Increasing the reverse gate bias is observed to decrease the sensitivity of J_G to stress. The sensitivity of J_G to stress decreased from $1.7 \pm 0.3 \text{ \%}/100\text{MPa}$ at $V_G = -0.25 \text{ V}$ to $0.6 \pm 0.1 \text{ \%}/100\text{MPa}$ at $V_G = -4 \text{ V}$ as

shown in Figure 63. To interpret the decreasing sensitivity for increasing reverse gate bias, the dominant gate leakage transport mechanism needs to be analyzed.

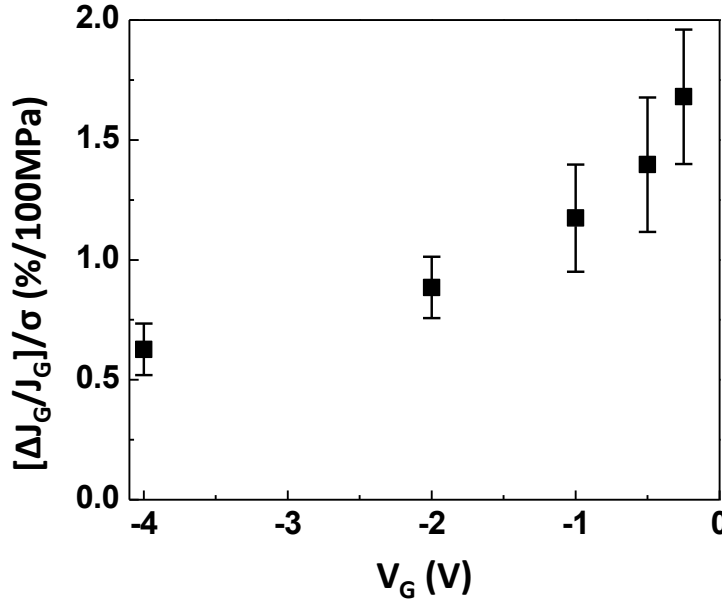


Figure 63. Experimentally measured stress sensitivity of J_G per 100 MPa of stress, as a function of reverse gate bias.

7.4.3 Determining the Vertical Electric Field under the Gate

The dominant leakage mechanism is strongly dependent on the materials and processing conditions and the electric field in the AlGa_N Barrier, E_{AlGaN} . To characterize the effect of mechanical stress on AlGa_N/Ga_N HEMT devices, an accurate model for the leakage mechanism is necessary. To compare different leakage models to the experimental measurements, an accurate calculation of E_{AlGaN} is needed. In past works, E_{AlGaN} has been simplified to a linear relationship with the gate voltage [Mitrofanov2004, Chikhaoui2009], simulated using Medici 2D simulations [Miller2000], and experimentally measured [Yan2010]. The $V_{DS} = 0$ state is of particular interest for exploring reliability since both the source and drain sides of the device gate are electrically stressed simultaneously.

1D electric field model

A one-dimensional (1D) calculation of E_{AlGaN} provides insight into the general relationship between voltage and field. In this condition, the gate is assumed to be infinitely wide. Also, for simplicity, E_{AlGaN} is assumed to be a constant throughout the entire thickness of the AlGa_N barrier. Based on these assumptions, a simple expression for the electric field in the AlGa_N barrier can be derived from the voltage drop across the AlGa_N barrier (V_{AlGaN}) from inspection of the energy band diagram (Figure 64). E_{AlGaN} can be written as,

$$E_{AlGaN} = \frac{V_{AlGaN}}{t_{AlGaN}} = \frac{\phi_b - (\Delta E_C - E_F)}{qt_{AlGaN}}$$

Recalling, n_s can be rewritten in terms of E_{AlGaN} ,

$$n_s = \frac{\sigma_{int}}{q} - \left(\frac{\epsilon_0 \epsilon_r}{q^2 t_{AlGaN}} \right) [\phi_b + E_F - \Delta E_C] = \frac{\sigma_{int} - \epsilon_0 \epsilon_r E_{AlGaN}}{q}$$

Then, the simple expression for E_{AlGaN} is

$$E_{AlGaN} = \frac{\sigma_{int} - qn_s}{\epsilon_0 \epsilon_r}$$

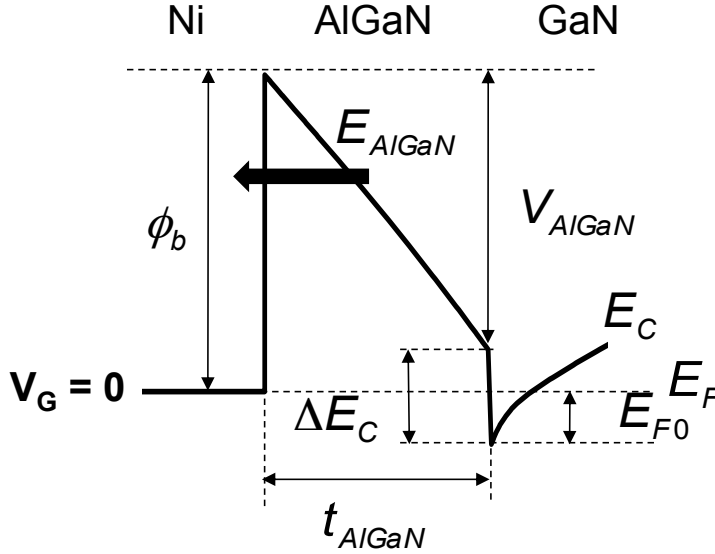


Figure 64. Energy band diagram schematic showing Ni/AlGaN/GaN interface.

In the expression for E_{AlGaN} , only the 2DEG sheet carrier density (n_s) is a function of gate voltage. The total fixed charge density at the AlGaN/GaN interface (σ_{int}) is assumed to be independent of bias because it is based on the polarization. Charge trapped at the AlGaN/GaN interface is estimated to be constant with bias. To analyze the dependence of n_s with gate voltage, n_s is rewritten to include the contribution of V_G in terms of the equilibrium 2DEG concentration n_{s0} .

$$n_s = \frac{\sigma_{int}}{q} - \left(\frac{\epsilon_0 \epsilon_r}{q^2 t_{AlGaN}} \right) [q\phi_b + E_{F0} - \Delta E_C + qV_G] = n_{s0} + \left(\frac{C_{AlGaN}}{q} \right) V_G$$

where, $C_{AlGaN} = \frac{\epsilon_0 \epsilon_r}{t_{AlGaN}} C_{AlGaN} = \frac{\epsilon_0 \epsilon_r}{t_{AlGaN}}$ is the AlGaN capacitance per unit area. At equilibrium,

$V_G = 0$ V and $n_s = n_{s0}$, which is the maximum induced 2DEG sheet carrier density. The fixed positive charge at the AlGaN/GaN interface induces accumulation of electrons at the interface in the GaN. The electrons that form the 2DEG originate from the AlGaN surface [Ibbetson2000], not from the source, drain, and substrate as in a Si MOSFET inversion layer. A negative bias applied to the gate depletes the 2DEG, decreasing n_s linearly. The threshold voltage for the depletion mode AlGaN/GaN HEMT is defined as the voltage required on the gate to entirely deplete the 2DEG ($n_s = 0$). Since the AlGaN/GaN HEMT is a depletion mode device with a negative V_T , the device is considered to be turned off below threshold ($|V_G| > |V_T|$). Above

threshold, the 2DEG is formed ($|V_G| < |V_T|$). Below threshold, the 2DEG remains depleted. Since the intrinsic carrier concentration of GaN is extremely low ($n_i \sim 1 \times 10^{-10} \text{ cm}^{-3}$ at 300 K), hole accumulation at the surface is negligible. The fixed charge density at the AlGaN/GaN interface ($\sigma_{int} = 2.2 \times 10^{-6} \text{ C/cm}^2$) is a result of the polarization differences between AlGaN and GaN.

To express E_{AlGaN} as a function of gate voltage, the voltage dependent 2DEG equation was incorporated into the expression for E_{AlGaN} to give,

$$E_{AlGaN}(V_G) = \frac{-\left(\frac{\epsilon_0 \epsilon_r}{qt_{AlGaN}}\right) [q\phi_b + E_{F0} - \Delta E_C + qV_G]}{\epsilon_0 \epsilon_r} \text{ for } V_G > V_T$$

For gate bias below threshold, E_{AlGaN} saturates at

$$E_{AlGaN} = -\sigma_{int} / (\epsilon_0 \epsilon_r) \quad E_{AlGaN} = -\sigma_{int} / (\epsilon_0 \epsilon_r). \text{ Estimation of } E_{AlGaN} \text{ for an actual AlGaN/GaN}$$

HEMT device based on the 1D model requires both σ_{int} and n_s to be experimentally measured. The threshold voltage determined by the standard linear extrapolation method ($V_T = -4 \text{ V}$) is not consistent with the definition of $V_G = V_T$ when $n_s = 0$. A more accurate threshold of -1.9 V is obtained based on the initial increase of the capacitance-voltage curve (Figure 65). From the definition of threshold ($V_G = V_T$ when $n_s = 0$), the 2DEG sheet carrier density at $V_G = 0$ can be calculated from the measured V_T

$$n_{s0} = \frac{-C_{AlGaN} V_T}{q}$$

which gives $n_{s0} = 5.3 \times 10^{12} \text{ cm}^{-3}$ for $V_T = -1.9 \text{ V}$. Then, the fixed charge at the AlGaN/GaN interface can be estimated by solving for σ_{int} in :

$$n_{s0} = \frac{\sigma_{int}}{q} - \left(\frac{\epsilon_0 \epsilon_r}{q^2 t_{AlGaN}}\right) [\phi_b + E_{F0} - \Delta E_C]$$

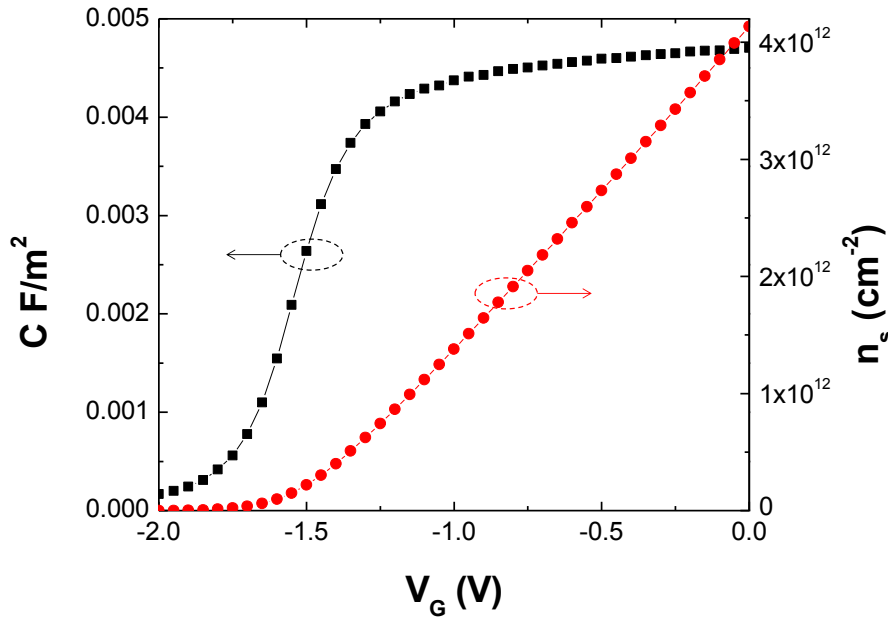


Figure 65. Capacitance-Voltage measurement, which is integrated in order to determine $n_s(V)$.

which results in $\sigma_{int} = 1.25 \times 10^{-6} \text{ C/cm}^2$ that is nearly half the ideal value ($\sigma_{int} = 2.2 \times 10^{-6} \text{ C/cm}^2$). The interface trapped charge density is estimated from the subthreshold slope (SS) measurements [Chung2007, Chung2008],

$$SS \approx \frac{kT}{q} \ln 10 \left[1 + \frac{C_{it}}{C_{AlGaN}} \right]$$

The capacitance associated with the interface trapped charge (C_{it}) can be related to the density of interface traps by $C_{it} = qD_{it}$. For the measured device with $SS = 100 \text{ mV/dec}$, the interface trap density corresponds to $D_{it} = 1.92 \times 10^{12} \text{ cm}^{-2}\text{eV}^{-1}$. Assuming all traps are full, integrating over the bandgap of AlGaN gives an interface trapped charge of $Q_{it} = 1.2 \times 10^{-6} \text{ C/cm}^2$. Figure 66 shows a bar chart of the charge density in the ideal device compared to the actual device. In the ideal device ($Q_{it} = 0$) and $\sigma_{pz} = \sigma_{int}$. However, in the actual device, the fixed charge at the AlGaN/GaN interface induced by polarization is reduced by negative trapped charge.

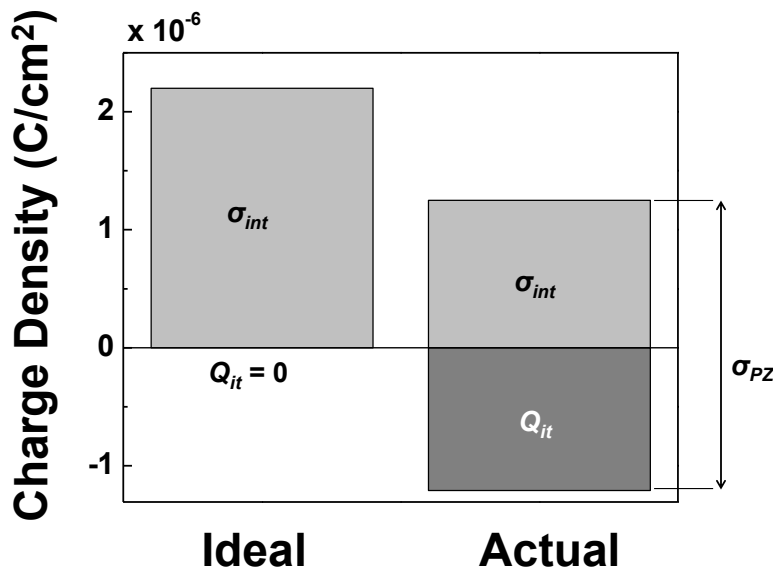


Figure 66. Bar diagram of the AlGaN/GaN interface charge for an ideal device with no trapped charge and an actual device. Trapped charge reduces the positive fixed sheet charge density at the AlGaN/GaN interface.

To obtain E_{AlGaN} for the actual device, the n_s versus V_G relationship needs to be obtained. A high-frequency (1 MHz) capacitance-voltage curve (Figure 65) was integrated from pinch-off to voltage V_G . The experimental bias range was limited to $V_G = -2 \text{ V}$ to 0 V to avoid additional charge trapping from larger applied biases. The value of $n_s(V_G)$ is also shown in Figure 65. The experimentally obtained n_s versus V_G relationship is used in Equation TN-8 to calculate the experimentally obtained E_{AlGaN} versus V_G relationship.

Implementing the experimentally determined σ_{int} and n_s versus V_G relationship provides the experimentally determined 1D calculation of E_{AlGaN} versus V_G . Figure 67 shows a comparison between the experimental and ideal 1D calculation for E_{AlGaN} versus V_G . Since both methods are based on the 1D expression, they have similar trends. Above threshold, $|E_{AlGaN}|$ increases

linearly with increasing reverse bias, and below threshold E_{AlGaN} saturates at

$$E_{AlGaN} = -\sigma_{int} / (\epsilon_0 \epsilon_r) E_{AlGaN} = -\sigma_{int} / (\epsilon_0 \epsilon_r). \text{ The presence of } Q_{it} \text{ reduces } \sigma_{int} \text{ and the}$$

magnitude of the saturated value of E_{AlGaN} below threshold in the actual device compared to the ideal 1D calculation. In addition, V_T is shifted toward the positive direction by the negative Q_{it} . At $V_G = 0$, the experimental $|E_{AlGaN}|$ is larger than the ideal 1D case because the experimentally extracted n_{s0} is lower than what is theoretically predicted, making the numerator of Equation TN-8 larger.

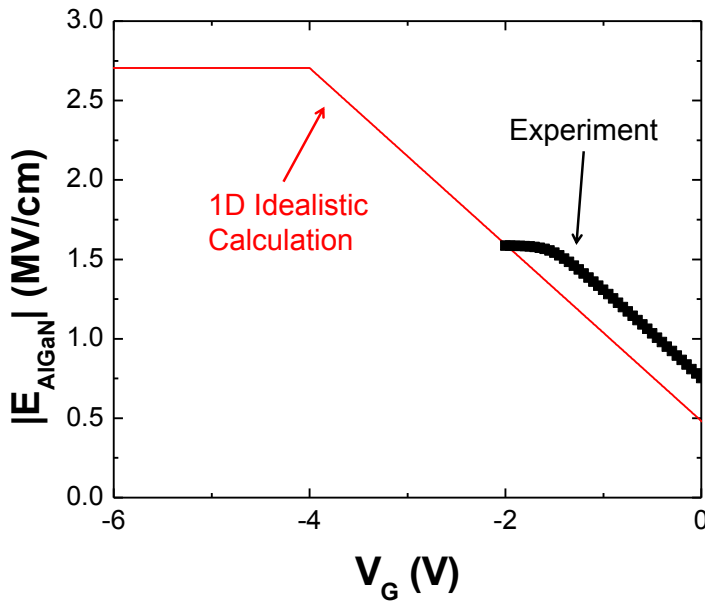


Figure 67. 1D ideal (no interface trapped charge) calculation and the experimental result from experimental parameters obtained by adjusting σ_{int} and obtaining n_s from C-V.

2D TCAD simulation

The AlGaN/GaN HEMT structure was simulated using the Sentaurus device simulator. A two-dimensional (2D) simulation was performed to gain a physical understanding of 2D effects on E_{AlGaN} . The thin (~ 1.5 nm) GaN cap layer was neglected in the simulation for simplicity. The device structure is quantized into a mesh or grid of discrete elements. A rectangular gate is assumed for simplicity. The grid was condensed in areas where large variations of carrier concentration are expected at short distances to optimize computational accuracy (Figure 68).

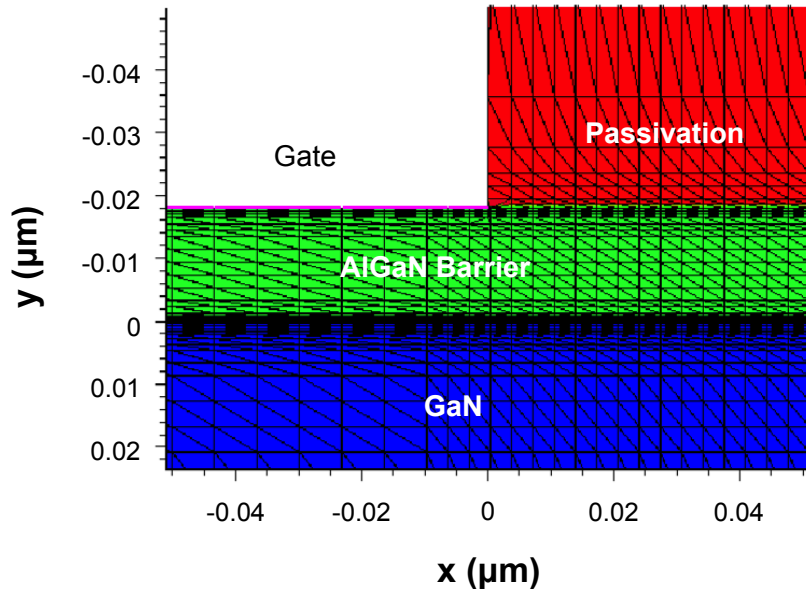


Figure 68. Optimized grid for Sentaurus simulation of the AlGaIn/GaN HEMT device.

At each point on the grid, three variables are solved for simultaneously. The electrostatic potential, electron concentration, and hole concentration are solved for through Poisson's equation and the electron and hole continuity equations respectively. The boundary conditions used to solve for the three variables are: the metal-contact work function difference, the ohmic contacts at the source and drain, and local conservation of charge. In the actual device, the high resistivity Si layer isolates the GaN layer from the back side of the wafer, leaving it electrically floating. The bulk is left floating in simulation to model this. Shockley-Read-Hall recombination and generation were included in the calculation. Also, a hydrodynamic model was used where the carrier temperature is not assumed to be equal to the lattice temperature. Electron mobility was modeled including doping dependence, high field saturation, and temperature. Doping was introduced under the source and drain contacts to emulate metal spikes to provide an ohmic contact to the 2DEG [Kolaklieva2009]. The piezoelectric effect is modeled by incorporating a fixed charge at the AlGaIn/GaN interface equal to σ_{int} and at the AlGaIn surface equal to σ_{PZ} to match experiment.

The simulated dependence of E_{AlGaIn} versus V_G at the center of the gate is compared to the 1D model with experimentally determined parameters (Figure 69). In the simulation, σ_{int} was matched to the experimentally obtained value of $1.25 \times 10^{-6} \text{ C/cm}^2$. The trend of the 2D simulated E_{AlGaIn} is similar to the 1D calculation. Above threshold, $|E_{AlGaIn}|$ increases until threshold with decreasing reverse gate bias. Below threshold, $|E_{AlGaIn}|$ tends to saturate. Although σ_{int} is matched, the saturation value of E_{AlGaIn} in the 2D simulation at the center of the gate is slightly lower than the experimentally determined curve. Since the simulated device has a finite gate width (1 μm), it is important to analyze the edges of the gate for a comprehensive understanding of the E_{AlGaIn} versus V_G relationship.

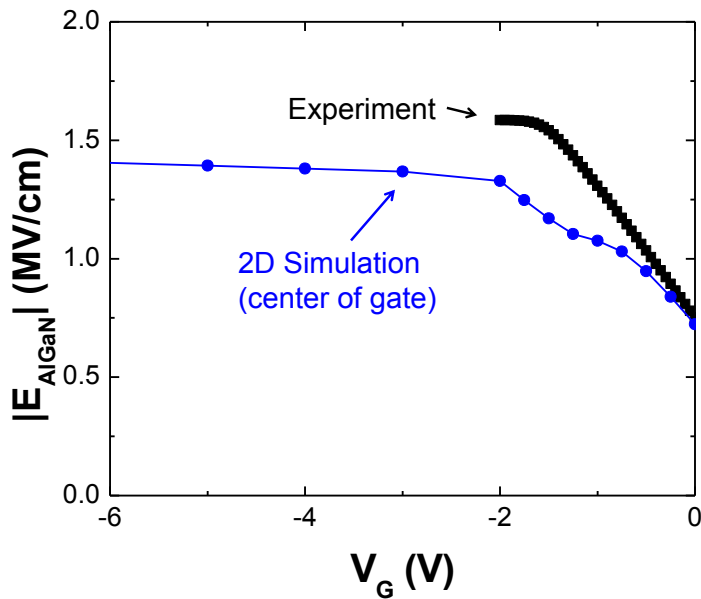


Figure 69. Experimental calculation of E_{AlGaN} versus V_G compared to 2D simulation results.

7.4.4 Gate Leakage Mechanisms

Several GaN HEMT gate leakage mechanisms have been proposed in the literature, such as the Direct Tunneling [Zhang2006], Poole-Frenkel Emission (PFE) [Mitrofanov2004, Yan2010], bulk defect-assisted tunneling [Karmalkar2003, Sathaiya2006], and defect band induced leakage [Yan2010]. Despite many models, the dominant leakage mechanism depends on temperature, gate bias, and device quality. Figure 70 schematically illustrates these leakage processes.

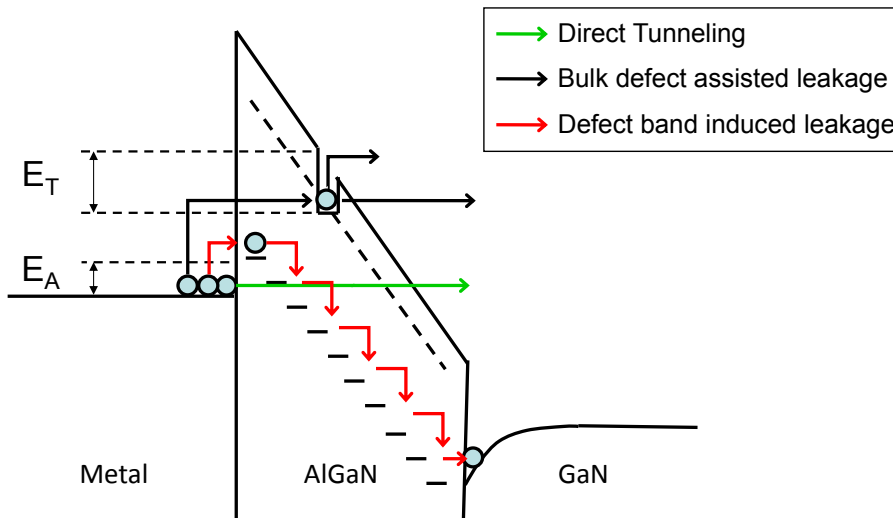


Figure 70. Schematic illustrations of the gate leakage processes in a reverse biased GaN HEMT.

Direct tunneling

Due to the large electric field across the AlGa_N barrier, the direct tunneling in GaN HEMT mainly includes the Fowler-Nordheim tunneling (FN) and Thermionic Field Emission (TFE). Both the FN and TFE models are well established in literature and can be expressed analytically below for the FN tunneling [Jensen2003].

$$J = \frac{q^2 (m_e / m^*)}{8\pi h \phi_B} E^2 \exp\left(-\frac{8\pi\sqrt{2m^*} (q\phi_B)^3}{3qhE}\right)$$

and these for the TFE [Fleisher1992], respectively

$$J = \frac{qA^*T}{k} \int_0^{\phi_B} f_{FD}(\phi) P(\phi) d\phi$$

$$f_{FD} = \frac{1}{1 + \exp\left(\frac{\phi_B - \phi}{kT/q}\right)}$$

$$P = \exp\left(-\frac{8\pi\sqrt{2m^*}q}{3hE} \phi^{3/2}\right)$$

Here, q , m_e , h , k , and A^* are the electron charge, the free electron mass, the Planck constant, the Boltzmann constant, and the effective Richardson constant, respectively. E is the electric field strength in the AlGa_N layer. m^* is the out-of-plane effective mass of electrons inside AlGa_N. f_{FD} is the Fermi-Dirac distribution function of electrons on the metal side. ϕ_B is the Schottky barrier height between the metal gate and the AlGa_N, obtained from the equation below considering the barrier lowering due to image force and band gap narrowing [Karmalkar2003]. The values of ϕ_{B0} , γ_1 , and γ_T are 1.4eV, 0.4, and 2.4×10^{-4} V/k for AlGa_N [Karmalkar2003].

$$\phi_B = \phi_{B0} - \gamma_1 \sqrt{\frac{q}{4\pi\epsilon}} \sqrt{E} - \gamma_T T$$

Figure 71 shows the simulated direct tunneling current and the experimental measured gate current at room temperature. The result shows that the direct tunneling currents are several orders smaller than the experimental observation until at least 2.5MV/cm. This is expected since the AlGa_N layer (18nm) is too thick for the electrons to have a high tunneling rate. In addition, the Schottky barrier height (~1.4eV) is unlikely to result in a high thermal emission rate at room temperature.

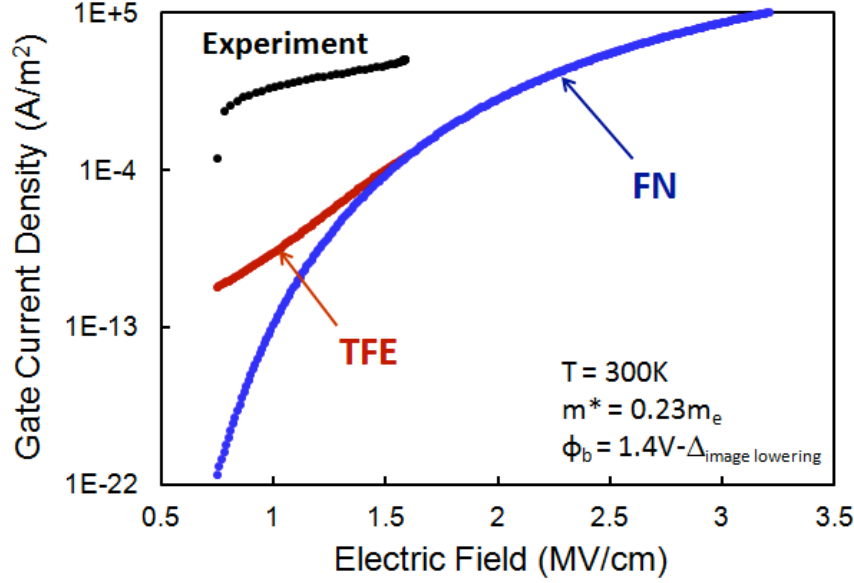


Figure 71. Simulation results of the FN tunneling current and the TFE current at room temperature.

As a result, direct tunneling is not the dominant leakage mechanism in these devices when biased above the threshold ($V_G > -1.9V$). At below threshold, there can be a direct tunneling path at the edge of the gate once the edge electric field is high enough.

Bulk trap-assisted leakage

To consider the possibility of GaN HEMT gate leakage following the bulk trap-assisted leakage mechanism, this work adopts Fleischer's two-step leakage model [Fleisher1992] and develops it to incorporate the thermal contribution in step 2. In the first step of our model, the electrons tunnel from the metal gate to the trap level through direct tunneling or thermal-assisted direct tunneling. In step 2, electrons escape from the trap into bulk GaN through direct tunneling, Poole-Frenkel emission [Frenkel1938], or Phonon-assisted tunneling [Pipyns2006, Ohlckers2008]. The complete leakage process is shown schematically in Figure 70. The tunneling (emission) rates of step 1 and 2 are calculated from :

$$R_1 = C_t N_t f_{FD} (1 - f) P_1$$

$$R_2 = C_t N_t f P_2$$

Here, N_t is the bulk defect density, f is the probability that the defect level is filled with an electron, P_1 and P_2 are the tunneling (emission) probability, and C_t is given by

$$C_t = \left(\frac{m^*}{m_e} \right)^{5/2} \left(\frac{8E_1^{3/2}}{3h\sqrt{E_T - E_1}} \right)$$

where E_T is the defect level referring to the conduction band edge, and E_1 is the total energy of an electron (0.2eV [Fleisher1992]). P_1 is calculated following the standard direct tunneling expression

$$J = \frac{q^2 (m_e / m^*)}{8\pi h \phi_B} E^2 \exp \left(- \frac{8\pi \sqrt{2m^*} q}{3hE} (\phi_B^{3/2} - \phi^{3/2}) \right)$$

and P_2 is calculated using either the FN tunneling model, the classical Poole-Frenkel emission model, or the phonon-assisted tunneling model developed by Pipinys et al.[Pipinys2006]. At steady state, R_1 should equal R_2 . After a straight forward mathematical derivation, the tunneling rate R is obtained,

$$R = N_t \cdot \left(\frac{1}{C_i f_{FD} P_1} + \frac{1}{C_i P_2} \right)^{-1}$$

The overall gate current density is then calculated by integrating R over the thickness of the entire AlGaIn barrier.

$$J = \frac{q}{E} \int_{\phi_i}^{E \cdot d} R(\phi) d\phi$$

In the current model, a uniform defect distribution is assumed across the AlGaIn barrier. The AlGaIn potential profile is assumed to be triangular, which is reasonable for devices biased above threshold. We also considered only one single effective defect level as a fitting parameter. Figure 72 shows the calculated and experimental gate current density at room temperature, with $N_t=5 \times 10^{17} / \text{cm}^3$ and $E_T=0.82\text{eV}$. The value of E_T significantly affects the resulting current magnitude. In fact, E_T has opposite effects on P_1 and P_2 . With small E_T , the energy difference between the metal gate Fermi level and the defect level is large, and the first step of electrons tunneling from the metal gate into the defect level is unlikely to happen. With large E_T , the energy difference between the defect level and the AlGaIn conduction band is large, and the step two probability of electrons undergoing PFE or PAT becomes smaller. The value of $E_T=0.82\text{eV}$ was estimated by trying to fit the two step model and the experimental results within the same order of magnitude, under a reasonable defect density $N_t=5 \times 10^{17} / \text{cm}^3$. Under this condition, it is found that the calculated current density does not depend on the chosen mechanism for the P_2 step. This indicates that the first step of electrons tunneling from the metal gate into the defect level limits the bulk trap-assisted leakage current.

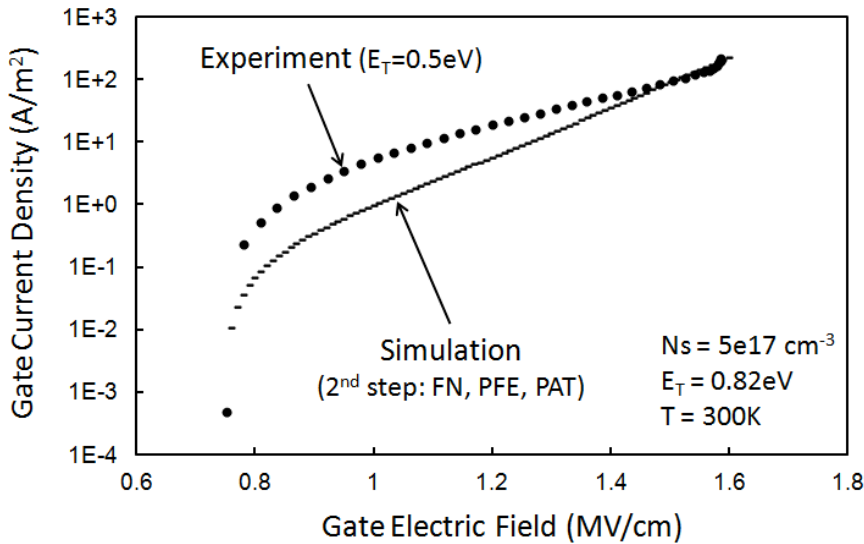


Figure 72. Simulation result of the 2-step bulk trap-assisted leakage current at room temperature.

Regardless of what leakage mechanism for step two and fitting parameters are chosen, a good match between the model and experimental results is unachievable. This suggests that the

bulk trap-assisted tunneling mechanism may not be the dominant leakage mechanism in these GaN HEMT devices.

Defect Band Induced Gate Leakage

It has been proposed in literature that defects with a large dispersion in energy exist throughout the AlGa_N barrier layer [Arehart2009, Sghaier2004, Okino2004, Wolter2003, Bradley2001, Tartarin2007]. These defects can form a conductive path which has an effective energy E_A above the metal gate Fermi level, as shown in Figure 70. At room temperature or at elevated temperature, some electrons from the metal gate may gain sufficient thermal energy to overcome the barrier between the metal gate and the defect band, and emit into the defect band states. Once the electrons reach the defect band, they may undergo trap-to-trap transitions toward the GaN substrate by high vertical electric field-induced elastic and inelastic trap-to-trap tunneling due to the high density of traps.

The accurate modeling of the defect band induced gate leakage is complex. It highly depends on the defect distribution in both energy and real space. Qualitatively speaking, we expect this leakage current to increase with increasing vertical electric field, larger defect density, lower gate-to-defect barrier height (E_A), higher temperature, and smaller electron out-of-plane effective mass. This mechanism may explain our experimental results since the energy barrier is reduced compared to the bulk trap-assisted, Poole-Frenkel, and direct tunneling leakage mechanisms. The details of model development for the defect band induced gate leakage require further investigation.

x.4.5 Stress-Dependent Parameters

This section qualitatively discusses the effects of external mechanical stress on the GaN HEMT gate leakage, by considering the stress-altered electron out-of-plane effective mass, the AlGa_N electric field, and the defect energy level.

We used the sp^3d^5 - sp^3 tight-binding model to calculate the change of electron out-of-plane effective mass under both uniaxial and biaxial stress. In the experiment, the uniaxial stress is induced by wafer bending, and the biaxial stress is induced by the inverse piezoelectric effect when gate bias is present. Figure 73 shows the tight-binding calculation results for both uniaxial and biaxial stress. It is observed that the electron out-of-plane effective mass has negligible change under both stresses (<0.5% per 400MPa).

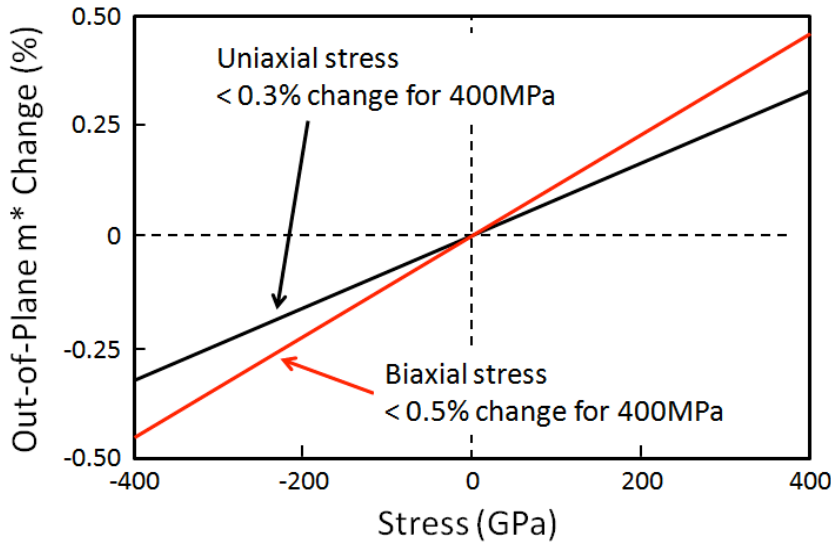


Figure 73. Change of the electron out-of-plane effective mass under uniaxial and biaxial stress.

Stress causes variation in the AlGa_N polarization due to the piezoelectric effect, leading to a change in the electric field strength. As mentioned before, this additional piezoelectric polarization can be calculated by $P^{PE, mech} = e_{ij} \cdot \varepsilon$, where e_{ij} is the piezoelectric constants, and ε is the strain. Approximately 0.7% and 1.4% change in polarization is predicted for 400MPa uniaxial and biaxial stress, respectively. This observation indicates a weak stress dependence of the AlGa_N electric field.

Stress has been proposed to shift the defect energy level by changing the atom-defect bond angle and bond length [Choi2008]. It was observed that both tensile and compressive stresses decreases Pb₁ (or Pb₂) defect levels for Si MOSFETs, resulting in an increase of gate leakage current [Choi2008]. For GaN HEMTs, our experimental results in Figure 61 show that tensile stress increases gate current, while compressive stress decreases gate current. This can be explained qualitatively with Figure 74, taking the N-vacancy as an example. As mentioned before, approximately 2.8GPa biaxial stress is present in the AlGa_N layer due to lattice mismatch. Compared to the unstrained lattice, the bond angle θ_1 decreases and θ_2 increases, and the bond length L_1 decreases and L_2 increases. The defect in the AlGa_N becomes less stable under this large stress, and its energy level shifts up towards the conduction band. When a tensile wafer bending stress is applied, a similar trend of bond angle and bond length variation is expected. It adds to the effect of biaxial stress and shifts the defect level further up. In contrast, a compressive wafer bending stress tends to relax the strain from the lattice mismatch, therefore results in a downward shift of the defect level towards its original state. Since the gate current exponentially depends on the defect level, a decrease (or increase) of the defect level from tensile (or compressive) stress increases (or decreases) the gate current.

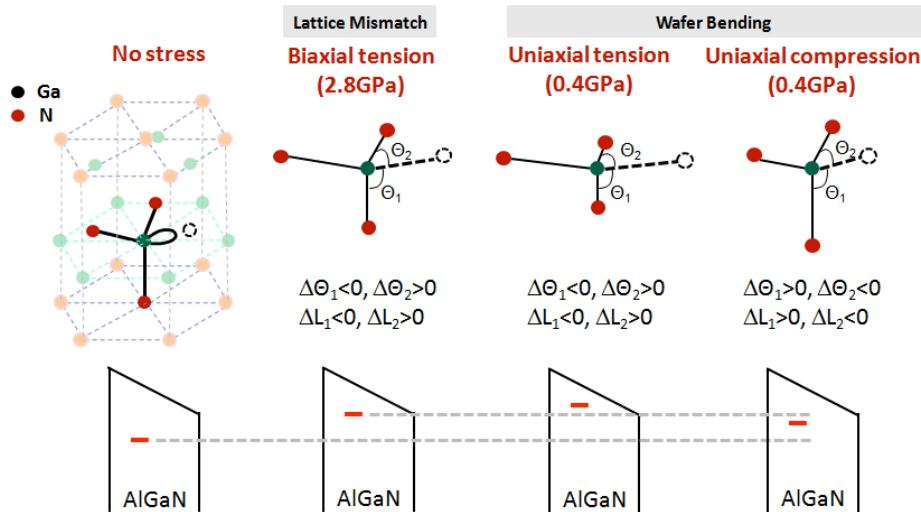


Figure 74. Schematic illustrations of the defect bond angle and bond length variation, and the defect level shift under lattice mismatch and wafer bending stress.

The overall effect of mechanical stress on the GaN HEMT gate leakage is a combination of the above discussed factors. The shift of the defect activation energy (or defect band energy) is expected to dominate the leakage variation, due to the negligible change of electric field and effective mass, as well as the exponential dependence of gate leakage on the defect level. A rigorous modeling of the stress-altered defect level is needed.

7.5 Time-dependent electrical degradation of AlGaN/GaN HEMT

7.5.1 Electrical step stress with varying time-step

The onset of electrical degradation in AlGaN/GaN HEMTs has been studied by conducting an electrical step stress experiment [Joh2008, Chini2009, Lo2011]; where the electrical bias is stepped incrementally while simultaneously monitoring an electrical parameter. The voltage at which the device undergoes a sudden increase in the degradation of the electrical parameter is termed the critical voltage (V_{crit}). However, it has not been proven that the so-called critical voltage is actually a threshold, independent of the duration of the voltage step. A modified electrical step stress experiment is conducted in this work where a set of degradation tests are performed with varying time-steps (or length of time for which each voltage step is applied) and the ‘critical voltage’ is determined for each test. The main objective is to investigate the effect of varying the time-steps on the ‘critical voltage’ at which device degradation occurs. If the so-called critical voltage varies as a function of the time-step, then the picture of degradation cannot be as simple as a single critical voltage. Understanding the time dependence may provide insight into the complex degradation mechanism that determine the reliability of AlGaN/GaN HEMTs.

7.5.2 Experimental Procedure

A 150 μm wide, 2-finger Al_{0.28}Ga_{0.72}N/GaN HEMT grown on SiC substrate, with gate length $L_G=1\mu\text{m}$, Ni/Au gate and SiN_x passivation is used for this experiment. Electrical step stress is performed by stepping the reverse gate bias in steps of -1V/step, beginning with $V_{GS}=-$

10V at $V_{DS}=0V$ and at room temperature. The length of time for each voltage step is varied as $t=10\text{sec}$, 100sec , 500sec and 1000sec for four different tests performed separately on four identical devices for comparison. Devices are assumed to be identical if they demonstrate similar electrical characteristics before the electrical stress, such as saturation drain current, threshold voltage, and gate leakage current. The gate current I_G is simultaneously monitored while the voltage step stress is applied using a Keithley 4200 semiconductor characterization system with the I_G compliance set at $100\ \mu\text{A}$ to prevent internal heating of the device. A user-defined module is coded, compatible to run with Keithley's KITE platform, to apply any desired voltage step stress.

7.5.3 Results and Discussion

All four step-stress tests depict I_G trapping transients at each voltage step prior to breakdown. When a critical voltage is reached, a sudden increase in I_G is observed indicating onset of irreversible degradation. This is followed by multiple smaller jumps in I_G . I_G continues to increase beyond the 'critical voltage' until it hits the set current compliance limit. This indicates that once initiated, device degradation continues to proceed until compliance is reached which is preset on the Keithley 4200 to protect the instrument. Figure 75 depicts I_G degradation due to electrical step stress with $100\text{sec}/\text{step}$ time-step.

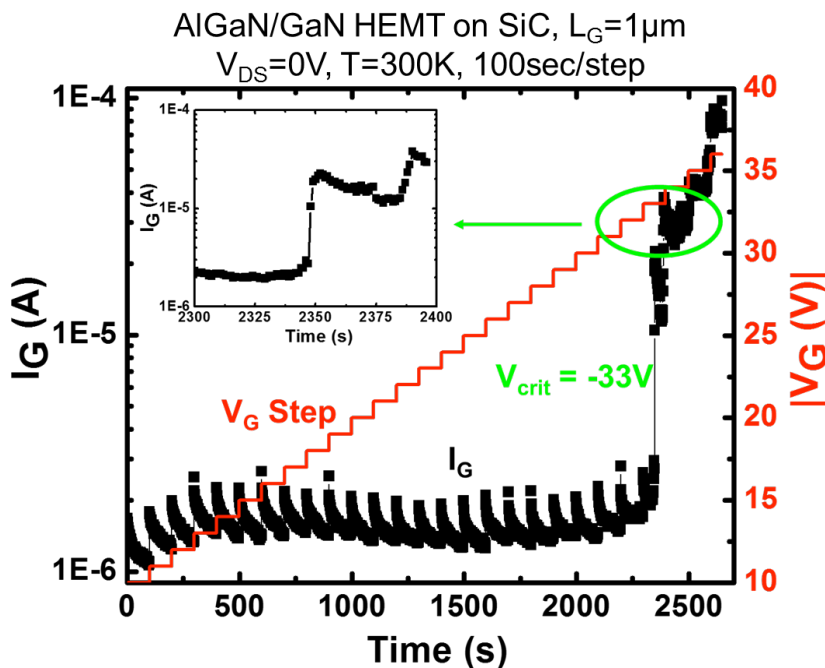


Figure 75. I_G degradation of AlGaIn/GaN HEMT at $V_{DS}=0V$ during electrical step stress test with $100\text{sec}/\text{step}$ time-step. Inset shows I_G progression during “critical voltage” step, indicating time dependent degradation of I_G .

It is observed that the critical voltage at which I_G begins to degrade depends on the time-step (or length of time for each applied voltage step) and it decreases with increase in time-steps as shown in Figure 76. Devices that are electrically step stressed with longer time-steps begin to degrade sooner (at smaller critical voltage) than the devices that are step stressed with smaller time steps. Figure 77 shows a plot indicating linear dependence between critical voltage or

breakdown voltage (from each electrical-step stress test) versus square root of corresponding time-step. This implies that a diffusion phenomenon may be playing a role in determining the critical voltage for a device because Fick's mathematical model for diffusion exhibits a $\sqrt{\text{time}}$ dependence. Since a thin oxide layer has been observed at the gate-metal/semiconductor Schottky interface, it can be hypothesized that this oxide layer undergoes a diffusion due to excessive strain under the gate from the high electrical field (from the applied voltage step) or due to the presence of threading dislocations that potentially act as hot spots. A longer time-step (at each voltage step) allows more time for slow diffusion of the oxide layer at each voltage step, until the oxide layer weakens, loses its integrity and ruptures potentially around the threading dislocations. This is observed as a sharp increase in I_G and marked by a critical voltage. Hence, the electrical step stress test with longer time-step gives a smaller critical voltage for the device.

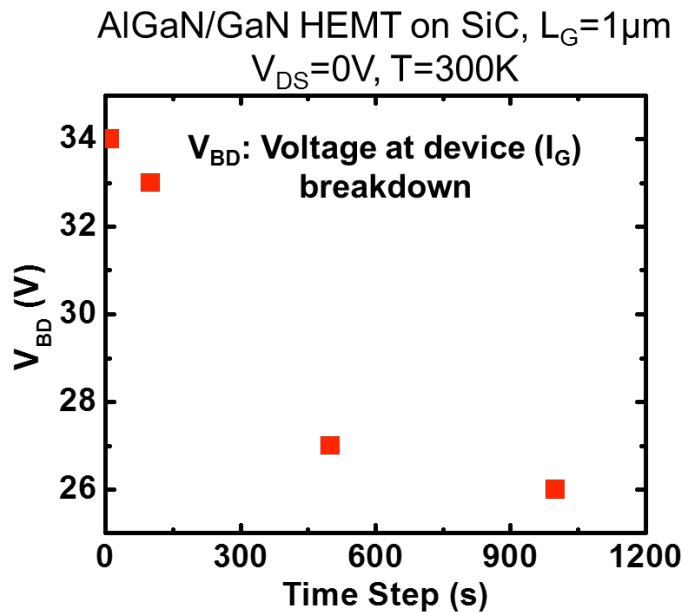


Figure 76. Dependence of “critical voltage” (voltage at onset of I_G breakdown) on time-step (length of time for each applied voltage step) in electrical step stress test.

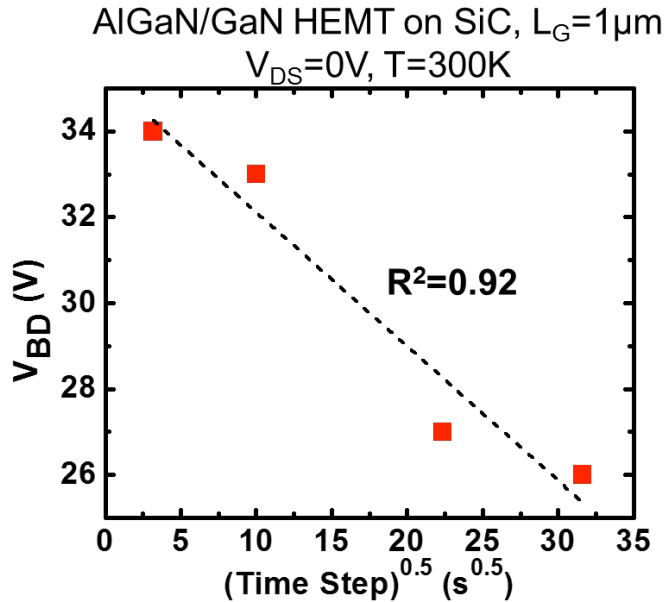


Figure 77. Linear dependence between “critical voltage” and time-step indicates potential role of diffusion phenomenon in determining critical voltage.

The inset of Figure 75 shows the time evolution of I_G during the ‘critical voltage’ step for electrical step stress test with 100 sec/step time-step. It is observed that the gate current undergoes significant enhancement not immediately but after some elapsed time of the application of the critical voltage indicating that degradation in AlGaN/GaN HEMTS is time dependent. The diffusion of the oxide layer is potentially a time- and stress-dependent phenomenon.

A potential metal diffusion of gate metal into the AlGaN epilayer (initiated by the oxide layer rupture followed by its diffusion into AlGaN epilayer) can alter the barrier width, thus increasing the gate current and resulting in permanent device degradation. Assuming a limited source diffusion model, the gate current will mainly be concentrated at localized areas of metal diffusion. The gate current measured during device degradation is compared with a metal-semiconductor tunneling model where the transmission coefficient for electrons tunneling from metal into semiconductor depends on the tunneling barrier width in Figures x-29 and x-30. The qualitative agreement between measured and simulated gate current using a diffusion-modulated tunneling barrier metal-semiconductor tunneling model suggests that barrier width reduction possibly due to oxygen diffusion followed by metal diffusion is a potential failure mechanism causing device degradation in AlGaN/GaN HEMTs.

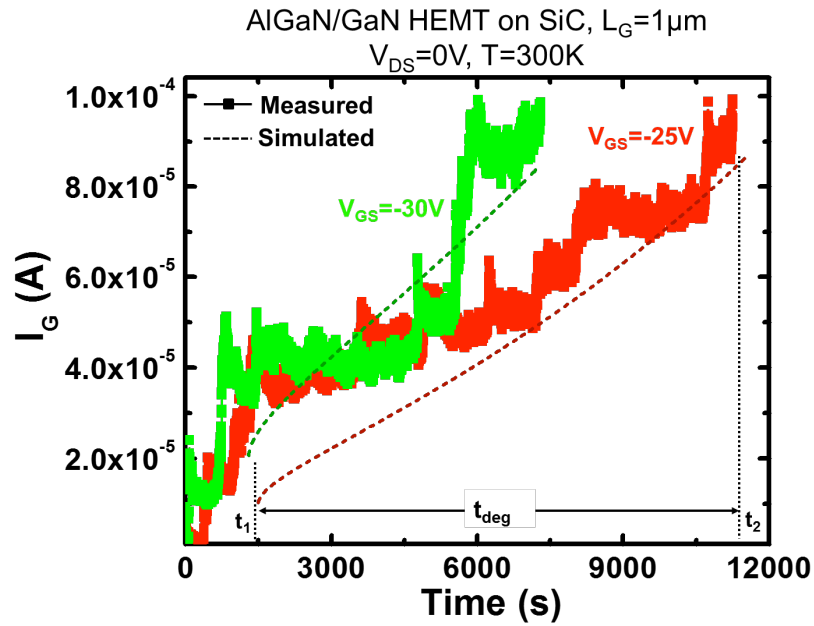


Figure 78. Simulated and measured I_G indicating time dependent degradation in AlGaIn/GaN HEMT at varying reverse gate biases.

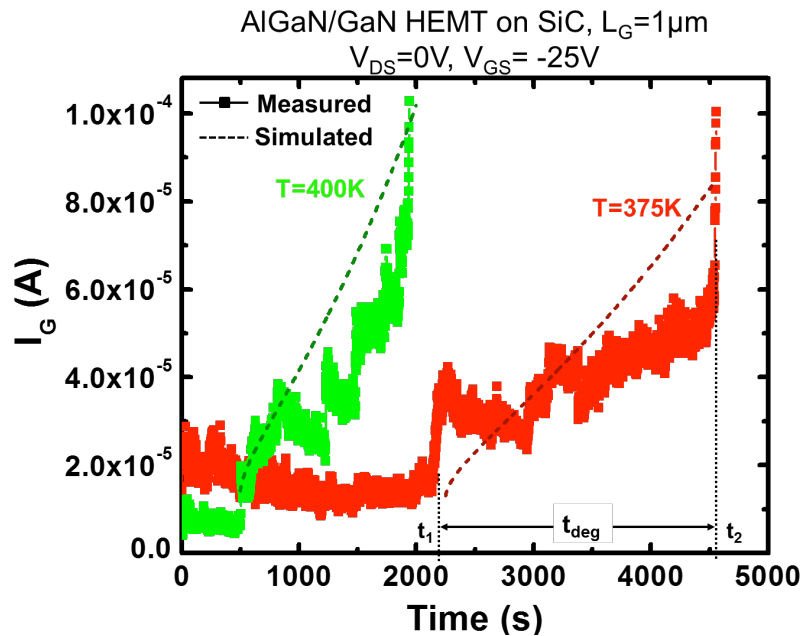


Figure 79. Simulated and measured I_G indicating time dependent degradation in AlGaIn/GaN HEMT at varying temperatures.

7.6 Optical characterization of AlGaIn/GaN HEMT traps

7.6.1 Experimental Setup

To investigate the trap generation behavior in AlGaIn/GaN heterostructures, the experimental setup shown in Figure 80 is designed to implement trap generation and characterization, via electrical stressing and photoionization spectroscopy techniques

respectively. For the characterization of the traps, a continuous wavelength sweep monochromator is used. This ensures that a sufficient resolution in trap energy distribution can be achieved. The continuous wavelength sweep capability is realized by using the 300W arc lamp coupled with a computer controlled MS257 Oriel spectrometer. The beam at the monochromator aperture is collimated and focused using two optical neutral density lenses, while it is shone directly on the GaN sample in the stress jig using a metal mirror. The size of the beam spot on the sample is as small as approximately 3mm by 1mm, which in return increases the photon flux density incident to the DUT. By avoiding an optical fiber light guide, intensity loss is minimized. During PS experiments, a Keithley 4200 system is used in the sampling mode to measure the linear drain current as a function of time. The measurement speed, filtering and delay settings are optimized to achieve a desirable tradeoff between signal to noise ratio and sampling rate to capture fast trapping-detrapping behaviors. The drain voltage is set to a value within the linear operation regime of the device during PS measurements to ensure that the current forced through the device does not cause further degradation or additional trap generation.

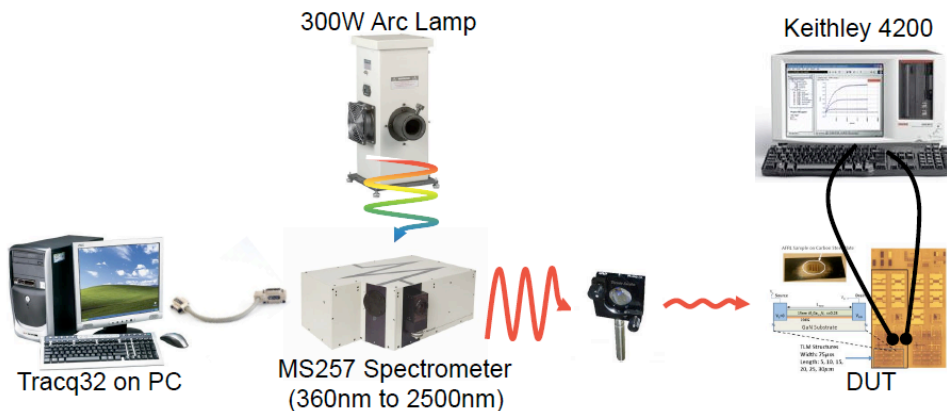


Figure 80. Photoionization spectroscopy setup for optical characterization of AlGaIn/GaN HEMT traps.

During the wavelength sweep, a UV-VIS band grating with 1200 lines/mm and a blazing wavelength of 350nm is used to decompose the wavelengths of the radiation from the arc lamp. In order to avoid additional electron-hole pair photogeneration, subbandgap illumination is performed, setting the shortest photon wavelength to 365-360nm range. To determine the value of the longest incident photon wavelength, the effects of higher-order stray light is taken into consideration. For a given incident angle of arc lamp radiation to a grating set to wavelength λ , the higher-order photons with wavelengths of λ/n leak from the grating at a reduced intensity. For example, a grating set to choose 680nm red illumination would also pass UV components at 340nm, 170nm, etc. with ever increasing attenuation. If the higher-order leaks are not blocked, this would lead to multiwavelength illumination for a given set wavelength and result in an erroneous trap characterization effort, especially in the case of higher-order above GaN bandgap components. To minimize the experimental errors due to higher-orders and to increase the measurement accuracy, we have placed a UV-rejection longpass filter with cut-on wavelength at 345nm. The measured transmission characteristics of the UV-rejection filter is shown in Figure

81. By checking the longest filtered wavelength (340nm), we set the maximum of the PS wavelength sweep to 680nm. This enabled us to perform a higher-order free illumination from 680nm to 360nm without any attenuation caused by the UV-rejection filter.

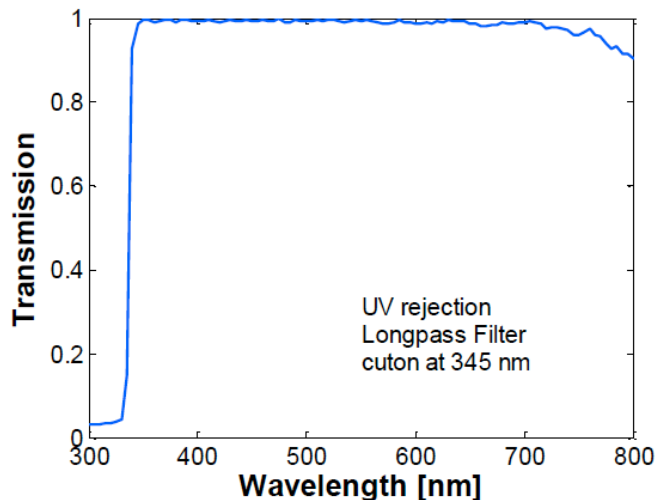


Figure 81. Transmission characteristics of the UV-rejection higher order filter.

The optical intensity spectrum is measured using a combination of Oriel 70124 pyroelectric detector, Spectra-650 colorimeter and Oriel 77346 photomultiplier tube. The reason to use multiple detectors is that none of the three covers the wavelength range of interest completely. The pyroelectric detector has flat responsivity for wavelengths longer than the cut-off at 580nm. Hence, the pyroelectric detector is used to verify the reading from the Spectra-650 colorimeter for wavelengths longer than 580nm. While the Spectra-650 is verified, it has a cut-off for lower than 380nm. Finally, by using the Oriel 77346 photomultiplier tube and the colorimeter for the 400nm to 360nm range, we were able to obtain the optical intensity for the entire range of interest. By normalizing the optical intensity with the incident photon energy, we have obtained the relative photon count for each wavelength. Consequently, the extracted data from the PS measurements are calibrated with the relative photon count data to normalize the measured areal trap density at each energy. While the Keithley 4200-SCS system is used during the most of the study, the high power state electrical stressing of the devices were with the custom built electrical stress & characterization system located at the Nanoscale Research Facility at University of Florida. This high power system is capable of applying $\pm 60V$ to all three terminals of the device while passing several hundreds of milliamperes for a desired period of time and type, such as step stress, constant stress, step-recovery stress, pulse-recovery stress, etc.

7.6.2 Results and Discussion

A typical photoionization spectroscopy data measured from a $5\mu m$ TLM site on Si substrate is shown in Figure 82.

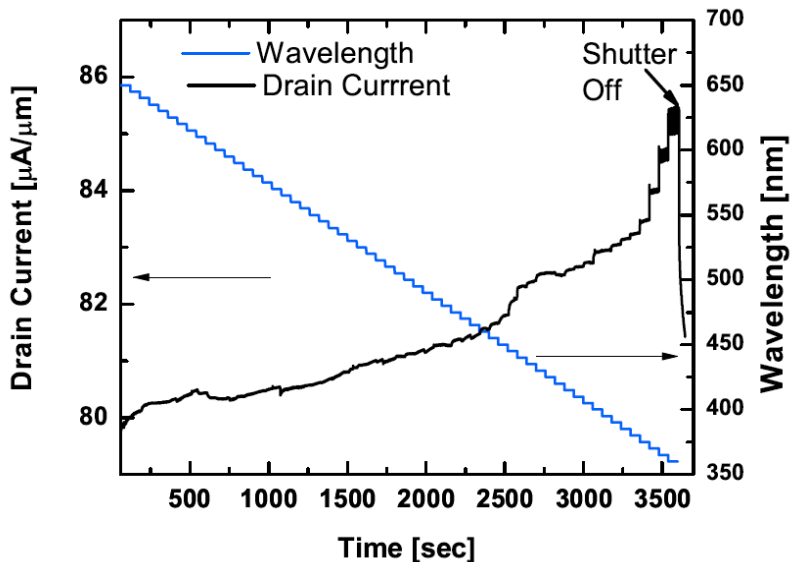


Figure 82. A typical photoionization spectroscopy data from a 5 μm TLM site on Si substrate is shown. For a wavelength sweep of 650nm to 360nm with decrements of 5nm and exposure time of 60 seconds, the photoexcited drain current evolution with changing wavelengths over time is presented.

The wavelength is swept from 650nm to 360nm with decrements of 5nm and an exposure time of 60 seconds at each wavelength. The shutter is turned off after 60 seconds of band gap illumination at 360nm. After the light is turned off, the linear drain current decreases immediately due to the recombination. The initial sharp drop due to recombination is a very fast transient due to the very low intrinsic carrier concentration of the GaN ($\sim 10^{-10}\text{cm}^{-3}$) [Levinstein2001]. After the initial sharp drop, the linear drain current decays exponentially. The evolution of the near steady-state non-equilibrium photoexcited drain current with time is used to obtain the relative changes between increments in the photon energy. Figures x-34 and x-35 shows the extracted normalized energy distribution of areal trap density for TLM structures on Si and SiC substrates respectively. The total trap density in SiC substrate devices is found to be smaller compared to the Si substrate devices. The main difference between SiC and Si substrate device traps is observed at the near bandgap trap densities. The Near band gap trap density in SiC based devices is less than the half of that in Si substrate. It is shown that the near bandgap traps are attributed to structural defects in GaN [64, 96]. Since SiC has a better matching lattice constant with GaN compared to Si (111) substrates, a lower structural density is expected, reducing the photosensitivity of the drain current to near band gap illumination.

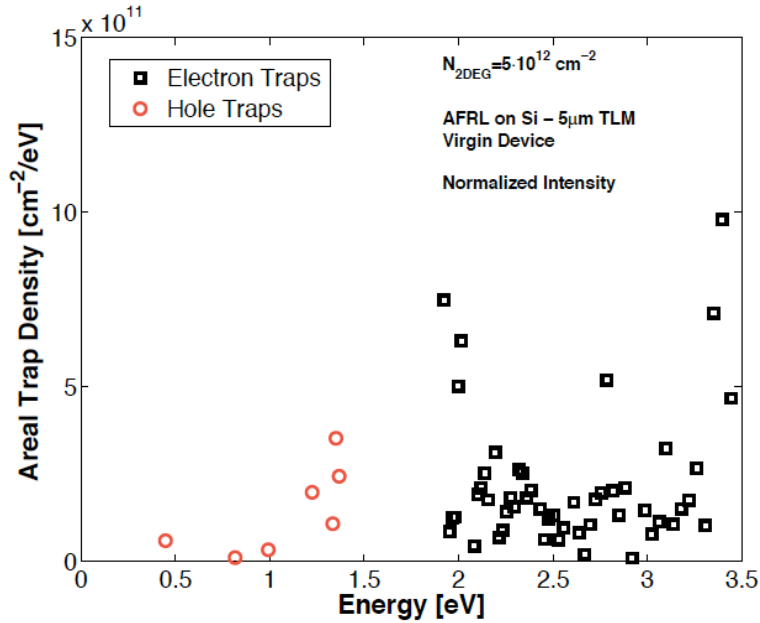


Figure 83. Extracted normalized energy distribution of the areal trap density is shown for a 5 μm TLM structure on the Si substrate. The 2DEG density is approximated as $5 \times 10^{12} \text{ cm}^{-2}$ using the CV data from the CV-dot site.

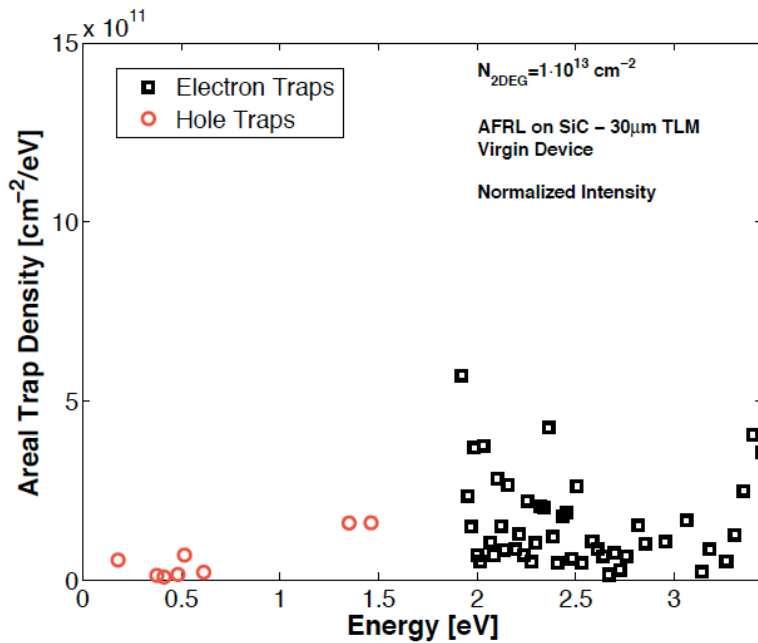


Figure 84. Extracted normalized energy distribution of the areal trap density is shown for a 30 μm TLM structure on the SiC substrate. The 2DEG density is approximated as $1 \times 10^{13} \text{ cm}^{-2}$ using the CV data from the CV-dot site.

7.7 Conclusion

Stress is inherent to AlGaIn/GaN HEMTs, and can benefit or degrade performance and reliability depending on the operating condition. Lattice mismatch stress between AlGaIn and GaN benefits the device by inducing polarization and creating the 2DEG, while additional stress generated via the inverse piezoelectric effect can induce degradation. Mechanical stress applied by four-point wafer bending is used to isolate the effect of stress on the AlGaIn/GaN HEMT devices in order to study the impact of stress on performance and reliability.

The effect of strain on AlGaIn/GaN HEMT drain current and gauge factor was investigated experimentally and theoretically. A novel technique was developed to apply external stress to small ($\sim 1 \text{ cm}^2$) wafer samples while simultaneously taking electrical measurements. The enormous variation in AlGaIn/GaN HEMT gauge factor measurements (4 to -40,000) reported in literature was explained as a likely result of charge trapping effects. After eliminating the charge trapping effects, the measured gauge factor of the AlGaIn/GaN HEMT was determined to be -2.8 ± 0.4 . This gauge factor indicates a small stress dependence on the device resistivity. The strain-altered 2DEG sheet carrier density and electron mobility were considered. It was found that externally applied mechanical stress has negligible effect on the electron density, due to the near cancellation of the stress-induced piezoelectric polarization in both the AlGaIn and GaN layers. Strain is incorporated into an sp^3d^5 tight-binding model to calculate the mobility change under uniaxial and biaxial stress. The simulation result suggests negligible mobility change due to the fact that the single GaN conduction band barely warps. Comparing simulation with the experimental results, the best fit set of material parameters was determined.

To investigate the dominant gate leakage mechanism in reverse-biased GaN HEMT, a thorough investigation of the relationship between E_{AlGaIn} and V_G is provided. In a simple model of an ideal 1D device, E_{AlGaIn} has a linear relationship to V_G above V_T and saturates below V_T . Adjusting σ_{int} and n_s based on experimental measurements provided an accurate V_G versus E_{AlGaIn} relationship above threshold. Also, a 2D simulation was performed to provide insight on E_{AlGaIn} for large reverse biases much below V_T .

Several possible gate leakage mechanisms were investigated by comparing the experimental observations and theoretical modeling. The direct tunneling and bulk trap-assisted leakage mechanisms are unlikely to dominate the gate leakage in reverse-biased GaN HEMT. The theory of defect band induced leakage is feasible to explain the experimental measurement, though it requires further investigation. The gate leakage increases (decreases) with tensile (compressive) stress and its stress sensitivity decreases at larger reverse bias. To fully understand the stress-altered gate leakage, the effects of mechanical stress on individual contributing factors need to be further clarified and properly combined.

Strain relaxation in heterostructures can occur either through trap generation or self- or inter-diffusion, and the process with more favorable kinetic conditions takes place. A modified electrical step stress experiment is designed to investigate the dependence of the 'critical voltage' (at which permanent electrical degradation begins) on varying time-steps or the length of time for which each voltage step is applied. It is observed that degradation in AlGaIn/GaN HEMTs is time dependent and can also take place at voltages below the critical voltage. The time dependence of the gate leakage current transient that occurs for a step function change in gate voltage is a topic that will be investigated further.

A metal-semiconductor tunneling model through a triangular barrier to simulate gate current across Ni-AlGaIn Schottky interface is studied by varying the tunneling distance. The tunneling distance is varied due to gate metal diffusion using a Fick's limited-source diffusion model. A close fit of simulated current, under varying biases and temperatures, with

experimentally measured IG degradation provides further evidence that a metal diffusion mechanism may potentially be causing the observed time-dependent I_G degradation in AlGaN/GaN HEMTs.

Using the photoionization spectroscopy technique, we have devised an experimental baseline to measure and characterize traps in AlGaN/GaN based devices. The details of the method and the experimental setup are provided. Energy distribution of the areal electron and hole trap densities from TLM and HEMT devices with both Si and SiC substrates are extracted. It is found that the SiC based devices have much lower trap densities around the GaN bandgap, which is attributed to the structural defects in the GaN.

Section 8 - Reliability Simulation

Multiphysics modeling is useful for a variety of applications. The modeling of some micro-electro-mechanical systems (MEMS) requires physics from the electrical, thermal, and mechanical domains. Thermal actuators, for example, rely on Joule heating of materials that have mismatched coefficients of thermal expansion to induce mechanical deformation. Similarly, electro-thermo-mechanical (ETM) simulations enhance reliability assessment and performance prediction of AlGaN/GaN high electron mobility transistors (HEMTs). Under normal operating conditions these high-power devices can undergo significant self-heating and non-uniform strains may arise due to the inverse piezoelectric effect in the AlGaN and GaN layers.

Multiple commercial tools handle various aspects of multiphysics modeling and tend to be application specific. Silvaco Atlas and Sentaurus SDevice are routinely used for modeling transistor device performance since their handling of electronic transport in semiconductors is robust. They each have fully coupled, electro-thermal solvers, but limitations in the mechanical domain. Atlas does not have a mechanical solver and SDevice does not support the inverse piezoelectric strain or a temperature dependence on Young's modulus. COMSOL provides ETM simulations and is well suited for MEMS among many other modeling applications where electronic transport in semiconductors is unnecessary.

Up to now, researchers who need to model in all three domains and a rigorous treatment of electronic properties in semiconductors use a combination of commercial software packages or write their own code. Venkatachalam et al. used a combination of Sentaurus for the electrical simulation and COMSOL for the thermal-mechanical simulation to model GaN-based HFETS [Venkatachalam2011]. Gao et al. used Silvaco Atlas and in-house software to simulate ETM effects on a GaN HEMT [Gao 2010]. In both cases the mechanics were one-way coupled to the electrical part. Thus, any strain-induced change on electrical performance could not be captured. One group has amassed capability of fully-coupled simulation of strain and electronic transport in nanostructured devices [der Maur 2011]. However, thermal effects were not considered.

Fully-coupled ETM simulations could benefit reliability assessment of AlGaN/GaN HEMTs. Horton et al. show that mechanical strain in the device enhances impurity diffusion on the drain side of the gate in the off state, which ultimately affects I-V characteristics.

We have augmented the Florida Object-Oriented Device Simulator (FLOODS) to handle physics in the electrical, thermal, and mechanical domains in a fully coupled, self-consistent way using the finite-element discretization method (FEM). This solver is both general and specific enough to support many different applications (eg. MEMS and transistor devices) and is flexible enough to account for new physics in a simple way. The structure of this paper is as follows: the general differential equations used to comprise the ETM domains are discussed along with our approach to numerical discretization in Section II. Section III includes comparisons of simulation results to commercial software and a novel application of ETM modeling on an AlGaN/GaN HEMT.

8.1 ETM Physics and Simulation Methods

FLOODS can simultaneously solve the governing partial differential equations in the electrical, thermal and mechanical domains. Carrier transport models including conventional drift-diffusion to the hydrodynamic model using energy balance equations described in are all possible. Moreover, the FLOODS platform has the flexibility to incorporate various physical models for heat generation, mobility, or piezoelectric effects, for example. Full self-consistency and coupling is possible through the use of the finite element method.

Alagator

FLOORS employs a scripting language (Alagator), originally developed for process simulation, to describe the governing physical partial differential equations. The equations are stored as character strings in a parameter database that is initialized on startup with appropriate defaults. Each solution variable / material combination can have a different differential equation. Interfaces between materials are treated as a different material, so interface transport can be handled. A matrix is then constructed of rows of solution variables (electrostatic potential, holes, elastic stress) and columns of materials (GaN, AlGaN, Interface between GaN and AlGaN). This allows different approximations in different regions for different solution variables.

Advantages for Reliability Simulation

Our simulator provides three major advantages for reliability simulations. By using FEM discretization, full self-consistency and coupling exists between all physical domains. Though self-consistency may not be necessary for every reliability simulation, it is conceivable that for certain applications this would be useful. Moreover, the incorporation of various physics (for example: the effects of single event upsets to strained-nMOS devices [Cummings 2010] and radiation induced oxide charging [Rowsey 2012]) are easily implemented within the same simulation platform using Alagator.

The common partial differential equations that model electrostatics and charge transport in semiconductors, heat conduction, and linear elastic behavior of solids are presented :

$$\begin{aligned}\nabla^2\psi &= -\frac{q}{\epsilon_p}(p - n + N_D - N_A) \\ \frac{\partial n}{\partial t} &= \frac{1}{q} \nabla \cdot J_n - r_n + g_n \\ \frac{\partial p}{\partial t} &= \frac{1}{q} \nabla \cdot J_p - r_p + g_p \\ c \frac{\partial T}{\partial t} - \nabla \cdot K \nabla T &= Q \\ \nabla \cdot \sigma &= 0\end{aligned}$$

The Poisson equation is given first, where ψ is electrostatic potential, n is the density of electrons, p is the hole density, N_A and N_D are ionized acceptor and donor densities, respectively, q is charge, and ϵ_p is permittivity. Equations for continuity of electrons and holes are second and third, where J_n and J_p are the electron and hole current densities, respectively, and r and g are recombination and generation terms. The thermal domain is characterized by the heat conduction equation (fourth), where T is temperature, c is the specific heat capacity, K is thermal conductivity, and Q is the heat generation term. The mechanical equilibrium equation (fifth) governs elastic deformation with no external forces. Stress σ is related to strain ϵ by the constitutive relation $\sigma = D(\epsilon - \epsilon_0)$, where D the stiffness matrix is a function of Young's modulus and Poisson's ratio. Mechanical strain caused by a mismatch of the thermal coefficient of expansion between two materials is modeled by a definition for initial stress given as

$$\epsilon_0 = \alpha_{mismatch} \Delta T,$$

where $\alpha_{mismatch}$ is the difference in the coefficients of thermal expansion. Strain due to the inverse piezoelectric effect is modeled by:

$$\epsilon_0 = \nabla \psi \cdot d_{pz},$$

where d_{pz} is the matrix of inverse piezoelectric coefficients.

The Scharfetter-Gummel (SG) formula and finite volume or finite-difference discretization schemes have historically made mathematical modeling of electronic transport in semiconductors possible. In this method,

the formulation of the current density, J_n and J_p , in the continuity equations includes separate drift and diffusion terms. Many commercial and noncommercial device simulators including PICES-II, PADRE, Sentaurus SDevice, and Silvaco Atlas are based on this method. On the other hand, mechanical solvers conventionally employ finite-element methods. Solving coupled, partial differential equations in the three domains in a concurrent and self-consistent way poses a computational challenge if different discretization methods are used. We have circumvented this challenge by formulating the drift and diffusion current as quasi-linear functions of the gradients of the quasi-Fermi levels and using finite-element methods to discretize the electron and hole continuity equations. An example of this formulation for electron current density is given below

$$J_n = -q\mu_n n \nabla \phi_n,$$

where μ_n is mobility and ϕ_n is the quasi-Fermi level that can be related to the electrostatic potential by the Boltzmann relation. A previous paper shows good agreement between a finite-volume method based on the Scharfetter-Gummel formula and the afore-mentioned finite-element method based on the quasi-Fermi representation; plus the FEM approach showed even better numerical accuracy for applications that require isotropic current flow [Cummings 2009]. With this method, a heat generation term due to Joule heating may be directly computed using the formulation given by: [Wachutka 1990].

$$Q = q |J_n|^2 / (\mu_n n) + q |J_p|^2 / (\mu_p p)$$

8.2 Simulation Results

Calibration

To validate FLOODS' ETM capabilities, 2-D simulation results from FLOODS are provided on examples of a MEMS thermal actuator and an AlGaIn/GaN HEMT and compared to results from COMSOL or Sentaurus. The first results are for a thermal actuator. Fig. 85 shows the mechanical deformation caused by a 3 V bias on the resistive heating element inside the bimorph beam. Dirchlet boundary conditions for the displacement and temperature were assigned to the bottom of the structure (bulk Si). Small deformation and plane strain approximations were used for both simulations. Fig. 86 shows good agreement between results from FLOODS and COMSOL of displacement along the top of the beam.

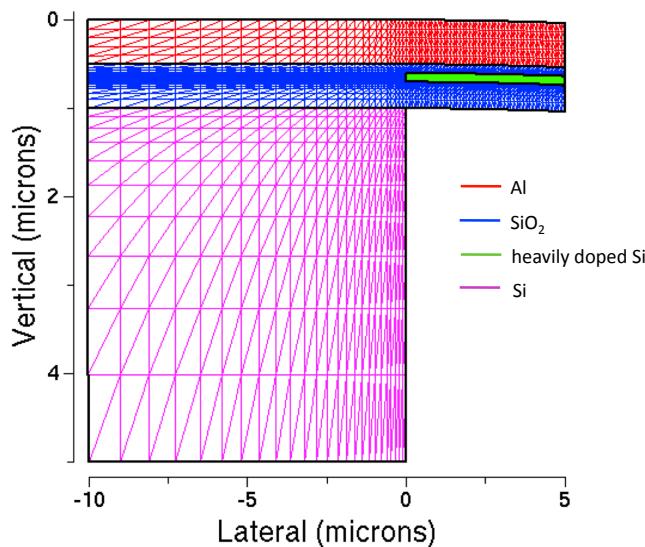


Figure 85. FLOODS electro-thermo-mechanical simulation of a 2-D MEMS thermal actuator showing the resulting beam deformation with 3V bias across the polySilicon heater.

Next, an electro-thermal simulation of an AlGaN/GaN HEMT in FLOODS is compared to one done in Sentaurus SDevice. The HEMT structure used in both simulators consisted of an undoped 1.0 μm SiC substrate, an undoped 0.20 μm AlN layer, a 1.775 μm GaN layer with an acceptor doping level of $6.5 \times 10^{16} \text{ cm}^{-3}$, and an undoped 0.025 μm

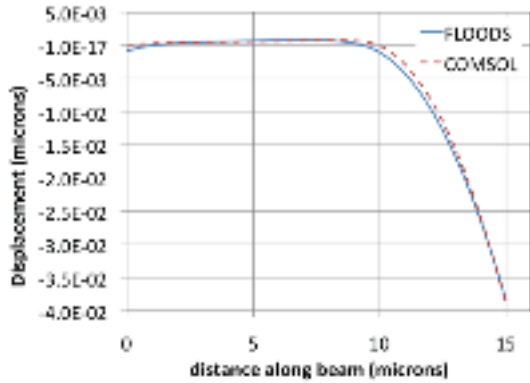


Figure 86 – Electro-thermo-mechanical simulation validation on a 2-D MEMS thermal actuator showing vertical displacement at the top of the beam. The FLOODS results are compared to COMSOL results.

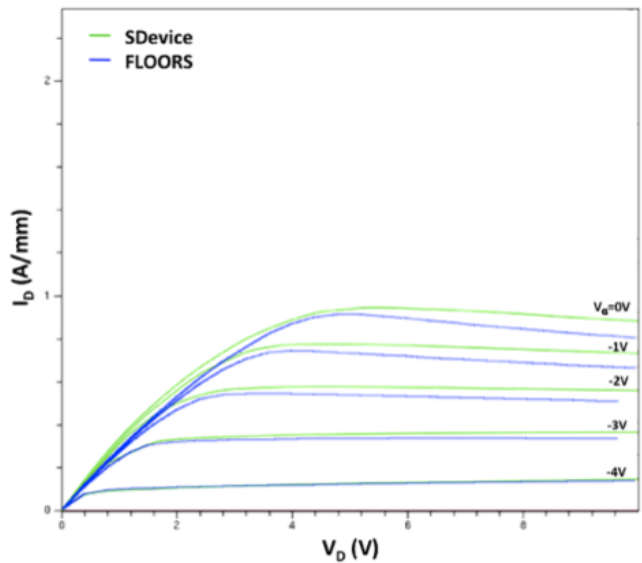


Figure 87. Drain current as a function of drain voltage for various gate voltages of an AlGaN/GaN HEMT. The FLOODS simulation results are compared to results from Sentaurus SDevice.

$\text{Al}_{0.26}\text{Ga}_{0.74}\text{N}$ layer. The structure was 4.0 μm wide. A 0.25 μm t-gate was contacted at the center of the surface of the AlGaN layer and source and drain were contacted to the AlGaN at the left and rightmost regions of the layer. An insulating oxide layer was created on top of the AlGaN layer that also surrounded the contacts. An interface charge of 1.17×10^{13} was placed between the AlGaN and GaN layers to reflect the spontaneous and piezoelectric polarization charge. Fig. 87 compares I-V plots for gate voltages ranging from 0 to -4 V. The characteristic decrease in drain current from self-heating at high drain bias is in good agreement with theory. The main difference in the curves is due to the treatment of lattice temperature. The

influence of the inverse piezoelectric effect and self-heating can be seen in the plot of vertical strain right below the AlGa_N surface shown in Fig. 88. The compressive strain peaks at the drain edge of the gate due to a corresponding peak in electric field and is in good qualitative

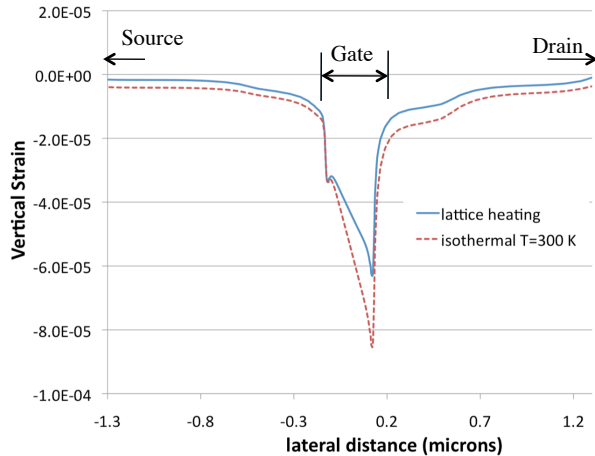


Figure 88. Effect of lattice temperature on the vertical strain along the AlGa_N layer of a HEMT simulated in FLOODS. The ETM model shows a decrease in compressive strain from the isothermal case, relating relaxation of the lattice. The bias conditions are $V_{gs}=0.0$ V and $V_{ds}=3.0$ V.

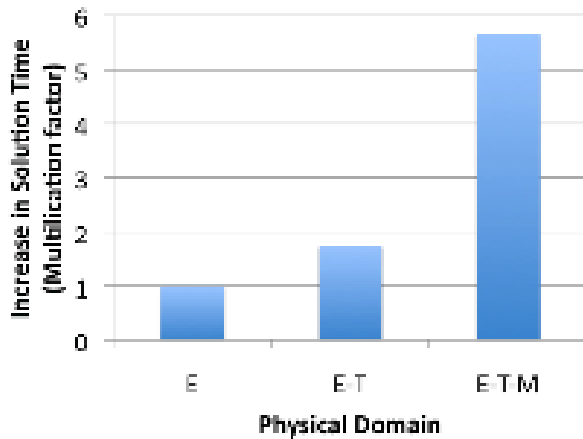


Figure 89. Comparison of solution time for the electrical-only, electro-thermal, and electro-thermo-mechanical simulations in FLOODS. [reprinted with permission from ...]

agreement with simulation results from Gao et al. [Gao 2010]. For the HEMT simulation, the Young's modulus was made dependent on temperature. Thus at elevated lattice temperatures, the decreased Young's modulus and addition of tensile strain due to thermal expansion of the AlGa_N act to decrease the compressive strain as compared to an isothermal simulation shown in Fig. 88.

Fig. 89 compares the increase in simulation time with increase in domains. Electro-thermal simulations take about twice as long to run than electrical simulations, while electro-thermo-mechanical simulations take about six times as long as electrical simulations.

Example: Reliability Study of an AlGa_N/Ga_N HEMT

Although excellent AlGa_N/Ga_N HEMT performance has been demonstrated, electrical stability and reliability issues of these devices remain obstacles to further development. Understanding the degradation mechanisms is necessary for improving the performance and reliability of AlGa_N/Ga_N HEMTs. From

observations performed by Joh [Joh 2008] and Ren [Ren 2011] it has become apparent that the degradation mechanism responsible for off-state reliability observations is not the same mechanism responsible for on-state reliability observations. Pit-like defects at the gate edges shown to be composed of the gate metal dominate in the off-state degradation mode. Hot electron effects have been suggested as a mechanism for on-state degradation [Miller 2000].

A. Off-State Degradation Model

Diffusion of Ni/Au metal stack from the gate of an AlGaN/GaN HEMT enhanced by mechanical strain from the inverse piezoelectric effect has been proposed as a mechanism for electrical degradation of AlGaN/GaN HEMT's in the off-state [Kuball 2011]. Ni diffusion from Ni/Au gates have been observed in degraded areas of devices, and characteristic bulk diffusion models have been matched to increases in trap concentration over time [Ren2011, Tapajna2010]. These observations have been linked to documented unrecoverable decreases in drain current and corresponding increases in gate current. FLOORS electro-mechanical device and process capabilities are used to model this multiphysics problem.

Using a model for strain-enhanced diffusion, Fig. 90 shows a comparison of the simulated metal diffusion derived from the previous strain conditions and a TEM showing metal diffusion in at the gate edges. The spatially varying metal diffusion profiles were then added to Poisson's equation as charged impurities. The newly added Ni metal impurities in the AlGaN layer, essentially acting as dopants, result in a new electrostatic potential distribution within the device. New IV curves at zero gate voltage are obtained for each of the bias conditions and diffusion profiles. Fig. 91 shows the simulated IV curves of these bias conditions. These compare well to the observed non-recoverable reductions in I_{ds} during off-state step-stress experiments performed by Joh *et al* [Joh 2008].

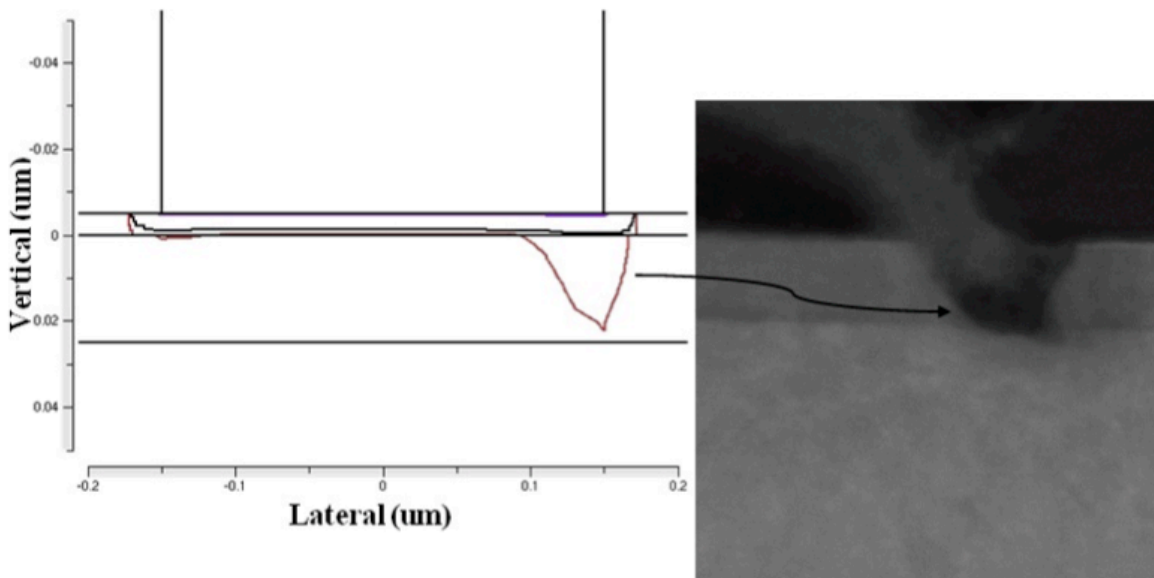


Fig. 90. Simulation of metal diffusion compared to TEM close-up of gate area showing metal diffusion in the OFF-state with $V_{gs}=-5V, V_{ds}=35V (V_s=0)$. Contours in simulation show enhanced diffusion at drain edge (right side) of gate where compressive strains are higher. Reprinted from [12] ©2012 IEEE

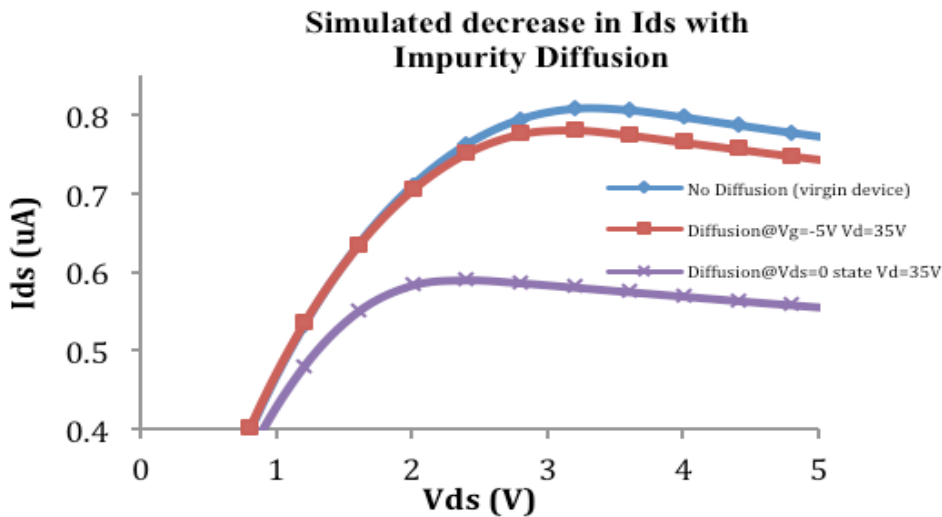


Fig. 91. Simulated IV curves for impurity diffusions formed by bias conditions shown in the data labels. I_{Dmax}/I_{Dmax0} Top blue curve shows the simulated I_{ds} for a device with no impurity diffusion into the AlGaN.

On-State Degradation Model

During an on-state bias condition, the vertical electric field under the gate contact is much less concentrated as compared to the off-state (~ 2 - 5 MV/cm vs 1 - 2 MV/cm peaks for off- and on-state respectively). This leads to a condition where the significant compressive strains at the gate edge, which develop in the off-state condition, no longer exist in the on-state.

As a result the degradation cannot be attributed to enhanced metal diffusion and this observation is indeed not seen in TEMs. There is however, significant self-heating in the lattice and very high electron temperatures which drive hot electron effects. The hot electron effect is modeled as a field driven Fowler Nordheim tunneling of energetic electrons through the AlGaN layer, coming to rest at the nitride passivation interface. To solve for the electron temperature, the hydrodynamic carrier transport model is implemented in FLOODS and a tunneling current is computed. The tunneling current quantifies how much trapped charge exists in the nitride and a resultant drain current reduction may be computed. Fig. 92 shows the simulation results of reduced drain current compared to experimental values.

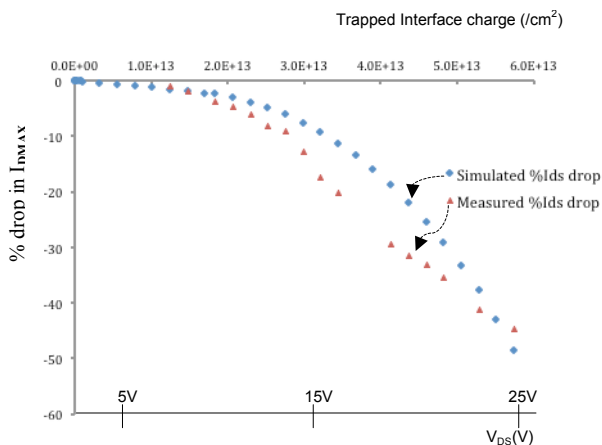


Fig. 92. (blue diamonds) Simulated % current drop vs. Increasing trapped charge (top horizontal axis). (red triangles) Measured %current drop vs Increasing drain bias (bottom horizontal axis).

Appendix A - References

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Appendix B – Publications from this MURI

Books

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“Reliability Simulation,” M.E. Law, M. Griglione, E. Patrick, N. Rowsey, D. Horton, Materials and Reliability Handbook for Semiconductor Optical and Electron Devices, Part II, Editors: O. Ueda and S. J. Pearton (Springer-Verlag, New York, 2013) Ch. 16, pp. 515-544.

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Dissertations

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- “Proton Irradiation Effects on InAlN/GaN HEMTs”, C.-F. Lo, L. Liu, H.-Y. Kim, J. Kim, S. J. Pearton, O. Laboutin, Yu Cao, J. W. Johnson, I. I. Kravchenko and F. Ren, 2012 Annual Joint Symposium and Exhibition, Florida Chapter of the AVS Science and Technology Society (FLAVS) and Florida Society for Microscopy (FSM), Orlando, FL, March 2012
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- “Trap Detection through Optical Pumping AlGaIn/GaN HEMTs”, D. Cheney, R. Deist, B. Gila, F. Ren, and S. Pearton, 2012 ROCS Workshop, Boston, MA, April 2012.
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- “Structural Defect Formation in Ni-Gated AlGaIn/GaN HEMTs”, M. Holzworth, N. G Rudawski, P. G Whiting, C.Y. Chang, E. A Douglas, S. J Pearton, K. S. Jones, L. Liu, T. S. Kang, F. Ren, L. Zhou, M. R. Johnson, D. J Smith, G. D.Via, 2012 Spring MRS, San Francisco, April 2012
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- “Proton irradiation effects on InAlN/GaN high electron mobility transistors”, Fan Ren and S. J. Pearton, GaN Materials and Devices VIII, SPIE Photonics West, San Francisco, Feb. 2013
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- “A Modeling Study of Proton Irradiation in AlGaN/GaN HEMTs Applied to Understanding the Increase of Critical Voltage for Pit-Shaped Defect Formation”, E. Patrick, M.E. Law, L. Lu, F. Ren and S.J. Pearton, 2013 IEEE Nuclear and Space Radiation Effects Conf, July 8-12, 2013, San Francisco, CA.
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- Weikai Xu and Gijs Bosman, “Space charge limited gate current noise in AlGaN/GaN High Electron Mobility Transistors,” ICNF 2013, June 2013, Montpellier, France. Published in the proceedings of the 22nd International Conference Noise and Fluctuations (ICNF), 2013, pp 1-4.
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- “Impact of proton irradiation on the dc and rf performance of AlGaN/GaN high electron mobility transistors”, L. Liu, Y. Y. Xi, F. Ren, S. J. Pearton, H.-Y. Kim, J. Kim and I. Kravchenko, ECS Fall Meeting, San Francisco, Oct 2013

Appendix C - Students and Post-docs

Mehmet Baykan (Turkey), Graduated, PhD

Christina Casler (US) undergraduate graduated

David Cheney (US)-PhD Dec 2012

Min Chu (China), Graduated, PhD

Camilo Velez Cuervo (Columbia) - PhD student supported

Blake Darby (US) graduate student switched to another project graduated

Ryan Davies (US) – MSE PhD student, graduated 12-2009; post-doc supported 1-2010 to 8-2010

Richard Deist (US citizen) – undergraduate student supported 10-2011 to May 2013

Robert Dieme (Nigeria), Post-doctoral Researcher

Erica Douglas (US)- Ph.D Dec 2011

Ben Gilstatd (US), MS Student, Graduated

Michelle Griglione (US), Post-Doc

Kenneth Hill (US) – undergraduate student, currently enrolled in graduate school at UF

Ray Holzworth (US) PhD student graduated

David Horton (Trinidad-Tobago), PhD expected in December 2013

David Hwang (US) undergraduate graduated

Ys-His Hwant (Taiwan) – PhD student supported

Amit Gupta (India), Graduated, PhD

Tsung-Sheng Kang (Korean) – PhD expected in 8-2014

Varun Khandelwal (India), MS ECE 2013

Andrew Koehler (US), Graduated, PhD ECE

Chien Fong Lo (Taiwan)-Graduate Ph.D

Liu Lu (China)-Ph.D. expected in December 2013

Vivian Munsey (US) undergraduate graduated

Jennilee Navales (US) –undergraduate student

Kathryn O'Hara (US) undergraduate graduated

Erin Patrick (US), Post-Doc

Henant Rao (India), PhD graduated

Nicole Rowsey (US), PhD student, graduated

Nick Rudawski (US) Post Doc

Nicholas Vito (US) PhD graduate student switched to another project

Xiaotie Wang (Chinese) - PhD expected 8-2014

Laurel Welch (US) undergraduate graduated

Pat Whiting (US) PhD student graduated

Weikai Xu (China) PhD expected Summer 2014

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Organization / Institution name

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Award Information

Grant/Contract Title

The full title of the funded effort.

A 21st Century Approach to Electronic Device Reliability

Grant/Contract Number

AFOSR assigned control number. It must begin with "FA9550" or "F49620" or "FA2386".

FA9550-08-1-0264

Principal Investigator Name

The full name of the principal investigator on the grant or contract.

Mark E. Law

Principal Investigator Name

Program Manager

The AFOSR Program Manager currently assigned to the award

James Hwang

Report Information - Annual Report

Report Information - Final Report

Report Information - Conference/Workshop Report

Report Information - Equipment Report

Report Information - Patent/Invention Report, DD882

Report Information - Financial Report, SF425

Report Information - STTR Status Report

Report Information - STTR Annual Progress Report

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Abstract

Lifetime prediction for device operation has usually relied on accelerated testing at elevated temperature and then extrapolation back to room temperature operation. This technique frequently fails for scaled, high current density devices found in modern technologies. Device failure is driven by electric field or current mechanisms or low activation energy processes that are masked by other mechanisms at high temperature. Device degradation can be driven by failure in either active structures or passivation layers. We have seen that many issues have an affect on compound semiconductor performance and reliability, including the material quality, strain state, surface cleaning process, and the actual voltage and current conditions during aging. We have conducted comprehensive plan of reliability engineering for III-V device structures. This includes materials and electrical characterization and reliability testing. These techniques were utilized to develop new simulation technologies for device operation and reliability. This allows accurate prediction not only of reliability, but the ability to design structures specifically for improved reliability of operation. Our intensely integrated approach of utilizing new characterization methods, device simulations and realistic device stressing and aging provided new insights into device failure mechanisms.

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Archival Publications (published) during reporting period:

Books

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Changes in research objectives (if any):

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None

Extensions granted or milestones slipped, if any:

None

For an STTR Status or STTR Annual Progress Report, please e-mail your program manager directly.

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Program Manager: James Hwang

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Abstract: Lifetime prediction for device operation has usually relied on accelerated testing at elevated temperature and then extrapolation back to room temperature operation. This technique frequently fails for scaled, high current density devices found in modern technologies. Device failure is driven by electric field or current mechanisms or low activation energy processes that are masked by other mechanisms at high temperature. Device degradation can be driven by failure in either active structures or passivation layers. We have seen that many issues have an affect on compound semiconductor performance and reliability, including the material quality, strain state, surface cleaning process, and the actual voltage and current conditions during aging. We have conducted comprehensive plan of reliability engineering for III-V device structures. This includes materials and electrical characterization and reliability testing. These techniques were utilized to develop new simulation technologies for device operation and reliability. This allows accurate prediction not only of reliability, but the ability to design structures specifically for improved reliability of operation. Our intensely integrated approach of utilizing new characterization methods, device simulations and realistic device stressing and aging provided new insights into device failure mechanisms.

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