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14. ABSTRACT
The goal of this project is to develop a modular, heterogeneous integration process to combine III-V tunable VCSELs, silicon photonic integrated circuits, and CMOS ICs in a seamless manner, and demonstrate a single-chip FMCW (Frequency-Modulated Continuous-Wave) LADAR source. In Phase 2, we have successfully developed through-silicon-vias (TSVs) on Si photonics at wafer level, and stacking the Si photonic dies on top of CMOS at die level. Electrical and mechanical properties of the bonded systems were characterized. FPGA and CMOS programming using a custom graphical user interface have been implemented, and optical and electrical interfacing to the system has been achieved. Demonstration of generation of a linearly ramped frequency chirp in closed loop operation has been demonstrated with the 3D integrated system. Quantitative results on the locking behavior have been obtained and are reported for the integrated system. We have obtained a very high ranging precision of 4.4um at 5cm, and have successfully imaged an 3D object (mechanical gear).

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MEMS-ELECTRONIC-PHOTONIC HETEROGENEOUSLY INTEGRATED FMCW LADAR SOURCE

Final Technical Report

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Program Manager: Dr. Josh Conway

UC Berkeley

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1. Introduction

The goal of this project is to develop a modular, heterogeneous integration process to combine III-V tunable VCSELs, silicon photonic integrated circuits, and CMOS ICs in a seamless manner, and demonstrate a single-chip FMCW (Frequency-Modulated Continuous-Wave) LADAR source. Our guiding principle for the heterogeneous integration is to leverage on the available foundry capabilities (CMOS and silicon photonics), and the ability to test individual components before integration ("known good dies" or "known good wafers"). We have adopted a three-dimensional (3D) integration strategy: The CMOS, silicon photonics, and the III-V lasers are initially fabricated by separate foundries (or in-house cleanroom facility), functionally tested at wafer level, and then heterogeneously integrated by wafer bonding. The electrical signals are connected with through-silicon-vias (TSVs), and optical signals are coupled through grating couplers. This approach has several advantages. It is modular, flexible, and can take advantage of the most advanced technology developed at foundries of individual components.

1.1. E-PHI Phase 2 – MEMS LADAR Source

In Phase 2, we continue the development of the FMCW LADAR source by advancing the development of new individual components and the integration processes through short-loop experiments. The continuously developed components are inserted into our system testbed, and their performance will be compared with the COTS baseline and theoretical models. We are porting our silicon photonics circuits, including passives and Germanium Photodiodes, onto a full 6" wafer process at UC Berkeley, with integrated TSVs. CMOS circuitry has been designed and fabricated through multi project wafer runs at TSMC. 3D Integration of Silicon Photonics and CMOS is performed on die level. MEMS Tunable VCSEL integration onto silicon photonics is developed separately, in order to minimize turnaround in short loop experiments. First experimental results on a hybrid Si/III-V HCG-DBR cavity laser are included in this report. The FMCW LADAR source demonstrator at the end of phase two will thus include a combined CMOS-Silicon Photonics integrated die, and light will be coupled into it from the MEMS tunable hybrid Silicon-III/V laser by fiber grating couplers.

1.2. Summary of Accomplishments

In Phase 2, **3D integrated systems of silicon photonics and CMOS were successfully fabricated**. This included the development of the processes for **under bump metallization** on the CMOS dies and **flip-chip bonding** of the CMOS and silicon photonics dies. **Electrical and mechanical properties** of the bonded systems were characterized. **FPGA and CMOS programming** using a custom graphical user interface have been implemented, and optical and electrical interfacing to the system has been achieved. Demonstration of **generation of a linearly ramped frequency chirp in closed loop operation** has been demonstrated with the 3D integrated system. **Quantitative results** on the locking behavior have been obtained and are reported for the integrated system. In parallel, advances in the development of the tunable VCSEL have led to a **heterogeneously integrated MEMS tunable VCSEL**, using stepper-based lithography defined MEMS actuated silicon high contrast gratings and III-V active region.

2. Frequency-Modulated Continuous Wave Lidar

Figure 1 Illustrates the operation principle of FMCW lidar. In this ranging method the frequency of a tunable laser is chirped linearly and periodically. When this chirp passes through an interferometer with an arbitrary but fixed path delay, τ, the light from the two paths interferes to create a beat frequency in optical intensity. This beat frequency is proportional to the delay, τ, and the frequency-sweep rate, γ, and can be measured to determine the path difference between the two arms of the interferometer, hence the target distance.

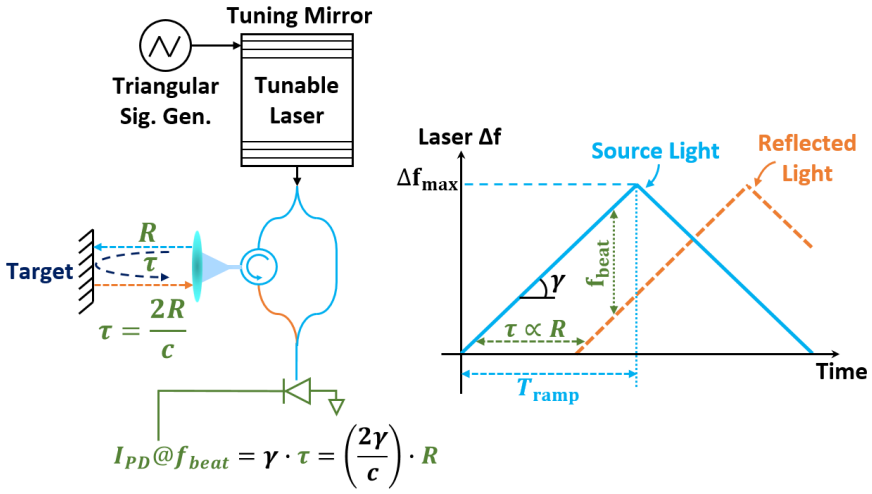

Figure 1: Operation principle of FMCW lidar

In the ideal case, the modulation rate, γ, is constant so that for a fixed target a single-tone beat signal is detected. In practice, however, many factors such as inherent nonlinearity of the laser tuning characteristic, temperature drift, aging, etc. can contribute to deviation from expected performance. In order to observe these effects the frequency of the laser is tuned with a triangular waveform generator and the beat signal from a fixed-length MZI is measured. The result of this measurement is shown in *Figure 2*.

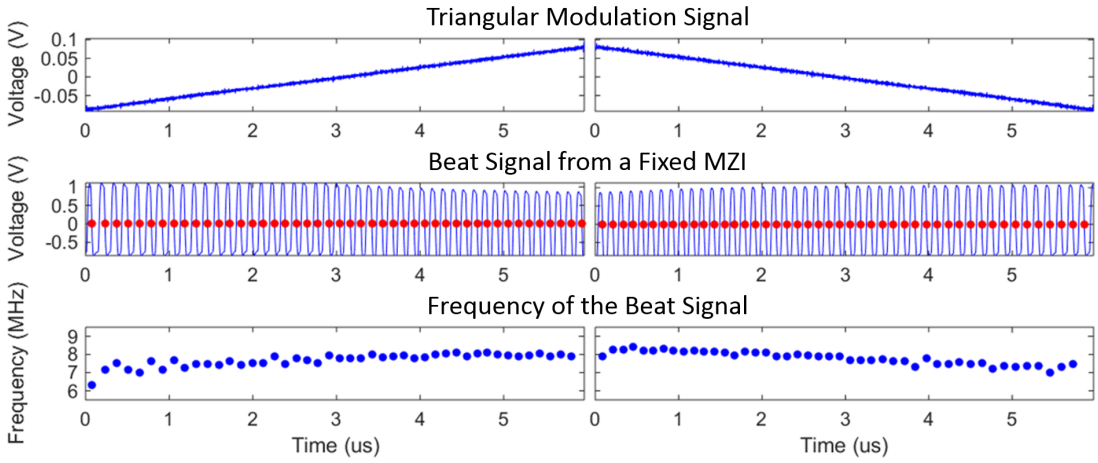

Figure 2: Beat signal and its corresponding frequency from zero-crossing measurements for a fixed length MZI

In order to have more quantitative picture from this result the systematic and stochastic errors in the measured beat signal should be decoupled. In order to do so, we perform the measurement of *Figure 2* for 100 successive modulation periods. Then, the systematic error in the beat frequency that is equivalent to the nonlinearity in the laser tuning characteristic is extracted by performing a point-by-point average on the beat frequency for corresponding points of all modulation periods. The result of this process for up-ramp parts of 100 successive modulation is shown in *Figure 3*. According to this figure the nonlinearity of the tuning characteristic causes 9% peak-peak variation (normalized to the last measurement point of the modulation period) in the beat frequency for a fixed target. This increases the effective bandwidth of the beat signal and in presence of wide-band added noise such as detector shot noise reduces its SNR and, consequently, degrades the sensitivity of the lidar in a ranging measurement.

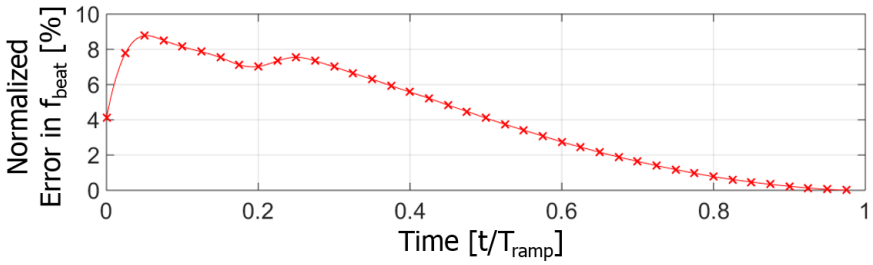

Figure 3: Normalized systematic error on f_{beat} averaged over 100 successive up-ramp modulations.

Similarly, in order to see the effect of stochastic errors the beat frequency is measured over 100 successive modulation periods, but this time it is averaged over each period separately and the histogram of the fluctuations across these 100 averages is shown in *Figure 4*. These results show that not-only γ has systematic error within each modulation period, it also experiences severe ramp-to-ramp fluctuation that can result in poor ranging resolution.

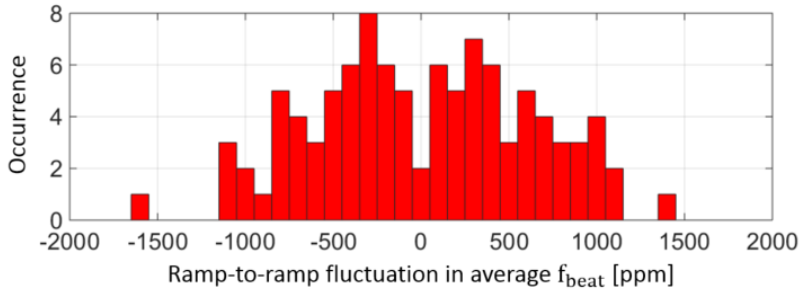

Figure 4: Distribution of the error in average beat frequency for 100 successive modulation ramps

In the next section it is shown that an electro-optical PLL (EO-PLL) can both linearize the modulation characteristic and reduce the ramp-to-ramp fluctuation in the modulation characteristic.

3. Electro-optical PLL: System and Circuits

As it was described in previous section, due to nonlinearity and drift in of the laser tuning characteristic, high-precision FMCW lidar cannot be accomplished open-loop laser modulation and a feedback loop is needed to correct and compensate the errors. In this section detailed description and design procedure of such a system and its important circuit blocks are given.

3.1. Laser modulation with EO-PLL

In order to implement a feedback mechanism the parameter that needs to be fixed is the modulation rate, γ. The feedback loop should comprise two functions: first to measure the error on γ, and second to provide a control mechanism to fix the error.

It was already discussed that the beat frequency at the output of a reference interferometer in the configuration of **Error! Reference source not found.** can be used to measure γ. Figure 5 shows a similar setup except that the modulation signal is now generated by alternating and integrating a slowly varying voltage, V_{in}.

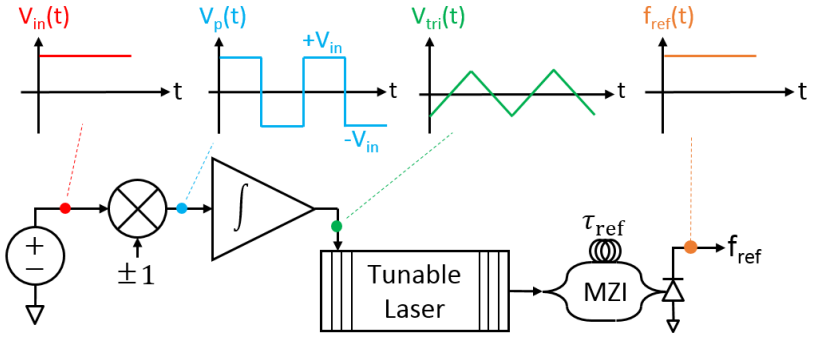

Figure 5: Demonstration of the combined functionality of integrator, laser, and MZI/PD as a voltage-controlled-oscillator

From Figure 5 it can be seen that the level of the input voltage, V_{in} can be used to control the slope of the triangular waveform and consequently f_{ref}. Thus, the combination of the integrator, tunable laser, and MZI/PD acts as a voltage-controlled oscillator (VCO).

It is well-known in electronics that a phase-locked loop (PLL) can stabilize the frequency/phase of a VCO with respect to a reference local oscillator. Such an architecture can used to lock the frequency f_{ref} in Figure 6 to a stable clock frequency f_{LO}. Thus, from Eq. **Error! Reference source not found.** we will have:

$$\gamma(t) = \frac{f_{ref}}{\tau_{ref}} = \frac{f_{LO}}{\tau_{ref}} \qquad (3.1)$$

Hence, by employing a stable electronic oscillator and a stable reference MZI, linear and stable frequency-modulation of the laser can be achieved. *Figure 6* shows an electro-optical PLL architecture that can perform this task. The control signal that alternates the input voltage of the integrator is provided by a hysteresis comparator that senses the modulation voltage level at the laser tuning port and at preset

upper or lower limits switches the sign of the integrator input voltage and, hence, the modulation ramp direction.

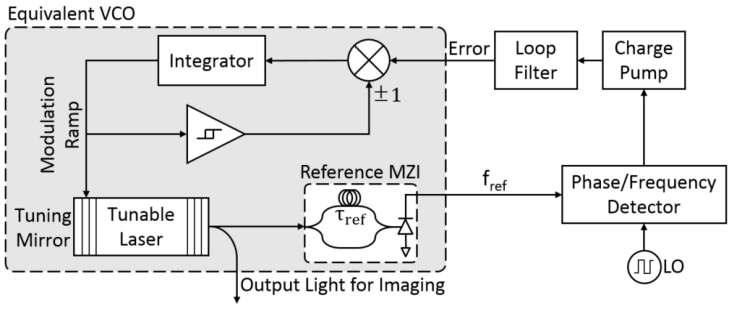

Figure 6: Electro-optical PLL for chirp linearization

The equivalent VCO of *Figure 6* operates like an electronic VCO, expect for the effect of transitioning between up and down ramps as shown in *Figure 7*.

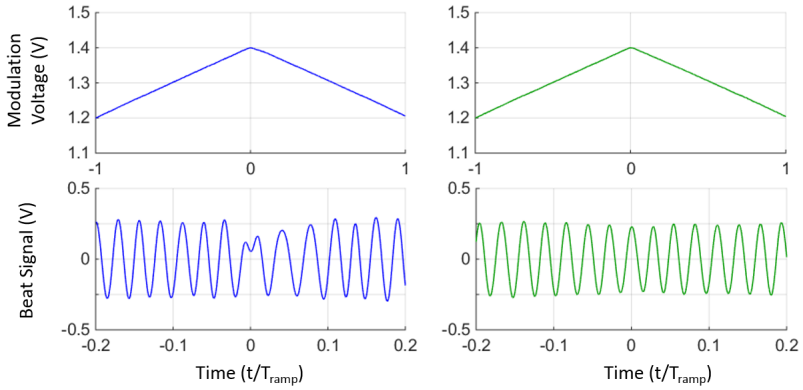

Figure 7: Effect of switching between up and down ramps at arbitrary phase (left) and peak (right) of the beat signal

The effect of ramp-switching can be understood by looking at the phase of the reference beat. Assume that the phase of the reference beat when the modulation signal transitions from up to down ramp is equal to φ_{sw}. Then, during the up-ramp the phase can be written as given below:

$$\varphi_{\mathrm{ref,up}}(t) = \varphi_{sw} + 2\pi \cdot \tau_{\mathrm{ref}} \cdot \gamma_0 \cdot (t - t_{sw}) \tag{3.2}$$

In this equation t_{sw} is the time at switching instant. For the down-ramp after switching:

$$\varphi_{\mathrm{ref,down}}(t) = \varphi_{sw} - 2\pi \cdot \tau_{\mathrm{ref}} \cdot \gamma_0 \cdot (t - t_{sw}) \tag{3.3}$$

In order to see a continuous beat without disturbance, equations (3.2) and (3.3) should result in the exact same waveforms for all *time* before and after switching instant:

$$\sin\left(\varphi_{\mathrm{ref,up}}(t)\right) = \sin\left(\varphi_{ref,down}(t)\right) \quad , \quad \text{for all } t \tag{3.4}$$

One possibility to satisfy Eq. (3.4) is to have $\varphi_{\mathrm{ref,up}}(t) = 2k\pi + \varphi_{ref,down}(t)$ which, according to Eq. (3.2) and Eq. (3.3), cannot hold; the other possibility is given below:

$$\varphi_{\mathrm{ref,up}}(t) - (2k+1)\pi = -\varphi_{ref,down}(t) \quad , \quad \text{for all } t \text{ and } k \in \mathbb{Z}$$

$$\Rightarrow \varphi_{sw} = k\pi + \frac{\pi}{2} \quad , \quad \forall k \in \mathbb{Z} \tag{3.5}$$

Hence, if ramp-switching happens at the peak of the reference beat, as it is the case in the right panel of *Figure 7*, then it won't disturb the beat waveform and EO-PLL will continue its operation under normal condition. For switching at any point other than beat peak, there will be an abrupt jump in the beat phase as shown in the left panel of *Figure 7*. This jump will be sensed by the phase detector of the EO-PLL shown in *Figure 6* and will cause it to exhibit a settling behavior. Therefore, the EO-PLL architecture of *Figure 6* removes the inherent nonlinearity of the laser modulation characteristic, but introduce a new source of error to γ.

As it was discussed in previous section any error on γ can have negative impact on the performance of the lidar based on this EO-PLL. The effect of switching error due to its stochastic nature can be worse than a systematic nonlinearity. Without any control on the switching instant with respect to the beat phase, the switching can introduce a random initial error between $\pm 180°$ and cause an entirely random settling pattern based this initial error. The point-by-point standard deviation of the settling error over 100 modulation ramp is shown in *Figure 8*.

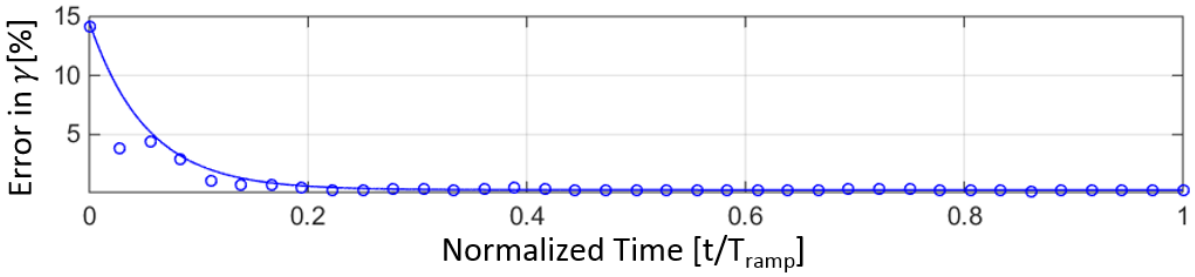

Figure 8: Point-by-point standard deviation of the random switching error over 100 modulation ramps

3.2. Proposed EO-PLL architecture with gated ramp-switching

According to the discussion in previous section, in order to avoid disturbing the EO-PLL performance the ramp-switching should happen at peak of the beat signal. This can be done by gating the output of the hysteresis comparator responsible for the ramp-switching. The clock-edge for this gate should be at peak of the reference beat or, in other words, in quadrature with its zero-crossing as shown in *Figure 9*.

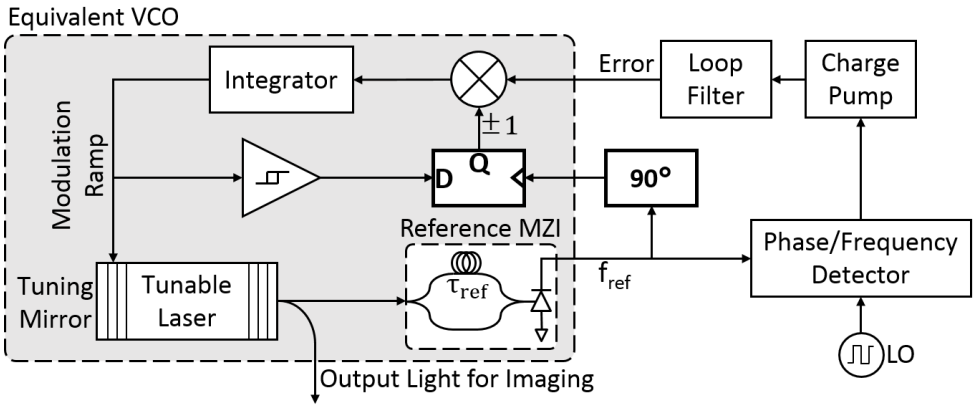

Figure 9: EO-PLL with gated ramp-switching

The system in *Figure 9* could potentially solve the problem with switching error, but the switching signal generated by the DFF has to go through the integrator, laser, reference MZI and PD before appearing on the reference beat. Hence, an adaptive ramp-switching mechanism should be employed to generate the optimum gate clock which may not necessarily be in quadrature with the reference beat. In order to generate clock edges at any arbitrary phase of the beat signal a multiplicative electronic PLL can be used. Since LO and beat signal are locked, LO can be used as the reference for this PLL. Architecture of such a PLL is shown in *Figure 10*.

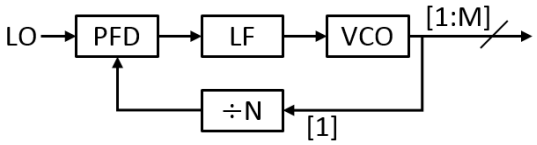

Figure 10: Multiplicative PLL to generate reference clock for adaptive gated switching

The PLL of *Figure 10* employs a VCO with M phases each at a frequency N times higher than the LO. Hence, $M \times N$ equally spaced clock edges are generated within each LO cycle. A digital control unit can be used to select any of these clock edges to gate the switching signal.

In order to pick the optimum clock edge for switching, the control unit should also be provided by the switching error. The error in the beat frequency after each switching event is measured using a counter-based time-to-digital converter (TDC). The reference clock for the TDC is also provided by the same PLL. After each switching instant the number of the clock edges from all *M* PLL phases between two successive zero-crossings of the beat signal are counted. If the beat is perfectly locked to LO this number should be equal to $M \times N$. Any deviation from this number is an indication of error and the control unit sweeps the switching instant until the error is minimum.

Figure 11 illustrates the high level block diagram of the EO-PLL with adaptive gated switching mechanism. The phase multiplexer uses the control bits from the digital unit to select one of the $M \times N$ phases from the PLL for switching.

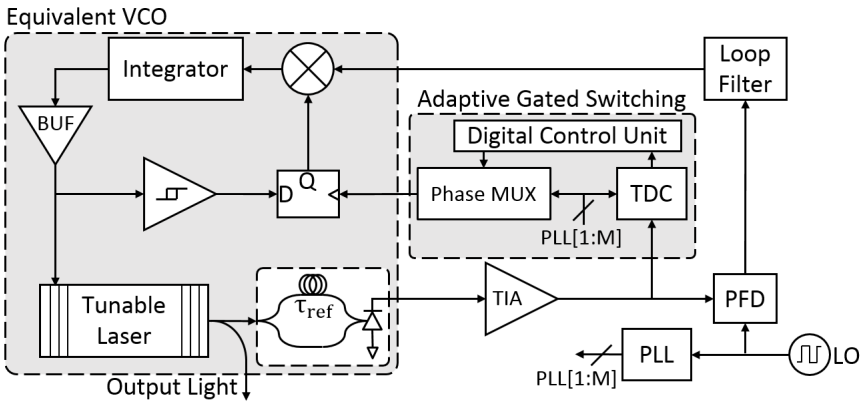

Figure 11: Final Architecture of the EO-PLL with adaptive gated ramp-switching

3.3. EO-PLL analysis and design criteria

So far it was shown that the proposed EO-PLL architecture in *Figure 11* can be used for triangular frequency modulation of the tunable laser and while employing gated ramp-switching to avoid disturbing the EO-PLL performance at turning points of the triangular waveform. In this section the design procedure will be discussed and optimum values for system variables such as τ_{ref}, T_{ramp}, f_{LO}, loop filter, etc. will be determined.

An important aspect of this design is integration. Among all the elements in *Figure 11* tunable laser, electronic LO, and the digital control unit will be off-chip discrete parts, but all the rest of the electronic and optical elements will be on either CMOS or silicon-photonic chips respectively. This way of implementation will have certain implications in the design procedure that should be considered.

3.3.1. EO-PLL transfer function design

The EO-PLL transfer function consists of the tunable laser, MZI, loop filter and integrator. The tunable laser is a packaged semi-commercial part and the MZI with 330ps differential delay is fabricated on the silicon-photonic chip. Hence, the transfer function design only involves determining the integrator gain and the loop filter shape.

The tunable laser is an edge-emitting laser with DBR facets and its frequency can be modulated by carrier injection. Its tuning port is terminated with 40Ω small-signal resistance. The DC tuning gain is 24.4 GHz/mA that combined with 40Ω termination translates to 610GHz/V. Hence, the transfer function from applied tuning voltage to the output phase of the laser can be written as given below:

$$T_{\mathrm{laser}}(s) = \frac{2\pi\times 610}{s}\,[\mathrm{Grad/V}] = \frac{3.83}{s}\,[\mathrm{Trad/V}] \tag{3.6}$$

The MZI has 330ps differential delay, hence the transfer function from the phase of its input light to the phase of its output beat tone can be written as given below:

$$T_{\mathrm{MZI}}(s) = 1 - e^{-s\cdot\tau_{ref}} \approx s\cdot\tau_{ref} = 330\times 10^{-12}\times s\ \ [\mathrm{rad/rad}] \tag{3.7}$$

Combined with the integrator, the transfer function of the equivalent VCO would then be:

$$T_{VCO}(s) = \frac{k_{int}}{s} \times T_{MZI}(s) \times T_{\text{laser}}(s) = \frac{1.25 \times k_{int}}{s} \text{ [krad/V]} \tag{3.8}$$

In order to phase-lock the beat signal to LO a type-II PLL should be employed. One of the poles at origin comes from the equivalent VCO and the other should be included in the loop-filter transfer function. In addition to the pole at origin, loop-filter should also include a zero to provide enough phase-margin for stability of the feedback loop. Finally, similar to other charge-pump PLLs, an extra pole (not at origin) should be include in the loop filter to suppress the effect of the pulse series from PFD. The frequency of this pole is generally chosen 5 to 10 times above the frequency of the zero; however in this case due to the extra delay in the loop and in order to not reduce the phase margin further, it is chosen 20 times above the frequency of the zero. Without loss of generality we can assume that all the gain from equivalent VCO, PFD, charge pump, and loop filter is embedded in a single parameter k. Then the overall loop gain will be given with the following equation:

$$LG(s) = \frac{k(1 + s/\omega_z)}{s^2(1 + s/\omega_p)} \tag{3.9}$$

The EO-PLL corrects any stochastic or systematic error on the γ within its bandwidth; hence larger bandwidth is desired. However, the delay in the feedback loop due to fiber connection from laser and other discrete optical parts such as isolator and polarization controller large loop bandwidth can instability. The delay from the fibers is around 20ns. In order to limit the phase shift caused by this delay to lower than 5° the unity-gain bandwidth of the loop should satisfy the following equation:

$$20\text{ns} \times \omega_u = 5° \Longrightarrow \omega_u \approx 2\pi \times 700 \text{ krad/s} \tag{3.10}$$

For 70° phase margin ω_z should be chosen 3 times lower than loop bandwidth, hence:

$$\omega_z \approx 2\pi \times 235 \text{ [krad/s]} \tag{3.11}$$

$$\Longrightarrow \omega_p = 20 \times \omega_p = 2\pi \times 4.7 \text{ [Mrad/s]} \tag{3.12}$$

Finally, from Eq. (3.9) and with $\omega_u/\omega_z = 3$ it can be shown:

$$k = \frac{{\omega_u}^2}{3} = 6.5 \times 10^{12} \text{ [}s^{-2}\text{]} \tag{3.13}$$

The nonlinearity of the modulation characteristic causes a periodic disturbance in the beat frequency with a repetition period of $2 \times T_{\text{ramp}}$. It will be shown in later sections that the effect of nonlinearity needs to be suppressed at least by 30dB to be considered negligible compared to the RMS value of the beat frequency noise caused by the laser phase noise. In order to have 30dB suppression, and considering the shape of the EO-PLL noise transfer function the modulation frequency should be at least 2.6 times lower than ω_z:

$$2 \times T_{\text{ramp}} > \frac{1}{235\text{kHz}/2.6} \Longrightarrow T_{\text{ramp}} \gtrsim 5.5 \text{ [}\mu s\text{]} \tag{3.14}$$

Combined with the tuning depth of the laser $\Delta f = 122\text{GHz}$, the reference MZI delay of 330ps and with $T_{\text{ramp}} = 5.6\mu s$, the following equation can be used to find f_{LO}:

$$\gamma = \frac{\Delta f}{T_{\text{ramp}}} = \frac{f_{\text{LO}}}{\tau_{\text{ref}}} \Longrightarrow f_{\text{LO}} = 7.2\ [\text{MHz}] \tag{3.15}$$

The other constraint on f_{LO} in a charge-pump PLL comes from its sampling effect in PFD that can cause extra delay and, hence, instability in the feedback loop. Due to this effect, f_{LO} is usually chosen 10 times larger than loop bandwidth. Since for the value of the f_{LO} in Eq. this condition is already met, it can be used without concern about the loop stability.

Finally, the calculated value for *k* should be distributed among all gain stages in the loop to finalize the design. The contribution of the laser and MZI are already fixed by device design as it is given in Eq. (3.8). The integrator input is provided by the loop filter. Considering that the loop filter is implemented in 1.8V CMOS, the desired DC set-point for its output voltage to provide maximum swing is 0.9V. This voltage should be integrated to provide 0.2Vp-p ramp with 5.6µs duration:

$$k_{int} = \frac{0.2\text{V}/5.6\mu\text{s}}{0.9\text{V}} = 39.7\times10^3\ [s^{-1}] \tag{3.16}$$

From equations (3.8), (3.13), and (3.16) the transfer function of the loop filter and the charge pump, k_{LF-CP}, can be found:

$$T_{LF-CP}(s) = \frac{131\times(1 + s/\omega_z)}{s(1 + s/\omega_p)}\ [\text{kV/rad}] \tag{3.17}$$

In the next sections it will be shown that how these numbers translates into real values of the physical circuit elements.

3.3.2. EO-PLL noise analysis

The noise sources in EO-PLL can be divided in three categories: the laser phase noise, the photodetector shot noise, and the noise from electronic circuitry including 1/f Flicker and white thermal noise. By proper sizing and power consumption, the electronic circuits can be designed so that their noise becomes negligible compared to the fundamental laser phase noise and detector shot noise. Hence, in this section we will focus on analyzing the effect of these two fundamental noise sources and the noise analysis of the electronic circuits will be differed to the next sections to be discussed as part of their design criteria.

The phase noise of the laser has two main components, one from the spontaneous emission in the active region, and the other from the tuning process. The spontaneous emission can be modeled as a white frequency noise source that causes angle-random-walk and, hence, a Lorentzian laser spectrum. The tuning DBR section of the laser can be electronically modeled as a forward biased PN junction in series with a 40Ω resistance. In the linear region where the diode is on and the slope of the I-V curve is dominated by the 40Ω resistance, the conversion gain is 610GHz/V or equivalently 24.4 GHz/mA. The shot noise and thermal noise from the tuning section gets converted to the laser frequency noise with this gain. The bandwidth of the conversion due to the carrier life-time in the PN junction is limited to 60MHz; however,

it can be shown that for the purpose of this analysis the effect of limited bandwidth is negligible and the contribution of the tuning noise can also be modeled as white frequency noise similar to the effect of spontaneous emission. The noise from the spontaneous emission and the tuning process are uncorrelated and can be added to find the total frequency noise of the laser.

In this analysis we are interested in the phase noise of the beat signal from interference of the two delayed versions of the laser light detected by the photodiode. This can be found by passing the total laser frequency noise (f_n^2) and also the phase noise induced by the detector shot noise (φ_n^2) through the transfer functions of the EO-PLL as shown in *Figure 12*. In this figure the blocks associated with the switching control that have no impact on the noise analysis are not included and all other blocks are modeled with linear transfer functions.

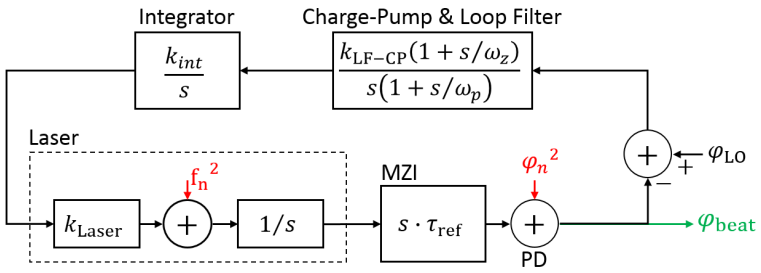

Figure 12: Block diagram of the linear transfer function of EO-PLL elements and its dominant noise sources

The values of the parameters in the transfer function were found in previous section. In order to find the output phase noise spectrum we need to find the values of f_n^2 and φ_n^2. The first component of f_n^2 comes from the spontaneous emission of the laser. The linewidth associated with spontaneous emission of the laser is about 5MHz and hence:

$$f_{n,spe}{}^2 = \frac{\Delta\nu_{spe}}{2\pi} \cong 8\times10^5 \ [\mathrm{Hz^2/Hz}] \tag{3.18}$$

The second component of f_n^2 is from tuning process. The bias current of the tuning section is about 12.5mA. With this bias the current noise density will be:

$$i_{n,tune}{}^2 = 2qI_B + \frac{4kT}{R} = 4.4\times10^{-21} \ [\mathrm{A^2/Hz}] \tag{3.19}$$

Considering the conversion gain of G=24.4 GHz/mA we will have:

$$f_{n,tune}{}^2 = i_{n,tune}{}^2\times G^2 \cong 2.63\times10^6 \ [\mathrm{Hz^2/Hz}] \tag{3.20}$$

The total white frequency noise density would then be:

$$f_n{}^2 = f_{n,spe}{}^2 + f_{n,tune}{}^2 = 3.43\times10^6 \ [\mathrm{Hz^2/Hz}] \tag{3.21}$$

This translates to a linewidth of $\Delta\nu = 2\pi\times f_n{}^2 = 21.5\mathrm{MHz}$. The Lorentzian spectrum as a result of this analysis and also the measured spectrum by a long (1μs) MZI are shown in *Figure 13*.

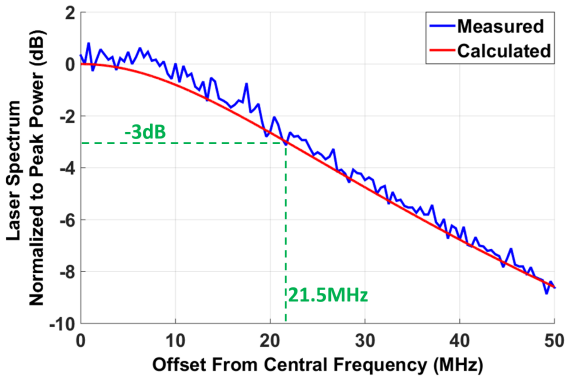

Figure 13: Calculated and measured spectrum of the laser with 10mA DBR bias current.

The second important noise component is ${\varphi_n}^2$ caused by the detector shot noise. The DC current in the detector is close to 50µA and the peak-to-peak value of the beat current is around 10µA. Hence, the resulted phase noise can be found as:

$$ {\varphi_n}^2 = \frac{2qI_{DC}}{{i_{rms}}^2} = 1.28\times10^{-12}\ [\mathrm{rad^2/Hz}] = -119\ [\mathrm{dBc/Hz}] \tag{3.22} $$

Considering the block diagram of the *Figure 12* and using the results from equations (3.21) and (3.22) we will have:

$$ \left|{\varphi_{\mathrm{n,beat}}}^2(s)\right| = {\varphi_n}^2 \times \left|\frac{1}{1+LG(s)}\right|^2 + {f_n}^2 \times \left|\frac{2\pi\cdot\tau_{\mathrm{ref}}}{1+LG(s)}\right|^2 $$

$$ \Rightarrow \left|{\varphi_{\mathrm{n,beat}}}^2(s)\right| = 1.47\times10^{-11}\times\left|\frac{1}{1+LG(s)}\right|^2\ [\mathrm{rad^2/Hz}] \tag{3.23} $$

Contrasting this result to Eq. (3.22) shows that the phase noise of the beat signal is clearly dominated by the laser phase noise and that it is shaped by the EO-PLL closed-loop gain.

The frequency noise spectrum based on zero-crossing measurement after filtering the beat signal with 7MHz single-side bandwidth around the 7.2MHz carrier can be found as given below:

$$ \left|{f_{\mathrm{n,beat}}}^2(s)\right| = \left|{\varphi_{\mathrm{n,beat}}}^2(s)\right| \left|\frac{f_{\mathrm{beat}}}{2\pi}\cdot\frac{\left(1-e^{-s/f_{\mathrm{beat}}}\right)}{1+s/\omega_{p,ss}}\right|^2\ [\mathrm{Hz^2/Hz}] \tag{3.24} $$

And hence, the RMS frequency noise will be:

$$ f_{\mathrm{n,beat,RMS}} = \sqrt{2\int_0^\infty \left|{f_{\mathrm{n,beat}}}^2(f)\right| df} = 14.5\ [\mathrm{kHz}] = 0.2\%\ [f_{\mathrm{beat}}] \tag{3.25} $$

In previous section it was indicated that reducing the nonlinearity by 30dB would suffice to bring it below the level of instantaneous fluctuations on the beat signal caused by laser phase noise. Further discussion

about that statement was differed to this section. According to *Figure 3***Error! Reference source not found.** the open-loop variation in beat frequency, or equivalently γ, due to the nonlinearity of the tuning characteristic is equal to 9% peak-to-peak or 3.2% RMS. Reducing this number by 30dB brings it down to 0.1% RMS which is below the amount of variation due to phase noise from Eq. (3.25). Hence, the statement from previous section is valid and by the proposed design the effect of nonlinearity will reduce to a negligible level compared to the effect of laser phase noise.

3.3.3. EO-PLL circuit blocks

In addition to system level design, the individual circuit blocks from *Figure 11* have direct impact on the EO-PLL performance. The TIA that converts the photocurrent into a voltage to derive the PFD, the integrator followed by a buffer to drive the laser tuning port, and the electronic PLL to generate the clock reference for gated switching operation are the most important circuit blocks that will be discussed in this section.

TIA

Ideally the beat photocurrent is a pure sinusoidal, but due to the wavelength dependent of the laser output power it experiences low-frequency baseline and amplitude variation as a result of triangular frequency modulation. For this reason the TIA should have bandpass transfer function to remove the slow baseline variation and high frequency noise components. It should also remove the low-frequency envelope, which can be done via a Schmitt-Trigger output stage. The circuit diagram of the TIA used in this design is shown in *Figure 14*.

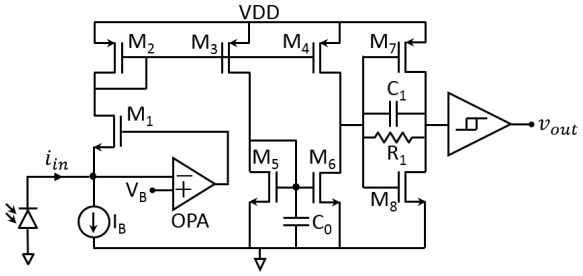

Figure 14: Circuit diagram of the trans-impedance amplifier (TIA)

The TIA of *Figure 14* employs a common-gate input stage, M_1, along with a gm-boosting amplifier, OPA. This configuration has a few features that makes it suitable for this particular design. Firstly, due to the fabrication imperfections, the PDs on the silicon-photonic chip should be biased below 300mV to limit their dark current to a level that doesn't saturate the input stage of the TIA. This can be done by setting $V_B = 300mV$ without any negative impact on the operation of input transistor M_1. Secondly, the gm-boosting amplifier reduces the input impedance of the TIA proportional to its voltage gain, which relaxes the required gm from M_1, hence reduces its power consumption and current noise. Finally, the current noise of M_1 that is small to begin with, experiences a very low impedance at the source of M_1, thus circulates within its own channel and has nearly no contribution to the output noise of the TIA. Hence, with this configuration the photocurrent is fully collected from the detector with a noise factor close to 1.

The current from M_1 then flows into M_2 and is mirrored and high-pass filtered with the combination of M_3 to M_6 to remove the baseline variation. The output current from this stage is low-pass filtered and

converted to a voltage through R_1 in parallel with C_1. Finally, a Schmitt-Trigger stage removes the amplitude envelope and send the square wave to the PFD.

The noise of this TIA is dominated by the transistors M_2 to M_4. Considering that, similar to the detector shot noise, the noise from the TIA will be shaped by the EO-PLL, the resulted input referred phase noise on the beat signal due to the transistors M_2 to M_4 will have the following form:

$$\left|\varphi_{\mathrm{n,beat}}{}^2(s)\right| = \frac{3\times\left(4k_BTg_m + {i_{n,F}}^2(s)\right)}{{i_{s,\mathrm{rms}}}^2}\times\left|\frac{1}{1+LG(s)}\right|^2 \tag{3.26}$$

In this equation gm is the trans-conductance of the transistors M_2 to M_4 and ${i_{n,F}}^2(s)$ is their Flicker noise current. The gm of these transistors is desired to be small for lower thermal noise, however this requires decreasing the size of transistors to maintain the bandwidth, which in return increases the Flicker noise. As a result gm is chosen equal 1.6mS which allows increasing the size of the transistors enough to push the corner frequency of the Flicker noise below the EO-PLL bandwidth (700 kHz). Under this condition the Flicker noise will be suppressed by the EO-PLL and its contribution to the beat phase noise will be negligible. Thus, Eq. (3.26) can be reduced to the following form:

$$\left|\varphi_{\mathrm{n,beat}}{}^2(s)\right| = 6.36\times10^{-12}\times\left|\frac{1}{1+LG(s)}\right|^2 [\mathrm{rad}^2/\mathrm{Hz}] \tag{3.27}$$

The level of phase noise in this equation is less than half of the phase noise contribution from the laser given in Eq. (3.23). Thus, effect of the TIA noise on the EO-PLL performance is negligible.

Integrator

The other important block that can limit the EO-PLL performance if not designed carefully are the integrator. In order to have a reference for the acceptable noise level for the integrator we can refer the frequency noise density of the laser from Eq. (3.21) to its tuning port and find equivalent voltage noise level that can cause the calculated frequency noise. Using the conversion gain of 610GHz/V we will have:

$${v_{n,t}}^2 = \frac{{f_n}^2}{{k_{laser}}^2} = \frac{3.43\times10^6\ [\mathrm{Hz}^2/\mathrm{Hz}]}{(610\ [\mathrm{GHz/V}])^2} = 9.2\ [\mathrm{nV}^2/\mathrm{Hz}] \tag{3.28}$$

Hence, the noise on the tuning voltage from the integrator and the buffer should be smaller than this value to be considered negligible compared to the inherent frequency noise of the laser.

The integrator can be modeled with a simplified circuit shown in *Figure 15*. The circuit is essentially a charge pump where the value of its current is set be the output voltage of the loop-filter and a switching signal, SW, changes the direction of integration to generate the triangular pattern. Considering the sizing of the transistors M1 to M5, the main contribution of the noise is from M_3 and M_5. At each moment the integrator can be modeled with the equivalent circuit on the right side of the figure where g_m is the small signal conductance of the transistor providing the current (M_3 or M_5) and V_{ov} is the overdrive voltage of that transistor.

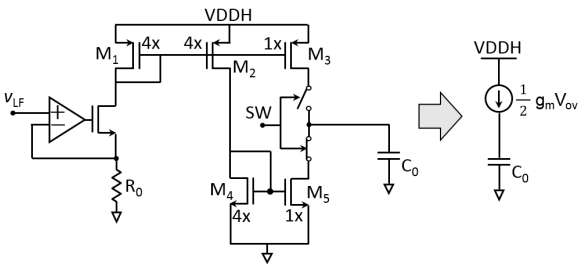

Figure 15: Circuit diagram of the integrator.

In order to get 0.2V/5.6µs we should have:

$$\frac{\frac{1}{2}g_m V_{ov}}{C_0} = \frac{0.2\ [\mathrm{V}]}{5.6\ [\mu s]} \Longrightarrow \frac{g_m V_{ov}}{C_0} = 36\ [\mathrm{mV/\mu s}] \tag{3.29}$$

The spectrum of the integrator noise in an open-loop configuration will have a $1/f^2$ characteristic due to the integration effect. Hence, it is important to make sure that the noise density is lower than the value specified by Eq. (3.28) at low frequencies. Since the noise of the integrator will also be shaped by the loop-gain of the EO-PLL, we just need to ensure that the noise is low enough at the frequency equal to the *zero* of the loop-filter (235 kHz) to get second-order shaping on the integrated noise. Hence we should have:

$$\frac{4k_B T g_m}{(2\pi \times 235\ \mathrm{kHz} \times C_0)^2} < 9.2\ [\mathrm{nV^2/Hz}] \tag{3.30}$$

Assuming $V_{ov} \approx 0.2\ V$ and by using the result of Eq. (3.29)in Eq. (3.30) we will have:

$$C_0 > 148\ [\mathrm{pF}] \tag{3.31}$$

As it is expected, this result tells that in order to improve the noise performance of the integrator the value of its capacitance should increase. Furthermore, in order to maintain the desired gain the value of its current, and thus power consumption, should increase as well. The amount of current needed to charge this capacitance is at 0.2V/5.6µs rate is equal to 5.3µA.

Electronic PLL

The last important circuit block that needs to be discussed is the electronic PLL. The architecture of the electronic PLL was given in *Figure 10*. At this point we know that its reference frequency LO should be equal to 7.2MHz, but we still need to calculate the required values for number of its phases, M, and its frequency multiplication factor, N. From the explanation in section 3.2 we know that the electronic PLL will provide a quantization step equal to the period of the beat signal divided by $\mathrm{M}\times\mathrm{N}$. This timing resolution will be used to determine the error in the beat signal period after switching and also will be used to fine-tune the switching time to reduce this error. From Eq. (3.25) it can be seen that the random error caused by the laser phase noise on the frequency/period of the beat signal is equal to 0.2%. Hence, by setting the ½LSB of the quantization step to a value lower than 0.2% of the period of beat signal will suffice:

$$\frac{1}{2}\frac{1}{M \times N} < 0.2\% \Longrightarrow M \times N > 125 \tag{3.32}$$

It is more convenient to set $M \times N = 128$ to have an integer number of quantization bits (i.e. $2^7 = 128$). M and N can take many different numbers to satisfy this condition, but based on experience a good design choice will be $M = 8$ and $N = 32$. The eight phases can be provided by a VCO with four differential stages, and the frequency multiplication can be accomplished with 5-stage TFF-based frequency-divider in the feedback of the PLL.

3.4. EO-PLL implementation and test results

As it was mentioned in previous section, the MZI and the photodiode of the EO-PLL are implemented on the silicon-photonic chip and all its electronic circuitry are on a 0.18µm CMOS chip. The TSV interconnects carry the photocurrent from the silicon-photonic chip to the TIA on the CMOS chip.

In order to test the effect of the EO-PLL on the modulation linearity, the beat frequency at the output of the reference MZI is compared for the open-loop and closed-loop laser tuning in *Figure 16*. As it can be seen, the fluctuation in the beat frequency is reduced to values lower than the frequency noise induced by the laser phase noise.

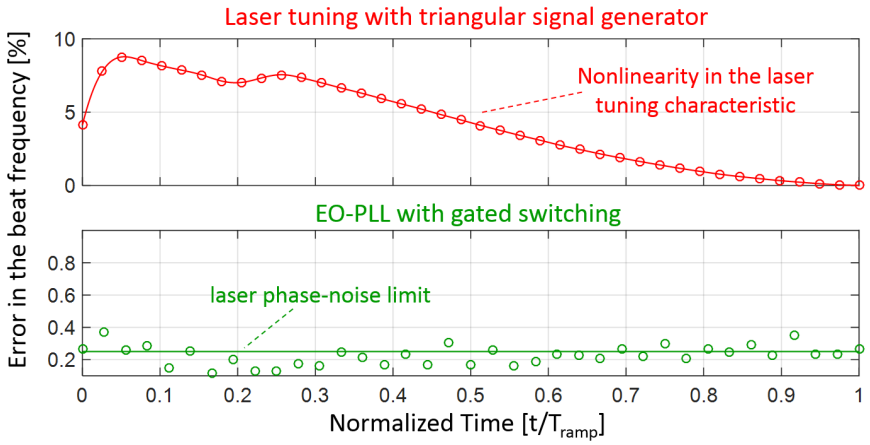

Figure 16: Measured beat frequency within one ramp period.

The ramp-to-tamp stability of the EO-PLL is tested by plotting the histogram of the average beat signal over one ramp for 100 successive ramps as given in *Figure 17*.

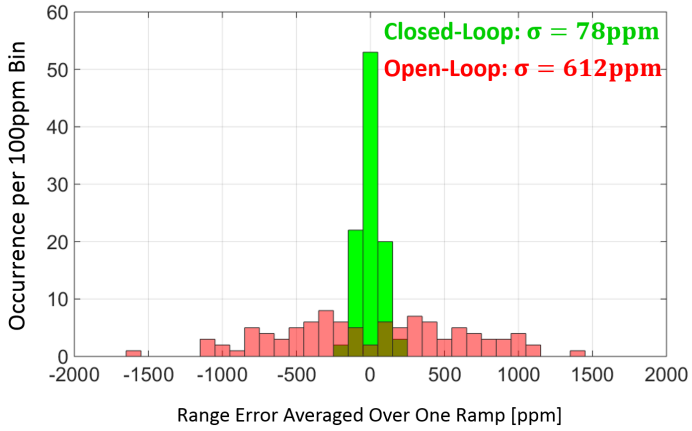

Figure 17: Distribution of the error in average beat frequency for 100 successive modulation ramps.

This plot clearly confirms the effectiveness of the EO-PLL in stabilizing the modulation characteristic of the laser and, thus, the measured beat frequency.

4. Tunable VCSEL

In this section, we report a tunable VCSEL directly integrated on SOI. High-contrast grating (HCG) mirror, the bottom mirror of the VCSEL, is directly fabricated on the SOI. The tunable VCSEL is achieved by etching the buried-oxide layer in HF vapor and releasing the silicon HCG, as shown in the schematic in Figure 18. The MEMS structure in Figure 19 consists of 15 µm-long and 1 µm-wide beams across a four-anchor suspended frame that is 450 nm thick (Si device layer). The buried oxide layer (BOX) is 1 µm thick. The HCG reflector pictured is 16 µm x 16 µm, including the frame, and has an HCG with a period of 650 nm with a 50.77% duty cycle.

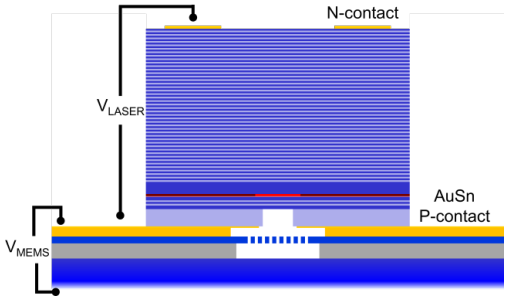

Figure 18: Schematic of tunable Si HCG VCSEL.

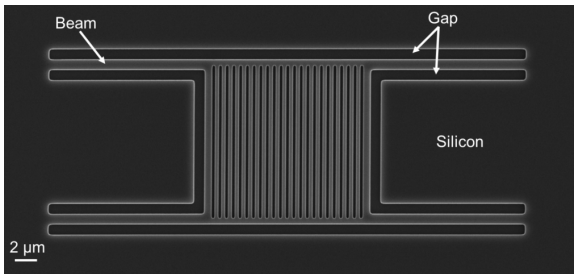

Figure 19: SEM of suspended HCG.

4.1.1. Electrostatic actuator modeling

The actuator can be modeled as a parallel plate capacitor. This well-known system has a pull-in condition that can be described by the voltage V:

$$V < \sqrt{\left(\frac{2}{3}d_0\right)^3 \frac{k}{\varepsilon A}} = \sqrt{\frac{8}{27}d_0^{\,3}\frac{k}{\varepsilon A}} \simeq 0.544\sqrt{d_0^{\,3}\frac{k}{\varepsilon A}} \qquad (4.1)$$

Where d_0 is the initial gap distance (the BOX layer thickness), k is the spring constant of the actuator, A is the area, and ε is the permittivity of free space. Using the model described by Mateus et al. (*Sensors Actuators A Phys. 119, 2005*), the spring constant of a 4-beam actuator can be described by:

$$k = 32Y\left(\frac{t}{L}\right)^3 w \qquad (4.2)$$

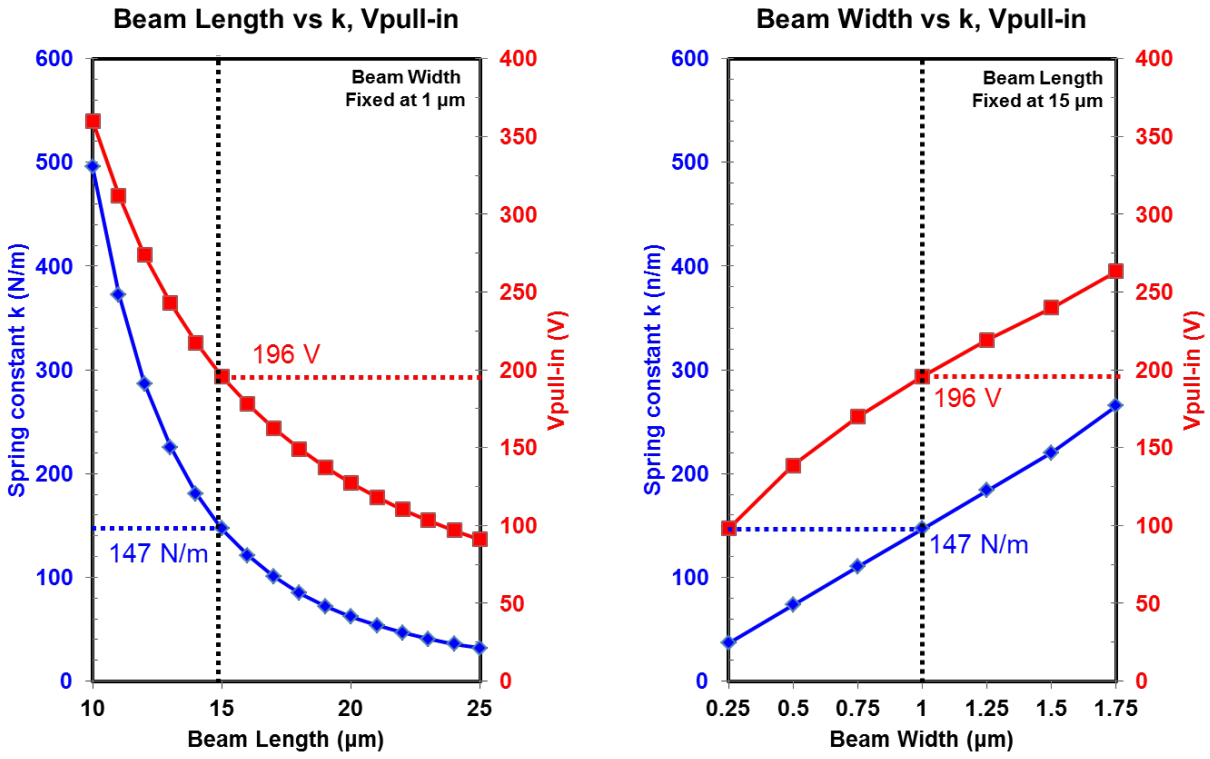

Figure 20 Beam length vs spring constant, k, and pull-in voltage maintaining a fixed beam width of 1 µm. Beam width versus spring constant, k, and pull-in voltage, maintaining a fixed beam length of 15 µm.

Where *Y* is the Young's modulus of the membrane material, *t* is the thickness of the membrane, *L* is the length of the spring arm, and *w* is the width of the beam. For the silicon HCG from Figure 19, we have:

$$k = 32 * 0.170 \times 10^{12} \left[N/m^2 \right] \left(\frac{450 \times 10^{-9} [m]}{15 \times 10^{-6} [m]} \right)^3 * 1 \times 10^{-6} [m] = 146 \left[N/m \right] \qquad (4.3)$$

Applying the result from (4.3) into Eq. (4.1) provides a pull-in voltage of 196 volts. A series of calculated spring constants and pull-in voltages for various actuator designs is shown in Figure 20 and Figure 21.

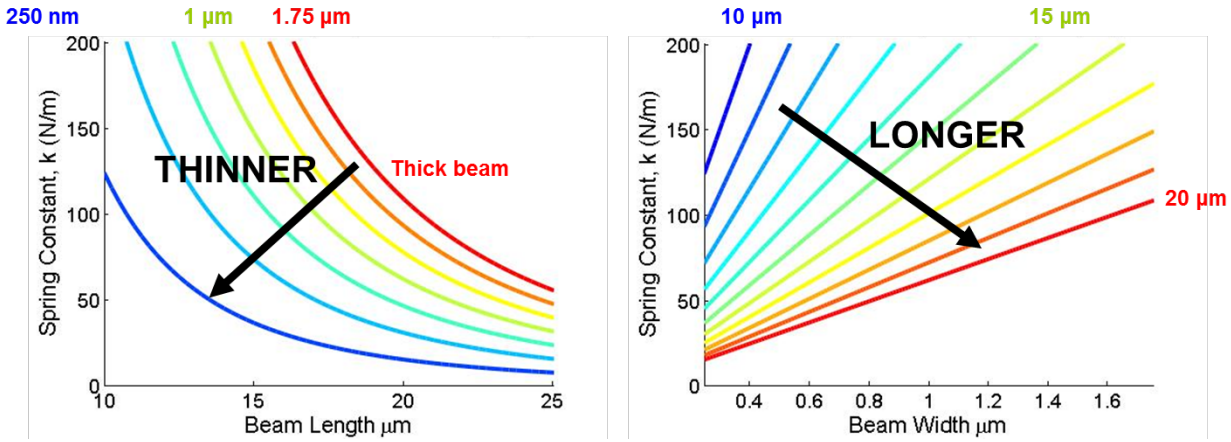

Figure 21 Family of curves of spring constant k for (a) variety of beam widths, and (b) variety of beam lengths.

With a known spring constant, k, and bias voltage V, we can use an electrostatic-spring equilibrium condition to determine the actuator displacement:

$$F = kz - \frac{1}{2}\frac{\varepsilon A}{(d_0 - z)^2}V^2 = 0 \tag{4.4}$$

$$kz = \frac{1}{2}\frac{\varepsilon A}{(d_0 - z)^2}V^2 \tag{4.5}$$

For our structure, a 25:1 nm tuning efficiency is expected from FDTD simulations. In the previous report, we measured displacements up to 400 nm, which would account up to 18 nm in wavelength tuning. Using Equation (4.5), here we show the calculated values for a stiff spring constant of 147 N/m.

Table 4.1 Calculated actuator displacement versus voltage.

Tuning Bias Voltage	Expected Displacement	Expected Tuning
10	0.7 nm	28 pm
20	3.1 nm	124 pm
30	7.0 nm	280 pm
40	12.7 nm	508 pm
50	20.1 nm	804 pm
60	29.5 nm	1180 pm

4.1.2. VCSEL tuning results

Figure 22 shows preliminary light-current-voltage (LIV) characteristic of a VCSEL with CW operation with >0.3 mW CW power out-coupled from the semiconductor DBR at 15 ºC. The device temperature is controlled with a thermo-electric cooler on a copper chuck. A Keithley current source is used to bias the VCSEL via electrical probing. Light is collected by a large-area germanium photodetector placed above the

VCSEL. The VCSELs exhibit thermal rollover with increasing current bias due to gain spectrum red-shifting more rapidly than the resonant cavity spectrum, an effect typical in VCSELs. The device threshold current i_{th} is 2.3 mA, substantially lower than fixed wavelength HCG VCSELs. This is attributed to the higher index contrast of the released reflector. The ripples on the LI curve are due to residue reflection from the back of the silicon substrate/air interface, as verified by the output spectra measured at various currents corresponding to the peaks and valleys of the L-I curve and the substrate thickness. The L-I ripples can be eliminated with backside roughening of the substrate.

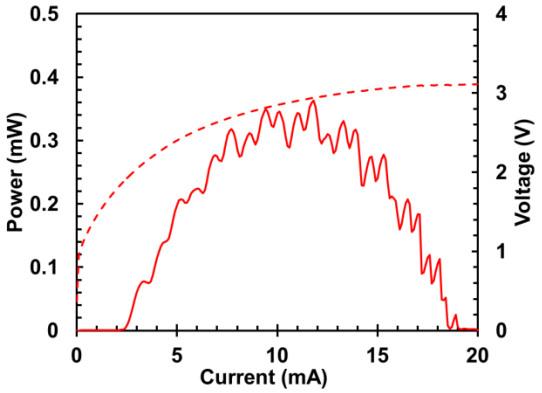

Figure 22 CW LIV of Si HCG VCSEL with suspended HCG from 0 to 20 mA. Threshold current is 2.3 mA, and peak CW power is 0.36 mW at 11.8 mA forward injection current. Light is collected with a large-area Ge photodiode for the LI measurement.

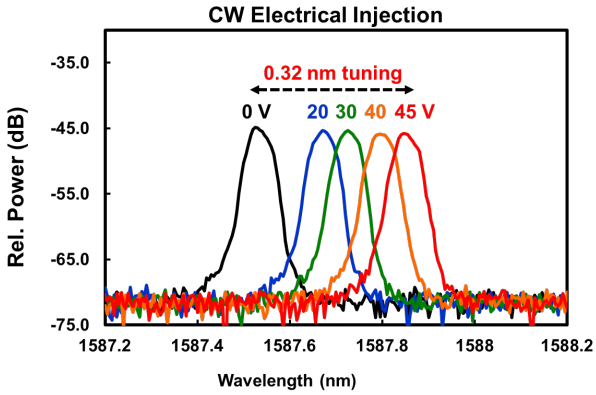

Figure 23 Spectrum of Si HCG VCSEL at different V_{MEMS} bias voltages, ranging from 0 to 45 V. Wavelength peaks are recorded to measure shift for varying V_{MEMS} bias.

Furthermore, a secondary voltage source (V_{MEMS}) is used to actuate the suspended Si HCG to perform wavelength tuning of the VCSEL. A voltage sweep from 0 to 45 V provides 0.32 nm of wavelength tuning, shown in Figure 23. The tuning efficiency can be improved in at least two ways: (i) by reducing the actuator spring constant with narrower, longer, and thinner beams to a target of 15 [N/m]; and (ii) by redesigning the contact scheme and addressing *individual* VCSELs with an applied tuning bias. In our current contact scheme, the MEMS actuators are addressed as an ensemble across the entire chip. As a result, many shunt paths exist along the contact plane of the SOI and the backside of the device reducing the actual tuning voltage across the actuator. The applied tuning bias has to overcome an ensemble parasitic resistance to actuate a single VCSEL. Although we applied the same bias from the actuator experiment described in the Q4 report (400 nm HCG displacement), the applied voltages seen in Figure 23 are not directly across the tuning junction. Thus, the tuning efficiency can also be improved by reducing the parasitic resistance of an ensemble actuation.

5. 3D Integration

This section reports on the 3D Integration between Silicon Photonics and CMOS using a Cu/Sn bonding process. The Cu/Sn bumps on the backside of the silicon photonics wafer are matching the pattern on the CMOS wafer. CMOS metallization in MPW runs is commonly Aluminum. In order to obtain a compatible material for bonding deposited on the wirebond pads of small CMOS dies as obtained from a MPW run, we work with CVInc Packaging Solutions (Richardson, TX). We used two different under bump metallizations (UBM) on the Aluminum wirebond pads: A Cu deposit and an Au deposit. Cu is the material compatible with CMOS process and would allow for wafer scale integration, while electroless gold deposition was used for ease of processing. Figure 24 shows an example of a CMOS die with selective electroless copper deposition on the aluminum wirebond pads.

The mask layout of the silicon photonics chips is shown in Figure 25. The layout includes 4 areas: (1) and (2) are two variants of the full photonics circuits for the LADAR source, (3) a dedicated area for calibration of losses in waveguides, couplers, splitters and of the MZI frequency response, and (4) an area dedicated for Ge photodiode characterization structures. While (1) and (2) are matched to fit the TSMC CMOS, (3) and (4) are matched to the previous CMOS layout, which allowed bond recipe development.

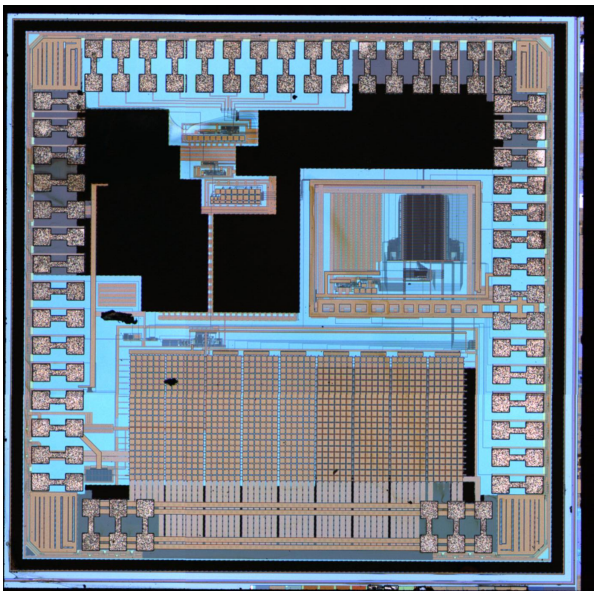

Figure 24: Overview of a MPW CMOS die after electroless copper deposition. The deposit is selectively applied on the Aluminum wirebond pads. The pads are matching the silicon photonics layout No.1 and No.2 in Figure 25.

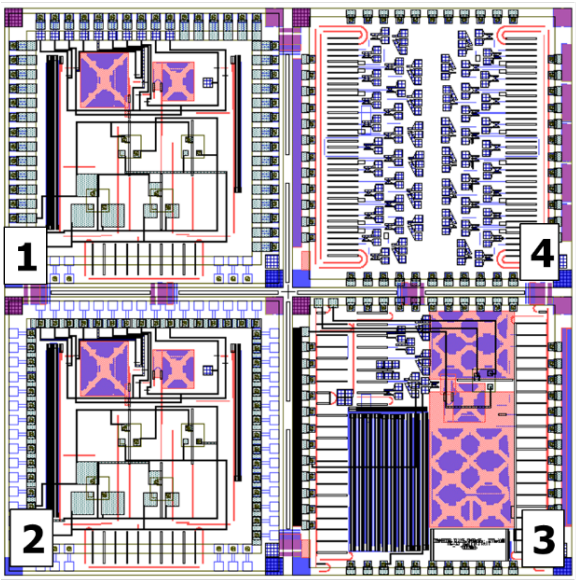

Figure 25: Full field layout, including 4 dies with a size of 3.1mm x 3.1mm each. 1) and 2) include full E-PHI circuitry, while dies 3 and 4 are reserved for silicon photonics passives calibration and photodiode test structures

5.1. Bond Bump Characterization

Four Silicon Photonics Wafers were fabricated at UC Berkeley. The TSV filling, planarization and Cu deposition were performed at RTI. In the previous report, we showed verification of photodiode and silicon photonics functionality after processing. In the past quarter, we performed intensive

characterization of the bond bumps. We observed wafer-to-wafer variation as well as die-to-die variation on a single wafer.

The wafer-to-wafer variation of the bond bumps was manifested in varying bond bump quality. 2 Wafers presented good bond bump quality, while two wafers presented bond bump degradation, as shown in Figure 26. Only dies from Wafer 2 and Wafer 3 have successful bonding. It is suspected, that the electroplating process in Wafer 1 and Wafer 4 was not successful.

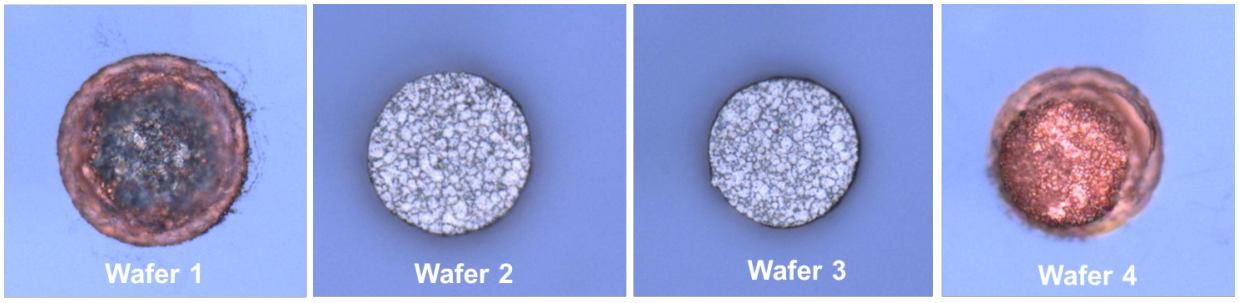

Figure 26: Wafer-to-wafer variation of the bond bump deposit. Each microscope image shows a single bond bump that is representative for the majority of bond bumps on the respective wafer. Wafer 1 and 4 contained non-succesful bond bump deposition, while wafers 2 and 3 contain successfully deposited bond bumps.

All wafers also showed some die-to-die variation. A first variation is the amount of TSV revealed. This can be attributed to a tapering in the deep trench etch process and in wafer thickness variation after grinding/polishing. These variations can be mitigated by adjusting the TSV etch, the size of the bond bump, and by adjusting the amount of grinding/polishing, adjusting the final thickness of the TSV. Figure 27 shows the typical of a successful bond bump candidate for bonding. The microscope image shows that the TSV is revealed by a typical red Cu color. The height measurement in the same image reveals, that the Cu-TSV is slightly lower than the Si backside surface, forming a moat type structure around the bond bump. Typically, this moat is a few hundreds of nanometer deep. Additionally a 'dishing' phenomenon has been observed, lowering the center of the bond bump compared to the outer edge of the bond bump. For well-deposited bond bumps, we measured 2.0 – 2.5 micrometers for the edge height, with a dish center typically a few hundreds of nanometers lower. The uniformity is typically better than 100nm over a single die, which is well suited for flip chip bonding.

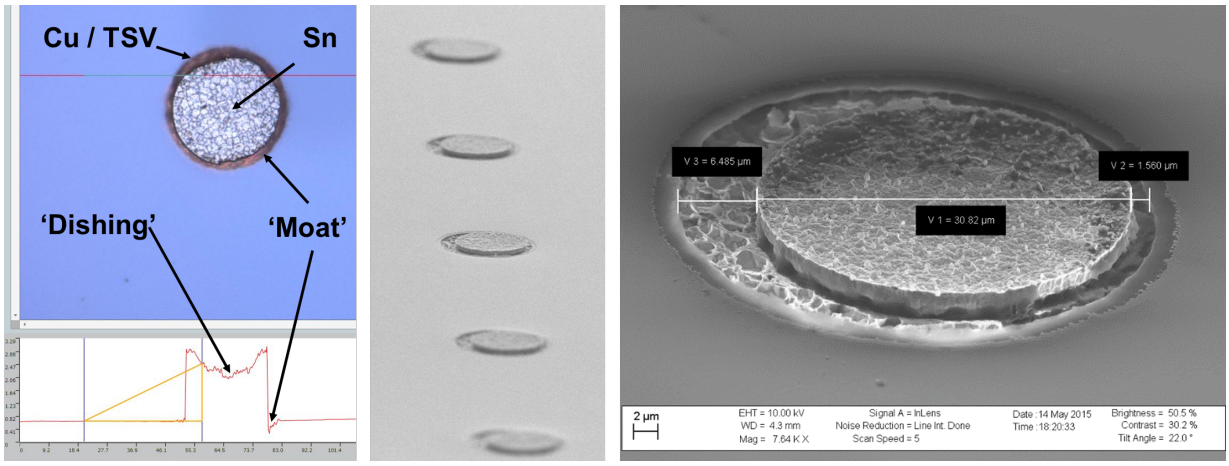

Figure 27: Measurements and SEM images on a typical bond bump on wafer three. A typical dishing of the bump in the center can be observed, as well as a moat around the bond bump. The profile measurement and the tilted SEM images show the 3D structure of the bond bump and the good alignment above the TSVs.

5.2. Under-Bump-Metallization

Two types of UBM deposits were performed in collaboration with CVinc on the CMOS bond pads, to allow for bonding: electroless Cu (30 dies) and Au (10 dies). Figure 28 shows a detail SEM view of an Au deposit, while Figure 29 shows the result of a Cu deposit. Uniform thickness of the Au was obtained over all dies. For this particular run, the deposited Au reached a level 1.7um below the highest feature on the CMOS die. Thicker deposits can be obtained. For eCu, copper deposits about 3um above the surface were obtained. Both processes showed, that selective deposition on the Al pads with sufficient thickness for bonding can be obtained. It is to be noted, the electroless deposition method was chosen due to the die size of the CMOS dies obtained from the MPW run. It is understood, that the deposition can more easily be done on wafer level with standard lithography and metallization processes.

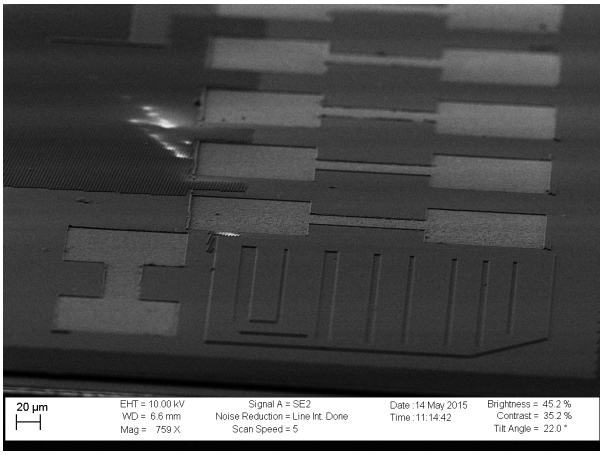

Figure 28: SEM image of a CMOS die with electroless Au deposit on the wirebond pads.

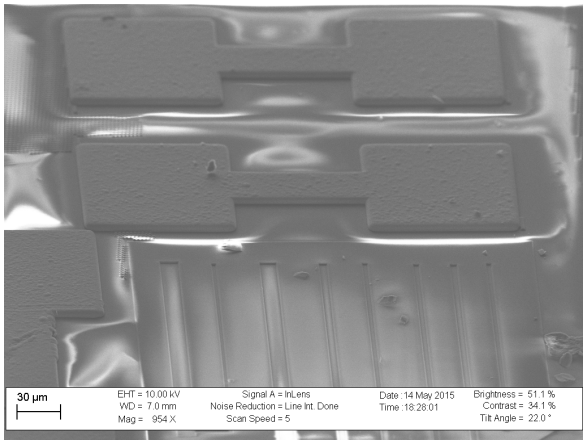

Figure 29: SEM image of a CMOS die with electroless Cu deposit on the wirebond pads.

5.3. Bonding Process and Verification Procedure

The silicon photonics and the CMOS dies were flip-chip bonded using a finetech fineplacer lambda. A photograph showing the top views of the two dies side by side is shown in Figure 30. The two dies have matching size of 3.1mm x 3.1mm, with a thickness of 200um for the Silicon Photonics and 300um for the CMOS respectively. Figure 31 shows the overlay image of the backside of the Silicon Photonics die and the top side of the CMOS die. The only features on the Silicon Photonics die being the bond bumps, they are visible as dark circles, placed above the square bond pads on the CMOS die. The patterns are well matched and good alignment is achieved.

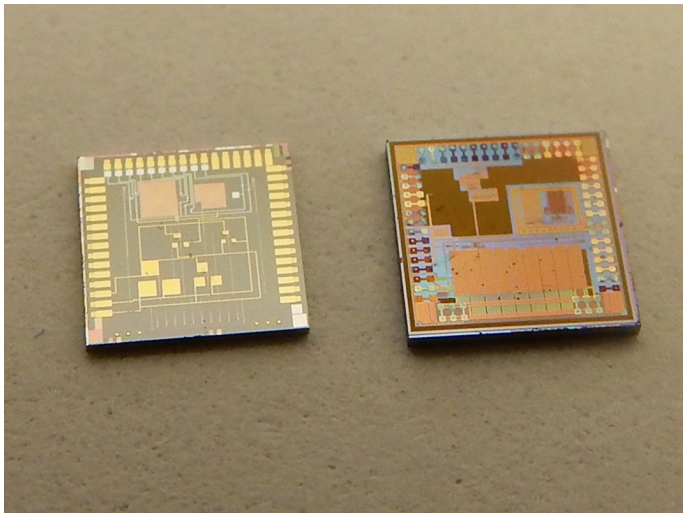

Figure 30: Photograph of the silicon photonics die (left) and the CMOS die (right). Both dies are showing the top side with the matching wirebond pad patterns for electrical interface.

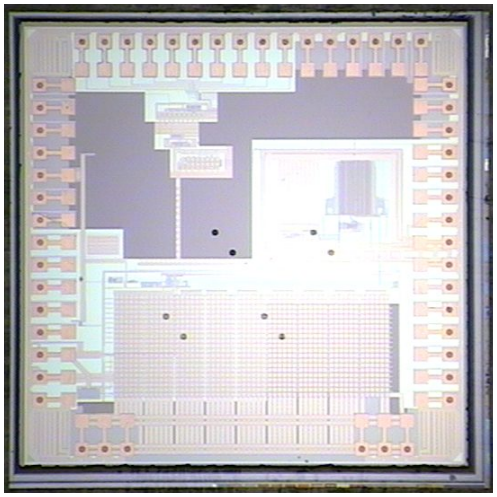

Figure 31: Overlay image of the bottom side of the silicon photonics die (dark circles are bond bumps) and CMOS top side (with circuitry and bond pads visible). Picture taken in the flip chip bonder during alignment procedure, just prior to bonding.

The bonding process was adjusted to the silicon photonic and CMOS dies. A recipe using 300°C for 30s at 20N applied on the chip surface during bonding yielded good results. In order to obtain successful bonding for Cu UBM, native surface oxide on the Cu pads was removed by wet etch and forming gas was flown during the bonding process. A tilted cross section SEM of the bonded stack is shown in Figure 32, showing the top Silicon Photonics layer above the CMOS, while the cross section SEM in Figure 33 reveals the alignment, contact and height of Silicon Photonics and CMOS.

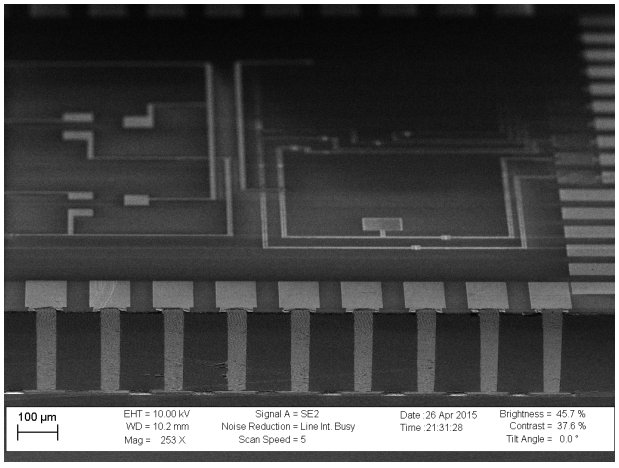

Figure 32: Tilted view of a bonded and diced pair of silicon photonics and CMOS dies, showing the cross section of TSVs and the patterning on the silicon photonics top die surface including routing layer and wirebond pads.

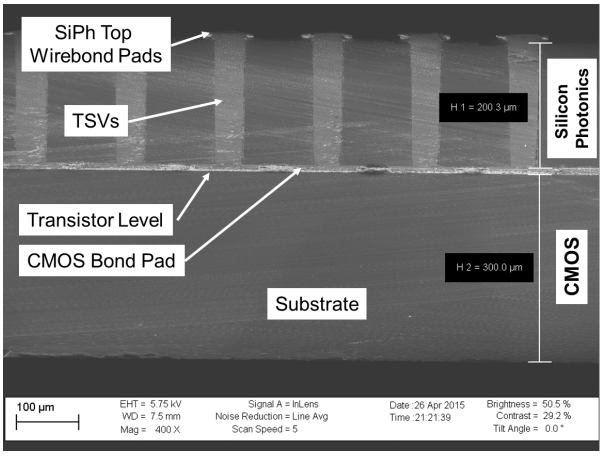

Figure 33: Cross section detail of the bonded pair. The cross section image show voidless filling of the TSVs and good alignment of the bond bumps above the CMOS bond pads. The total stack thickness is 500um.

5.3.1. Electrical: TSV conductivity

Electrical conductivity was tested in two steps. Immediately after bonding, 6 contact pairs were tested for electrical conductivity on a probe station. Each of these pairs was electrically shorted on the CMOS side. By probing the pairs from the top wirebond pad of the silicon photonics surface, the electrical conductivity of the TSV and bonding could be verified. Typically, this resistance was measured in the range of 100 mΩ. The successful bonding candidates were then die attached and wirebonded to one of our custom designed daughterboards. For extraction of the resistance without contact resistance, a four-point probe measurement was performed, according to the schematic in Figure 34b. Figure 35 shows a recorded IV curve of such a measurement with a total resistance of 180mOhm. This resistance includes 2 x wirebond on PCB + 2 x wirebond on Silicon Photonics pad + 2 x Bonding interface + 2 x TSV resistance + resistance on CMOS chip, which indicates, that the resistance of a single TSV is well below 100 mΩ.

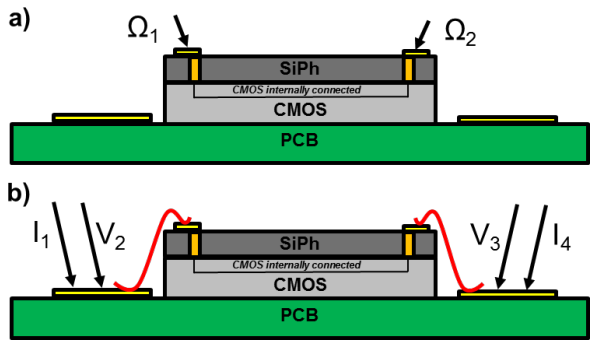

Figure 34: TSV conductivity measurement a) for short loop verification and b) four point probe measurement to extract resistance without probing contact resistance.

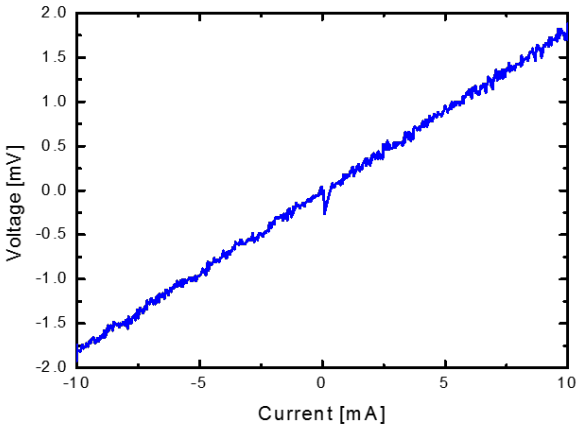

Figure 35: Four point probe measurement according to method shown in Figure 34. The total resistance measured on the PCB pads amounts to 180mOhm, indicating low resistance in the TSV.

5.3.2. Mechanical: Bond Shear Testing

The bond strength was measured using a Nordson Dage Bond Tester 4000. As the shear test is destructive, we performed the shear tests on bonded pairs that were only partially (or not at all) electrically connected. With 52 bond pads per die, die shear force up to 126g (gold under bump metallization (UBM)) and 49.1g (copper UBM) were measured. This indicates that good bond strength can be obtained, and it can be expected, that the bond strength is higher for fully working devices. After shear test, bond failure mode analysis was performed. The sheared surfaces for a pair using Au UBM are depicted in Figure 36. The inspection reveals, that various failure modes can occur on a single die. In the first depicted detail view, the bond bump was completely transferred to the CMOS die, and during shear test, a part of the silicon was removed from the silicon photonics die. This failure mode allows for two conclusions: first, the TSV in this particular die was not fully revealed, which is the probable cause that no electrical connection was obtained. Second, the bond strength is sufficient, that the shear test leads to rupture of the silicon rather

than separation of the bond bump from the gold interface, indicating very good bond strength. In the second depicted detail view, a second type of bond failure is obtained, were the bond bump only a negligible amount of material was transferred to the CMOS bond pad. The origin of this failure mechanism can possibly be attributed to local height variation, particle contamination or local temperature variation, all of which can be mitigated with additional process control.

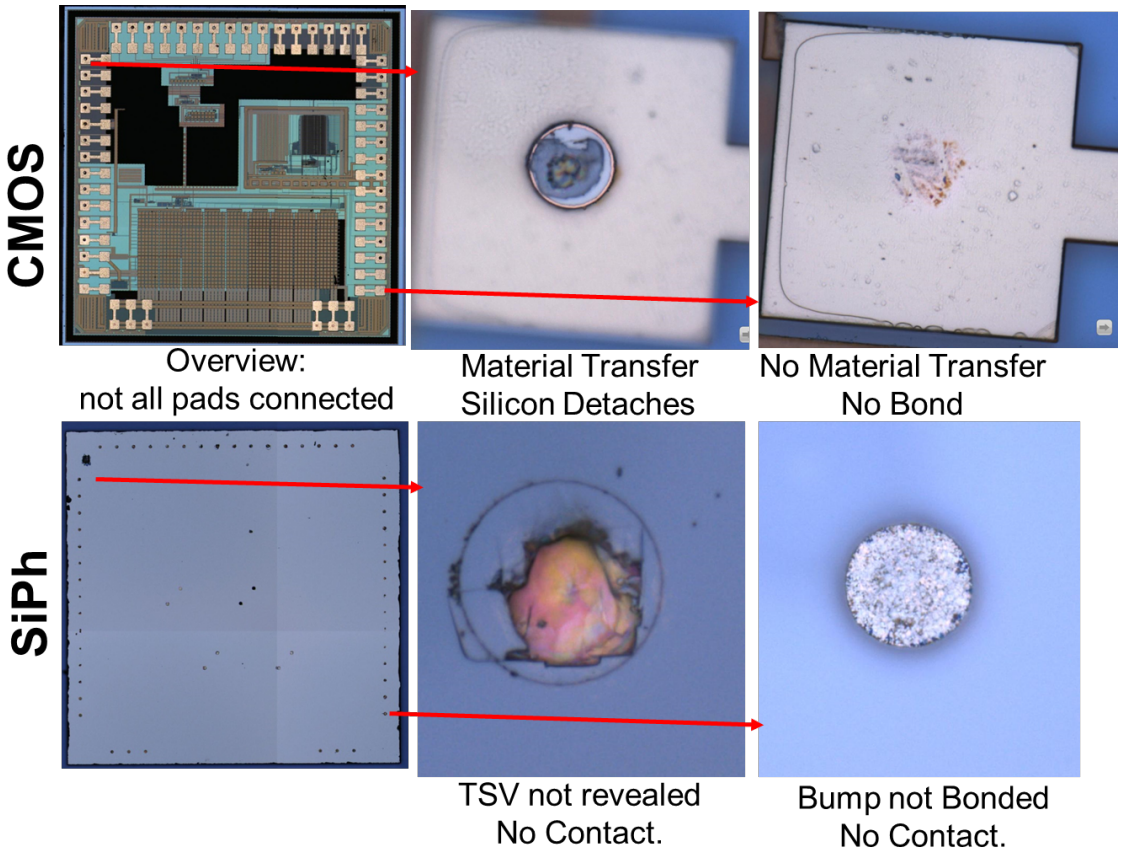

Figure 36: Bond failure mode analysis by microscope inspection after bond shear test. The top images show the CMOS die (with detail view of two bond pads) and the bottom images the Silicon Photonics die (with the corresponding detail views of two bond bumps) after separation of the two bonded dies.

5.4. 3D Integrated System

We fabricated a fully functional 3D integrated pair of Si-photonics and CMOS dies, using gold under bump metallization (UBM). A photograph of the 3D integrated system is shown in Figure 38. Optical interface to the photonics chip is achieved using on-chip grating couplers and a fiber array. Electrical interface between photonics chip photodiodes and CMOS electronics is achieved using through-silicon-vias, demonstrating pairwise functionality between the chips. The CMOS electronics are interfaced with FPGA programming, off-chip biases, and probe points by wirebonding to PCB. This system was used to characterize OPLL performance in Section 3, as well as ranging performance, covered in Section 6.

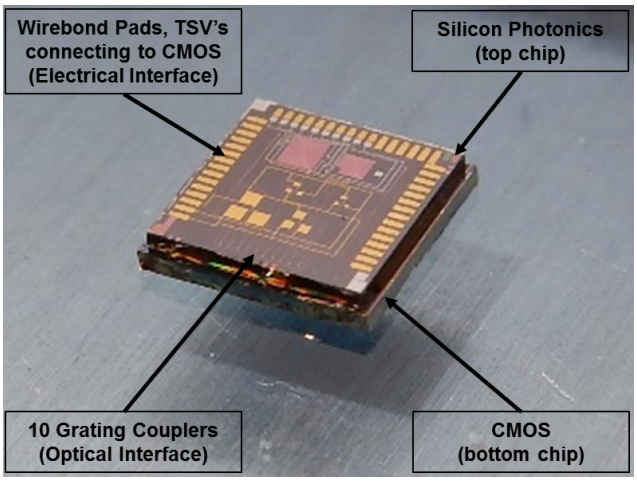

Figure 37: Fully 3D Integrated silicon photonics and CMOS system before electrical and optical interfacing.

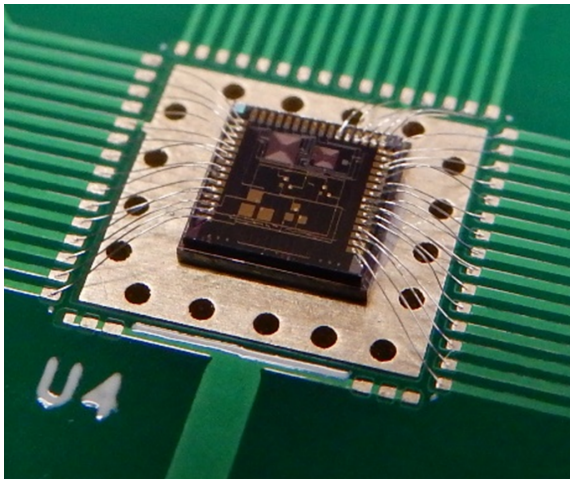

Figure 38: Fully 3D Integrated silicon photonics and CMOS including wirebonding to daughterboard.

6. Results – Integrated OPLL in FMCW Lidar

In this section, we report the performance of the integrated OPLL in FMCW configuration. Figure 39 illustrates the block diagram of ranging experiments using the integrated OPLL. Figure 40 shows a photo of the ranging setup used to obtain range-precision measurements and 3D images.

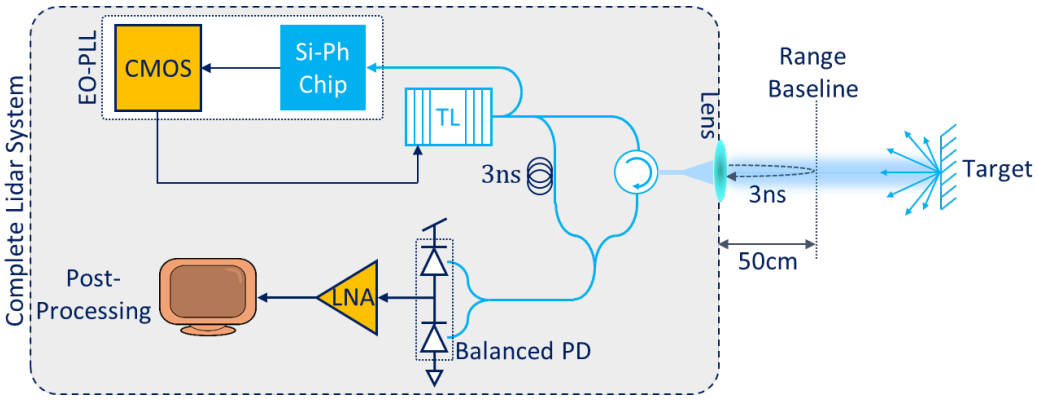

Figure 39: Block diagram of ranging experiments using integrated OPLL. Optical taps and single-mode fiber are used to emulate a lidar receiver.

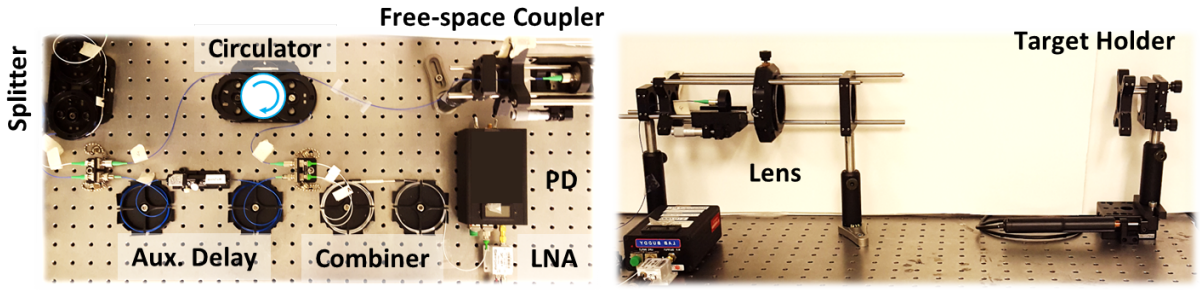

Figure 40: Photograph of free-space ranging setup. The optical chirp is focused onto a target at arbitrary standoff distances, and the target position is stepped to emulate single-beam rastering.

Under closed-loop configuration, the optical chirp is considered linear with chirp-rate, gamma. With a target that creates the long arm of an interferometer, the measured beat frequency at the output of the interferometer is proportional to the round-trip target distance (with some offset). We know gamma by design, so we can calculate absolute target distance simply by measuring target frequency.

We employ a post-processing method to obtain a frequency measurement for use in range acquisition. First, zero-crossing measurements of the sinusoidal trace are performed. Second, we find the average of all zero-crossing measurements for a single up- or down-ramp to obtain a single-ramp beat frequency estimate. We measure the accuracy of this estimate by calculating its standard deviation over many ramp periods. In order to achieve high range resolution, it is desired to average beat frequency estimates over several ramps, which contributes to acquisition time for a single pixel.

Several artifacts can have effects on these final beat frequency estimate, including optical chirp settling time, chirp slope inaccuracy (offsets in gamma from designed value), and chirp non-linearity (deviation of gamma from constant). We expect the ranging precision of the lidar system to scale with the locking precision of the OPLL, thus we expect to see improved lidar performance with closed-loop configuration over open-loop configuration.

We can perform several measurements regarding range precision using our system. In simple precision verification experiments, we can displace a cooperative target with micrometer accuracy, measuring target beat frequency for many successive ramps. For example, Figure 41 shows the target beat frequency for a target that is stepped with 200um increments. It is important to perform this experiment at several ranges in order to determine the phase noise-limited range of the system, since there is a tradeoff between range and range accuracy for FMCW systems. We perform these measurements at 5cm, 30cm, and 70cm range, illustrating two results: first, improvement of closed-loop ranging accuracy over open-loop accuracy; and second, a very high ranging precision of 4.4um at 5cm. These results are shown in Figure 42.

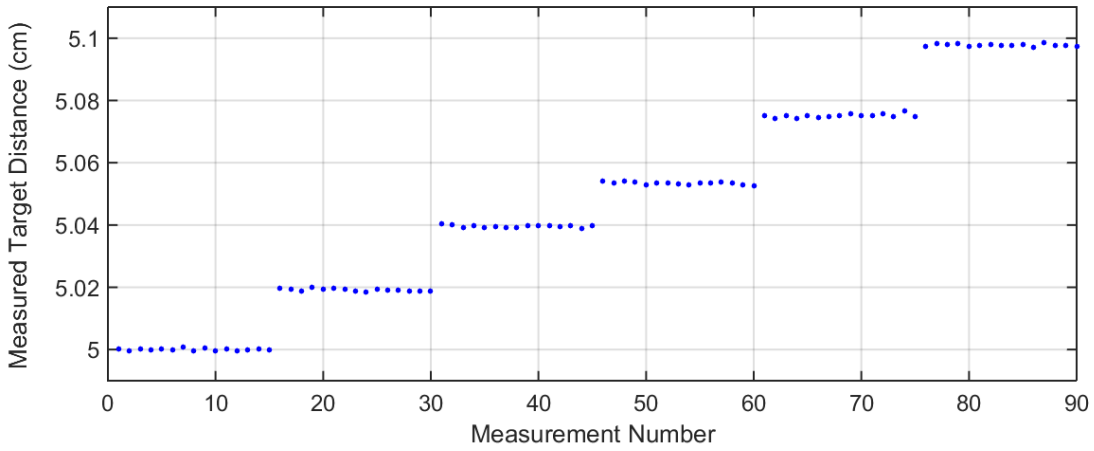

Figure 41: Average beat frequency per ramp over successive ramps, with target displacement at increments of 200 um. Target distance from baseline ~5cm.

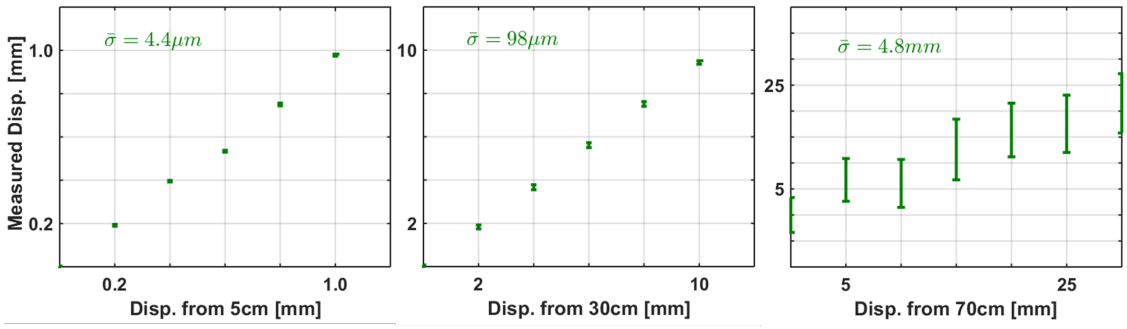

Figure 42: Range precision as a function of range and OPLL condition (open- or closed-loop).

Measurements in FMCW systems can be performed with different "baseline" distances because the interferometer beat frequency is related to the path *difference* between the two arms, and not the absolute length of the target arm. Effects of laser phase-noise are minimized when the path difference between the arms is zero, resulting in precise ranging measurements only limited by target SNR. In our imaging setup, we use a baseline delay of 3ns, equivalent to a 50cm baseline distance in free-space. Therefore, targets present at ~40cm and ~60cm will yield measured distances of 10cm and corresponding range precisions. The actual target distance is calculated after adding the baseline delay to the measured delay.

Finally, we demonstrate the use of this system in an imaging configuration, in which we used this system to obtain a three-dimensional image of a small (~1mm thick) gear. This image is shown in Figure 43. The image was taken at ~40cm standoff distance from the lens with 50cm baseline distance, and achieves ~11um precision, limited by the residual phase-noise in the chip-level OPLL. The data in Figure 43 represents data that is post-processed to map range to x-y position. This post-processing step can later be integrated into CMOS or PCB electronics.

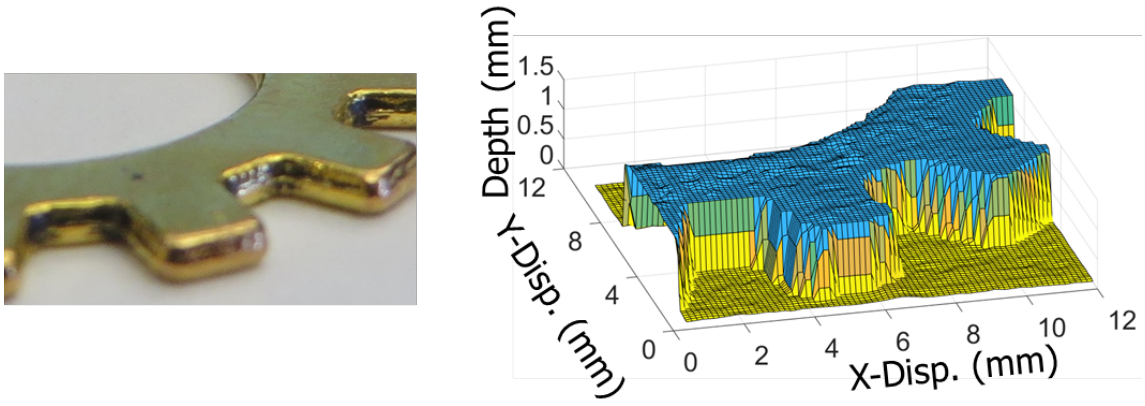

Figure 43: Photograph of 1.1mm thick gear (left) and a 3D image from a gear with 1.1mm thickness placed at 40cm distance from the imager taken with chip-level OPLL