ErAs epitaxial Ohmic contacts to InGaAs/InP

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We report epitaxial ErAs semimetal Ohmic contacts onto *n*-type $In_{0.53}Ga_{0.47}As$ grown on InP. The contacts were formed by molecular beam epitaxial growth of ErAs on InAs/InGaAs. Transmission line measurements showed minimum specific contact resistivities of $1.5 \pm 0.4\ \Omega\ \mu m^2$ (horizontal specific contact resistivity ρ_H, 4.20 $\Omega\ \mu m$) for the ErAs/InAs/InGaAs contact. The extracted contact resistance is larger than the true value because of the lateral oxidation of ErAs. The contacts degrade over time and at elevated temperatures because of the oxidation of the ErAs, making it difficult to use as surface contacts, but they are suitable as low-resistance buried contacts. © *2009 American Institute of Physics*. [DOI: 10.1063/1.3087313]

Low resistance metal-semiconductor Ohmic contacts play a significant role in all electronic and optoelectronic devices. Poor Ohmic contacts degrade the power efficiency through excess dc voltage drop and increase the *RC* delay of circuits. InGaAs is a widely used semiconductor in both high speed electronics and optoelectronic devices. So there exists strong motivation to develop reliable, low-resistance, Ohmic contacts to InGaAs. For both III–V heterojunction bipolar transistors (HBTs) and field effect transistors (FETs), an extremely low contact resistivity (ρ_c) of $\sim 1 \times 10^{-8}\ \Omega\ cm^2$ ($1\ \Omega\ \mu m^2$) is required to achieve simultaneous 1.5 THz f_t and f_{max}.[1,2]

The resistance of a metal-semiconductor contact depends on the energy barrier an electron sees when flowing from the metal to the semiconductor, or vice versa. Theoretically, a low resistance contact can be obtained by choosing a metal with a work function such that there is no barrier between the metal and the semiconductor. However in reality the typical metal/III–V (GaAs, InGaAs, and InP) interface contains many interface states that pin the Fermi level within the bandgap.[3] As a result there is always a barrier from metal to semiconductor independent of the contact metal. Also the interface states within the bandgap capture the electrons from the doped semiconductor, resulting in a depletion region. The contact resistance is determined both by the barrier height and the depletion width in the semiconductor. The electron transport is predominantly through quantum mechanical tunneling through the depletion region when either the barrier is small or the depletion region is narrow, common in Ohmic contacts. The contact resistance can be lowered by reducing the barrier height and/or decreasing the depletion width through increased doping.

Interface traps on a semiconductor can be caused by chemisorption of oxygen and other atmospheric elements on the surface, as well as the termination of the periodicity of the lattice itself.[4,5] They introduce energy states within the bandgap, depleting the underlying semiconductor in order to maintain charge neutrality. These surface states persist even after metal deposition on the semiconductor. Fermi level pinning from these surface states defines the barrier height and in conjunction with doping, the depletion width, thus increasing the contact resistance. Besides the chemical induced surface states, any physical damage to the semiconductor surface during device fabrication can increase the contact resistance by increasing the interface state density.

Highly degenerate doping of the semiconductor is generally required to promote low-resistance tunneling through the potential barrier at the interface. Previously, *n*-type *ex situ* contact resistivity of $0.5–2.7\ \Omega\ \mu m^2$ was reported by careful surface preparation before contact metal deposition.[6–8] However, *ex situ* contacts are sensitive to the exact details of the surface preparation and can show poor reproducibility. *In situ* formed contacts, where the contact metal is deposited immediately after semiconductor growth without breaking vacuum, give low contact resistance ($<1\ \Omega\ \mu m^2$) and show good repeatability.[9] Even an *in situ* formed metal-semiconductor interface will have surface states because of dangling bonds, vacancies, and metal induced gap states.[4] An epitaxial metal-semiconductor contact with a low barrier may be a "perfect" contact as it will have low interfacial defects. This could potentially be an extremely low resistance Ohmic contact.

Here we report *in situ*, ErAs epitaxial semimetal contacts to *n*-type $In_{0.53}Ga_{0.47}As$ that were prepared under ultrahigh vacuum (UHV) with molecular beam epitaxy (MBE). ErAs is a semimetal, thin layers of which can be grown epitaxially on InGaAs lattice matched to InP.[10,11] Low noise epitaxial ErAs/InGaAlAs Schottky diodes have been fabricated suggesting a low defect interface.[10,11] ErAs is thermodynamically stable in contact with III–V,[12] which means that the contacts should be stable under high temperature and high current densities. The ErAs/InGaAs interface is free of extended defects and has a continuous As sublattice.[13] As the ErAs is grown on InGaAs without breaking UHV, there is little risk of interfacial oxides. This epitaxial interface will have low surface states hence smaller depletion width. The Fermi level of ErAs is measured to be 0.15 eV below the

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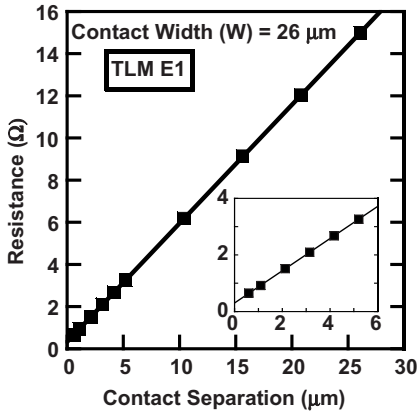

FIG. 1. Measured resistance vs contact separation for the ErAs/InAs/InGaAs contact (TLM E1). Contact width is 26 μm. The inset magnifies the range from 0.6 to 5 μm. The sheet resistance and contact resistance are calculated from the slope and *y*-intercept of the line fit.

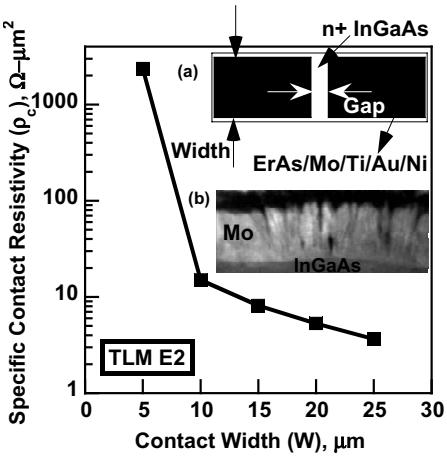

FIG. 2. Specific contact resistivity of TLM E2 as a function of the lithographic width of the contact. Inset (a) shows the top view schematic of a typical TLM structure. Inset (b) shows TEM of 20 nm Mo on InGaAs.

conduction band edge of InGaAs.[10] A theoretically perfect low-interface state and zero-barrier contact can be realized by ErAs contact to InAs/InGaAs, as the Fermi level is calculated to be above the conduction band edge of InAs. In principle, the contact resistance will be limited only by quantum mechanical reflections at the Mo/ErAs, ErAs/InAs, and InAs/InGaAs heterointerfaces.

Samples were grown by solid-source MBE. First, an unintentionally doped 1000 Å of InAlAs buffer was grown on (100) semi-insulating InP followed by 950 Å of highly doped InGaAs ($Si=8.0\times10^{19}$ cm^{-3}, $n=3.6\times10^{19}$). An additional 50 Å of Si ($Si=8.0\times10^{19}$ cm^{-3}) doped InAs was grown on top. Then 75 Å of ErAs was grown at 450 °C at 0.2 monolayers per second rate. The wafer was then transferred under UHV to an electron beam evaporator with a base pressure of 10^{-9} Torr and 200 Å of molybdenum (Mo) was deposited to protect ErAs from oxidation. The refractory metal Mo was chosen because of its thermal stability. The samples were then processed into transfer length method (TLM) structures with Ti/Au/Ni pads for contact resistance measurement.

The TLM method was used to measure contact resistance because of the high accuracy of the technique for properly designed test structures.[14] The TLM contact geometry and *n*-layer thickness was designed to accurately measure contact resisitivities of <1 Ω μm^2.[8]

Figure 1 plots the measured resistance versus the contact separation in the TLM structures (device run: TLM E1). Specific contact resistivity and *n*-InGaAs sheet resistance were calculated, respectively, from the *y*-intercept and slope of the linear fit to the measured data. The specific contact resistivity (ρ_c) for the ErAs/InAs/InGaAs contact was 1.5 ± 0.4 Ω μm^2 with error analysis according to Ref. 15. and the sheet resistance was 15 $\Omega/\square$.

The ErAs/InAs/InGaAs contact resistance, though very low, is higher than *in situ* Mo contacts to InAs/InGaAs.[9] The data from *in situ* Mo contact to InAs/InGaAs (Ref. 9) put an upper limit of 0.5 Ω μm^2 to both the InAs/InGaAs and the Mo/InAs heterointerface resistances. The Mo/ErAs interface resistance should be lower than Mo/InAs interface resistance because of higher electron density in ErAs. The higher contact resistance compared to *in situ* deposited Mo contact can be caused by oxidation of ErAs and depletion of carriers. ErAs can rapidly oxidize because of the strong affinity of Er to oxygen.[16] To evaluate whether oxidation of ErAs is the reason for higher contact resistance, TLMs (device run: TLM E2) were fabricated from the same wafer one year after storage in a N_2 box. A higher specific contact resistivity of 3.5 Ω μm^2 was obtained. Transmission electron micrograph (TEM) [Fig. 2(b)] of 20 nm Mo deposited under similar condition on InGaAs showed a nanoporous columnar morphology. The TEM cross-section samples were prepared by standard techniques including mechanical polishing using diamond lapping films followed by 4.5–1 kV Ar ion milling, as the final step. We believe the ErAs layer oxidized through the 20 nm columnar Mo. The oxidized ErAs region around the nanopores has high contact resistance. So the true ErAs contact area is smaller than the lithographically defined area. This makes the extracted contact resistivity higher than the true contact resistivity.

Figure 2 shows the contact resistance of TLM E2 as a function of the lithographic contact width (W). The extracted contact resistivity increased from 3.5 Ω μm^2 to 2.46 kΩ μm^2 when the contact width decreases from 25 to 5 μm. The 0.5 μm gap of the 2 μm wide TLM gave a high resistance of 5.5 kΩ. We attribute the increase in contact resistance at smaller contact widths (W) to lateral oxidation of ErAs under Mo. Besides the slow vertical oxidation through the Mo layer, there is rapid lateral oxidation of ErAs under the metal contact once the Mo cap layer was etched off to fabricate TLMs. The two orders of increase in specific contact resistivity of the 5 μm wide TLMs suggests almost complete oxidation of ErAs under the metal contact giving 2.5 μm as an approximate estimation of the lateral oxidation. The extremely high measured resistance of smallest gap of the 2 μm TLM indicates complete oxidation, suggesting at least 1 μm lateral oxidation. Because of lateral oxidation, the actual contact area is smaller than the lithographically defined contact area. So the extracted contact resistivity is larger than the true contact resistivity. The *y*-intercept in TLM measurement is extremely sensitive to the contact separation. The lateral oxidation of ErAs introduces large uncertainty (±3 μm) in the contact separation, which introduces large errors in estimating the true specific contact resistivity.

Thermal stability studies on the contacts were carried out by annealing the contacts under N_2 flow for 1 min at various temperatures. Figure 3 plots the specific contact resistivity as

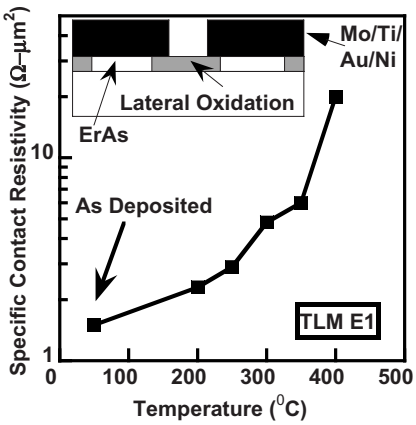

FIG. 3. Specific contact resistivity of TLM E1 as a function of the anneal temperature, for a duration of 1 min, in a flowing N_2 ambient. The inset shows a cross-section schematic of the TLM structure.

a function of the anneal temperature. The specific contact resistivity of TLM E1 increased gradually from 1.5 to 20 $\Omega\ \mu m^2$ after a 400 °C anneal. We attribute the increased contact resistivity with annealing to enhanced lateral oxidation of ErAs at higher temperatures. Before the anneal, the chamber was purged with N_2 for 3 min at 9 l/min flow rate. We believe that ErAs oxidized by reacting with the adsorbed oxygen on the wafer and residual moisture in the chamber. The contacts also degrade overtime, the contact resistivity of TLM E1 increased to 40 $\Omega\ \mu m^2$ when they were measured again, one year after fabrication. This shows that the ErAs layer continues to oxidize over time.

In conclusion, we fabricated ErAs/InAs/InGaAs epitaxial contacts with a minimum measured specific contact resistivity of 1.5 $\Omega\ \mu m^2$ (4.2 $\Omega\ \mu m$). The calculated contact resistivity is an overestimate because of lateral oxidation of ErAs. The real contact resistance is potentially very low at the ErAs/InAs interface. However it is difficult to measure the real contact resistivity using TLMs as there is rapid oxidation of ErAs once the TLMs are fabricated. It is difficult and impractical to integrate these contacts into scaled devices because they degrade rapidly over time and at elevated process temperatures. Thicker Mo may resolve the slow vertical oxidation problem, thus increasing the shelf life. The ErAs contacts can be effectively used in devices with buried contact structures as they are less likely to be prone to lateral oxidation.

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