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# PROCEEDINGS OF

# THE ADVANCED DIGITAL TECHNOLOGY

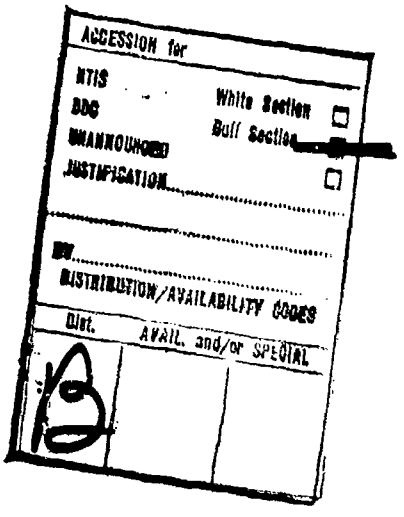
# CONFERENCE

VOLUME I

Naval Ordnance Laboratory
Silver Spring, Md.
8-10 June 1971



Sponsored by the Naval Air Systems Command
Washington, D.C.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# PROCEEDINGS OF

# THE ADVANCED DIGITAL TECHNOLOGY CONFERENCE

**VOLUME I**

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Silver Spring, Md.
8-10 June 1971.

Volume I.



Sponsored by the Naval Air Systems Command
Washington, D.C.

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AGENDA ITEMS WITH AN ASTERISK [*] ARE INCLUDED IN THESE PROCEEDINGS. THE REMAINING PAPERS WERE RECEIVED TOO LATE TO BE PUBLISHED.

CHARLES D. CAPOSELL
CONFERENCE COORDINATOR

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8-10 June 1971

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# ADVANCED DIGITAL TECHNOLOGY

# CONFERENCE

## OPENING COMMENTS

8 JUNE 1971

A. David Klein
Naval Air Systems Command
Washington D.C. 20360

THIS CONFERENCE BRINGS TOGETHER MANY DIVERSE RESEARCH AND DEVELOPMENT PROGRAMS. A GREAT MAJORITY OF THE PROGRAMS TO BE PRESENTED REPRESENT ONGOING OR RECENTLY COMPLETED EFFORTS WHICH WERE GOVERNMENT SUPPORTED. HOWEVER, SEVERAL PAPERS REPRESENT JOINT GOVERNMENT/INDUSTRY SUPPORTED PROGRAMS OR PROGRAMS SUPPORTED ENTIRELY BY THE INDUSTRY WHICH WERE INVITED DUE TO THEIR TECHNOLOGICAL SIGNIFICANCE AND TIMLINESS.

TOPICS TO BE PRESENTED COVER THE RANGE FROM MATERIAL GROWTH AND PREPARATION THROUGH THE IMPACT AND IMPLICATIONS OF NEW COMPUTER ARCHITECTURE ON THE EFFECTIVENESS OF MEMORY TECHNOLOGY. BETWEEN THESE EXTREMES WILL BE PAPERS IN THE AREAS OF MICROELECTRONIC PROCESSING, SWITCHING AND MEMORY DEVICES AND CIRCUITRY, LSI CIRCUIT INTERCONNECTION TECHNOLOGY, LSI TEST GENERATION AND ARRAY TESTING, LSI PACKAGING AND PACKAGING TECHNOLOGY, AND OPTICAL COMMUNICATION WITHIN SUBSYSTEMS.

ONE MIGHT CONCLUDE, AFTER LOOKING AT THE AGENDA FOR A MORE DETAILED VIEW OF THE TOPICS TO BE PRESENTED, THAT THIS CONFERENCE APPEARS TO BE AN ASSEMBLAGE OF NON-RELATED BITS AND PIECES OF TECHNOLOGY. HOWEVER THIS IS A SHORT SIGHTED AND INCORRECT CONCLUSION. SUCH A CONCLUSION COULD RESULT FROM A LACK OF UNDERSTANDING OF THE NATURE OF THE LSI TECHNOLOGY, WHAT IT IS, HOW IT CAN BE USED, AND ITS IMPLICATIONS RELATIVE TO FUTURE SUBSYSTEM ARCHITECTURE.

WE AT THE NAVAL AIR SYSTEMS COMMAND HAVE MADE A CONCERTED EFFORT TO EFFECTIVELY PLAN FOR THE USE OF LSI IN OUR FUTURE AVIONIC SYSTEMS. THIS CAN BE SEEM FROM THE SORK CARRIED OUT TO DATE IN PROGRAMS SUCH AS ADVANCED AVIONIC DIGITAL COMPUTER (AADC), WHICH MOST OF YOU ARE QUITE FAMILIAR WITH, INTEGRATED TACTICAL AIR CONTROL SYSTEM (ITACS), NAVAIR'S CNI PROGRAM, WHICH YOU WILL HEARING MORE ABOUT AT A CONFERENCE TO BE HEOD LATER THIS MONTH, AND SOLID STATE ELECTRIC LOGIC (SOSTEL), A PROGHAM RECENTLY REVIEWED AT NADC JOHNSVILLE IN THESE PROGRAMS, EFFORT HAS BEEN DIRECTED, FROM THE TIME OF PROGRAM INITIATION, TOWARD THE INCLUSION WITHIN THE SYSTEM APPROACH OF THE ABILITY TO BE TECHNOLOGICALLY FLEXIBLE. TOO MANY SYSTEMS IN THE PAST HAVE GIVEN TECHNOLOGY ONLY CURSORY CONSIDERATION AND ADDITIONALLY IN AN AFTER THE FACT MANNER MUCH TOO LATE IN THE DEVELOPMENT CYCLE TO HAVE ANY IMPACT UPON SYSTEN DESIGN. AS A RESYLT, NEW TECHNOLOGY HAS BEEN SHOEHORNED INTO BLACK BOXES RESULTING IN POOR PERFORMANCE, UNRELIABILITY, AND SYSTEMS WHICH ARE DIFFICULT TO MAINTAIN AND SUPPORT. ATTEMPTS TO UPDATE SYSTEM HARDWARE WHILE IN OPERATIONAL USE, USUALLY RESULT IN MAJOR REDESIGN IF NOT TOTALLY NEW SYSTEN DEVELOPMENT.

NEW SYSTEM ARCHITECTURE MUST BE COMPATIBLE WITH FUTURE TECHNOLOGY AND VICA VERSA. TO AVOID THE PITFALLS OF THE PAST, A WORKING INTERFACE MUST BE ESTABLISHED BETWEEN THE SYSTEM DESIGNER AND COMPONENT DEVELOPER. THE EFFECTIVE USE OF LSI, AS WELL AS OTHER ADVANCED TECHNOLOGIES, IN SYSTEM CAN BE ACCOMPLISHED ONLY THROUGH THE EARLY

INCORPORATION WITHIN THE SYSTEM APPROACH OF HARDWARE, MAINTENANCE AND SUPPORT CONCEPTS COMPATIBLE WITH THE CHARACTERISTICS OF THESE TECHNOLOGIES. EMPHASIS MUST BE PLACED EARLY IN THE DEVELOPMENT CYCLE ON EXPLORING AND ENHANCING TECHNICAL OPTIONS, PROVIDING A SOLID TECHNOLOGY BASE FOR THE FUTURE SYSTEM AND OVERCOMING PRESENTLY KNOWN TECHNICAL PREBLEMS THROUGH A CAREFULLY PLANNED PROGRAM OF RESEARCH AND DEVELOPMENT.

FOR INSTANCE IN THE LSI TECHNOLOTY, PROBLEMS WHICH ARE TODAY WELL RECOGNIZED SUCH AS PHOTO-PROCESSING ERRORS, DIELECTRIC PINHOLES, INTERLAYER CONTACTING, METAL CRACKING AT INSULATOR STEPS, ELECTRO-MIGRATION, DIE ATTACH FAILURE, ELECTRICAL BOND FAILURE, AND PACKAGE SEALING, NEED NOT HAVE THE PROFOUND EFFECT ON FAILURE RATES OF FUTURE LSI THAT THEY NOW DO. BY ISOLATING AND CHARACTERIZING THE PREDOMINANT FAILURE MECHANISMS AND DEVELOPING IMPROVED TECHNIQUES, MAJOR IMPROVEMENTS MAY BE MADE IN THE RELIANILITY AND COST OF FUTURE SYSTEMS.

THIS, GENTLEMEN, IS THE ESSENCE OF THE ADVANCED DIGITAL TECHNOLOGY CONFERENCE: THE EXPLORATION OF NEW TECHNOLOGY, SOLUTION OF PRESENT PROBLEMS AND PROVISION OF TECHNOLOGY BASE FOR FUTURE SUBSYSTEMS. IN THE SESSIONS WHICH FOLLOW YOU WILL BE HEARING PAPERS ON PROGRAMS WHICH COVER SEVERAL TECHNOLOGY AREAS. TODAY'S SESSIONS WILL BE CONCERNED BASICALLY WITH MATERIALS THIS MORNING, AND DEVICE PROCESSING THIS AFTERNOON. TOMORROW, THE MORNING SESSION WILL COVER LSI PACKAGING AND WHOLE WAFER MULTILEVEL INTERCONNECT TECHNOLOGY: THE AFTERSOON SESSION LSI ARRAY TESTING. ON THE THIRD DAY THE

MORNING SESSION WILL EXPOSE SEVERAL NOVEL DEVICE AND CIRCUIT CONCEPTS AND THE AFTERNOON SESSION NEW MEMORY TECHNOLOGY BEING CONSIDERED FOR THE AADC.

THE TECHNOLOGY PRESENTED HAS DEFINITE APPLICATION IN FUTURE DIGITAL SYSTEMS INCLUDING BUT BY NO MEANS LIMITED TO COMPUTERS. IT CAN BE USED TO PERFORM SIGNAL PROCESSING AND CONTROL FUNCTIONS IN SYSTEMS AREAS SUCH AS COMMUNICATIONS, NAVIGATION, IFF, RADAR, ELECTRONIC WARFARE, POWER DISTRIBUTION, DISPLAYS, AND GUIDANCE AND FIRE CONTROL. I HOPE, AS DOES ADMIRAL CLANCY, THAT THIS CONFERENCE WILL RESULT IN A BETTER UNDERSTANDING ON YOUR PART OF THE NAVAL AIR SYSTEMS COMMANDS TECHNOLOGY DEVELOPMENT PROGRAM, IMPROVED COOPERATION AND COMMUNCATION, AND THE STIMULATION OF NEW IDEAS WHICH WILL BENEFIT ALL OF US.

I WOULD LIKE, AT THIS TIME, TO THANK OUR PROGRAM SPONSORS, MR. FRANCIS LUEKING, NAVAL AIR SYSTEMS COMMAND, MR. NATHAN BUTLER, NAVAL ELECTRONICS SYSTEMS COMMAND, MR. DAVID BRAUNSTEIN, OFFICE OF THE CHEIF OF NAVAL MATERIAL, AND MR. JEROME PERSH, OFFICE OF THE DIRECTOR OF DEFENSE RESEARCH AND ENGINEERING, DEPARTMENT OF DEFENSE, FOR THEIR SUPPORT OVER THE YEARS.

IN ADDITION I WOULD ALSO LIKE TO EXTEND MY GRADITUDE TO CHARLES CAPOSELL WHOSE MOMENTOUS EFFORT MADE THIS CONFERENCE POSIBLE AND TO ANDREW GLISTA AND BARBARA ELLIS FOR THEIR ASSISTANCE.

AS SEVERAL PAPERS ARE INVITED AND OTHERS BASED UPON WORK THAT HAS NOT BEEN COMPLETED VIEWPOINTS EXPRESSED ARE NOT NECESSARILY THOSE OF THE NAVAL AIR SYSTEMS COMMAND.

# KEYNOTE ADDRESS
# CONFERENCE ON ADVANCED DIGITAL TECHNOLOGIES

RADM A. H. CLANCY, Jr.

ASSISTANT COMMANDER FOR MATERIAL ACQUISITION, NAVAIRSYSCOMHQ

IT IS MY PRIVILEGE TO ADD MY WELCOME TO THIS CONFERENCE ON ADVANCED DIGITAL TECHNOLOGY. I AM HAPPY TO SEE SUCH A LARGE AUDIENCE, INCLUDING SOME OF OUR SCIENTIFIC AND ENGINEERING FRIENDS FROM THE ACADEMIC COMMUNITY AS WELL AS THOSE PERSONNEL WITH INTERESTS AND CONTRIBUTIONS FROM THE NON-DOD CONTINGENT OF THE FEDERAL GOVERNMENT.

TODAY, EXCHANGES OF INFORMATION AS PROVIDED BY THIS CONFERENCE ARE BECOMING INCREASINGLY SIGNIFICANT. IN AN OPEN FORUM, SUCH AS THIS, WE CAN TAKE STOCK OF OUR SITUATION, IMPROVE OUR RELATIONS, ASSESS THE STATE OF THE ART, RE-ESTABLISH OUR GOALS AND PRIORITIES, AND COORDINATE TECHNICAL PROGRESS IN RESPECTIVE FIELDS OF INTEREST.

HERE, WE HAVE A REPRESENTATIVE CROSS SECTION OF THE GOVERNMENT, INDUSTRY, AND UNIVERSITY RESEARCH AND DEVELOPMENT COMMUNITY WHO ARE ENGAGED IN TECHNOLOGICAL ADVANCEMENTS OF UTMOST IMPORTANCE TO THE FUTURE OF NAVAL WEAPONS SYSTEMS. THE NAVY, AS A SPONSOR, AND YOU, AS A PARTICIPANT ARE PROVIDING A VITAL MANAGEMENT FUNCTION IN EVALUATING MUTUAL PROGRESS BASED ON A REALISTIC, FACTUAL, TECHNICAL INFORMATION EXCHANGE. I URGE EACH OF YOU TO CONTINUE THE DIALOGUE INITIATED TODAY. YOUR IDEAS, WHETHER PRESENTED AS CONFERENCE PROCEEDINGS OR INFORMALLY OVER A CUP OF COFFEE, REPRESENT THE BASIC BUILDING BLOCKS OF OUR TECHNOLOGY.

I AM SURE THAT EACH OF YOU RECOGNIZES THE INTENSE COMPETITION FOR RESEARCH DOLLARS IN TODAY'S MARKETPLACE. THIS COMPETITION IS NOTHING NEW. HOWEVER, IN AN ERA OF DECREASING BUDGETS, THE NAVY IS CHARGED WITH THE RESPONSIBILITY OF PROVIDING TO THE FLEET A SUPERIOR CAPABILITY AT THE LEAST POSSIBLE COST. THIS ATMOSPHERE OF INCREASING COST CONSCIOUSNESS IMPOSES SEVERE CONSTRAINTS ON OUR RESEARCH AND DEVELOPMENT PROGRAMS. FOR EXAMPLE, OUR PROGRAM MANAGERS ARE COMMITTED TO A POLICY OF REDUCED MAINTENANCE AND INCREASED RELIABILITY IN THE VERY EARLY PHASES OF R & D. THIS EARLY CONCERN FOR RELIABILITY AND MAINTAINABILITY DESIGN INCREASES OUR BASIC DEVELOPMENT COSTS AND THUS DECREASES DOLLAR AVAILABILITY FOR NEW PROGRAMS USING NEW TECHNOLOGIES THAT ARE THEORETICALLY PROMISING BUT EMPERICALLY UNDEMONSTRATED. HOWEVER, THE NAVY BENEFITS BY THIS APPROACH AS WE PROGRESS THROUGH DEVELOPMENT PHASES WITH A RESULTANT REDUCTION IN LIFE CYCLE COSTS DUE TO A POLICY OF EARLY CONCERN FOR MAINTAINABILITY AND RELIABILITY.

ANOTHER AREA IN WHICH WE ARE ATTEMPTING TO MAXIMIZE THE BENEFIT OF OUR DEVELOPMENT DOLLAR IS SYSTEMS DESIGN BASED UPON MODULARITY. HERE, WE ARE TRYING TO REDUCE INITIAL DEVELOPMENT COSTS BY PROVIDING AVIONICS SUBSYSTEMS IN THE FORM OF MODULAR FUNCTIONAL HARDWARE WITH MULTIPLE SYSTEM AS WELL AS PLATFORM APPLICATIONS. THIS NOT ONLY REDUCES INITIAL SUBSYSTEM DEVELOPMENT COSTS BUT ALSO CONTRIBUTES SIGNIFICANTLY TO MINIMIZING LIFE CYCLE COST BY REDUCING THE OPERATIONAL SUPPORT BURDEN IN AREAS OF MAINTENANCE AND PROVISIONING.

THE FINAL POINT I WOULD LIKE TO MAKE REGARDING COST IS THAT THE NAVY CANNOT SUPPORT THE TOTAL SPECTRUM OF RESEARCH AND DEVELOPMENT NECESSARY TO ACHIEVE ITS GOALS. WE RECOGNIZE THE FACT THAT INDUSTRY SPENDS LARGE AMOUNTS OF MONEY FOR

INTERNAL RESEARCH AND DEVELOPMENT BASED ON THE CONCEPT OF PROVIDING PRODUCTS THAT WILL OUTSTRIP THE COMPETITION IN THE MARKETPLACE. GENTLEMEN -- WE NEED THIS KNOWLEDGE -- THE NAVY CAN PROVIDE THE MARKETPLACE AND IN FACT THAT IS ONE OF THE UNDERLYING REASONS FOR THIS CONFERENCE. WE HOPE THAT IN MAKING OUR CAPABILITIES KNOWN TO YOU, YOUR INGENUITY CAN BE BROUGHT TO FRUITION IN NAVY ORIENTED PROGRAMS. SOME OF YOU HAVE ATTENDED OUR CONFERENCES IN THE PAST -- NOTABLY THOSE CONCERNING THE ADVANCED AVIONICS DIGITAL COMPUTER AND THE SOLID STATE ELECTRONIC LOGIC PROGRAM. YOU ARE PROBABLY AWARE THAT ON THE 29TH OF JUNE WE HAVE PLANNED A CONFERENCE ON THE INTEGRATED TACTICAL CONTROL SYSTEM. TO BE PERFECTLY HONEST, WE ARE TRYING TO INFLUENCE YOU TO THINK -- NAVY. WE NEED YOUR HELP -- WE ARE TELLING YOU OF OUR PROGRESS AND ACCOMPLISHMENTS -- OUR GOALS AND REQUIREMENTS ARE YOURS TO PURSUE.

I WOULD LIKE TO PROGRESS NOW FROM EXHORTATION TO INFORMATION. IN LOOKING AT NAVY GOALS AND THEIR RELATIONSHIP TO PROGRESS BEING REPORTED AT THIS CONFERENCE WE SEE THAT GENERALLY, THE DEVELOPMENT OF MATERIALS, COMPONENTS AND TECHNOLOGY FOR FUTURE AVIONIC SYSTEMS HAS THREE PRIMARY OBJECTIVES: FIRST, TO PROVIDE A BASELINE FOR THE GENERATION AND DEVELOPMENT OF NEW SUBSYSTEMS CONCEPTS AND HARDWARE TO COUNTER ENEMY THREATS; SECOND, TO IMPROVE THE PERFORMANCE LIMITS OF PRESENT SUBSYSTEMS, THUS REDUCING AIRCRAFT VULNERABILITY AND ATTRITION; FINALLY, TO REDUCE THE SUPPORT BURDEN IN THE FLEET THROUGH THE DEVELOPMENT, WHENEVER POSSIBLE, OF AVIONIC SUBSYSTEMS IN THE FORM OF MODULAR FUNCTIONAL HARDWARE WITH MULTIPLE AIRCRAFT APPLICATIONS INCLUDING BUILT IN TEST AND THROW AWAY MAINTENANCE AT THE MODULE LEVEL. EFFORT IN THIS AREA IS BEING DIRECTED AT

DEFINING THE THEORETICAL AND ENVIRONMENTAL LIMITS OF NEW ELECTRONIC, ELECTRICAL, AND ELECTRO-MECHANICAL MATERIALS AND DEMONSTRATING THE FEASIBILITY AND PERFORMANCE LIMITS OF NEW AND IMPROVED COMPONENTS AND TECHNIQUES WITH RESPECT TO FUTURE SUB-SYSTEM APPLICATION. IN ADDITION WORK IS UNDERWAY IN CONJUNCTION WITH SUBSYSTEM PROJECT ENGINEERS AND SYSTEMS PROGRAM MANAGERS, TO ASSIST IN THE DEFINITION AND DEVELOPMENT OF THE MOST EFFECTIVE SYSTEMS AND HARDWARE CONCEPTS AND PHILOSOPHIES TO OBTAIN THE MAXIMUM BENEFIT FROM NEW TECHNOLOGIES AVAILABLE IN TERMS OF PERFORMANCE AND SUPPORT REQUIREMENTS. FUTURE EFFORT WILL SEE PROGRESS IN THE AREAS OF AUTOMATING AND IMPROVING THE QUALITY OF LSI FABRICATION PROCESSES, DEVELOPMENT OF STANDARD LSI PACKAGES FOR FUTURE AIRBORNE COMPUTERS ALONG WITH ASSOCIATED PACKAGING TECHNIQUES, INVESTIGATION OF OPTICAL DATA LINKS FOR HIGH DATA RATE EMI INSENSITIVE INTERNAL COMMUNICATIONS, AND DEVELOPMENT OF IMPROVED ELECTRONIC COOLING TECHNIQUES, DATA CONVERSION DEVICES AND POWER SUPPLY TECHNOLOGY.

IN CLOSING, LET ME AGAIN WELCOME YOU TO THIS CONFERENCE. I HOPE THAT THE FOLLOWING SESSIONS WILL EFFECT IMPROVED COMMUNICATION AND COOPERATION AMONG ALL SECTORS OF THE TECHNICAL COMMUNITY WITH A RESULTANT GENERATION OF NEW IDEAS LEADING TO IMPROVED TECHNOLOGY FOR FUTURE SYSTEMS AS WELL AS SOLUTIONS OF OUR PRESENT PROBLEMS.

# ADVANCED AVIONIC DIGITAL COMPUTER STATUS REPORT

8 June 1971

Ronald S. Entner
Naval Air Systems Command
Washington, D.C. 20360

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# ADVANCED AVIONIC DIGITAL COMPUTER STATUS REPORT

Ronald S. Entner
Naval Air Systems Command
Washington, D.C. 20360

## Introduction

The Advanced Avionic Digital Computer (AADC) Program has, since 1968, been attempting to develop a modular, building block computer system which will optimally utilize the hardware and software technologies of the 1975 to 1985 time frame. Toward this end, the Naval Air Systems Command and the Naval Electronic Systems Command have supported and are continuing to support analytical and developmental efforts on a wide technological front. These efforts have brought together Government and Industry personnel in a coordinated effort that has resulted in new capabilities in computer design, digital technology and microelectronics in general.

The AADC program is conceptually partitioned into four major areas of concern:

- o Weapon System Analysis
- o Computer System Analysis
- o Software
- o Technology

Today I will address some of the desired goals and the progress to date in each area. Where possible, I will outline future planning.

## Weapon System Analysis

The purpose of the work carried out under the heading

of Weapon System Analysis is to insure that the AADC will be responsive to fleet needs in the 1975 to 1985 time frame and beyond, if possible. Toward this end, studies were initiated to investigate the nature of digital processing as could best be projected for that time frame. These studies have looked at fighter, attack, antisubmarine warfare, airborne early warning and reconnaissance missions, and have resulted in a fairly large body of documentation which includes mission profiles, mode analyses, processor task definitions, data and iteration rates, algorithms and assorted computer architectures.

Figure 1 lists the major weapon systems studied, who performed the work and tentative plans for FY'72. A bibliography does exist which provides particulars concerning the documentation.

Computer System Analysis

In the category of Computer System Analysis, we address the design of the computer system itself. Figure 2 illustrates an updated version of the AADC Baseline Organization, which besides being a very powerful architecture, presents all of the hardware elements currently projected for AADC. The major areas of development to date have been the Master Executive Control (MEC), the Arithmetic and Control (AAC) portion of the Processing Elements (PEs) and the Matrix-Parallel Processor (MPP).

There presently exists a set of English language

flowcharts which describe the performance of the MEC for an earlier Baseline configuration and six other versions of AADC, including some where the executive hardware has either failed or does not exist. This work was performed by Honeywell, Inc., with consultants at Analysts International Corp. and the University of Minnesota. Current plans call for expanding the executive system to perform the function of I/O controller for AADC as well as the Multiple Interior Communications System (MINCOMS). This concept was addressed briefly in the seventh AADC Progress Report. Additional analysis will investigate the MEC/Internal Communications System (ICS) interface and the design requirements for the Control portion of the PE to permit it to perform the MEC control and arithmetic functions. If successful, this approach will reduce executive hardware and software costs substantially, and provide a means for reverting gracefully to a floating executive in the event of an executive hardware failure.

The work on the Arithmetic and Control portion of the Processing Element has proven unusually productive. First, we have had the opportunity to evaluate, in somewhat rigorous detail, the advantages and disadvantages of the hard versus soft machine. Much is being said these days concerning the advantages of microprogrammed computers over hard-wired designs. These advantages were not made obvious by our studies. If anything, it was discovered that microprogramming can become a very expensive proposition, which provides design flexibility that can lead to significant

management problems, especially in the area of software development and maintenance. For the moment, we have decided to leave the soft machine to the Giant killers, and the Giants who prefer to make themselves elusive targets.

The hardwired design which we are using as the basis for further development provides significant performance advantages over present airborne computer architectures. These include:

- o Very high throughput
- o Efficient instruction utilization
- o Higher Order Language object code
- o Floating point and fixed point arithmetic
- o Multiple addressing, list and stack operations
- o Very rich instruction repertoire, including trigonometry, logrithms, hyperbolic functions, matrix, vector and complex arithmetic.

The Raytheon design is, in fact, capable of handling as primitives the entire repertoire proposed in the Systems Consultants study on the same subject, which is also listed in the bibliography.

Plans for this year include improvement of A&C/HOL compatibility, A&C/MEC commonality and firming up the A&C physical interface with the Internal Communications System (ICS). An additional, and extremely valuable task in light of NRL simulation findings, will result in providing additional logic to implement a memory paging strategy within the Control function of the PE. This should result in extremely

efficient utilization of BORAM and internal bus resources.

Another effort presently being weighed for FY'72 procurement, is an analysis effort in the area of the internal AADC bus system, or ICS. Due primarily to the very high data rates within the computer, compounded by the desire for "plugable" modularity, various design approaches are being considered for this application. One approach centers about the use of Time Division Multiplexing (TDM) to reduce pin counts, coding to provide bit synchronization and optics to provide a cost-effective means to communicate at rates above 200MHz. Figure 3 illustrates the type of approach which might be used to implement an optical simplex data bus. A major concern with this technique is the complexity required to implement a cost-effective, multiport, duplex fiber optic bus.

Since the initiation of the AADC program, it has been argued that some form of bulk parallel processor will be required within the general purpose computer framework for use in the post 1975 time frame. None of the work which has transpired to date has modified this position. If anything, the requirements for such processing have become better defined, and a sense of finally having one's finger on the problem is a fair way to describe where we think we are today.

While much work has been done to develop a cellular associative processor with sophisticated processing capability, analyses have caused us to reevaluate this approach in light of system hardware and software operating efficiency

and cost. Figure 4 of a General Purpose Array Processor illustrates an alternative architecture which provides, among other advantages, hardware and software commonality with the sequential simplex and multiprocessor organizations, as well as an innate capacity for resource optimization; that is, machine architecture which physically resembles a two dimensional array is only used efficiently when computing a full matrix of the same size as the hardware. More often than not, this situation will not exist in the real world.

Figure 5 summerizes the work which has been accomplished to date under this heading.

Software

The principle work which has occured to date in the software area has resulted in the recognition that:

- Present high level aerospace programming languages are not sufficiently broad for economical use outside the limited area of applications programming
- Problem Oriented Languages (POLs) are required to provide dynamic computer utilization by persons other than experienced programmers.

In response to the first deficiency, a funded program is planned which will investigate extentions to the current Navy CMS-2 programming language. These extentions will permit efficient programming in the areas of:

- Applications
- Executive
- Input/Output

o Test

o Display

o Array processing.

An additional element of the planned effort calls for investigation of data descriptive language techniques. These techniques, which provide for language independent data declarations, may help in the future integration of large processing systems which have been programmed in different languages.

The need for developing facilities to program in Problem Oriented Languages is being investigated by the Navy under the sponsorship of the Office of Naval Research. One method under consideration uses interactive graphics to provide cues to the programmer, and inclusive validization programs to assure the quality of the composed programs. The system, called the Tactical Interactive Programming (TIP) Facility is illustrated in Figure 6.

Other work in the software area includes initiation of efforts to define and develop the programming tools needed to truly implement software modularity, or software engineering, in light of the AADC's modular hardware. This work could ultimately lead to a Metaplex compiler.

As mentioned previously, the present Arithmetic and Control subsystem design provides a high degree of HOL compatibility. How this capability will effect the requirements for language and compilers will be investigated in FY'72. Our opinion for the time being is that this facility will not do as much to reduce programming requirements

as it will assist in the mainteranoe and debugging of these programs.

Figure 7 summerizes the work which can be collected under the software heading.

Technology

The fourth, and final area of concern is technology. Under this heading we place all the work which relates to the physical constituants of the AADC -- the hardware which will go into making the PEs, the RAMs, the BORAMS, the buses, etc.. In the end, it will be the technology which will manifest itself as the computer.

From the inception of the program, the technology aspect of AADC has always been the area which has caused most of you to raise an eyebrow -- or two. In effect, this is one reason why there is a conference on digital technology. But, it has also been said by us that AADC does not depend on advanced technology for its feasibility. In fact, we still say the same thing today; only, we don't pretend that a state-of-the-art AADC would be the same revolutionary machine that advanced technology will make it.

We at NAVAIR and NAVELEX have been fortunate to view and have a hand in the development of the technology which will be state-of-the-art five and ten years from now. This perspective has helped mold the AADC concept into what it is today. My fondest hope is that as a result of this conference, some people, especially those of you who are in a position to chart the course of your own in-house technology and computer

developments, will go back and measure their own work against the work of an audacious segment of the digital technology industry.

For the sake of completeness, Figure 8 illustrates the technology work that has taken place or else is planned which directly relates to AADC. As this work, along with other equally significant contributions to the technology will be presented in detail over these next few days, there is little reason for me to continue my discussion. Instead, I prefer to take this opportunity to personally thank all of you for being here. I think you will find that the papers you are going to hear auger new possibilities in this, our mutual field of interest. I think that AADC is only one of those possibilities. Thank you again.

8 June 1971

| AREA OF CONCERN | CONTRACTOR | OUTPUT | FY-72 PROGRAM PLAN |
|---|---|---|---|
| I. WEAPON SYSTEM ANALYSIS | | | |
| AEW | GENERAL ELECTRIC<br>RAYTHEON | REPORT<br>" | AADC/ATCS ANALYSIS |
| ASW | HONEYWELL<br>HUGHES | "<br>" | LAMPS ANALYSIS |
| ATTACK | IBM<br>NADC | -<br>REPORT | EXPAND NADC IAD |
| FIGHTER/ATTACK | HUGHES<br>RAYTHEON<br>WESTINGHOUSE | "<br>"<br>" | FARS ANALYSIS<br>CONTINUE MATRIX-PARALLEL PROCESSOR STUDIES |
| F-14C | GRUMMAN | " | EXPAND INVESTIGATION OF I/O AND OBC |
| RECONNAISSANCE | RAYTHEON<br>WESTINGHOUSE | " | SAME AS FIGHTER/ ATTACK |

FIGURE 1

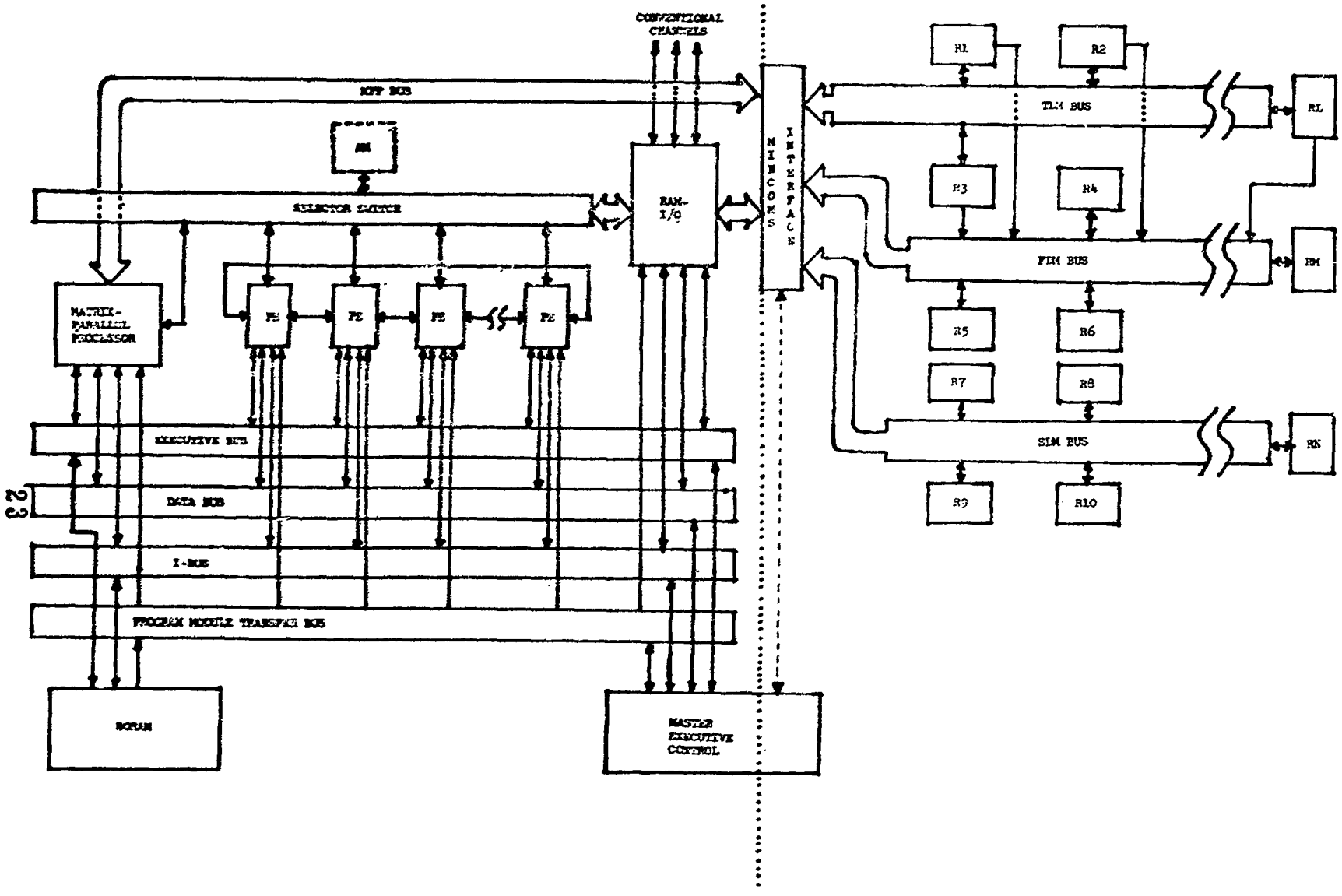


Figure 2 : ADVANCED AVIONIC DIGITAL COMPUTER BASELINE

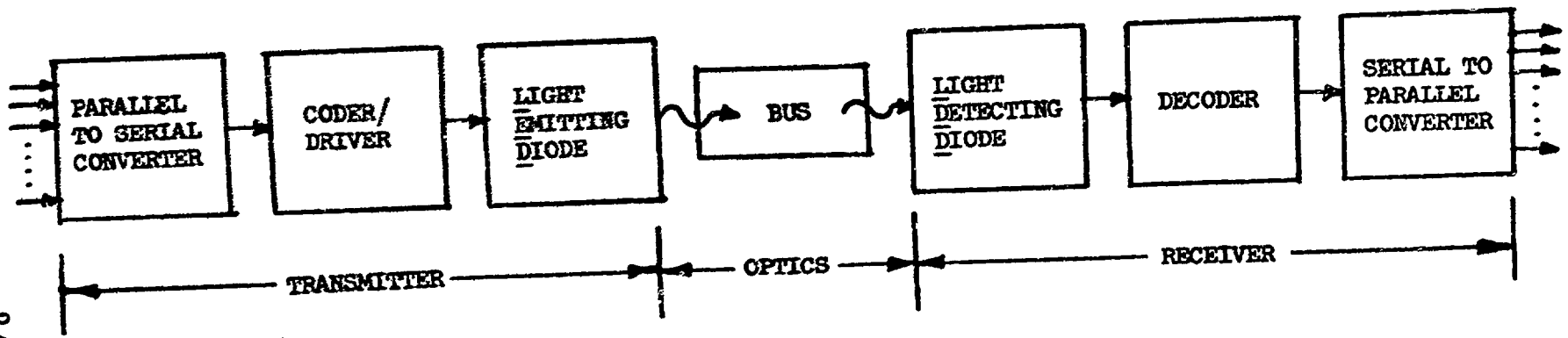


FIGURE 3: SIMPLEX OPTICAL BUS

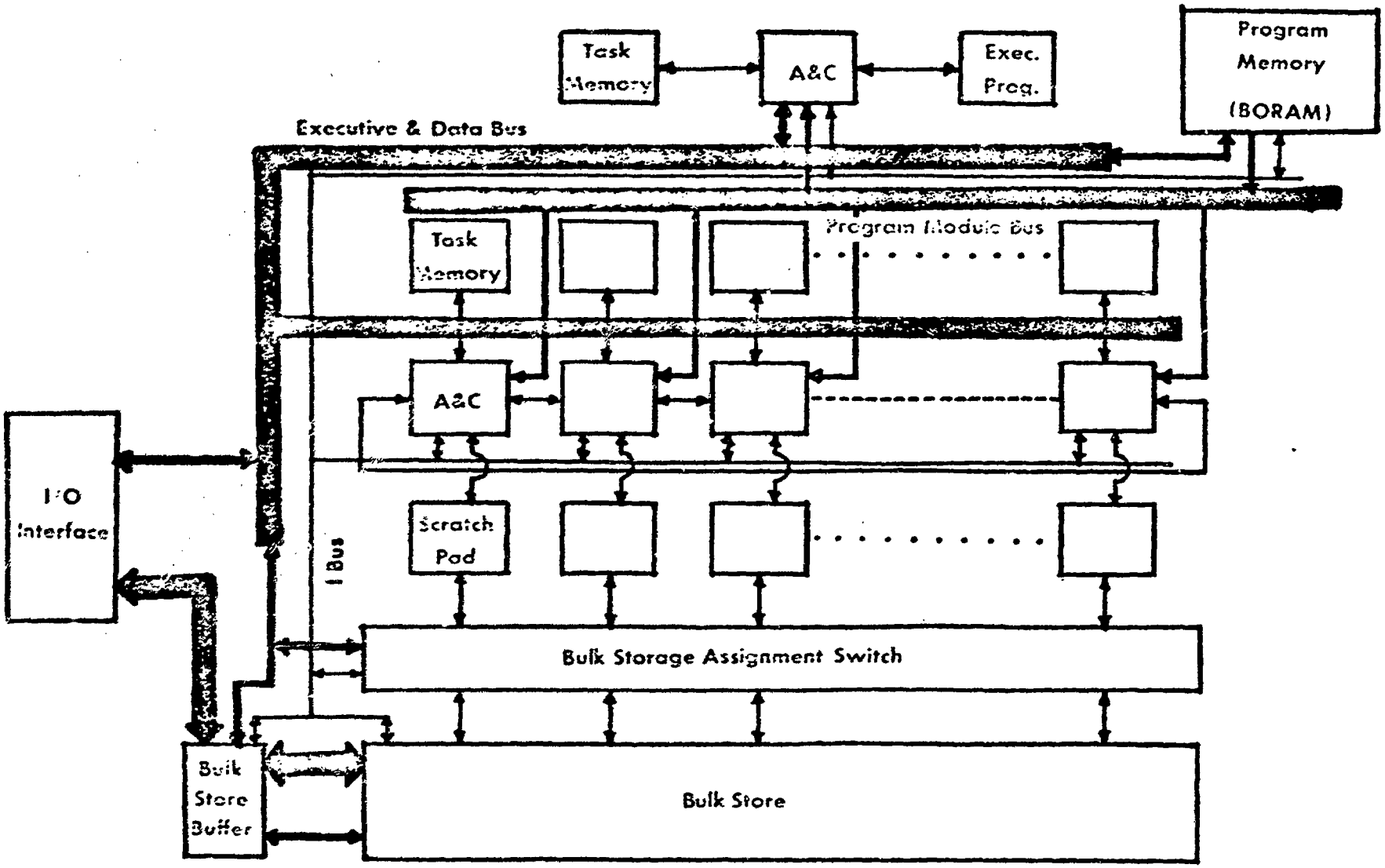


FIGURE 4: GENERAL PURPOSE ARRAY PROCESSOR

| AREA OF CONCERN | CONTRACTOR | OUTPUT | FY-72 PROGRAM PLAN |
|---|---|---|---|
| II. COMPUTER SYSTEM ANALYSIS | | | |
| MASTER EXECUTIVE CONTROL (MEC) | HONEYWELL | MEC FLOWCHART DESIGN. | IMPROVE PRESENT DESIGN. PROVIDE I/O CONTROL FEATURES. DEFINE HARDWARE REQUIREMENTS FOR FEDERATED MEC. |
| ARITHMETIC AND CONTROL (A&C) | RAYTHEON<br>HUGHES | LOGIC LEVEL DESIGN.<br>REGISTER LEVEL DESIGN. | COMPLETE LOGIC DESIGN. IMPROVE HOL FACILITY. PROVIDE PAGING CAPABILITY. |
| INSTRUCTION REPERTOIRE | SYSTEMS CONSULTANTS<br>NRL<br>RAYTHEON/WESTINGHOUSE/<br>HONEYWELL | REPORT | COMPLETE INSTALLATION OF EMULATION FACILITY AT NRL USING BURROUGHS' D-MACHINE. |
| ASSOCIATIVE (ARRAY) PROCESSING | NRL<br>SRI<br>RCA<br>WESTINGHOUSE | AP DESIGN.<br>CONSULTATION.<br>CMOS CHIPS.<br>PRELIMINARY GP DESIGN. | CONTINUE TO STUDY APPLICATIONS OF ARRAY PROCESSING. INITIATE GP ARRAY DESIGN EFFORT. |
| GENERAL | NRL<br>UCLA | SIMULATOR<br>CONSULTATION | INTEGRATE NRL FACILITY. INCORPORATE COST-EFFECTIVENESS FEATURE. DEVELOP GP TRANSFORM METHODS. |

FIGURE 5

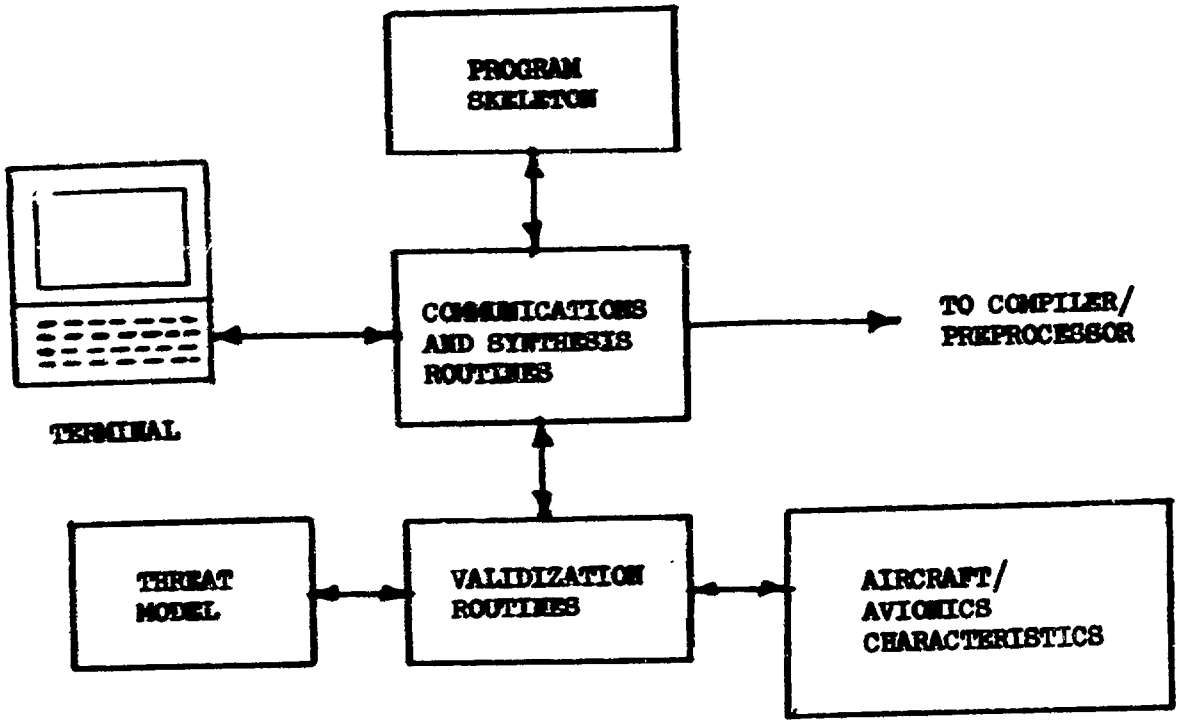


FIGURE 6: TACTICAL INTERACTIVE PROGRAMMING (TIP) FACILITY

| AREA OF CONCERN | CONTRACTOR | OUTPUT | FY-72 PROGRAM PLAN |
|---|---|---|---|
| III. SOFTWARE | | | |
| LANGUAGE | NELC/FCPCPAC | ANALYSES/RFP | DEVELOP CMS-2 EXTENTIONS TO PROVIDE TOTAL HOL PROGRAMMING CAPABILITY. INITIATE DEVELOPMENT OF METAPLEX COMPILER. |
| COMPILERS | SYSTEMS CONSULTANTS | REPORT ON REQUIREMENTS TO RUN CMS-2 ON AADC HARDWARE. | AS ABOVE. |
| HOL/HARDWARE COMPATIBILITY | RAYTHEON | A&C DESIGN INCLUDES DEFFERAL MECHANISM WHICH CAN BE USED TO EXECUTE HIGH LEVEL STATEMENTS DIRECTLY. | COMPLETE HOL COMPATIBILITY DESIGN ANALYSIS. CONTINUE REPERTOIRE STUDIES. |
| ARRAY PROCESSING | NRL | MATRIX AND FFT ALGORITHMS. | DEVELOP HOL CAPABILITY IN THE AREA OF ARRAY PROCESSING. |
| ALGORITHMS | BOEING | TRAJECTORY PREDICTION ALGORIHMS. | DEVELOP ADDITIONAL LIBRARY FUNCTIONS. |



FIGURE 7

| AREA OF CONCERN | CONTRACTOR | OUTPUT | FY-72 PROGRAM PLAN |
|---|---|---|---|
| IV. TECHNOLOGY | | | |
| SEMICONDUCTOR | HUGHES | PAD RELOCATION ANALYSIS. ION IMPLANTATION. | DEVELOP TEST TECHNIQUES COMPATIBLE WITH PAD RELOCATION AND WHOLE WAFER LSI. |
| | RCA | MOS THRESHOLD LOGIC. | |
| | TEXAS INSTRUMENTS | STEPLESS INTERCONNECT. EUTECTIC WAFER BONDING. | DEVELOPMENT AND DELIVARY OF MOS THRESHOLD ARRAY. DEVELOP PROCESSES |
| | WESTINGHOUSE | HYBRID LSI INTERCONNECTION TECHNIQUE. ELECTRON IMAGE PROJECTION. | COMPATIBLE WITH 3" WAFERS. FABRICATE AND DELIVER SAMPLE WAFERS. DEVELOP SPIDER BONDING TECHNIQUES. |
| MAGNETICS | AMPEX | CLOSED FLUX PATH MAGNETIC THIN FILM MEMORY ANALYSIS. | DEVELOP AND DELIVER PARTIALLY POPULATED CFM MEMORY SYSTEM. |
| | LITTON DATA SYSTEMS | POST AND FILM MEMORY ANALYSIS. | REFINE FERROACOUSTIC MEMORY TECHNOLOGY. |
| | GENERAL DYNAMICS | FABRICATE PARTIALLY POPULATED FAME MEMORY SYSTEM. | DEVELOP AND DELIVER A PARTIALLY POPULATED SONISCAN MEMORY. |
| | SYLVANIA | SONISCAN ENVIRONMENTAL AND PERFORMANCE ANALYSIS. | |
| PACKAGING | KEARFOTT | LSI PACKAGES | STANDARD PACKAGES WILL BE TESTED BY NAFI AGAINST MIL-E-5400 CLASS 4X. SPECIFICATIONS WILL BE PREPARED. SECOND LEVEL PACKAGE WILL BE INVESTIGATED. |
| | WESTINGHOUSE | LSI PACKAGES | |
| | NAFI | 3" THICK FILM TEST SUBSTRATES. | |
| $S^2VC$ | ELECTRON EMISSION SYS. | TWO POWER SUPPLY MODULES | APPLY $S^2VC$ TECHNOLOGY TO REPLACE TRANSFORMERS. |

FIGURE 8

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# GROWTH OF CONTROLLED PROFILE CRYSTALS FROM THE MELT

A. I. Mlavsky and H. E. LaBelle, Jr.

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# GROWTH OF CONTROLLED PROFILE CRYSTALS FROM THE MELT

by

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## ABSTRACT

Prompted by the need for a high modulus, high strength, coreless continuous filament for use in high performance structural composites, we investigated various techniques for the growth of sapphire filaments directly from the melt. Efforts to produce objects from the melt in directly useable form date back to 1857 (G. Bessemer). In 1922 von Gomperz used the floating disc on a melt surface to produce controlled shape metal single crystals. More recently interest in the growth of semiconductor ribbon has stimulated dendritic growth, web growth, and ribbon growth by melt guidance techniques.

Under support from the Air Force Materials Laboratory, Nonmetallic Materials Division and subsequently also the Manufacturing Technology Division, Wright-Patterson Air Force Base, we have developed growth techniques for the continuous production of controlled profile crystals from the melt. The primary emphasis has been on sapphire, or alpha-alumina,since filaments of this material exhibit high strength, high modulus, and low density. Also other sapphire crystals such as tubes and ribbons have optical and electronic applications because of the transparency, hardness, chemical resistance and refractoriness of the material. The technique is, however, equally applicable to a large range of materials including incongruently as well as congruently melting ones. It is only necessary that the material melt without producing a high vapor pressure of any or all

constituents, and that a suitable crucible material for it can be found.

Some properties of the products so far produced by this technique will be described including those of filaments which have been grown in lengths of several hundred feet and the diameter range from a few mils up, and of sapphire ribbons 1" wide x 5' long with thicknesses around 30 mils. Other materials which have been grown include spinel, various ferroelectrics, and both ionic and metal single crystals. It is accordingly postulated that the technique can readily be applied to the growth of continuous semiconductor ribbons.

## INTRODUCTION

The growth of continuous sapphire filaments from the melt[1] was undertaken following the demonstration that small sapphire whiskers produced in a batch process can exhibit extremely interesting mechanical properties and that these properties can be exploited in composites. It was expected that a continuous preparation process would lead to ease of handling, improved composite fabrication, and economic cost of production of the filament.

As a candidate for use in a composite, sapphire has very attractive physical properties including a high modulus of elasticity, low density, and potentially high tensile strength both at room and elevated temperatures. Its chemical inertness suggests that it would be promising in high temperature metallic composites, and its high dielectric strength makes it an excellent choice for epoxy composites in applications where electromagnetic radiation transparency is essential, e. g. in radomes. Further, other sapphire shapes, such as tubing and ribbon, have applications in a number of optical and electronic devices.

Single crystal sapphire ($\alpha$-$Al_2O_3$) has previously been available in three distinctly different physical forms: bulk crystals grown by melt[2, 3], vapor[4], and hydrothermal[5] techniques; platelets grown by flux/solvent[6] techniques; and whiskers grown by vapor techniques[7]. Except for vapor growth these techniques, as previously practiced, have not yielded a continuous process.

A good deal of information has been generated on the mechanical properties of both large melt grown materials[8] and micron-sized vapor grown whiskers[9]. It is obvious that whiskers can, in fact, approach the theoretical strength of sapphire, while melt grown material has generally been considerably weaker, typically 20 - 30 times lower in tensile strength. (A mean strength of $1.6 \times 10^6$ psi has been reported[9] for whiskers having cross-sectional areas in the 0.1 $\mu^2$ - 1.0 $\mu^2$ range.) The most generally accepted reason for the high strength of whiskers is that they have fewer defects, based simply on the fact that the probability of a surface flaw is considerably less for the micron-sized whisker. Investigations have shown, however, that even submicron-sized whiskers have surface steps or flaws. In recent work by F. P. Mallinder and B. A. Proctor[10], centerless ground sapphire rods were carefully fire polished before testing, yielding maximum bending strengths close to 1,000,000 psi. This, of course, is strong evidence that the apparent weakness of bulk sapphire is mainly due to its surface quality. As Mallinder, et al state, this evidence suggests that large sapphire crystals could be produced having strengths comparable to those of whiskers. In fact, measurements on sapphire filaments grown from the melt by the process to be described below tend to corroborate this hypothesis.

## HISTORICAL SURVEY OF THE MELT GROWTH OF SHAPED CRYSTALS

Scientists have for a number of years concerned themselves with the problem of producing objects from the melt in their directly useable form, i.e. in contrast to melting the raw material, solidifying it in one form, and then forging and working it into another. It is obvious, for instance, that any continuous production of sapphire whiskers should avoid mechanical working of the surface.

Experiments along these lines were reported as early as 1857. Thus, according to Stepnov[11], the English metallurgist G. Bessemer experimented in forming metal articles directly from the melt, this work being later extensively extended by Stepnov and co-workers.

In 1922 von Gomperz[12] reported the use of a floating mica disk with a hole at its center to control the shape of metal crystals grown from the melt. In recent years this type of approach was introduced into the semiconductor industry for the production of device quality ribbons of germanium and silicon continuously from the melt. The advantages of such a process are obvious if one considers the economics involved in slicing and polishing device material from a large boule versus transversely cutting the ends of a ribbon to the desired length.

The interest in the growth of semiconductor ribbon can be appreciated from the large volume of scientific literature which has been published on the topic. There were at least two basic approaches used for ribbon growth. Initially, the majority of investigators used dendritic growth[13-18] with specially twinned seed crystals. In dendritic growth, the growth interface advances into a supercooled area of the melt. Since the latent heat of solidification can readily be transferred from the growth

interface to the cooler surrounding liquid, growth usually takes place at a rapid rate (e. g. 7 in/min for sapphire filaments). In the special case of dendritic ribbon growth of germanium, a mu'ti-twinned seed crystal[13] has been found necessary for continuous propagation.

Simultaneous work initiated on the ribbon growth of germanium by the Czochralski technique through melt guidance[19] seems to have been neglected later compared with the investigations on dendritic growth. Briefly the Czochralski technique employs a seed crystal which is in contact with a melt of the same material, the melt being contained in a non-reactive crucible. As the seed is withdrawn molten material solidifies on to it, producing a crystal at a relatively slow rate (e. g. 6 in/hr for silicon). In this process the solid-liquid interface is maintained close to the equilibrium crystallization temperature.

Recently, the observed non-dendritic growth of both silicon[20] and germanium[21] has been published. In comparing this with the dendritic technique, it would appear that dendritic growth should offer the greater growth speeds (due to the supercooled-dendritic growth mechanism), while the non-dendritic technique should offer the greatest versatility; (a single crystal is grown instead of a specially twinned morphology).

## EXPERIMENTAL APPROACH

In an attempt to grow sapphire filament and other shapes from the melt, both dendritic and non-dendritic techniques were considered. A prerequisite to continuous dendritic growth experiments was determination of the proper seed to employ (with respect to orientation) and twinning.

Sapphire dendrites were produced spontaneously to obtain this information. Dendrites were produced in a standard Czochralski puller using a molybdenum crucible with a carbon susceptor. A sapphire seed of arbitrary orientation or a tungsten rod was introduced into a crucible containing molten alumina, and the power to the furnace was shut off. Dendritic growth proceeded radially from the seed along the top surface of the melt; the growing mass was then rapidly removed before complete solidification of the melt could occur. Dendrites such as the one shown in Fig. 1 were broken from the mass. X-ray examination of some dendrites produced in this manner showed the c-axis to be at least one of the major axes for dendritic growth. We therefore chose to attempt filament growth using a c-axis ( 0001) seed.

The apparatus used was essentially a modified crystal pulling furnace. A major modification was the use of a needle valve controlled, hydraulic-pneumatic piston to produce uniform linear motion of the seed shaft over a speed range of several inches per hour to several inches per minute. For the growth of continuous filaments, a pair of endless belts was used as the pulling mechanism, and a friction-clutch spool was used to collect the filament. A schematic of the crucible, susceptor, etc. is shown in Fig. 2. A feature of this part of the apparatus is the use of carbon cloth for radiation shielding: three turns of cloth held in place by carbon yarn increased the temperature by 200-500$^{o}$C for a given power input. Another feature is the use of water cooling between the two concentrically positioned quartz tubes. Since a majority of the infrared is absorbed in the water, a microscope for visual observation can be positioned close to the rf coil without excessive heating. Helium or argon was used as the atmosphere.

Early attempts to grow sapphire filament employed the setup as is shown in Fig. 2, with various additional radiation shielding on top of the crucible. Since induction heating was used, the temperature distribution could be changed by variations in the radiation shield design and by deliberately supplying more heat to either the bottom or top of the crucible through changes in its position relative to the work coil.

A typical experiment involved (1) melting the sapphire, (2) inserting the c-axis seed into the melt, (3) supercooling the melt, and (4) withdrawing the seed. Under some conditions of thermal distribution, we observed that dendrites up to several millimeters in length propagated vertically downwards into the melt.

The experimental evidence implied that controlled vertical growth required the use of radiation shielding such that annular rings having a small inside diameter (on the order of 1/32") should be placed on top of the crucible. This assumes that heat loss would be greatest in a small region at the center of the melt surface.

An alternate technique which suggested itself was to place a shield directly on the surface. If such a shield were rigidly held by mechanical means, however, a continuous adjustment would be required as a consequence of the liquid level changing as material was removed. A more practical solution was found by using a shield which would float, and therefore always remain on the melt surface regardless of its position relative to the crucible. This type of arrangement is shown in Fig. 3. A molybdenum annulus having a 1/16" diameter orifice at its center was placed directly on the melt surface. Since molybdenum is heavier than molten alumina, the floating orifice was fashioned into a boat, although it

might be expected from the high surface tension of the molten material (690 dyne/cm) that a thin sheet of molybdenum placed on the surface would float.

Using a floating shield and orifice in the apparatus shown in Fig. 2, we were able to grow filaments of sapphire simply by seeding in the orific , supercooling the melt, and subsequently retracting the seed at rates of up to several inches per minute. Accurate temperature measurements are difficult at these temperatures; (the melting point of sapphire has been reported by several investigators, the most generally accepted being 2072°C). However, evidence that molten alumina could be supercooled up to at least 100°C at fast cooling rates was obtained by placing a standard tungsten-rhenium thermocouple in the melt and recording its output as the material was cooled and solidified. The latent heat of solidification released is substantial and can be seen as a bright flash as the material solidifies. This, of course, is further evidence that solidification can take place at a very rapid rate.

A c-axis filament grown at 6 in/min is shown in Fig. 4. It should be noted that the filament was between .004 - .020" in diameter (tapered along its length) and was grown from a 1/16" diameter orifice. This filament is typical of our early results, although in some cases much more complicated habits were formed. Fig. 5 shows four typical types of habits formed. All of these crystals had faceting on their surface, with type A being most nearly circular. A detailed analysis of these different filaments was not made; however, Laue-back reflection photographs showed type A to be grown in the c-direction, with subgrain boundaries being present.

The tensile strength of these faceted filaments was approximately $125 \times 10^3$ psi as measured in flexure. In these cases the filaments were growing dendritically from an orifice 1/32" - 1/16" in diameter, at rates up to several inches per minute. It should be noted that although a floating orifice was used, it was not employed to guide the melt, but to achieve the proper thermal distribution. This is attested to by the fact that the filaments are not necessarily the shape or size of the orifice.

Recent advances in technique have enabled the production of single crystal sapphire filaments as small as 1.5 mils in diameter, having non-faceted surfaces and being free from easily detectable subgrain boundaries. Most commonly, 10 mil diameter filaments are produced in lengths of several hundred feet (Fig. 6). Further refinement in means for controlling the profile of the growing crystal have led to the growth of sapphire tubes up to 1" in diameter, ribbons up to 5 ft long x 1" wide, and other more complex shapes, as shown in Fig. 7. The technique has also been extended (with the help of a number of our colleagues at Tyco) to the growth of a number of other crystalline materials, including BeO, $LiNbO_3$, LiF, $BaTiO_3$, Cu-Au solid solutions, NaCl, $MgAl_2O_4$, and others. $LiNbO_3$, in particular, has been grown as single crystal, single domain ribbons 1/4" wide by over 21" long (Fig. 8).

## MECHANICAL PROPERTIES OF SAPPHIRE FILAMENT

As mentioned previously, the tensile strength of the highly faceted filaments appeared to be low. It should be noted, however, that cross-sectional area measurements were difficult in many cases. The smooth filaments recently produced yielded an average room temperature tensile strength of greater than 370,000 $lb/in^2$, with maximum values in excess of

500,000 lb/in$^2$ in the 4-6 mil diameter range. A maximum value of 625,000 psi has been obtained on a 1.5 mil diameter filament. All of these strengths were measured in tension. Modulus of elasticity measurements on long filaments yield a value of 67,000,000 psi in tension.

In comparing the strength of these filaments with other forms of sapphire, the material is much stronger than the bulk sapphire previously tested by Watchman and Maxwell[9] where bending strengths of 102,000 psi were observed on centerless ground fire polished c-axis sapphire.

The results of Mallinder and Proctor[10] showed bending strengths ranging from 280,000 psi to nearly 1,000,000 psi, for one millimeter diameter centerless ground fire polished sapphire. In the latter case extreme care was taken during the fire polishing technique; the rods were carefully selected for perfection; the apparent gauge length was 3 mm. In contrast, the melt grown sapphire filaments were tested in tension with 25-50 mm gauge lengths and without critical inspection or handling. As the bending strengths generally give greater values than the tensile strength, the filaments should be on the average considerably stronger than the 1 mm rods tested. The average strengths are weaker than vapor grown whiskers; however the larger whiskers having diameters in the range of the filaments have strengths equal to or lower than the filaments[9]. This is more significant since the gauge length for the whiskers is considerably smaller.

## SUMMARY

A process has been developed to produce single crystal sapphire filament of one mil in diameter or greater in continuous lengths. The strength of these filaments is essentially the same as that of other high

modulus filamentary materials commercially available, such as boron and silicon carbide. The feasibility of producing many filaments continuously from a single piece of equipment has been demonstrated. The successful use of this material now depends on its compatibility in composites and, ultimately, on the economics of the process.

The process has been extended to the growth of sapphire with essentially any cross section (over very broad limits); thus sapphire filaments, rods, ribbons, and tubes of various shapes have been grown. It is also of interest that the process is by no means limited to sapphire, but has been demonstrated to be applicable to a wide range of other crystalline materials, including even some non-congruently melting ones.

We believe that this technique is the first one that produces truly continuous single crystals from the melt at fast rates, and with accurately controlled cross sections. It appears clearly applicable to the growth of ribbons of silicon and other semiconductors.

ACKNOWLEDGMENTS

We would like to acknowledge the valuable assistance of our many colleagues who have contributed to this work, specifically Dr. G. Hurley and W. Sherman who were responsible for the mechanical measurements; B. diBenedetto, W. Clements, and C. Cronan who grew many of the sapphire shapes as per Fig. 7; S. Mermelstein, L. Bellomo, and H. Binney who designed and constructed equipment for continuous filament growth; Dr. G. A. Wolff and Dr. B. Das who assisted in crystallographic and X-ray analysis; and J. Bailey and W. Little who assisted in various phases of crystal growth.

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REFERENCES


1. LaBelle, H. E. Jr., and Mlavsky, A. I., Nature, 216, 5115 (1967) 574.

2. Verneuil, A., Ann. Chim. Phys. 3 (1904) 20.

3. Paladino, A. E. and Roiter, B. O., J. Am. Ceram. Soc. 47 (1967) 456.

4. Schaffer, P. S., J. Am. Ceram. Soc. 48 (1965) 508.

5. Laudise, R. A., and Ballman, A. A., J. Am. Chem. Soc. 80 (1958) 2655.

6. White, E. A. D., Nature, 191, 4791 (1961) 901.

7. Webb, W. W., and Forgeng, W. D. J. Appl. Phys. 28 (1957) 1449.

8. Watchman, J. B. and Maxwell, L. H., J. Amer. Ceram. Soc. 42, 432 (1959)

9. Mehan, R. L. and Feingold, E., Chapter 15 in Strengthening Mechanisms, Metal and Ceramics (Burke, J. J., Reed, N. L., and Weiss, V., ed) 1966.

10. Mallinder, F. P. and Proctor, B. A., Phil Mag 13 (1966) 121.

11. Stepanov, A. V., Soviet Physics - Tech. Phys., 4 (1959) 339.

12. von Gomperz, E., Z. Physik., 8, 184 (1922).

13. Bolling, G. F. and Tiller, W. A., in Metallurgy of Elemental and Compound Semiconductors, 97 (Interscience Publishers, New York and London, 1960).

14. John, H. F. and Faust, J. W. Jr., ibid. pg. 127.

15. O'Hara, S. ibid pg. 148.

16. Holmes, P. J. ibid pg. 161

17. Wagner, R. S. ibid. pg. 177.

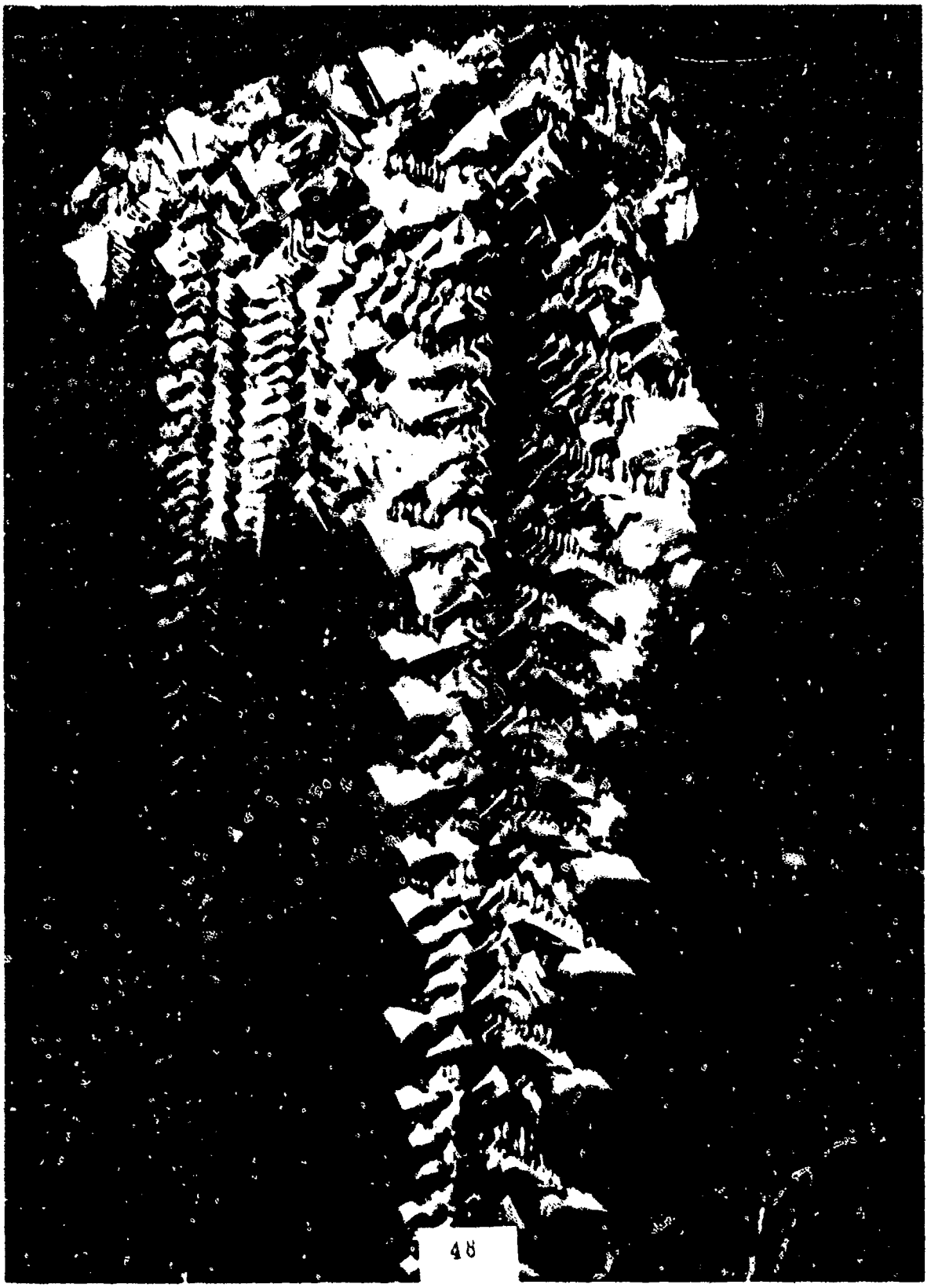
18. Jillson, D. C. and Hysell, R. E. ibid. pg. 187.

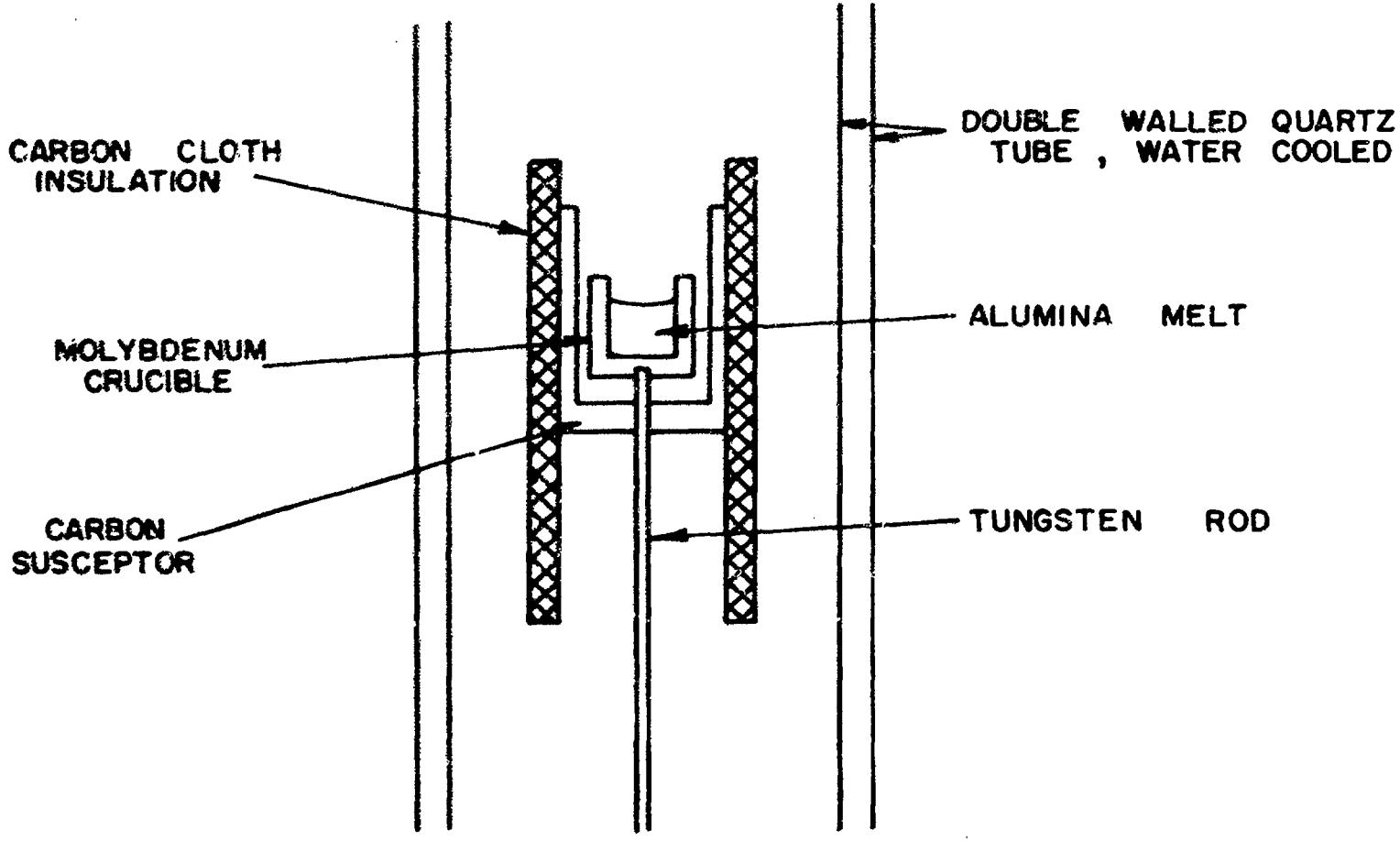
19. Gaule, G. K. and Pastore, J. R., ibid. pg. 201.

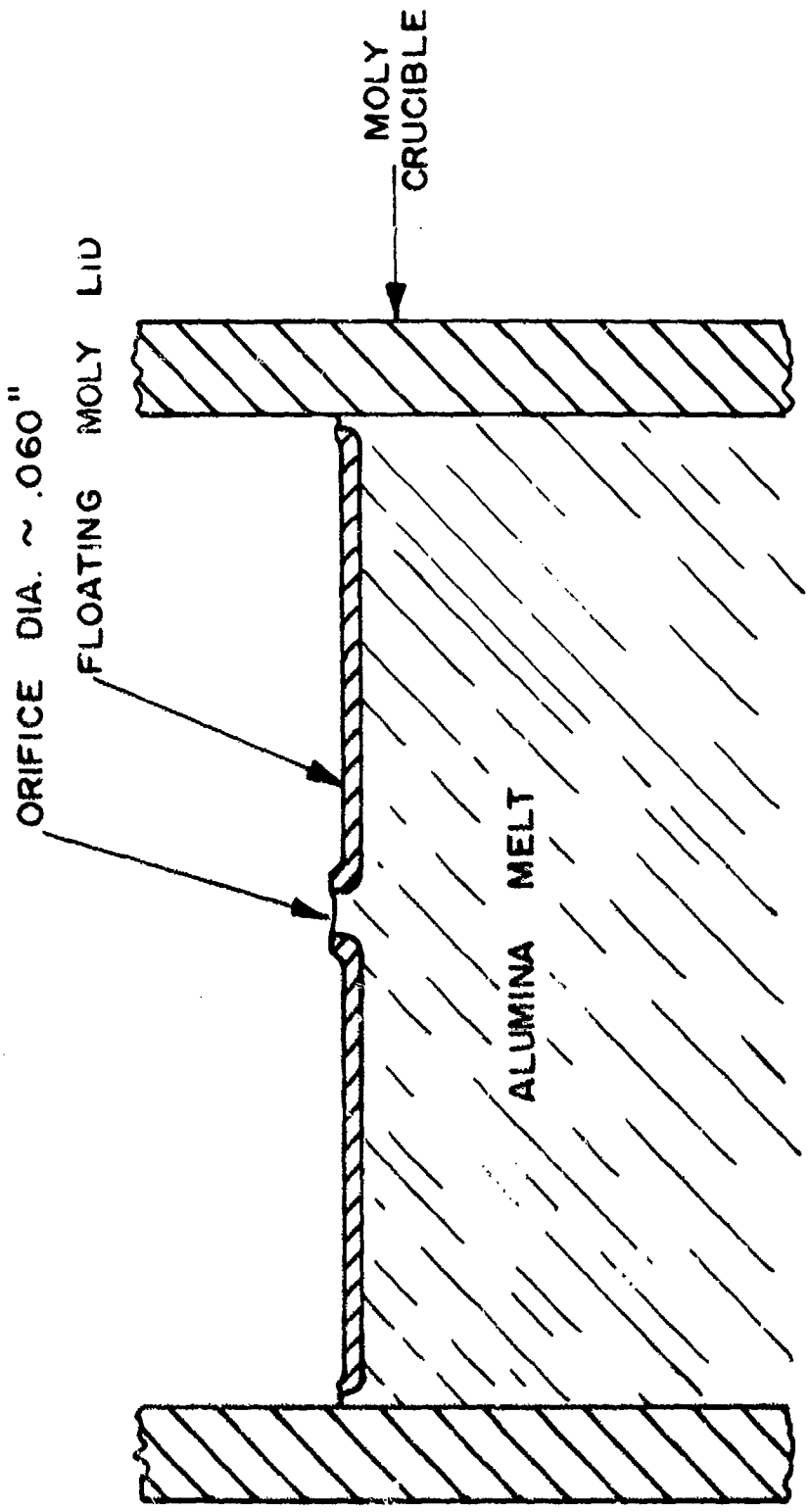
20. Boatman, J. C. and Goundry, P. C., J. Elec. Tech., 5, (1967) 98.

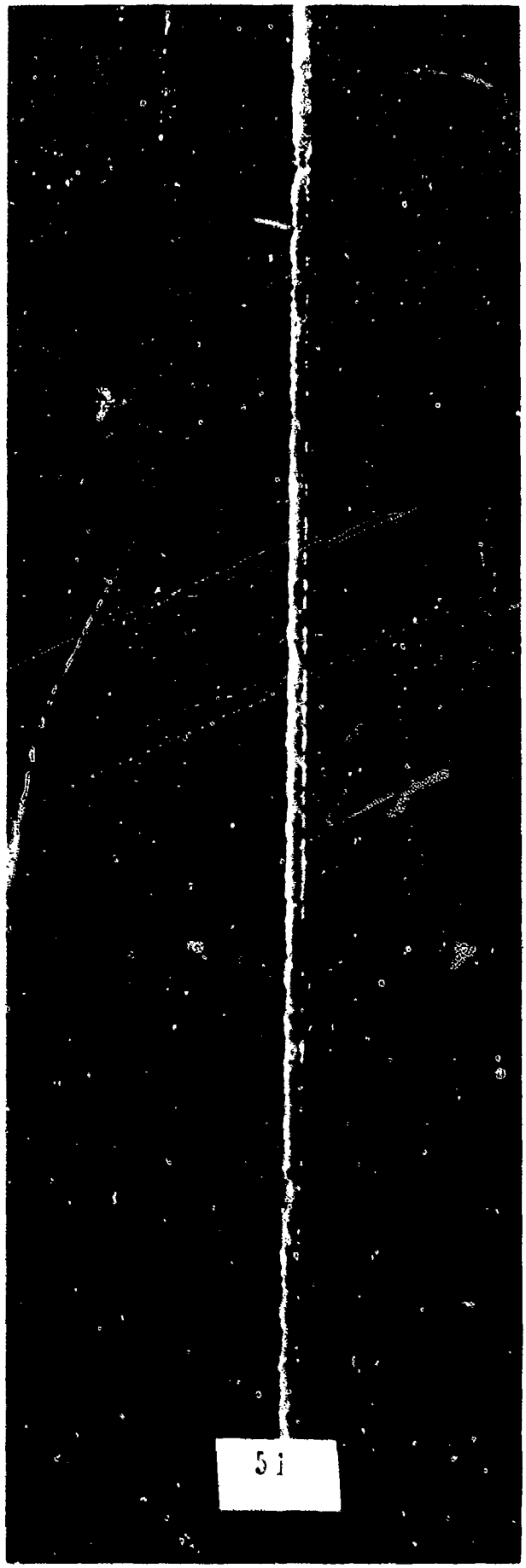
21. Swets, D. E., J. Elec. Tech. 5, (1967) 385.

## LIST OF FIGURES




CARBON CLOTH INSULATION
DOUBLE WALLED QUARTZ TUBE , WATER COOLED
ALUMINA MELT
MOLYBDENUM CRUCIBLE
CARBON SUSCEPTOR
TUNGSTEN ROD


MOLY
CRUCIBLE
FLOATING MOLY LID
ORIFICE DIA. ~ .060"
ALUMINA MELT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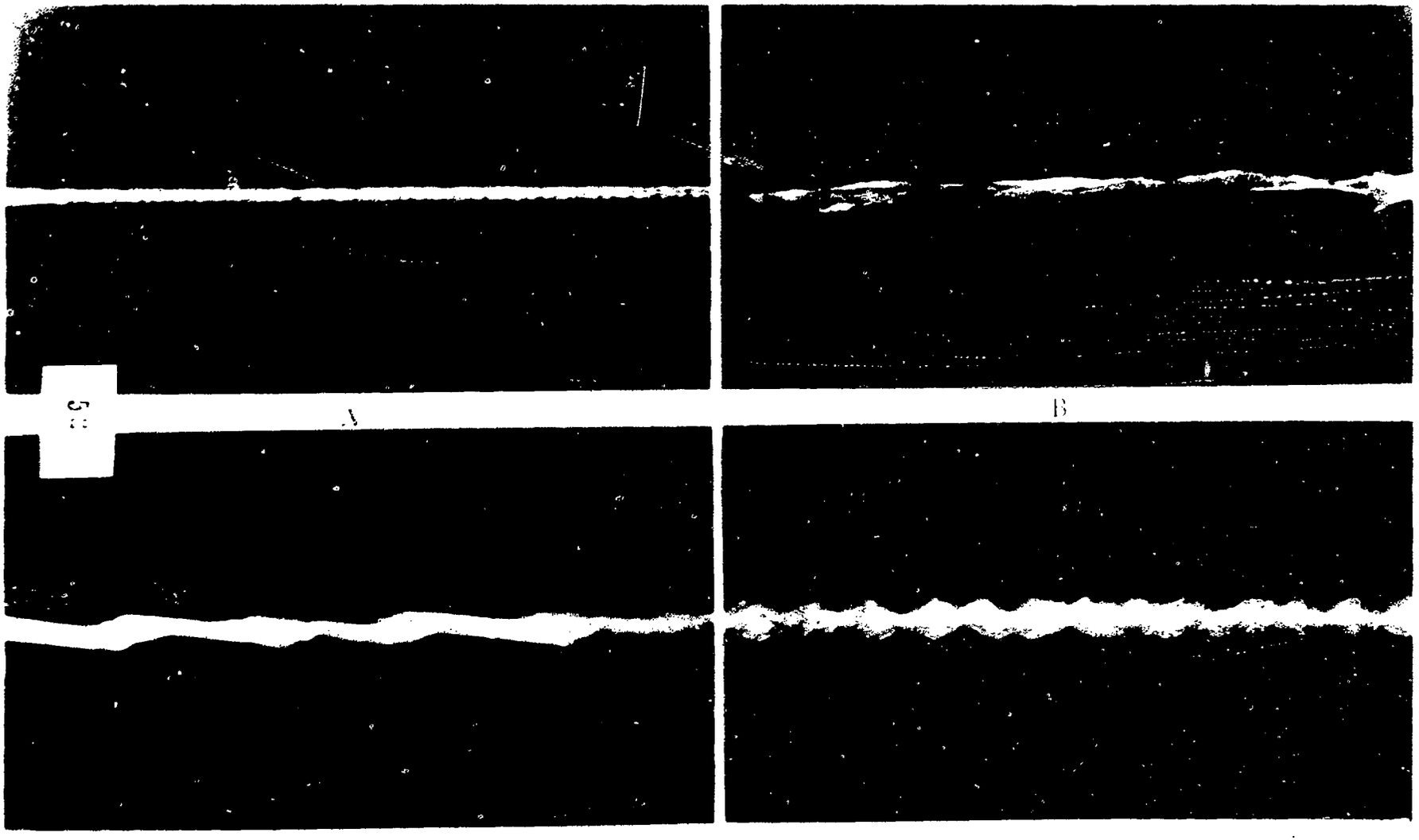
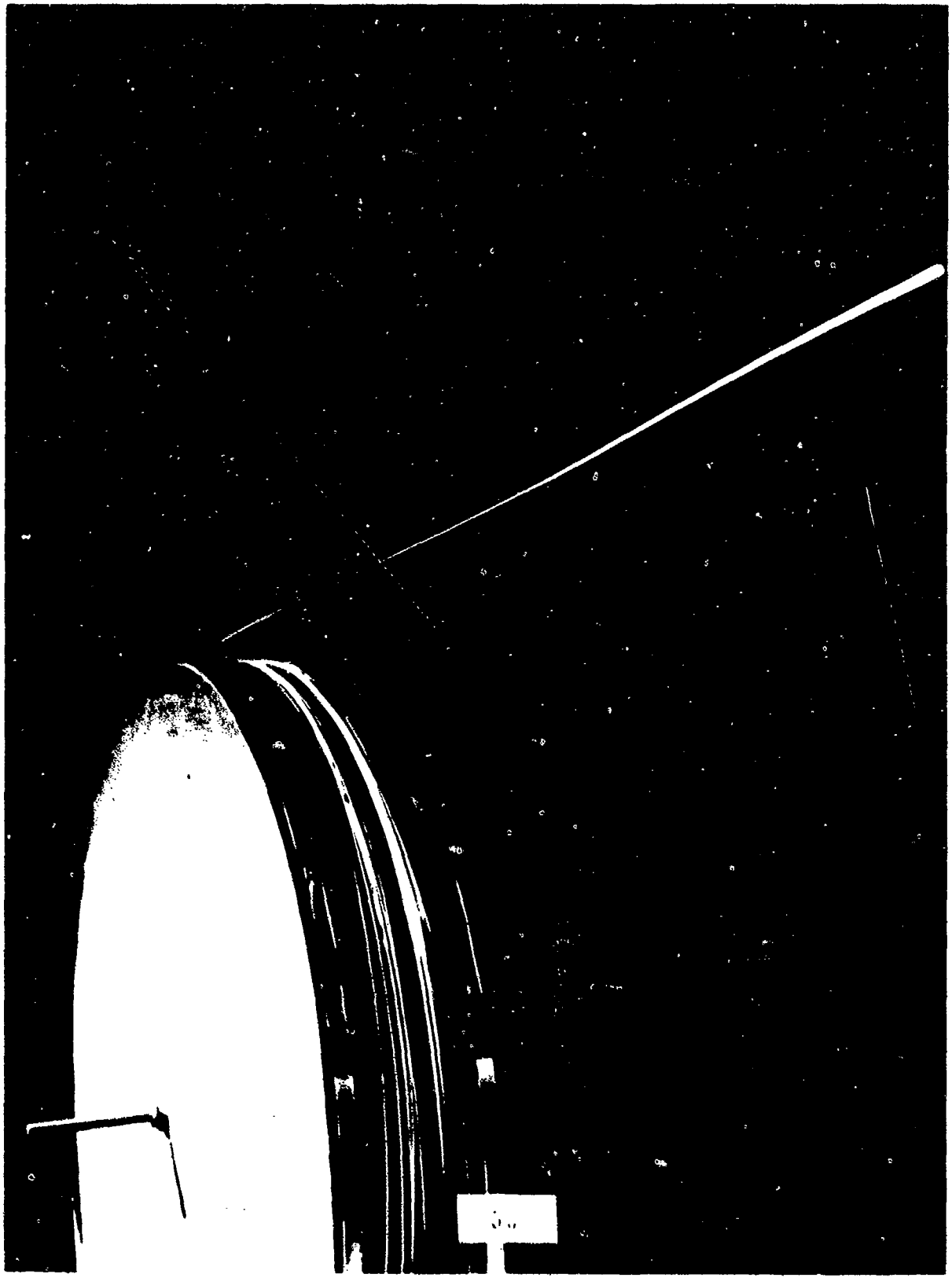
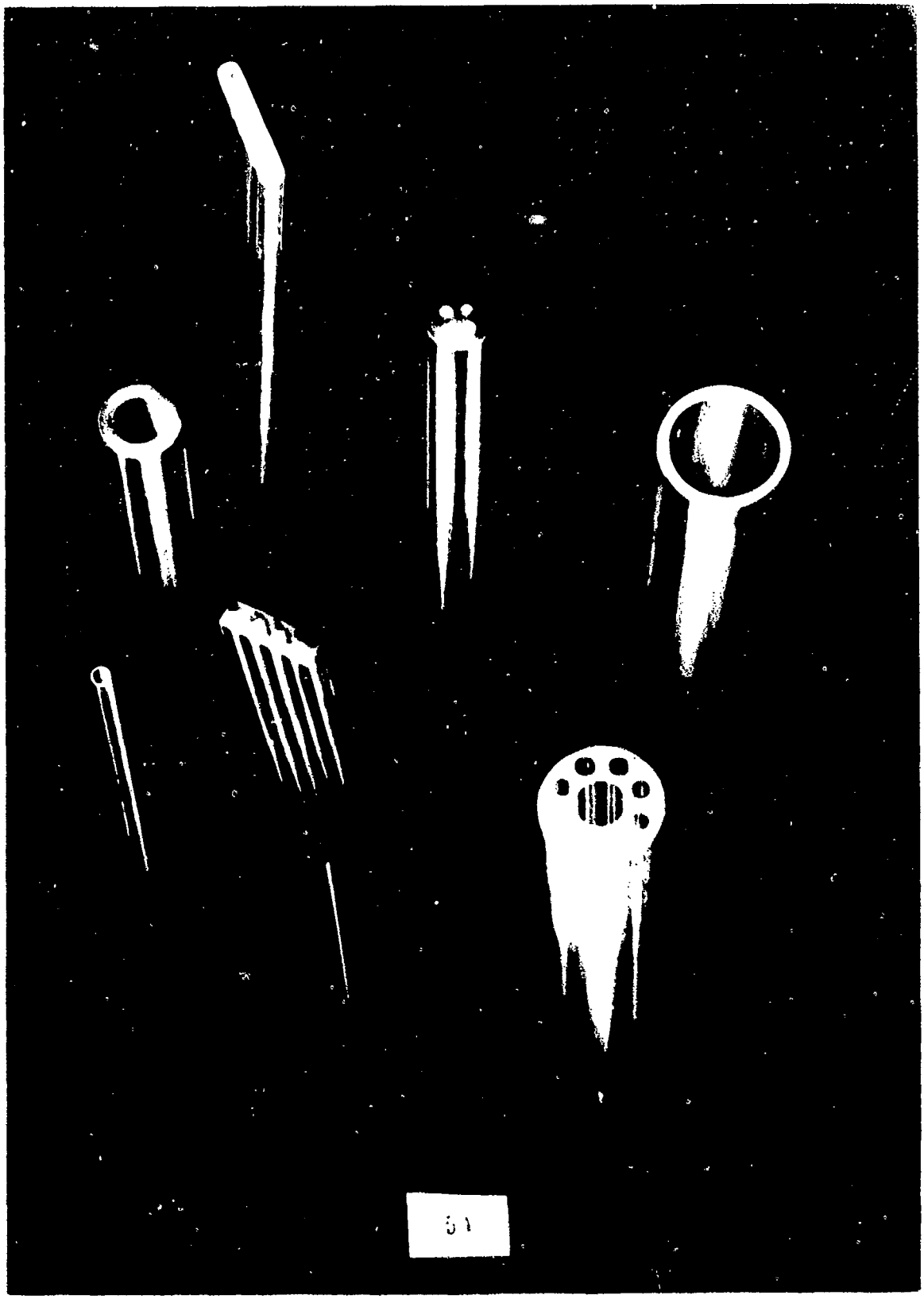

A
B

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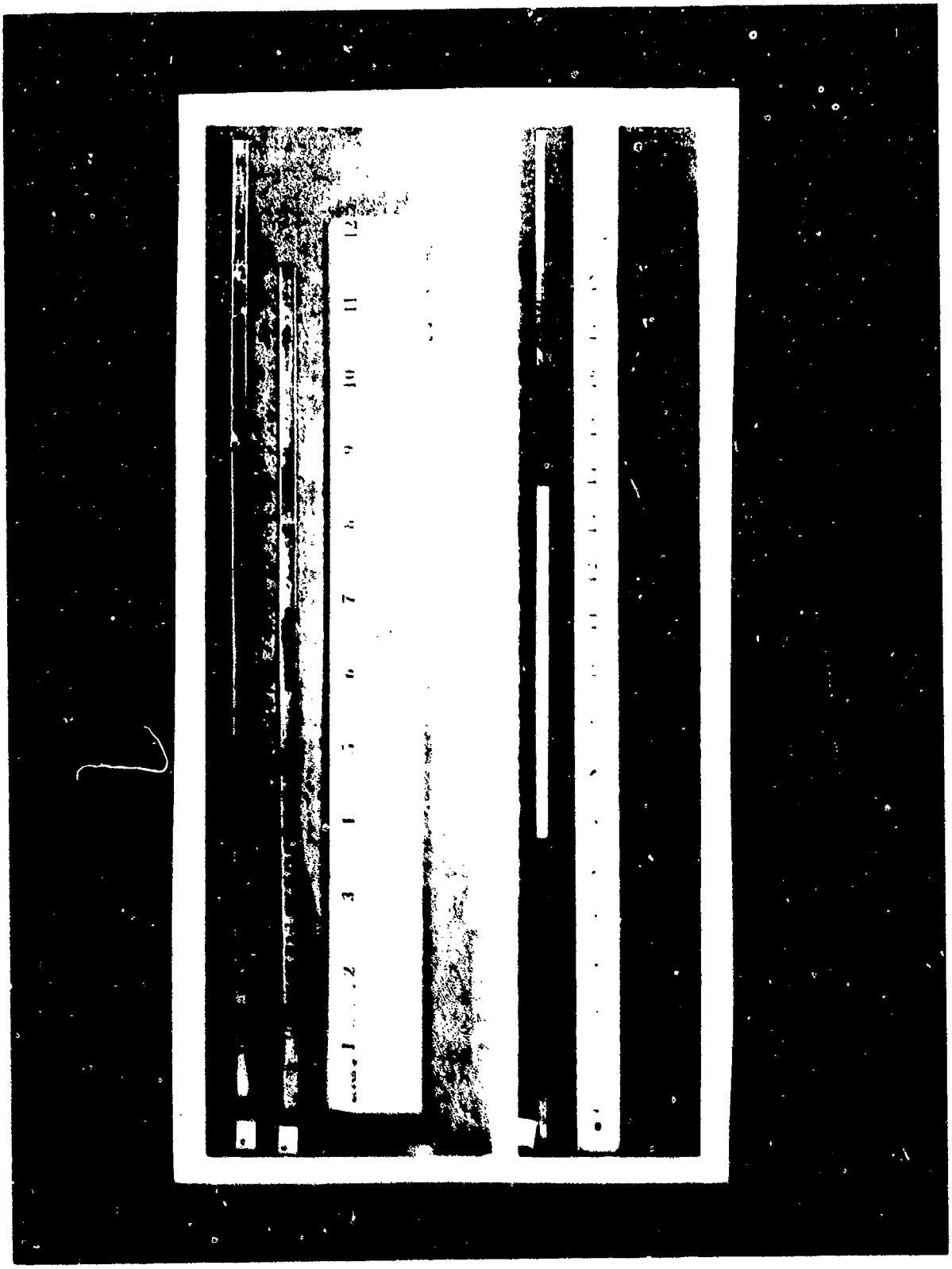

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DR. A. I. MLAVSKY, Vice-President; and Director, Corporate Technology Center

Dr. Mlavsky received a B. Sc. with First Class Honours in Chemistry (1950) and a Ph. D. in Physical Chemistry (1953) from Queen Mary College, University of London. His doctoral studies involved research on the sorption of organic vapors on liquid sulfur.

From 1953 until 1956, Dr. Mlavsky was on the scientific staff of General Electric Company, Ltd., and became involved in the emerging field of semiconductor metallurgy. His research led to many key innovations, including the development of the earliest techniques for both the crystal growth of silicon under vacuum conditions and the preparation of monocrystalline silicon with uniform chemical and physical properties.

After coming to the United States in 1956, Dr. Mlavsky joined the staff of Transitron Electronic Corporation where he conducted research on a wide variety of solid state problems. These included silicon crystal growth, the metallurgy of transistors, epitaxial crystal growth of silicon carbide, and the physics and metallurgy of transistors, epitaxial crystal growth of silicon carbide, and the physics and metallurgy of new thermoelectric materials and devices.

He joined the Materials Research Laboratory of Vestar, Inc., in 1960 to direct the company's research activities in energy conversion. Upon the incorporation of Tyco Laboratories (1962), he became a Vice-President; three years later he was elected to the Board of Directors of the Corporation.

Since 1966 Dr. Mlavsky has been responsible for coordinating the technical affairs of the company; he continues this function as Director of the newly formed Corporate Technology Center. Among

his most recent technological accomplishments have been the development of the "travelling solvent method" as a general technique for the crystal growth of compound electronic materials and the introduction of "auto-dendritic growth" as a means for preparing refractory materials in continuous single crystal form.

Dr. Mlavsky is a member of The Electrochemical Society, the Instrument Society of America, and the New York Academy of Sciences, His scientific publications and patents are as follows:

Control of the Properties of Single Crystal Silicon, "Semiconductors," Proc. of British Physical Society, (1956)/ The Evaporation of Impurities from Silicon, J. Electronics 2, 134 (1956)/ Epitaxial and Single Crystal Growth onto Silicon Carbide Seeds, in Silicon Carbide, Ed., O'Connor and Smiltens, p. 60, Pergamon Press (1960)/ Thermal and Electrical Properties of Some Silicides, in "Properties of Elemental and Compound Semiconductors," Ed. H. Gatos, p. 261, Interscience (1960)/ The Travelling Solvent Method of Crystal Growth, J. Electrochem. Soc., 108, 263C (1961); 109, 202C (1962)/ Bonding of Lead Telluride to Pure Iron Electrodes, Rev. Sci. Inst. 33, 1119 (1962)/ The Surface Barrier Photovoltaic Effect on Silicon, J. Electrochem. Soc. 109, 203C (1962)/ Measurement of Thermal Conductivity at High Temperatures, Adv. Energy Conv. 2, 23 (1962)/ Crystal Growth of GaAs from Ga by a Travelling Solvent Method, J. Appl. Phys. 34, 2885 (1963)/ Thermoelectric Properties of Pyrolytic Graphite, Bull. Am. Phys. Soc. 8, 337 (1963)/ The Voltage Breakdown of GaAs Abrupt Junctions, Appl. Phys. Letters 2, 97 (1963)/ Travelling Solvent Method of Crystal Growth, III. Grown P-N Junctions in SiC, GaAs, and GaP, J. Electrochem. Soc. 110, 56C (1963)/ Crystal Growth of $\alpha$-SiC from Various Chromium Alloys by a Travelling Solvent Method, J. Electrochem. Soc. 110, 185C (1963)/ The Growth of Single Crystal $SrTiO_3$ by a Travelling Solvent Method, Bull. Am. Ceram. Soc. 42, 529 (1963)/ Preparation and Properties of Epitaxial GaAs-GaP, GaAs-Ge, and GaP-Ge Heterojunctions, J. Electrochem. Soc. 111, 6 (1964)/ Growth of GaP Crystals and P-N Junctions by a Travelling Solvent Method, J. Appl. Phys. 35, 1892 (1964)/ Growth of $\alpha$-SiC Single Crystals from Chromium Solutions, J. Electrochem. Soc. 111, 805 (1964)/ Impurity Diffusion in $\alpha$-SiC P-N Junctions Grown by TSM, J. Electrochem. Soc. 111, 61C (1964)/ The Growth of Crystals by Solvent Zone Techniques - A Review, Intern. Conf. Crystal Growth, Nancy, France (1965)/ Dislocations in Gallium Arsenide Grown From Gallium by a Travelling Solvent Method, J. Appl. Phys. 37, 160 (1966)/ Radiant Energy Reactor

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Mr. LaBelle was employed by the Physical Science Laboratory of New Mexico State University from 1959 to 1960, where he was involved in computing wind effects on ballistic missiles. In 1961 he joined Raytheon to investigate the monocrystalline growth and electrical properties of thermoelectric materials.

Since joining Tyco Laboratories in 1962, his work has been closely connected with the development of single crystal growth by both the travelling solvent and travelling heater methods. Most recently, he has been instrumental in the development of growth techniques to produce continuous lengths of single crystal sapphire of various predetermined cross sections. Mr. LaBelle was recently awarded the Tyco Distinguished Technical Achievement Award for his work on continuous single crystal sapphire filaments. For his work in the same field, he also received the I-R 100 Award given by Industrial Research magazine to the developers of the 100 most important new product of 1967.

At the present time, Mr. LaBelle is Manager of the Saphikon (TM for Tyco sapphire) Division in the Corporate Technology Center. The activities in this Division include development and manufacture of sapphire crystals.

His publications and patents are as follows:

Dislocations in GaAs Grown From Gallium by a Travelling Solvent Method, J. Electrochem. Soc., 110, 185C (1963)/Growth of ZnO Single Crystals by a Travelling Solvent Zone Technique, J. Amer. Ceram. Soc., 48 (1965)/Dislocations in Gallium Arsenide Grown From Gallium by a Travelling Solvent Method, J. Appl. Phys., 37, 2913 (1966)/Growth of Sapphire Filaments From the Melt, Nature, 216, No. 5115 (1967)/Solution Growth of (Zn, Hg) Te and Ga(P, As) Crystals, Trans. AIME, 242 (1968)/Strength and Fracture ofLong Single Crystal Sapphire Filaments, submitted to SAMPE Journal, 1969.

Growth of Inorganic Filaments, U. S. Patent 3, 471, 266/Method of Growing Crystalline Materials, pending/Method of Apparatus for Growing Inorganic Filaments, pending/Growth of Inorganic Filaments, pending.

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# ION IMPLANTATION
## and Beam Technologies for LSI and Advanced Computers*

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## ABSTRACT

Ion implantation and beam technologies are beginning to demonstrate advantages in device and circuit processing for computer applications as well as other LSI and systems applications. More significant advances can be anticipated in the next few years because these technologies are still in their early years of development and some distance from their fundamental limitations.

This paper comprises a view of ion implantation and related beam technologies from the basic concepts of the techniques through current device and circuit production capabilities and applications and on into projected future applications and performance. Included are a tutorial review of ion implantation, a discussion of the advantages and unique features of ion implantation, and a discussion of some device applications from the research and development phase to production.

Some specific areas discussed which are related to computer applications are improved overall device and circuit resolution, device size, packing density, speed, and power consumption, automatic, computer-modifiable mask generation, and more vacuum processing steps.

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## INTRODUCTION

Charged particle beams have been receiving more attention recently for the fabrication and diagnostics of microelectronics devices and circuits and especially for LSI because it has become clear that the fundamental limitations on light and chemical techniques (photolithography and wet chemistry) have been or are rapidly being reached and that any significant advances now must come from the development of fundamentally different fabrication technologies. For example, the resolution and narrowest line which can be made using photolithography (1 μm) is limited by light diffraction in the projection aperture or the mask or by lens aberrations. The use of ion and electron beams will also be limited by diffraction and lens aberrations but at much lower magnitudes. For example, deflection-controlled electron beams have been focused to $\sim 10^{-3}$ μm and commercial electron beam systems which are being used to fabricate devices and circuits (as well as diagnose) have beam spots of $\sim 10^{-2}$ μm. With present electron resist techniques, lines as small as about 0.2 μm are being fabricated in device structures. Modest advances in techniques of employing electron resists combined with the uni-directional action of ion beam etching (micromachining) which causes no undercutting and of ion implantation doping which causes no spread of dopant under the mask, line sizes and resolutions for device elements and LSI should soon be below the 0.1 μm dimension. Fundamental particle beam limitations should not appear for at least another order of magnitude. Ion beam techniques (focusing lenses and scan systems) have not been pursued in the past to the degree of electron beams, but more attention is being given to ion beams now as the techniques of ion implantation and ion beam etching are demonstrating value as small device and LSI fabrication techniques. Scanned ion beams only as small as about 0.5 μm have been

made and the application for the equipment (e. g., ion microanalysis) does not yet lend itself easily to device and circuit fabrication. Commercially available equipment, suitable for device and circuit fabrication using tiny ion beams, may not be available for several years.

Looking to the future, we may envision the use of computer-controlled electron and ion beams, possibly combined in a single vacuum system, and used for the high resolution maskless fabrication and in situ testing of integrated circuits. In the near future, however, we are going to see beam techniques gradually combined with conventional processes where advantages are to be gained. While any all-beam/vacuum processing technology is more than five years away, the individual beam processes must be developed in parallel efforts to be able to meet the needs at the required time. A few government agencies, e.g., Naval Air Systems Command and Air Force Systems Command, and a few industrial organizations are cooperating to carry out such development. The ultimate result of these programs could be the development of a complete new technology for fabricating microelectronics devices and LSI arrays (for advanced computers and microwave systems among other applications) entirely by the use of beams – in vacuum, with improved yield, speed, packing density, power consumption, etc.

## ADVANTAGES OF BEAMS

Charged particle beams offer several important advantages over present photolithographic and chemical technologies. Because of these advantages, beam techniques are beginning to demonstrate substantial advances in semiconductor and microelectronics processing, LSI, higher frequency discrete devices, and improved yields and lower costs. Some primary advantages of charged particle beams which allow the advances are: 1) They can be focused to smaller diameters than light beams and therefore structures with smaller dimensions and higher edge resolution can be fabricated. 2) Their charged nature allows them to be deflected rapidly and precisely in two dimensions by electrostatic and/or electromagnetic fields which can be controlled by computer programming, allowing pattern writing which can be easily modified. 3) Their charged-particle nature also allows them to be accurately counted, leading to better control and reproducibility of the processes. 4) Processing steps which can be done by beams can be performed in vacuum. Vacuum processes are inherently cleaner and with associated mechanical handling, fewer human handling steps are required. The cleaner environment can be utilized properly to reduce imperfections and failures attributable to contamination of several forms.

## PHYSICAL PROCESS OF ION IMPLANTATION DOPING

In the process of ion implantation, atoms of the desired doping element are ionized and accelerated to high velocity and then caused to enter a substrate lattice by virtue of their kinetic energy (momentum). After the energetic ion comes to rest and equilibration has occurred, the implanted atom can be in a position in which it serves to change the electronic properties of the substrate lattice, i.e., doping occurs.

When high energy ions strike a target material, the resulting energy loss processes, particle trajectories, implanted impurity distribution, etc., are derived from the interaction mechanisms of the incident ions and the target atoms – individually in the case of amorphous materials, and also in ensemble of the target material exhibits crystalline (lattice) characteristics. A series of related one-atom-to-one-atom events may occur until the incident ion comes to rest, or a longer-duration encounter with the lattice may occur as part of the total stopping process for an ion. The model used to treat these dynamic phenomena requires the definition of two primary types of interaction – electronic collisions and nuclear collisions. Electronic collisions occur when the energy transfer occurs between the electrons of the incident and target atoms. These electrons may be excited to higher energy states or removed entirely (stripping) leading to further ionization. Nuclear collisions are the stronger electrostatic force (coulomb) interactions between the nuclei of the incident and target atoms. This is a repulsive force and can occur at a relatively large distance, resulting in a gentle deflection or it can occur at short range and be a violent collision. In the latter case, strong changes in direction occur and target atoms may be displaced. This displacement has no consequence in amorphous material, but in a crystalline target, it results in the creation of Frenkel

pairs - interstitial and vacancy pairs. These displaced lattice atoms or "primary knock-ons" can go on to create more Frenkel pairs. The products of this phenomenon - interstitials and vacancies, together with the stopped incident ion can interact with the lattice and with one another to cause a number of other effects, e.g., radiation damage (dislocation loops, precipation centers, vacancy-enhanced diffusion). These results can then have an effect on the interaction of subsequently incident ions and the complete problem becomes time dependent.

The surface damage can, to a certain extent, be continuously annealed out by maintaining the crystal at a high enough temperature that the displaced atoms can, by thermal motion, return to lattice sites before another ion subsequently arrives in the vicinity. This temperature is about 360 C for silicon for moderate ion bombardment rates (fluxes).

If a model of a crystal lattice is observed (see Fig. 1), channels and fairly open planes among rows of atoms can be seen in certain (crystallographic)directions. In other directions, the atoms of the lattice appear to have a random orientation and the cyrstal appears about the same at all points. Using this model, two substantially different kinds of interaction of incident ions with the lattice can be described which produce significantly different dopant distributions – the random or amorphous interaction and the channeling interaction.

A fraction of the ions in moderate current density beams, in which the ion trajectories are focused to be parallel with each other and with an open crystallographic direction (within $\lesssim 0.1^{\circ}$), impinging a crystal will penetrate deeply into the substrate lattice via channels (proper channeling) or via the space between lattice planes (planar channeling). This channeling process provides a means for creating deeper junctions or dopant profiles

without going to higher ion energies. On the other hand, channeling must be prevented in order to control profiles for shallow doping. Channeling allows ions to penetrate from 3 to 7 times deeper than the amorphous range. A relatively high current density beam (or a large dose at any density) can cause severe surface damage, to the extent that the surface region becomes amorphous (even if the beam is well aligned with a crystal direction), thus inhibiting channeling. A predoping bombardment by an inert ion beam can create an amorphous layer and prevent channeling. The problem of ion penetration through an amorphous layer has been treated analytically[1] and the total and projected ranges and the standard deviation can be calculated. The results for several ions in several substrates are shown as a function of ion energy in Fig. 2 and for a number of ions in silicon in Fig. 3. It is seen that the heavier ions (higher Z) will not penetrate as deeply as the lighter ions.

The effects described briefly above can result in any one or a combination of several types of profiles (volume dopant density versus depth into the crystal) as shown in Fig. 4. Referring to Fig. 4, the amorphous peak A or A' is generated by ions A' entering a crystal at random directions to the lattice direction, or by ions A in well-aligned trajectories, but which impact substrate atoms at the end of lattice rows. This amorphous distribution exhibits a Gaussian shape characterized by the mean projected range $R_p$ and standard deviation $\sigma$ (see insert of Fig. 2). The channeling peak C comprises ions whose trajectories are within the critical angle (see Fig. 4) of the crystal direction, and whose place of entrance into the crystal is greater than some minimum distance approximately the Thomas-Fermi radius ($\sim 0.1$ Å) from a lattice row; these ions lose energy by electronic collisions and channel to approximately the maximum range.

The shape of the channeling peak, which is 5 to 7 times deeper than the amorphous peak, is similar to the amorphous peak except that it falls more sharply on the high-energy side.

Ions entering the lattice with angles just greater than a critical angle, or aligned, but close to an atom row or encountering a channel-blocking particle, will be "dechanneled" before reaching the maximum range and will form intermediate or dechanneled region B. When dechanneling is predominant and only a few ions approach the maximum channeling range, a distribution such as C' results. An exponential channeling distribution (only fair channeling condition) can be exhibited (curve D Fig. 4). Ions which come to rest in either the amorphous or channeled regions where the lattice disorder is high and vacancies are abundant can diffuse (probably by pairing with vacancies or some type of defect) deeper into the undamaged crystal (beyond the maximum range), to form a low concentration "tail" on the distribution D.

While in the diffusion doping process, the diffusion temperature governs the surface solubility and diffusion constant, and combination with time determines the dopant depth, in ion implantation, the dopant distribution is determined by amorphous and channeling range-energy considerations and sometimes by vacancy-enhanced diffusion. The relative importance of these processes is determined by the ion dopant and substrate species, the ion energy, the substrate temperature, the substrate crystallographic orientation, the beam-substrate alignment, beam parallelism, and substrate surface conditions. The electrical nature of the dopant is determined by the position of the "ion" in the substrate lattice (substitutional or interstitial), by dislocation trapping, by clustering, and by vacancy-ion, oxygen-ion, or intrinsic impurity-vacancy pairing.

For fabricating devices, one is interested in the distribution, the mobility, and the activation energy of the electrically active species. Phenomena influencing these properties are dissociation of clusters and crystalline regrowth of the damaged substrate region during annealing, migration of dopant species from interstitial to substitutional sites, a different annealing characteristics for different dopant species.

Lattice damage caused by bombarding ions can be both advantageous and disadvantageous. Damage by heavy ions introduces vacancies, interstitials (both substrate and dopant), precipitation centers, recombination centers, and shifts in Fermi levels. On the positive side, bombardment damage creates vacancies which dopant ions can fill substitutionally, and it may allow enhanced "vacancy" diffusion effects. On the negative side, bombardment damage may produce electrically active defect centers and interstitial ions (both dopant and substrate) which may complicate the electrical behavior; subsequent aggregation of point defects into stable complexes, e.g., dislocation networks, may result. Interstitial atoms of either species produced by bombardment damage may block the lattice channels and interfere with channeling experiments or prevent the formation of a doping profile based on channeling phenomena. While the maximum ion range may not be decreased by bombardment dose (damage), the dopant distributions may be greatly altered; the greater the dosage, the more the distribution is shifted toward the surface.

For ion-implanted semiconductor materials, the temperatures required to anneal bombardment damage and to produce the maximum number of electrically active dopants are lower than diffusion temperatures in the same materials. The required anneal or activation temperatures must be investigated for each ion dopant-substrate material combination. These

temperatures in Si are often between 400 and 1000 C for material implanted at room temperature. For some substrates implanted at elevated temperatures, lower anneal temperatures have been shown to be required. For example, the active dopant concentrations for Sb in Si and for Zn in GaAs decrease slightly with increasing anneal temperature for material implanted hot (~ 500 C). This effect may indicate supersaturation. An increasing dependence of electrical activity on temperature has been observed for many other ion-substrate combinations.

If energetic ions are to be used to dope substrate materials, then how do we mask against them? Four masking techniques are: 1) exposed resists, 2) passivation/protection layers (e.g., oxides/nitrides), 3) metal device contacts or special thin films, and 4) contact metal masks. A fifth way precludes masks altogether – the use of tiny, programmed ion beams. This technique is illustrated in Fig. 5. An ion beam can be focused to a small diameter, blanked, and deflected by computer-programmed varying potentials to write patterns. This concept is the subject of a program sponsored by Naval Air Systems Command.

## ADVANTAGES OF ION IMPLANTATION

A few ion implantation research programs were begun about seven years ago. Since then many organizations have entered the field and expanded the breadth of investigation. Device development programs have grown from these in an effort to capitalize on the advantages found. Today the process has advanced to the point of being used in integrated circuit production. Certain advantages offered by the process have thus been clearly proved; others are still being demonstrated in the laboratory, and some are just being uncovered by research.

Advantages (together with some limitations), regardless of their degree of demonstration, are listed in the several pages of Table I. The uses to which these advantages are being put and some of the meaningful results are also listed in some cases. Most of the advantages can be grouped under two main ones: the nonthermal nature of the process - meaning ions can be implanted in any substrate at any temperature, and the charged-particle nature of the ions.

The last item of Table I is a potential limitation of ion implantation - the difficulty in controlling the ion channeling phenomenon. Three methods of preventing or decreasing channeling are illustrated in Fig. 6.

While the choice of dopant species for diffusion doping is limited by the solubility and diffusibility (diffusion coefficient) of the dopant in the substrate material, the choice of dopants for ion implantation is potentially unlimited because ions of any element in the periodic table can be generated and implanted in any substrate material. Ion implantation is not an equilibrium process; ions can be injected in concentrations exceeding thermal equilibrium or solubility. However, not all of these implanted ions will necessarily become electrically active, and interstitial and substitutional

active doping must be distinguished. Ion implantation can be advantageously used to dope certain materials with species which have suitable solubilities but which are slow diffusers in the material.

Ion implantation allows better junctions to be made in high temperature materials like SiC and therefore allows improved high-temperature devices to be fabricated. Diffusion doping in SiC requires temperatures exceeding 2000 C, making the use of masks difficult. Doping SiC by ion implantation is superior because vacancies are caused by the damage which can be filled by dopant atoms, whereas in the thermal techniques, high temperatures are required to generate sufficient vacancies for diffusion to occur. SiC has been successfully doped n-type by ion implantation. In materials that decompose at low temperatures (like GaAs or CdTe), diffusion temperatures may be above the substrate decomposition temperatures. Because ions can be implanted at any temperature, doping can be performed below decomposition temperatures. Annealing of damage and dopant activation can then be carried out up to the maximum tolerable temperatures. In some cases, such as CdTe, these anneal temperatures may still be low enough that complete activation is difficult to achieve.

Doping profiles (including junction locations) can be controlled in a known manner (determined by experimental investigation) if the required control and stability of ion beam parallelism, beam-substrate orientation (alignment), ion energy, and anneal temperature is provided. One of the keys to controlled profiles is the control of the existence or magnitude of channeling of ions in preferred crystallographic directions and of the phenomenon of enhanced diffusion.

Because ions can have rather definite ranges in amorphous or crystalline substrates, as determined by their energy and the substrate

orientation (more so than for diffusion), large area junctions of uniform depth can be produced by controlling beam parallelism over large area. Submerged junctions can be created by causing the dopant profile peak to rise above the substrate doping level at a distance below the surface. The implanted peak can still rise orders of magnitude above the substrate doping level (see Fig. 7).

If sufficiently high energy ions are employed, junctions can be formed beneath oxide or other passivating layers. However, other deleterious effects may occur, such as damage or conductivity changes in the passivating layer, introduction of impurity centers, creation of charge centers and surface states, and surface charging effects. Gradually the effects on the electrical properties of structures formed by doping through passivating layers are being learned and techniques are being found to control the effects.

An oxide layer causes only a small decrease in the maximum range of ions corresponding to that predicted (calculated) for the energy loss in traversing a thin amorphous oxide layers; but it can have a greater influence on the dopant distribution (profile) when channeling is employed to produce larger dopant concentration deeper in the substrate. The oxide layer causes dechanneling and shifts in the dopant concentration toward the surface. Normal handling procedures and vacuum conditions probably result in approximately 20 Å of oxide on Si surfaces, which will have little effect, but passivation layers (> 3000 Å) will have a significant effect.

Problems will be caused in ion implantation doping by the presence on the substrate surface of dust particles or spots of oxide or other contamination, including background vapors and condensed oil vapor or other system fluids. Nonuniformities, pipes, and other junction imperfections

may result, leading to junction shadowing or shorting. Careful handling procedures and good vacuum environments and techniques have been shown to make these potential problems negligible.

The use of deflected, small diameter (~0.5 to 200 μm) ion beams offers the advantage of doping predetermined localized substrate regions without the use of masks and the accompanying wet chemistry and photolithography processes. Patterns and arrays of doped regions can be considered for fabrication in vacuum. The low temperature nature of ion implantation allows the use of evaporated metal or oxide masks directly for doping when masks are desired, in comparison to the more limited use of high temperature masks and wet chemistry associated with diffusion doping processes.

Fabrication of $N^+$ and $P^+$ high concentration layers on surfaces or in very localized regions for contact metallurgy can be achieved by low-energy ion implantation because higher dopant concentrations can be achieved than by the equilibrium process of diffusion. In some cases, ions of a desired species can be implanted in materials for contacts which could not be done at all by diffusion techniques. For contact formation, all implanted ions need not be electrically active, only present in the metallurgical sense. Therefore almost arbitrarily large concentrations can be achieved.

When a sequence of doping steps are desired, ion implantation is advantageous for interchangeability of doping steps because subsequent doping steps do not influence previous ones. Earlier ones, however, may influence later ones if some of the bombardment damage introduced is not entirely annealed out. Proper treatment may avoid this problem.

Conceptually, junctions of almost any desired depth can be formed by ion implantation doping by varying and controlling the ion energy. Low ion energy or matching of ion energy with oxide layer thickness may be employed to produce shallow junctions. Large total dosages of ions can provide high doping concentrations in such shallow depths, something which is difficult or impossible by diffusion techniques.

## DEVICES FABRICATED BY ION IMPLANTATION

Many of the devices which researchers have tried to make or to improve using ion implantation are listed in the four pages of Table II. The advantages of ion implantation described in the preceeding section are noted on the right-hand side in many cases. In some cases achieved device performance data are also shown. In some cases, reasonable goals for near future performance are included. The primary categories of devices are microwave, MOS and integrated circuits, photodiodes, and transistors. The last group, the non-active elements, e.g., resistors and contacts are certainly not the least important applications of ion implantation. They are finding wide spread application.

A current application of ion implantation to an integrated circuit is illustrated by the 2048-bit read-only memory in which the memory pattern is created by selective ion implantation to activate the desired MOS devices. This implantation is carried out as the final processing step, using a resist mask; thus the uncoded circuits can be made and stored prior to coding. The memory pattern could be written with a small programmed ion beam (i.e., without a mask) when this technology is sufficiently developed. This circuit exhibits a 100 nsec cycle time, comprises 3000 MOS devices, and is contained on a 0.100" x 0.100" chip.

An example of a device which employs to advantage ion implantation in combination with the other beam techniques of electron-beam pattern fabrication and ion beam etching is a junction field effect transistor switch (JFET). The fabrication of this device is described briefly to show an example of what combined beam technologies may be doing in the future.

The development of large, electronically scanned radar systems has generated a need for low control power microwave switches. Hughes is

currently developing junction field effect transistor devices characterized by small dimensions of the drain and source terminals to obtain a low parasitic resistance with the minimum possible parasitic capacitance. In fact, the dimensions are such that standard optical masking techniques are inadequate and electron-beam exposure and fabrication techniques are required to obtain the desired resolution. Once the proper pattern is exposed in the photoresist by the electron beam, the drain and source fine interdigitation are formed (doped) by ion implantation through an ion beam etched thin metal mask. Devices have been built and tested. Control power requirements are roughly two orders of magnitude less than required by other devices as p i n diodes.

In this device the source and drain are diffused into the epitaxial layer which acts as gate. The device conductance is increased by extending the source and drain electrodes by means of an array of interlocking fingers which are fabricated starting with electron beam exposure of resist which covers a gold layer. The developed resist is used as a mask against ion beam sputtering to define the finger pattern in the gold, which is then used as a mask for implantation of the fingers into the epitaxial layer. The finger pattern and an enlargement (scanning electron microscope picture) of the fingers are shown in Fig. 8. The implanted fingers are about 1.3 μm wide, with an edge resolution of 0.1 - 0.2 μm. A single device involves a finger pattern about 0.4 mm square, with 1180 fingers; the total beam-on time was 118 seconds. More details of the fabrication of this structure can be found in an article by Wolf et al.[2]

Another potential benefit of the smaller devices and interconnect lines possible be electron beam techniques is in higher device density of LSI arrays. Figure 9 shows a plot of component density versus time taken

from Brewer.[3] The dots were derived from Phillips et al for bipolar devices; the triangles represent present or projected MOS devices. An upper limit for optical techniques (based on minimum line width of 2 μm) as calculated from the bipolar device model used by Phillips et al, is shown by the dashed line. The triangle in the upper right corner of Fig. 9 was calculated using a model of an MOS device, based on a minimum line width of 0.5 μm which should be possible by electron beam techniques. A similar value of component density would result from the use of 0.5 μm in the bipolar model equation. While many challenging technical problems associated with other complementary process steps and the real economics of beam processes remain to be determined (e.g., can an economical batch process be developed to retain the resolution capability of a single field exposure), the potential benefit of this new technology in LSI systems appears substantial. For example, smaller, close-packed devices result in faster circuit operation; the speed-power product is increased. Lower area per device should result in higher yield, which increases exponentially as the area is reduced.

The density of implanted ions which is necessary to produce the desired electrical properties of the substrate (semiconductor) and device characteristics varies from $\sim 10^{11}$ to $10^{15}$ ions/cm$^2$. For a required dose of $\sim 10^{14}$/cm$^2$ and an ion current of the desired species at the target of $\sim$ 10 μA distributed uniformly over an area of $\sim$20 cm$^2$ (a 2-in. wafer), an implantation time of $\sim$ 30 sec is required.

The number of ions implanted is seen to correspond roughly to one monolayer on the crystal surface. Ion implantation systems and ion sources must therefore be capable of delivery to the target a current on the order of 10 μA of the desired ion species. The ions desired are generally those which

will become substitutional donors of acceptors in the crystal. The types of ions required and the modest energies required are therefore the main factors which differentiate the ion implantation system technology from much of the prior ion beam generation work.

TINY ION BEAM PROGRAM*

As discussed above, ion beams can be focused to small diameters and can be deflected rapidly and accurately over a target surface which could be microelectronics circuitry. This is a vacuum process which can conceptually be automated, computer-controlled, and combined with other beam processes.

If ion beams can be generated and focused to a small enough spot while carrying sufficient current, they can be used in a programmed manner to achieve ion implantation doping without the use of masks. An indication of the expected spot diameter can be obtained, as shown in Fig. 10. The parameters chosen are indicated in the figure. The spherical and chromatic aberration coefficients are chosen to be higher than the value commonly used for electron beams to be appropriate for electrostatic lenses which are required to focus ions. The source current density $J_s$ is assumed to be 0.1 $A/cm^2$, which is compatible with higher current density ion sources (e.g., duoplasmatrons ) but is high for present day lower-energy electron impact ion sources. The 100-kV ion energy is representative of medium mass ions for simple present applications. These current density and aberration parameters are difficult, but not impossible to achieve in practice. A minimum spot diameter around 1 μm is predicted for realistic values of ion beam current ($10^{-9}$ to $10^{-8}$ A); smaller spots can probably be achieved with reduced beam currents. It is seen that the effect of chromatic aberration is not important in the case studied here and that the diffraction limit ($d_d$ in the electron beam chart) will not appear in the ion beam sizes

* Supported in large part by Naval Air Systems Command

desired. This curve suggests however, that with improved sources of dopant-type ions and good electrostatic lenses and power supplies, a tiny programmed ion implantation beam is achievable.

The 300-kV research implantation system in which the experimental aspects of this program will be carried out is shown schematically in Fig. 11 and in the photograph of Fig. 12. This system is also typical of general research systems in which the work discussed earlier is performed.

## MANUFACTURING METHODS FOR ION IMPLANTATION*

As discussed above, some devices and circuits made to advantage using ion implantation have progressed to the production stage. An example are p-channel MOS integrated circuits. This work is being performed in the MOS Division of Hughes Aircraft Company at Newport Beach, California. The goal of this 2-year program is to convert ion implantation from a proved laboratory technique to a reliable and economical manufacturing process for p-channel MOSFET integrated circuitry.

Prior to this program, Hughes had carried out the necessary research and advanced device and system development to such a stage that the laboratory feasibility of ion implantation doping as a semiconductor device and circuit process step had been well demonstrated. Prototype MOSFET samples had been furnished to Hughes systems for test, including some for the Air Force AMSA system and several for various experimental Hughes systems developments. These implanted devices had shown such superior performance compared with diffused devices that the response from users had been enthusiastic and quantity production requirements for system use had been established. The technology of ion-implanted silicon MOSFET devices at Hughes had advanced to the point where it was necessary that serious consideration be given to manufacturing technique development in order to meet needs for systems.

Under this program, a manufacturing ion implantation system was designed and constructed, specifically optimized for the p-channel MOSFET class of device. The system was designed with consideration of reliability,

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* Supported in large part by the Manufacturing Technology Branch of the Air Force Systems Command

safety, ease of maintenance, and economy of manufacturing processes. A target chamber was developed to allow more than 20 2-in.or 3-in.wafers to be implanted for each pump down. The target chamber and beam transport and handling system were designed to be compatible, to have a short cycle time, and to be operated easily by a production worker at a rate of at least 150 wafers per day. The implantation cycle is under automatic control.

The implantation system will be used extensively for implantation of devices and integrated circuits under manufacturing conditions. Manufacturing techniques for implanted devices are to be developed which are compatible with present planar MOS technology. Life tests will be performed on certain of the implanted circuits appropriate.

A photograph of this production implantation system is shown in Fig. 13. Table III is a list of specifications of this system. With several hundred circuits on each wafer, the wafer rate corresponds to a production capacity of over $10^7$ per year. For comparison, the characteristics of a more versatile Hughes implantation system for device development are shown in Table IV.

## CONCLUSIONS

Ion implantation and beam technologies are beginning to demonstrate advantages in device and circuit processing for computer applications as well as other LSI and systems applications. More significant advances can be anticipated in the next few years because these technologies are still in their early years of development and some distance from their fundamental limitations. Some specific areas discussed which are related to computer applications are improved overall device and circuit resolution, device size, packing density, speed, power consumption, automatic computer-modifiable mask generation, and more vacuum processing steps.

## REFERENCES


1. J. Lindhard, M. Scharff, and H. E. Schiøtt, Mat. Fys. Medd. Dan. Vid. Selsk. 33, No. 14 (1963).

2. E. D. Wolf, L. O. Bauer, R. W. Bower, H. L. Garvin, and C. R. Buckey IEEE Trans. on Electron Devices ED-17, 446 (June 1970).

3. George R. Brewer, "The Application of Electron/Ion Beam Technology to Microelectronics," Submitted to IEEE Spectrum.

TABLE I

ADVANTAGES OF ION IMPLANTATION - 1

NONTHERMAL PROCESS

- DOPE ALL MATERIALS/PROCESS AT ANY APPROPRIATE TEMPERATURE

  LEADS TO NEW CLASSES OF DEVICES
  LOW TEMPERATURE MATERIALS (e.g., CdTe, InAs)
  HIGH TEMPERATURE DEVICES (e.g., in SiC, GaAs).

- CAN EXCEED SOLID SOLUBILITIES OR DIFFUSION RATES

  MAKE NEW MATERIAL (THIN LAYERS) e.g.
  TAILORED BAND-GAP MATERIALS (e.g., GaAlAs, PbSnTe)

- BETTER DEPTH UNIFORMITY AND CONTROL – e.g., → NO MICROPLASMAS

  LEADS TO HIGHER PERFORMANCE DEVICES
  HIGHER YIELDS - LOWER COSTS

- MASKED BY ANY DENSE MATERIAL – INCLUDING LOW TEMPERATURE, e.g.

  RESISTS, ALUMINUM, THICK PASSIVATION LAYERS, DEVICE CONTACTS
  SELF ALIGNED GATE STRUCTURES → HIGHER SPEED MOS e.g.
  PERFECT REGISTRATION → BETTER YIELD AND COST

- INTERCHANGEABILITY OF DOPING AND PROCESSING STEPS

  LEADS TO GREATER CIRCUIT FLEXIBILITY
  SEVERAL DEVICE TYPES ON WAFER
  USE OF METALLIZATIONS FOR MASKING
  LOWER COSTS

## ADVANTAGES OF ION IMPLANTATION - 2

### CHARGED-PARTICLE NATURE OF BEAMS.

- ABILITY TO COUNT ATOMS INTRODUCED - LEADS TO BETTER CONTROL OF CONCENTRATIONS AND REPRODUCIBILITY
- EASILY VARIABLE OR PROGRAMMABLE ENERGY - DIRECTLY RELATED TO DEPTH

  MORE ABRUPT JUNCTION DEVICES
  SUBMERGED JUNCTION DEVICES
  SHALLOW, HIGH-CONCENTRATION REGIONS
  FLAT CONCENTRATION REGIONS

  See Fig ___

- DIRECTIONALITY OF BEAM/DOPANT - LEADS TO LITTLE LATERAL SPREAD

  SHARPER DEVICE EDGES
  NARROWER OR SMALLER DEVICE DIMENSIONS
  GREATLY REDUCED OVERLAP CAPACITANCE → HIGHER SPEED

- DOPING POSSIBLE THRU PASSIVATION LAYER

  LEADS TO PRE-PASSIVATED DEVICES WITH REDUCED LEAKAGE
  BETTER YIELD AND PERFORMANCE

- ABILITY TO FOCUS TO MICRON OR SUBMICRON SIZES AND DOPE

  WITH NO LATERAL SPREAD, ALLOWS SMALLER DEVICES →
  HIGHER FREQUENCY DEVICES AND
  HIGHER DEVICE PACKING DENSITIES

- ABILITY TO DEFLECT IN A PROGRAMMED MANNER

  MASKLESS CIRCUIT/DEVICE FABRICATION STEPS
  ELIMINATION OF SOME WET CHEMISTRY AND PHOTOLITHOGRAPHY STEPS →
  LOWER COST, HIGHER YIELD
  COMPUTER-PROGRAMMED CIRCUIT FABRICATION STEPS →
  QUICK, EASY, INEXPENSIVE CIRCUIT MODIFICATION

- VACUUM PROCESS

  CLEANER PROCESSING STEPS / LESS HUMAN HANDLING →
  HIGHER YIELDS → LOWER COST

## ADVANTAGES OF ION IMPLANTATION - 3

### ASSOCIATED BOMBARDMENT DAMAGE

CREATION OF LOCALIZED VACANCIES

| | |
|---|---|
| BY DOPANT: | HIGHER ELECTRICAL ACTIVITY IN CONTROLLED REGIONS AT LOWER ANNEALING OR PROCESSING TEMPERATURES |
| BY INERT IONS: | CONTROLLED VACANCY-ENHANCED DIFFUSION → PROFILE CONTROL AND FLEXIBILITY |

### POTENTIAL LIMITATIONS

DIFFICULT OR IMPOSSIBLE FOR SOME ION/SUBSTRATE COMBINATIONS TO:

- EXCEED SOLID SOLUBILITY
- ACHIEVE FULL ELECTRICAL ACTIVITY AT LOW ANNEALING TEMPERATURE
- REMOVE ALL DAMAGE IN EASILY-DAMAGED MATERIALS FOR HIGH DOPING → FORMATION OF VACANCY CLUSTERS, DISLOCATION LOOPS, PRECIPITATION CENTERS, CHANNEL BLOCKING
- PREVENT JUNCTION MOVEMENT DURING ANNEALING
- COMPLETELY PREVENT CHANNELING - POOR CONTROL OF JUNCTION LOCATION AND CONCENTRATION AT LOW CONCENTRATIONS

## TABLE II

## DEVICES FABRICATED USING ION IMPLANTATION - 1

### MICROWAVE DEVICES

- **IMPATT DIODES**
- **TRAPATT DIODES**

CONTROLLED, ABRUPT, UNIFORM JUNCTION DEPTH IN THIN EPI LAYERS →

HIGHER FREQUENCY, BETTER THERMAL CONDUCTIVITY → COOLER OPERATION AND HIGHER OUTPUT POWER

IMPATT: 1 W @ 60 GHz, 14%
TRAPATT: 1.5 W @ 4 GHz, 21%

- **p i n SWITCHING DIODES**

LOW TEMPERATURE PROCESSING OF HIGH-ρ MATERIAL

INCREASE OF 10 IN RECOMBINATION LIFETIME → 10 x FORWARD RESISTANCE → LOWER RF LOSSES
$V_B$ of 500 V

- **JFET SWITCH**

NARROW FINGERS (1 μm) → INCREASED CHANNEL CONDUCTANCE
SLIGHTLY HIGHER FREQUENCY
MUCH LOWER INPUT POWER ($10^{-2}$)
INCREASED YIELD
APPLICATION TO LARGE, ELECTRICALLY SCANNED RADAR SYSTEMS

- **VARACTOR AND MIXER DIODES**

PROFILE FLEXIBILITY
CONTROLLABLE C vs V

## DEVICES FABRICATED USING ION IMPLANTATION - 2

### MOS DEVICES AND IC's

- **SHIFT REGISTERS**
  - HIGHER FREQUENCY (30 MHz +)
  - LOWER CLOCK VOLTAGE (15 V)
  - LOWER INPUT POWER
  - HIGH VOLTAGE OPERATION $V_{SD}$ to 200 V
- **PRE-SELECTED THRESHOLD CMOS**
  - SHIFTS OF OVER 4V
  - LOWER THRESHOLDS TO < 1 V
  - CONTROL THRESHOLDS TO ± 0.1 V
  - II - LOW DOSE THRU OXIDE TO CHANNEL - NOT CONVERTED
- **MEMORIES**
  - READ ONLY
  - RANDOM ACCESS
  - READ/WRITE
  - ADDRESSABLE (ASSOCIATIVE)
  - SELECTIVE DOPING - EASILY CHANGED PATTERNS BY COMPUTER PROGRAM
  - LARGER ARRAYS AT GIVEN SPEED BECAUSE LOWER CAPACITANCE AND HIGHER PACKING DENSITY
  - LOWER POWER
  - I/O MILLER CAPACITANCE ~0 $C_{gs}$ ~ 1/4
  - STORED INFORMATION WRITTEN BY IMPLANTING DRAINS AFTER CHIP PROCESSED

## DEVICES FABRICATED USING ION IMPLANTATION - 3

| | |
|---|---|
| ● PHOTODIODES<br>SILICON<br>GaAs<br>IR DETECTORS | LARGE-AREA, UNIFORM JUNCTIONS - NO MICROPLASMAS<br>IMPROVED S/N RATIO - IR DETECTORS<br>GOOD GaAs DOPING → GAINS > 300 |
| ● BIPOLAR TRANSISTORS<br>SILICON<br>GaAs | HIGH GAIN-BANDWIDTH (9 GHz CUTOFF, 8dB POWER, 4 dB NOISE)<br>BETTER BASE WIDTH PROFILE CONTROL (B BASE, As EMITTER)<br>THIN (0.05 μm) AND REDUCED BASE RESISTANCE (MANY TIMES LOWER THAN DIFFUSED)<br>ELIMINATION OF PUSH-OUT IN n-p-n |
| ● SiC FET | HIGH TEMPERATURE DEVICES (n in p ONLY) AT LOW TEMP. + ANNEALING (1000 to 1500 C) |
| ● ELECTROLUMINESCENT DIODE | GaAlAs - FORMATION OF TERNARY CPD. LAYERS<br>BAND GAP TAILORING (Al → GaAs, THEN Zn →) |
| ● VIDICONS<br>GERMANIUM (p ONLY)<br>SILICON | LOW TEMP. PROCESSING BETTER THAN DIFFUSION IN Ge<br>DAMAGE ALSO p-TYPE, BETTER UNIFORMITY |
| ● SOLAR CELLS | NOT SUPERIOR TO DIFFUSED |

## DEVICES FABRICATED USING ION IMPLANTATION - 4

- **ACOUSTIC AMPLIFIERS**
  - LAYERED
  - MONOLITHIC

  SHALLOW N REGIONS → LOW THERMAL GENERATION POTENTIAL TO DOPE PIEZOELECTRIC MATERIALS

  N-TYPE IN SELECTED REGIONS → MORE EFFICIENT AMPLIFICATION AND MONOLITHIC ACOUSTIC CIRCUITRY

### NONACTIVE ELEMENTS

- **RESISTORS**

  DOPING CONTROL AND HIGH YIELD
  HIGH $\rho_s$, NARROW LINES
  $\geq 10^4$ Ω/□ AND ≃ 20 MΩ → $10^8$ Ω

- **CONTACTS**

  ANY ION/SUBSTRATE COMBINATION
  LOW TEMPERATURE PROCESS
  SHALLOW HIGH CONCENTRATION
  TRANSPARENT TO IR RADIATION, etc.

- **PRE DEPOSITIONS**

  CONTROLLED OXIDE DOPING PRIOR TO DIFFUSION

## TABLE III

## MOS PRODUCTION SYSTEM

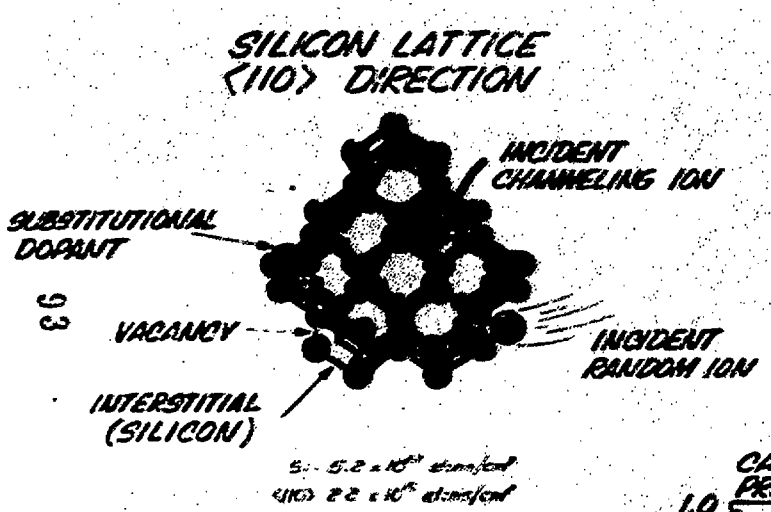
| | |
|---|---|
| Dopant Species: | Boron (phosphorus) |
| Substrates: | ~ 40 2-in. wafers; up to 4" diam. wafers<br>~ 25 3-in wafers; any mixture of pieces |
| Ion Energy: | 20 to 120 keV (20 to 250 keV ($P^{++}$) ) |
| Dopant Depth: | 0.1 to 1 μm (0.1 to 0.6 μm) |
| Beam Current: | 0.1 to 10 μA |
| Dopant Purity: | mass separation → B only from $BCl_3$ (P only from $PF_5$) |
| Dose Range Capability: | $2 \times 10^{11}$ to $10^{15}$ ions/$cm^2$ |
| Doping Uniformity and Reproducibility: | ~ ± 2% |
| Substrate Temperature: | Ambient |
| Vacuum.: | ≤ $2 \times 10^{-6}$ Torr reached in < 10 min. |
| Wafer Rate: | 1000 to 2000/week at $10^{14}/cm^2$, ~$10^4$/week at $10^{12}/cm^2$ |
| Capital Cost Per Circuit: | < ~ 1¢ (3 years) |

FIGURE CAPTIONS

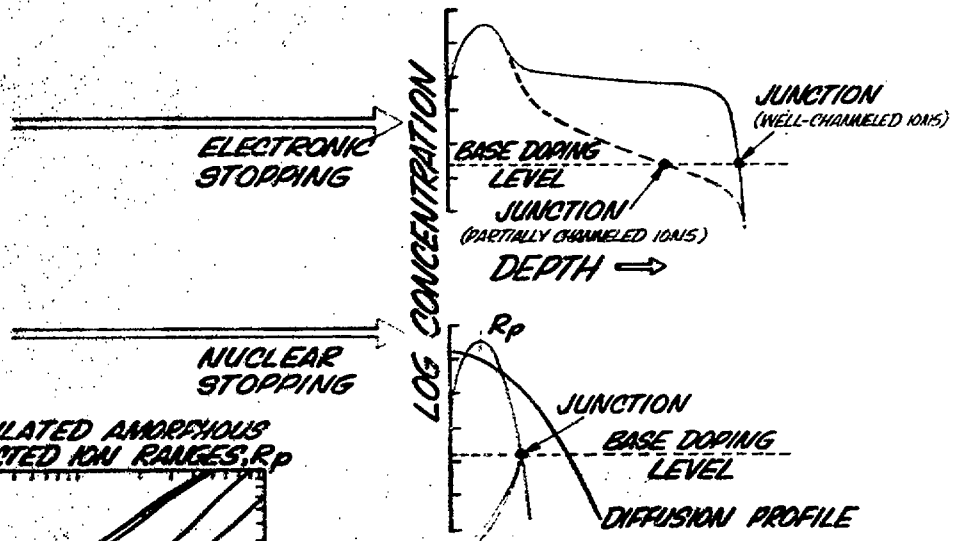
1. Model of silicon lattice
2. Range-energy relationship of several ions in several substrates.
2. Range-energy relationship for ions in silicon.
4. Ion implantation dopant distributions and lattice interactions.
5. Tiny, programmed ion beam circuit fabrication concept.
6. Methods of preventing or decreasing channeling.
7. Ion implantation junction profiles.
8. The exposure of resist by an electron beam to form windows in a gold mask by ion beam etching through which active fingers are ion implanted to make a high conductance FET device shown.
9. Plot of the evolution of component density of an LSI array versus time. The potential increase in component density by the use of a tiny electron beam is shown in the upper right; this point illustrates only the higher resolution pattern capability of the electron beam technique.
10. Calculated spot diameter versus convergence angle for an ion beam.
11. 300-kV research implantation system — schematic.
12. 300-kV research implantation system — photo.
13. MOS production implantation system.

# ION IMPLANTATION DOPING

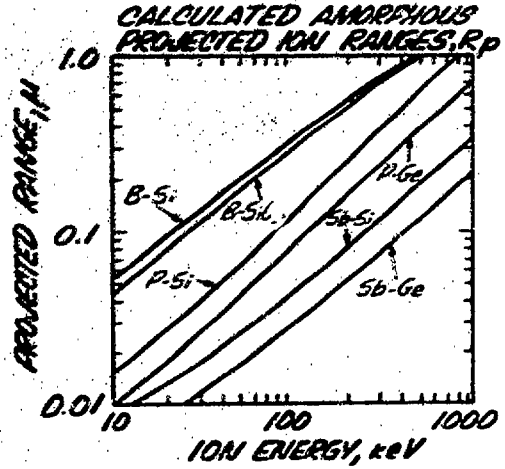
## ● DOPANT METHOD

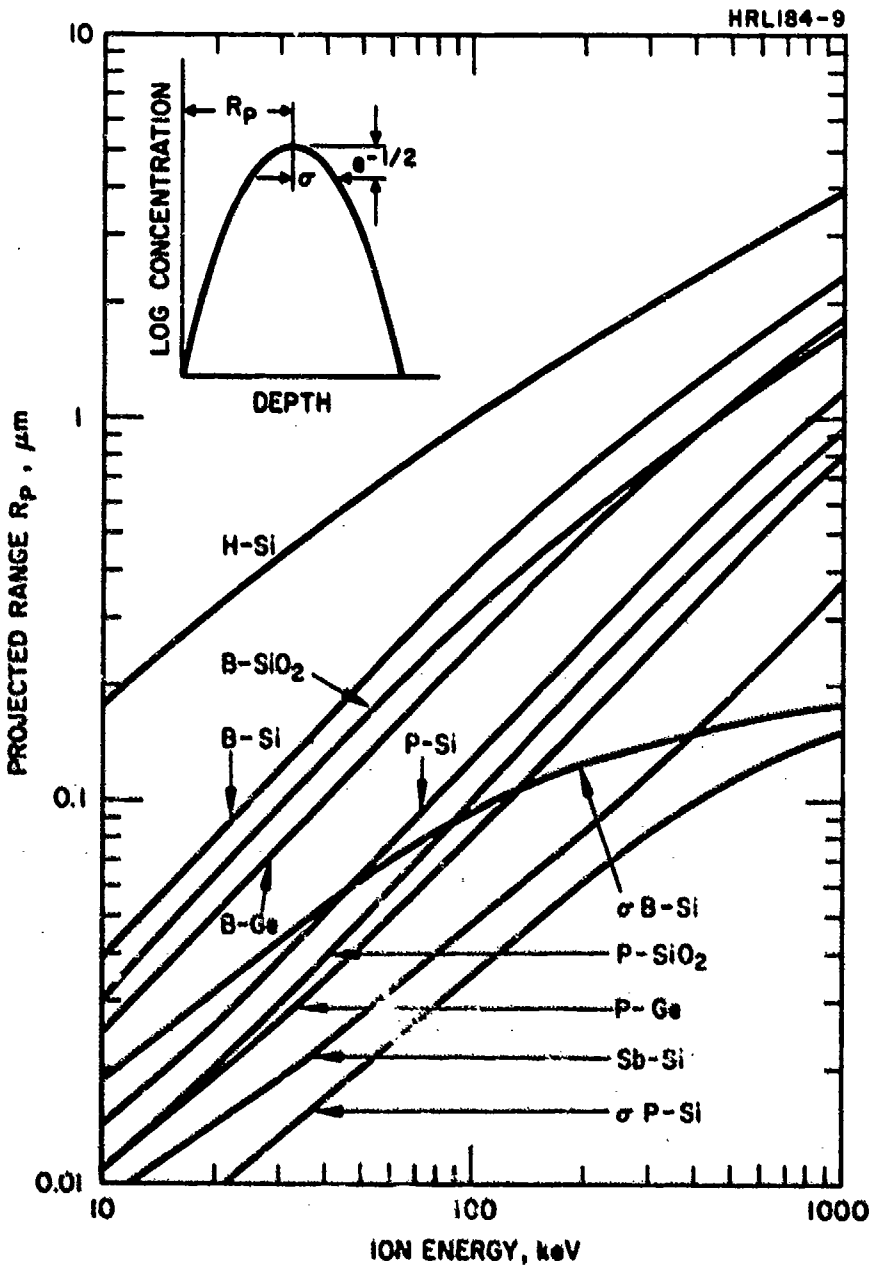


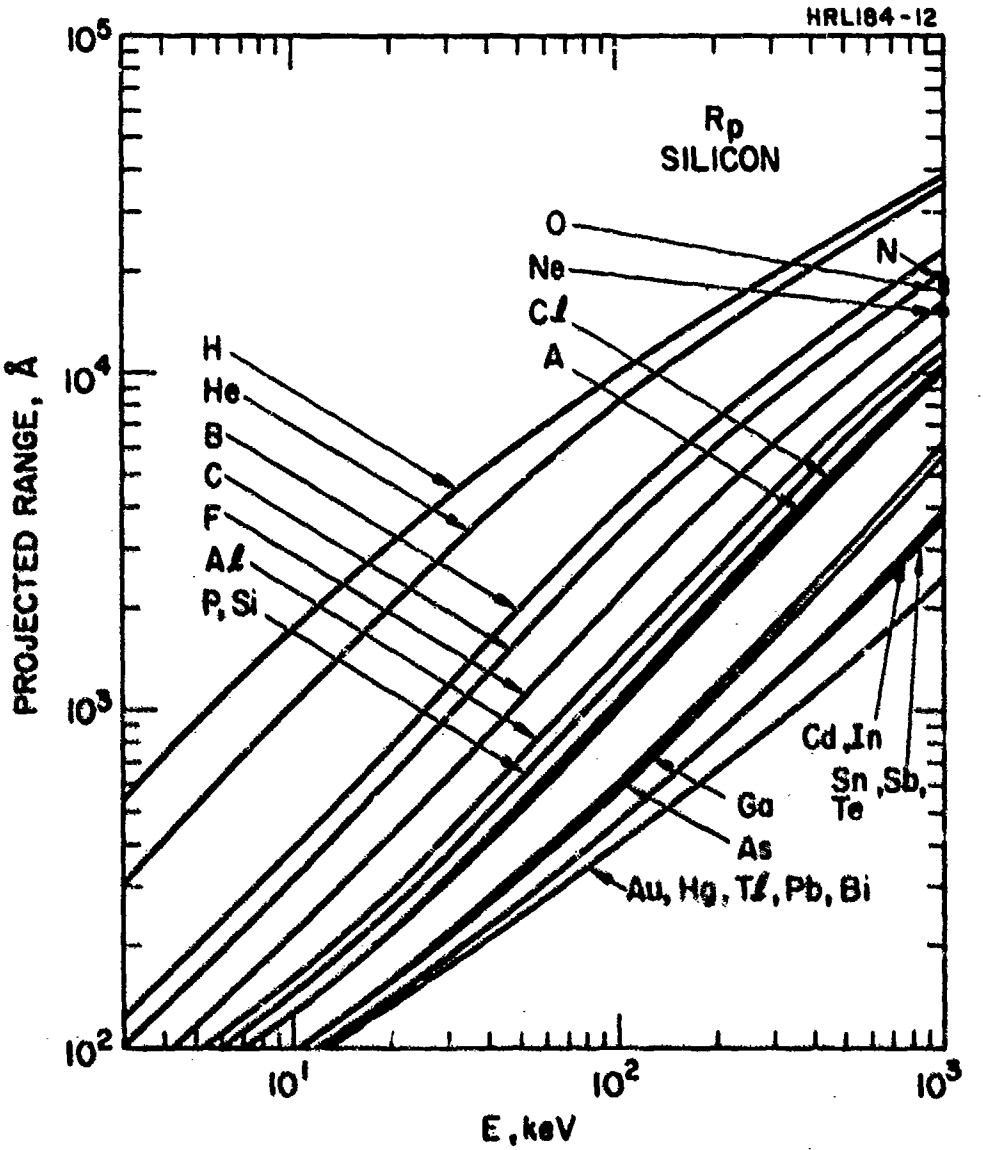

## ● DOPANT DISTRIBUTIONS

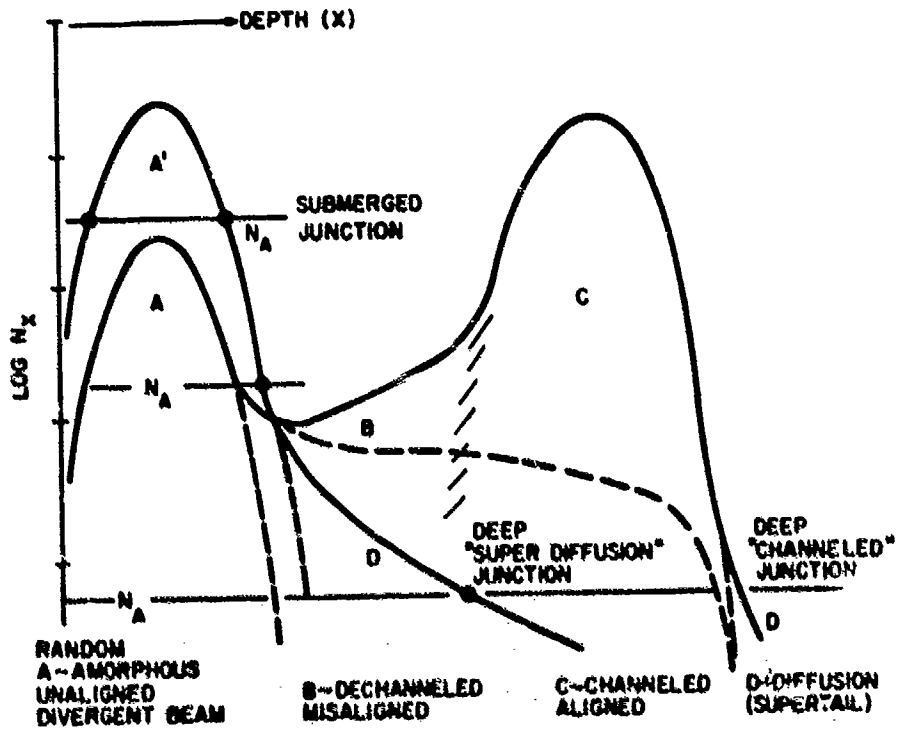


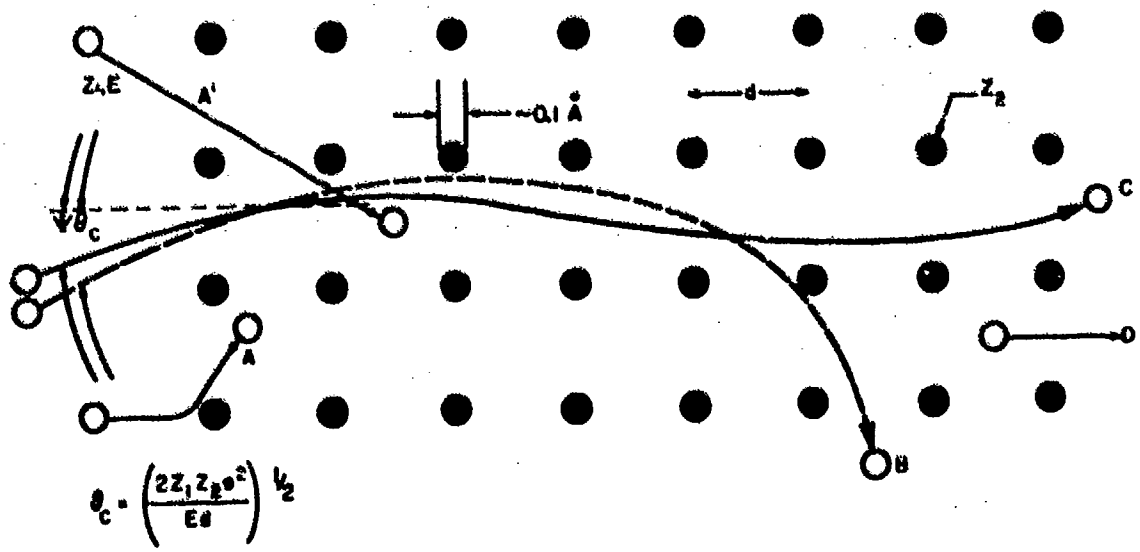

## ● DOPANT DEPTHS

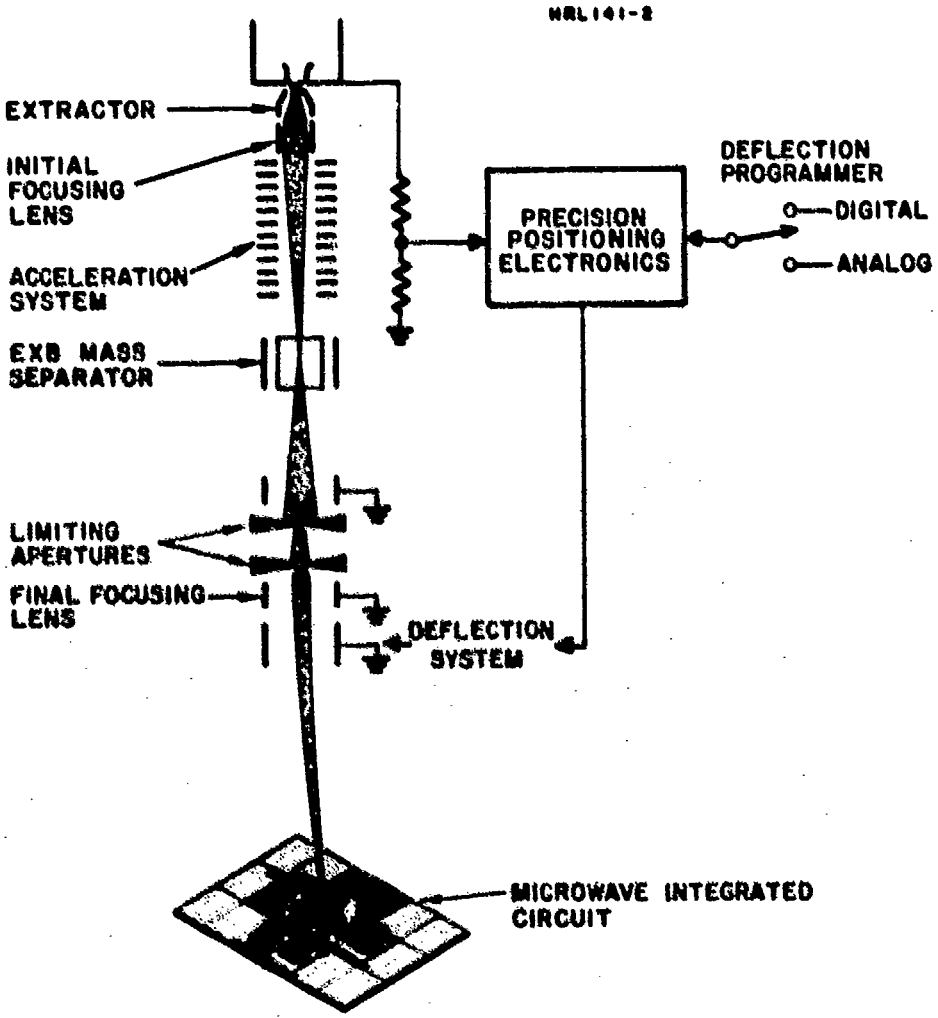


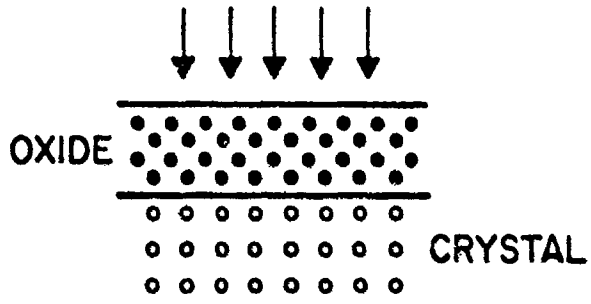

HRL184-9
10
1
0.1
0.01
PROJECTED RANGE $R_p$ , μm
LOG CONCENTRATION
$R_p$
σ
$e^{-1/2}$
DEPTH
H-Si
B-SiO$_2$
B-Si
P-Si
B-Ge
σ B-Si
P-SiO$_2$
P-Ge
Sb-Si
σ P-Si
10
100
1000
ION ENERGY, keV


HRL184-12
$R_p$
SILICON
PROJECTED RANGE, Å
E, keV
$10^5$
$10^4$
$10^3$
$10^2$
$10^1$
$10^2$
$10^3$
O
Ne
Cl
A
N
H
He
B
C
F
Al
P, Si
Cd, In
Sn, Sb, Te
Ga
As
Au, Hg, Tl, Pb, Bi

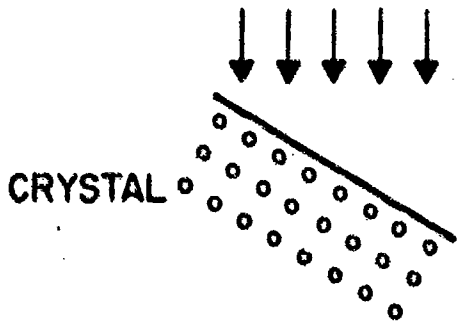

DEPTH (X)
LOG $N_x$
A'
A
B
C
D
$N_A$
SUBMERGED JUNCTION
DEEP "SUPER DIFFUSION" JUNCTION
DEEP "CHANNELED" JUNCTION
RANDOM
A~AMORPHOUS
UNALIGNED
DIVERGENT BEAM
B~DECHANNELED
MISALIGNED
C~CHANNELED
ALIGNED
D~DIFFUSION
(SUPERTAIL)


$Z_1E$
A'
~0.1 Å
d
$Z_2$
$\psi\theta_c$
C
A
D
B
$\theta_c = \left(\frac{2Z_1Z_2e^2}{Ed}\right)^{1/2}$

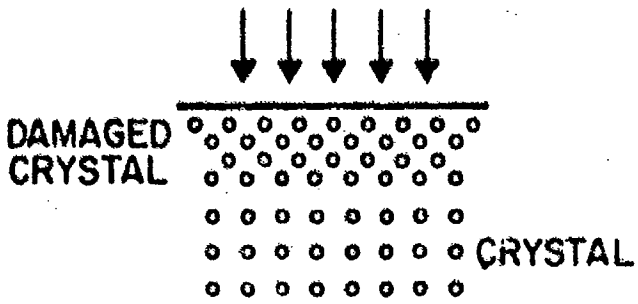

NRL 141-2
EXTRACTOR
INITIAL FOCUSING LENS
ACCELERATION SYSTEM
EXB MASS SEPARATOR
LIMITING APERTURES
FINAL FOCUSING LENS
DEFLECTION SYSTEM
PRECISION POSITIONING ELECTRONICS
DEFLECTION PROGRAMMER
DIGITAL
ANALOG
MICROWAVE INTEGRATED CIRCUIT




(a) IMPLANT THROUGH AN AMORPHOUS OXIDE LAYER

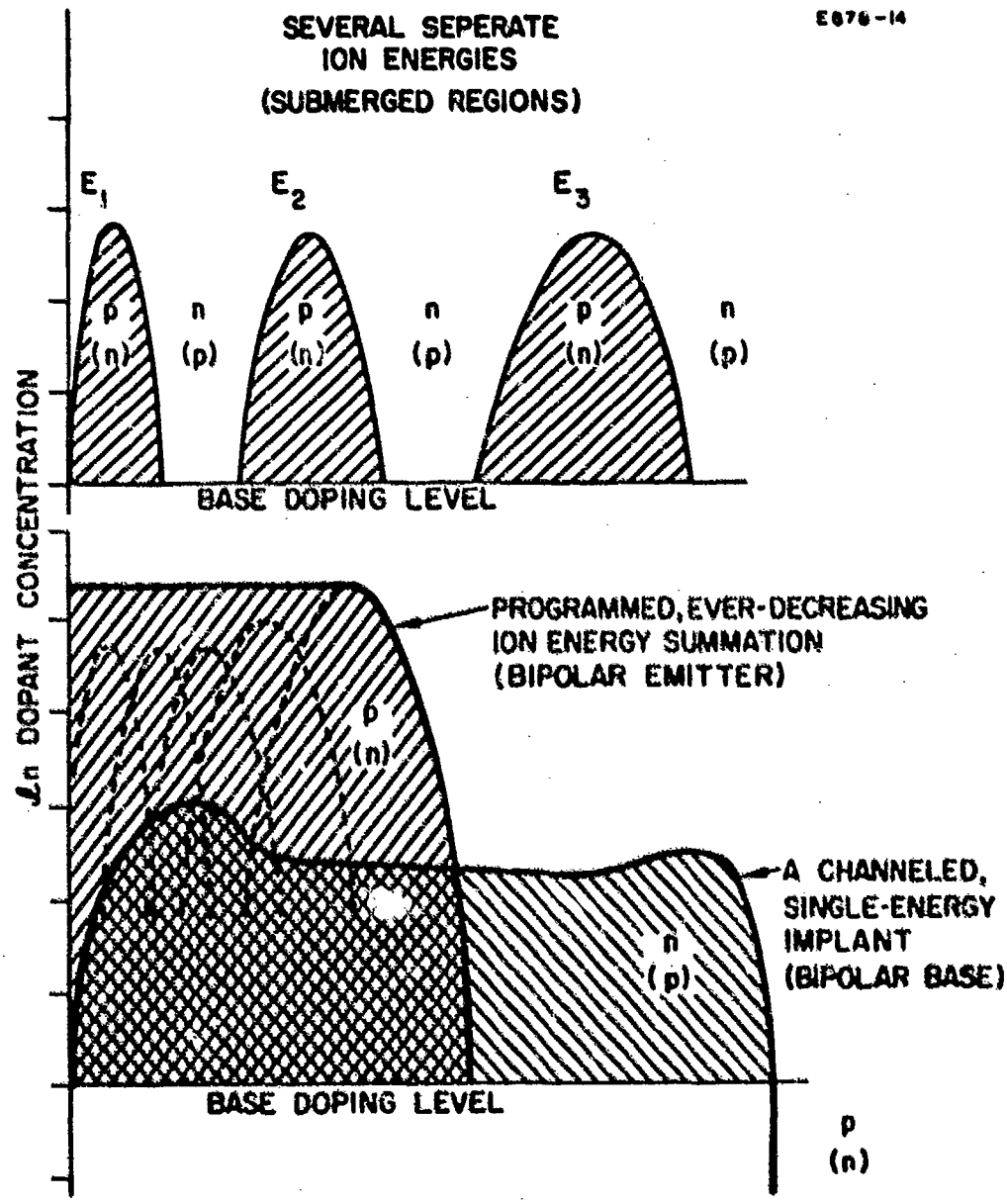


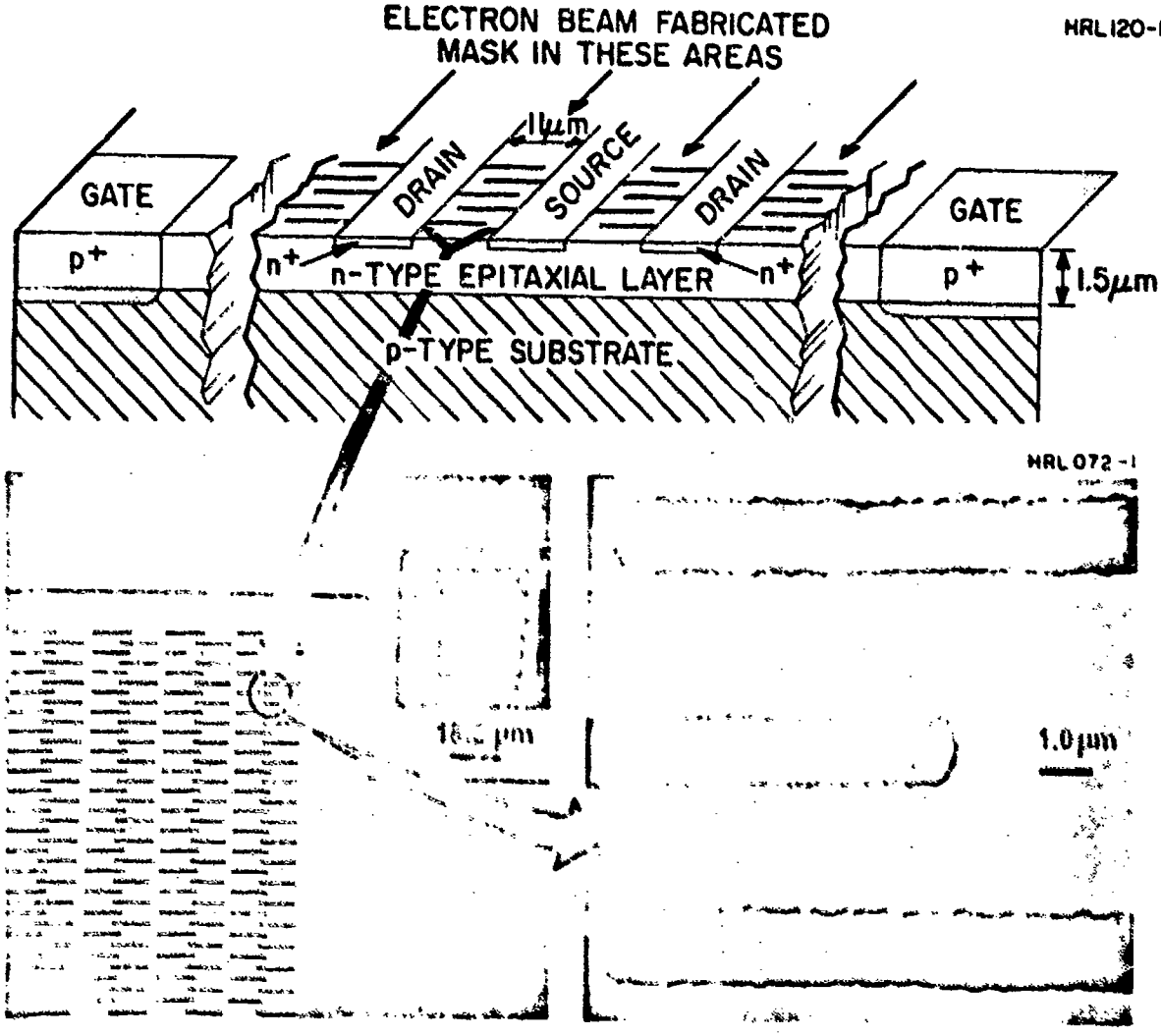

(b) MISORIENT THE BEAM DIRECTION TO ALL CRYSTAL AXES




(c) PREDAMAGE THE CRYSTAL SURFACE

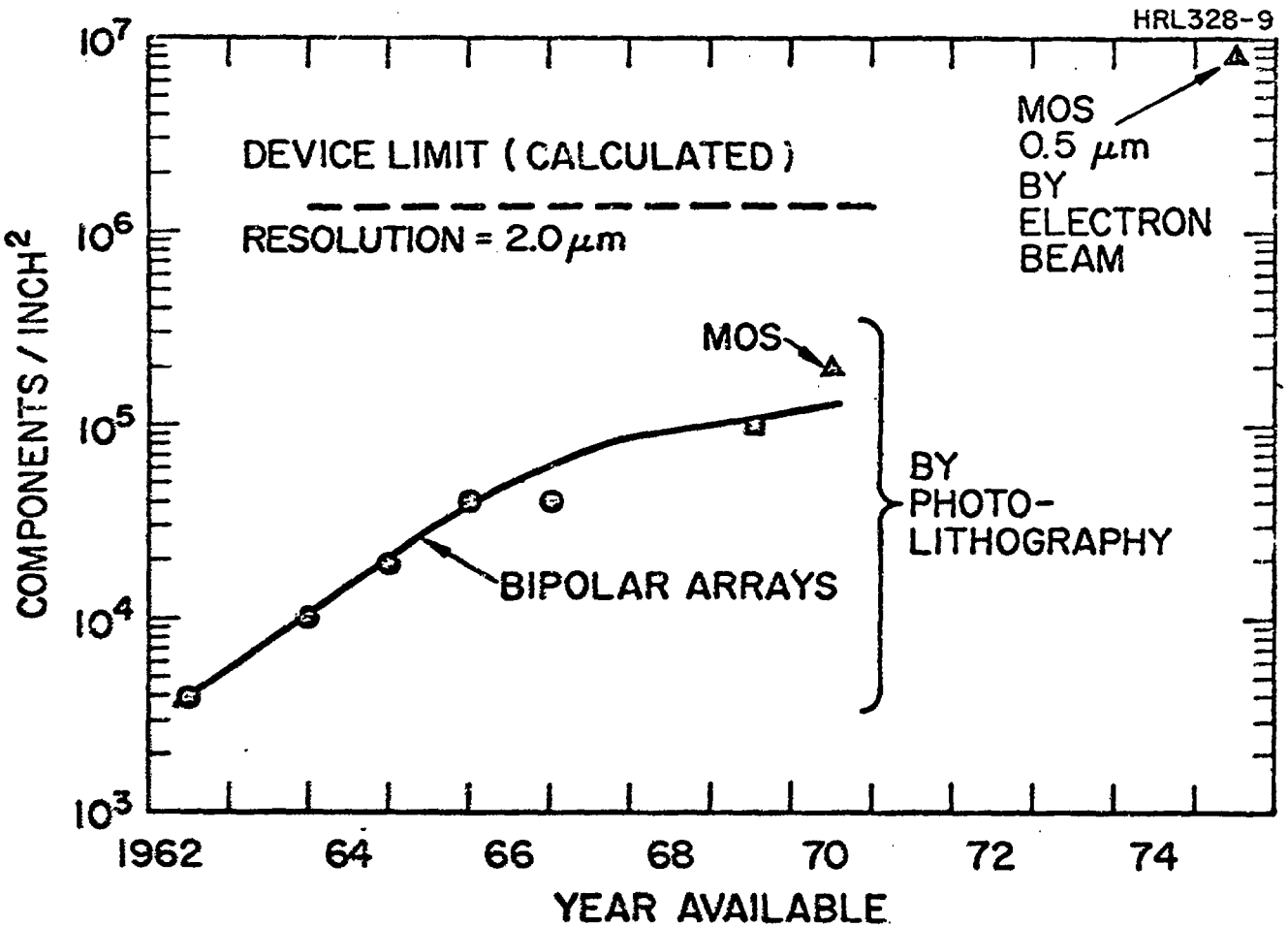
Fig. Methods for preventing channeling.


SEVERAL SEPERATE
ION ENERGIES
(SUBMERGED REGIONS)
E6T6-14
E1
E2
E3
p
(n)
n
(p)
BASE DOPING LEVEL
Ln DOPANT CONCENTRATION
PROGRAMMED, EVER-DECREASING
ION ENERGY SUMMATION
(BIPOLAR EMITTER)
A CHANNELED,
SINGLE-ENERGY
IMPLANT
(BIPOLAR BASE)

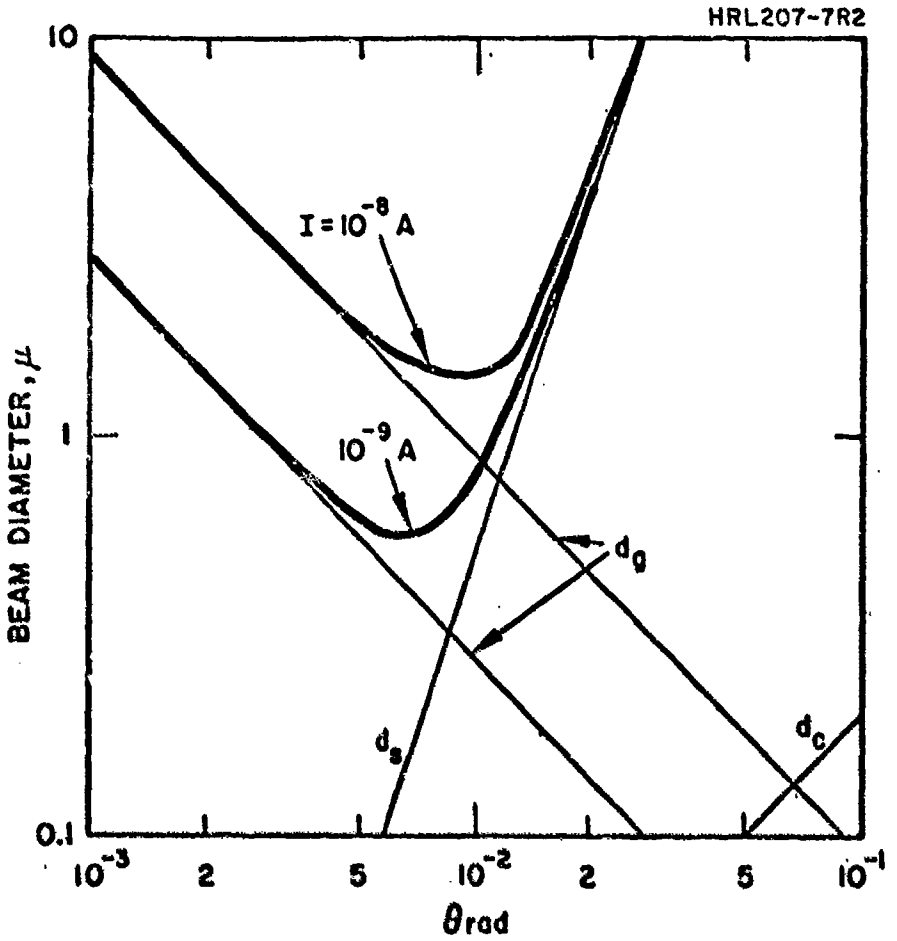



The exposure of resist by an electron beam to yield windows in a gold layer through which fingers are ion implanted to make the high conductance FET device shown.

## GROWTH IN LSI DEVICE DENSITY



*ION BEAM*



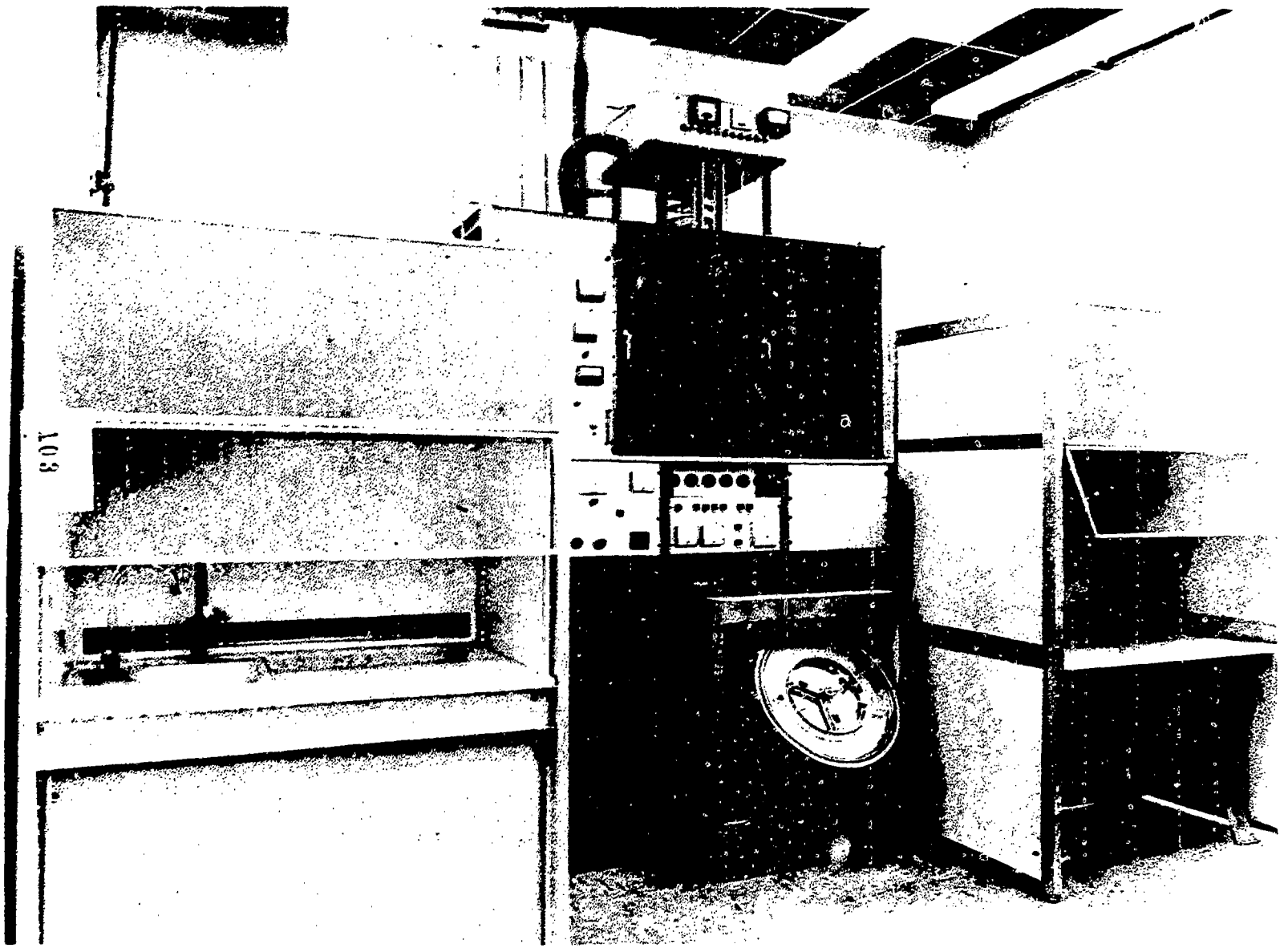

$C_s$ = 100 cm

$C_c$ = 5 cm

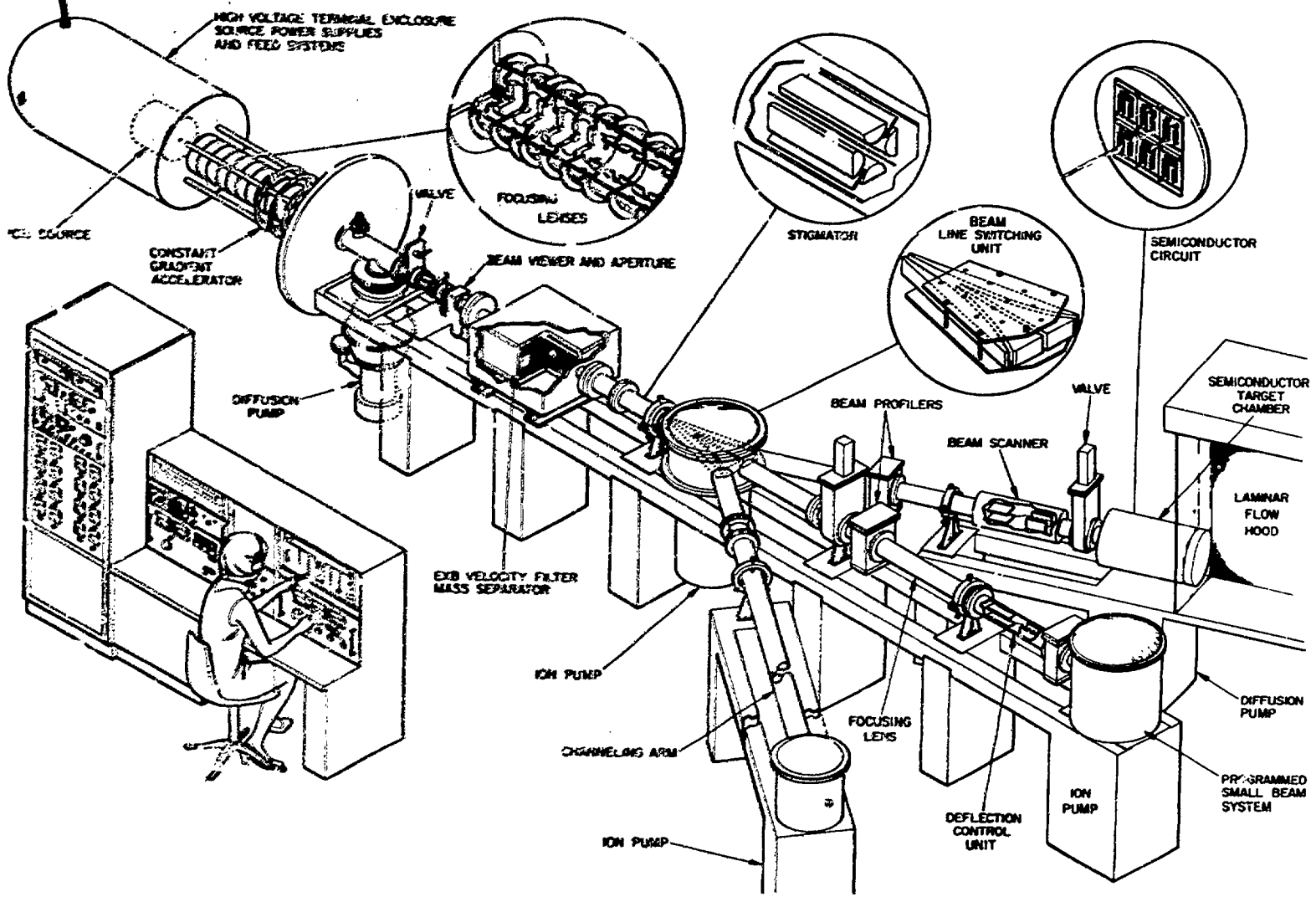
$J_c$ = 0.1 a/cm$^2$

$\frac{\Delta V}{V} = 2 \times 10^{-5}$

V = 100 kV



# 300KV ION IMPLANTATION AND BEAM TECHNIQUE DEVELOPMENT SYSTEM



# ELECTRON PROJECTION SYSTEMS FOR MICROCIRCUIT LITHOGRAPHY

by
R. B. Fritz
and
W. R. Livesay

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NEWBURY PARK, CALIFORNIA

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## INTRODUCTION

This paper describes the development of a production model electron projection system for microcircuit lighography. The system described uses the electron image converter technique to convert a mask pattern to an electron pattern and then projects this electron pattern onto a silicon wafer which is coated with an electron resist. Performance characteristics of a research model system are presented and design changes dictated by an evaluation of the system are discussed. A photograph of the research model electron projection system used for this evaluation is shown in Figure 1.

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## WHY AN ELECTRON PROJECTION SYSTEM?

At the present state of the art, the photo-lithographic step in the manufacture of an integrated circuit is most commonly done by contact printing, either from an emulsion mask or a chrome mask. In order to obtain the intimate contact necessary for high resolution, fairly high contact pressures are required. The abrasion which results from the contact of the mask with the silicon wafer causes defects both in the photoresist surface of the wafer and in the mask. As a result, emulsion type masks commonly show defects after only two or three usages and have to be discarded after five to ten usages. Chrome masks have a longer life but still cause defects in the wafer surface and thereby contribute to a low yield. An obvious solution to the problem is to project the image rather than to contact print the image. However, optical projection systems introduce a new set of problems. The area which can be projected with high resolution is very limited, and the depth of field is extremely shallow. The largest area which can be optically projected to obtain usable 1-micron line widths is less than one inch in diameter, and the depth of field at that resolution would be less than four microns.[1]

The electron projection system dispenses with the optical system entirely and employs instead a patterned electron beam. The electron beam technique still uses a resist coating on the silicon wafer, but one which is sensitive to electrons rather than light. The scheme for producing the patterned electron beam and focusing it on the resist-coated silicon wafer target is shown in Figure 2. The electron beam is produced by a photocathode surface which is excited by an ultraviolet source. The photocathode consists of a thin layer of palladium which is deposited over a titanium dioxide mask. The titanium dioxide mask is of a geometry identical to that which is to be exposed on the silicon wafer. Where ultraviolet light passes through the titanium dioxide mask, the palladium emits photoelectrons at energies of a few tenths of an electron

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[1]R. E. Tibbets, OSA Topical Meeting on Optics in Microelectronics

volt. A uniform 10 kv/cm electric field then accelerates the electrons from the cathode to the silicon target through an axial magnetic field of approximately 1,000 gauss, which is generated by the focus coils. This arrangement causes electrons coming from a given cathode point emitted at any angle to be focused at a corresponding point on the wafer. The result is a 1 to 1 projection of the entire pattern on the silicon wafer. The electron beam resist (poly-methyl-methacrylate) is developed in a solvent which removes the depolymerized pattern. The remainder of the wafer processing steps follow conventional practice.

The patterned photocathode is the electron optical equivalent of the photo mask in the optical process, but since the electron beam system uses projection rather than contact printing, there is no mask wear and no danger of silicon damage. The mask in the electron beam system has essentially infinite lifetime. If the emission of the palladium layer drops too low, the metal can be stripped away and a new layer evaporated on. In addition to eliminating defects caused by contact of the mask with the wafer, the electron beam process has several additional advantages:

1. The achievable resolution is approximately seven times better than optical techniques.

2. The depth of field is 14 times that of an optical projection system.

3. The achievable image diameter is limited only by the size of the focus coils. Present equipment will accommodate wafers up to 2-1/2 inches in diameter.

4. The electron beam can be magnetically deflected, thereby making it possible to adjust the pattern position electronically rather than mechanically.

PHOTOCATHODE LIFE

One of the earliest concerns in deciding whether the electron image projection technique was commercially feasible was cathode life. How many exposures could be made before the cathode emission dropped to a point where exposures were intolerably long?

Early studies indicated that photocathode degradation was due primarily to outgassing of the electron resist and substrate under electron bombardment. Cathodes which were operated in a clean environment (that is, an ion pumped system, baked and operating at a pressure of $10^{-7}$ torr or below) exhibited unlimited life. However, when the electron resist coated wafer was introduced into the system, the emission levels dropped sharply after only a few exposures. It was found, by monitoring the system with a quadrapole mass analyzer, that the principle contaminants produced by the electron bombardment of the electron resist were water and oxygen.

Consequently, the prototype electron projection system was designed in such a manner as to provide the maximum possible vacuum conductance in the region of the photocathode in order to reduce cathode fatigue from subsequent ionization and ion bombardment from these contaminants.

When cathode emission drops to an unusably low value, several rejuvenation techniques are available. Another very thin layer ($\approx$ 20Å) of palladium may be evaporated on the top of the original. This process may be repeated as many as 3 times. After that, the palladium can be stripped off with a hot nitric acid solution and a new palladium layer evaporated on. The palladium may be stripped from the titanium dioxide mask as many times as desired without damaging the mask. Another rejuvenation technique is to bake the photocathode in the vacuum to drive off adsorbed surface films. This can be done with the UV source which is used for exposure or, more quickly, with an infrared heat lamp.

The life test data on the prototype system is shown in Figure 3. Curve A shows the emission versus number of exposures for a fresh cathode, that is, a cathode which was put in the system immediately after the palladium film had been evaporated on. Note that the emission drops rather sharply after the first few exposures and then levels out in a hyperbolic fashion.

Curve B shows the emission history of a photocathode that has been renewed by evaporating an additional 20Å layer of palladium over the initial 40Å layer.

In both of the above tests, each exposure was of 10-second duration and the wafers were cycled in and out at the rate of one every 4 minutes. This produced a pressure in the image tube of approximately $2 \times 10^{-5}$ torr during exposure. Development was normal after 50 exposures and there was no visible degradation of image quality. The measured current density after 50 exposures was 1.5 $\mu amps/cm^2$ for a fresh cathode and 1.0 $\mu amps/cm^2$ for the rejuvenated cathode. Ten-second exposures have been made with current densities as low as 0.3 $\mu amps/cm^2$. These exposures yielded acceptable results and are regarded as the lowest limit of useful emission from a cathode. Extrapolating curves A and B out to 100 exposures, it appears that they would be well above the lower emission limit after 100 exposures.

Curve C shows the emission history of a cathode which has been returned to air several times and then baked to restore its emission. The bake was done simply by exposing the cathode to the normal ultraviolet excitation and monitoring the emission current while baking. Approximately 20 minutes baking was required after each exposure to atmosphere to bring the cathode back up to its peak emission. The excitation, in all cases, was a low pressure mercury arc lamp formed in the shape of a pancake spiral operating at normal voltage. Operating in this manner, the lamp produces over 90% of its output at 2537 angstroms, which is the wavelength desired to match the work function of the palladium photoemitter.

By increasing the voltage drop across the electrodes of a low pressure mercury arc lamp, an increase in total output illumination can be achieved at the expense of radiant output efficiency at 2537 angstroms. This is due to the fact that as the electrons are elevated to higher energies they ionize more of the gaseous mercury and increase the pressure inside the lamp. This increase in pressure results in the resonance radiation of the 2537-angstrom line being reabsorbed by other atoms and an excitation of atoms into higher energy levels, which subsequently re-emit by means of low energy transitions and, therefore, at longer wavelengths. However, by cooling the outer envelope of the mercury bulb, one may decrease the pressure and still maintain a high efficiency output of 2537-angstrom radiation. The increase in emission at 2537 angstroms is due to the greater number of electrons available for causing resonance transitions and the lower pressure towards the outer portion of the positive column creating a longer mean free path for 2537-angstrom photons. By operating the lamp in this manner, a 50% increase in photocathode current density has been achieved.

This, coupled with a highly improved pumping system using cryo-panels in the image tube area as shown in Figure 13 to remove the water and oxygen, is expected to improve photocathode life to at least 500 exposures.

## PHOTOCATHODE FABRICATION TECHNIQUES

In order to produce fine geometry patterns in titanium, it is necessary to use a disposable mask technique[2] rather than simply etching the titanium directly. This is primarily due to titanium's resistance to most common etchants. When etched, it has a very nonuniform etch rate, producing undercutting and poor edge definition. Since disposable mask techniques involve many more process steps which increase the probability of pinholes and defects, we have expended considerable effort in searching for a more suitable material for the mask. The characteristics which would be most desirable for a photocathode mask are as follows:

1. Opaque to ultraviolet light in thicknesses of less than 1,000 angstroms
2. Can be etched directly to line widths of less than 0.5 μ
3. Not photo-emissive under 2537Å excitation
4. Not attacked by solvents of palladium (so that palladium can be stripped without damaging mask)
5. Hard and durable

A proprietary material satisfying these requirements has been found and is now being used in all photocathodes.

The pattern can be defined in the mask material in either of two ways. For line widths of 2 microns or more, satisfactory masks can be made by coating the mask with photoresist and contact printing the desired pattern. The masks which were used to project the patterns shown in Figures 6, 7 and 8 were made in this manner. Note that the lines under 2 microns wide are very marginal in quality. In order to utilize the ultimate resolutions of the electron projection system and use mask patterns with line widths below 2 μ and down to 0.5 μ, it is necessary to define the patterns in electron resist using a scanning electron beam. The mask which was used to project the 1/2 μ line pattern shown in Figure 5 was made in this manner.

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[2]K. C. Hu, Expendable Masks, Electronic Packaging & Production, October 1967

ELECTRON RESIST

The electron resist used with the system is poly-methyl-methacrylate. It is a positive-acting resist which depolymerizes when exposed to an electron beam but which is insensitive to light of any wavelength. Resists of this type commonly have a sensitivity of about $10^{-4}$ coulombs/cm$^2$.[3] However, by using special processing both in making the resist and in development, the sensitivity can be increased to approximately 3 x $10^{-6}$ coulombs/cm$^2$. This means that 10-second exposures can now be achieved with electron densities as low as 0.3 μamps/cm$^2$. This increases the effective cathode life so that recoating is only necessary after several hundred exposures.

Characteristics of the RES-developed resist are summarized below:

1. Sensitivity (to electrons) - 3 x $10^{-6}$ coulombs/cm$^2$
2. Sensitivity to light - none
3. Resolution limit - limited only by electron scattering, which depends on coating thickness and substrate material
4. Shelf life - excellent, more than 6 months
5. Exposure latitude - more than 10 times normal (over-exposures are easily compensated by using weaker developer)

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[3] I. Haller, M. Hatzakis, R. Srinivasan, IBM Journal of Research and Development, 12, 251 (1968)

ELECTRON OPTICAL PERFORMANCE

The resolution of an electron projection system is influenced mainly by four factors:

1. Uniformity of the electric field
2. Uniformity of the magnetic field
3. Velocity distribution of emitted electrons
4. Electron scattering in the resist

By careful design of the geometry of the system, uniformity of the electric field can quite easily be held within acceptable limits. A uniform magnetic field can be achieved by careful focus coil design and by taking care to avoid magnetic materials near the imaging area. The velocity distribution of the emitted electrons is controlled by using ultraviolet excitation which is close to the work function of the photocathode material so that electrons are emitted at very close to zero velocity.

Figure 4 shows a comparison of resolution limits of an optical projection system and an electron projection system as a function of contrast ratio. The optical system is diffraction limited and the electron projection system is limited by the velocity of emitted electrons. The electron curve is drawn for an electron energy spread of 0.1 eV. Note that at the minimum usable contrast ratio for microcircuit fabrication ($\approx$ 40%) the electron beam has a resolution of approximately 0.2 $\mu$. This is confirmed by resolution tests on the system in which 0.5 $\mu$ lines have been reproduced with approximately 0.2 $\mu$ edge definition. See Figure 5 for photographs of these lines.

A unique feature of axial electric and magnetic field focusing is that there is no curvature of field, coma or astigmatism. Consequently, there is no difference in the resolution at the edge of an image from that in the center, so long as the electric and magnetic fields are uniform. The off-axis resolution of the RES system is demonstrated by the photographs in Figure 6. Both photographs show the 7 and 8

patterns of a standard Air Force resolution chart. The narrowest lines in the 8 group are 1.1 μ wide. Since these patterns were contact printed on the photocathode from an emulsion mask, the quality of the 8 group leaves something to be desired; but, nevertheless, they are there. View (a) is taken at the center of a 2" diameter wafer, and View (b) is taken approximately .050" from the edge of the same 2" diameter wafer. Note that there is no observable difference in resolution.

Defocusing caused by the alignment deflection system is negligible. No line broadening is detectable in a 1-micron line when the pattern is deflected to its maximum (0.010 inch).

Depth of field of the system is approximately ± 25 microns for 1 μ resolution. Figure 7 shows three exposures: (1) at nominal focal distance, (2) at the nominal focal distance +25 microns and (3) at nominal +50 microns. The line width of the smallest pattern is 1.2 μ. The line broadening of the 1.2 μ lines is not discernible at 25 μ and becomes barely noticeable at 50 μ out of focus.

The ability of the system to reproduce both dark field and light field images is shown in Figure 8.

AUTOMATIC ALIGNMENT

The first prototype system used electron beam induced conductivity (EBIC) in the wafer oxide layer as a detection mechanism for pattern alignment errors.[4] Briefly, the system operated as follows.

An electron beam impinging upon an $SiO_2$ layer will induce conductivity which is inversely proportional to the thickness of the layer. If a bias voltage is connected across the layer as shown in Figure 9, the current will vary as a function of the beam position when the electron beam passes over a step etched in the oxide. To achieve automatic alignment, this phenomenon was used in the following manner:

a. During the first exposure of the wafer, a tapered cross pattern is projected onto the wafer by the photocathode. This pattern is etched in the $SiO_2$ layer during normal processing.

b. During the second and subsequent exposures, the tapered cross pattern on the photocathode is projected on the identical pattern etched in the $SiO_2$ layer.

c. Alignment-sensing circuits measure the induced current and determine the degree and direction of misalignment.

d. X and Y adjustments are made by driving the X and Y deflection coils.

e. Angular adjustment ($\theta$) and magnification are established by varying the current ratio in the A, B and C focus coils.

f. Digital optimizing circuits adjust X, Y and $\theta$ until maximum output is achieved, thus indicating alignment within $\pm$ 1/4 $\mu$m.

Although this technique will produce acceptable alignment performance, the EBIC detection mechanism requires several processing steps which are undesirable in the production of integrated circuits. One problem is that oxide thicknesses

[4] T. W. O'Keefe, IEEE Transactions on Electron Devices, ED-17, No. 6, 465-469, June 1970

of approximately 10,000 angstroms are required in the detector area in order to assure that there will be no shorts to the silicon via pinholes or other defects when the area is aluminized. Oxides of this thickness are incompatible with the fabrication of submicron geometry devices for which this system was designed. A second drawback is the necessity of aluminizing the contact area before each exposure. This is further complicated by the necessity to isolate the two contact areas from each other and from the rest of the wafer.

Because of these problems, we found it necessary to pursue a simpler approach to the problem of alignment error detection. Therefore, we have abandoned the EBIC approach in favor of a much simpler system using primary beam current to detect a permanent mechanical marker on the wafer. We are presently using two .010" diameter holes as markers in the wafer and detecting the primary beam current reaching the rear side of the wafer through these holes from alignment marks in the photocathode.

Figure 10 shows a diagram of the system. The alignment mark is so designed that it produces the maximum amplitude signal when it is centered about the wafer hole. A computer-controlled scan pattern first locates the hole and then scans successively smaller patterns, recalculating the center each time until an optimum alignment is attained. The total alignment time is approximately 1 second, and the system will detect and correct alignment errors as small as 0.2 $\mu$. Using this technique, the size of the hole is not critical, nor is it critical if it grows or shrinks during the processing steps, so long as it changes uniformly.

This approach has the following advantages over the EBIC alignment:

1. Only one processing step is required to make the apertures in the wafer, and it only has to be done once before the first exposure.

2. The alignment apertures survive all IC processing steps, including epitaxial growth.

3. No aluminizing is required before each exposure.

4. No electrical contacts need be made to the wafer for alignment.

5. Yield of wafers capable of being automatically aligned is much higher.

6. Placement accuracy of the alignment apertures on the wafer is not critical; it can easily be done in a mechanical jig.

7. Alignment signal amplitude is more predictable since we are detecting primary current directly rather than an induced current which has a variable gain from wafer to wafer.

8. There is no phase shift in the alignment signal due to capacitance across the oxide layer in the wafer as there is in EBIC.

9. Alignment apertures can be placed closer to the edge of the wafer than with EBIC masks since oxide or crystal defects do not affect the usability of an aperture.

IMAGE ROTATION

The first system which was built achieved image rotation for alignment by altering the uniformity of the magnetic focusing field in such a manner as to cause an angular shift in the projected pattern.[5] The magnetic field uniformity was controlled by adjusting the relative currents flowing through the two outside coils and the center coil. The two outer coils are spaced just slightly greater than the Helmholtz spacing so that by adding a small amount of current in the center coil a uniform field is achieved. This is illustrated in Figure 11. This produces zero rotation. If the current in the center coil is decreased and the current in the outer coil is increased by a corresponding amount to keep the total field constant, a small image rotation is produced. Conversely, if the current in the outer coil is reduced and that in the center coil is increased proportionately, the image will rotate the other direction. The total rotation achievable by this technique is approximately ± 1.5 milliradian. However, since the axial magnetic field is caused to increase or decrease radially during rotation, the image focus deteriorates as a function of the rotation angle and the distance from the center of the image. This relationship is shown in Figure 12. The dotted line is the theoretical degradation predicted on the basis of the change in magnetic field as a function of radius and rotation angle. The solid line shows experimental results. The coil geometry was such that the most uniform field condition was not located midway between the rotation extremes but rather was obtained with most of the current flowing in the outer coils.

From Figure 12, it is clear that magnetic rotation has unacceptable defocusing characteristics for patterns demanding resolution below 4 microns over a 2-inch diameter wafer. Even with 4 μ geometry, the rotation angle is limited to less than ± 1.5 milliradians, which allows a very small tolerance on mechanical wafer placement accuracy; and, for 3-inch wafers, magnetic rotation is clearly out of the question.

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[5] T. W. O'Keefe, J. Vine, Adv. Electronics & Electron Physics, Vol. 28A, p. 47, Academic Press, N.Y., 1969

Therefore, RES has developed a hybrid alignment system which utilizes magnetic deflection for X and Y corrections but uses a proprietary mechanical system for angular corrections. The mechanical system we are using is somewhat unique in that it uses no bearings and can be accurately moved in increments of 1 microradian with a total excursion of ± 10 milliradians. Using a mechanical rotation system eliminates the need for the center focus coil and greatly simplifies the focus coil power supply. Eliminating the center focus coil also greatly simplifies the automatic handling system and permits a much more efficient vacuum system in the region of the photocathode.

AUTOMATIC HANDLING SYSTEM

The automatic handling mechanisms for the wafers and photocathodes are diagrammed in Figure 13. Trays containing 40 wafers each are loaded in Chambers A and B. A tray containing 20 photocathodes is loaded in Chamber C. These trays rest on poppet valves which open and lower the trays into operating position when the pressure in the loading chamber reaches $10^{-5}$ torr. Then a stepping motor moves Tray A down one step at a time as the Transfer Mechanism A slides the wafer out of the tray and places it on the wafer platform. At the same time the photocathode tray is indexed to the position of the desired mask pattern selected from the master control panel and Transfer Mechanism C slides it out of the tray and positions it over the alignment pins above the wafer. At this time, the wafer platform is elevated approximately 1/2 inch which locks the wafer in position and lifts the photocathode off the transfer mechanism and allows it to center itself on the alignment pins. After alignment and exposure, the wafer platform is lowered and the wafer is replaced in the tray and the next wafer is selected. When all of the wafers in Tray A have been processed, the tray is raised back up to the loading position, thereby closing the poppet valve. While the tray is removed and replaced with a fresh batch, Tray B is processed in a manner identical to that for Tray A.

Tests with a prototype system indicate that a wafer can be placed on the wafer platform and clamped into position with a mechanical accuracy of about ± .005", which is well within the deflection capabilities of the automatic alignment system. The cycle time for the mechanism is approximately 5 seconds. Since it takes approximately 10 seconds to align and expose the image, the total throughput rate is one wafer every 15 seconds, or 240 per hour.

## THE FUTURE

Applications for electron projection systems are quite diverse. Its ability to reproduce extremely high resolution patterns makes it the ideal tool for making high density MOS memories, surface wave acoustic transducers for use in the gigahertz and above range and very high resistance precision resistors. It can also be used as a precision mask duplicator. Because of its potential for higher yield, large scale integration becomes feasible for production.

Delivery of the first fully automatic production machine which will process 4 wafers per minute is expected in about 5 months. Research model systems which will align and expose one wafer every 5 minutes are available immediately.

RES is also developing an automated scanning electron beam pattern generation system for mask making. The system is computer-controlled and can be used to make either conventional masks or the masked photocathodes for the electron projection systems. This will provide the necessary companion to the electron projection systems for producing masks for submicron geometry circuits.

BIOGRAPHY OF AUTHORS

R. B. Fritz

Mr. Fritz is currently Vice President of Engineering at Radiant Energy Systems in Newbury Park, California. Prior to joining RES, Mr. Fritz was Manager of Systems Engineering at the Aeronutronic Division of Philco-Ford in Newport Beach, California. Mr. Fritz has an extensive background in the systems design of precision electro-optical-mechanical systems. He participated in the early development of the Falcon missile at Hughes Aircraft in Culver City, California and later on the Shillelagh and Chaparral missile systems at Philco-Ford. He received his Master of Science degree in Applied Physics from the University of California at Los Angeles in 1956.

W. R. Livesay

Mr. Livesay is currently Manager of Electron Physics at Radiant Energy Systems in Newbury Park, California, where he is engaged in the research and development of pattern generation systems, electron projection systems and electron optical devices. Prior to joining RES, he was in charge of the R&D Optical Lab at Electro-Optical Systems in Pasadena, California, where he was engaged in the design and testing of prototype image tubes, night vision systems and image intensifier cameras. He received the B.Sc. degree in Physics from California State Polytechnic College, San Luis Obispo, in 1967. Mr. Livesay is a member of the Electron Microscopy Society of America and the Optical Society of America.

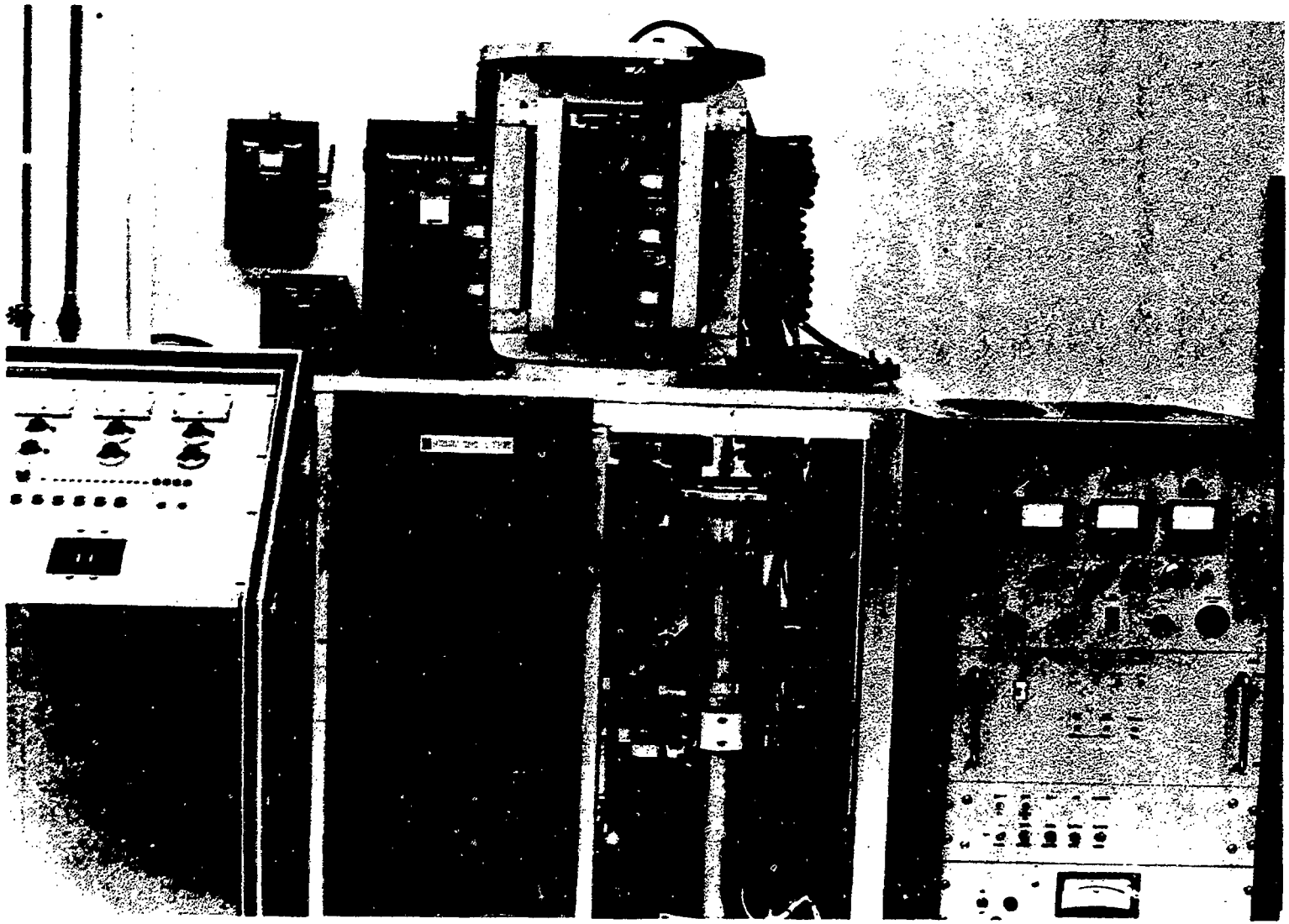


Figure 1. Research Model Electron Projection System

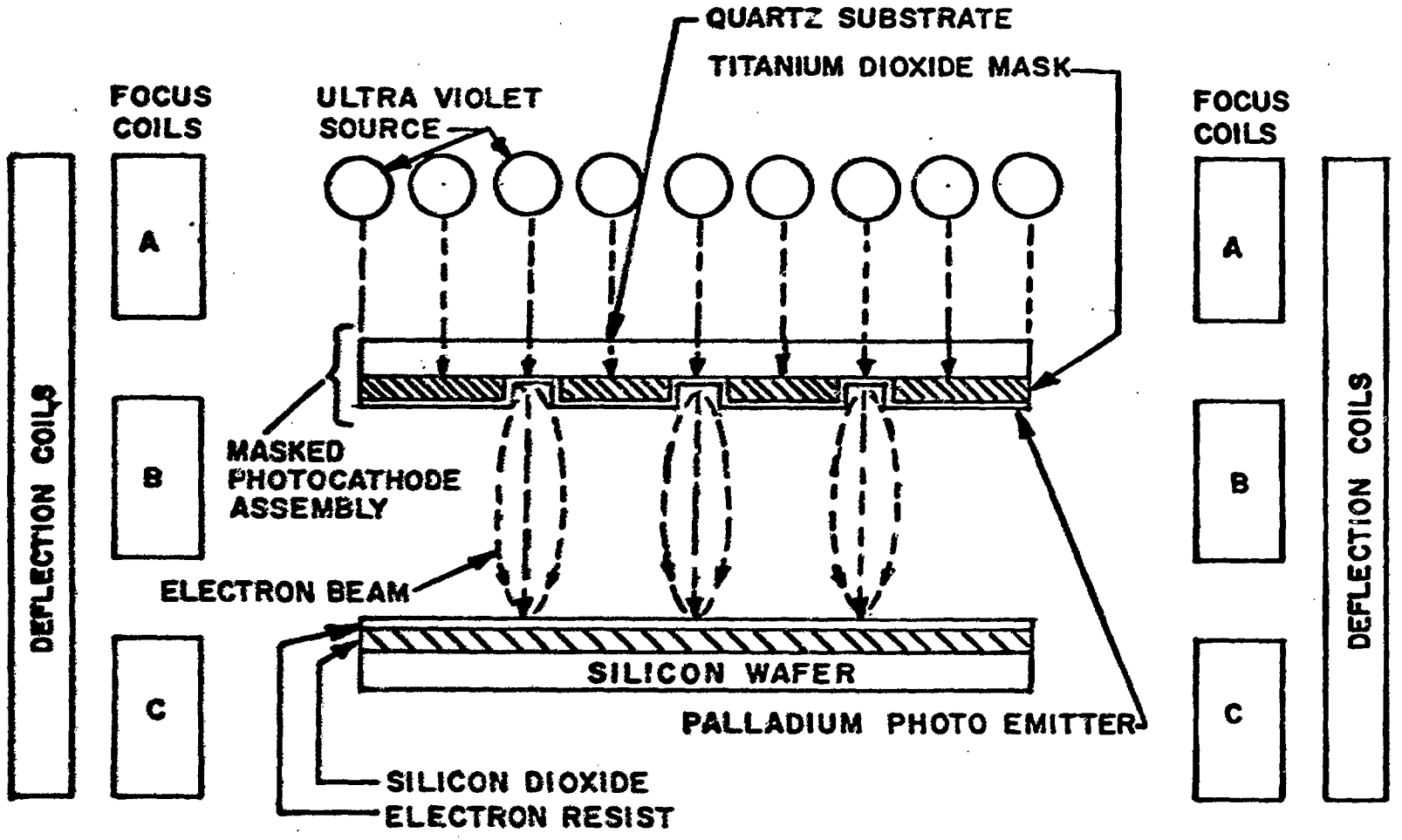



Figure 2. Diagram Illustrating Principles of Electron Pattern Projection

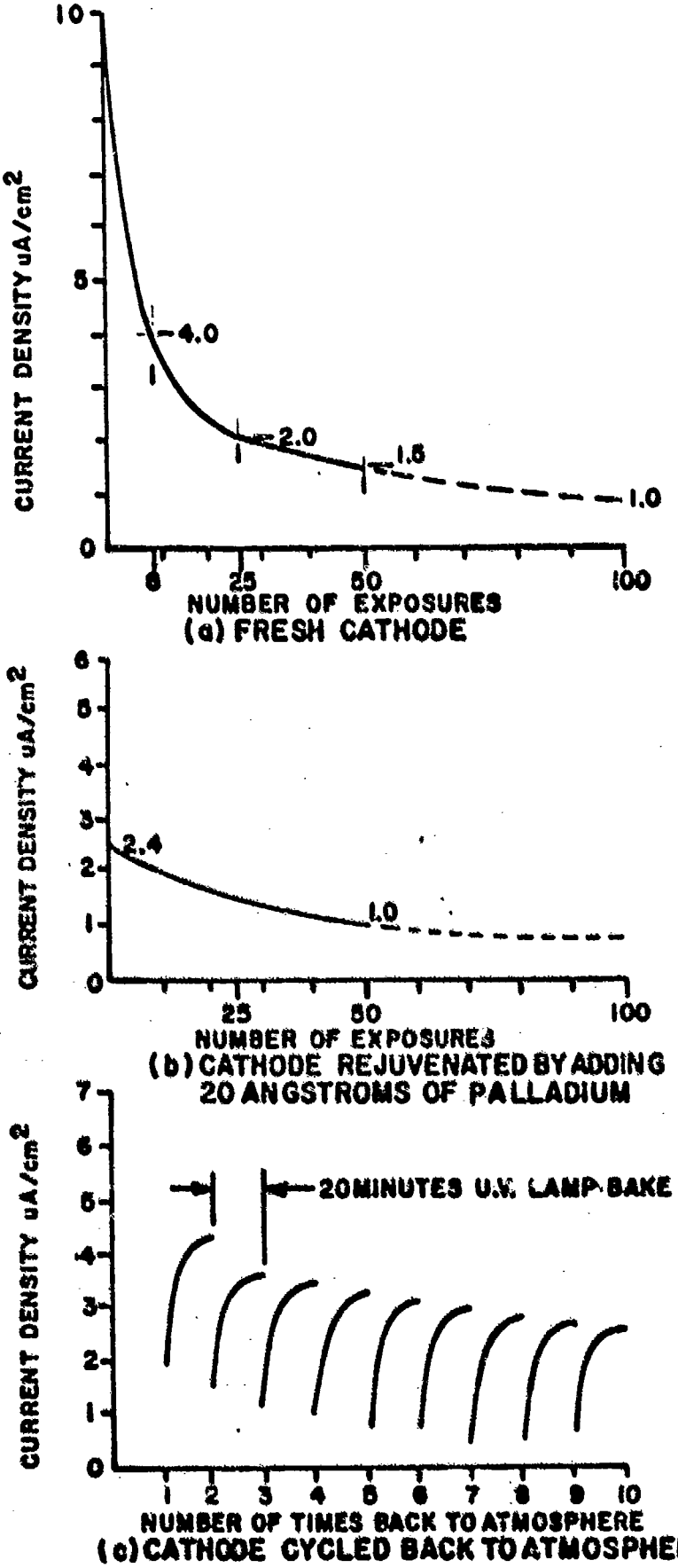



Figure 3. Cathode Life Study Test Results

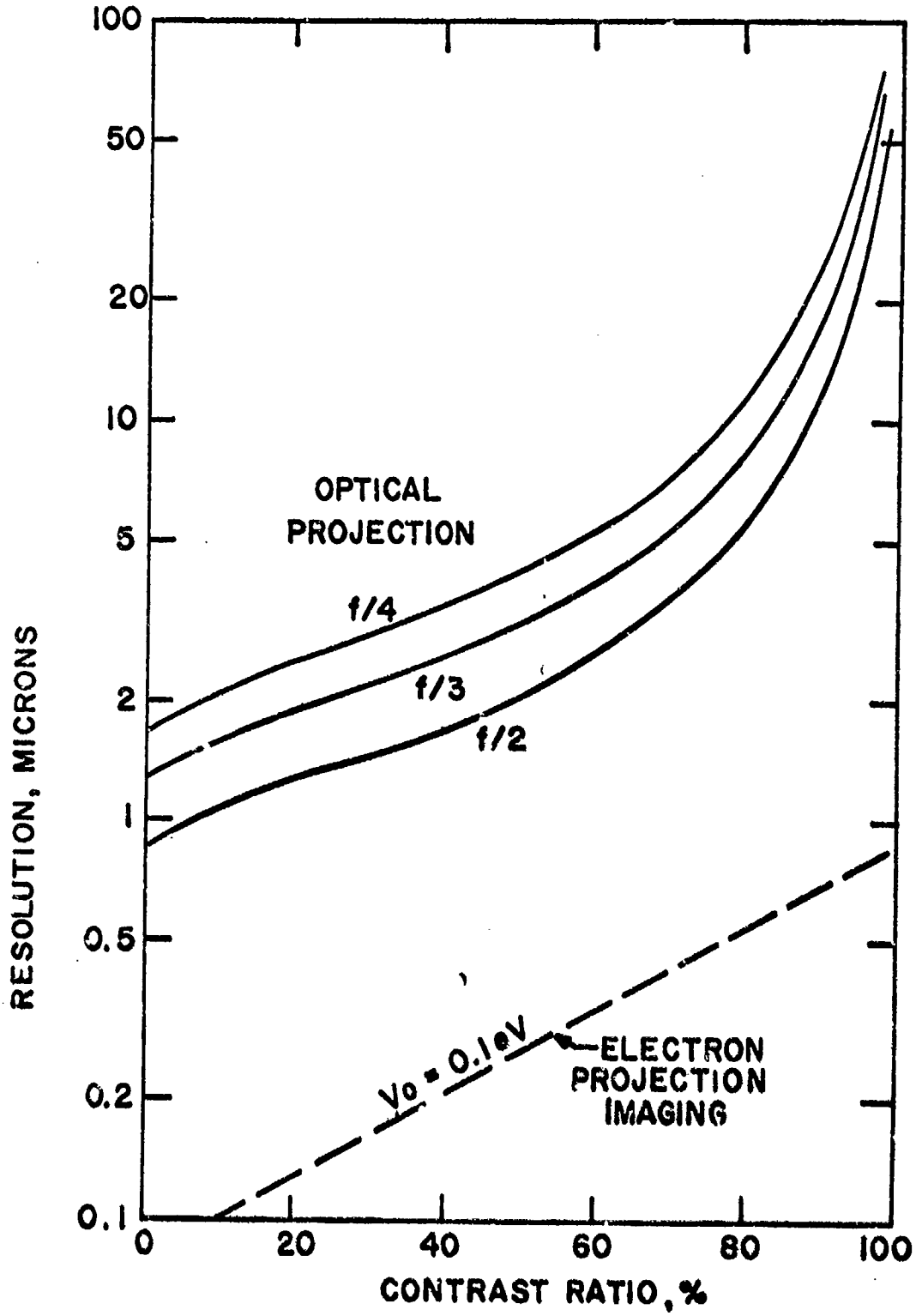
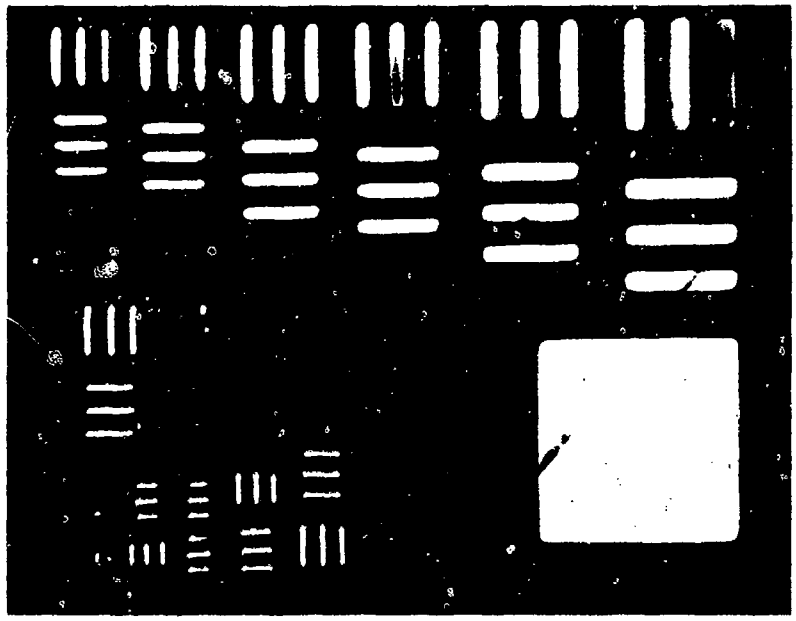
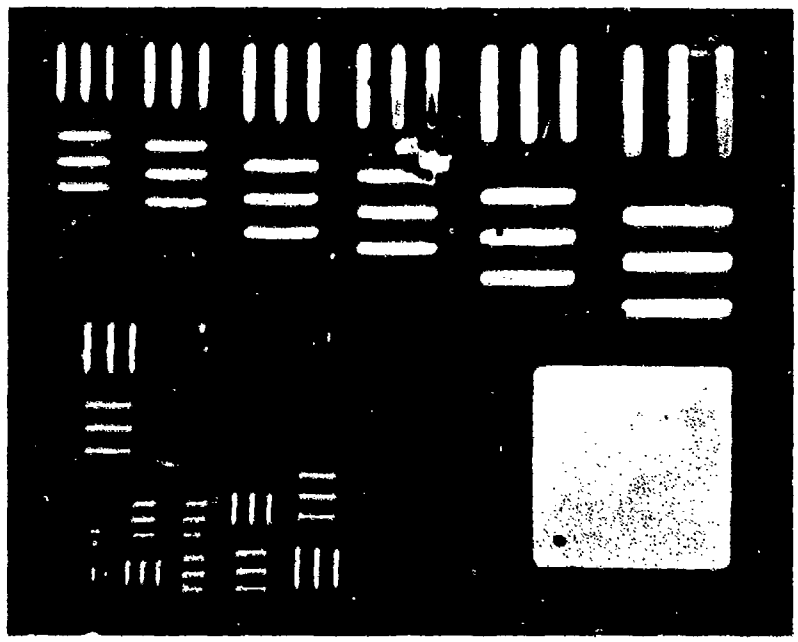



Figure 4. Comparison of Resolution Limits of an Optical Projection System versus an Electron Projection System

Figure 5. 1/2 Micron Lines on 2-1/2 Micron Centers Printed on Resist by Electron Projection System

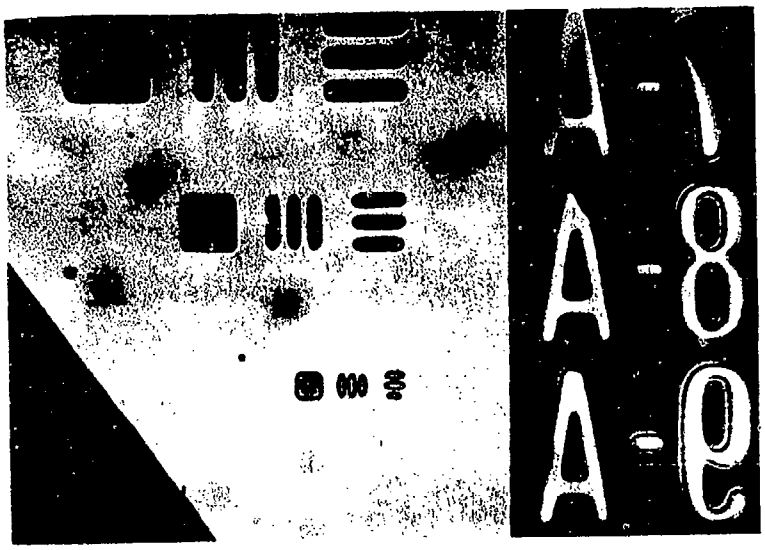


(a) Center of Wafer

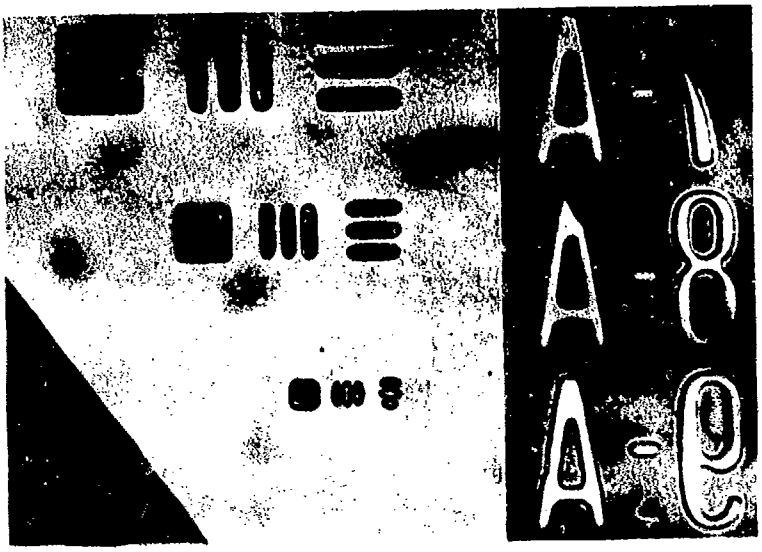


(b) Edge of 2-Inch Wafer

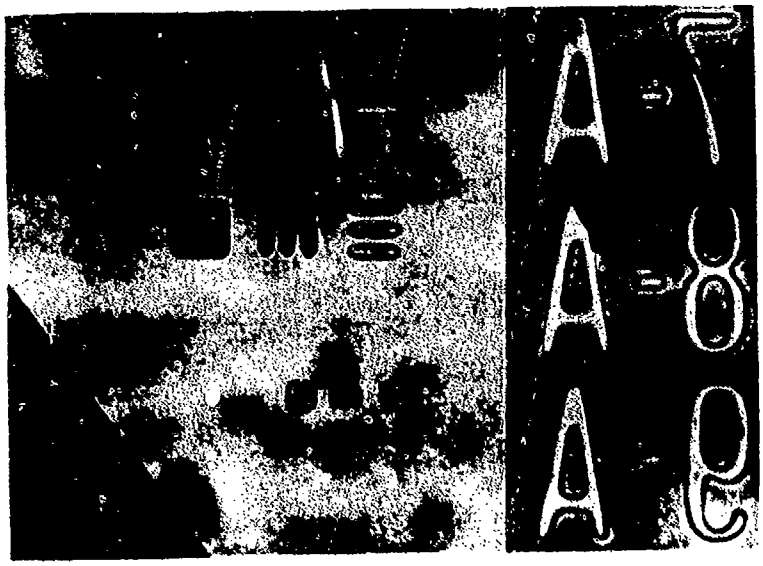
Figure 6. Resolution at Center and Edge of 2-Inch Wafer



(a) Nominal Focus



(b) Nominal Focus + 25 Microns



(c) Nominal Focus + 50 Microns

Figure 7. Resolution Charts Illustrating Depth of Field

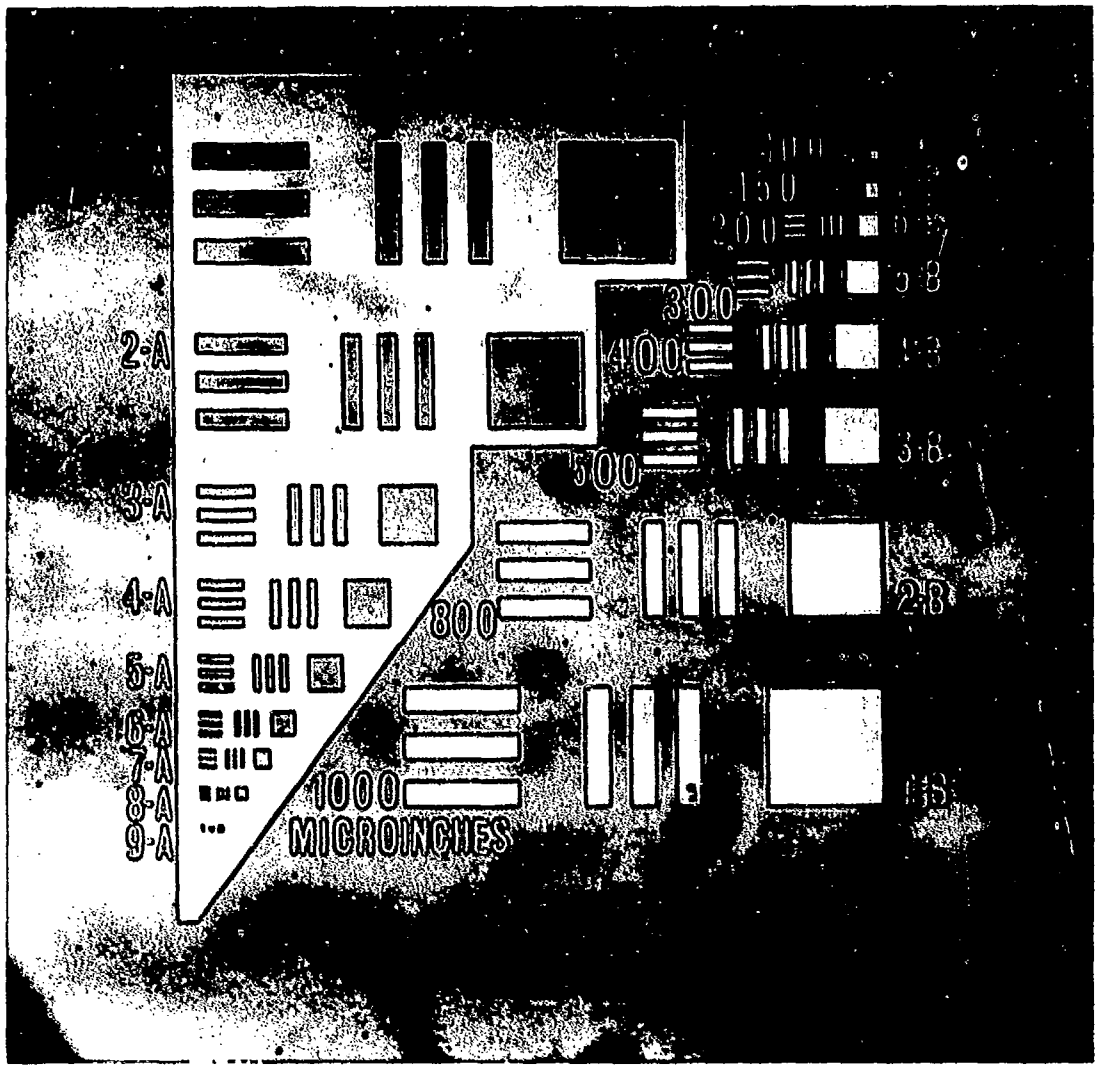



Figure 8. Performance of the Electron Projection System with Dark and Light Field Images

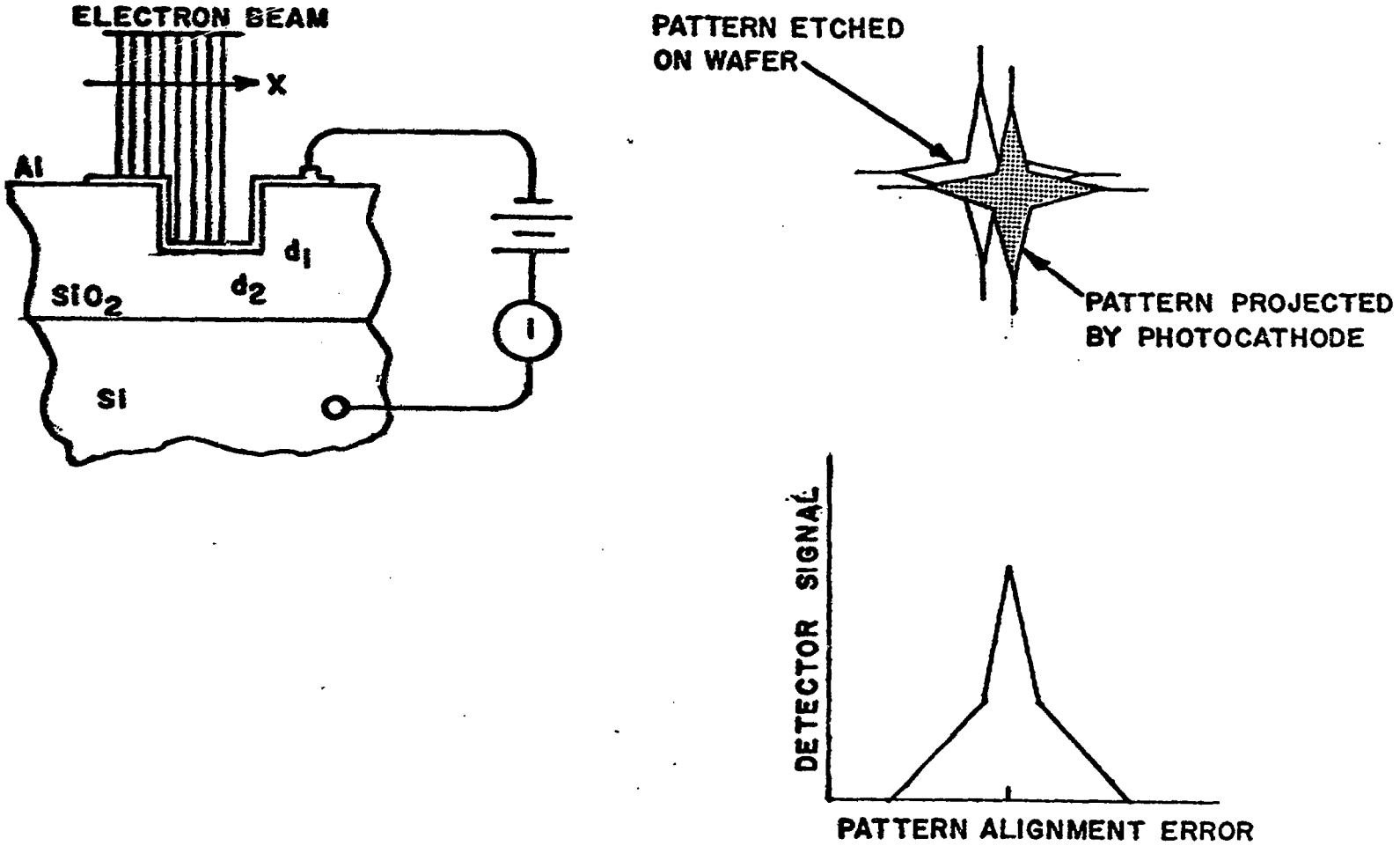
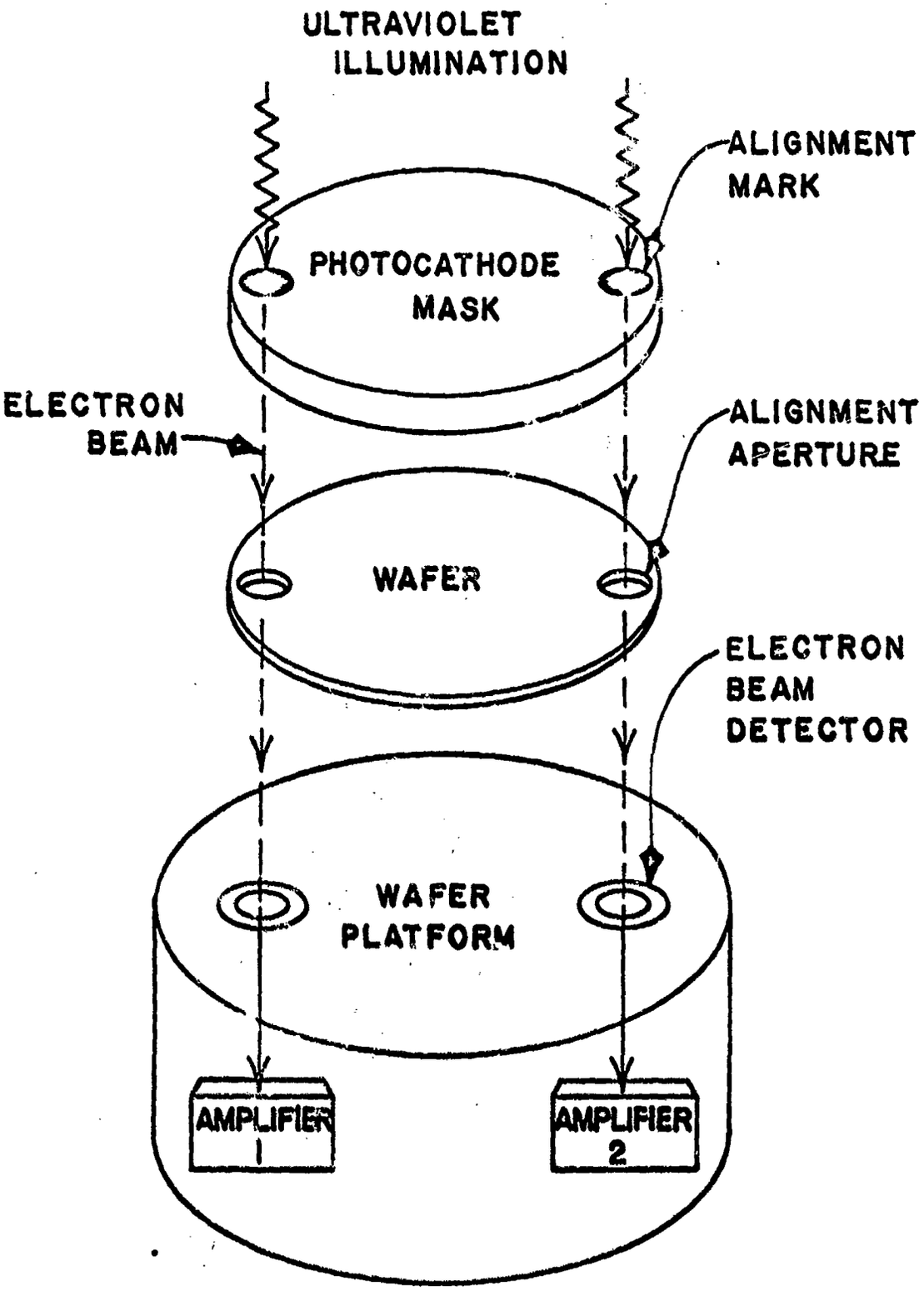



Figure 9. Alignment Detection System Using EBIC Effect




ALIGNMENT DETECTION MECHANISM

Figure 10. Alignment Detection Using Holes in Wafer

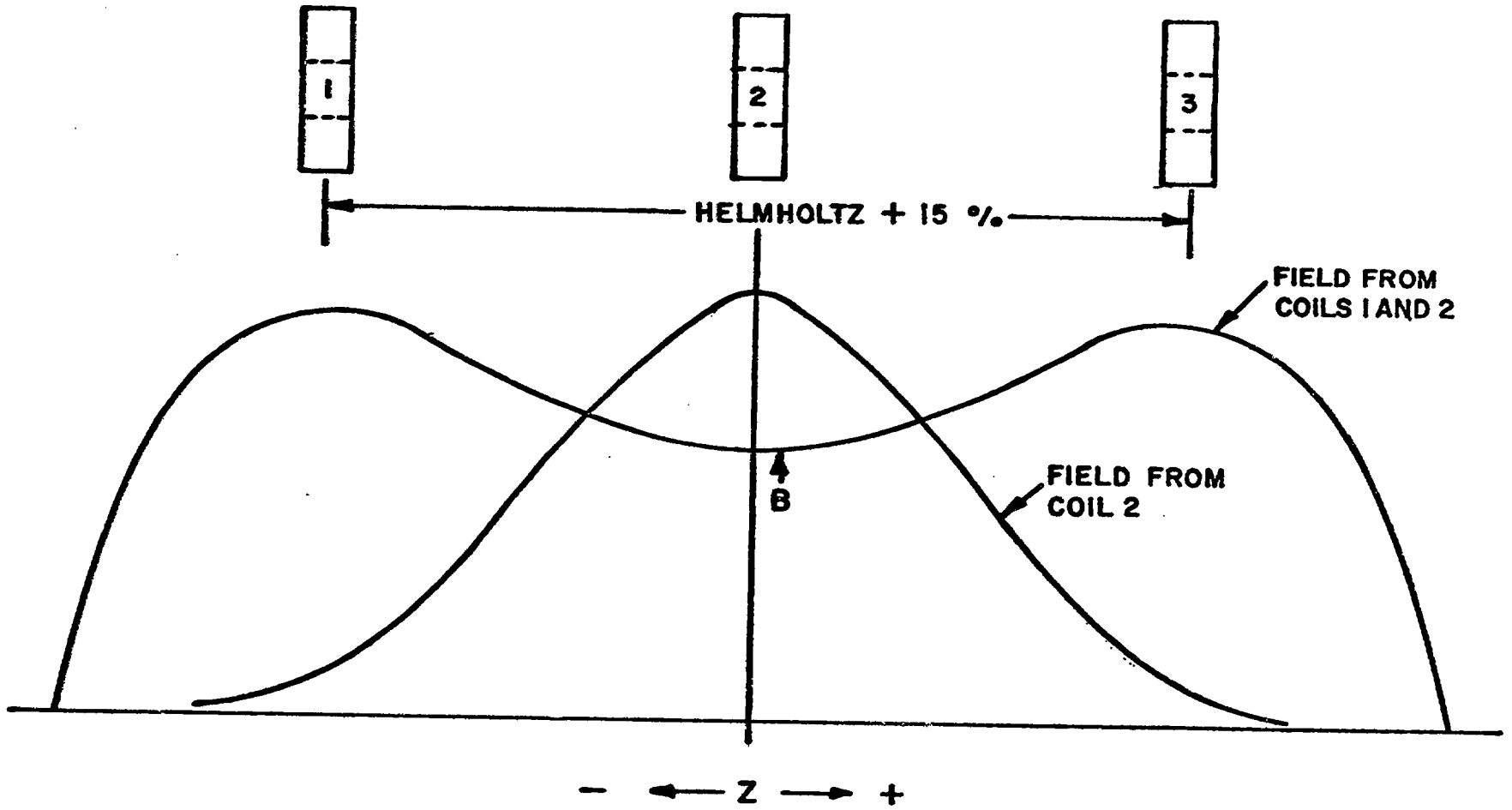



Figure 11. Image Rotation by Magnetic Field Distortion

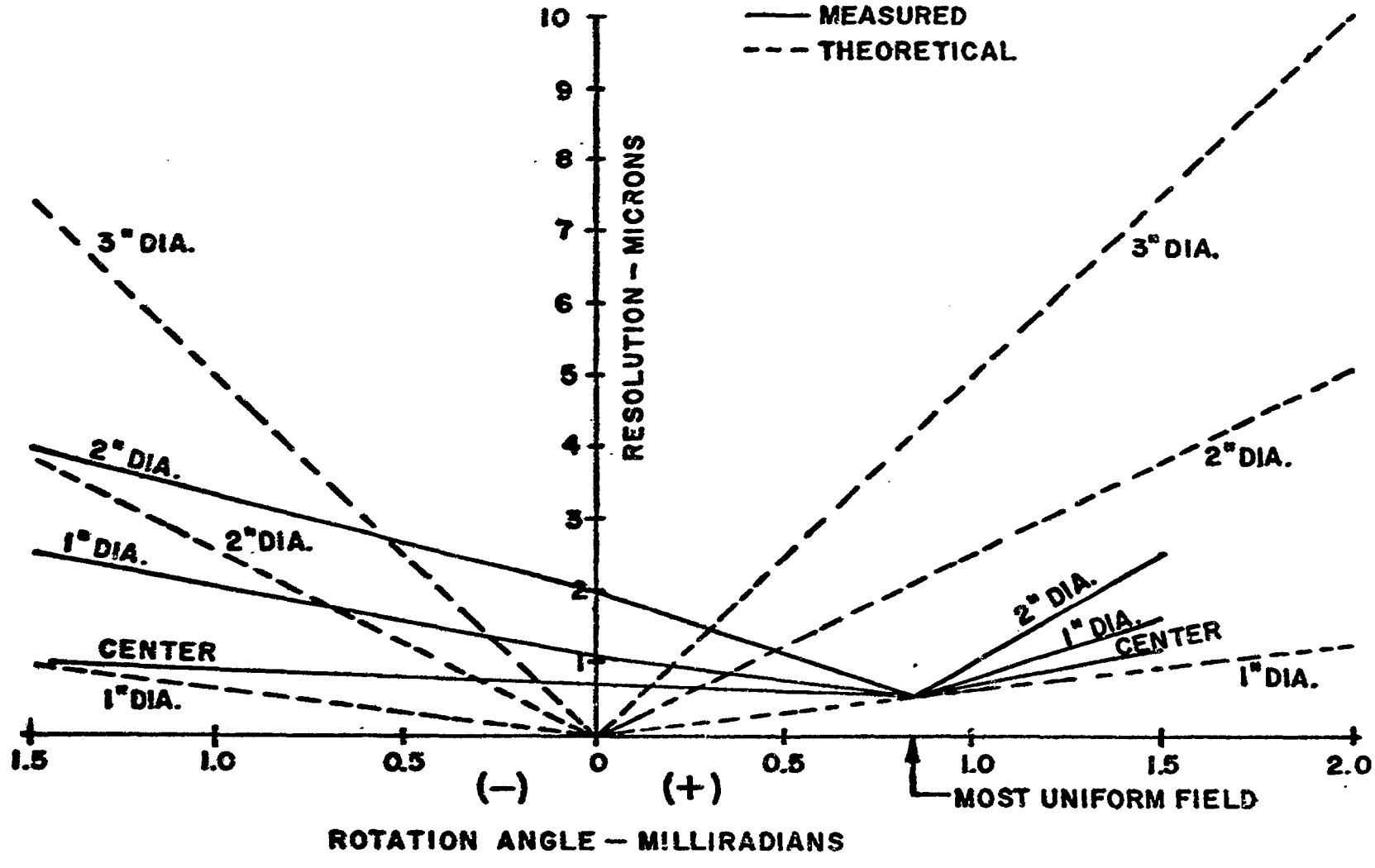



Figure 12. Defocusing Due to Magnetic Rotation

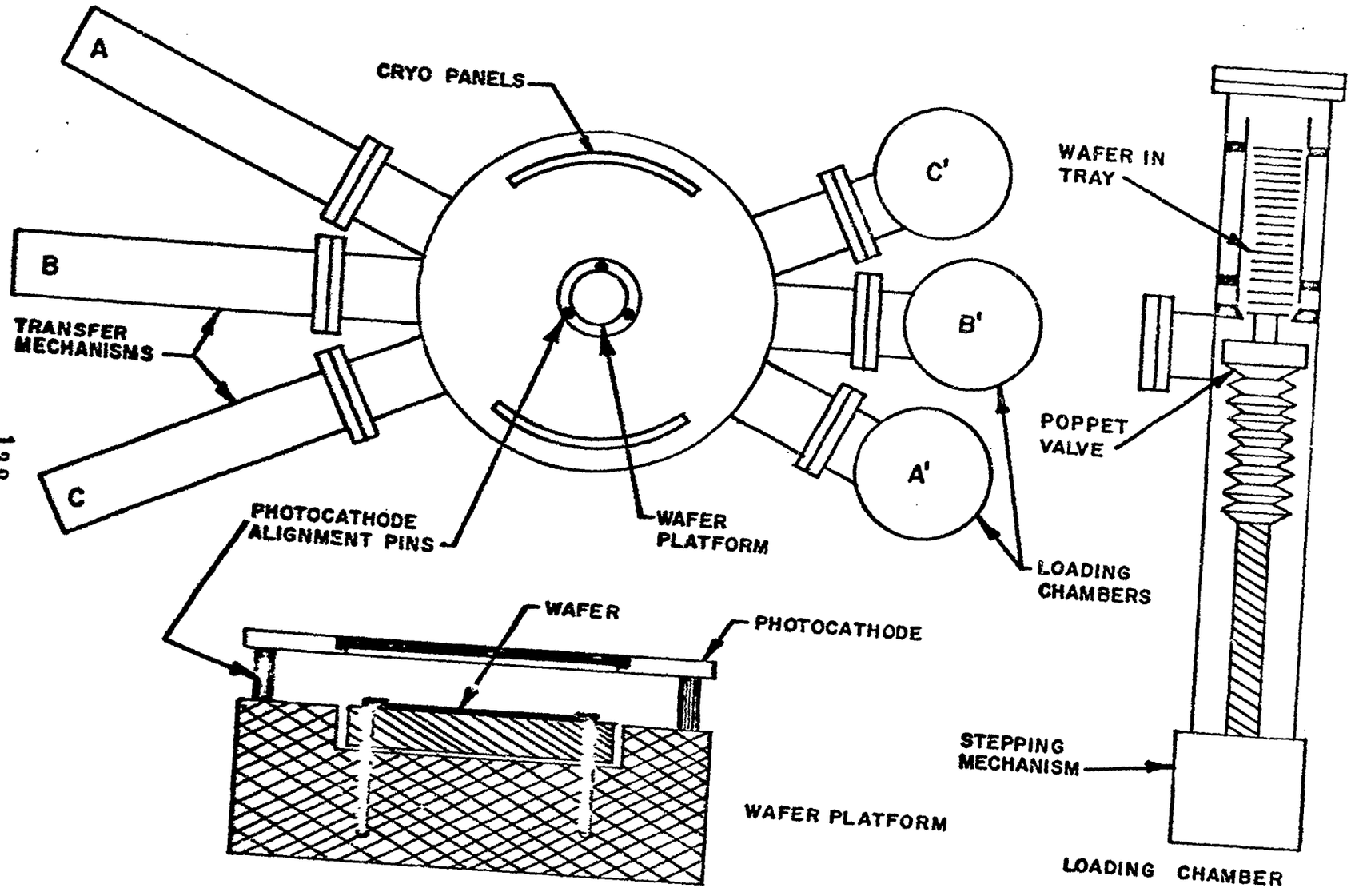



Figure 13. Automatic Wafer Handling Mechanism

# METALIZED MULTILEVEL FILM FOR HYBRID LSI INTERCONNECTS

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## I. ABSTRACT

The work described in this paper is sponsored jointly by the Naval Air Development Center and Naval Air Systems Command. The program has as one of its prime goals the development of a compatible multilayer system including LSI wafer interconnection in small or large microcircuit packages. This results in a multilayer interconnection form with high yield, low cost, and high reliability. The technical objectives are: (1) elimination of interconnection complexities, required by hybrid I/C's and large LSI wafers, (2) adequate environmental protection, and (3) increased thermal/weight efficiencies so as to achieve modules suitable for a broad range of applications from dc to high frequency or high power systems.

The technologies involve a multifunctional package that allows a multilayer interconnection capability through the use of metallized discrete dielectric films mounted on a rigid base (ceramic substrate). The design

is compatible to full automation of fabrication and electrical test. Batch fabrication techniques which are conducive to low cost and high yield are used here. No restrictions are put on integrated circuit chip configuration, i.e. plain chips may be successfully interconnected as well as chips with bumps or beam leads.

## II. INTRODUCTION

The current trend in electronic design and mechanical packaging is in the direction of multifunctional microelectronic packages. This is accomplished by mounting bare integrated circuit chips on dielectric substrates and interconnecting them will metallization and wire or face bonding techniques. Because of the small size, the interconnecting microcircuitry is frequently needed in multilayer form in order to make the proper electrical hook-up. The present method for accomplishing the multilayers of interconnections employs alternate layers of metallization and insulation on a rigid substrate, usually ceramic. The processes require as many as six deposition and etching steps. The deposition steps could be performed on many parts simultaneously. However, the imaging and etching steps are done on an individual basis. The advantage of the flexible film technique is that through step and repeat photography, many alike patterns exist on a single sheet of film, so imaging and etching are performed at one time for many patterns. In addition face bonded chips must be of the bump or beam lead configuration thus putting restraints on chip selection. The face bonded chips with bumps are not visually inspectable for joint integrity.

## III. APPROACH

### THE CONCEPT

The basic concept of the program started as a multifunctional packaging technique that allows multilayer interconnection capability through the

use of discrete metallized flexible dielectric films. The films are processed for interconnecting circuitry and then assembled with bare I.C. chips prior to placement into a package with hermetic sealing capabilities. Figure 1 shows the basic concept being discussed.

The basic construction of the multifunctional package is as follows:

The first layer of metallization is produced on a ceramic substrate in the appropriate interconnecting pattern. Many metallization materials could be used, but as an example this layer could be made from molybdenum magnanese and gold. An insulating dielectric layer is applied over the interconnecting microcircuitry to prevent shorting to other layers of conductors in the package. As an example this insulating dielectric layer was made using a high temperature polymer.

Multilayers of interconnecting circuitry are produced on a flexible dielectric film (using any desired thickness) such as

Kapton. The circuitry is produced in double sided fashion with metallized holes through the dielectric film. More than one piece of flexible film may be used if more circuitry layers are required.

Bare integrated circuit chips are bonded and interconnected to the flexible film and the assembly is than bonded and interconnected to the circuitry on the base substrate.

TECHNIQUES

The development work on the dielectric film was performed on Kapton because of its high temeprature characteristics. The dielectric film is processed to provide a series of through holes for accomplishing side to side interconnections on the film for double sided circuitry. Photo etching techniques are employed to produce the desired hole pattern in the film.

The film is then processed using techniques such as vacuum deposition and/or plating to produce metallization on both sides of the film and in the holes in an uninterrupted layer. Figure 2 shows a vacuum chamber with rotating fixture specifically designed to produce the deposited through holes. This method was found to be most consistent.

Several metallization techniques were investigated in order to arrive at the best one from a reliability and cost standpoint. One of these was a chromium-gold system. A comparatively thick (1000 Å) layer of chromium used for the base adhesion layer was followed by 25,000 Å of gold. The gold thickness was further increased to 125,000 Å or 0.5 mils through electroplating. However this approach was abandoned due to the complexity and incompatibility with production line fabrication of interconnects.

Another process studied was the deposition of aluminum through boron nitride boats. These boats are essentially a conducting intermetallic composite ($TiB_2$-BN). They are used in a variety of applications because of their ability to withstand alloying with aluminum during deposition. A boron nitride boat is shown in figure 3. This boat deposited up to 0.0003" of aluminum on Kapton film.

The third method used to metallize the films was chemical electroless nickel and copper baths. Both of these baths, although very economical, produced unreliably adherent deposits which were attached during subsequent electroplating in both acid and basic media.

Another technique to be described later in this paper shows far more promise than the previous ones. This is the electron beam bombardment of aluminum in a vacuum.

Figure 4 shows a cross section of a vapor deposited through hole. The final interconnecting conductor pattern is then produced using photoetching techniques.

Integrated circuit chips may be obtained in a number of configurations for attachment, i.e., plain, with bumps or with beam leads. This packaging concept is compatible with all forms. The chips are attached and interconnected to the flexible film using ultrasonic bonding techniques. It should be noted that the flexible characteristic of the film makes the interconnecting of plain bare chips (i.e. without bumps or beams) a practical technique. Figure 5 shows the plain bare chip bonded to circuitry on the flexible film. The bonding operation may be performed with a multipoint probe making all bonds at one time for each chip. This capability will also allow a much larger selection of the I.C. chip sources. After chip attachment is completed the assembled film is a fully electrically testable item prior to assembly into a package for hermetic sealing.

This design imposes no restrictions on final package configuration. An all alumina package or a metal can with an alumina insert are both compatible packages for housing the flexible film. As an example, figure 6 shows various steps in the processing of a typical all alumina package. Figure 6-1 shows the package as purchased. Figure 6-2 shows the interconnecting circuitry as etched on the alumina base. The next step is to isolate this circuitry from the circuitry on the flexible film. This is done by placing an insulating liquid film such as Amide-Imide in the package, drying it and then etching the required hole pattern in the dried film. This is shown in Figure 6-3. Figure 6-4 shows the flexible metallized film prior to being inserted into the ceramic package.

The interconnecting of the various layers of circuitry is accomplished by placing the flexible film on the ceramic and after proper alignment, applying heat and pressure through a multipoint tool to the proper points of interconnection. Figure 7 shows the tool and interconnected substrate. This results in the simultaneous joining of all points of interconnection between the various layers. The same procedure may be used to join additional layers of flexible film within the same package. The package is given a final electrical test and then hermetic sealed using standard sealing techniques.

## ELECTRICAL CONSIDERATIONS

One of the most important considerations in using this multilayered dielectric structure is that of capacitance due to conductor crossover. This can lead to trouble in pulse rise times if it is too high. For a typical situation where a rise time of 20 nanoseconds or less is desired, the capacitive loading should be less than 15 pf (maximum load for TTL on each output). If one mil thick Kapton is used, the capacitive load is 7.6 pf, well below the allowable figure.

Other items of interest are electrical conductivity, or conversely, conductor resistance, shielding, both electric and electromagnetic, and crosstalk. The electrical resistance of the metallization on Kapton is only 0.4 ohms per running inch, assuming a thickness of 0.0002 inches and width of 0.015 inches which is generally the case. In general, with thicknesses upwards of 100 millionth of an inch, bulk resistivity values apply.

Shielding is more a function of system design and does not apply specifically to metallized Kapton interconnection techniques within the package. This is so because ferromagnetic metal cans may be used which contain the Kapton circuitry. Judicious circuit layout will minimize crosstalk interference within the package, and outside the package other techniques can be used such as short path conductors, twisted pairs, and active filters for long conductors.

## MATERIALS and PROCESSES COMPATIBILITY

A careful review of the detailed sequential packaging and processing steps was made. In general the criteria used to judge acceptability were: metals in contact should not be susceptible to corrosion from galvanic action; processing temperatures should not exceed materials capability; processing materials (chemicals and solvents) should be able to be removed as completely as possible. There are further considerations which under long-term conditions may be important, such as the inclusion of certain plastics (polyimide) in the package. These were investigated and were found to be innocuous.

The study of processing techniques has indicated that no incompatibility exists as the total package is conceived at this time. For instance, if chips are bonded to Kapton at 150°C, there is no problem due to outgassing and subsequent contamination since Kapton's vapor pressure is still very low at 200°C. The choice of high temperature materials were initially made in order to alleviate this type of problem. Processing chemicals and solvents used to photoetch the patterns, create holes in the Kapton film, and clean the surfaces for metallization and bonding are: hydrazine ($NH_2$ $NH_2$), toluol, acetone, isopropyl alcohol, iodine, acetic acid, and trichloroethylene. Hydrazine rather than caustic soda was used to etch the Kapton to that even selective etching would result and so that no Na+ ions would remain. The other solvents are typical of those used in semiconductor manufacture, and all were electronic grade-rated. Since vapor degreasing was used to clean films and substrates, minimal residues existed on the surfaces, and they are composed of innocuous elements. Chip bonding temperatures are sufficiently low (150°C) so as not to be considered contributory to deterioration.

## THERMAL MANAGEMENT

The problem of heat removal from devices interconnected by metallized Kapton is inherently one of providing efficient thermal paths to the heat sink or exchanger. If the package housing is intimately connected to heat transfer surfaces, or if coolant (air for example) is made to pass over the package with sufficient velocity to effect thermal transfer, then the manner in which the devices are mounted inside the package becomes the critical link.

Devices that are eutectically mounted or cemented to substrates are able to expel four times the heat generated than they could if they were mounted by their electrical connections in a face-down mode. This conclusion was reached as a result of a computer study of conduction through package interface at operating power levels which would not force the device junction temperatures above 125°C. Tests were conducted which confirmed the computer analysis so that the program could be used for other similar problems in future NADC work.

## IV. FUTURE PROJECTIONS OF TECHNOLOGIES

The techniques which were developed in working with standard smaller I/C chips have also been extended to larger devices and even very large whole wafers. For instance, the method for producing etched holes led to experiments with making relatively large windows in the films. These windows accommodate larger chips (0.125" square at the present time) and ultimately will be adaptable to wafers. Concurrent with large window developments, other metallizing and conductor etching efforts led to a configuration which uses heavy metallizations or beam like conductors to connect to the pads of very large LSI wafers. These conductors which are an integral part of the flexible film carrier can be bonded simultaneously, reducing assembly time and costs. The devices have the advantage of being mounted in intimate thermal contact with the substrate without sacrificing any interconnection features that the flexible film technique provides.

Provisions are being made for nuclear radiation hardening in the overall system of packaging. This is being done through material selection for survival compatibility in radiation environments. The all-aluminum metallization on Kapton is an example of this.

## V. CONCLUSIONS

In summary, we have shown a series of techniques which are important to advanced in hybrid and large LSI wafer interconnection packaging. These techniques have the following advantages:

1. Batch processing allows for significant savings in time and effort.

2. Although more processing steps are required than on other current multilayer microcircuit packaging techniques, more parts can be processed simultaneously offsetting the additional cost.

3. Pin-hole problems in dielectric layers are eliminated with the discrete flexible film.

4. Homogenous monometallic interconnections between circuitry on opposite sides of dielectric film are produced with the continuous metallization process.

5. No restrictions are put on I.C. chip configurations, i.e., plain chips may be successfully interconnected as well as chips with bumps or beam leads.

6. The compliant characteristic of the dielectric film allows for simultaneous bonding of all interconnecting points on the flexible film to circuitry on base substrate.

7. Maximum thermal dissipation is possible by eutectic bonding all chips to the rigid substrate base when necessary.

8. The interconnected flexible film assembly can be electrically tested prior to bonding to the rigid substrate base.

9. Automated manufacture and automated test are possible on the dielectric film level as well as on the final assembly.

10. Since the number of processes are reduced, and most of these processes are automatable, then the cost for a throw-away modular microcircuit package is reduced.

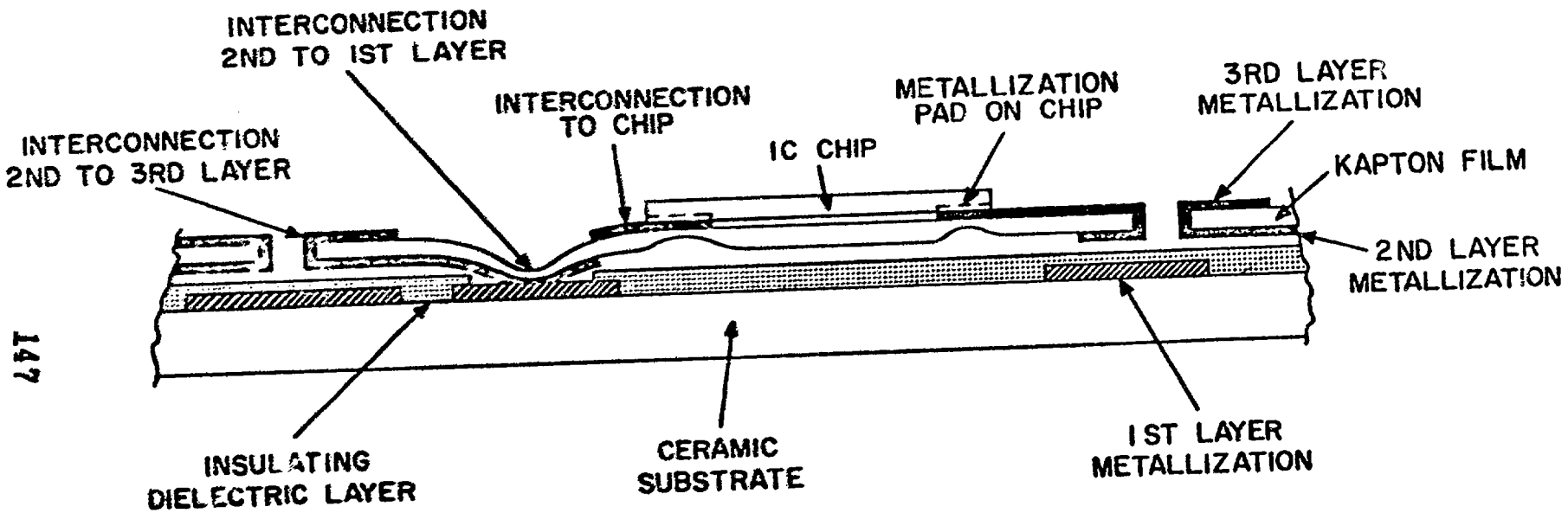


Figure 1 Basic Concept for Multilayer System

Figure 2 Evaporator with Rotating Fixture Suspended From Top Plate. Thickness Monitor is Placed Adjacent to Jar.

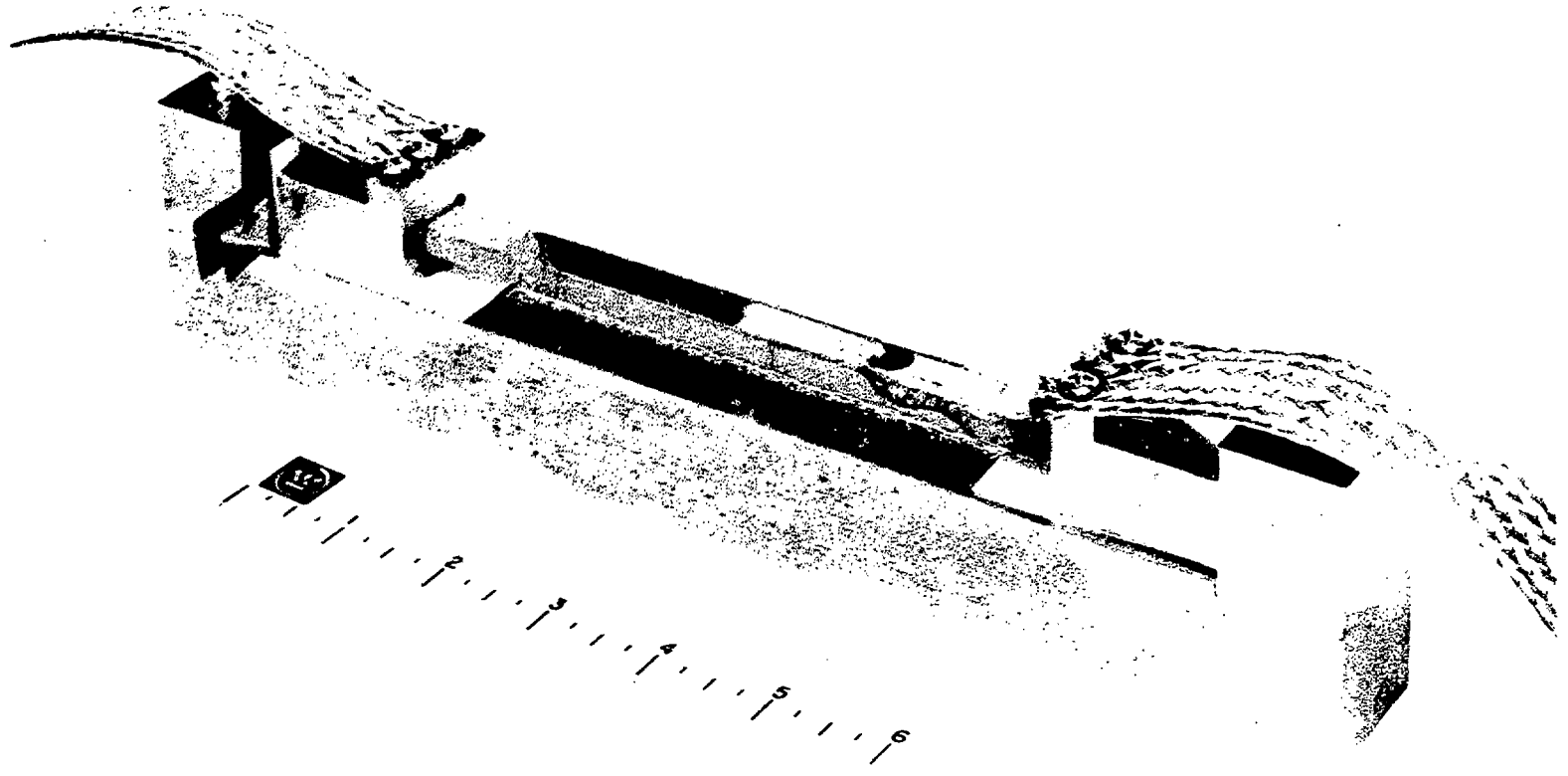

Figure 3 - Boron Nitride Boat Containing Aluminum

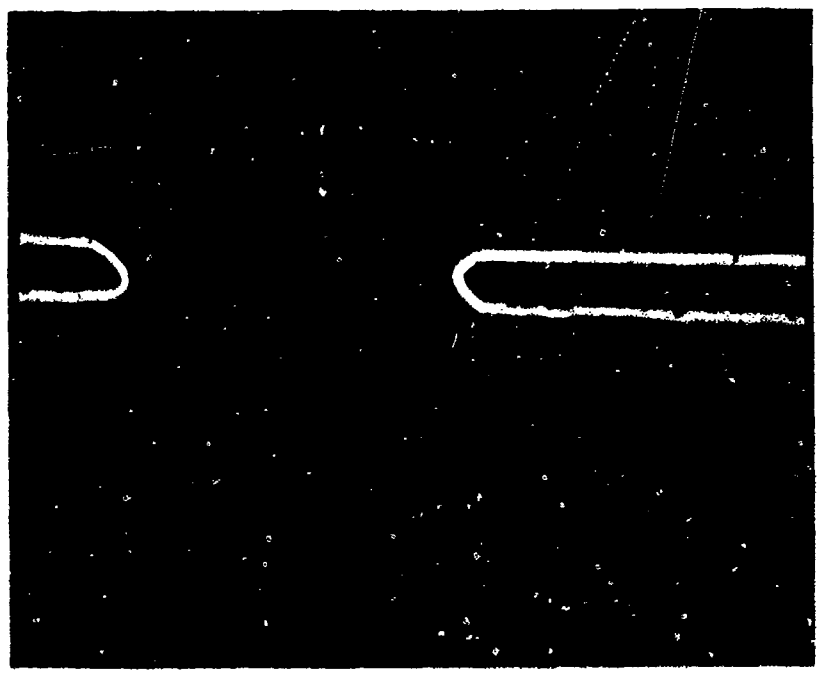

Figure 4 - Cross Section of Joint Formed on Rotating Fixture in Vacuum Chamber

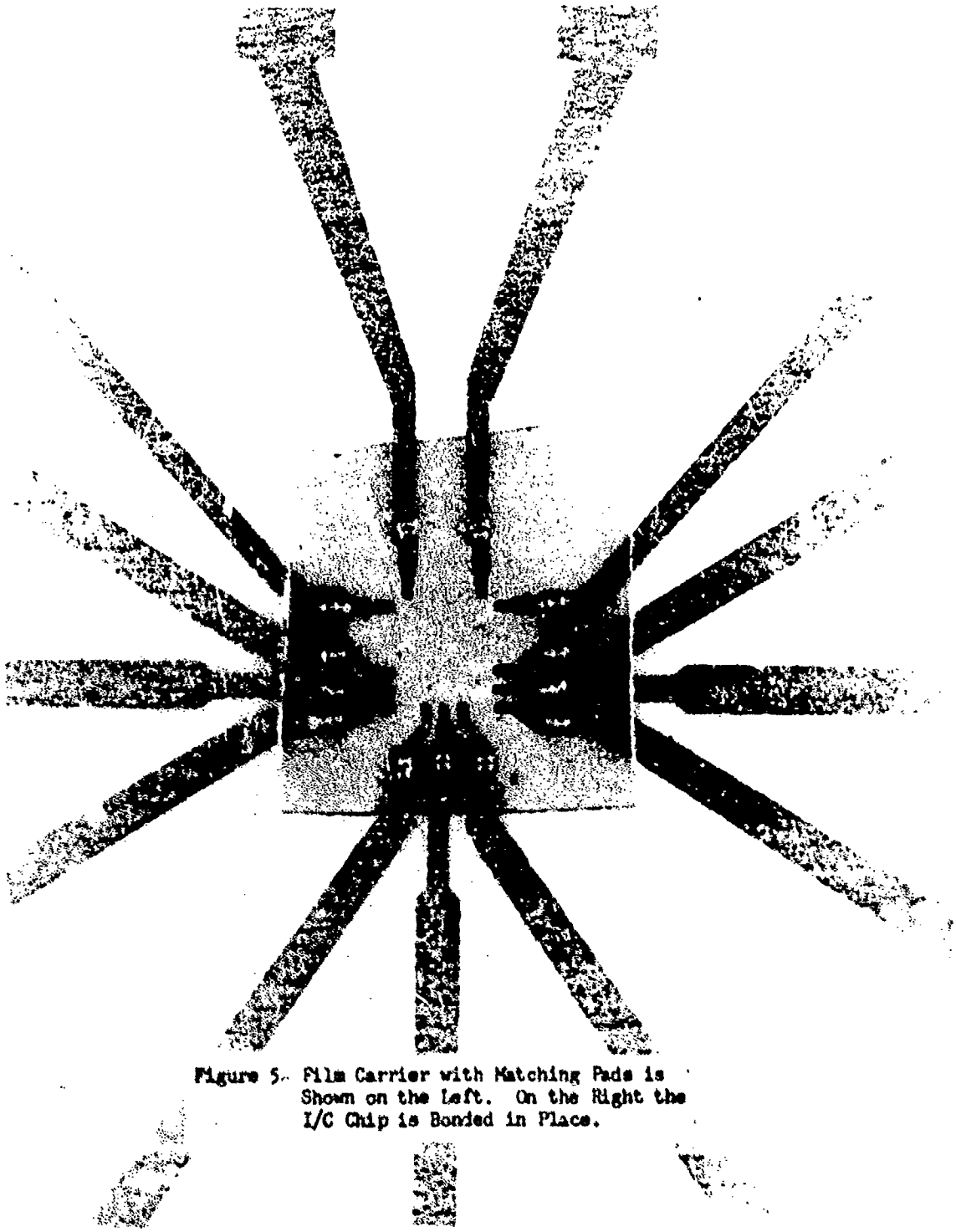

Figure 5. Film Carrier with Matching Pads is Shown on the Left. On the Right the I/C Chip is Bonded in Place.

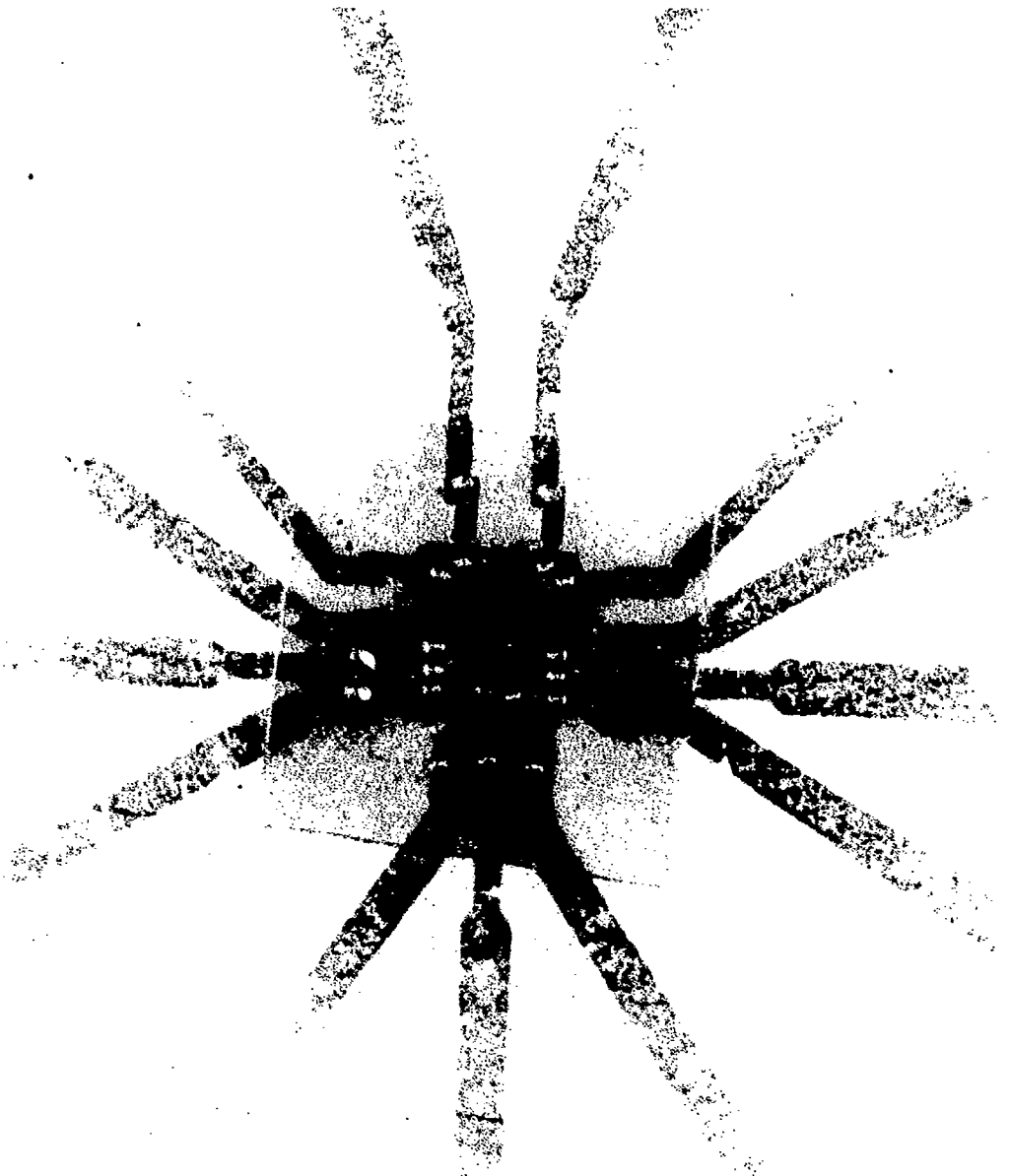

Figure 5: Film Carrier with Matching Pads is Shown on the Left. On the Right the I/C Chip is Bonded in Place.

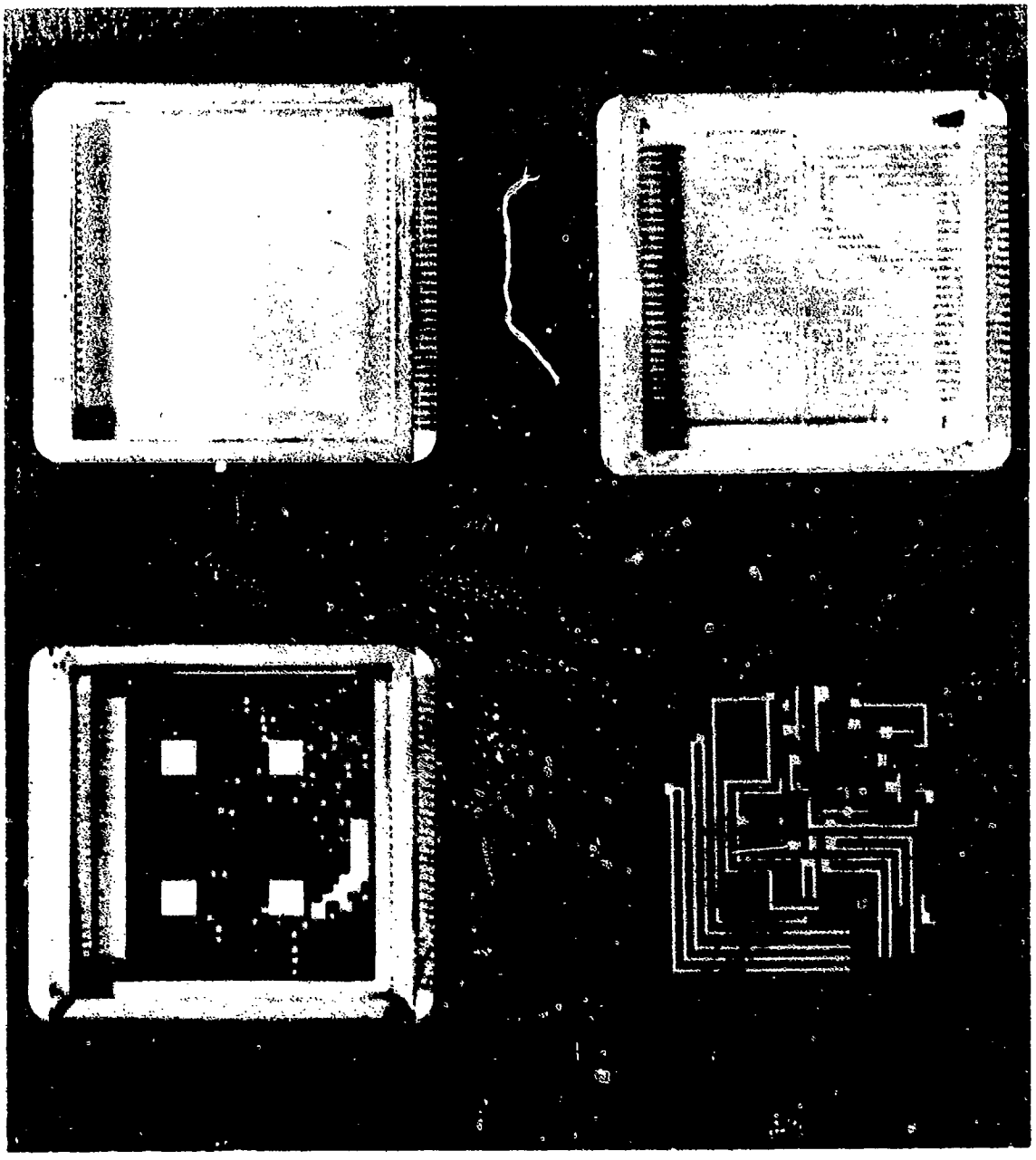


Figure 6 Processing Steps for 3 Layer Circuitry

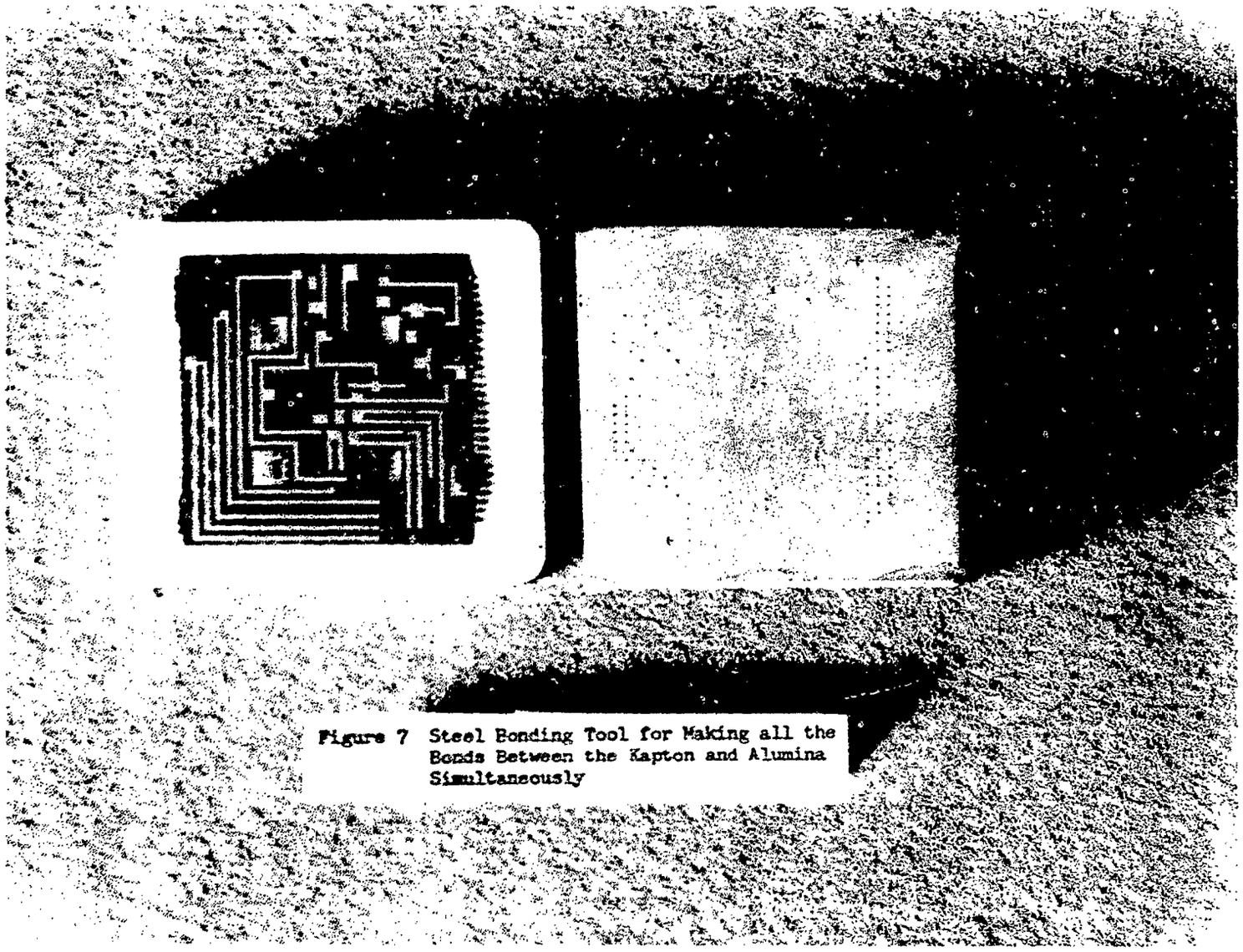

Figure 7 Steel Bonding Tool for Making all the Bonds Between the Kapton and Alumina Simultaneously

# DESIGN AND DEVELOPMENT OF
# THE BUILDING BLOCK MODULE
# FOR THE ADVANCED AVIONICS DIGITAL COMPUTER

FOR PRESENTATION AT

THE ADVANCED DIGITAL TECHNOLOGY CONFERENCE

JUNE 8 - 10, 1971

SPONSORED BY

NAVAL AIR SYSTEMS COMMAND

AUTHOR

L. LAERMER
DIGITAL COMPUTER DEPARTMENT
SINGER-KEARFOTT

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## ILLUSTRATIONS

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INTRODUCTION

The Kearfott Division of Singer-General Precision, Inc., in combination with Frenchtown/CFI, has developed under NASC sponsorship the AADC Building Block Module that is capable of retaining a 3-inch diameter, silicon wafer or a 3-inch diameter hybrid circuit substrate. The attendant specified requirements are:

- External Connections - 300
- Power Dissipation - 20 watt
- Power Densities - 3 watts/sq in
- Environment MIL-E-5400 Class 4X
- Storage at 200°C
- Hermetically Enclosed
- Guiding, Keying and Clamping provisions.

The module is illustrated in Figure 1. The design incorporates features that facilitate bonding and interconnection of the substrate, while providing an efficient interface with the next higher level package. The major features are:

- Size 4 in x 4 in
- Weight 0.4 lb
- Integral heat exchanger
- Parallel cooling system
- Zero insertion force 300 terminal interconnect system (via cam operated connectors)
- Fool-proof module keying, guiding and locking
- Vibration resonant frequencies above 2000 Hz

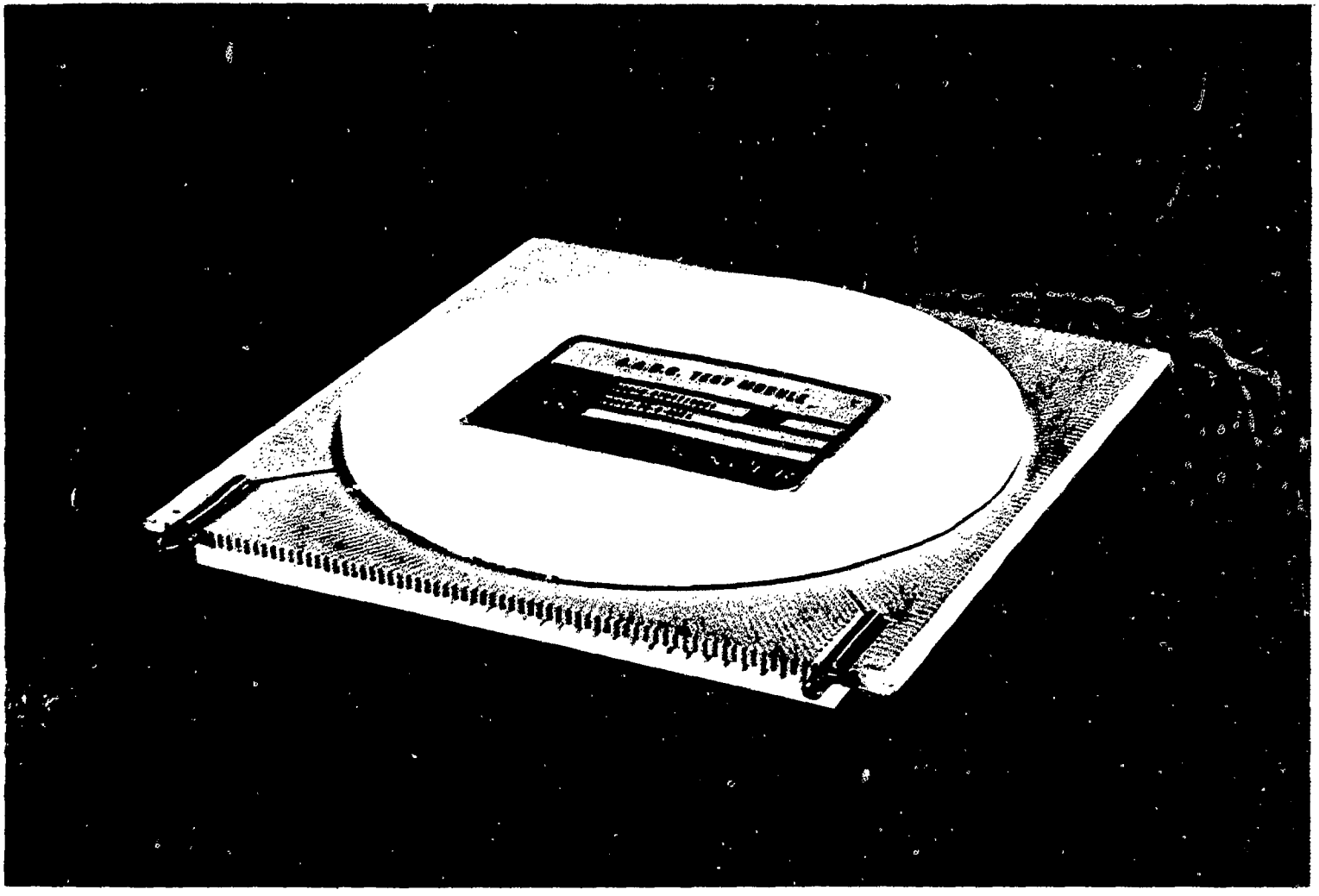


FIGURE NO. 1 - AADC -
BUILDING BLOCK MODULE

- High speed circuit compatibility
- Ease of replacement.

Prior to arriving at this configuration, an extensive trade-off study was undertaken. The significant elements of the study are highlighted.

DESIGN TRADE-OFF

The design optimization process concerned itself with trade-offs in three major areas:

1. Interface with the next higher level package.
2. Mounting and interconnection of the 3-inch diameter wafer or hybrid substrate.
3. Module sealing, line routing and manufacturing processes.

Connector configurations, cooling techniques, keying, guiding and module retention methods were examined. A wafer bonding interface, having adequate flatness without compromising accepted manufacturing techniques, was developed. Substrate and wafer mounting and interconnecting techniques were developed that are compatible with the metallurgical peculiarities of the wafer, and the module sealing and hermeticity requirements.

Characteristics that are unique to the module, such as distribution of leads from the wafer to the external interconnection points, were optimized. Manufacturing techniques and processes related to designs using Kovar, ceramics, glass and other materials were studied in depth. A cost effective mix of current and advanced manufacturing techniques is reflected in the design.

THERMAL CHARACTERISTICS

It was recognized that the thermal interface would be a major factor in establishing the module configuration since integrated circuit Mean Time Between Failure (MTBF) decrease rapidly as the operating temperature increases. An efficient cooling mechanism became a primary consideration

First, the characteristics of the cooling air that would most likely be supplied to the module and component operating temperatures were established. Current high performance aircraft specifications were used as a guide.

| | Worst Case | Avg. |
|---|---|---|
| Cooling Air Flow (lb/min/kw) | 8 | 10 |
| Cooling Air Temp (°C) | 55 | 30 |
| System Pressure Drop (in $H_2O$) | 3.0 | 2.0 |
| Component Temperature (°C) (i.e., at wafer interface) | 90 | 55 |
| Δ+ above inlet cooling air (°C) | 35 | 25 |

Thus, it is fair to assume that 0.2 lb/min of cooling air will be supplied to the 20-watt module. Temperature rises of 25°C from inlet cooling air to wafer would be a minimum design objective. To achieve the desired performance, the characteristics of standard cooling techniques were reviewed. Initially, due to their simplicity and low cost, existing techniques that make use of conductive cooling to heat exchangers were reviewed for possible application.

CARD CONFIGURATIONS

Designs of this type employ a metal-cored card which conducts the heat from the components to the heat exchanger via thermal clips or similar clamping devices as illustrated in Figure 2. A card design employing this approach, which has been used extensively at Kearfott over the past six years, is illustrated in Figure 3.

Power levels of 5 watts with average power densities of 200 MW/sq in are typical. A design approach employing these concepts extended to the LSI module, yields configuration similar to that illustrated in Figure 4.

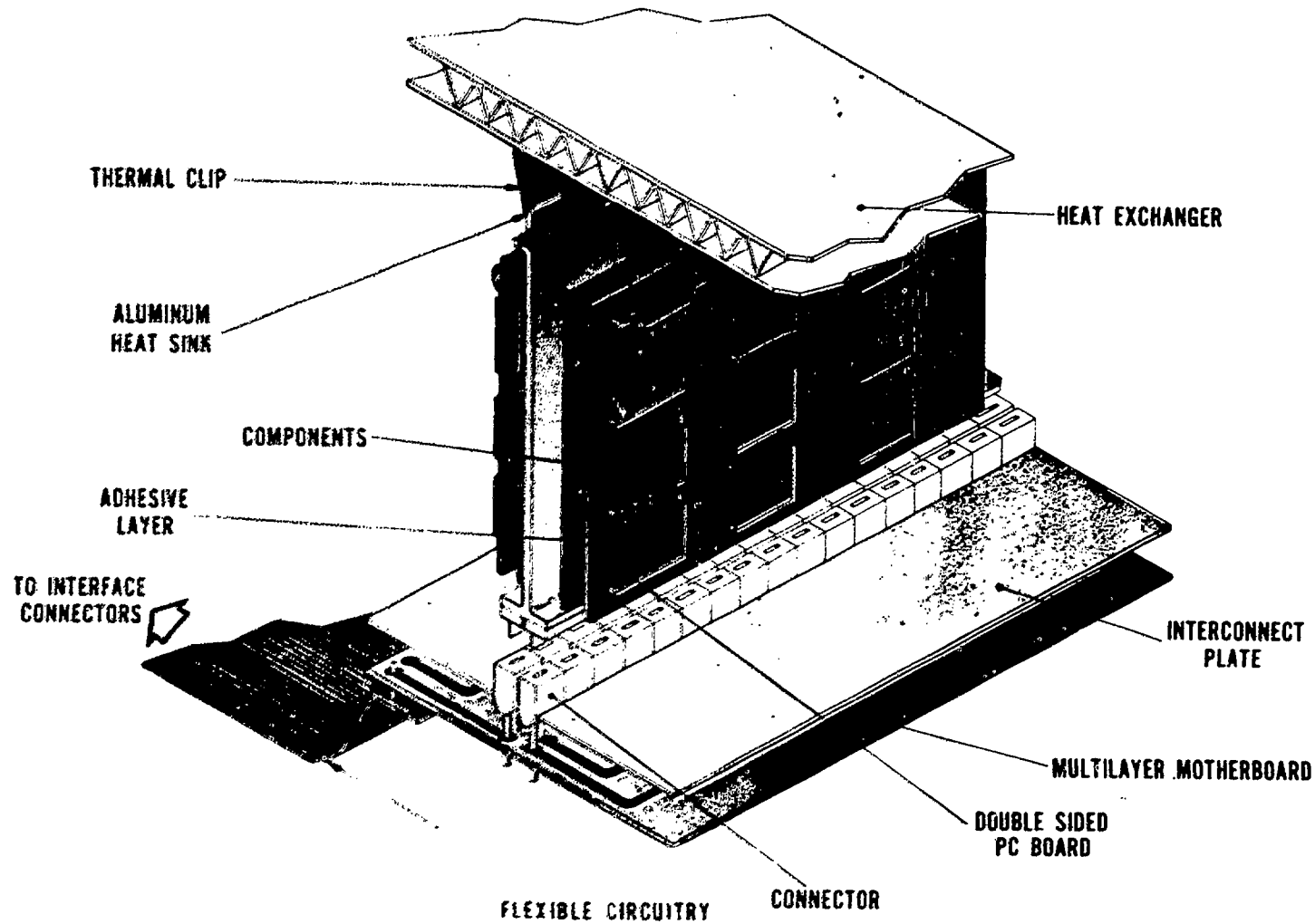
The module would have leads on four sides and be mounted on a circuit board laminated to a heat sink. Good thermal contact is provided by a compliant material between the module and the board. A wafer dissipating 20 watts will experience a temperature 78°C above the cooling air temperature. A level that is unacceptable in light of our criteria of 25°C. The temperature rises are distributed as follows:

Air Rise - 13°C
Air to Heat Exchanger - 25°C
Thermal Clip to Frame - 15°C
Frame Edge to Center of Card through Core - 25°C.

Improvements in clamping and increased heat exchanger size will reduce the gradients. However, the magnitude of the improvement in thermal characteristics cannot be justified in terms of weight and size. It becomes apparent that a more direct cooling technique was required. Designs utilizing features that have the module mounted on thin circuit

SINGER
KEARFOTT DIVISION

FIGURE NO. 2 CONDUCTIVE COOLING CONFIGURATION



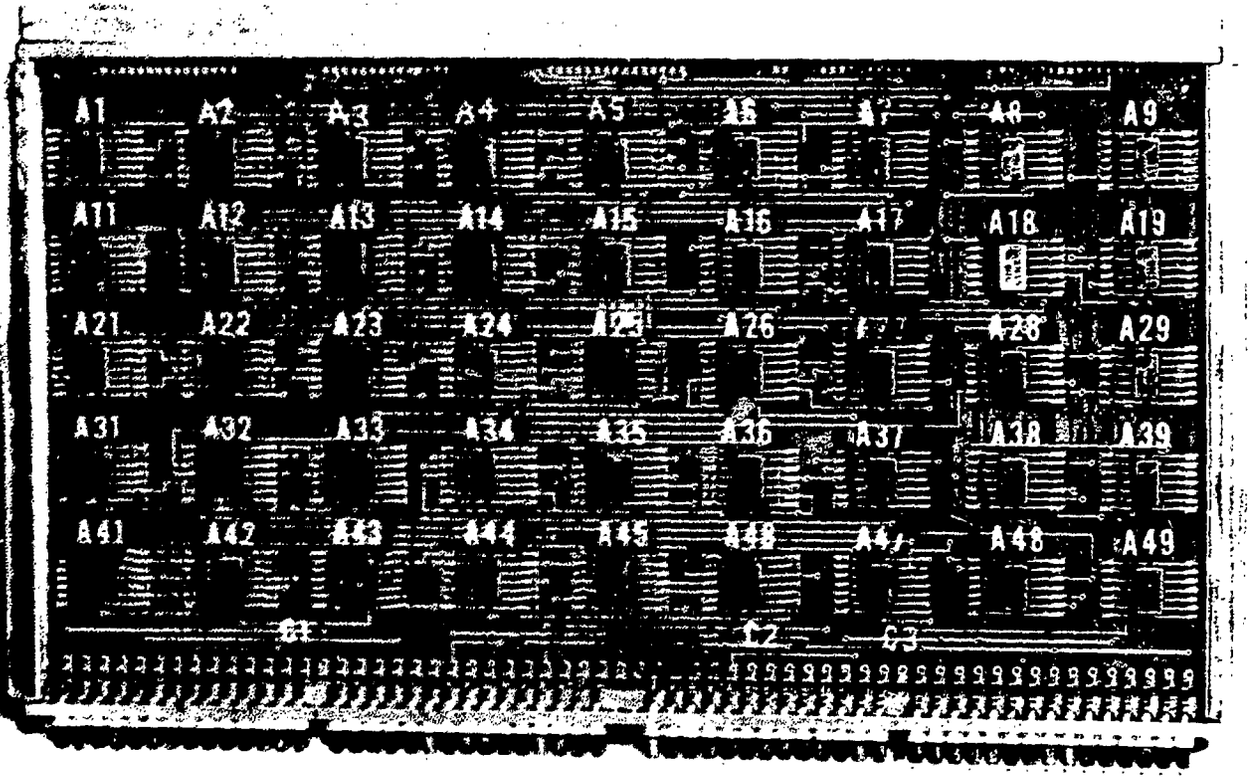
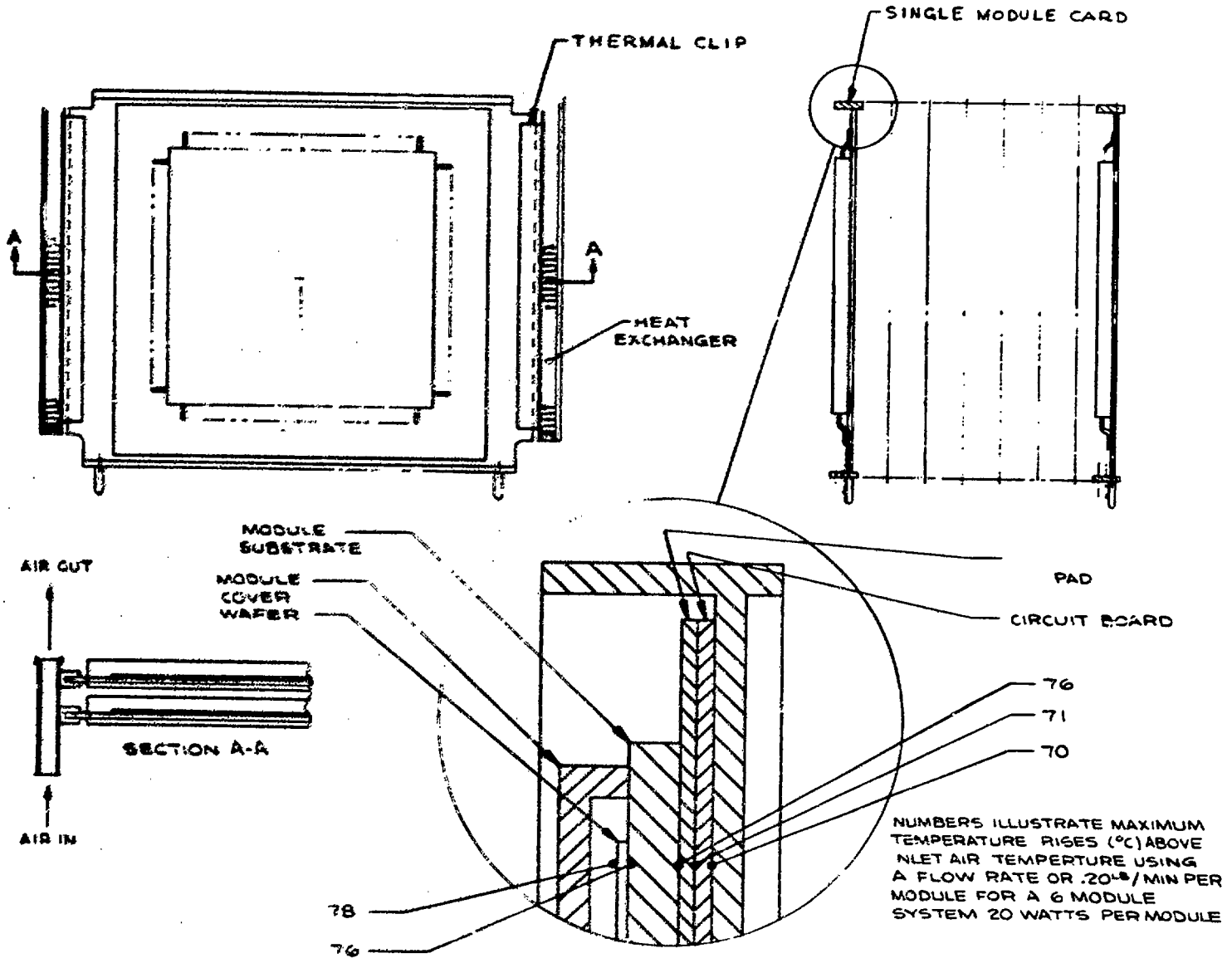



FIGURE NO. 3
CONDUCTIVE COOLING CARD




CONDUCTIVE COOLING CONFIGURATION **FIGURE NO.- 4**

cards laminated directly to a heat exchanger were considered next.

The approach is similar to the hollow card cooling technique which is currently being employed in the Kearfott SKC-2000 Computer series. The module would be mounted on a hollow card as illustrated in Figure 5. Cooling air now passes directly behind the power dissipating components. The design concept applied to the LSI module results in a configuration similar to Figure 6.

The temperature rise from inlet cooling air to the silicon wafer is 26°C. Thus, the design objective has been achieved. The improvement over the previous design can be attributed to the reduced length of the thermal conducting path and the increased heat exchanger surface area. Figure 7 compares the maximum temperature rise above the cooling air inlet temperature vs the flow rate per module and clearly illustrates the thermal advantage of the latter design.

Figure 8 is a plot of pressure drop through the heat exchangers. System entrance and exit losses would be similar for both systems. For six-module systems, the losses would be in the order of 0.5 inches of water with a cooling air flow rate of 0.2 lb/min per module. It is apparent that both designs have pressure drops that are well below the design goal of 2 inches of water for a flow rate of 0.2 lb/min module.

The design employing a solid core represents a serial cooling flow system wherein the pressure drop through the heat exchanger increases

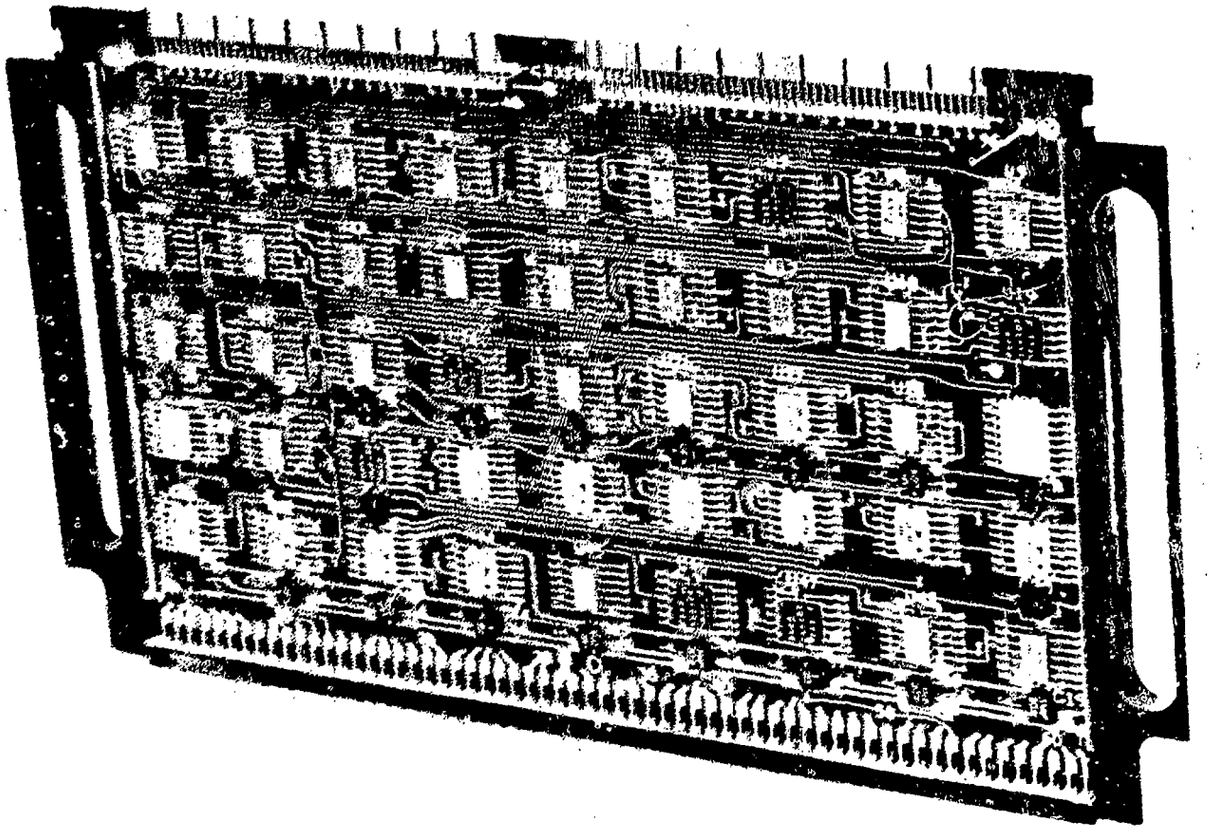
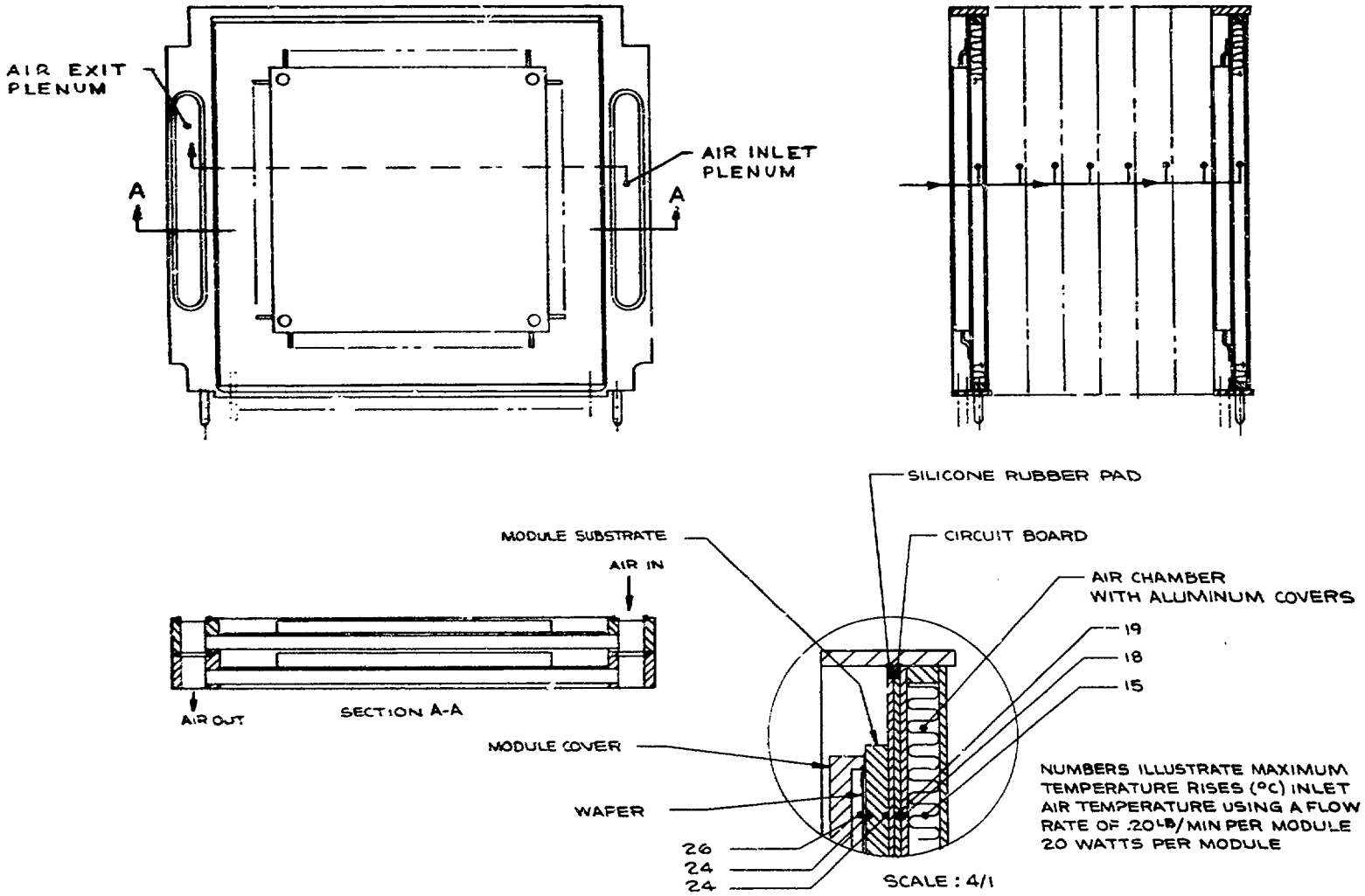
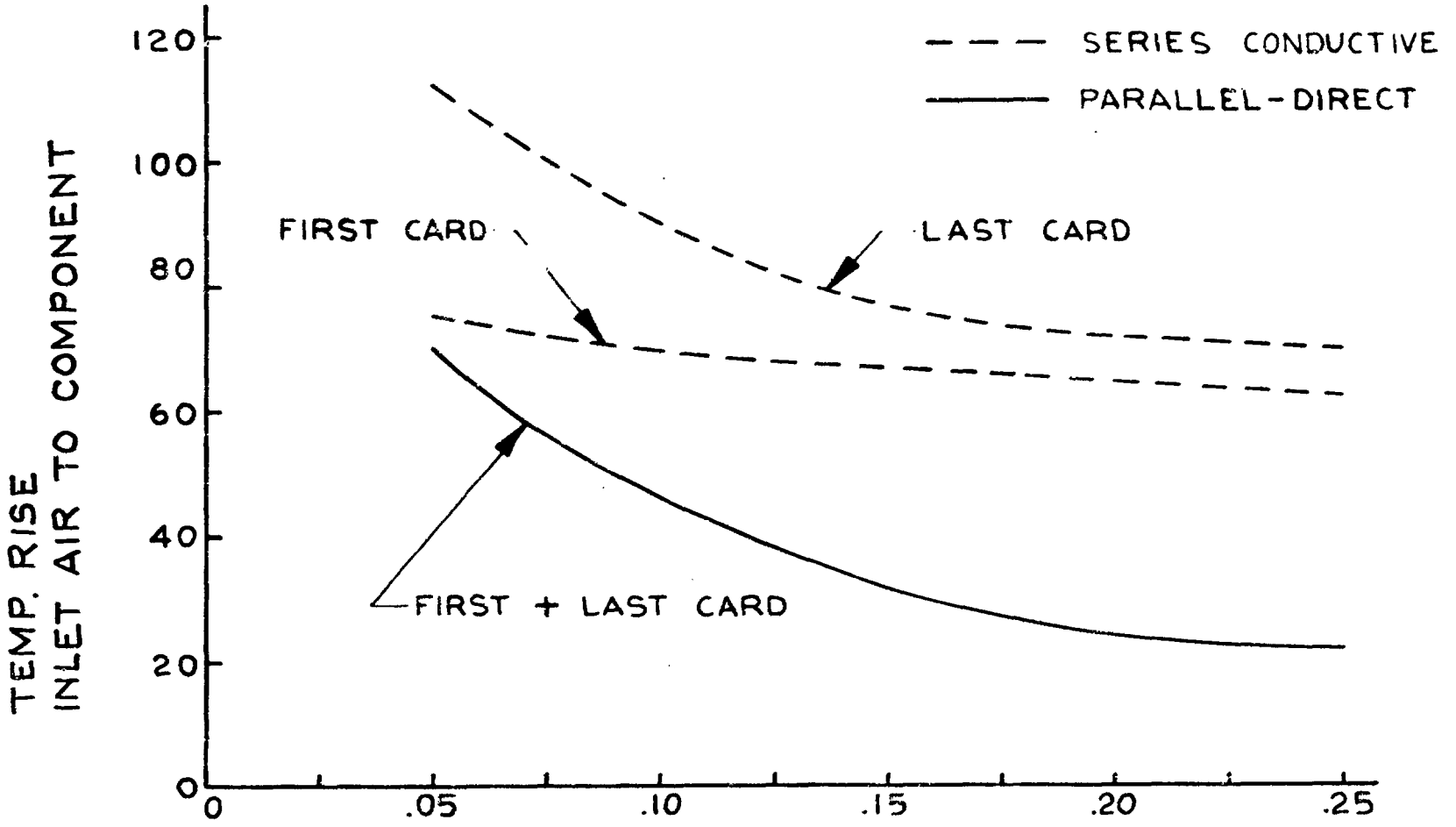


FIGURE NO. 5
SKC-2000 CARD



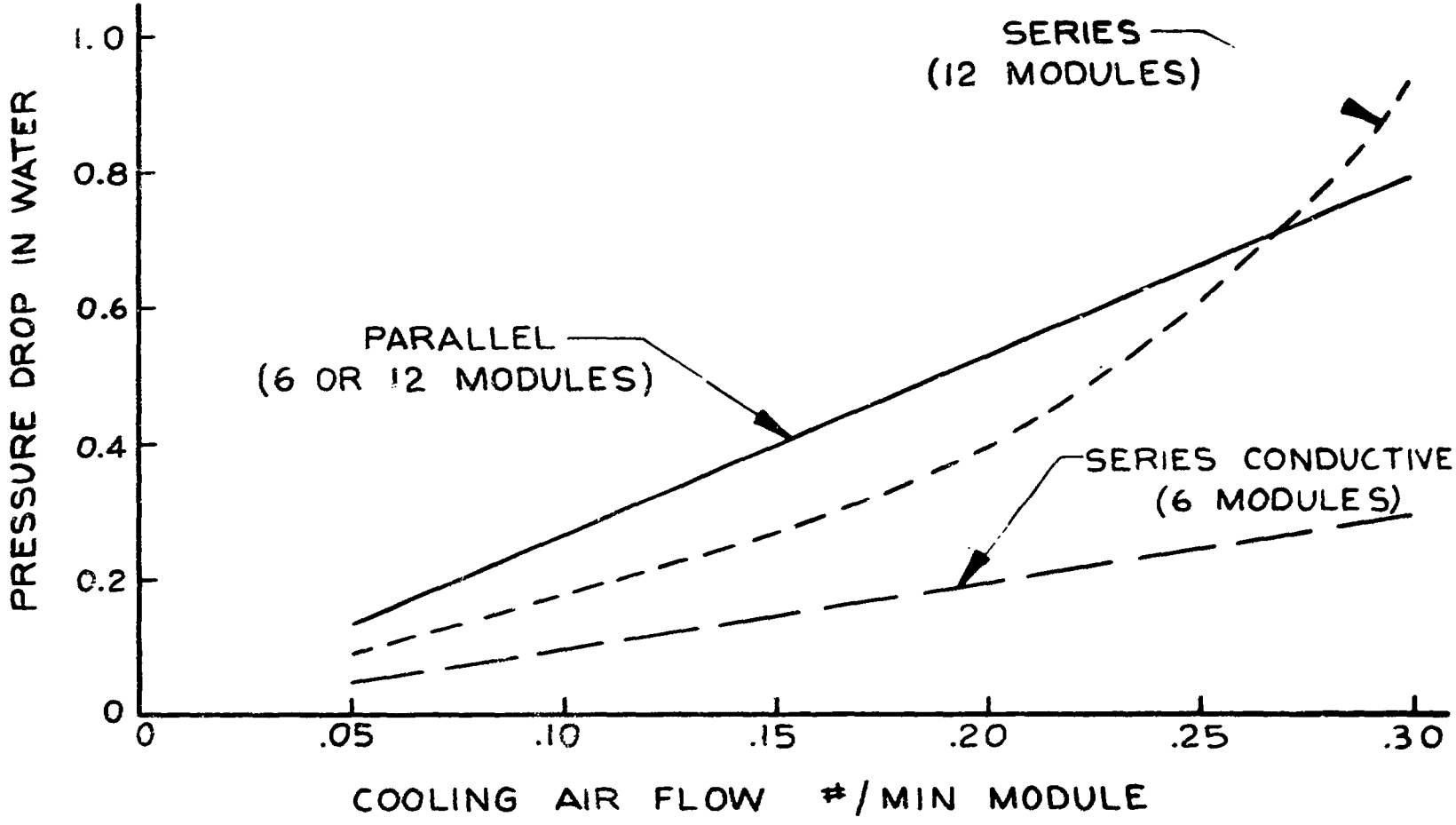

DIRECT COOLING CONFIGURATION

FIG 6




THERMAL CHARACTERISTICS
HIGHER LEVEL PACKAGE

FIG 7




PRESSURE DROP CHARACTERISTICS
THROUGH HEAT EXCHANGER
FIG 8

with the number of modules per system. The latter design represents a parallel flow system. Pressure drop remains constant regardless of the number of modules.

The latter design, (Figure 6), has the basic features that will meet the keying, guiding and card retention requirements. However, bringing out 300 leads from the lower edge of the assembly will preclude the use of a connector having a low insertion and removal force without impacting size. A 300-pin pressure type connector placed along the lower edge would most likely require a five row pin configuration resulting in a card width of 0.500 inch. Card withdrawal and insertion forces would be higher than 100 lb. The line fan out to the connector would be a major factor in increasing the card size to 7 in x 6 in.

INTEGRAL HEAT EXCHANGER DESIGN

A design that retains the thermal advantages of direct cooling and eliminates the problems associated with the connector evolved after several more iterations. The configuration was illustrated in Figure 1.

The significance of an integral heat exchanger and a zero force connector system can now be fully appreciated. The integral heat exchanger design further improves the thermal characteristics of previous approaches. Elimination of the system interface board aids in the solution of the connector problem. A system package having minimum size (4x4x.35) and weight (0.4 lb) is now realized.

The unit consists of a ceramic slab containing the line routing from the 15 external connector terminations along each of the two edges to the 3-inch wafer. A Molybdenum Manganese (Mo/Mn) metalized sealing ring facilitates hermetic sealing of the ceramic or Kovar cover. Keying pins which guarantee a unique module location in the higher level system package are brazed to the base slab. The heat exchanger is cemented to the back of the base slab. Interconnections to the system are made via a set of cam operated connectors along each of the two edges, thereby insuring zero insertion force. Additional design details will be described later.

## HEAT EXCHANGER

The heat exchanger was sized to insure a maximum component temperature of 25°C above the inlet air temperature. All heat is removed by the cooling air. Heat lost to, or infiltrated from, a typical environment can be considered negligible when several modules are contained in a higher level package.

Various materials, metal and ceramic, have been considered for the heat exchanger. Kovar offers no significant advantage over $Al_2O_3$, both materials have similar thermal conductivity. High conductivity metals, such as aluminum and copper, introduce a thermal stress problem. It appeared that a dry pressed ceramic heat exchanger would provide the desired thermal performance without having a significant cost impact. A series of thermal analyses were performed to establish the advantages

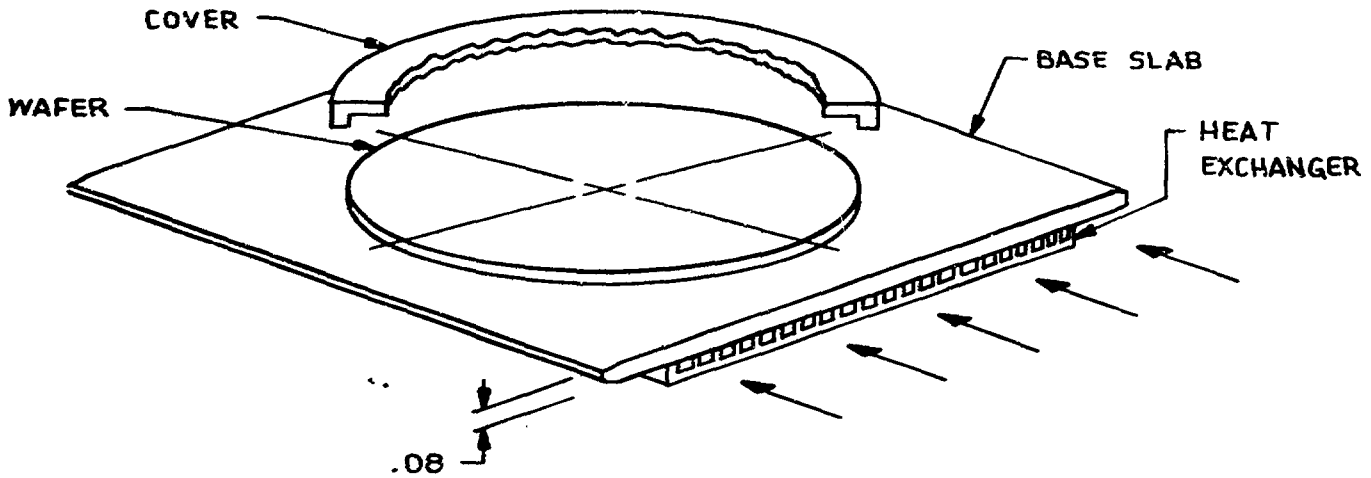
of BeO and various heat exchanger configurations.

Table I lists the average component temperatures for $Al_2O_3$ and BeO designs. BeO has a thermal conductivity approximately 9 times greater than $Al_2O_3$. The 30°C cooling air is supplied at a flow rate of 0.1 and 0.2 lb/min with 20 watts of power uniformly distributed over the wafer. The performance of the interrupted fin and the continuous fin heat exchanger is illustrated in Table I.

It appears that for most applications an all-$Al_2O_3$ design employing a finned heat exchanger is quite adequate. When it is desired to limit the temperature gradients, an $Al_2O_3$ base with a beryllium heat exchanger is optimum. No justification appears to exist for an all BeO design when the power is 20 watts per module and uniformily distributed.

WAFER INTERFACE

Having decided on the general configuration, the wafer bonding, module sealing, and wafer interconnect design details were resolved. The designs had to be evaluated in light of available and advanced manufacturing techniques. The degree to which the state-of-the-art could be extended and still realize a readily producible module became a major consideration. The design optimization process can be most effectively illustrated by lescribing the relative characteristics of approaches that were given serious consideration. The material trade-offs were narrowed to $Al_2O_3$, BeO, Kovar-glass and their combinations since their




| MATERIAL | $Al_2O_3$ BASE-$Al_2O_3$ HEAT EXCHANGER | | | | BeO BASE-BeO HEAT EXCHANGER | | | | $Al_2O_3$ BASE-BeO HEAT EXCHANGER | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| FIN | CONTINUOUS | | INTERRUPTED | | CONTINUOUS | | INTERRUPTED | | CONTINUOUS | | INTERRUPTED | |
| COOLING AIR LBS/MIN | 0.1 | 0.2 | 0.1 | 0.2 | 0.1 | 0.2 | 0.1 | 0.2 | 0.1 | 0.2 | 0.1 | 0.2 |
| AVG. WAFER TEMPERATURE | 65.1 | 57.0 | 59.7 | 49.7 | 62.9 | 53.3 | 59.4 | 48.0 | 63.9 | 53.9 | 60.5 | 48.7 |
| AXIAL GRADIENT | 18.2 | 15.3 | 17.0 | 14.2 | 3.0 | 3.2 | 3.1 | 3.1 | 4.8 | 5.8 | 5.1 | 5.3 |
| MAX WAFER TEMPERATURE | 70.9 | 72.3 | 66.0 | 55.3 | 63.8 | 53.8 | 61.0 | 48.5 | 65.3 | 55.5 | 62.7 | 50.6 |

WAFER INTERFACE TEMPERATURE
20 WATT MODULE 30°C INLET AIR TEMPERATURE

TABLE I

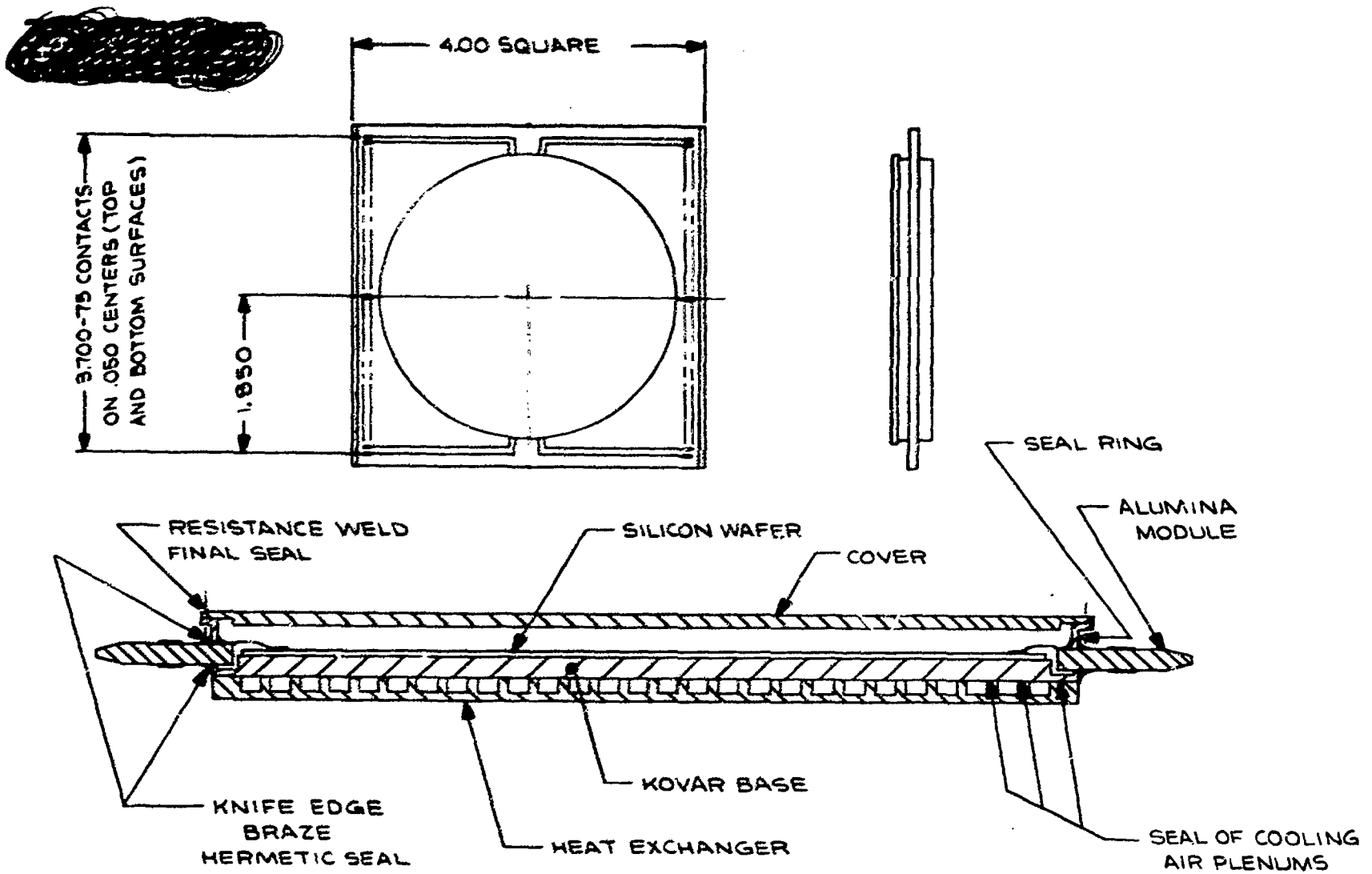
thermal expansion coefficients approach that of silicon and hybrid substrates. Table II represents a summary of the combinations that received most serious consideration. Designs employing Kovar for the base and cover were eliminated due to their reliance on glass for electrical insulation of the leads. Potential cracking problems, associated with a 300 lead glass header during processing and during thermal shock testing, proved to be the major disadvantages. In addition, an all Kovar-glass design did not offer sufficient flexibility in fanning out the 300 leads. Thus, a design employing a ceramic base slab appeared to offer optimum flexibility and reliability. Techniques for screening and firing MoMn line patterns on $Al_2O_3$ or BeO at the required densities are well established and appeared ideally suited for the 300 line pattern that had been envisioned. All ceramic packages or those employing a combination of ceramic and Kovar remained to be considered.

## CONFIGURATION TRADE-OFFS

A configuration consisting of a combination of Kovar and $Al_2O_3$ is illustrated in Figure 9. The design represents an extension of techniques used by several manufacturers of I.C. packages. A Kovar slug is brazed, via a knife edge seal, to a MoMn metalized ring on the base slab. The slab contains the interconnect line work to the edge pads. Figure 9 contains a cross-section of the seal area. MoMn line pattern is fired, then covered with a ring of ceramic glaze into which the MoMn sealing ring is fired. A Kovar seal ring is brazed to the MoMn. Resistance welding or soldering can be used to join the cover to the Kovar

# TABLE 2
## MODULE-MATERIAL COMBINATIONS

| COMBINATION NO. | BASE | COVER | BASE COVER SEAL | LEAD SEAL | HEAT EXCHANGER |
|---|---|---|---|---|---|
| 1 | KOVAR | KOVAR | RESISTANCE WELD LASER OR ELECTRON BEAM. WELD SOLDER COLD WELD | CLASS | CERAMIC KOVAR |
| 2 | KOVAR | CERAMIC | SOLDER | CLASS | CERAMIC KOVAR |
| 3 | CERAMIC-KOVAR SLUG -KOVAR SEAL RING | KOVAR | SAME AS NO. 1 | CERAMIC GLAZE | CERAMIC KOVAR |
| 4 | CERAMIC-KOVAR SLUG | CERAMIC | SOLDER-METALIZED SEAL RING | CERAMIC GLAZE | CERAMIC KOVAR |
| 5 | CERAMIC-KOVAR TAPE SEAL RING | KOVAR | SAME AS NO. 1 | CERAMIC TAPE | CERAMIC KOVAR |
| 6 | CERAMIC-TAPE | CERAMIC | SOLDER-METALIZED SEAL RING | CERAMIC TAPE | CERAMIC KOVAR |
| 7 | CERAMIC-KOVAR DRY PRESS SEAL RING | KOVAR | SAME AS NO. 1 | CERAMIC GLAZE | CERAMIC KOVAR |
| 8 | CERAMIC-DRY PRESS | CERAMIC | SOLDER-METALIZED SEAL RING | CERAMIC GLAZE | CERAMIC KOVAR |




CERAMIC – KOVAR BASE MODULE DESIGN
FIG 9

ring. The design has several favorable features.

- The processes permit machining the Kovar slug so that a flatness of better than 0.0015/inch can be maintained at the wafer mounting interface.
- A recessed surface can be provided for upbonding.
- Cover sealing can be confined to a localized heating process, resistance welding being a typical method.

The disadvantages are:

- The package seal depends on additional brazed joints
- The heat exchanger surface is limited to the slug diameter
- The option for generating an interconnect pattern within the cavity on the module base is eliminated.

Thus, a design employing an all-ceramic base slab appears to offer significant advantages provided the flatness requirements of 0.0015/inch can be maintained at the wafer and cover sealing interface.

Two basic manufacturing processes are available. One process dry presses the $Al_2O_3$ powder in a die. The other process, which is currently used extensively for dual in-line and flatpack I.C. packages, employs tapes, (see Figure 10) wherein the aluminum oxide is cast as a slurry in a continuous sheet. Butyrate binders render the tape flexible after drying, permitting it to be stamped, printed and handled on a spool similar to sheet metal. Several layers can be fired simultaneously to produce a multi-layer construction. Although the tape technique appears

to offer the potential advantage of high volume, low cost production, several inherent characteristics make it unacceptable for use at this time. The high content of volatile materials in tapes will create venting problems when firing the relatively large slabs containing screened line work. A shrinkage rate of 20 percent during firing will create registration problems and make it virtually impossible to retain the desired flatness of 0.0015/inch. In addition, a homogeneous high density cannot be guaranteed.

The use of a dry pressed ceramic slab in the order of 0.080-inch thick appeared to be the best choice. Flatness would be ensured by grinding prior to screening and firing the line work. Considerable know how in ceramic process techniques still had to be applied to retaining flatness during successive firing processes. Initial ceramic firing is performed at 1500°C. MoMn metalization is fired in at approximately 1450°C, which is within the softening range of the base ceramic.

## FINAL CONFIGURATION

Figure 11 illustrates the modules that have been fabricated using an integral $Al_2O_3$ base slab with a BeO heat exchanger. The left hand unit represents an all-ceramic construction. The other employs a Kovar cover. Cross-sections of the two configurations appear in Figure 12.

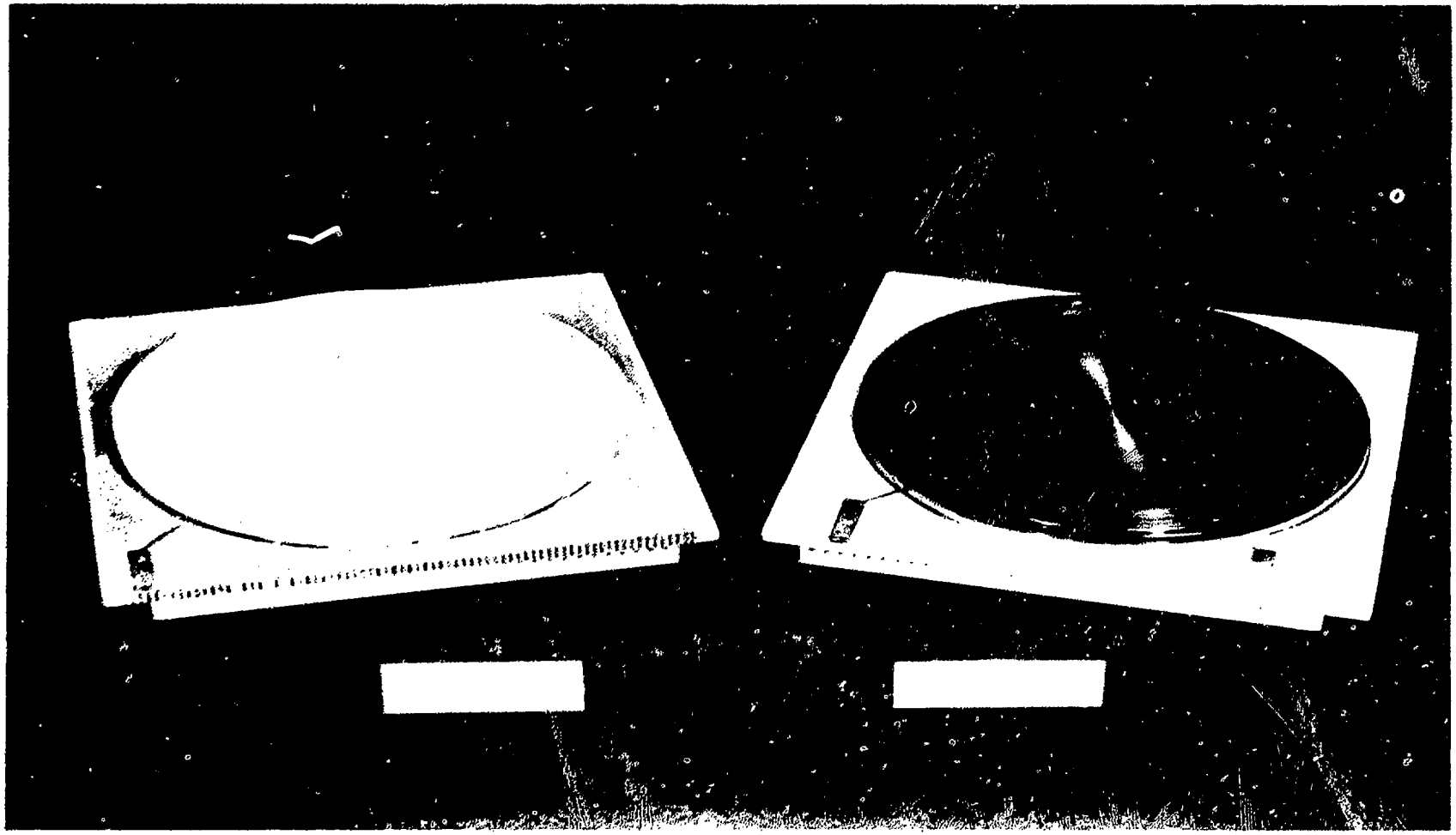
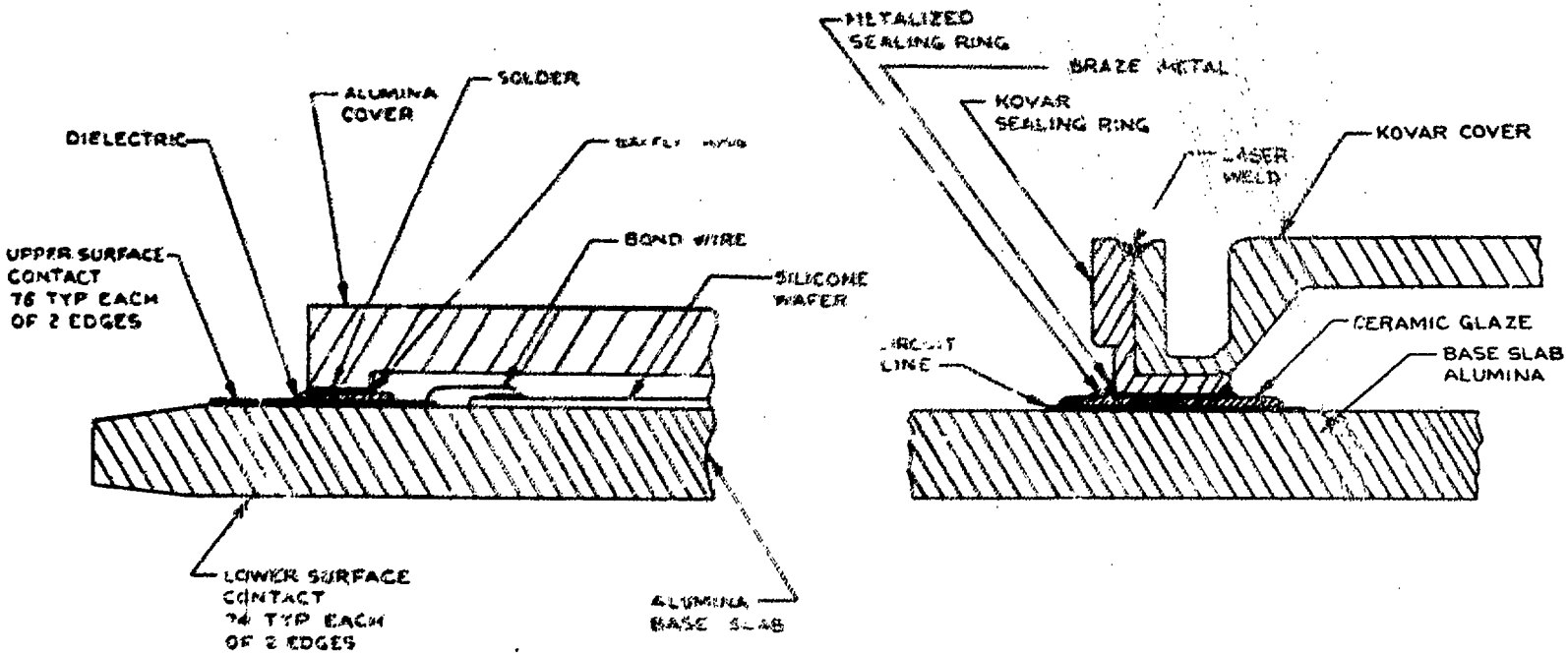


FIGURE NO. 11-ALL CERAMIC -
CERAMIC KOVAR MODULES




CERAMIC COVER

KOVAR COVER

FIGURE 12

The sealing ring interface is similar to that previously discussed in Figure 9. For the all-ceramic unit, a splash guard is included in the seal ring design to preclude injection of solder into the cavity during the sealing operation. The MoMn interconnecting line work is plated with copper, nickel and gold to reduce the line resistance below 0.25 ohms. Both configurations illustrate the aluminum wire bond interconnect system. Several techniques using spider arrangements for batch soldering have been designed. However, it should be pointed out that the 300 interconnections were made in less than 1 hour on the Kulika and Soffa 484 ultrasonic bonder. An automatic looping feature insures that all connections have a uniform loop and a consistent appearance. Bond strengths on test samples were greater than 6 grams. To minimize the area required for the line work, a wrap-around configuration is used. Figure 13 illustrates how the line work is distributed. Each quadrant has 75 leads radiating from the hermetic enclosure. Thirty-eight leads terminate on pads located on the front of the base slab. Thirty-seven are wrapped around the upper edges and terminate on the back.

A somewhat unique approach has been taken in configuring the wafer or substrate metalization area on the base slab. It was recognized that gas entrapment during the wafer bonding process may create some difficulty. A line pattern, which would guarantee gas escape paths, was used (Figure 13). Detailed thermal analysis indicates that a broken pattern in constrast to a continuous disc pattern would have an insignificant effect on the temperature gradient from the wafer to the heat exchanger. The external line pattern is protected by a high temperature conformal

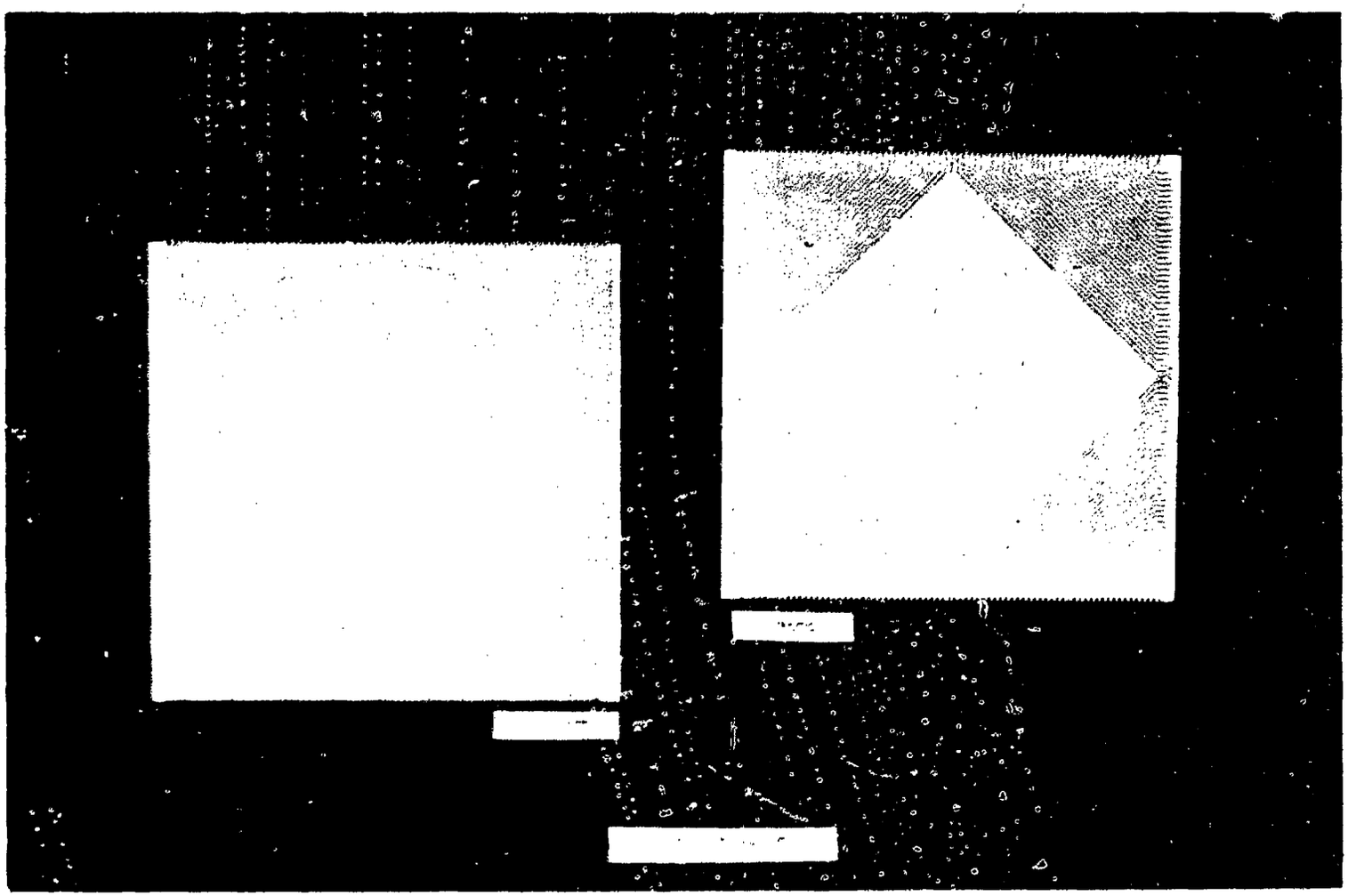


FIGURE NO. 13
BASE LINE SLAB PATTERN

coating.

As previously mentioned, the initial set of units includes a BeO heat exchanger since it will yield somewhat better thermal characteristics than an $Al_2O_3$ heat exchanger. BeO used in this manner will not have a significant cost impact since the heat exchanger will be produced as a dry pressed part, having no critical dimensions and requiring no machining.

SEALING

The all-ceramic unit (Figure 11) contains a ceramic cup shaped cover. The major advantage being that an all ceramic design has optimum radiation and thermal shock resistance. A potential disadvantage is that the cover to base seal is most readily performed in an oven wherein the wafer circuits are subject to the elevated sealing temperatures. Gold Tin eutectic solder was used for the sealing operation.

The Kovar cover design, as illustrated in Figures 11 and 12, can be sealed using localized heating techniques. The unit illustrated was laser welded. Component temperature rise was limited to 40°F. The operation was performed at Holobeam with their series 2500-4, 400 watt continuous beam YAG type laser operating at 300 watts. A rotary fixture moving at 2 rpm holds the module during the welding operation (Figure 14).

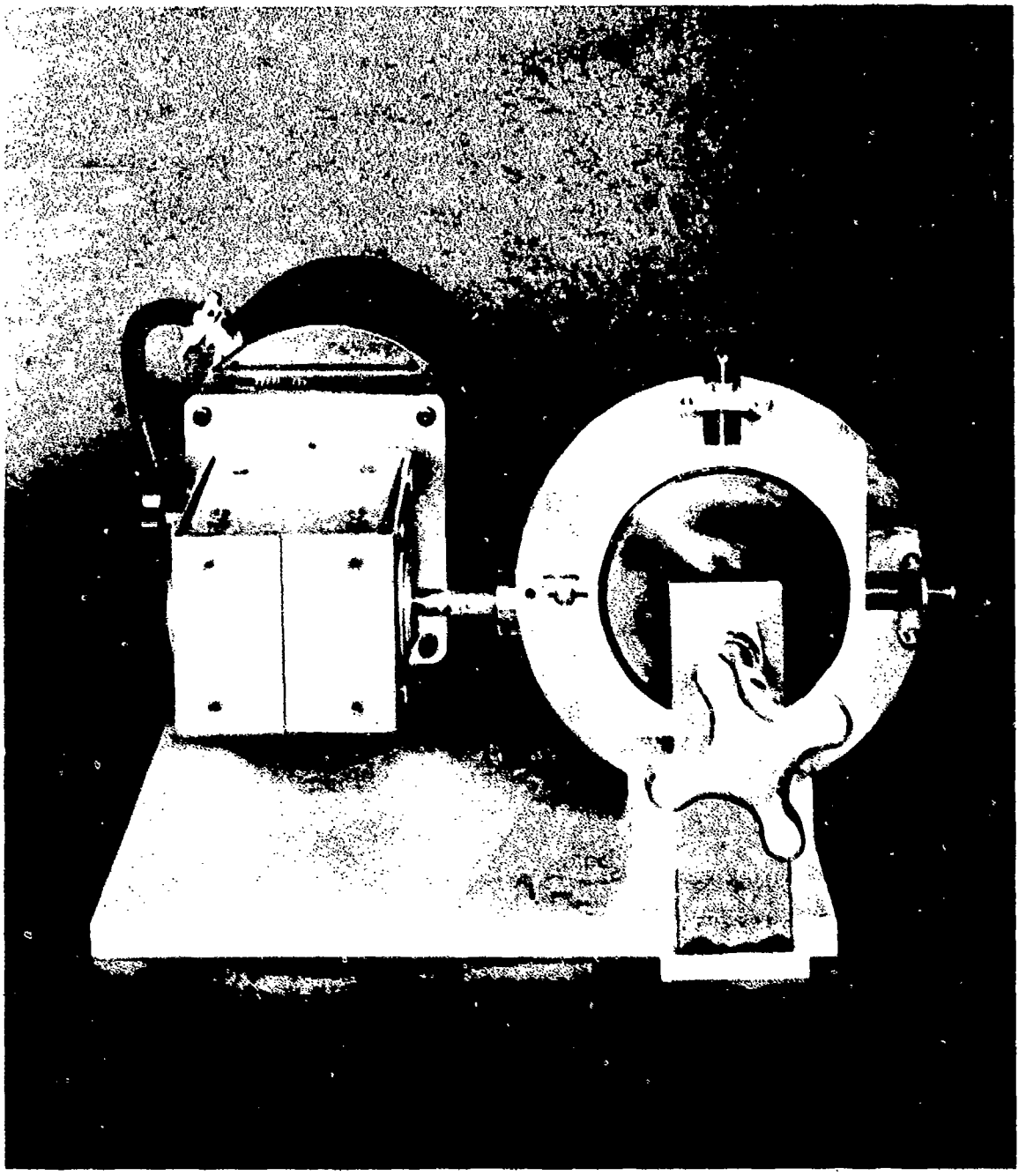


FIGURE NO. 14
LASER WELDING FIXTURE

A significant advantage of the Kovar design is that the unit can be reworked. The weld penetrates approximately 0.020 of an inch, thus, permitting it to be cut away. Three welds can be expected. Resistance welding equipment can be used with minor modifications. Thermal stress relief and resistance to high pressures during leak testing are inherent characteristics of the seal ring and cover design.

Measured leak rates of $2 \cdot 10^{-7}$ have been obtained with the Kovar and ceramic cover designs. This compares quite favorably to the MIL-STD-883 leak rate of $7 \cdot 10^{-7}$ for I.C. packages of 0.1cc to 10cc especially in light of the fact that the cavity volume is 6.8 $cm^3$.

Graphite fixturing, illustrated in Figure 15, was used to align and retain the substrate on the base slab. Similar fixtures were used to seal the cover and braze the keying pins.

## SUMMARY

An effort has been made to describe the general philosophy that was applied in arriving at a particular configuration for the AADC module. Design procedures and prototype manufacturing techniques have been developed which form a sound basis for further refinements that can be incorporated in high volume production units. The design configuration is compatible with the next higher level package and meets all the stipulated performance criteria.

Test procedures have been formulated by NAFI which will evaluate the

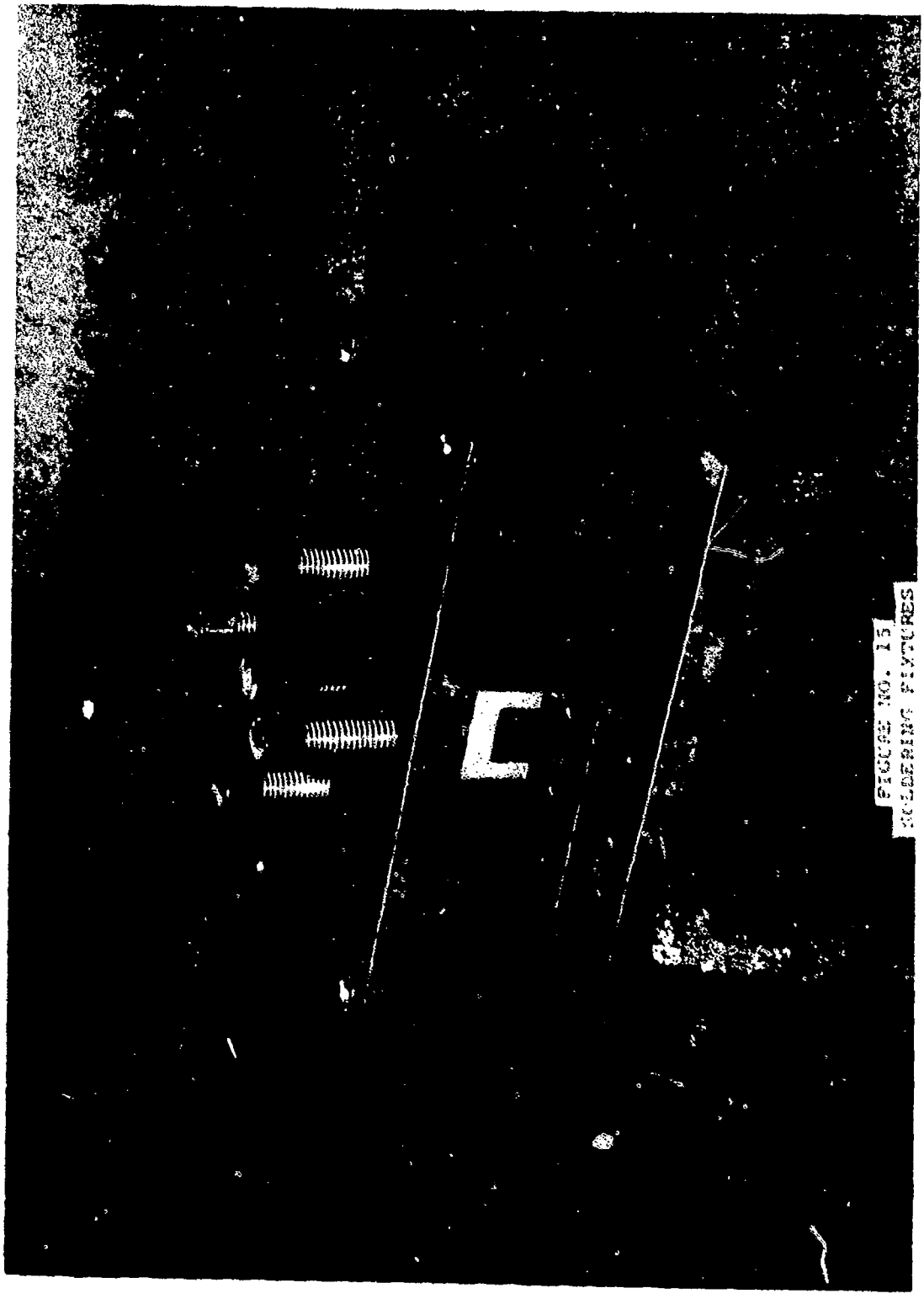


FIGURE NO. 15
WELDING FIXTURES

six units during the following months. Test substrates supplied by NAFI containing screened resistors to simulate heat loads have been mounted in all the units. Thermocouples, distributed across the substrate, establish temperature rises and gradients for various air cooling conditions.

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# LSI PACKAGING FOR ADVANCED AVIONICS DIGITAL COMPUTERS

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## Introduction

The use of microelectronic techniques in electronic systems places many sophisticated packaging requirements on equipment design. The small size capability has resulted in building more functions into a system rather than building smaller less capable systems. This philosophy has led to the concept of hybrid circuits, medium scale integration and large scale integration. Recently, the need for large monolithic LSI wafers up to 3" in diameter has been foreseen for use as building blocks in the construction of Advanced Avionics Digital Computers. To package such large devices requires a highly versatile modular concept which must be capable of meeting many electrical and mechanical requirements reflecting both low cost and high reliability.

In anticipation of meeting the needs of the AADC requirements the Naval Air Systems Command has numerous design and development programs under contract. This paper covers the work of one of these study programs concerning the development of a modular building block packaging concept. The work was performed by the Systems Development Division of the Westinghouse Electric Corp. for the Naval Air Systems Command under contract number N00019-70-C-0505.

## Design Requirements

Electrical requirements include various types and complexity of

circuitry to be packaged such as monolithic LSI wafers, whole LSI substrates, and individual integrated circuit chips, discrete components, and combinations thereof. Also included is the need of providing electrical connections from electronics packaged within to other modules or a higher level of packaging. Requirements may be as high as 300 electrical connections. The electrical interface must be compatible with high speed circuitry (10 nanosecond logic).

Mechanical requirements are extremely broad. The size of the module must be capable of housing whole monolithic LSI wafer(s) up to 3 inches in diameter as well as provide for 300 electrical terminations. It must be capable of overcoming the problems associated with the insertion and removal of 300 connections. Power dissipation can vary between 1 and 20 watts with a maximum thermal density of 3 watts/$in^2$. The module housing must be capable of shielding electrical and magnetic fields associated with the EMI environment specified in MIL-STD-461. Special attention must be given to the hermetic sealing process to avoid environments that might degrade or adversely affect chip/wafer attachment, substrate metallization, etc.

Design Evaluation

Evaluation of the module is to be based on results of environmental and mechanical testing as specified in MIL-STD-883 series 1000 and 2000 respectively. Electrical testing will be performed as specified in MIL-STD-202C, Class 300. Testing is to be performed by the Naval Avionics Facility, Indianapolis on 6 deliverable models. The test circuitry packaged within the modules is government furnished.

Additional evaluation of the program includes consideration for the higher levels of packaging associated with the module in the following areas.

1. Interconnection between modules
2. Mechanical support for modules and interconnection
3. Configuration of modules and interconnection into a final assembly
4. Provisions for assembly cooling (MIL-E-5400, Class 4X, forced air)
5. Electrical connection to final assembly
6. The ease of maintenance of the proposed design down to the module level

Design Approach

The work effort on this program was conducted in 2 phases. Phase I covered the design and development of the module. Areas of study include:

1. Basic Module Configuration
2. Vendor Selection
3. Stress Analysis
4. Thermal Management
5. Materials Compatibility
6. Electrical Interfaces
7. Electromagnetic Radiation - Radiation Hardness
8. Module Terminations

A final module configuration has been designed and prototype models have been fabricated for evaluation testing.

Phase II of the program covered the next higher levels of packaging. This effort includes:

1. Interconnections between Modules
2. Structures and Module Mounting

3. Thermal Control

4. Electrical Connection to Assembly

5. Maintainability

6. Reliability

Phase I

Basic Module Configuration

A complete review of all requirements was made as the initial step in the program. These requirements were related to past Westinghouse experience with similar microelectronic packaging designs and a basic module configuration was defined. A major objective in the basic configuration was to allow maximum flexibility in the design for instituting design changes as the program progressed and as further information was developed.

Initial efforts included a review of the published literature to determine any previous available useful data.

In general, the ideal substrate or packaging material should have the following characteristics:

1. High dielectric constant
2. Low dissipation or loss tangent
3. Dielectric constant should remain constant over the frequency and temperature ranges of interest
4. High purity and constant thickness
5. High surface smoothness
6. High resistivity and dielectric strength
7. High thermal conductivity

Both alumina and beryllia have been considered for this package. Alumina has been selected for its higher strength, higher surface smoothness,

non-toxicity, and ease of fabrication. Although beryllia has better heat transfer characteristics than alumina the actual difference in this design would only be about one degree centigrade. This small difference is felt to be negligible compared to the other benefits of using alumina.

Consideration was given to mechanical, electrical and environmental parameters in establishing the design. As a result the design concept selected was a ceramic substrate mounted in a ceramic package. Figure 1 shows details of the basic package construction.

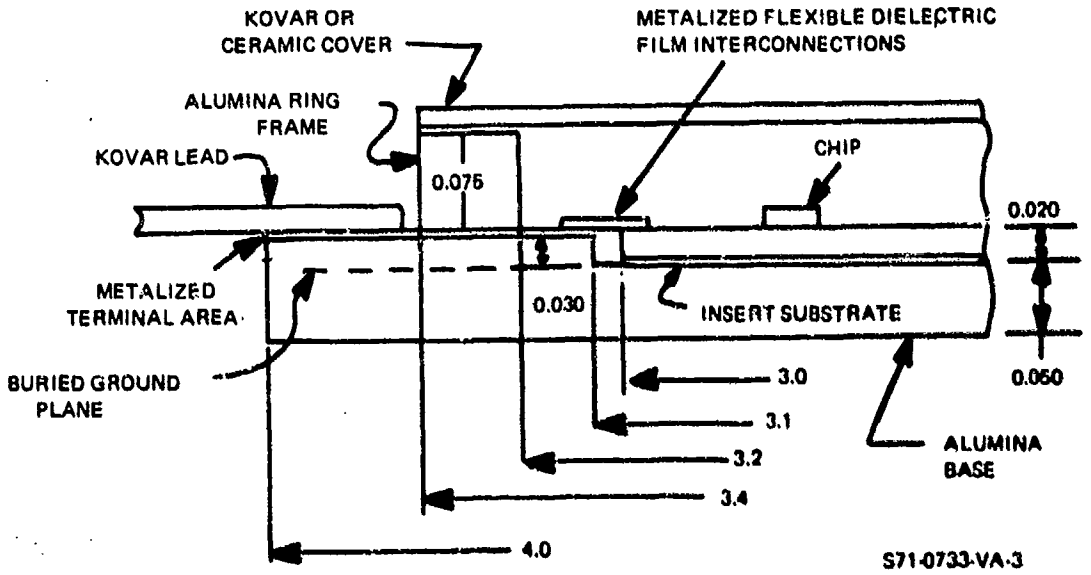



Figure 1 Basic Package Construction

Vendor Selection

A questionnaire of pertinent information on large ceramic packages was developed and used as a basis for a survey of ceramic manufacturers active in the electronic package field. Many manufacturers had previously expressed interest in this program. Twenty two companies were contacted of which 7 had a definite interest in the program. Three of these 7 companies appeared to have the capability to produce the design concept developed by Westinghouse. An engineering appraisal was made of the remaining three companies based on the following:

1. Experience
2. Facilities
3. Tooling and piece part costs
4. Willingness to work closely with Westinghouse and the Navy
5. Ability to meet the schedule
6. Confidence in the company

In establishing all of the design features of the package numerous studies were necessary. Included were the following:

1. Stress Analysis
2. Thermal Analysis
3. Materials Studies

Stress Analysis

A stress analysis was made on the lid and base of the package. The study showed that when the package was placed in the helium leak tester and subjected to 5 atmospheres of pressure the maximum stress in the lid and base is at the center. The yield strength of ceramic is about 20,000 psi. A lid and base thickness of .050" will result in a stress of about

10,800 psi or a safety factor of about 2.

Thermal Management

Thermal requirements for the package include a maximum thermal density of 3 watts/in$^2$ and a total density of 20 watts. The method of heat transfer for this package is primarily conduction with the ultimate removal by forced air as specified in MIL-E-5400, Class 4X.

A study of the thermal capability of the selected package construction was made for the worst case condition using a one dimensional analysis. Figure 2 shows the cross section of the various materials involved. The Dual JK Flip Flop 74H108 with a chip size of .110" x .070" and a power dissipation of .100 watts was used in the analysis. The basic formula used in the analysis was

$T = Q R$ where $T$ = Temperature Drop, $Q$ = Power Dissipated, $R$ = Thermal Resistance

$R = \frac{t}{KA}$ where $t$ = Thickness, $K$ = Thermal Conductivity, $A$ = Area

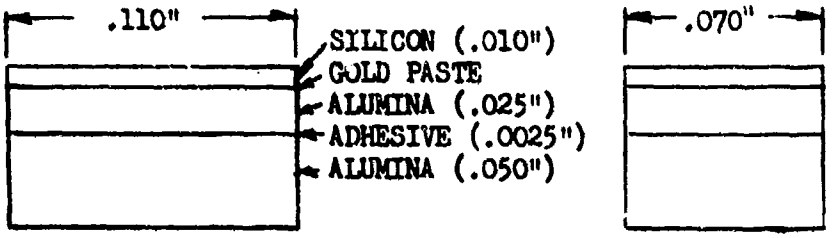



Figure 2 Cross-section of Thermal Path

In the analysis the thermal resistance for each material in the thermal interface was calculated and summed for a total thermal resistance. The temperature drop for the case studied was 6.75°C for alumina and about 1°C less for beryllia.

The major problem in the thermal management of this or any other similar type of microelectronic package is in the removal of the heat away from the package. In the requirements of MIL-E-5400, Class 4X the cooling air temperature could be as high as 125°C. First calculations of required air flow for maintaining a maximum device junction temperature of 135°C resulted in an impractical high air flow. Using the total package area instead of the one dimensional approach reduces the air flow requirements

but it would still be an order of magnitude too high. It was apparent that additional cooling area (in the form of fins) would be needed.

A study of fin requirements was conducted. From the standpoint of cost the best solution would be aluminum fins but the method of attachment is a problem since a material compatible to both alumina and aluminum is not available. In addition the large differences in thermal coefficients of expansion would result in large thermal stresses. The next suitable solution appeared to be alumina fins. Fourteen fins on a three inch square directly underneath the module does result in a reasonable air flow. The dimensions of the fin (alumina), to insure strength as well as high efficiency while reducing weight, is .250" high x .060" thick with .167" between fins. The efficiency might be improved by using beryllia, however, because of the lower strength of beryllia and its toxicity problem alumina is felt to be the better choice.

A differential analysis performed on the proposed fin design indicates that temperature at the end of the fin is 85 percent of the temperature at the base. Assuming the temperature is 25°C at the base, the temperature at the end of the fin is 21.3°C which is adequate for the design requirements.

Materials Compatibility

One of the more critical design parameters in a package of this size is materials compatibility. As previously discussed the use of the more efficient materials, such as beryllia or aluminum for the fins, is not always possible because of their incompatibility with other materials used in the design. Frequently, specified environmental requirements will also eliminate certain materials because of their limitations in these environments.

In the selection of the basic package material for this program both ceramics and metals were investigated. Ceramics were selected for their better overall compatibility with the components and substrates to be packaged. Both alumina and beryllia were considered as candidate materials. Although beryllia has the better thermal capability its toxicity and lower strength characteristics outweigh its advantages for our application and alumina was selected. Similarly aluminum would be a good choice for the required cooling fins both from its thermal capability and low cost but it was necessarily eliminated because of its incompatibility with alumina from the standpoint of improperly matched thermal coefficients in the required temperature environments.

Another critical material is the wafer or substrate attachment solder in the package. The requirement of surviving a 16 hour soak at 200°C (reduced from a previous requirement of 260°C) requires a solder alloy with higher temperature capability than the more familiar 60/40 tin lead eutectic alloy. A number of alloys with melting points in the 280°-370°C range are under study.

Electrical Interconnections

In the design of a multichip or large wafer package, the restrictions placed on the interconnection scheme by the integrated circuit properties must be recognized. Both circuit noise immunity and input voltage limitations must not be exceeded by spurious voltage waveforms resulting from electrical line reflections or coupled crosstalk.

Typical circuit properties are summarized below:

| Circuit Type | Rise Time | Noise Immunity | Limiting Vin |
|---|---|---|---|
| $T^2L$, gold doped | 5 ns | 450 mV | Vin - 2V |
| ECL, 2nd generation | 4 ns | 175 mV | Vin -0.5V |

Both of these causes, reflections and crosstalk, can be minimized by following a conservative rule that the electrical length of all interconnect paths is less than half the circuit rise time. This electrical length of a path is the geometrical length of the path multiplied by the speed of travel for an electrical waveform. This speed ranges from 0.1 to 0.2 nonoseconds per inch. Logic circuitry having signal delays of 10 nanoseconds has circuit rise times of about 5 nanoseconds. Thus the conservative rule is to keep signal path lengths between logic circuits shorter than 0.5 to 1.0 inch. This rule can be relaxed according to the circuit properties and other design parameters. Some of these other design parameters are the interconnect dimensions which determine the characteristic impedance, $Z_o$, of the signal paths, namely path width, thickness, and distance from a ground plane.

| | | Maximum Line Lengths | | Minimum Line Separations |
|---|---|---|---|---|
| | | Reflection Limit | Crosstalk Limit | |
| Circuit Type | | | | |
| $T^2L$: | 5 ns | 16 inches | any length<br>7 inches | 31 mils<br>10 mils |
| ECL: | 4 ns | 8 inches | any length<br>10 inches | 17 mils<br>10 mils |

The logic types considered above - $T^2L$ and second generation ECL - fit the 10 nanosecond signal propogation speed which was given as an early guide to this effort. The method of analysis referred to above and the results presented can be rephrased for faster logic with generally more restrictions on the length of signal paths.

Path length on the Building Block Module connecting the three-inch wafer or substrate to contact areas near two edges will be from 0.5 to 2.5 inches. These paths will lie on top of the alumina body of the module and

will be about 10 mils wide. Provision of a ground plane on the underside of the package will provide a uniform transmission line characteristic. With this ground plane about 80 mils below the interconnect path on top of the ceramic the characteristic impedance, $Z_o$, will be about 106 ohms. This is a very desirable and commonly used value since twisted pair wiring has a $Z_o$ of about 110 ohms and such should be used between module contacts carrying signal and complement or signal and ground, for the highest speed logic.

The equation used to calculate $Z_o$ is as follows:

$$Z_o = \frac{60}{\sqrt{e_r'}} \ln \frac{4H}{D_o} \text{ ohms}$$

where: H is the thickness of the dielectric between the conductor path and the ground plane,

$e_r'$ is the dielectric constant of the path, being half air and half dielectric of dielectric constant value $e_r = 9$ for alumina, and $e_r' = 0.48\, e_r + 0.67 = 4.94$.

$D_o$ is the effective conductor diameter, found for a rectangular bar to be $0.567W + 0.67T$ with the width of the path (10 mils) and T the thickness of the path (about 1 mil).

Inclusion of this ground plane will permit the ceramic module to utilize even the very fast, 2 to 1 nanosecond Emitter-Coupled-Logic integrated circuitry without harmful reflections and similar disturbances. Also required is a ground plane on the printed circuit board which receives the module and careful wiring between connectors in higher-level assemblies. Without the ground plane on the ceramic module, the packaging system should

be restricted to slower ECL circuitry or 7 to 20 nanosecond TTL.

Electromagnetic Radiation - Radiation Hardness

Problem definition is the first step in radiation hardening. This requires establishment of three elements; the anticipated radiation environment, the effect of these various types of radiation on the circuit components to be used, and the functional requirements to be satisfied by the circuit. The amount of detail information required for description of the environment depends on the probable intensities of each type of radiation and the degree of perturbation that each is likely to cause within the circuit. For a radiation component which has a critical effect, it may be necessary to know such things as the energy spectrum, the number of pulses expected (including amplitudes, shapes, duration, and spacing), peak prompt-radiation rates, and total doses.

With the foregoing understood, it is possible to make some broad generalisations which, because of their nature, cannot be taken to apply without exception. There is little of significance one can do at the package level to alter a fast neutron spectrum. The threshold of vulnerability in conventional circuitry occurs at an integrated neutron flux level of approximately $10^{13}$ neutron/cm$^2$. If a conventional one megaton weapon is exploded in space, this flux density would exist at a distance of approximately 20 miles. If the same weapon were exploded at low altitude, it would exist at approximately 3000 ft. There is also little one can do to alter a hard gamma ray spectrum. Critical dose rate for conventional circuitry is approximately $10^7$ rad/sec. A one megaton weapon in space could produce this dose rate at distances of approximately 100 miles, while at low altitudes the threat distance would drop to a couple miles. At such close ranges,

blast and thermal radiation damage would probably have the dominant effect, anyway.

There are, however, two areas in which package design could affect hardness; EMP and thermal X-rays. Both areas are currently under study. The electro magnetic pulse has been characterized in the open literature as being simulated by magnetic and electric fields which peak at 0.2 ampere-turns/meter and several hundred volts/meter respectively with pulse widths of about 10 nanoseconds. The electric field part can be stopped by a good Faraday shield, and the magnetic part can be stopped by good use of ferromagnetic materials. Absorption cross-sections for X-rays above 100 kev are relatively independent of material choice, but in the 10-100 kev range, materials with high atomic number become much better absorbers, (scales as $Z^4$). This can lead to deposition of energy where it isn't wanted (thermo-mechanical shock) or it can be used to motivate choice of package materials. It should be noted, however, that thermal X-rays are heavily absorbed in the atmosphere. This means they exist as a primary weapon threat in space, not at low altitudes.

Most work reported on the effects of a high radiation environment on electronic components are based on the components being directly exposed to the radiation. This is normally not the situation in packaged electronic equipment, i.e., chassis, coatings, platings, etc. shield the components to some degree from the radiation environment. A general discussion of a typical installation using a gold plated chassis illustrates this situation.

Let us assume that an ad hoc X-ray spectrum deposits 800 cal/gm. Using a density of 3.00 gms/$cm^3$ for aluminum this is equivalent to 2400 cal/$cm^2$ per cm. For a typical chassis thickness of 0.050" or approximately 1/8 cm., this means that 2400 x 1/8 or 300 cal/$cm^2$ of incident hot X-rays are absorbed

by the chassis.

Assuming the X-ray spectrum lies in the 1-100 kev range, it is fair to assume the total absorption cross section is proportional to $Z^4$.

or $Z_{Al} = 13$

$Z_{Au} = 79$ $\qquad \frac{Z_{Al}}{Z_{Au}} = \frac{1}{6}$

$$\frac{Z_{Al}}{Z_{Au}}^4 \approx \frac{1}{(36)^2} \approx \frac{1}{1300}$$

So gold is 1300 times better absorber in this spectral range so the ad hoc X-ray spectrum deposits 800 (1300) cal/gm in Au or approximately $10^6$ cal per gm. Since Au is about 20 gms/$cm^3$ this is $2 \times 10^7$ cal/$cm^2$ per cm of Au for a chassis plated with 50 millionths of gold or ($5 \times 10^{-5}$ inches) (2.5 cm/in) = $1.25 \times 10^{-4}$ cm, the gold would soak up ($2 \times 10^7$) ($1.25 \times 10^{-4}$) = 2500 cal/$cm^2$, therefore, the actual radiation that penetrates the system enclosures becomes far less of a problem for components when the total cross section is taken into account.

Module Terminations

In considering terminal spacings for this package it is desirable to maintain wide separations for both electrical and mechanical reasons. This may be accomplished by utilizing all four edges of the package. This concept, unfortunately, is not compatible with the forced air cooling needed on this program. It is essential to have two opposite edges of the package free of obstructions for proper air flow. This requirement necessitates bringing the package leads out to the remaining two opposite edges. This may be accomplished in two ways. The termination leads may be brought out to two opposite edges on both sides using vias and buried conductor layers.

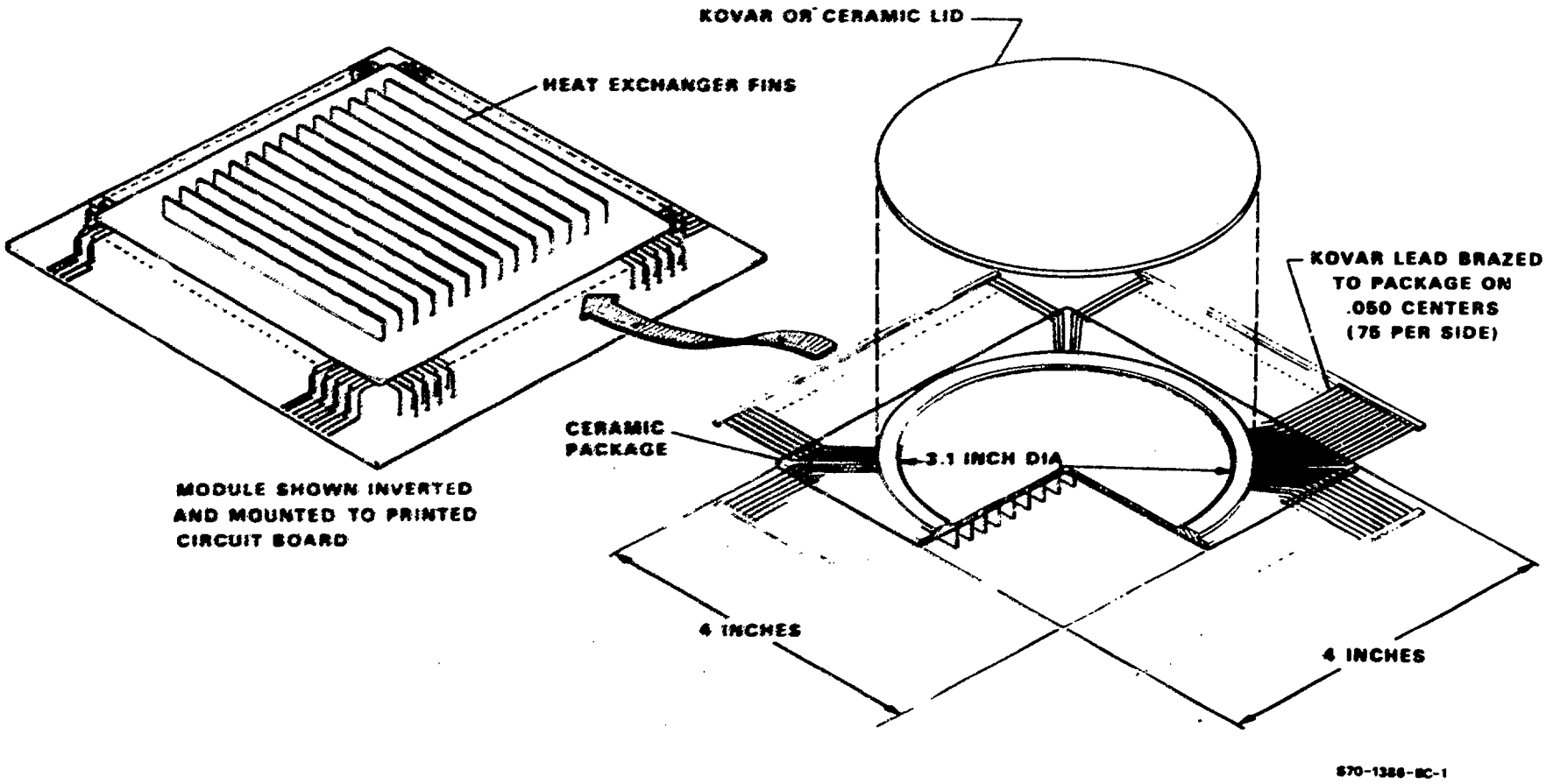
This will place conductors on .050" centers with 75 on each of the two sides or 150 to an edge for a total of 300 terminations for the two edges. A second method of achieving this arrangement is to use a printed wiring board for both mounting the ceramic package and for distributing the terminations to two edges. In this approach the terminations radiate to the four edges (one side only) on 0.050" centers. A lead frame is attached and preformed to meet the 0.100" hole pattern on a double sided printed wiring board which locates the terminations to the two opposite edges on both sides for a total of 300 terminations on 0.050" centers.

In evaluating these two approaches, the printed wiring board concept requires additional volume (about 30%) while the cost is less. Preliminary cost information indicates the cost differences of terminations on four edges to be as much as 50% less than terminations on two edges on both sides. The total cost difference would be closer to 30% when considering the cost of the printed wiring board fabrication and package to board assembly operation. Reliability of these two approaches must consider the reliability of additional interconnections (printed soldered joints) versus the reliability of vias and buried layers.

In light of the present level of the state-of-the-art of vias and buried layers, the concept selected by Westinghouse was a package with terminations on four edges on one side mounted to a printed wiring board as shown in Figure 3. As the state-of-the-art advances and reliability increases and cost decreases the design may be converted to the vias and buried layers concept.

The overall higher level of packaging developed for this program is compatible to both approaches.

# BUILDING BLOCK MODULE

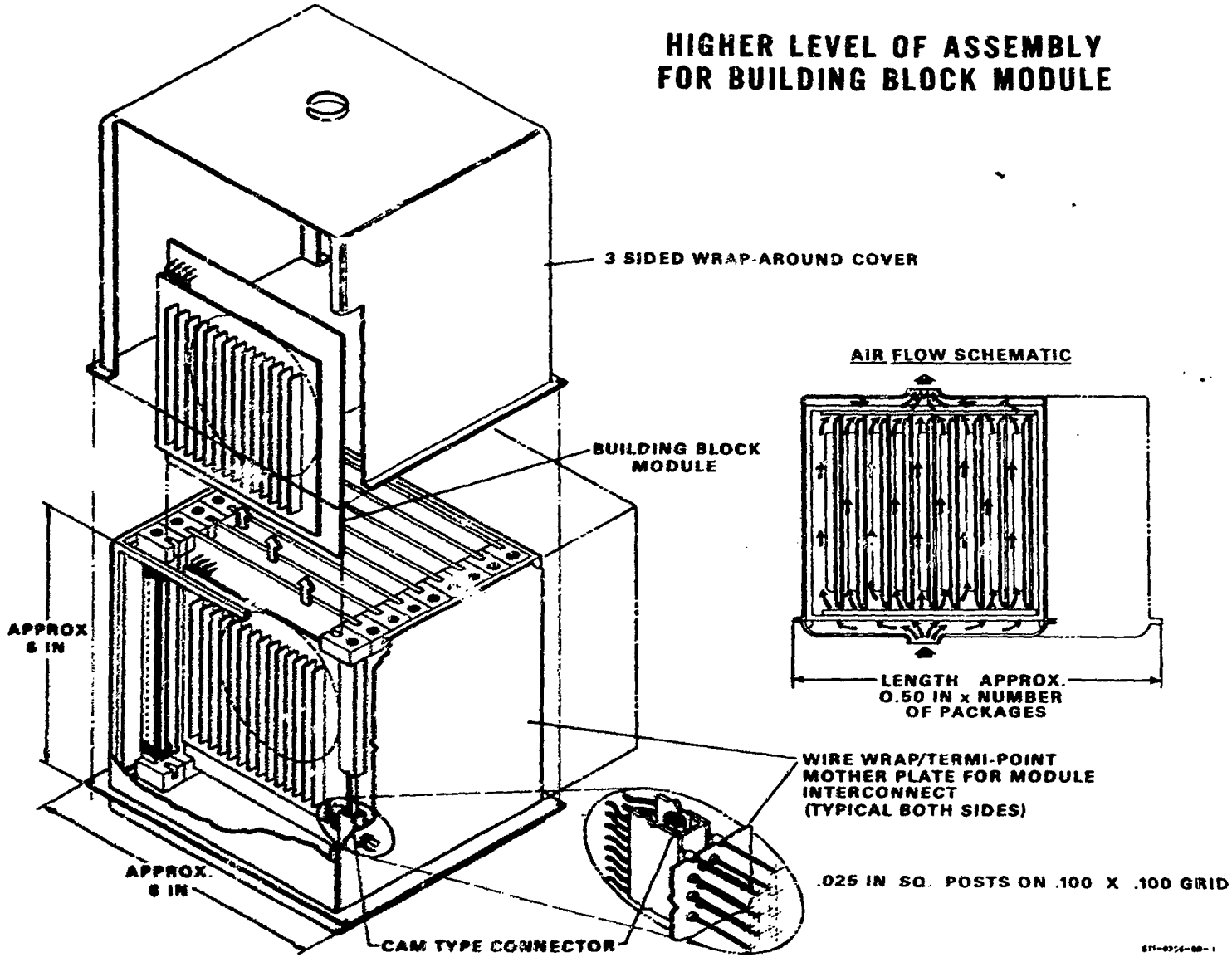


Phase II

The objective of Phase II of this program was to develop a concept for the next level of assembly for the Building Block Module. This requires a basic module design that is compatible with the next level of assembly, and lays the groundwork for the detailed design of the total assembly. The Phase II effort covered interconnections between modules, thermal control, other mechanical considerations, electrical considerations of interconnections, and maintainability and reliability.

The present design concept calls for the Westinghouse Building Block Module to be board mounted. The board essentially provides a method of getting all of the module I/O's to two edges, which is required to provide a clear path for the forced air cooling of the assembly. The board mounted module is placed in a stacked assembly and retained in position by two cam type connectors. (See Figure 4.) The cam type connectors have square post contact tails for wire wrap/termi-point interconnection capabilities. The assembly is forced air cooled to meet the conditions imposed by MIL-E-5400 for Class 4X equipment.

# HIGHER LEVEL OF ASSEMBLY FOR BUILDING BLOCK MODULE




AIR FLOW SCHEMATIC

Interconnections Between Modules

The development of the second level interconnection technique differed greatly from the module level. The situation presents larger sizes which result in electrical compatibility problems due to extended signal transmission lines. To achieve a successful integration for a total system an exploration study of state-of-the-art techniques was conducted.

The following areas were investigated:

1. Printed Circuit Boards
2. Wire Wrap, Welded Magnet Wire, and Termi-point
3. Flat Flexible Cabling

Determination of systems adaptability relies primarily on the circuit complexity, type of connectors, and system electrical requirements, as well as electrical, mechanical, and reliability considerations.

The mechanical connection techniques developed to interconnect modules permits automated design by computer aids to provide error free construction. The technique permits easy changes in the interconnections in the event of logic design change. Engineering logic changes generally persist well beyond the first model. Further, if only a limited number of a particular module assemblies are required, all models are best assembled the same way. A well known and commonly used technique that fits these two requirements - automated design and easy change - is wire wrap. A similar, but less widely used technique is termi-point.

Termi-point like wire wrap is a point to point wiring technique that can be handled on semi-automatic or fully automatic equipment. Either of these techniques may be used in the development stages of the AADC. Both can easily be replaced in high-quantity production with a multilayer printed circuit board for cost improvements.

Other Mechanical Considerations

A detailed investigation was made into the manner in which modules,

connectors, keying, and cooling hardware would be developed to yield a reliable, efficient system. As can be seen in Figure 4 approximately 8-9 module assemblies are combined in an assembly to form the basic computer.

The chassis used to house the modules is a welded and brazed, sheet metal assembly. There are two major parts to the chassis, a base and end walls subassembly and a three-sided wrap around cover. Both parts are necessary for structural reinforcement, cooling duct work, and retaining structures which are integral to their design. By removing the cover, modules are easily removed or installed in the assembly with interconnections readily accessible.

The module assembly, i.e, the board mounted module, is supported along all four edges when the module is in its normal operating position and the chassis cover is on. This is accomplished by the clamping action of the connectors on both side edges of the board, by a keyed-slot-arrangement on the bottom edge of the board, and by a resilient pad contained in the cover exerting pressure on the top edge of the board.

The keying is not shown in the figure, but it can be placed on each board assembly to eliminate insertion of incorrect modules. The method used to accomplish this keying would be an adaptation of the system developed by NAVWEPS in the Standard Hardware Program. Essentially, the male members, the pie-cut and the crescent shaped pins, can be permanently attached to the bottom edge of the board and the mating female members made part of the retaining slot in the bottom of the chassis.

The board edge connectors are the zero-insertion-force type, each connector containing 150 contacts with wire wrap tails. The proposed design allows the use of a standard screwdriver for actuating the connector. In its normal position the connector clamps the board exerting a force on each of the pads on the board. To remove or insert the board the cam is actuated, opening the connector. The contact tails are staggered on a

.100" x .100" grid to allow for automatic wire wrap capabilities. There have been several connector manufacturers working in the area of high density, zero-insert-force connectors of this type.

Thermal Control

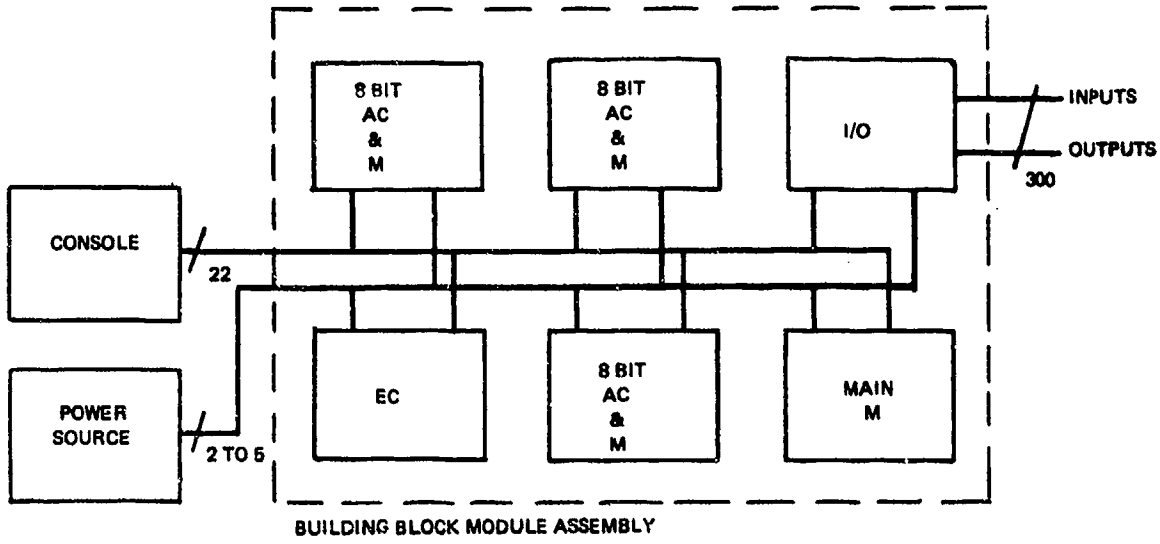
The main thermal consideration for cooling is to maintain the junction temperature at a value commensurate with high reliability. In the past the junction temperature of most solid state devices were designed to not exceed 135°C. This small temperature difference (135°C - 125°C) tends to establish a number of design restraints so that a satisfactory maximum temperature as well as temperature control can be attained. The methods of cooling considered in Phase II included: (1) direct air cooling, and (2) indirect air cooling using either liquid or a heat pipe for transport purposes.

Direct air is by far the simplest and has been used in the past with the least weight and volume penalties. Analysis has indicated that direct air will be sufficient for cooling purposes with the addition of alumina fins to the base of the package. The analysis was based on the 3 watts/sq. in. maximum density and total power output of 20 watts maximum. Other methods are currently being developed at Westinghouse for cooling high power microelectronic packages, such as heat pipes and a prefabricated, low cost heat sink material. Should the power requirements for the Building Block Module be increased above its present level, techniques will be available to handle these increases with a minimum of modifications to the existing design.

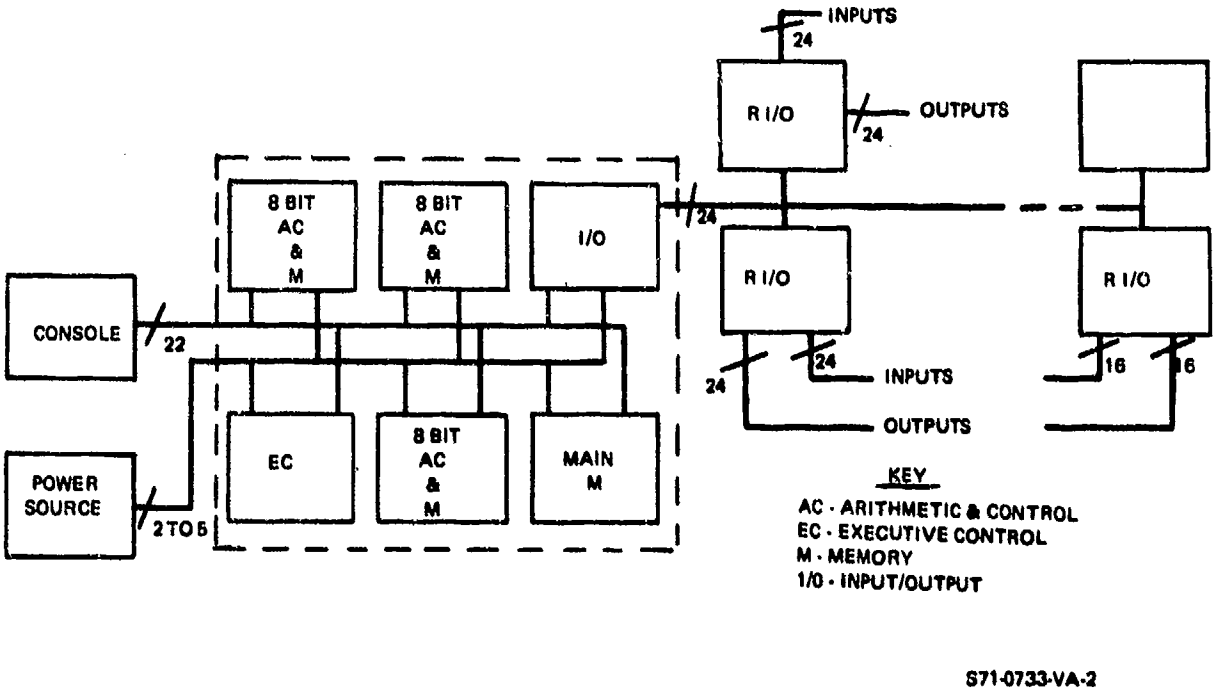
Electrical Connections to Assembly

The method used for electrical connection to the assembly of

Building Block Modules must recognize the function of these connections. Three functions must be considered: electrical power, signal connections with a console for control, loading program and indication, and signal connections with external signal sources and loads, i.e., input/output connections (I/O's). All of these can be handled with appropriate size cable connectors, with one possible exception, namely that the number of I/O signal sources and loads may be too great for reasonable size cables. Here is an opportunity for system design to ease a mechanical-electrical problem. An alternate system approach is to communicate with these I/O's by means of a multiplex data bus with remote I/O units which both collect remote signals, multiplex and send these to the central computer and also receive from the computer load commands, demultiplex, and distribute these to the loads. Figure 5 compares a direct wired I/O connection with a multiplexed I/O connection and shows the reduction in connections to the Building Block Module Assembly.




DIRECT WIRED I/O's




MULTIPLEXED I/O's

Figure 5 Direct Wired I/O's Versus Multiplexed I/O's

Such a multiplex scheme with remote I/O units has been proposed for distribution and management of electrical power in aircraft by the Naval Air Systems Command (especially by L. W. Wendling). This approach is variously known as Solid State Electrical Control (SOSTEL), Automatic Electrical Distribution System (AEDS), or Automatic Controlled Electrical System (ACES) and is currently being developed by Westinghouse and others.

Reliability and Maintainability

The complexity of the Advanced Avionics Digital Computer makes maintainability a mandatory requirement. The system concept has been significantly influenced by this factor with accessibility being the prime requirement. The use of cam type connectors will solve the major module removal problems associated with the required 300 interconnections.

The system concept has been developed to maintain effective thermal interfaces when the equipment is being serviced. The time for removal and replacement is minimal and no special tools are required. Interconnections are easily accessible for trouble shooting.

It is difficult to develop enough actual use of life testing data to determine the reliability of the Building Block Module in the span of this study. However, a high reliability design has been established by applying results of previous reliability studies to the development of the Building Block Module and its assembly.

A recent study on an airborne fire control system indicated that the reliability of hybrid microelectronic packages (a related, similar packaging concept) is primarily related to four major items.

1. Solder Joints
2. Printed Wiring Connector Interconnections

3. Ball Bonds

4. Integrated Circuit Chips

In addition to the various types and numbers of joints and interconnections a major consideration in reliability is the junction temperature of the integrated circuit chip. The partitioning and subsequent layout of the Building Block Module is critical to the cooling techniques available. The curve of failure rate as a function of temperature is shown in Figure 6. The slope of this curve was taken from the Van Hoorde report[1] (Generic Digital Failure Rate, pg. 23). The curve was drawn to give the same failure rate at 90°C as predicted by RADC Reliability Notebook, with appropriate modifiers.

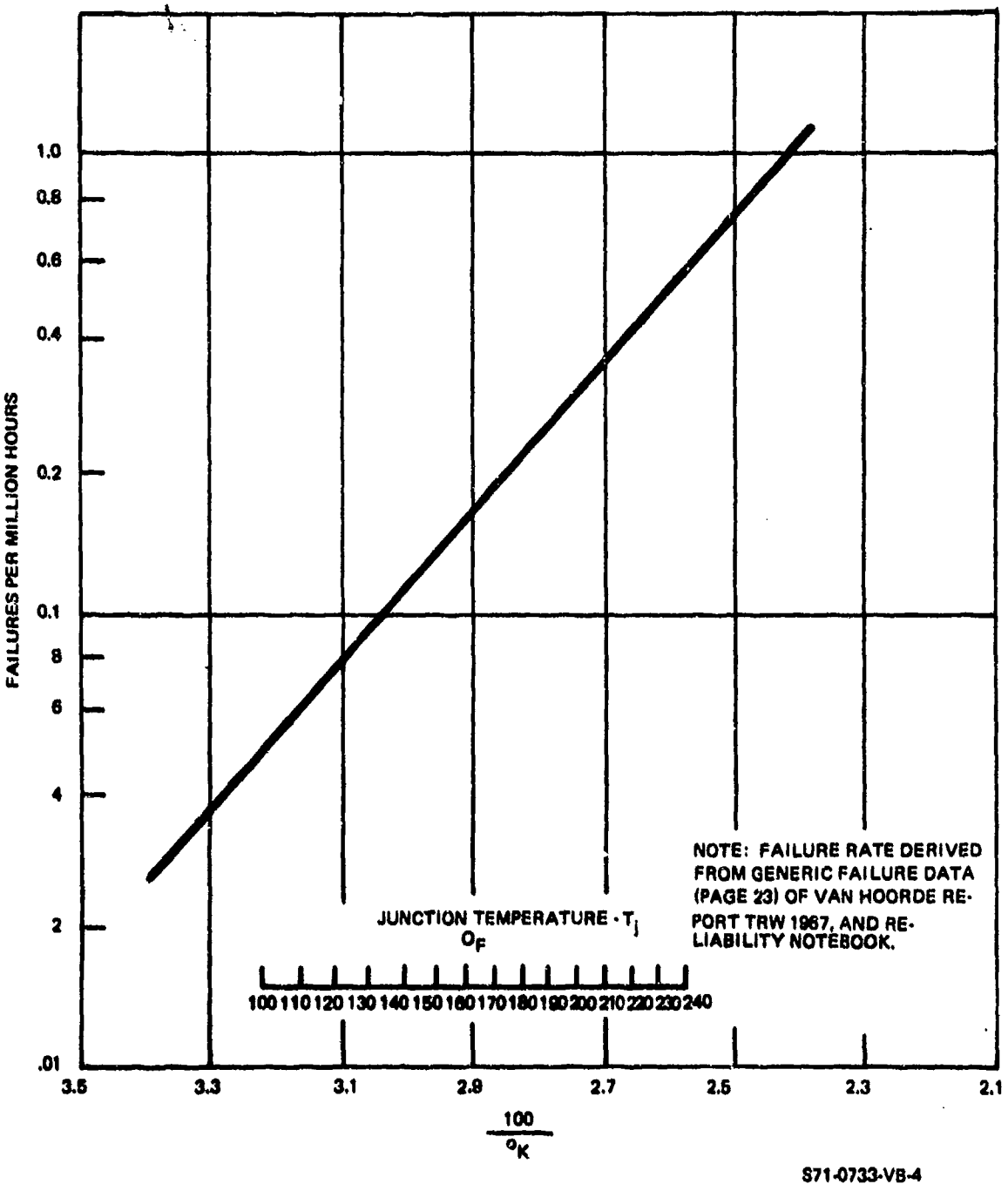



Figure 6 Failure Rate of IC's as a Function of Temperature

Some of the particular design recommendations from the above studies, included in the Building Block Module, for solder joints are proper lead size to hole diameter, observation of minimum annulus around the hole, and use of plated through holes. The design of the printed circuit connector will incorporate the features of adequate contact force and contact wiping action to assure reliable connections. Standards set for reliable ball bonds, including the length of the flying wire, will be observed in the assembly of the Building Block Module. In addition, the design for the Building Block Module permits 100% inspection of all bonds. The junction temperature will be controlled through the thermal design considerations of the Westinghouse design thereby increasing the reliability of active devices packaged in the Building Block Module. In summary, the Westinghouse Building Block Module will have every feasible reliability characteristic built into it, from module to system design, to yield reliability levels needed for successful airborne electronic equipment.

Areas of Future Growth

The development of a packaging concept for use in future systems frequently must use less than the optimum techniques when hardware must be delivered. This has been true on this program. It is therefore essential that the selected design reflect flexibility for ease of instituting changes as growth progresses. This has been a prime consideration in the Westinghouse concept for the Building Block Module.

Major areas of growth as seen at this time include:

1. Improved module construction through development of the green tape ceramic techniques resulting in a monolithic structure.

2. Improved module construction through development of more reliable buried layers and vias allowing the elimination of the present interconnecting printed wiring board.
3. Further investigation of an all aluminum metallization interconnect system for higher reliability and greater radiation resistance.
4. Improved internal interconnections through the use of metallized flexible dielectric films - this area is already under further study.
5. Expand the thermal capabilities of package through the investigation of more sophisticated cooling techniques.
6. Detail the design of the next level of assembly, including a zero-insertion-force connector, based on the concept developed in current program.
7. Conduct further studies in the area of radiation hardness. Determine effects of radiation on system parameters as opposed to analyzing the effects on a particular component.

Please note the following corrections to the paper

"LSI Packaging and Advanced Avionics Digital Computers"
by W. W. Staley, C. L. Marriott, R. C. Lyman

Page 11 - Line 5 nanoseconds (not nenoseconds)

Line 8 12 to 24 inches (not 0.5 to 1.0 inch)

Line 19 are faster than the 10 (not fit the 10)

Page 24 - Line 5 Automatically (not Automatic)

# DISCRETIONARY-WIRED LARGE SCALE INTEGRATION

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21 April 1971

## INTRODUCTION

The discretionary routing approach to large scale integration (LSI/DRA) conceived by TI in 1964 is based upon the following concepts:

- A large number of small area circuits can be processed on a slice of silicon.
- Circuits do not necessarily have to be of the same type; i.e., different circuit types can be fabricated on a slice of silicon at the same time by a common process.
- Circuits can be tested as part of the slice of silicon to a degree sufficient to identify the good circuits.
- A computer program can be developed which will generate automatically in inter-connection pattern of randomly located good circuits to form a large block of circuits.
- This computer program can accomplish the task in an economical and reliable fashion.
- Precision cathode ray tube photomask generation equipment can be invented which would make the required multilevel metallization and insulation masks at a low cost.
- A multilevel metallization and insulating system can be created to interconnect the known good circuits on the slice.
- A final test method can be devised to provide a high level of confidence that the completed logic array is a functional device.
- A package can be developed to provide a large number of input and output leads and be able to dissipate considerable power.

This monumental task of scientific achievements was accomplished successfully and demonstrated by the completion of an avionics computer in March 1969 for the Air Force under contract AF 33 (615) -3546. This computer (the original version of which contained 1735 logic flat packs) was completely re-implemented with only 34 LSI arrays. Since the fall of 1968, over 1700 LSI/DRA functional logic arrays have been built and delivered for use in experimental and operational equipment. These arrays have ranged in complexity from 150 to over 550 logic gates per wafer.

Shift registers of bipolar TTL (Transistor-Transistor Logic) circuits over 1000 bits in lengths have become routine products. These are capable of operating up to 10- MHz shift rate.

## WAFER TESTS QUALIFY CIRCUITS

Consider a 1-1/2-in. diameter slice of silicon containing five different TTL logic circuits as typical of an LSI wafer. This silicon slice can be batch processed to the same state that a normal integrated circuit slice is processed. That is, the complete diffusion cycles are carried out along with first-level metallization. At this point, the various transistors, diodes, resistors, and capacitors have been created and then interconnected with a metallization pattern to form complete circuits.

The normal IC wafer contains only one circuit type and is tested for basic standards. The bad circuits have an ink dot deposited on them; the slice is diced (broken into individual chips or bars); good chips are sorted from bad; and the good chips are packaged in a flat pack, ceramic, or plastic package for further testing and grading.

The different circuits on an LSI wafer must be tested while they are integral parts of the wafer to assure that the circuits which pass are good enough for interconnection into complete logic networks. In other words the circuits must be graded by a dc-probe test to certify them good enough for operation over the complete frequency and temperature range normally expected of a logic network.

Thus, the degree and quantity of tests performed on an LSI wafer at probe is much greater than that performed on normal ICs. The yield at probe of an LSI wafer is equivalent to the yield of ICs at final test after packaging. This yield, in a laboratory environment, has been maintained at well over 50%. This means, with 1000 gates designed on a wafer, over 500 would be suitable for interconnection into a logic array.

Techniques have been developed which allow an LSI wafer to be completely tested in minutes. Circuits on an LSI wafer are positioned with precise geometrical grids to allow the location of good circuits to be retained in the computer memory. The only print-out to the operator after probe test of a given wafer is the actual number of each circuit type which passed the tests. At this point, the wafer is placed in assignment inventory.

## MULTILEVEL PROCESSING VIA COMPUTER

The computer routing program for a multilevel process accepts as inputs the probe data (location of good circuits) from a given serialized LSI wafer being held in inventory and the circuit interconnection data for a given logic network. The computer generally uses (for random logic networks) two levels of interconnection, one vertically oriented and the other horizontally oriented.

A typical vertically oriented pattern (second-level metallization) contains heavy vertical bars spaced on the pattern for distribution of $V_{CC}$ to the circuits. Since $V_{CC}$ is distributed at second-level metal, it is separated from first-level metal by a layer of insulated material. Vias, or feed-throughs in first-to second-level insulation is provided only over those circuits which are to be interconnected or activated.

A typical horizontally oriented, third-level metal interconnect pattern contains bonding pads around the edge for wire bonding to the package lead frame. These provide connection to the external circuits. A composite of these two patterns illustrates the joining of second and third-level lines as well as the complexity of the interconnection. The computer routing program, in solving the interconnection of 500 equivalent gate complexity, is attacking a problem similar to that of interconnecting 100 14-pin IC flat packs on a two-sided printed circuit board.

The multilevel process requires that an insulation layer of silicon-dioxide be deposited over the wafer in order to separate first from second-level metal. Remember that first-level metal is used to interconnect the components within each cell area to form logic circuits as well as to provide a ground plane of metal around each major cell area. Then, the first discretionary mask is one of vias through this insulation to provide connections between first and second-level metal. Often many thousands of vias are required.

Both the first-and second-level metal interconnections are composed of a sandwich of molybdenum-gold-molybdenum about 17,000 ang thick and 2.5 mils wide. The mulybdenum separates the gold conductor from the

silicon insulation. This metallization was chosen, after much research, for its stability and current-carrying capacity. The third level discretionary interconnect, composed of molybdenum-gold, is also about 17,000 ang thick and 2.5 mils wide.

The output from the computer discretionary-routing program is a set of instructions which will cause a direct-view cathode ray tube with a 1-mil spot to be deflected in x-y coordinated movements. A 2:1 reducing lens focuses this spot onto a 70-mm film strip. The camera shutter is left open during a given sequence so that all movements of the cathode ray tube spot are traced on the film.

There are four basic sets of instructions from the computer program and subsequent film masks required for each wafer: a) set of vias in the insulation between first and second-level metal; b) second-level metal interconnections; c) set of vias in insulation between second-third-level metal; and d) third-level metal. Then, the film is processed, cut into appropriate sections, and used as direct-contact masks on the serialized wafer for the multilevel metallization process.

## ARRAY TESTING COMPLETES PHASE

The final phase of the process of creating an LSI array is the testing of the completed array to verify that the interconnections are valid and that the array will perform in accordance with the logic diagram. TI has developed a "single-fault modeling" approach, since testing an input logic array with all possible combinations of inputs that can occur is impractical. However, testing for a single type of fault at each node within the logic network is both practical and effective. This approach assumes that a set of inputs can be defined which not only will exercise each circuit output but also will test for the output being stuck-at-one or stuck-at-zero.

The number of tests required for a 200- to 400-gate array is in the thousands. But this is a reasonable number to generate and test through the use of computer programs and computer-controlled test equipment. The equipment at TI is capable of applying 5,000 tests per second to a 156 pin LSI.

This approach to tests does not require knowledge of the functional capability of a logic array. Therefore, a logic diagram can be provided, the multilevel interconnection accomplished, and the completed array tested without the operator knowing what the array does functionally. This gives the customer confidence that his circuit innovations are protected. In addition, he is guaranteed that his information is treated on a proprietary basis.

## PACKAGING THE LSI FOR INDUSTRY

A general-purpose package has been developed for containing whole wafers of monolithic semiconductor components. The package serves as a suitable container, protects the wafer from handling and environments, provides for adequate heat-transfer, and is capable of mounting and interconnection into customers' equipment. A 2-1/8 in. square, alumina-ceramic substrate with thick-film metallization leads is the package developed through extensive research. It provides 39 leads on 50-mil centers on all 4 sides of the package so that conventional solder or reflow solder techniques can be used.

The wafer is mourted with a special heigh-temperature epoxy adhesive providing a 3 C/W gradient between the silicon substrate and the ceramic header. The wafer is connected to the gold-plated lead frame with gold wires using conventional thermocompression techniques.

This results in an all-gold system with none of the "purple plague" characteristics of an aluminum-gold system. The standard package has an epoxy sealed ceramic lid, but a hermetically sealed package with a Kovar-type lid can be provided.

The standard logic wafer, referred to as the "L" slice, contains flip-flops and simple NAND gates. In addition, the "M", "N", and "P" slices are other standard wafers presently being produced. The "M" slice has been designed to create long shift register chains of high frequency bipolar logic. It contains input-output buffers, a patented 4-bit shift register cell, and clock drivers. It is completely TTL compatible, capable of over 10MHz shift rate and consumes an average of 1.5mW/bit. The clock drivers on the wafer, requiring an additional 3.5mW/bit, result in the highest frequency, lowest power, and longest shift register available.

The "N" slice standard LSI wafer contains more complex circuits in the form of AND-NOR-INVERT and EXCLUSIVE-ORs as well as standard NAND gates and the J-K flip-flop. Logic arrays of over 500 equivalent gate complexity can be implemented with this wafer.

The "P" slice is another complex-cell slice, that contains a large number of full-adders. This slice type is especially suitable for arithmetic functions for example, fast multiplier matrices of over 800 gate complexity are possible. This is approximately the limit of current 1.5 inch slices, although it might be said that, in the special case of the "M" shift register design, arrays having a complexity of thousands of gate equivalents have been built.

## INTERFACE METHODS NEEDED FOR LSIs

There are basically three interface methods that can be achieved with the technologies developed. The first is to implement a functional

bipolar logic requirement with the standard wafers currently in assignment inventory, i.e., the "L," "M," "N," or "P" slices. These types are currently in production and stacked waiting for assignment to a logic requirement. The addition of multilevel metallization converts these slices into functional arrays.

The circuits on the slices are standard series SN5400 TTL NAND gates whose design constraints have been well published. Partitioning the arrays to the number of circuits and types available on the wafer and limiting the number of input-outputs not to exceed 126 is all that is required. Presently, the time from logic diagram to completed array is in the range of 30 to 90 days.

The second interface method is provided by creating custom wafers using standard circuits which form a circuits library. The highest single cost in the design of ICs is the set of diffusion masks which are used to create the individual circuits. This high cost has already been expended in the design of standard circuits. Stepping and repeating these standard circuits around on a wafer to form a custom distribution or quantity of given circuit types is a relatively low-cost operation. Thus, a custom wafer containing a unique distribution of circuits for a specific application provides the interface.

TI is continuously expanding the present circuits library with new, more complex circuits. Most of these circuits will be similar, if not identical, to the circuits presently availableas standard Series 5400. Thus, implementing LSI arrays remains simple.

The third interface method with LSI is a full custom capability. A few thousand arrays of a single type may justify the expense of a custom

Circuit as well as a unique wafer. General-purpose logic arrays will provide 200- to 800-gate complexity while customized circuits and wafers can provide arrays of 500- to over 2000- gate complexity on a single monolithic substrate.

WHY USE LSI/DRA?

LSI/DRA offers advantage in size, weight, reliability, quick turnaround, and low-cost for custom design. For high volume applications, say 100,000 units per year, typical of large, complex systems, this high design cost and slow turnaround is not so easily tolerated, and computerized design with LSI/DRA is very much more attractive. For example, the total non-recurring design cost for a 500 gate LSI is about $6000, and total time from circuit diagram to delivered part is typically 30 to 90 days. The following comparisons might be made between LSI/DRA and MSI/SSI:

- Size is typically reduced as much as 10:1 at the component level and 2:1 at the equipment level. For example, the TI model 2502 computer was reduced from 0.75 cubic foot to 0.37 cubic foot when LSI replaced IC's.

- Weight may be reduced by 10:1 at the component level. A 500-gate LSI weighs 22 grams, or about 10,000 gates per pound. At the equipment level, improvement is typically 2:1. An airborne computer was reduced from 38 pounds to 35 pounds by substitution of LSI for IC's.

- Reliability is improved by reduction in number of packages, interconnections, solder joints, and connectors. Package count is reduced 40 to 200 times and interconnections by a factor of 5 to 10 times. For example, a 500-gate LSI using 100 signal pins has 0.2 pin/gate. A 14-pin, 5-gate SSI has 2.8 pins/gate, or an increase of 14:1 over LSI. A 20-gate, 16-pin MSI has 0.75 pin/gate, about 4:1. As another example, a 547-gate LSI was compared with a 43-package MSI implementation of the same function.

- Utilization of the LSI involved about 100 solder joints and gold wire bonds, compared to 688 for the MSI.

- Cost effectiveness is increased, by reduction in engineering time and testing. Input to the LSI System is a circuit diagram; output is a high-quality tested part at the sub-system level. Quick turnaround of logic change is possible, with new part in customer's hands in one to three weeks after change is requested.

## THE FUTURE: UNLIMITED POTENTIALS

Once the concept of discretionary-routed, multilevel interconnected logic arrays is accepted, the potentials for applying this technology seem unlimited. Large, complex arrays can be produced easily and economically. The complexity of the completed arrays is limited largely by the amount of customizing work in terms of partitioning and circuit design that is put into the array.

The more organized logic functions (such as memory structures) can be created easily with only one additional level of routed interconnections. More complex or general-purpose logic arrays require two additional levels of interconnection. Customizing circuit quantities and distribution on a wafer can provide very high complexity logic arrays with standard circuit designs.

Texas Instruments is actively pursuing a modified LSI structure, which makes possible the fabrication of generalized logic arrays with only one layer of metal interconnections in addition to the basic IC metal. The resulting simplified manufacturing process promises to add the advantage of a much lower per part cost to the already low design cost that was made possible by the highly computerized data-entry and test generation systems.

Other future improvements in LSI/DRA are foreseeable. For example, the complexity capabilities will increase because of a progression of slice sizes used. The 1.5 inch slices will give way to 2.0 inch slices; even larger slices will be used as the slices, packaging, and technology become available. Complexity capability will also be increased by the use of more powerful basic cells. Just as the "P" slice (which contains complex cells specialized for arithmetic functions) exceeds the capabilities of the general purpose "L" slice, then future specialized slices, containing "MSI" basic cells, will greatly increase the logical power of the single array. Another direction in which LSI/DRA could progress would involve the basic IC technology. For example, Schottky-clamped circuits might replace normal TTL circuits. Thus, the foreseeable future includes 1500-2000 gate arrays containing 3-ns gates.

## BIOGRAPHICAL INFORMATION

MERRYMAN, JERRY D.

Mr. Merryman joined Texas Instruments in 1963. He is presently responsible for design of Large Scale Integrated circuits, and for the development of computer-controlled cathode-ray-tube artwork generators used in LSI. In previous TI work, he designed a variety of integrated circuits, including many circuits involving optical and thermal effects. Prior to joining Texas Instruments. Mr. Merryman enjoyed a varied experience including the design of trasistor digital circuits, design of a special purpose computer used in problems of atmosphoric physics, theoretical investigation of the Solion Tetrode, and design of computer-controlled data collection systems. He has authored numerous articles that have been published in Proc. IRE, JOURNAL OF THE AMERICAL METEROLOGICAL SOCIETY, ELECTRONICS, etc.. He was a contributor to the McGraw-Hill AMPLIFIER HANDBOOK in (1966).

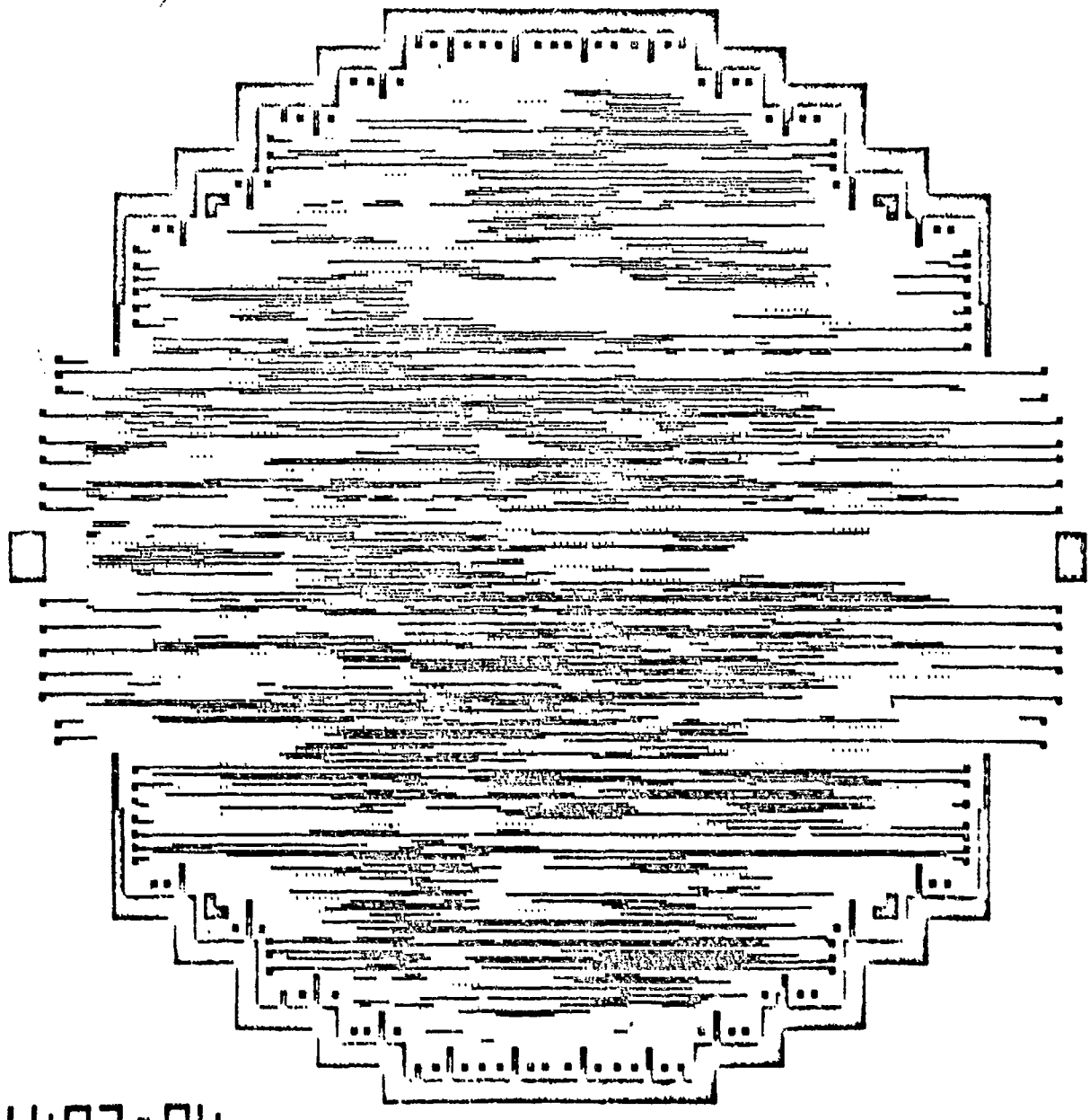


FIGURE 1: The final (third) layer of metal interconnect for a 4 1.5 inch diameter LSI slice.

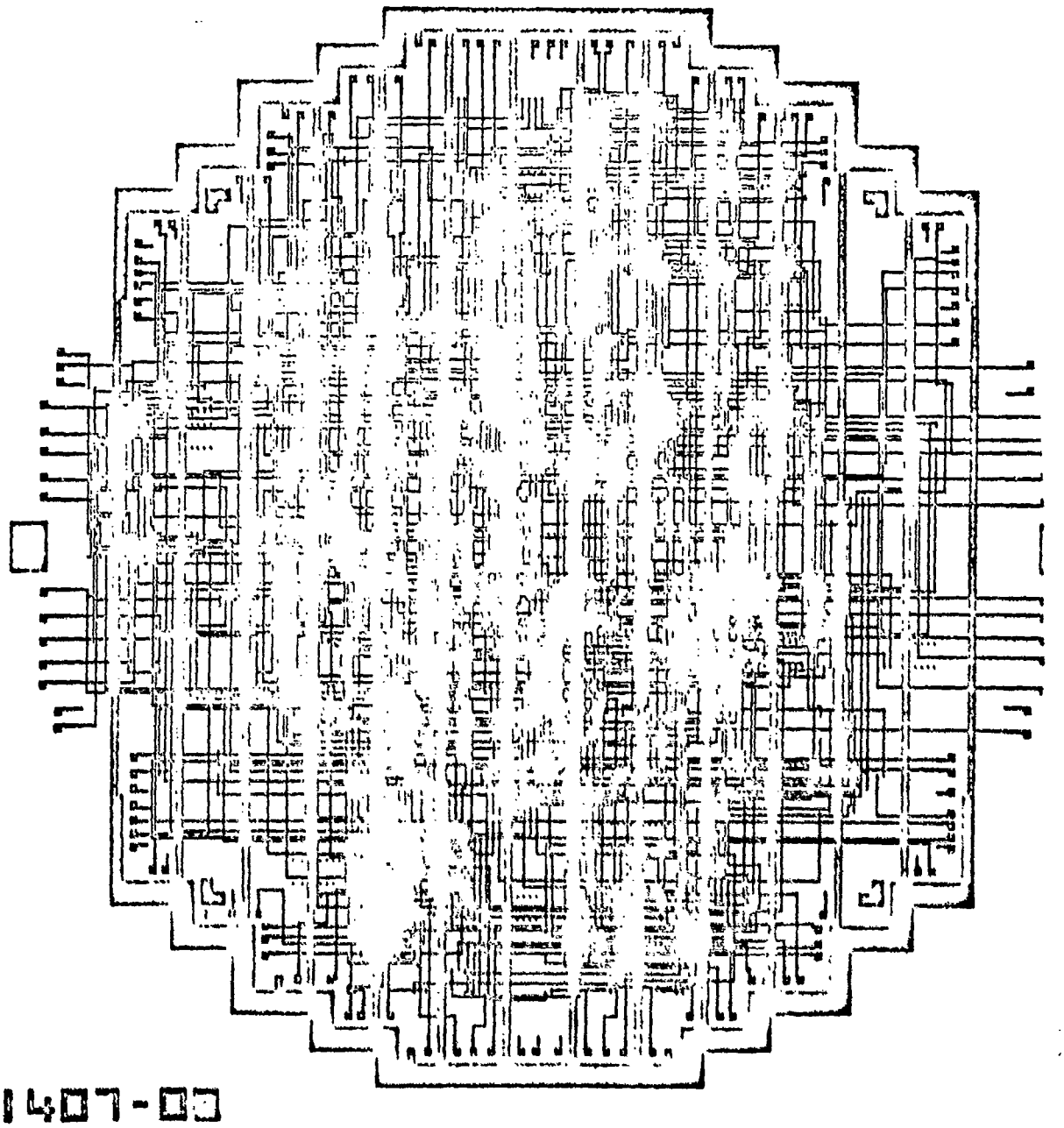

FIGURE 2: A composite of the second and third layers of metal interconnect.

# PAD RELOCATION LSI FOR ADVANCED FULL WAFER TECHNOLOGY

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Pad Relocation is an LSI interconnect design approach aimed at providing economy and flexibility for high complexity full wafer digital circuit arrays. The technique resulted from studies at Hughes Aircraft Data Systems Division to determine an optimal matching of digital military system requirements and advanced microelectronics capabilities. Military digital requirements are characterized, of course, by low cost, volume and weight, as well as various speed-power considerations. But also, there are important priorities on reliability, standardization, and multiple sources. These considerations and the fact that semiconductor military production quantities are typically quite small have greatly influenced the development of an LSI technology at Hughes.

The Pad Relocation technique was developed by Hughes in 1968-1969, and was first under government contract in December 1969 by Naval Air Systems Command for certain automation studies. During 1969-1970, nine related contracts have been granted, three requiring LSI hardware delivery and two LSI hardware designs. While refining and automating the Pad Relocation design during the last year, three sources of wafer fabrication and multi-level processing were developed. In addition, the approach has been applied successfully to seven different wafer types (six bipolar TTL and one P-MOS) with many working full wafer arrays (see Table 1) of typically

## Table 1. Status of Pad Relocation LSI Wafer Arrays

| Circuit Function | Wafer | Gate Equivalents | Application | Status |
|---|---|---|---|---|
| 5 Bit Sign Magnitude Multiplier | TI"K" | 207 | Radar Data Processor | Multiple working parts including extensive life tests |
| Pulsewidth Analyzer | Motorola 2" IC (3 Input NAND) | 288 | Threat Identification | In Final evaluation |
| Command Decoder | TI"K" | 326 | Missile Electronics | Multiple working parts |
| A and B Word Register | Hughes Adder Wafer | 160 (2 per wafer) | Tactical Information Display | Multiple working parts including extensive life tests |
| Digital Airborne Data System | TI"K" | 387 | Intra-Aircraft Data Transmission and Mux | In final test |
| SRD3-A | TI"K" | 286 | Communications System | Multiple working parts |
| SRD3-B | TI"K" | 274 | Communications System | Multiple working parts |
| 5 Mhz P-MOS Shift Register | Hughes P-Mos Wafer | 4000 bits | General Shift Register | Multiple working parts |
| CURRENT WORK INCLUDES | | | | |
| 9 Bit Sign Magnitude Multiplier | Hughes Adder Wafer | 616 | Radar Data Processor | Multiple working parts |
| 16 Bit Adder-Subtractor with input MPX | TI"P" | 462 | Radar Data Processor | Design Complete |
| Hughes Mini-Computer | | | | |
| Arithmetic | Hughes Adder | 500 | Missile Data Processor | Designs beginning |
| Control | Hughes And Nor | 300 | Missile Data Processor | Designs beginning |

300-600 logic gates already produced on four of the different wafer types. And the Naval Air Systems contract is now producing complete computer programs for the automation of the recurring Pad Relocation requirements from the wafer probe yield data to the final mask generation instructions as shown in Figure 1.

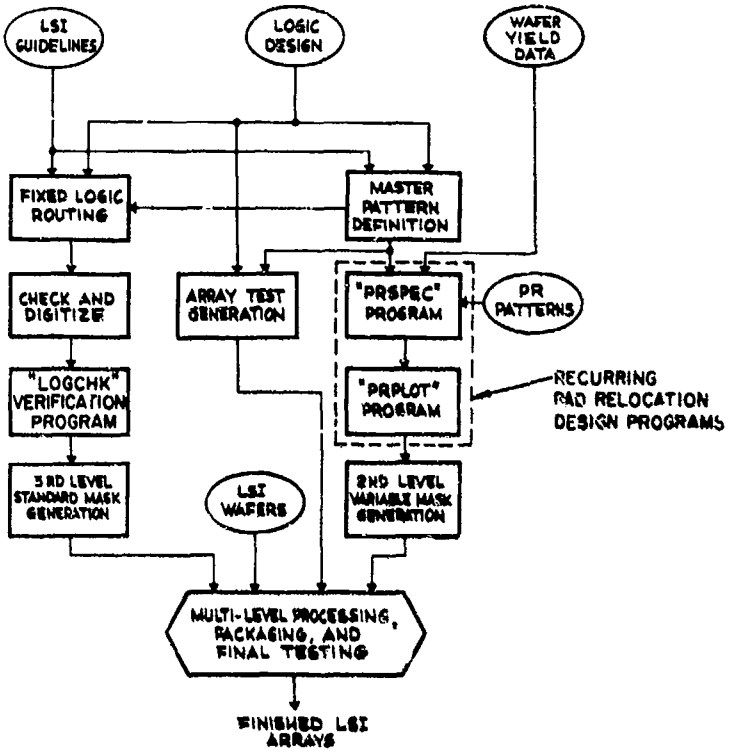


Figure 1. Hughes automated pad relocation LSI

High complexity standard digital circuit functions offer extreme advantages to military systems. This was proven in the transition from discrete components to integrated circuits and currently in the transition from simple IC's to higher complexity MSI chips such as for the standard functions of decoding, shifting, multiplexing, counting, adding, and certain memory requirements. Such common functions implemented with MSI chips obtain

a standardization, cost, reliability, and multiple source procurement not possible if a function is required for only one (or a few) particular military systems.

However, studies at Hughes have shown that commonly over half of a digital systems logic cannot, by current design approaches, be implemented with the standard higher level ("MSI") logic functions. For example, in a system using 500 IC packages, perhaps only 200 could have been replaced by say 15 standard MSI parts. Certainly, the reduction from 500 to the resulting 315 flatpacks is important to the system cost, reliability, volume, and standardization. But the effort at Hughes has been to also develop an LSI technology which is not limited in system applications to the lower complexity and repetitive functions which MSI circuits can meet. The results have been such as to allow the remaining IC packages to be replaced by 2-5 Pad Relocation LSI wafer arrays. The future potentials are much greater yet as the rapidly evolving technologies of new and higher density wafer circuits merge with wafer fabrication, multi-level processing, testing, and packaging.

Basically, the Pad Relocation technique* is an efficient and highly flexible means of standardizing the logic connections and mask generation for all LSI wafer parts of the same logic part type. This standardization is possible by using a prescribed portion of one of the typically three metalization levels (see Figure 2) to "relocate" the connection "pads" of operative circuits to master pattern circuit positions which are fixed for that part type.

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*For description of the technique see "The Pad Relocation Technique for Interconnecting LSI Arrays of Imperfect Yield," D. F. Calhoun, Proceedings, Fall Joint Computer Conference, vol. 35, 1969, pp. 99-109.

As a result, only the necessary and simple relocation patterns (which are now computer generated) change in accommodating any variations in the wafer yields, circuit designs, or even in the vendors processing or routing guidelines.

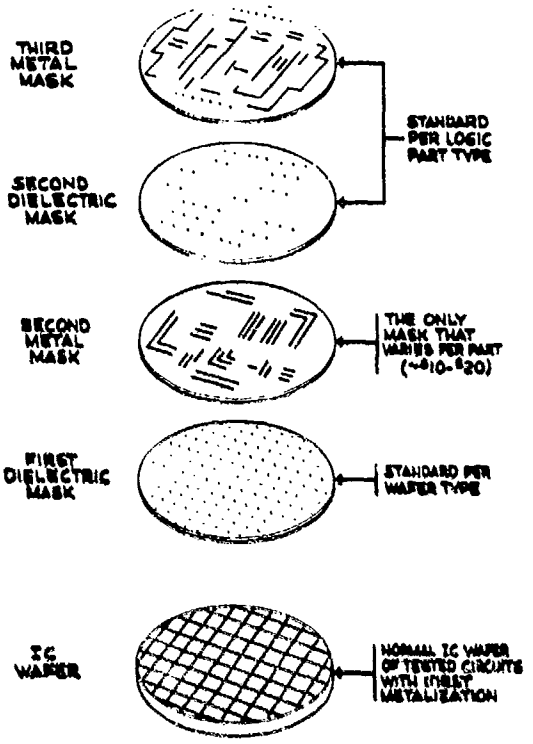



Figure 2. Low-cost high complexity LSI

The techniques simplicity thus provides such economical flexibility as will be required to optimally use the current and evolving wafer, circuit, and processing technologies. But it also provides the very low recurring design costs for military system quantities and the ease of developing and using multiple production sources. Since it addresses a high circuit complexity, monolithic, batch fabricated interconnect technology, the estimated

reliability is very high relative to IC's. And since it can make use of common IC wafers and the multi-level processing techniques being developed for high production MSI product lines, there is an optimal use of semiconductor and processing standardization.

LSI can be applied successfully to the broad range of digital systems whose circuit speed/power requirements can be met by LSI circuit types. Present TTL LSI can achieve speeds needed by the many systems of TTL logic of the medium speed (5400) class. Schottky TTL LSI will enable higher speed and lower power to be traded off. Full wafer MOS LSI will offer substantially greater complexity and density where lower speed is acceptable.

Logic circuits available in current bipolar LSI wafers are representative of medium speed, medium power TTL logic which might be used if systems were constructed of integrated circuits. Performance compatible with this circuit type is obtained. Circuits available include JK and D Flip Flops, And-Nor's (A/O/I's), Exclusive OR-NOR functions, Full Adders, as well as NAND gates. Thus, most elements used in IC logic design (though not most MSI parts) are available for LSI logic design. As a result, a logic function may be implemented efficiently with LSI as with integrated circuits. A great saving of volume, weight and signal pins (reliability), parts count, and cost is obtained through the placing of a complex function on a single wafer.

The range of LSI applications is greatly enhanced through the establishment of a flexible wafer library. The NAND IC wafer shown in Figure 3 contains only triple 3 input Nand gates, and although it can implement any logic function, it does so at some degree of logic inefficiency. The wafers designed

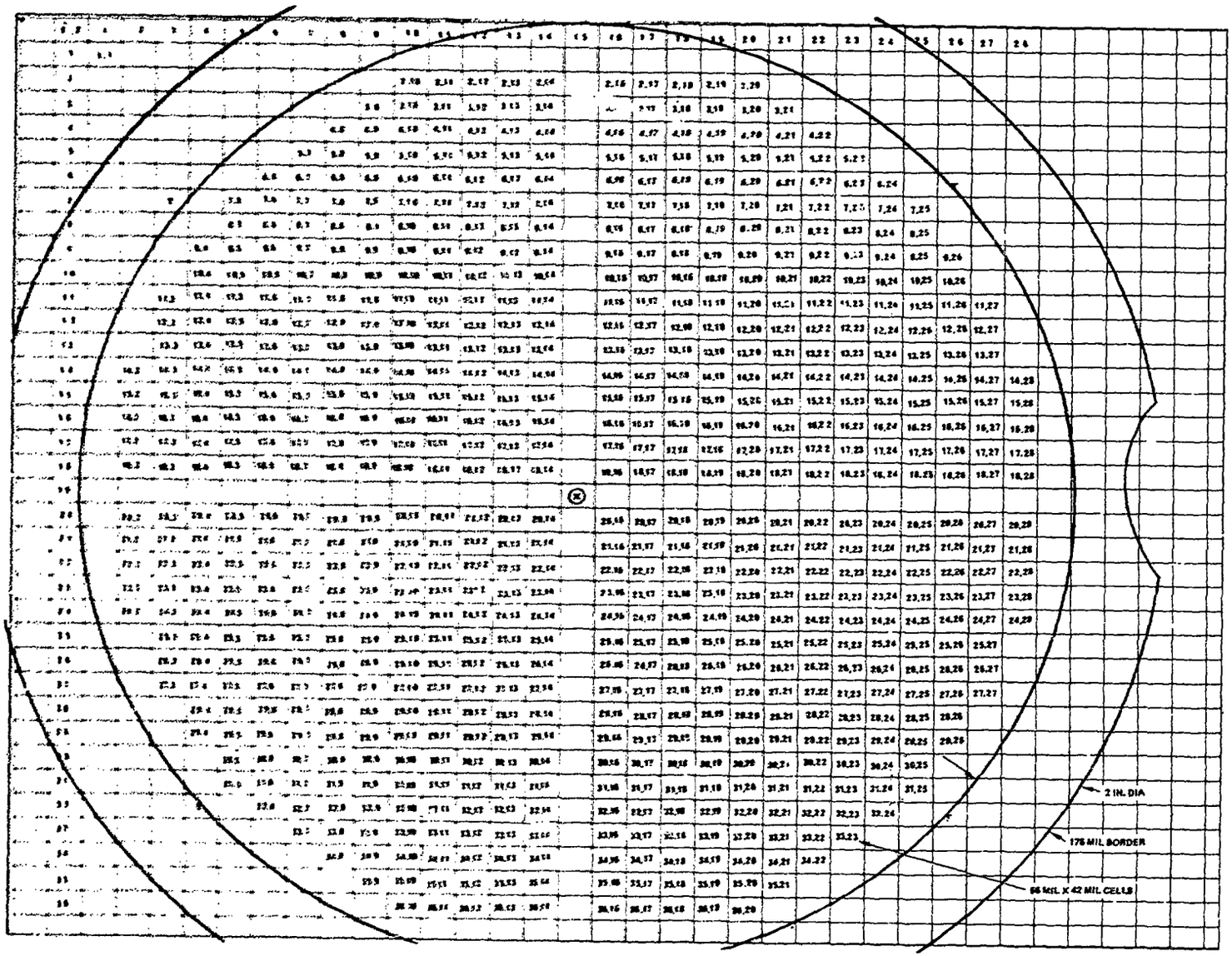



Figure 3. NAND IC wafer - 774 gate cells

for LSI at Hughes contain a mix of logic cells with higher level functions such as Flip Flops, Full Adders, And-Nors, more conducive to most classes of logic requirements.

The "Adder" Wafer shown in Figure 4 contains logic elements most conducive to arithmetic processing. Logic elements consisting of Full Adders, D Flip Flops and gates are listed in the accompanying table and shown in Figure 5. The "And-Nor" wafer shown in Figure 6 contains logic elements most conducive to multiplexing or buss-organized logic. Logic elements consisting of And-Nors, JK Flip Flops and other gates are listed in the accompanying Table and shown in Figure 7. The Logic wafer shown in Figure 8 contains elements for generalized, mixed logic; JK Flip Flops and gates are listed in the accompanying table and shown in Figure 9.

Design of these wafers was based upon the following criteria, listed in order of relative importance:

1. Logic capability (better capability where possible) to second source any design on other vendor wafers.
2. Cell row format selected to enhance pad relocatability and allow efficient second level power distribution system.
3. Row logic types selected to provide for optimum master pattern placement for typical distributed logic flow.
4. Cell logic containing multiples of one element type with I/O symmetry for efficient PR pattern generation.

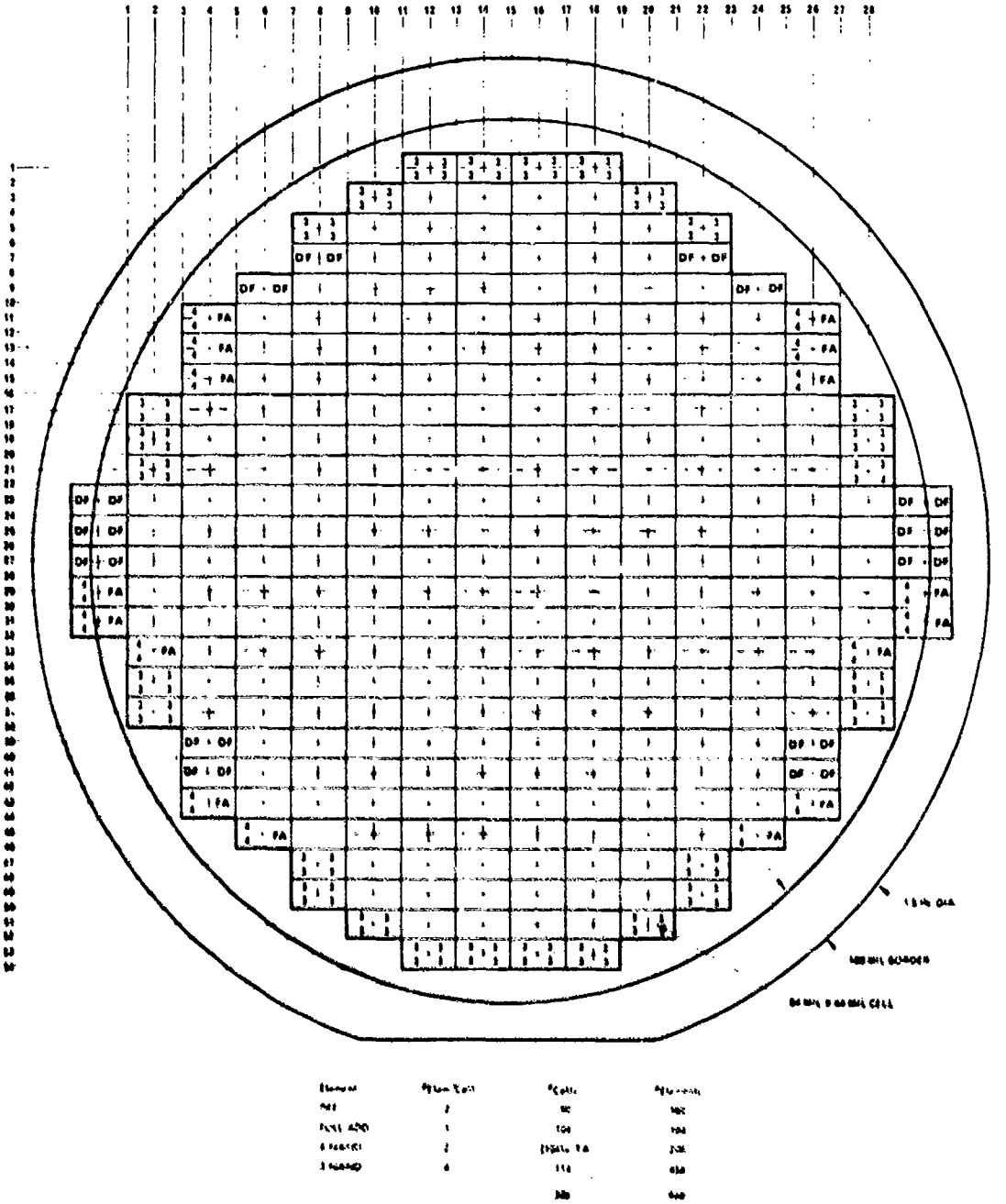
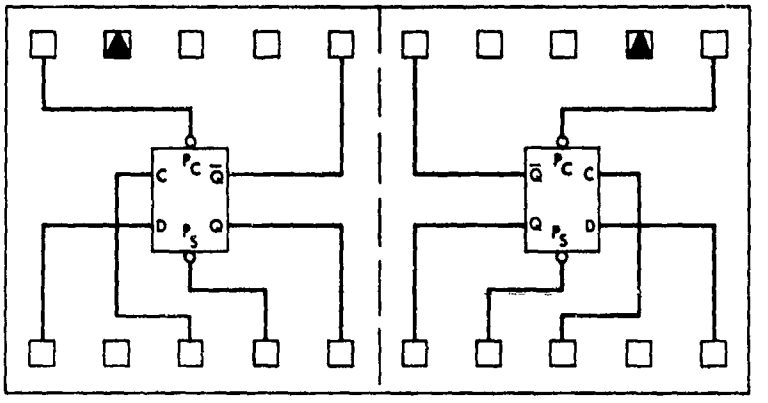
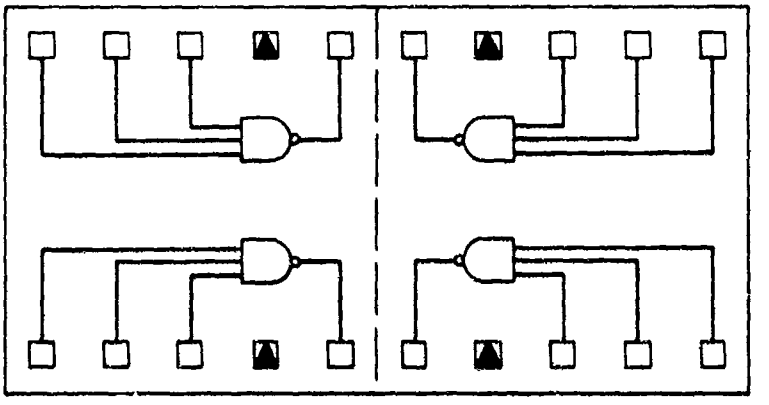


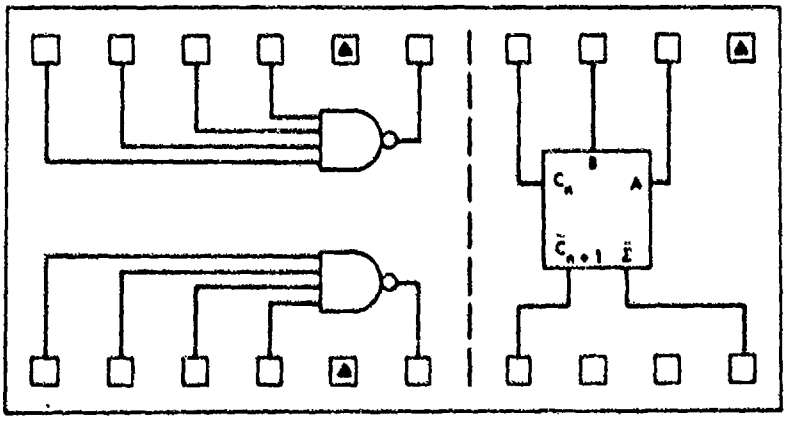
Figure 4. Hughes "Adder" wafer graticule




a. (DF) D Flip Flop cell

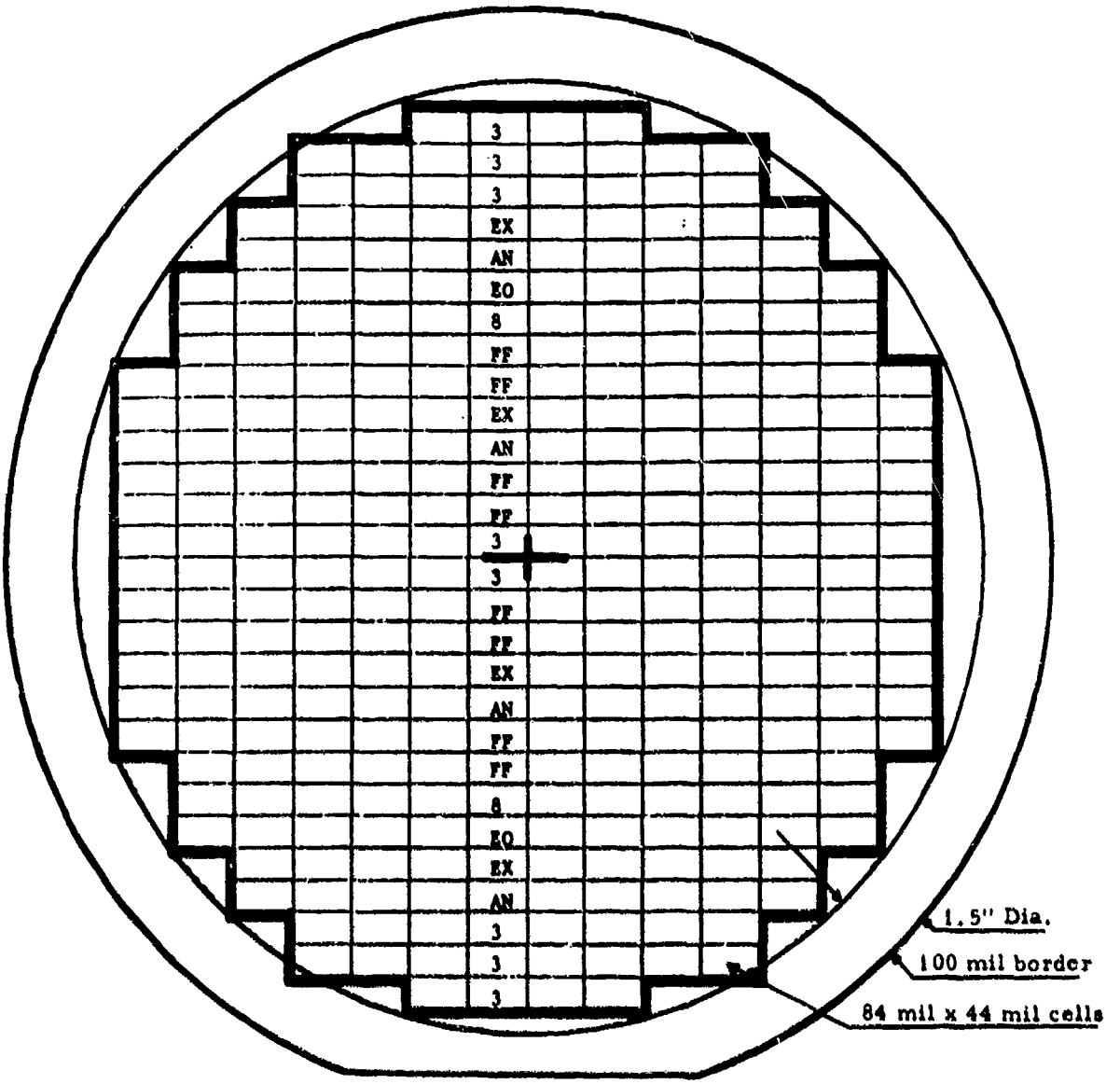


b. (3) 3 Input Nand cell



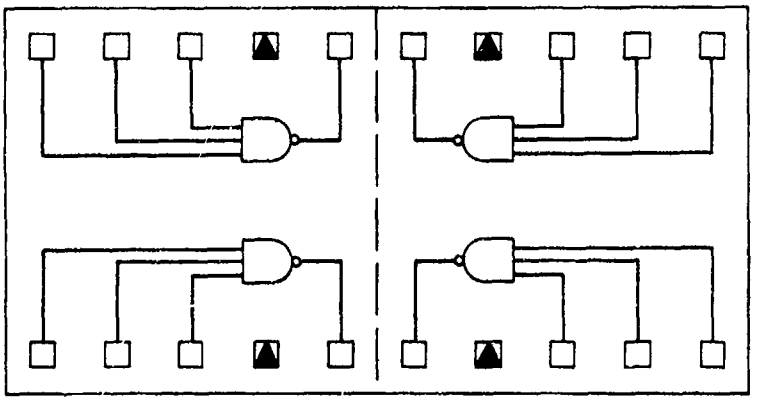

c. (FA) Full Adder cell

Figure 5. Cells available on "Adder" wafer

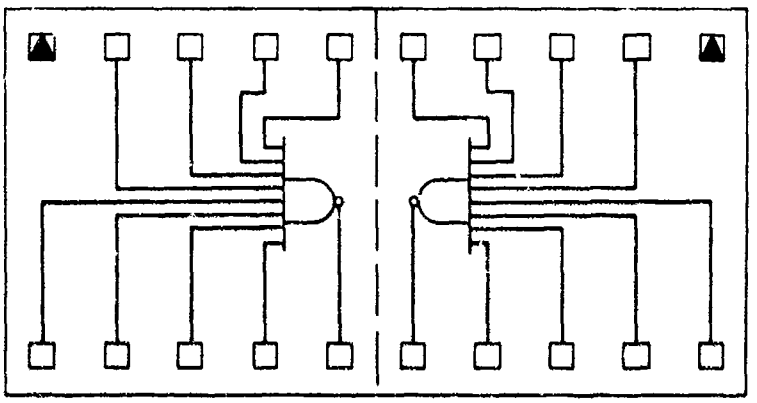



| Element | #Elem/Cell | #Cells | #Elements |
|---|---|---|---|
| JKFF | 1 | 108 | 108 |
| 3x2 AN | 2 | 48 | 96 |
| 2x3 EX | 2 | 48 | 96 |
| EO | 2 | 24 | 48 |
| 8 NAND | 2 | 24 | 48 |
| 3 NAND | 4 | 68 | 272 |
| 1 NAND | 1 | (108)w/JK | 108 |
| | | 320 | 680 |

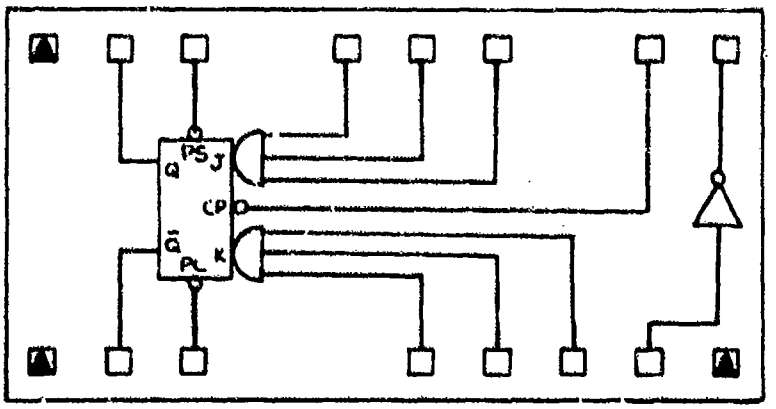
Figure 6. Hughes "And-Nor" wafer graticule



a. (3) 3 Input Nand cell

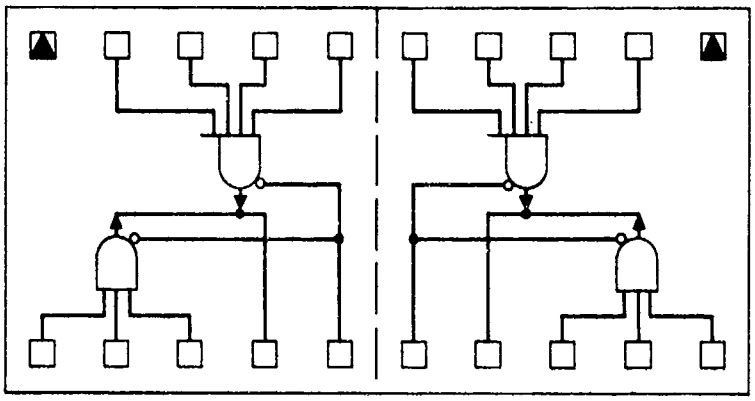


b. (8) 8 Input Nand cell

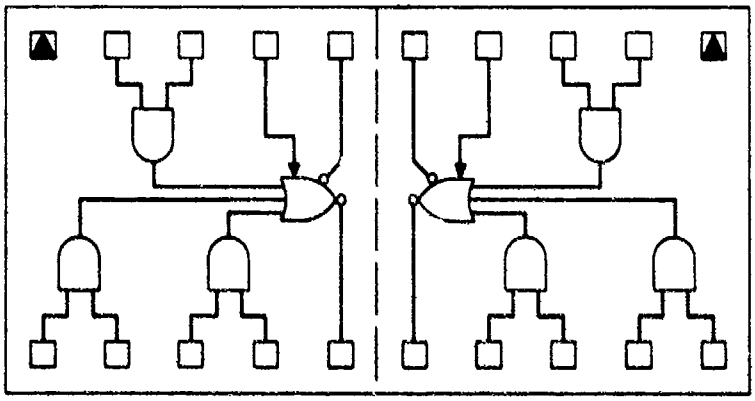



c. (FF) JK Flip Flop cell

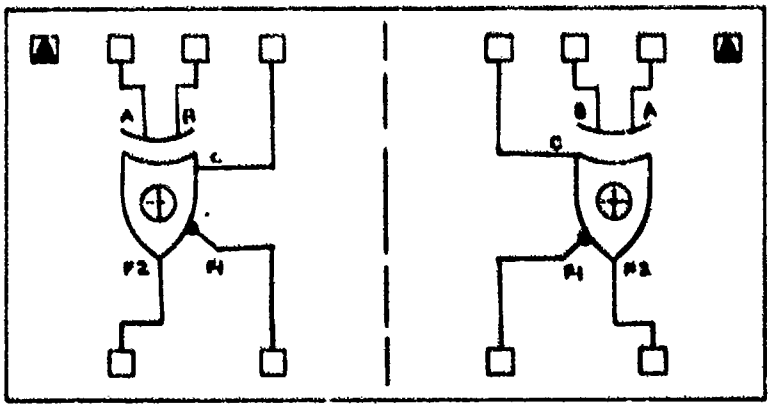
Figure 7. Cells available on "And-Nor" wafer (Continued)



d. (EX) 2 x 3 Expander cell

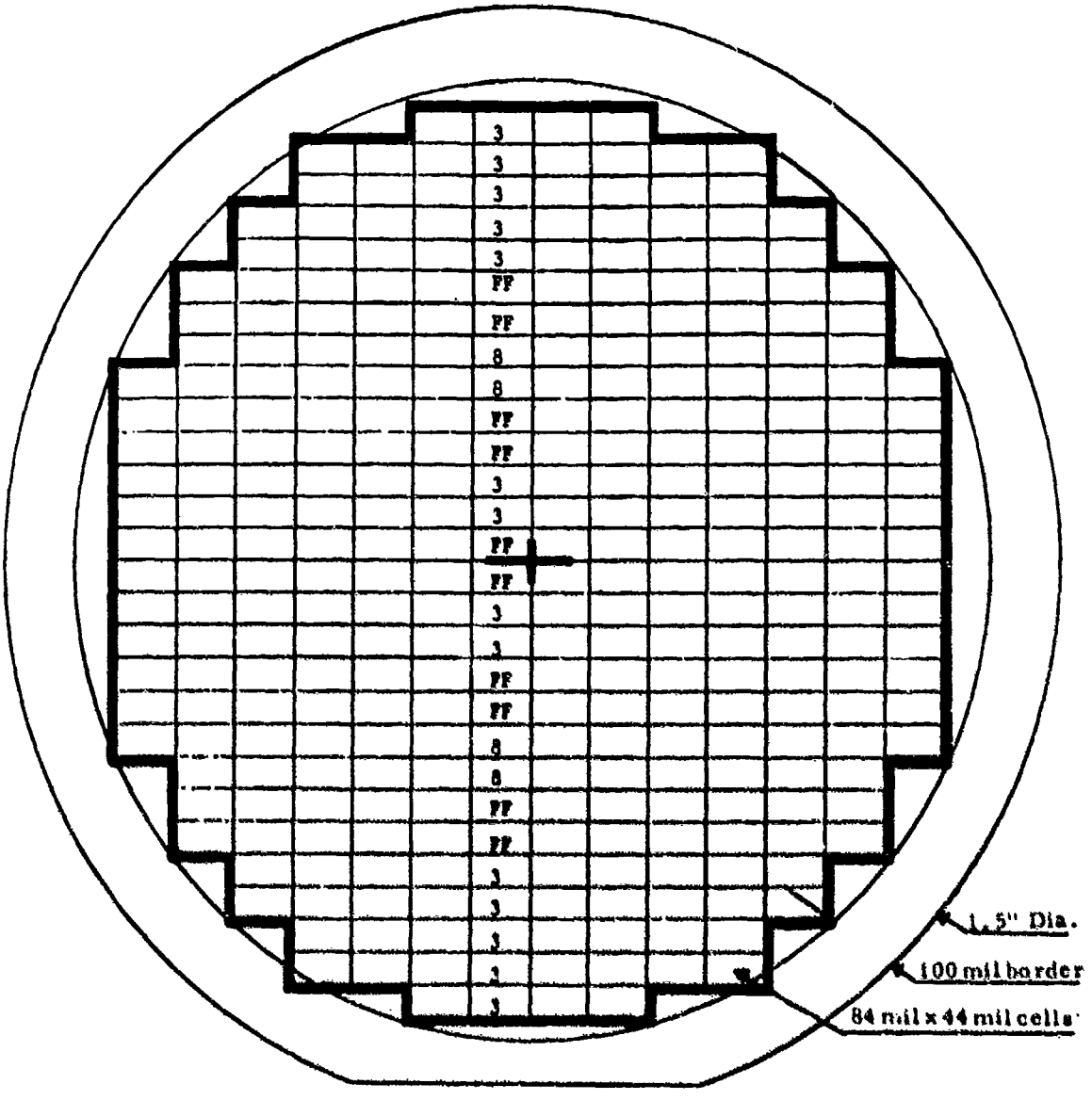


e. (AN) 3 x 2 And Nor cell



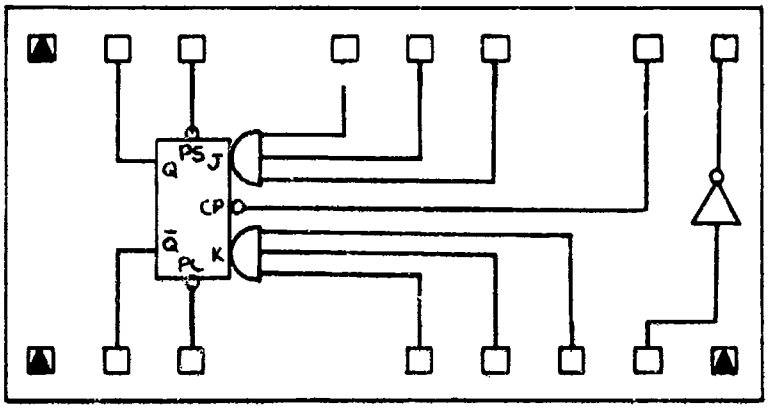

f. (EO) Exclusive Or Nor cell

Figure 7. Cells available on "And-Nor" wafer (Concluded)

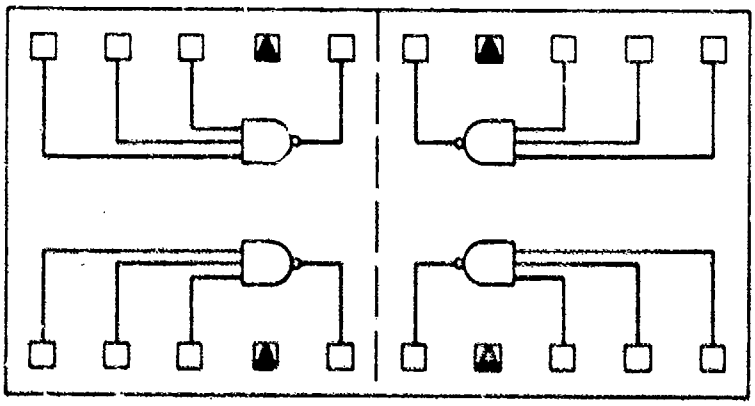



| Element | #Elem/Cell | # Cells | #Elements |
|---|---|---|---|
| JKFF | 1 | 132 | 132 |
| 8 NAND | 2 | 52 | 104 |
| 3 NAND | 4 | 136 | 544 |
| 1 NAND | 1 | (132)w/JK | 132 |
| | | 320 | 912 |

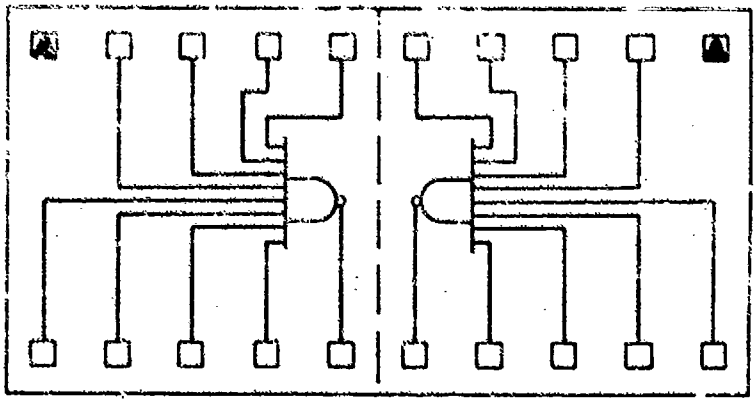
Figure 8. Hughes "Logic" wafer graticule




a. (FF) JK Flip Flop cell



b. (3) 3 Input Nand cell



c. (8) 8 Input Nand cell

Figure 9. Cells available on "Logic" wafer

5. Row logic symmetry with respect to wafers' horizontal and vertical centerlines to provide identical logic counts in half or quadrant wafer partitions.

6. Increased active area to within 100 mils of (1.5 inch diameter) wafer's edge allowing the processing of 320 84 mil x 44 mil cells.

The wafers derived have been applied to a large number of designs already realized in working hardware and planned for future applications.

With two inch IC wafer technology well established, the extension of LSI wafers to two inches is not only natural but desirable. Using the same logic cells, the two inch wafers contain twice as many circuits as one and a half inch wafers as shown in Figure 10. This allows the two inch wafers to contain logic formerly allocated to two "smaller" LSI's and provides system partitioning at a much higher level with much lower production costs. An example of such an application is realized in a mini-computer designed for two "small" LSI's plus MSI's. A two inch wafer was then recently designed to implement the entire mini-computer (less memory) as a second phase. Figure 11 shows the wafer graticule specification to realize this computer-on-a-chip design. Other two inch wafer designs are being pursued to implement more generalized functions as well as specific high density logic.

Cost studies in the area of full wafer LSI versus IC/MSI's have been made. Typically a full wafer one and a half inch LSI recurring costs are roughly $300 in 100-500 quantities. Equivalent 5400 IC Ceramic DIP components priced at Hughes cost roughly $500 in 100-500 quantities. The above

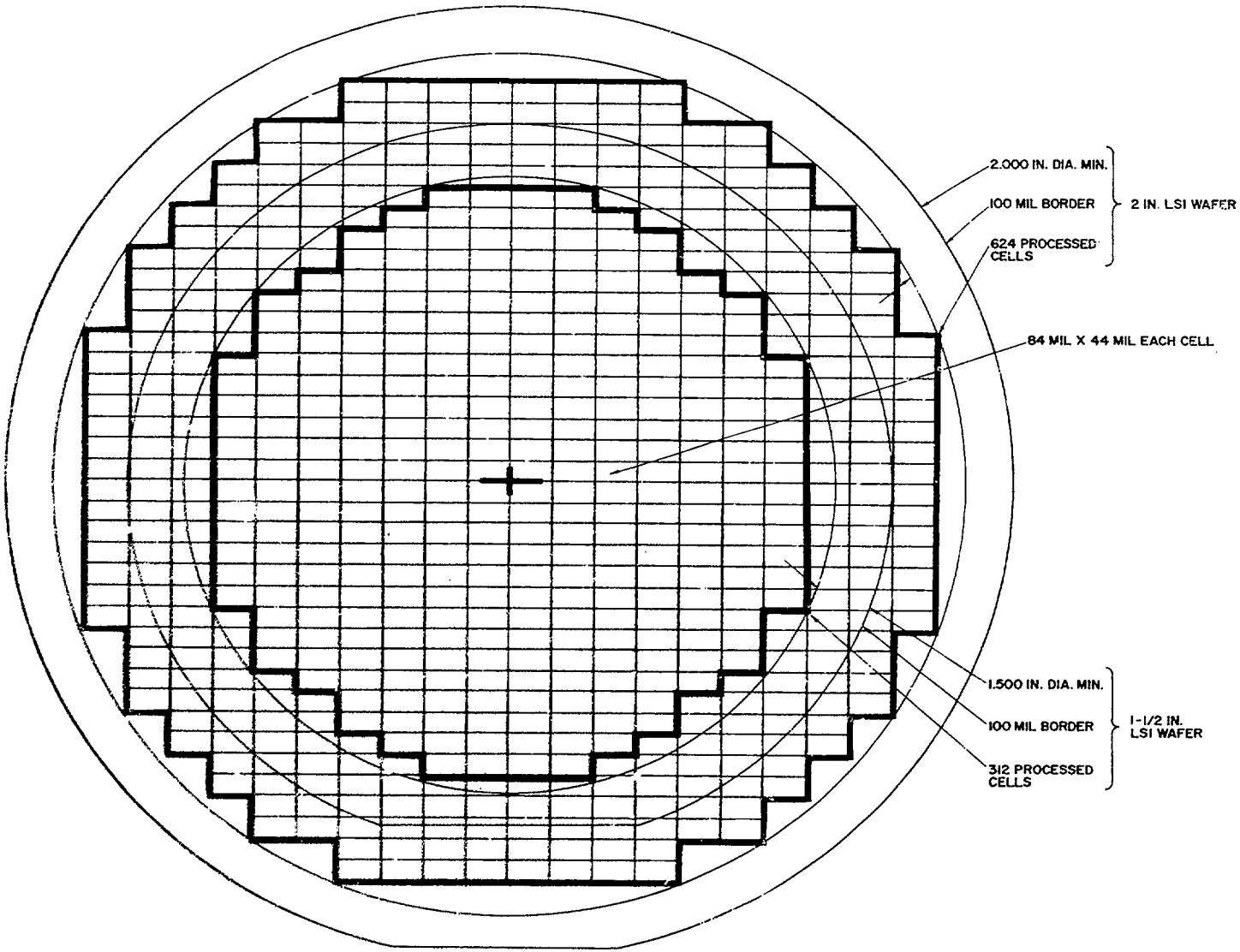



Figure 10. Hughes 2 inch LSI wafer definition with 1-1/2 inch wafer superimposed for comparison

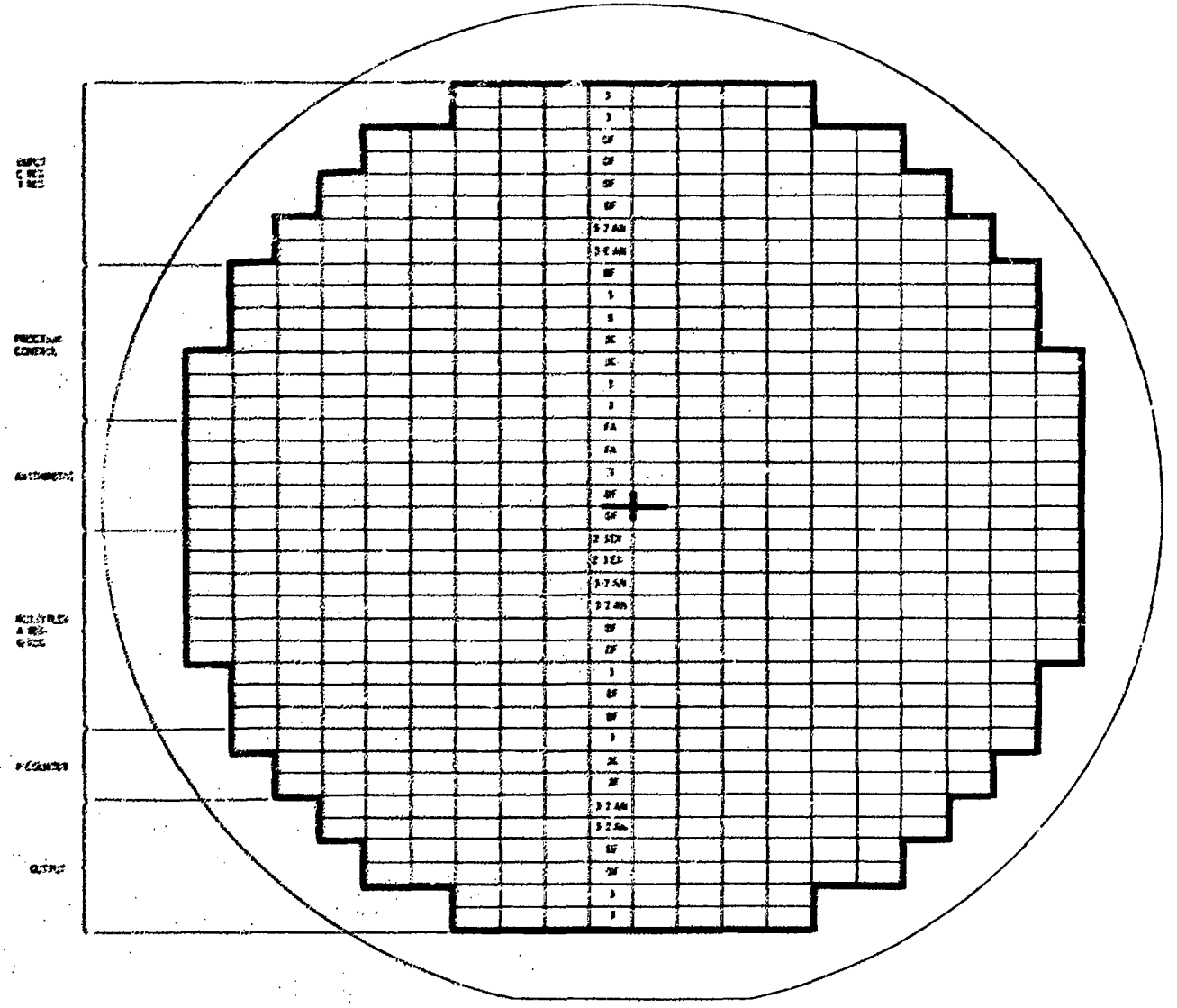


Figure 11. Graticule design of the mini-computer wafer

figures represent component costs only. In the case of the LSI, this includes fabrication and functional test, not included in the IC component cost. When inspection, test, assembly, board test, module interconnect and assembly are complete, LSI shows a clear cost advantage over the individual IC's for military production quantities; and this cost is still exclusive of inherent LSI cost advantages of higher reliability, and reduced weight and volume.

Systems can be constructed of LSI components in two general ways: (1) through standard functions with general utility designed for multiple use among several systems or classes of systems and (2) through specialized "random" logic arrays designed for a specific system.

Standard LSI functions offer several advantages:

1. LSI components are obtained without recurring costs for each new system. Off-the-shelf functions become available at several hundred gate complexity.
2. Lower cost is realized through greater production quantities of LSI parts. Advantages of large wafer production are brought to small part type production runs for military equipment.
3. Logistics problems are eased through reduction of part types and the use of types in several systems.
4. Design of new systems is aided by available components. Second sourcing becomes easier and more economical.

Standard LSI parts should have multiple system uses, at least within a class of systems, as radar or displays. Such functions are able to implement processing required by all members of a class of systems. The large potential production of standard functions achieves maximum benefits of pad relocation. Extensive use of such LSI functions will require relative high production rates. Advantages of standard LSI components must be traded off against design inefficiency required for generalized components.

With design for a range of applications the resulting logic will not be fully used for each application. This may take the form of additional logic which is only utilized for certain applications, or excess speed for others. Greater power dissipation than custom designs will then result.

The inclusion of logic not needed in all applications will incur no volume penalty in full water LSI. Overall dimensions of the wafer and wafer package are not affected by logic interconnect within the array. Using pad relocation techniques, the additional cost of logic used only for some applications is small. The only additional cost of consequence is that of one time routing the additional logic. (If the more complex wafer is to be routed anyway, this would not be an added cost.) In any case, additional cost per unit would be very small amortized over even a small number of units.

Additional logic would increase the silicon area used for the 100 percent yield approach. This would increase cost by lowering yield. Original mask design cost would also be higher. Although chip size may increase through logic only having application in some uses, overall package size would not change.

Greater power dissipation of additional logic and, perhaps, small incremental component cost must be compared with the advantages of high volume production of a small number of designs, and simplified logistics for elements common to many systems.

Examples of widely useful components of LSI complexity have been demonstrated through Hughes contractual effort to define such components for radar and communications digital filtering systems and contractual and internal studies of airborne data transmission, shipboard display logic, digital computer, and advanced standard hardware program (SHP) functions.

Five LSI components embodying commonality found in radar and communications filter processing systems, were defined and designed in study under Air Force Contract F33615-69-C-1804.* Using present LSI technology, the components defined perform digital filtering functions required for present and near future radar and communications processing.

Components of LSI complexity found to have the greatest commonality were a 3 input adder-accumulator, a multi-input carry save adder tree, an adder-subtractor with multiplex gating for one set of inputs, multipliers, and digital correlators. In combination with memory circuits, these components can modularly implement varying filter algorithms of different data rates and data word lengths. Filter processors which can be realized efficiently with the LSI components include linear digital filters, Fast Fourier Transform processors, add-only base processors, communications correlators, and pulse compressors of several code types.

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*N. Benowitz, J. K. Crosby, and I. Dlugatch, "Digital Filters for High Speed Data Processing", AFAL-TR-70-192 Volume I.

A set of 10 functions have been designed for LSI application to implement varying digital computer and computer-like hardwares.* The character set, as the building blocks are called, utilize microprogrammed ROM blocks for control, while storage, computational logic, and data paths are supplied by remaining characters and their interconnection. Characters include functions of register storage (G1 character), logic and arithmetic operations (L1 and L2), input/output (L3), microprogram storage and its control (M1, M2, and MM), scratch pad storage (P1), counter and related control (P2), and multiplexing (P3).

Study of a shipboard display console identified three other generalized LSI components which, through multiple use, might form well over half of the 47 LSI arrays needed to construct the console.

Under Air Force Contract F33615-70-C-1072 Hughes has designed a generalized aircraft fault-tolerant multiplex data transmission system (DADS) and, using pad relocation, successfully obtained an LSI design implementing a substantial portion of system logic. The DADS system can interconnect airborne equipments having a wide range of signal format, data rate, and reliability requirements. The system is modularly adaptable to meet current and future aircraft systems requirements.

LSI may also be used to implement and extend existing standard hardwares, as the Navy SHP program. One approach is to implement several SHP functions on a single wafer, scribe the wafer and individually package the resulting functions on SHP 1A cards. An alternative is to define standard functions of greater complexity.

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*"Characters-Universal Architecture for LSI," F. D. Erwin and J. F. McKevitt, Proceedings Fall Joint Computer Conference, vol. 35, 1969, pp 69-79.

The present full wafer TTL bipolar LSI designs have been successful in meeting fabrication requirements and in meeting requirements of systems employing 5400 class logic. The concept has been shown to be very feasible, thus extension of the present LSI technology has been examined. One of the most promising extensions seems to be in the use of MOS in full wafer LSI.

A preliminary study of MOS full wafer LSI was started at Hughes Aircraft Company late in 1970 with preliminary results being presented here. A sample system for MOS implementation was examined for applicability of the present existing LSI techniques as developed for bipolar pad relocated LSI. Some of the aspects are listed below.

1. Comparison and choice of MOS logic types (DC ratio, 2ϕ ratio, 2ϕ ratioless, 4ϕ ratioless, P-MOS, C-MOS, etc.) for use in full wafer pad relocated LSI.
2. Basic cell circuit function considerations.
3. Pad relocation considerations for a MOS cell.
4. Multilevel processing effects which influence circuit operation and pad relocation design rules.

Circuit, logic, processing and design factors were examined with the results indicating that the basic bipolar developed LSI techniques could be applicable to full wafer MOS LSI. The MOS logic types which seemed the most applicable were DC ratio and 2ϕ ratio. Though such things as packing density, power, and speed were considered, the main choice of applicability resulted from the ease of electrical design. Ratioless circuits were eliminated because they were thought to be too difficult to use in an LSI system which, by nature, has a large number of design variables. Many iterations

of design and layout are usually required with ratioless design before satisfactory operation will result. These iterations just do not fit in well with LSI whether it be full wafer pad relocated LSI or the standard library CAD MOS 100 percent yield LSI.

MOSFET circuits are generally slower and more sensitive to circuit drive requirements than bipolar, but possess the significant advantages of lower power, simpler processing, higher yield, lower cost, and higher packing density. The most efficient use of MOS circuits has been in the design of highly used complex logic cells such as DDA's, multiplexers, decoders, counters, shift registers, ROMs, etc. Such logic cells optimize the advantage of the MOS higher yields and component packing densities while also providing known load characteristics on all internal circuits. However, only a portion of conventional digital systems can make use of these higher level logic functions. Simple gates, flip-flops, adders, etc., must be interconnected to realize the other digital requirements, especially the control logic of general and special purpose processors. The use of simple elements, however, brings a low packing density due to the need of large probe pads for input-output which takes up a major portion of the cell area. In addition, exact load conditions at the outputs of these circuits are not known. Thus a standard load has to be assumed, producing no optimization of power as would be available in the internal elements of complex functions.

The basic cell study produced a set of three circuit cells which proved very effective for implementation of the example system. Such considerations as circuit speed, size, power and utilization were made in the design of the cells. Since these cells were designed to implement a particular

system, they were not truly universal logic blocks with which any logic system could be implemented. Advantage was taken of the fact that the example system displayed a limited repetition of a group of random logic blocks which in themselves showed a fair amount of similarity. The three circuit cells consisted of (1) a logic cell of five semi-interconnected gates which could be reconfigured into five differente gate configurations by metalization additions as part of the relocation pattern; (2) a flip-flop and gating which could be used by itself as a flip-flop or as the complement part of the partial counter cell; (3) a set of three flip-flops and gating which can be connected as a decimal or binary counter when used in conjunction with the flip-flop cell.

The cell circuit design exercise gave some insight into the difficulties involved with universal cell design. The study of pad relocation considerations for MOS cells showed that with very little extension of present techniques, MOS cells could be relocated even in the case of clocked logic elements.

The multilevel processing study provided practical limits for physical parameter values which influence circuit operation and processing. This study provided some assurance to the compatibility of MOS PR LSI design and near future physical or practical limits of multi-level processing. In addition to the study, actual experimental work to demonstrate MOS capability to multi-level processing has been conducted. Work done has included the interconnection of 2-phase dynamic shift-registers on a wafer. The metalization has been two levels of aluminum above that of the basic circuit metalization. Encouraging results have been gained with progress toward process finalization being planned.

Future MOS LSI work will include a study of the use of CMOS circuits and the actual design and fabrication of a MOS full wafer LSI of either conventional PMOS or CMOS. The use of ROM, multiplexers and functional cells in doing random logic will be examined. These approaches offer the potential of large gate complexity and yet allow a general enough usage. Items such as these take full advantage of the size, power, and complexity advantage of MOS, thus would use MOS potential better. In the direction of reducing power, low-voltage CMOS capability, which exists in-house, will be examined for reduction of operating power. This will complement the lower quiescent power available with MOS.

The complexities which might be possible for random logic full wafer PMOS LSI are in the 3000 to 5000 gate equivalent range. Operating speed would be about 1 Mhz. For CMOS random logic LSI, the possible complexity seems to be about 10,000 gate equivalents with an operating speed of about 2-5 Mhz. These figures are for 2" diameter wafers. Both limits are due to power considerations of the packaged array. Though CMOS and PMOS require different areas for circuit implementation, size does not seem to affect the complexity as much as the power aspects. The complexity figures are based on a reasonable usage of medium complexity cells.

Future bipolar LSI will extend into the areas of bipolar speed and lower power. Immediate work in higher speed circuits seems to favor the use of Schottky clamped TTL since this technology is basically similar to the TTL technology in LSI at the present time. The complexity of near future Schottky LSI will probably not increase too far above the 500-600 gate equivalent of present LSI due to the power dissipation limits of the LSI packages

presently available. The speed of operation will probably increase by a factor of 4 or 5, and with only a two-fold increase in power. Low power LSI seems to be an even easier extension of present technology. Since low power TTL dissipation is about 1/10 the power of conventional circuits, power limitations are secondary and size of circuitry assumes the main importance. A complexity of about 1,500 gate equivalents is thus a practical goal for such bipolar near future work.

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COMPONENTS GROUP

# Electrochemical Processing of Multilevel Interconnect Patterns for Micro-Circuits

## (Anodized Aluminum)

by

B. G. Carbajal and W. R. McMahon
Texas Instruments, Inc.
Dallas, Texas

## INTRODUCTION

Within the semiconductor industry, the need for multilevel technologies for fabricating interconnect patterns on circuits and/or on substrates increases continually. Increased complexity and speed, reduced geometries, reduce chip size and the inverse relationship between the yield and bar size all point to the requirement of a multilevel process. Those of us involved in development activities have long sought for a viable multilevel process. If bipolar memories are to make advancements in the near future, a multilevel technology is required. Because of the complexity and routing problems involved a simple and reliable two-level process is a must. The simplest form of multilevel interconnect pattern is comprised of a single level of metallic interconnect in conjunction with diffused tunnels in a semiconductor substrate. This paper deals however, with multilevel metal interconnect patterns which may or may not be fabricated on a substrate containing diffused tunnels. The process described may in fact be applied to interconnect patterns on insulating substrates, such as, substrates for use in a circuit packaging.

Yield loss and reliability failures in conventionally processed multilevel metal interconnects can be attributed in large measure to the topology of the surfaces upon which successive interconnect levels must be delineated. The topology upon which the first level must be fabricated is determined by the previous processing of the semiconductor and/or of the substrate material. All subsequent levels how-

ever, are fabricated over surfaces with topologies dominated by previous interconnect levels. Steps equalling or larger than the metal thickness are encountered at both crossovers and at via hole areas. Unless extreme care is exercised in the design of such circuits, these steps can exceed twice the metal thickness at the third level of interconnect pattern.

An electrochemical process is described in this paper which minimizes this problem of topology in multilevel processing. The use of the process described herein has a resultant structure in which the interconnect leads are embedded in an anodic insulating oxide. The anodic process is also used to create the insulating layer between the levels of interconnect. The planarity of the upper most surface of such an interconnect pattern provides an excellent surface topology for the fabrication of successive interconnect levels. An iteration of process steps is all that is required to add additional levels of conductor patterns.

Before entering into a discussion of the process and the steps involved in effecting the anodic process, let us consider the topology advantages to be gained via the anodic process. Figure 1 depicts a test pattern of a two-level interconnect pattern processed in a conventional manner. The metallurgy of the interconnect system is 99.99% aluminum and the multilevel insulator is deposited silicon dioxide. Delineation of the first level of interconnect pattern was accomplished in a conventional metal leach process. In the fabrication of the structure of Figure 1, little care was exercised to taper the edges of the first level metal. Upon subsequent deposition of the insulating oxide over the first level of interconnect pattern, there is a high probability of a re-entrant fold existing in the insulating oxide in those areas. These re-entrant folds often result in shorts between the first level and the second level of the multilevel structure. A second area of concern in conventional processing of multilevel interconnect patterns is at the via hole contact windows. In order to form the via holes in a conventional process one must chemically remove the deposited silicon dioxide film in the via

hole area in a matter so as to completely clear the hole and yet not overetch to the degree that one destroys the first level interconnect pattern in the via hole area. Etchants which are totally selective, that is etchants which will etch $SiO_2$ and have no effect upon aluminum, are not yet developed. Thus the etching of via holes is an extremely critical step in that if an underetch is encountered the via hole continuity will not exist and if an overetch is encountered the first level interconnect pattern can easily be destroyed. Assuming it were possible to fabricate multilevel structures to this point, that is to the point where the substrate is ready for deposition of second level metal, it becomes apparent that the topology created by the fabrication of the first level interconnect and by the via hole etchings offers a new problem area which is unique to the second level interconnect pattern. The steps encountered at the lead edges and at the via holes are at least equal to the thickness of the first level interconnect metal and of the insulating oxide. If care is not exercised in tapering the edges of the first level metal pattern and tapering the edges of the via hole, discontinuities in the second level metal interconnect pattern is not only possible but indeed quite probable as revealed in Figure 1.

If care is exercised, and steps are taken to taper the edges of the first level interconnect pattern, and if the deposited inculating oxide layer is deposited in such a manner that the upper most surface etches at a faster rate than the lower surface and via holes are there by tapered, it is possible as shown in Figure 2 to have a second level interconnect pattern with a high degree of integrity. Figure 2 then is similar to what one could expect from the most advanced methods of using conventional processing to fabricate multilevel interconnect pattern.

Figure 3 depicts the same structures of Figure 1 and 2 but in this figure an anodic process has been used to fabricate a two-level structure. There are several things to note about Figure 3, consider first the topology of the upper most surface of the insulating oxide over which the second level metal is deposited. Note the lack of steps at

the first level lead edges and the lack of a step at the via hole area. This figure clearly shows that the planarity of the surface upon which the second level metal must be deposited is superior to even the ultimate which can be achieved by conventional processing.

Figures 1, 2 and 3 are Scanning Electron Micrographs and are presented only as comparison of conventional processing versus anodic processing of two-level interconnect patterns. It should be noted that in all cases the second level pattern was delineated by a conventional metal etch technique. In the anodic process, for purposes of demonstration, the second level was also delineated by a conventional etch technique. If the second level of Figure 3 were to be fabricated by an anodic process the second level interconnect leads would be embedded in an anodic oxide as are those of the first level interconnect. A Scanning Electron Micrograph of such a structure would not reveal as clearly as does Figure 3 the topological advantages to be gained via the anodic process.

## ANODIZATION OF ALUMINUM

It has long been recognized that the corrosion resistance of aluminum is due to the natural oxide films which forms on the surface of the metal when it is exposed to any oxidizing conditions. This oxide film is only a few tens of angstroms in thickness but does act as a barrier against further corrosion of the metal surface. When an aluminum part is made the anode in a cell containing an appropriate dibasic acid a process takes place which is very similar in nature to the natural oxidization of aluminum when it is exposed to an oxidizing ambient. The difference being that the oxide growth mechanism is enhanced by the application of an electric field. It is possible to grow aluminum oxide films of several mils in thickness via this process known as anodization. The electrolyte used for the fabrication of multilevel interconnect patterns in this paper is one that has a finite solubility of the oxides which are formed in the anodization cell. Figure 4 represents the type of structure which results. When an electrolyte is used which does have finite solubility

for the oxide a porous structure results. Each pore has an associated cell surrounding it. These cells are comprised of aluminum oxide which varies in its compositions with electrolyte. There are several characteristics about the cell which are independent of the electrolyte used in the formation of the anodic oxide. First the pore is separated from the metal surface by a layer known as the barrier layer. This barrier layer varies in thickness with voltage applied to the anodic cell and is independent of the electrolyte used. The cell wall thickness is also proportional to the applied voltage in the anodization cell. The pore diameter has been found to vary with current density used in the formation of anodic oxides. The anodization process proceeds by means of ionic migration across the barrier layer at the pore base. This ionic migration forms new oxide at the metal-oxide interface. Simultaneously with the formation of this new oxide there is dissolution of oxide by the electrolyte at the pore base. Thus as the process continues an equilibrium state is reached in which the rate of formation of new oxide is equal to the rate of dissolution of oxide at the pore base. This process will continue so long as the voltage is applied and electrolyte is available for the oxidation process.

As the metal aluminum is anodically converted to its oxide there is an associated volume increase. This causes the anodic oxides to be in compressive state as they are formed. It is this compression factor which limits the thickness to which one may grow an aluminum oxide film. When growing films of excessive thickness steps must be taken to minimize or alleviate these compressive stress or else they will be self destructive. Such failure mechanisms are often noted when parts of the sharp edges are to be anodized. The films used in the fabrication of multilevel integrated circuits, as is purposes of this paper, were in the range of 1 to 1 1/2 microns in thickness. Total conversion of films of these thicknesses to their andoic oxide did not result in any failure mechanisms via this compressive mode. Since the oxides which are formed by an anodization mechanism are comprised atomistically of the metal atoms of the films themselves its adhesion is found to be excellent. The metal films of this paper

which were anodically converted to their oxides were vacuum deposited upon silicon dioxide surfaces. Aluminum films because of their electronegativity and/or oxygen affinity adhere very well to silicon dioxide surfaces. It has been found that when such adherent films are totally converted to their oxide, the oxide of aluminum also adheres well to be silicon dioxide surface. During the course of this investigation there was in no case any delamination noted of the oxide from the metal or from the silicon dioxide surface. Thus the mechanical stability of such a material system for the fabrication of integrated circuits is well demonstrated.

## THE ANODIC FABRICATION OF MULTILEVEL INTERCONNECT PATTERNS

Figure 5 depicts a sequence of processing steps used in the fabrication of a single level of the multilevel interconnect pattern. Figure 5a depicts schematically the structures upon which the interconnect patterns will be fabricated. It consists of a semiconductor substrate with its associated diffusions. Covering the surface of the semiconductor substrate is an oxide insulation level with contact windows cut in the oxide. An aluminum film of 1 to 1 1/2 microns in thickness is deposited on the surface then of this total structure. Figure 5b depicts the first step in the processes used to produce the multilevel interconnect pattern. The step introduced at this point is the masking of the via hole areas on the surface of the aluminum. The via holes are masked with photoresist and a conventional photo lithographic process. Following the masking step the structure is introduced into the anodization cell and made the anode of that cell. An oxide is then grown on all of the surface of the deposited metal film except at the areas of the via holes. During this anodic process there is a moderate volume increase which varies with electrolyte from 20 to 50%. At the end of this anodic process the via holes areas are still metallic and all of the areas are coated with an anodic oxide of aluminum. The thickness of this anodic oxide is controlled very simply by monitoring the current density and time. The thickness of oxide produced is directly proportional to these two parameters. This thickness may be varied

from a few angstroms up to more than a micron. Circuit parameters determine the desired thicknesses since it is the oxide that is grown at this point in the process which becomes the multilevel insulating oxide. Parasitic capacitances between the levels on interconnect thus dictate the thicknesses which must be grown at this point in the process step. Figure 5c depicts the next process step which is used in the fabrication of the interconnect level and shows the photomasking step in which the leads are defined in a photoresist pattern. This photoresist pattern serves to seal off the pores which were grown earlier in that portion of the wafer which is to contain the interconnect pattern. Following the masking step the wafer is re-introduced into the anodization cell and the anodic process continued. Those areas of the wafer which are masked will no longer anodize since the pore sturcture which was formed earlier is sealed off by the photoresist material. The area of the wafer which is unprotected by photoresist will continue to be anodized. The direction of the anodization front during this portion of the anodic process was pre-determined by the first anodization process. The pores which are found in the previously grown anodic oxide are oriented normal to the surface of the wafer and the process continues via new oxide growth at the base of these pores. Thus the direction of the anodization front is normal to the wafer and the process continues until all of the metal which is between the lead system is converted to the anodic oxide. The fact that the anodization front does have a pre-determined direction offers several advantages. The chief advantage being that the cross-sectional area of a given lead is maintained and there is no associated undercut of the photoresist material as is often noted in the conventional metal etching techniques. A second advantage is that because of the directionality of the anodization front the process is found to be a self limiting process. That is, when the metal between the interconnect patterns has been totally converted to the anodic oxide the current of the anodization cell drops to extremely low levels and the anodization process ceases. Anodization times of 300% greater than that required for the conversion of unwanted metal to its oxide have shown no

reduction in the cross-sectional area of the interconnect pattern. Thus the process lends itself well to a totally automated production facility. At this point in the process the photoresist materials are stripped from the surface of the wafer and the entire structure given a thermal threatment to totally dehydrate the anodic oxide. The wafer is then ready for an iteration of the process steps we have just gone through for the fabrication of the second level of the multilevel pattern. If the second level of the interconnect pattern is to be anodically fabricated as well as the first, a simple iteration of these process sequence is all that is required. However, one of the anodization parameters must be changed substantially, that parameter being the applied voltage in the anodization cell. If the same voltage is used in the delineation of the second level as was used in the delineation of the first level, the process is not self limiting. That is to say when the interconnect pattern has been delineated in the second level the anodic process will continue and the first level leads will be consumed. As was discussed earlier, the anodization process proceeds via a field enhanced diffusion mechanism of ions across the barrier layer formed at the pore base. The thickness of this barrier layer is therefore voltage dependent. If in processing the second level the voltage is used which is less than that which was used in the fabrication of the first level of interconnect pattern, the process becomes self limiting. That is to say that the barrier layer which was formed at the pore base of the first level interconnect pattern is of sufficient thickness to retard or to inhibit ionic migration under an applied field of lesser magnitude. It has been experimentally determined that if the voltage levels used during the fabrication of the second level of interconnects are 35% lower than those used in the fabrication of the first level the process is self limiting. This 35% reduction reduces the magnitude of the field found across the barrier of the first level interconnect pattern to a magnitude where ionic migration virtually ceases. If three or more layers are to be fabricated an iteration of the same process sequence is all that is required, but for each successive level a voltage reduction must be utilized. Associated with a voltage reduction there is of course a reduction in the current

densities which are encountered in the anodization cell. This reduction in current densities can change the pore diameter of the successive levels of multilevel insulators. However, for two-level structures there is no deleterious effects encountered when the second level is anodically fabricated. It should also be pointed out that the second level of a two-level interconnect pattern can be fabricated in a totally conventional manner. The anodic oxide which is formed on the surface of the lead system at first level does act as an effective etch stop against metal etchants which are used to delineate the lead pattern of the second level. The disadvantages of this system are obvious in that the second level interconnect pattern is totally exposed and has no chemical and/or mechanical protective overcoat. It would be totally possible to use deposited oxides for this purpose and thus use a hybrid type of fabrication method. Let us refer again now to the final structure shown in Figure 5d. It is interesting to note that the volume increase associated with the conversion of the metal aluminum to its anodic oxide does not introduce any major steps in topology of the upper most surface of the anodized interconnect lead pattern. Note that the lowest point on the surface of the pattern corresponds to the via hole area and the highest most point on that surface corresponds to the area between the leads. If an electrolyte is chosen which has an associated volume increase of 20% we have an 80% reduction of the step heights to be found at lead edges and an 80% reduction of the steps to be found at the via hole areas. Scanning Electron Microscopy work as well as Talysurf work has revealed that not only are the steps reduced in their magnitude but are gently sloping steps. Because of this reduction of 80% in magnitude and because of the tapering of the steps which are to be found on the surface of such an interconnect pattern it is a simple matter to form an additional level on interconnect pattern which has a high degree of integrity.

## PROPERTIES OF THE ANODIC OXIDE OF ALUMINUM

Although it is totally possible to introduce an additional

oxide as a multilevel insulator in the anodic process some of the topological advantages to be gained by the anodic process would be lost. It is therefore of interest to consider whether or not the anodic oxide of aluminum can be used as an effective two-level insulating material. In two-level structures the parameter of concern to the design engineer is the parasitic capacitances to be found between the levels of interconnect pattern. These parasitic capacitances are of course related to the thickness of the multilevel insulator as well as to the dielectric constant of that insulator. We have shown that the thickness of this indulating oxide can be made up to 1 1/2 microns in thickness, but a parameter over which we have no control is that of the dielectric constant of the anodic oxide. This dielectric constant has been measured by others as well as ourselves and our data is in good agreement with the literature. Figure 6 is a plot of the dielectric constant of the anodic oxide of aluminum versus the frequency of the field under which it was measured. It is interesting to note that there is very little frequency dependence of the dielectric constant and that its magnitude is in the 8.5 to 8.7 range. This magnitude is approximately twice that which is encountered in conventionally deposited $SiO_2$ films. It is a nearly impossible task for the design engineer to predict what are the limits of parasitic capacitances he can tolerate in a newly designed circuit. He can however use layout rules which minimize the area of the capacitors to be found in the multilevel circuit. In our evaluation we have used existing circuitry and applied the anodic process to the existing circuits. Although we well recognize that the parasitic capacitances in these circuits were increased in two ways by the application of the anodic process, that is by thinning of the multilevel insulator and by the increased dielectric constant of that insulator, we have found no deleterious effect to the operation of these circuits. Prior to the existance of the anodic process the multilevel insulators were made of thicknesses which ranged from 1 to 2 microns, these thicknesses were dictated by the need to have an effective insulator between the levels of interconnect pattern and not necessarily chosen to optimize the parasitic capacitance levels.

At this point it appears that a trial and error method must be used to determine whether or not parasitic capacitance problems will arise by the use of the anodic process. It is desirable from a structural point of view to minimize the thickness of the multilevel insulator thus reducing the stress levels shown found both in that insulator and in the corresponding metallic interconnect patterns. The anodic process will allow a very minimal thickness of multilevel insulator because of the integrity of the anodic oxide. Pin holes in the anodic oxide are virtually non-existant since the process by which the oxide is formed is inherently self healing process.

Figure 7 depicts another interesting property of the anodic oxide. This is a photomicrograph of an anodically processed interconnect lead which has been subjected to high temperatures such as found in the packaging of integrated circuits. Note that in the via hole area there is extensive nodular growth found on the surface of the aluminum, but yet on those surfaces of the aluminum stripe which are coated by an anodic oxide there is no nodular growth to be seen. This nodular growth is caused undoubtly by a surface migration phenomenon. The presence of the anodic oxide ties the surface of the aluminum stripe such that the surface migration no longer occurs. These nodular growths can grow to heights which are as thick as the films themselves. In conventional multilevel structures these nodular growths have been known to penetrate the multilevel insulating oxide and cause shorts between levels of interconnect. This failure mechanism is totally eliminated by application of the anodization process.

Another required property of the anodic oxide is to be used in processing of multilevel patterns is that its resistivity be high. The resistivity if the oxide in the plane of the oxide as well as in a direction perpendicular to that plane has been measured. Figure 8 is a tabulation of the data which we have measured giving the resistivity of the oxide in those two directions. The magnitude of this resistivity is such that no problems should be encountered in the fabrication of multilevel interconnect patterns via the anodic process. Another parameter of concern to the design engineer is that of the lost tangent

of the anodic oxide. Figure 9 is a compilation of the lost tangent of the anodic oxide and shows as well the comparative lost tangents of other oxide systems which have been used as the multilevel insulator. It is of interest to note that the lost tangent of the anodic oxide although high is quite frequency independent.

When aluminum is used as an interconnecting metal for multilevel interconnect patterns one must be concerned about the current carrying capability of the metallic stripes. Electromigration is a phenomenon which is more prevelent in aluminum than in many of the other alternative metals which one could use. Just as the presence of the anodic oxide inhibited the nodular growth during thermal treatment it is found that the presence of the anodic oxide on an aluminum stripe under high current stress inhibits the surface migration of the aluminum metal, thus prolonging the mean time to failure. Figure 8 gives mean time to failure data which we have measured at Texas Instruments showing that the presence of the anodic oxide gives approximately a factor of two increase in the mean time to failure. This factor of two allows for relaxation of design rules and/or an increase in the current carrying capability of leads of given cross-sectional area.

## MATERIALS REQUIREMENTS

All aluminum films do not anodize in precisely the same way. That is some of the aluminum films when they are totally converted to the anodic oxide leave behind residual islands. Figures 10-11 show the results of this study. If the aluminum film is a sufficiently small grain size the residual islands are virtually non-existant. Transmission electron microscopy and electron defraction studies were used to determine the grain size and the orientation of the aluminum films. These figures clearly indicate that a randomly orientated fine grain film is the type which is desirable if an anodic process is to be effective. Films with large grains such as those which are deposited in high temperature substrates may well be desirable in terms of carrying capability, but yet if they are to be used in the anodic process

residual aluminum islands are left. It may be argued that these islands are indeed only a cosmetic defect since when circuits are fabricated using such films no circuit parameter is affected. All of the metal films used in this study were deposited via E-beam evaporation from high purity aluminum source materials. At this point little can be said about added impurities in the metal films and their effect on the anodic process.

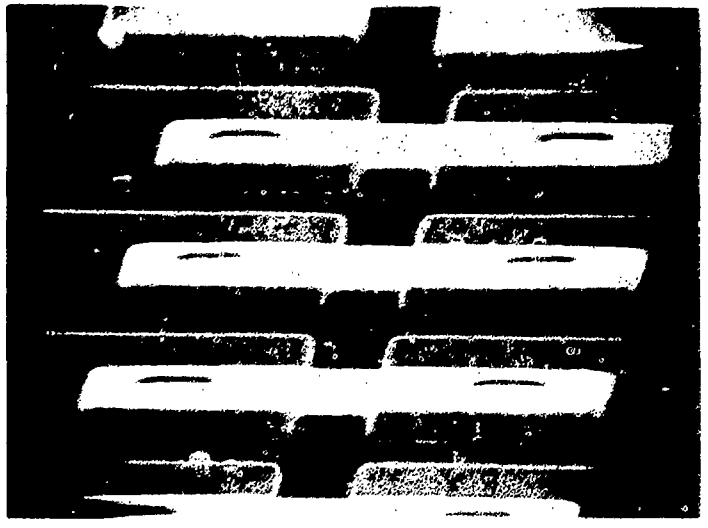
## RELIABILITY

Table 1 is given for the readers evaluation. Of the passivating capability of the anodic oxide it should be noted that this reliability study was directed towards those environments to which the aluminum metal is most subject to failure. Humid conditions under elevated temperatures and mechanical shocks are given emphasis. It is felt that this indicates that circuits which have been anodically fabricated indeed are a very reliable product.

## SUMMARY

A novel method for the fabrication of the multilevel interconnect patterns is presented. In the process all etching steps of either metal or oxides are eleminated. The topological difficulties introduced by multilevel processing by conventional methods are removed as a source of concern. The processes used in this method are extremely simple and self limiting thus lending themselves to ease of manufacture and automation. The resultant product is both chemically and mechanically reliable.

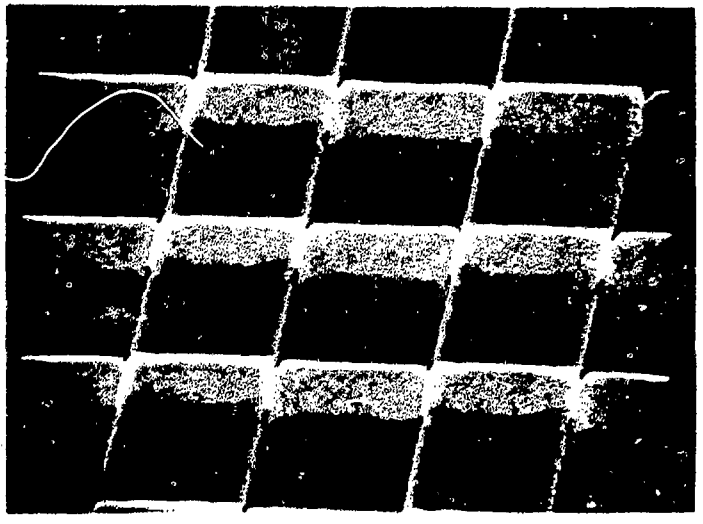
This work was sponsored in part by a contract awarded Texas Instruments Incorporated by Naval Air Systems Command.



STANDARD

CONVENTIONAL

PROCESS



FEED THRUS

CROSSOVERS

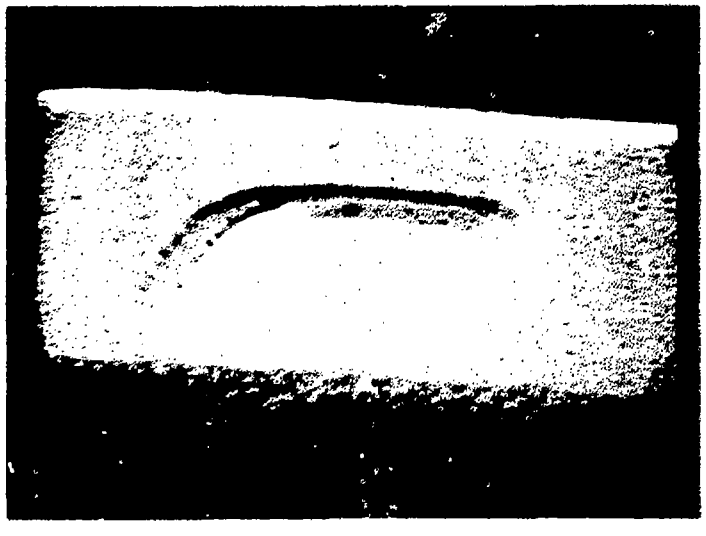
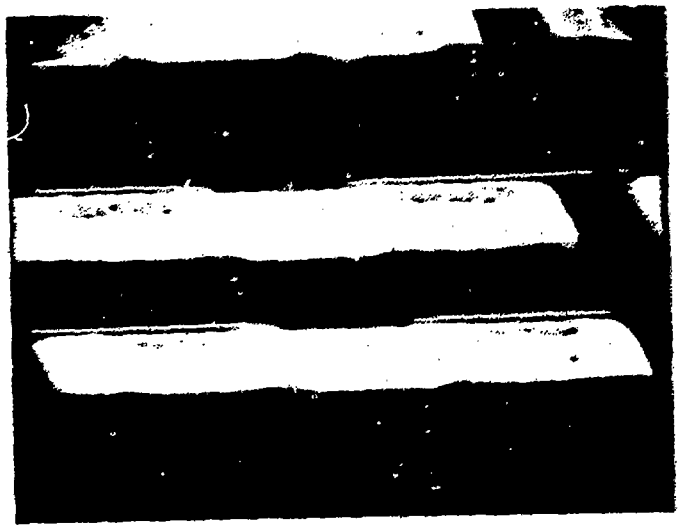


Figure 1



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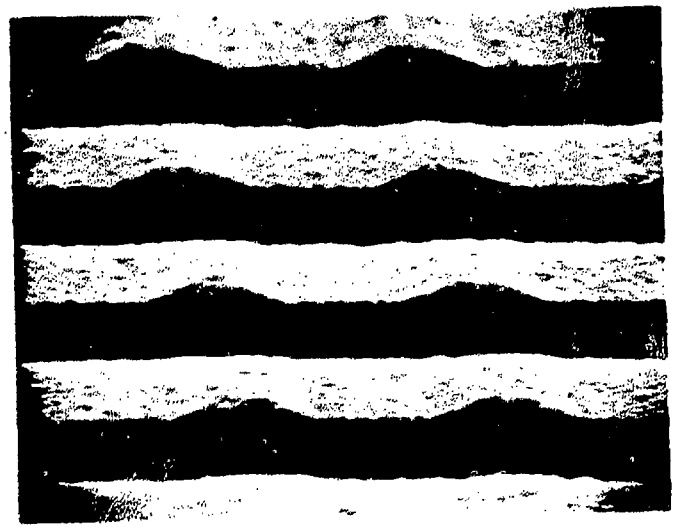
OPTIMUM

CONVENTIONAL

PROCESS



CROSSOVERS

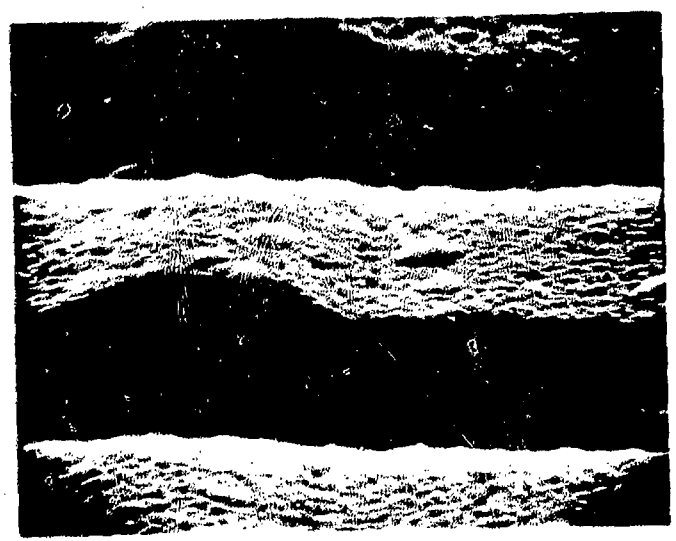
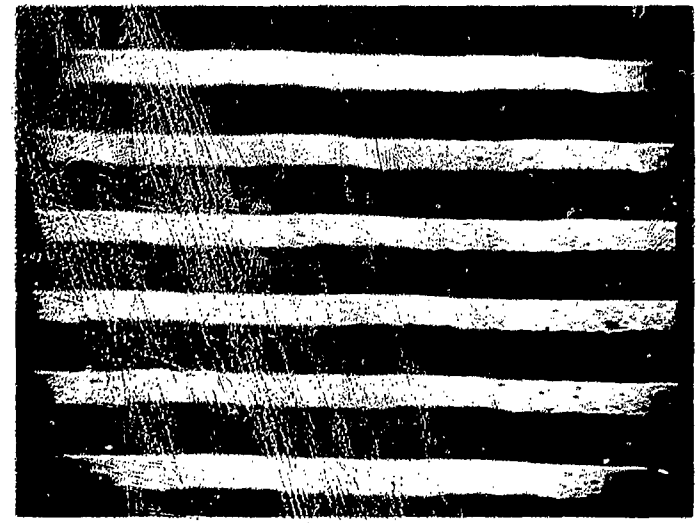


Figure 2

PRODIC

INLAID

PROCESS



FEED THRUS

CROSS OVERS

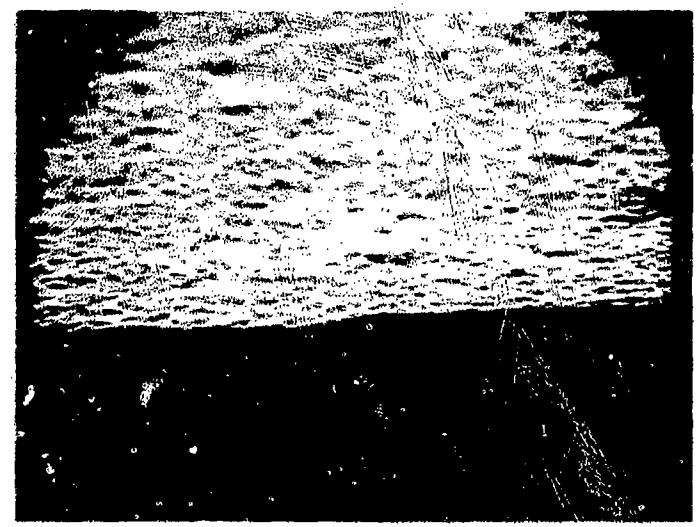


Figure 3

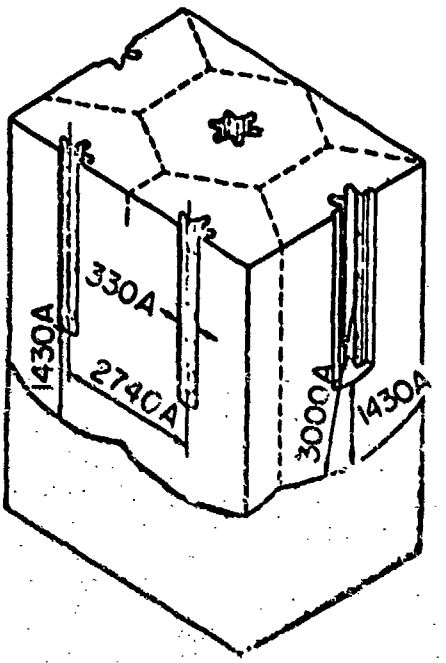



Figure 4 Representative Anodic Oxide Structure

From: Keller, Hunter and Robinson, J. Electrochem. Soc. 100 411-419 (1953).

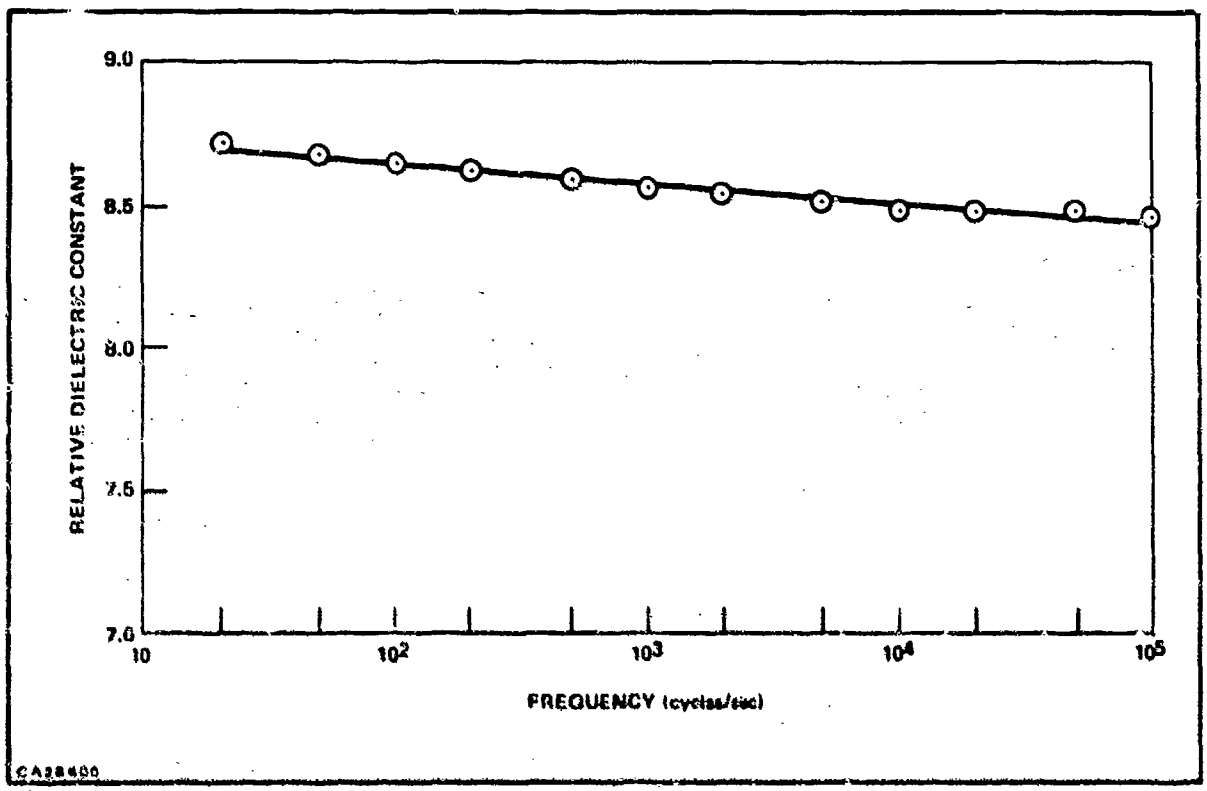

9.0
8.5
8.0
7.5
7.0
RELATIVE DIELECTRIC CONSTANT
10
$10^2$
$10^3$
$10^4$
$10^5$
FREQUENCY (cycles/sec)
CA28400

Figure 6

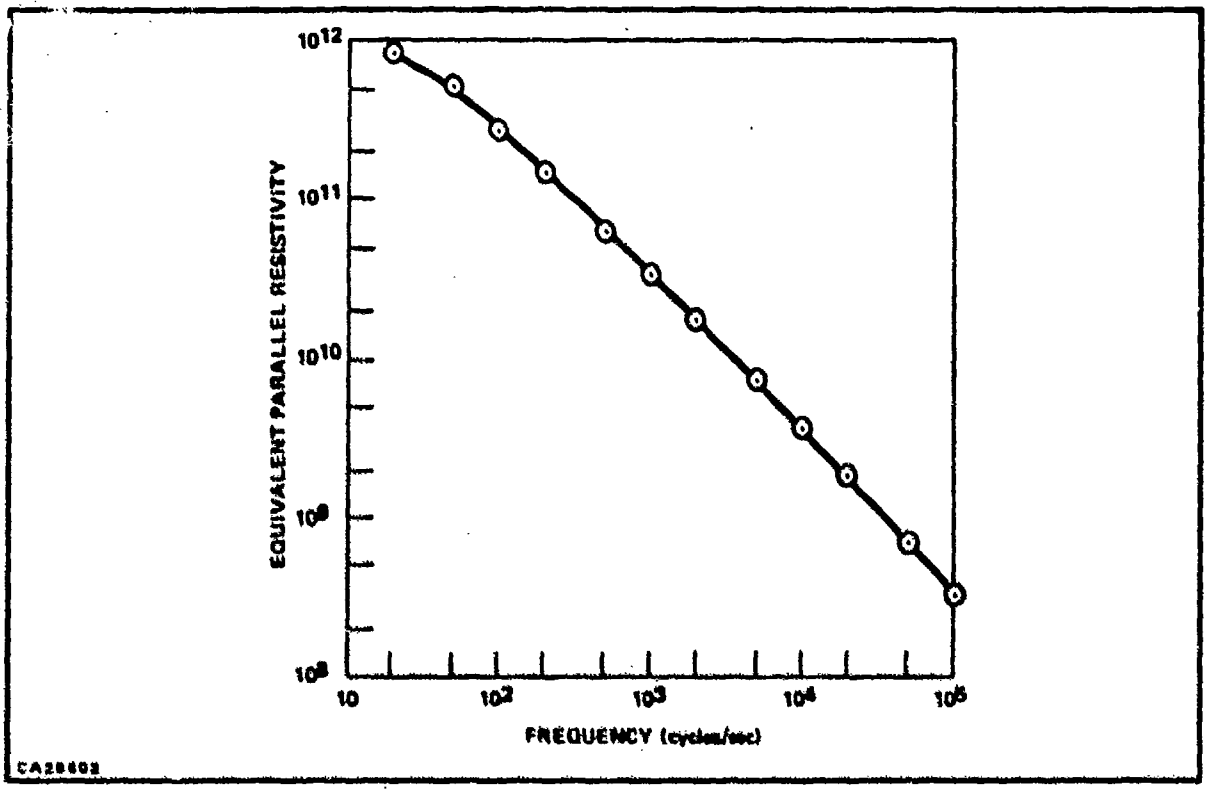

EQUIVALENT PARALLEL RESISTIVITY
$10^{12}$
$10^{11}$
$10^{10}$
$10^{9}$
$10^{8}$
10
$10^{2}$
$10^{3}$
$10^{4}$
$10^{5}$
FREQUENCY (cycles/sec)

Figure 8

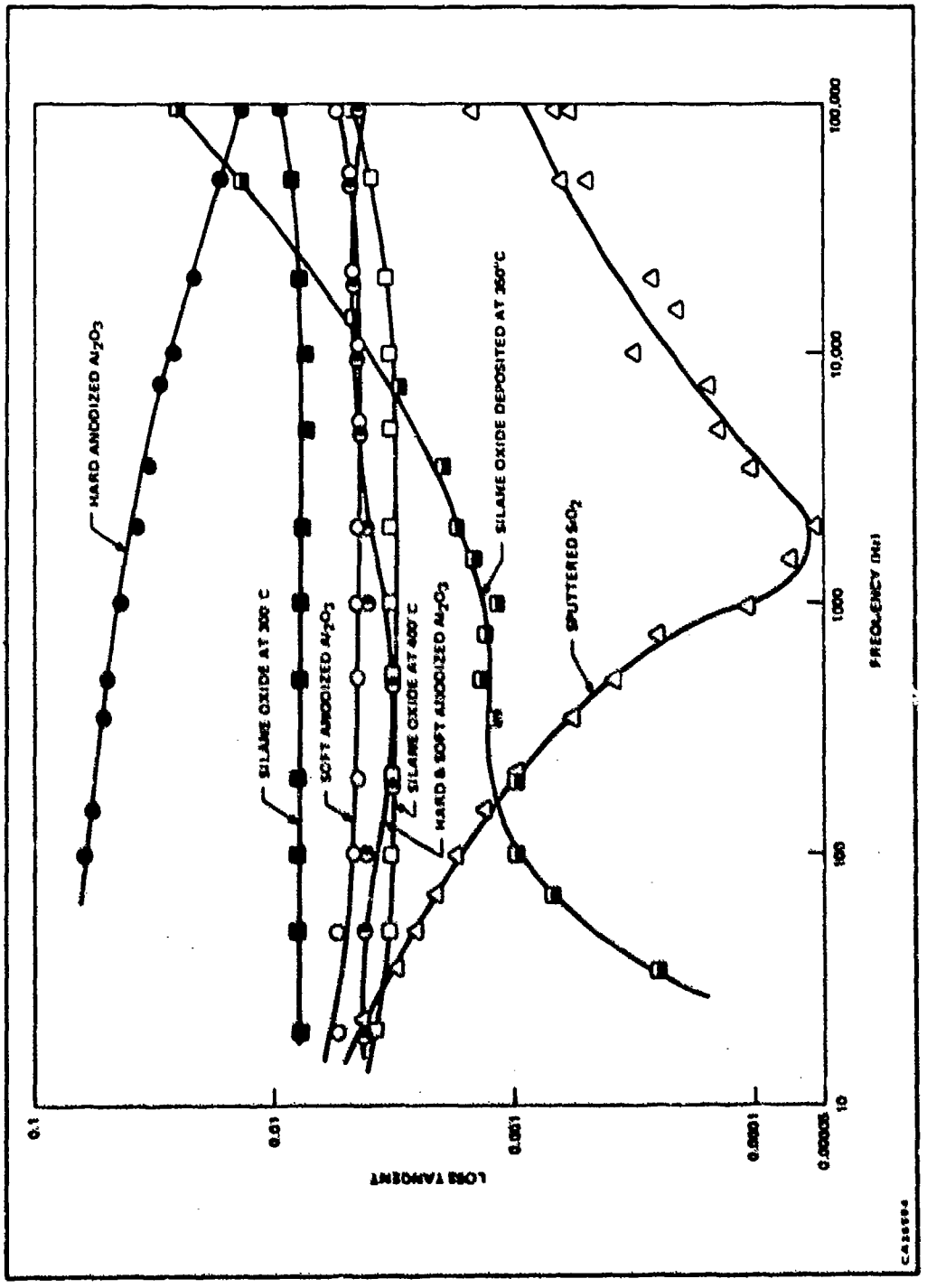
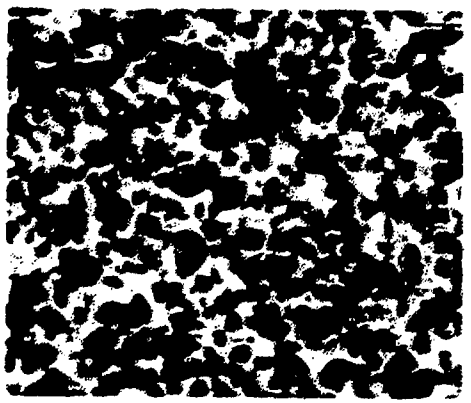
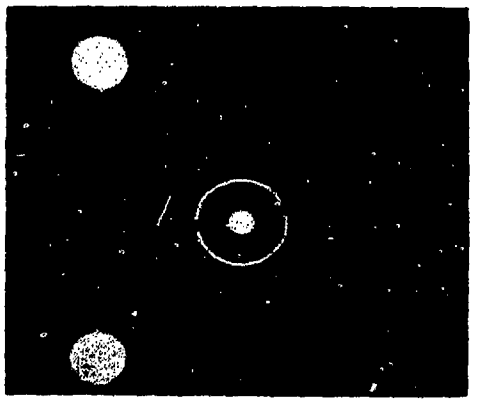

HARD ANODIZED $Al_2O_3$
SILANE OXIDE AT 300°C
SOFT ANODIZED $Al_2O_3$
SILANE OXIDE AT 400°C
HARD & SOFT ANODIZED $Al_2O_3$
SILANE OXIDE DEPOSITED AT 350°C
SPUTTERED $SiO_2$
LOSS TANGENT
FREQUENCY (Hz)
0.1
0.01
0.001
0.0001
0.00005
10
100
1000
10,000
100,000

Figure 10



TRANSMISSION ELECTRON MICROGRAPH
9450 X



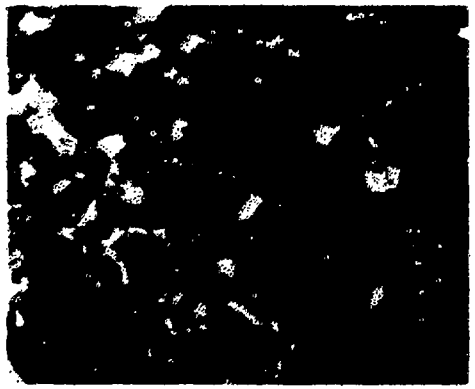
ANODIZED PATTERN
50 X

DIFFRACTION PATTERN

OVERALL VIEW OF THE ANODIZED FILM
AFTER KMER BAKE. 400 X

CA26586

Figure 11 Results of Anodization of Small-Grain Aluminum



TRANSMISSION ELECTRON MICROGRAPH
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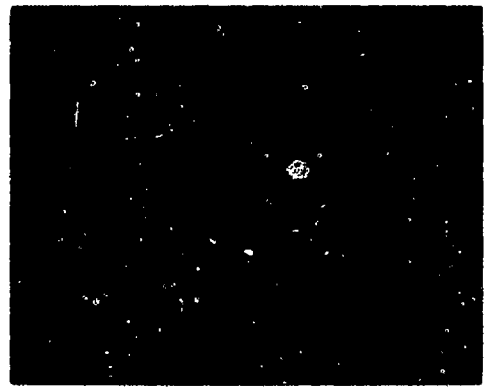
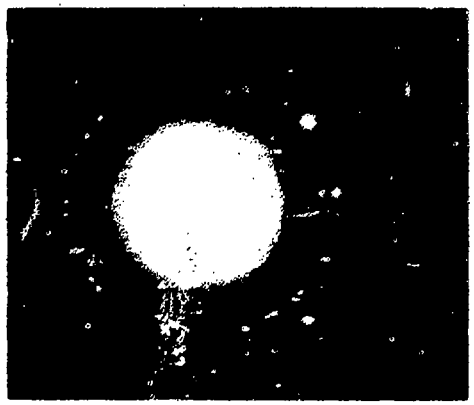
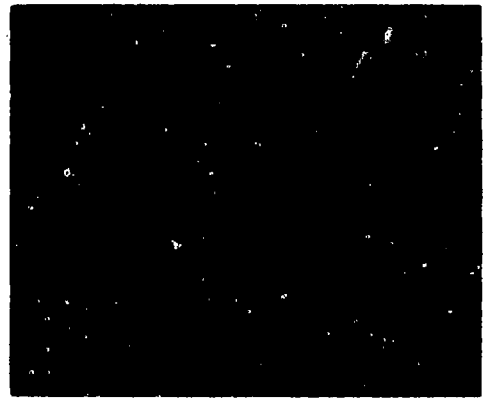


ANODIZED PATTERN
50 X



DIFFRACTION PATTERN



OVERALL VIEW OF THE ANODIZED FILM
AFTER KMER BAKE. 400 X

CA26591

Figure 12 Results of Anodization of Large-Grain Aluminum

## Table 1. Reliability Data

| Test | Hrs. | Results |
|---|---|---|
| 125°C Operational | 168 | 45/0 |
| | 336 | 45/0 |
| | 500 | 45/0 |
| | 1000 | 45/0 |
| | 2000 | 45/0 |
| 85°C/85% RH | 168 | 20/0 |
| | 500 | 20/0 |
| | 1000 | 20/1 |
| Pressure Cooker | 8 | 50/0 |
| | 16 | 50/0 |
| | 24 | 50/0 |
| | 32 | 50/0 |
| | 40 | 50/5 |
| | 48 | 45/6 |
| | 56 | 39/3 |
| Boil-In | 72 | 20/0 |
| | 96 | 20/0 |
| | 120 | 20/0 |
| | 144 | 20/0 |
| Extended Temp Cycle −65 + 150 | 50 Cyc | 48/0 |
| 85°C/85% RH Open Flat Pack | 500 | 25/0 |