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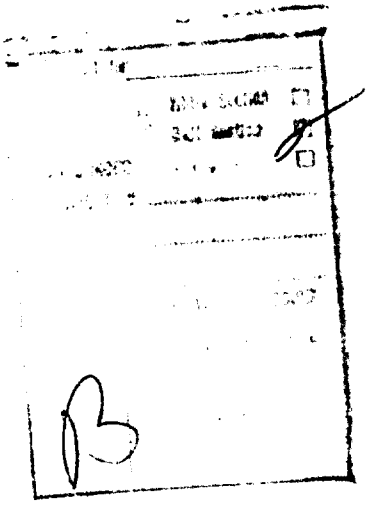
High-Speed Optical Data Link for Interconnection Between LSI Modules

Final Report

(March 1972 – March 1973)



High-Speed Optical Data Link

for Interconnection Between LSI Modules

Final Report

(March 1972 through March 1973)

April 1973

by

A.D. Damari
H.H. Bloem
D.J. Stigliani, Jr.
R.C. Clapper
H.C. Farrell

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Department of the Navy
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by

IBM, Federal Systems Division
ESC
Owego, New York

FOREWORD

This technical paper on a High-Speed Optical Data Link System, to provide intercommunication between LSI modules, describes and examines various packaging concepts and examines various elements of the system such as sources, detectors, optical transmission media, and optical interfaces. It concludes with a hardware section that describes the fabrication and operation of a five-module, 20-MHz functional model. The work was performed for the Naval Air Systems Command, under contract number N00019-72-C-0301, Mr. A.S. Glista, by the IBM Electronics Systems Center, Owego, New York during the period from March 1972 to March 1973.

Publication of this report does not constitute approval by the Naval Air Systems Command of the findings or conclusions contained herein. It is published for the exchange and stimulation of ideas.

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Al_2O_3	Alumina
B	Source Irradiance
ECL	Emitter Coupled Logic
GaAs	Gallium Arsenide
GaAlAs	Gallium Aluminum Arsenide
IR	Infrared
LED	Light-Emitting Diode
LID	Leadless Inverted Device
LOC	Large Optical Cavity
MBs	Megabits per Second
MHz	Megahertz
n	Refractive Index
pF	Picofarad
PD	Photodiode
PIN	P doped - Intrinsic - N doped
RC	Resistor-Capacitor
SH	Single Heterostructure
SNR	Signal-to-Noise Ratio
TTL	Transistor-Transistor Logic
U/S	Ultrasonic Bond
μm	Micrometer

Section 1

INTRODUCTION

This document is the final technical report for the Phase II High-Speed Optical Data Link, Contract No. N0019-72-C-0301. The program was performed for the Naval Air Systems Command by IBM; Federal Systems Division, Electronics Systems Center, Owego, N.Y. The intent of the task was to investigate and conduct a feasible conceptual design study of a complete high-speed optical data link system to provide intercommunication between large scale integrated (LSI) modules as typically proposed in the Navy Advanced Airborne Digital Computer (AADC) development program. The task culminated with the development and fabrication of a functional five-module model. Contractual effort covered a 12-month period beginning 2 March 1972.

1.1 PERFORMANCE DEFINITION

The performance of this research and development effort was divided into four subtasks. Subtask 1 involved an updated survey of appropriate devices and investigation of laser and PIN diodes for applicability to the data link. Section 2 of this report explains this effort and gives the results. Subtask 2 encompassed a study of all levels of packaging, from the basic device up to the module and final unit level. This study was configured around the basic unit and module design as proposed for the Naval Air Systems Command per Contract No. N00019-70-C-0504 dated 3 December 1971. Sections 3 and 4 describe this effort.

Subtask 3 contained in Section 5 of this report describes the basic philosophy and design details associated with the hardware phase of this program. This included the design and build of a state-of-the-art, solid state five-channel operating model capable of performing eight-bit parallel to serial and serial to parallel transformation along single and duplex data links. The fourth and final subtask was the analysis, summarization and documentation of all pertinent information and data accrued as a result of this effort and compiled in this report in Section 6.

1.2 SIGNIFICANT RESULTS AND CONCLUSIONS

Some of the more significant developments attained as a result of this contractual effort are as follows:

1) Established a feasible optical/mechanical systems approach
2) Developed an extremely efficient and compatible optical/mechanical/electrical configuration that virtually eliminates the need for avalanche detectors
3) Concluded from an on-wafer/off-wafer module configuration trade-off study that the off-wafer approach is the most feasible, efficient, and cost effective approach in the existing and near-future time frame depending upon data rate required
4) Successfully completed the fabrication of a fully functional 20-MHz prototype high-speed optical data link model. The model simulates a five module (LSI type) computer employing optical intercommunication between operating modules
5) Determined that heterojunction light-emitting diodes (LEDs) can produce faster risetimes than ordinary LED structures.
6) Concluded that improvements in LEDs and F/O cables are desirable particularly if high data rates are required.

Section 2

DEVICE INVESTIGATION

2.1 LIGHT SOURCE/DETECTOR CONSIDERATIONS

In attempting to establish optimum optical devices to be used in the Advanced Airborne Digital Computer (AADC), it is necessary to consider two primary paramaters;

1) Speed of operation (bandwidth)

2) Efficiency of signal transfer.

The bandwidth of the optical interconnection system is determined by the electro-optic devices used and, in particular, is limited by the light-emitting diode[1]. As was shown in Phase I of this study, the photodiodes can meet the projected data rates of ~200 megabits per second (MBs) for the AADC, whereas, commercially available LEDs today have a data capability of ~40 MBs. This by no means represents a limit of the LED, as special devices have been fabricated that operate considerably higher than 40 MBs. Both LEDs and photodiodes (PDs) will be discussed in more detail in Subsections 2.2 and 2.3, respectively.

The efficiency of signal transfer from the light-emitting diode to the photodiode is determined by the conversion efficiency of both devices and the optical losses associated with the optical channel. The conversion efficiencies of state of the art LEDs (~ 3%) and PDs (~ 70%) are well established, and sizable improvements will not materialize unless new materials or radically different device structures are developed. The maximum efficiency benefit would result from an improved LED. The light transfer efficiency, however, is a direct function of the AADC interconnection configuration, as well as the optical packaging of the individual devices. Figure 2-1 illustrates the optical flux received at a detector from an uncollimated LED (Lambertian source) as a function of separation distance. The flux at the detector is calculated using physical optics (refer to Subsection 4.2, Equation 4-11)

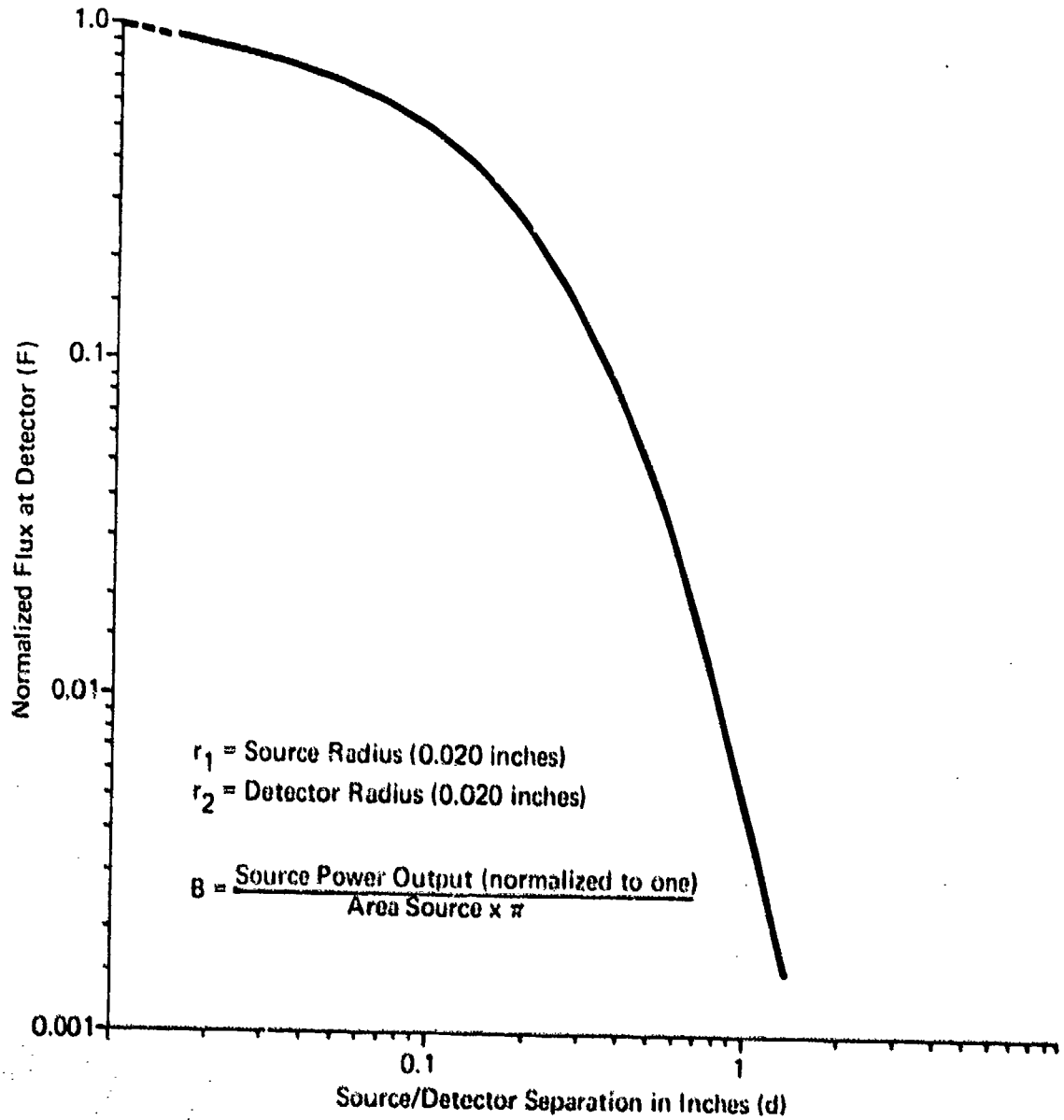


Figure 2-1. Optical Flux at Detector from Lambertian Source LED as a Function of Separation

and indicates that light coupling efficiency decreases rapidly with separation distance. For a source/detector separation of 0.5 inch (typical AADC module separation), only 4.5% of the light is incident upon the detector. Such large losses would necessitate very high gain receivers and/or avalanche photodiodes. The source/detector coupling efficiency can be improved considerably by using fiber optics to channel the light from the LED to the photodiode. Further improvement in efficiency can be realized by employing reflectors, lenses, index matching epoxy coatings, etc. These techniques and others are considered and utilized in Section 3 for the AADC optical interconnection configuration.

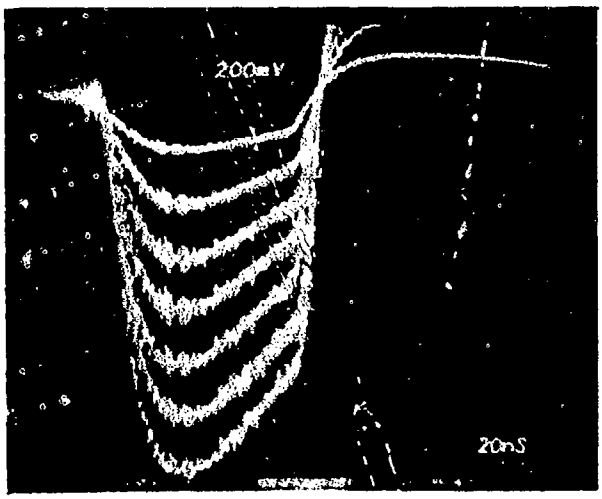
2.2 EVALUATION OF EXISTING LIGHT EMITTERS

The light source used in the AADC data link should incorporate some optical enhancement techniques to provide higher optical power output levels. This light source should be the same physical size or enhanced to have the same physical aperture as does the light transmission medium to provide adequate coupling to the transmission medium and be spectrally matched with the receiver detector to minimize amplifier requirements at the receiver. It is also suggested that current drive for this diode be increased to the thermal limits of the package, which is undefined. Evaluation of spontaneous emitting diode structures shows that all these requirements can be filled; however, in PN junction LED structures there is a speed versus light power output tradeoff involved. Investigations were performed on existing light emitter structures presently used for laser diodes to address this speed limitation found in PN junction LEDs.

2.2.1 EVALUATION OF LED STRUCTURES

The diodes tested were: IBM GaAlAs diode 15- by 15-mil chip, 4 mil thick. The chip was center contacted and mounted on a T046 Header and coated with epoxy. Texas Instruments' GaAs TIL09 Domed Flip Chip on a silicon substrate mounted on a T046 Header with no epoxy coating.

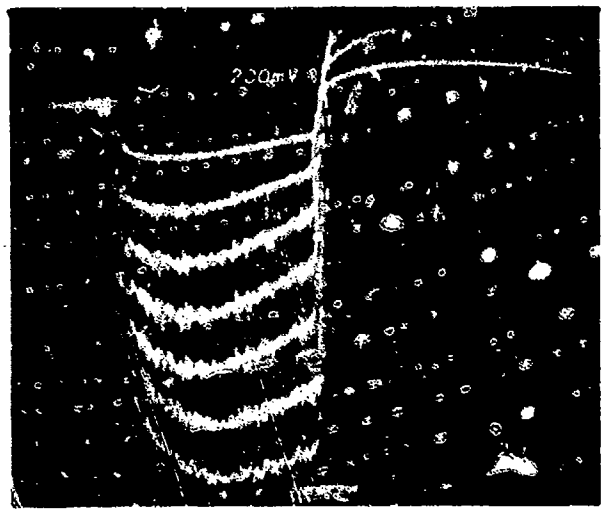
The IBM diode was slow with 28 ns risetime with no improvement in risetime with changes of current from 3 A to 20 A. (See Figure 2-2)



Drive Currents Equal:
3.25 A
5.75 A
8.50 A
10.75 A
13.50 A
16.00 A
19.25 A

Figure 2-2. Light Pulse Output of IBM GaAlAs LED

The Texas Instruments' TIL09 diode had a risetime of 5 ns from pulse start to midpoint and 30 ns from midpoint to pulse peak. No improvement in risetime was noted from 5 A to 20 A. (See Figure 2-3.)



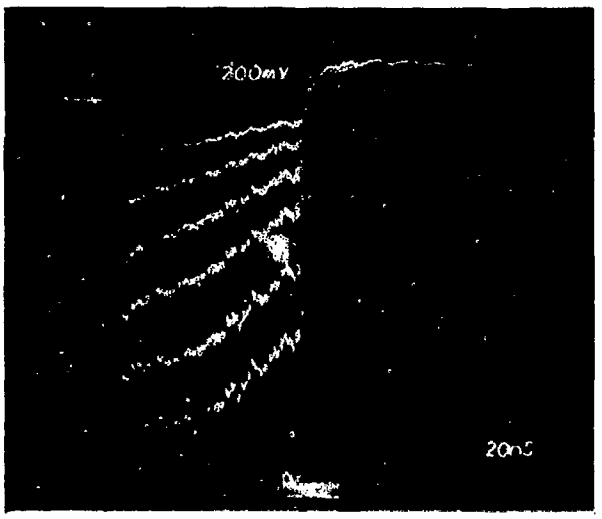
Drive Currents Equal:
2.50 A
5.00 A
8.00 A
10.75 A
13.50 A
16.50 A
19.50 A

Figure 2-3. Light Pulse Output of Texas Instruments TIL09 LED

2.2.2 EVALUATION OF LASER STRUCTURES

Laser diodes were tested in a nonlasing (spontaneous emission) mode by altering the metallurgy of the diode chip itself. The diodes tested were single heterojunction (SH) laser diode 4- by 12-mil chips which were center contacted like the IBM LED and mounted on a T046 Header with no epoxy coating. The light output was measured on the axis of normal stimulated emission output.

Fast start (5 ns) continues fast at high current density to peak in 6 ns. Rise-time is a function of current density showing a variation from 12 ns at low levels to 6 ns at high levels. (See Figure 2-4)



Drive Currents Equal:
5.00 A
7.25 A
9.25 A
11.25 A
13.75 A
16.50 A
19.50 A

Figure 2-4. Light Pulse Output of IBM SH Laser Structure Diode as LED

IBM large optical cavity (LOC) structure laser diodes in a laser diode configuration were monitored at the threshold point to observe risetime at this point. The transition point between spontaneous and stimulated emission shows that until the transition from spontaneous emission the risetime follows the trend seen in LEDs. After threshold, typical laser risetimes are noted. (See Figure 2-5)

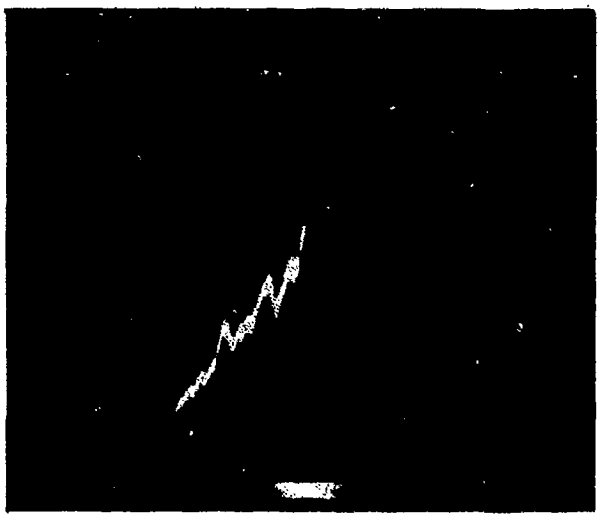
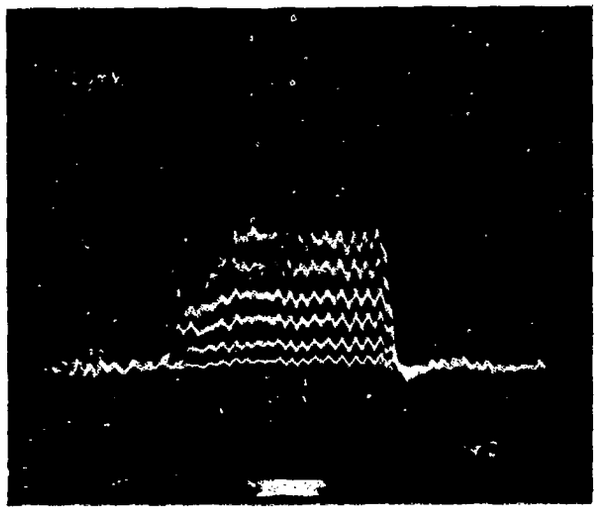


Figure 2-5. Light Pulse Output of IBM LOC Structure Laser L-21-10 with Drive Current Near Threshold

In the lasing mode, the LOC laser had a risetime of less than 2 ns and a fall time of less than 2 ns. Risetime is a function of current density with a variation from 2 ns at low levels to 1 ns at high levels. (See Figure 2-6)



Drive Currents Equal:
10 A
9 A
8 A
7 A
6 A
5 A

Figure 2-6. Light Pulse Output of IBM LOC Structure Laser L-21-10 with Drive Currents of 10 A, 9 A, 8 A, 7 A, 6 A, and 5 A

Observations made using an avalanche detector and a high-gain amplifier to observe threshold show that the stimulated emission pulse at threshold is always narrower than the spontaneous emission pulse. As the current density is increased, the risetime of the spontaneous emission will improve, the stimulated pulse will widen, and the risetime of the stimulated pulse will improve.

Typical risetimes of laser pulses from LOC structure laser diodes are less than 2 ns. Figure 2-7 is a typical example of stimulated emission pulse risetime. It should again be noted that the true risetime can be even faster than is shown, since this measurement is at the limits of the test equipment used in these evaluations.

2.2.3 EVALUATION TEST EQUIPMENT

The following test equipment was used in collecting data:

1) Pulse Driver - Hugging Laboratories Nanosecond Pulser, 961S
2) Photo Detector - ITT Biplanar Photodiode F-4000, F4502 Holder
3) Photo Detector - TI Avalanche Photodiode TIXL55

4) Wideband Amplifier - Avantek UTA-219M

5) Oscilloscope - Tektronix 7904, Vert 7A19, Horiz 7B92, Probe P6056.

The pulse driver produced either 26 ns or 80 ns pulses with risetimes of 0.5 ns and falltimes of 0.8 ns. The biplanar photodiode had specified risetime of 0.5 ns and falltime of 0.8 ns. The avalanche photodetector had a specified gain bandwidth product of 80 GHz measured at 1 GHz. The wideband amplifier has 42 dB gain from 5 MHz to 1000 MHz. The oscilloscope has a 1.2-ns risetime. This equipment was totally sufficient when used to measure LED light pulse characteristics, however, laser light pulse risetimes easily achieved the risetime capabilities of this test system. It should be made clear that measured laser pulse risetimes of 1.2 ns may be accuracy limited by the test equipment used and could be faster than the measurements indicate.

Figure 2-7. Light Pulse Output of IBM LOC Structure Laser L-21-10 Showing Stable Risetime of Stimulated Emission Pulse

2.2.4 SUMMARY OF LIGHT EMITTER EVALUATION

It appears that diode structures of the types used for laser operation produce faster risetimes than ordinary LED diode structures in the spontaneous emission modes. It also appears that risetime does not improve with increases in current density in ordinary LED structures but does improve with increases in current in laser structures.

Laser structures seem to have a period of spontaneous emission preceding the stimulated emission which varies with current density and quality of the junction and cavity. The risetime of stimulated emission pulses also seems to improve with current density.

From the data presented in this subsection, very short risetime LEDs can be fabricated for use in high data rate communication systems. Further material and device development is needed to make these heterojunction LEDs usable for the AADC.

2.3 EVALUATION OF PIN DIODE APPLICABILITY TO DATA LINK

The choice of the detector used in the AADC is not strictly that of selecting the most sensitive detector available. This device must be compatible with the light emitter, the selected transmission line, and have amplifier requirements suitable for use in a digital computer environment. Although it is not essential, it would be preferred if the detector used voltages normally found in a digital computer.

The characteristics of the light-emitting diode chosen will, therefore, fix many of the requirements of the detector. The spectral response, sensitivity, switching speed, and the detector signal amplification requirements are mainly determined by the LED. The microstrip circuit lines in the AADC will not significantly affect the detector since they are short in length and their physical size is controlled mainly by the LED; however, coupling losses due to interconnections in these lines will be a factor in detector sensitivity and/or amplifier gain requirements. To realize the detector speed requirements, the detector load must have a value in the range of 50 ohms, and the amplifier requirements will be controlled by the thermal noise generated by this resistor which in turn will reflect a minimum sensitivity requirement for the detector.

2.3.1 PIN DIODE SPECTRAL RESPONSE

The PIN diode spectral response closely matches the region in which the most efficient GaAs and GaAlAs LEDs are achieved. The response remains relatively constant with variations in reverse bias conditions and in special cases has been

made flat within less than 10% over the entire region covered by the previously mentioned LEDs. The spectral response also remains constant with modulating frequency, where the avalanche photodetector shows evidence of a shift in spectral response toward the red or less efficient area of state-of-the-art LEDs at the required higher frequencies.

2.3.2 PIN DIODE SPECTRAL SENSITIVITY

The sensitivity requirements set forth by the AADC application can be filled utilizing the PIN photodiode. The sensitivity that has been achieved is in the area of 0.3 A/W to 0.5 A/W as compared to 0.15 A/W for avalanche detectors. The manufacture of PIN structures with these sensitivities and with appropriate areas is commonplace in industry. Although avalanche detectors have the definite advantage of gain internal to the device to supplement lower spectral sensitivity, they also are small in area and not as compatible in this aspect as the PIN devices.

2.3.3 PIN DIODE RISETIME CAPABILITY

The LED, projected for use in the AADC, set the reasonable speed limit at about 200 MHz maximum. With this in mind, it can be shown from manufacturer's data that the PIN device will effectively fill the need. More conservative companies specify risetimes of PIN diodes in the area required between 2 ns to 4 ns while more optimistic companies choose to state 0.5 to 1.0 ns.

Since the load resistor used in conjunction with the detector must be considered due to the junction capacitance of detectors, it is also important to point out that PIN configurations generally have capacitances in the order of 2 pF to 10 pF. Small area avalanche detectors also have capacitances in this range, but larger area devices have much higher capacitance. This capacitance is an important point to consider since the R-C time constant of the diode junction and load resistor is a limiting factor of speed.

2.3.4 SUMMARY OF PIN DIODE APPLICABILITY

State-of-the-art PIN diodes do exist that will fill the requirements of spectral response, spectral sensitivity, and risetime. The devices are compatible with the

load resistor requirements and should provide signal outputs appropriate to amplifier requirements suitable for use in a digital computer environment. These devices also have the added advantage of not requiring a well regulated high voltage bias supply as does the avalanche photodiode.

2.4 DUPLEX DATA TRANSFER VIA ONE OPTICAL PATH

The use of optical communication allows the implementation of a multiplexing technique, wavelength division multiplexing, which can decrease the number of optical data paths required for signals. Wavelength division multiplexing involves the transmittal of data using light of different wavelengths. The various wavelengths are generated by different LEDs and are sorted out at the receiver by photodetectors tuned to the various wavelengths. The number of channels is primarily a function of the number of wavelengths available, LED and PD spectral widths, and the ability to optically couple the individual wavelengths into the fiber.

A $Ga_{1-x}Al_xAs$ diode used as a PD detector has a photo response versus wavelength of incident light distribution which is similar to the LED spectral distribution as shown in Figure 2-8. This effect is due to the optical properties of a material with a graded band gap. When light having the same spectral distribution as that emitted by the p-n junction enters the device from the high-band gap surface, it is strongly absorbed at the junction, generating hole-electron pairs which create a photovoltage. Light with a spectral distribution and peak energy other than that produced by the junction in electro-luminescence is absorbed away from the junction where the Al concentration and band gap are higher. Thus, using the graded band gap structure an identical pair of diodes can be used to transmit and receive information without interference from another pair having a different peak emission and detection energy. The emission spectrum of the LED and the detection spectrum of the same diode, while overlapping considerably, do not coincide exactly. This mismatch is caused by the heating of the p-n junction in the forward bias mode. Since the devices have a typical power efficiency of ~3%, most of the electrical power into the LED is converted into heat. It has been experimentally determined that the peak wavelength of the diode shifts at the rate of 1.3 Å per °C.

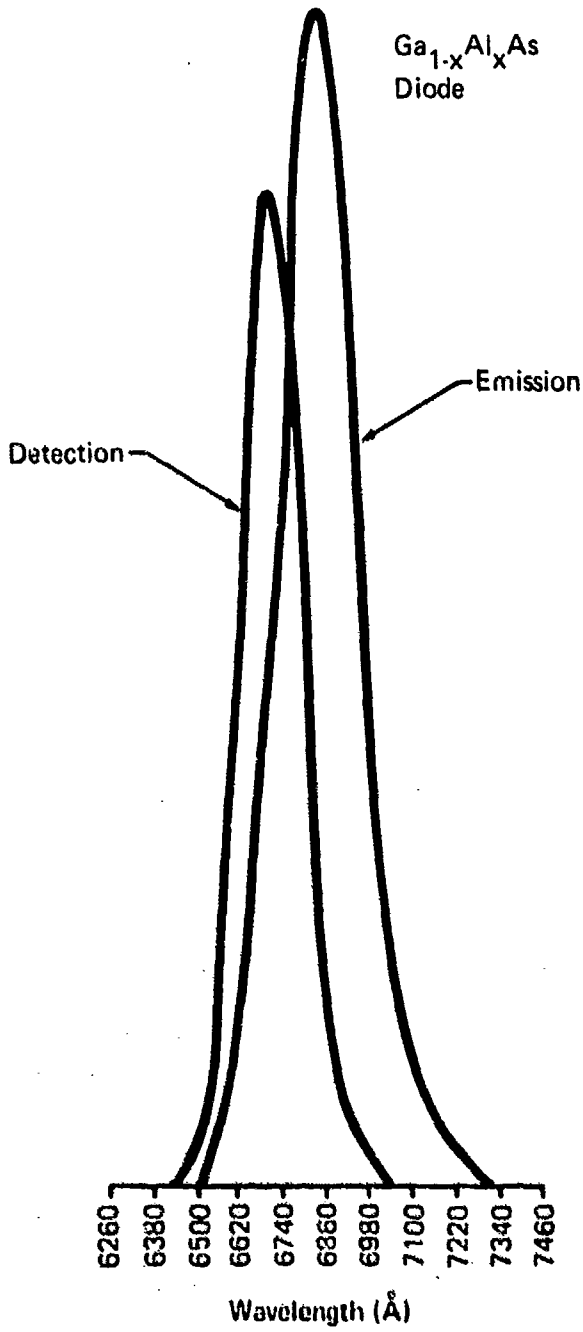


Figure 2-8. Emission and Detection Spectral Distribution for a $Ga_{1-x}Al_xAs$ Diode

This value is in good agreement with the linear variation of the band gap energy of semiconductors. It is expected that this effect is the same for both the emitter and detector diode.

Wavelength division multiplexing has been considered for the AADC module-to-module interconnection but cannot be used because of the high data rates required. GaAlAs diodes have not been optimized for photodetection operation and, consequently, have high capacitance. This capacitance limits the data rate speed to less than 2 MBs. It is anticipated, however, that some device development work in fabricating the diode for photodetection will considerably improve the data rate capability. This approach can be considered for the next generation optical interconnection technique.

Section 3

OPTICAL DEVICE PACKAGING AND INTERCONNECTION CONCEPTS

There are several possible ways of configuring the LSI module in the AADC in both the first and second level of packaging to accommodate optical interconnection. However, the apparent multiplicity of choices narrows down considerably when factors such as optical efficiency, power, power density, optical coupling losses, system cost effectiveness, and development costs as related to utilization of near and existing state-of-the-art techniques are considered.

Many of the optical interconnection configurations as presented in the previous report[1], although theoretically feasible, required either extensive reconfiguring of the AADC module and higher level packaging concepts as proposed, or necessitated utilization of repeaters, power splitters, special windows, etc. Therefore, it was decided that a system that was as closely compatible with the existing AADC packaging configuration as possible, and utilized state-of-the-art and near state-of-the-art design and fabrication concepts, was the most desirable.

3.1 OPTICAL INTERCONNECTION SYSTEM CONFIGURATION

A system that does have this potential and also appears to be the most efficient, and cost effective, is a simplex, one receiver for one transmitter, multiplexed serial data transmission system.

A simplified illustration of this approach is shown in Figure 3-1. This concept places both the source and the detector devices on a module with light transmission directed along the face of the module via a light pipe system out to the vertical edges of the module. From this point it passes across a small fixed air-gap to a fiber optic receptor housed in the unit side panels located along each side of the modules. This receptor directs the signal to the appropriate receiver in a preselected module. Hence, the side panels can be programmed with a matrix of

light guides to interconnect any series of modules desired. In an optimized system the use of a heterostructure LED in place of separate receive and transmit diodes in the modules would allow complete intercommunication flexibility between modules.

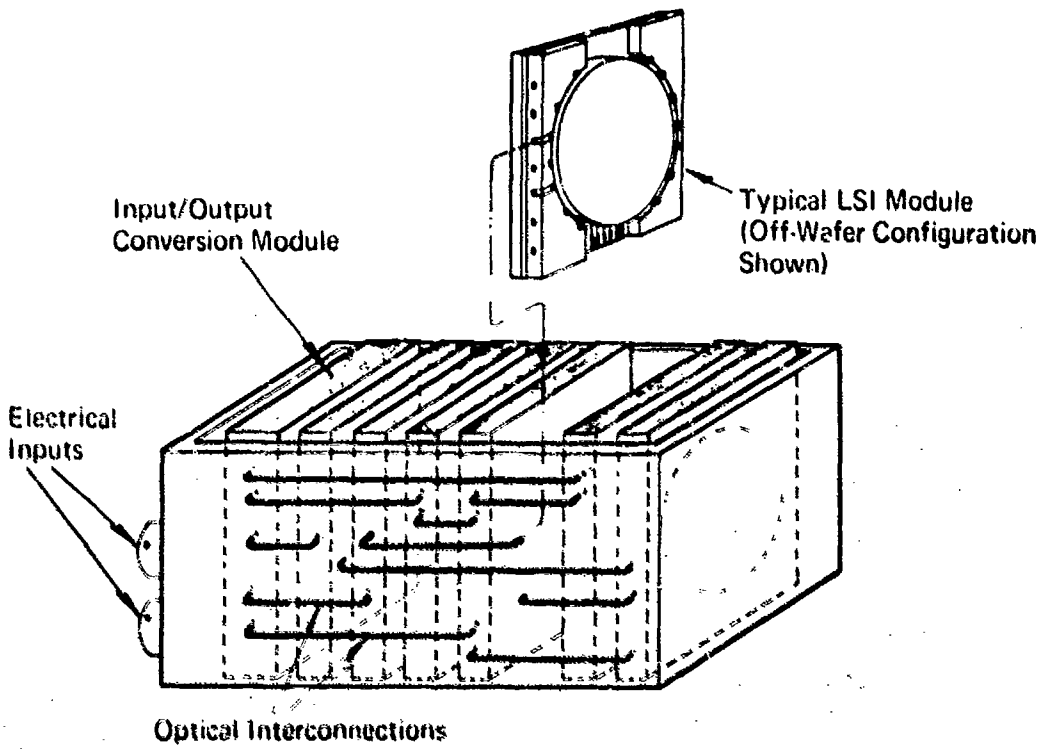


Figure 3-1. AADC Module Optical Interconnection Concept

At least one module in a machine, which we will refer to as a "conversion module," would be utilized to convert all input and output signals from electrical to optical data and vice versa. This module obviously should be located adjacent to the I/O connector end of the unit. A bottom panel or printed circuit (PCB) distribution panel would be located across the bottom of the modules for the purpose of carrying power and ground to each module via plug-in electrical connectors. Since there will generally be no more than six to eight contacts required for this function, the insertion and withdrawal forces normally associated with electrical interconnections is significantly minimized. The power connector may either be one-piece, located in the center of the module, or two smaller connectors positioned at either edge of the module. The latter configuration does not interfere

with the existing proposed location for the module inlet cooling air plenum. Figure 3-2 illustrates the possible power contact locations.

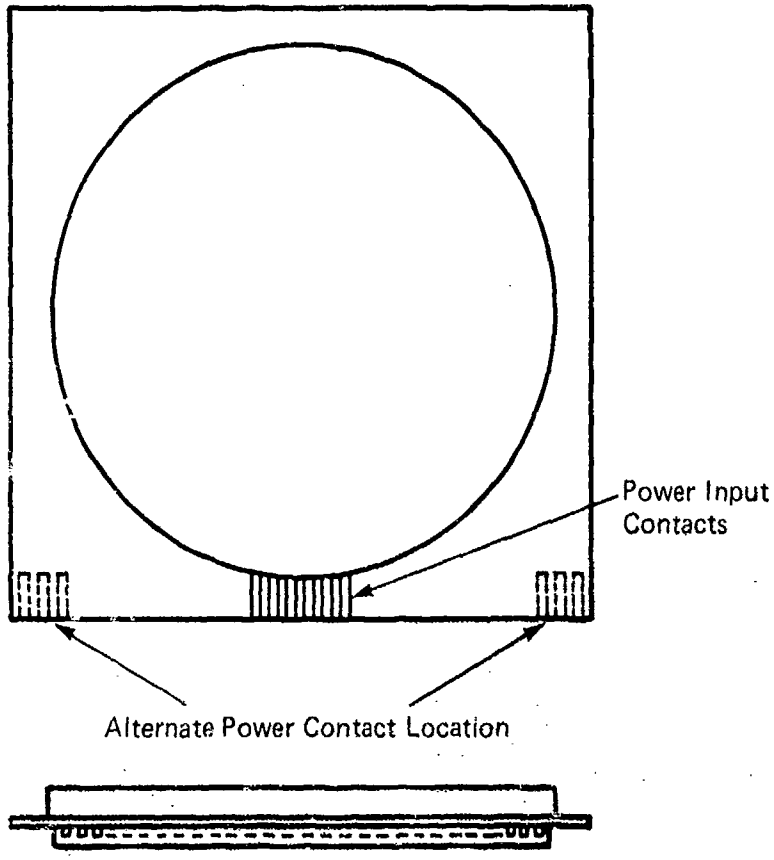


Figure 3-2. Module Power Contact Location

With the groundrule of one transmitter for one receiver, two possible configurations for the location of the transmitter and receiver diodes within the module become evident.

3.1.1 ON-WAFER CONFIGURATION

The first and probably most apparent concept is referred to as the "on-wafer" approach. This concept places the LED, together with its associated drive circuits, directly onto the silicon wafer. Here TTL or ECL circuits can be generated directly onto an epitaxial silicon wafer surface with the LED in leadless inverted device (LID) form attached to the wafer using appropriate hybrid bonding techniques. Four possible configurations to this approach are examined. In each case the LED

is attached to the periphery of the wafer such that its light output emerges in a plane normal to the wafer, passes partially through the substrate where it is deflected at a right angle (plane parallel to substrate) out to the edge of the module via a reflector and light transmission rod. Figure 3-3 shows a typical configuration.

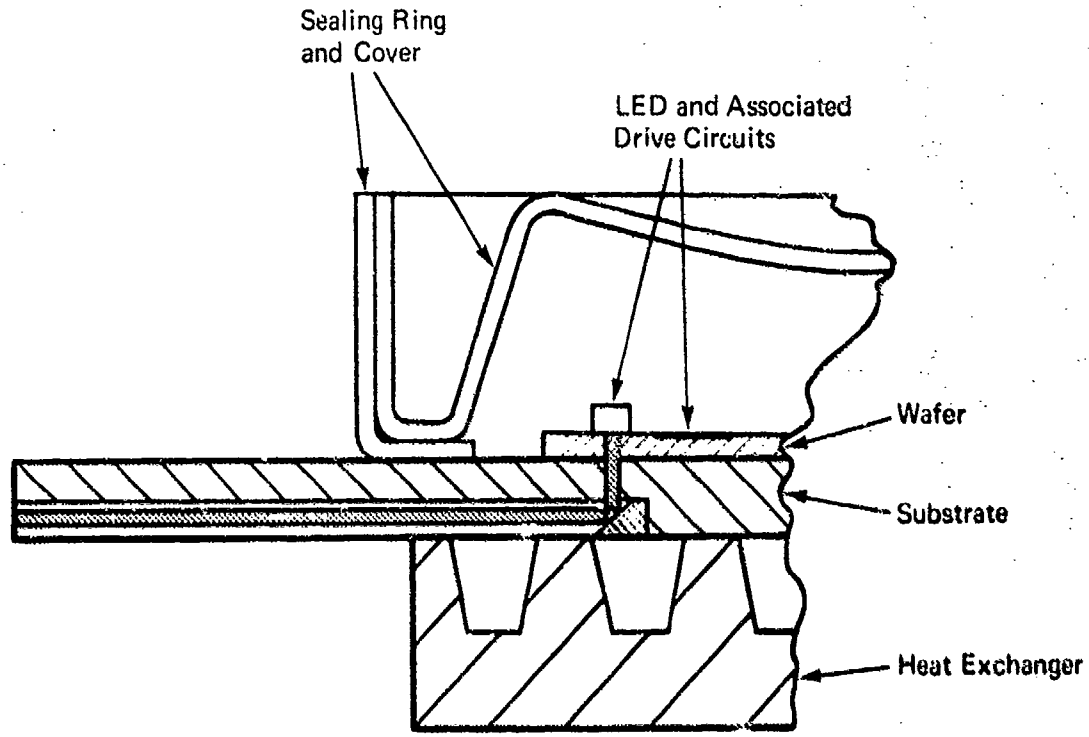
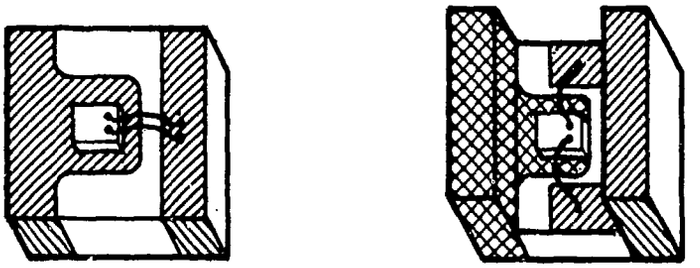


Figure 3-3. Basic On-Wafer Concept

3.1.2 OFF-WAFER CONFIGURATION

The other or alternate concept is the off-wafer approach. As the term implies, this approach places the LED devices outside of the wafer sealed cover area. Here the devices, either as chip or LID type packages, (see Figure 3-4) are bonded to appropriate land patterns provided just outside the hermetically sealed cover area. They are remotely connected to associated drive circuits on the silicon wafer via strip-line or tri-plate type printed wiring lines. This system is built up by sandwiching alternate layers of metallurgy and insulating materials directly onto the base alumina (Al_2O_3) substrate. The final sealing ring metallurgy is placed on top as shown in Figure 3-5.



Chip Type LED Package
(Off-Wafer)

LID Type LED Package
(On/Off-Wafer)

Figure 3-4. Proposed Hybrid Type LED Packages

State-of-the-art masking, deposition, and etching techniques may be used to provide the necessary circuit patterns and LED mounting pads. The associated driver and receiver circuits can be located around the periphery of the wafer similar to the on-wafer design. An appropriate light guide rod mated to each LED is permanently mounted to the topside of the substrate. This scheme provides for a highly efficient optical path between the LED and the edge of the module. Figure 3-6 illustrates this concept.

3.1.3 SUMMARY AND CONCLUSIONS

When parameters such as optical efficiency and fabrication complexity, development time and cost, and mechanical complexity are considered, the off-wafer approach is significantly more desirable than the on-wafer.

The on-wafer approach however, does offer significantly higher speed capability, limited only by the performance of the laser/LED selected for a particular system. This is attributed primarily to the very low-lead capacitances made possible by the ultra-short lead lengths inherent with this packaging approach.

The off-wafer approach is capable of achieving data rates up to 250 MHz. However proper electrical transmission design must be utilized to interconnect LED's and associated circuits.

This subsection described development of a candidate optical interconnection packaging concept. It also described two possible methods for configuring the

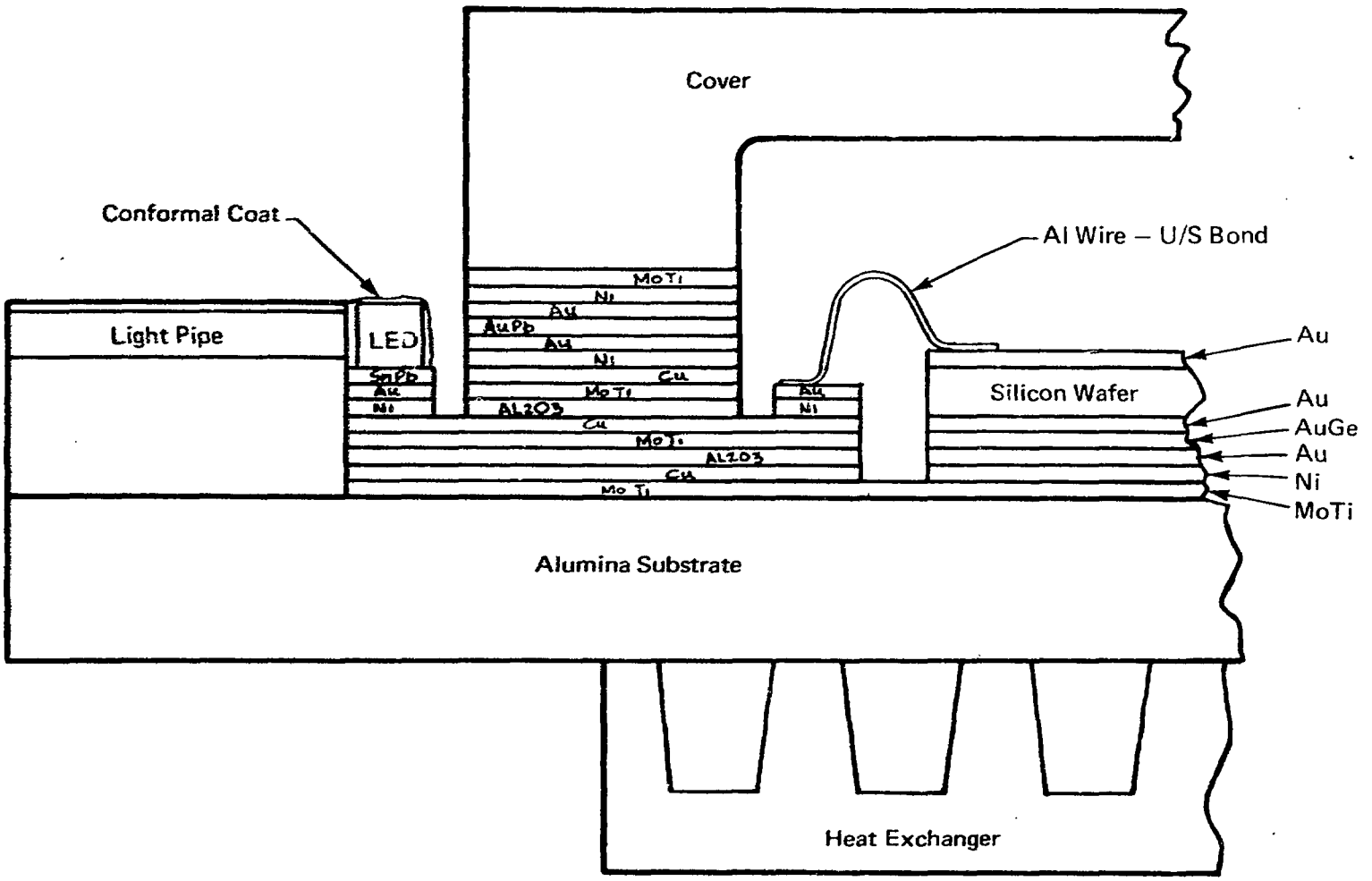


Figure 3-5. Typical Wafer Seal (Off-Wafer)

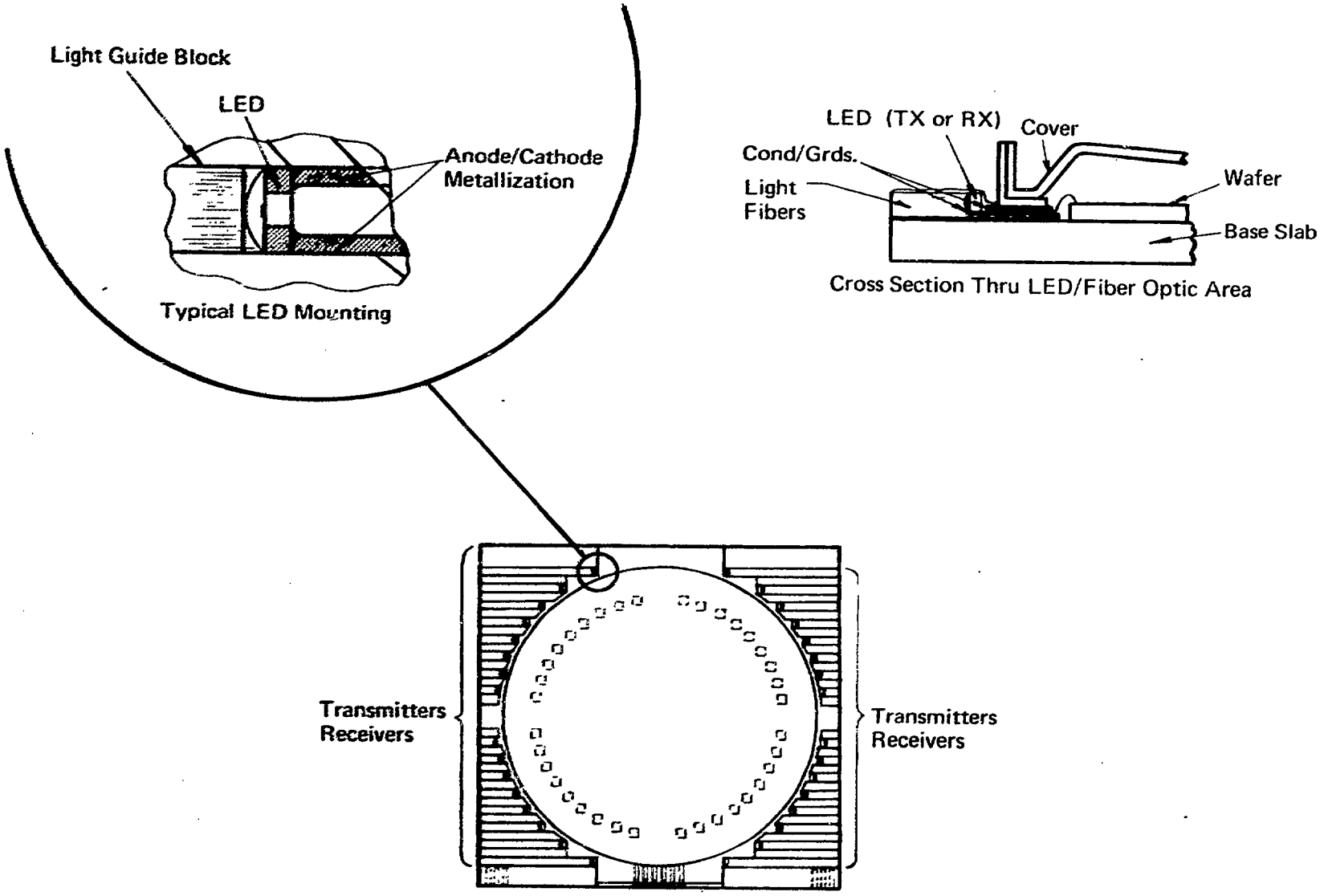


Figure 3-6. Proposed Off-Wafer Configuration

diode and circuits package within the module with emphasis placed on the off-wafer approach as being the most practical, efficient, and economical selection. Specific details and problems related to both approaches are discussed in the next subsection of this report.

3.2 PACKAGING CONSIDERATIONS

A decision to pursue either the on-wafer or the off-wafer configuration will depend primarily on the data rate selected for this specific application, commensurate with time and budget allocated to the design and incorporation of a light interconnection capability into the overall AADC package design. As discussed in Subsection 3.3, if speeds greater than 250 MHz are required, the on-wafer approach must be developed. This approach does however have some difficult development problems in attempting to get the light energy from inside the protective wafer cover out to the communicating edge of the module. Since this problem is unique to the on-wafer approach several design techniques are examined. Four of these concepts are illustrated in Figure 3-7.

Three of the LED mounting configurations examined place the source or receiver diodes on the topside of the silicon wafer in normal flip-chip fashion. This puts the active face of the diode in contact with the topside of the silicon wafer so that the infrared (IR) signal must pass directly through the silicon. However, the transmission properties of silicon are such that it will pass only the longer IR waves. The III-V compounds used to construct the emitters and receivers generally intended for use in this application emit at wavelengths of between 0.65 and 0.91 μm. The transmittance of silicon is between 1.2 and 15.0 μm. Therefore a window or hole must be provided in the silicon wafer to allow the light to pass through the wafer.

3.2.1 INFRARED TRANSPARENT MATERIALS

Since neither the silicon wafer nor the alumina substrate, as initially proposed for the AADC module, are transmissive at the desired wavelength, a suitable substitute material must be found. There are many materials that are IR transparent.

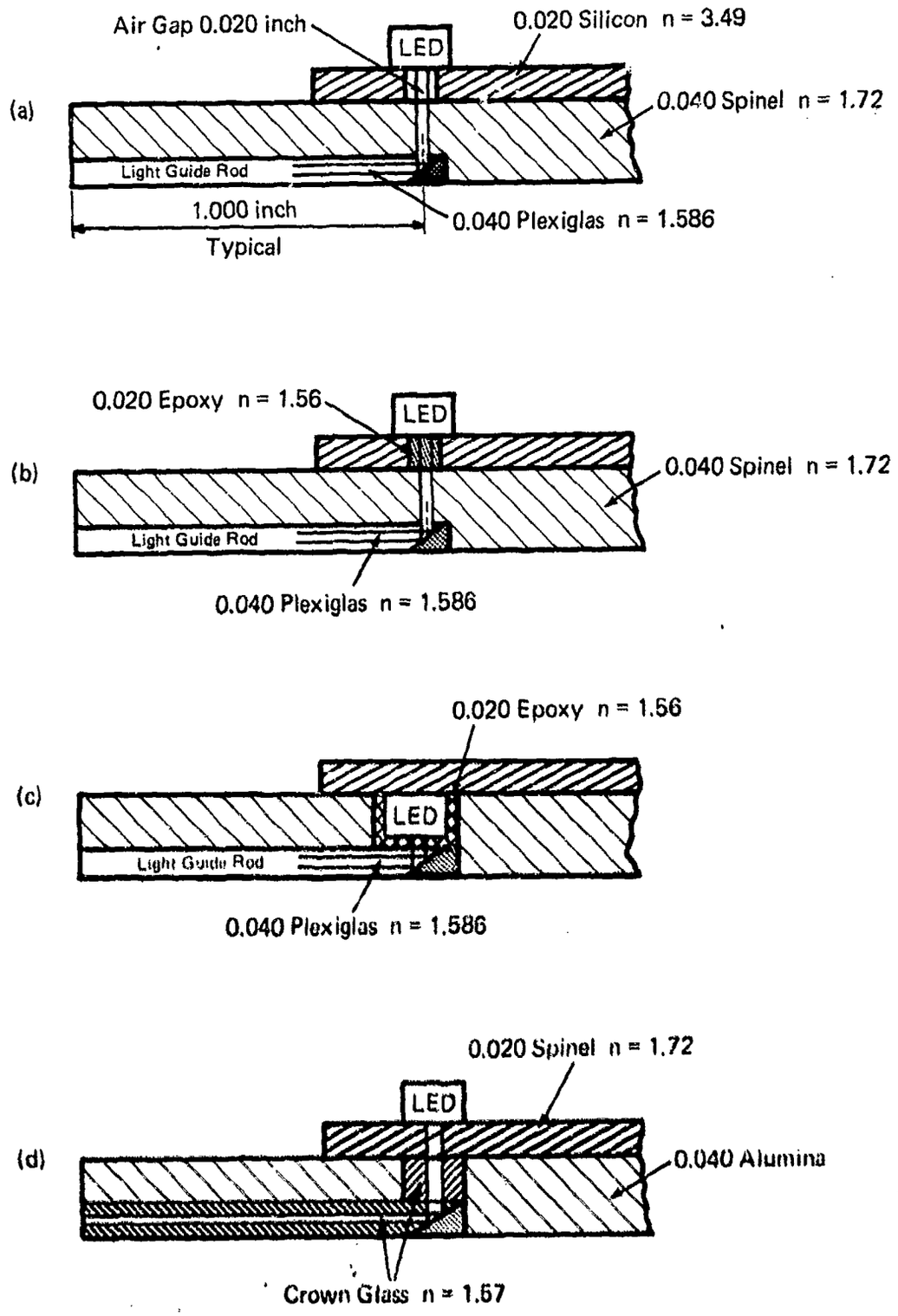


Figure 3-7. LED Mounting and Light Guide Configurations

However, to meet the needs of this particular application, only two materials, spinel and sapphire are seriously investigated. In selecting these materials the primary consideration was their light transmission characteristics, however, properties such as thermal expansion, index of refraction, thermal conductivity, and melting point were also important performance parameters. Both spinel and sapphire have very good transmission characteristics (82% to 85%) within the 0.7 to 0.9 μm bandwidth required, as shown in Figure 3-8. Also, there is very little spread in the light beam as it passes through appropriate thicknesses of either material as shown in Figure 3-9. This is important in this system because excessive beam spreading would drastically reduce the signal incident power received at the next interface resulting in a very high loss. These measurements were taken with a fixed gap between source and detector for both air and spinel/sapphire. This same gap was maintained when measurements using an interstitial material (microscopy immersion oil, n = 1.515) were taken to simulate bonded interfaces.

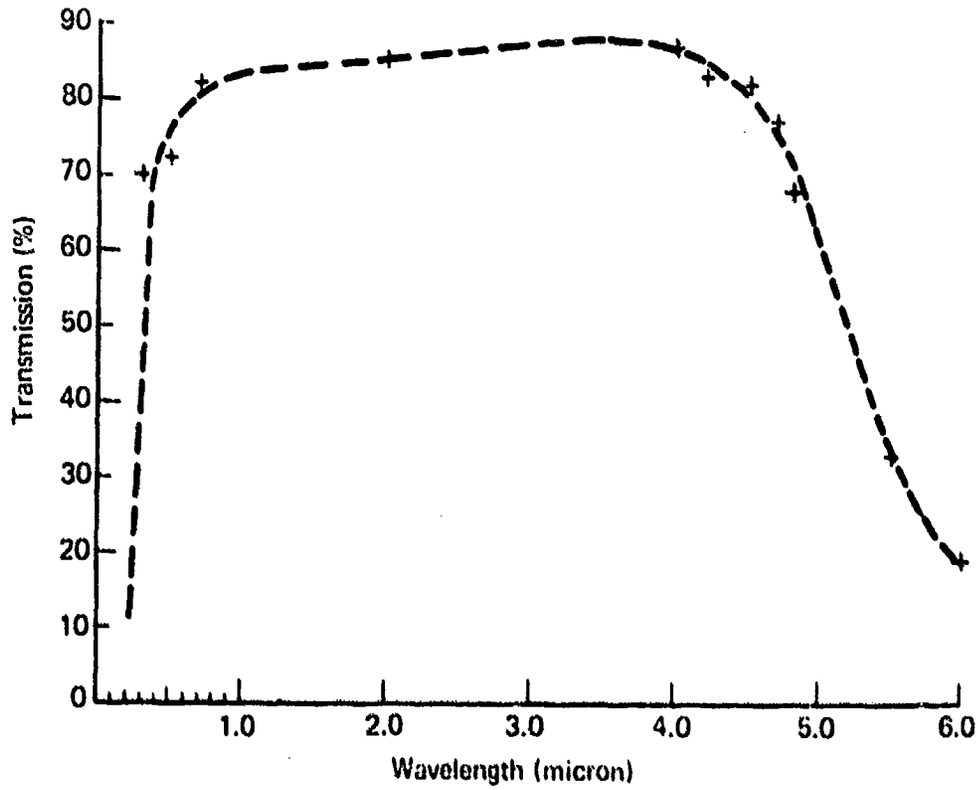


Figure 3-8. Light Transmission Characteristics of Sapphire or Spinel (0.215 inch thick sample)

A comparison of some of the more pertinent properties of spinel with sapphire, silicon, alumina and other related materials is shown in Table 3-1. Both of these materials can be supplied as either plain single crystal stock or as epitaxial (silicon on spinel/sapphire) wafers.

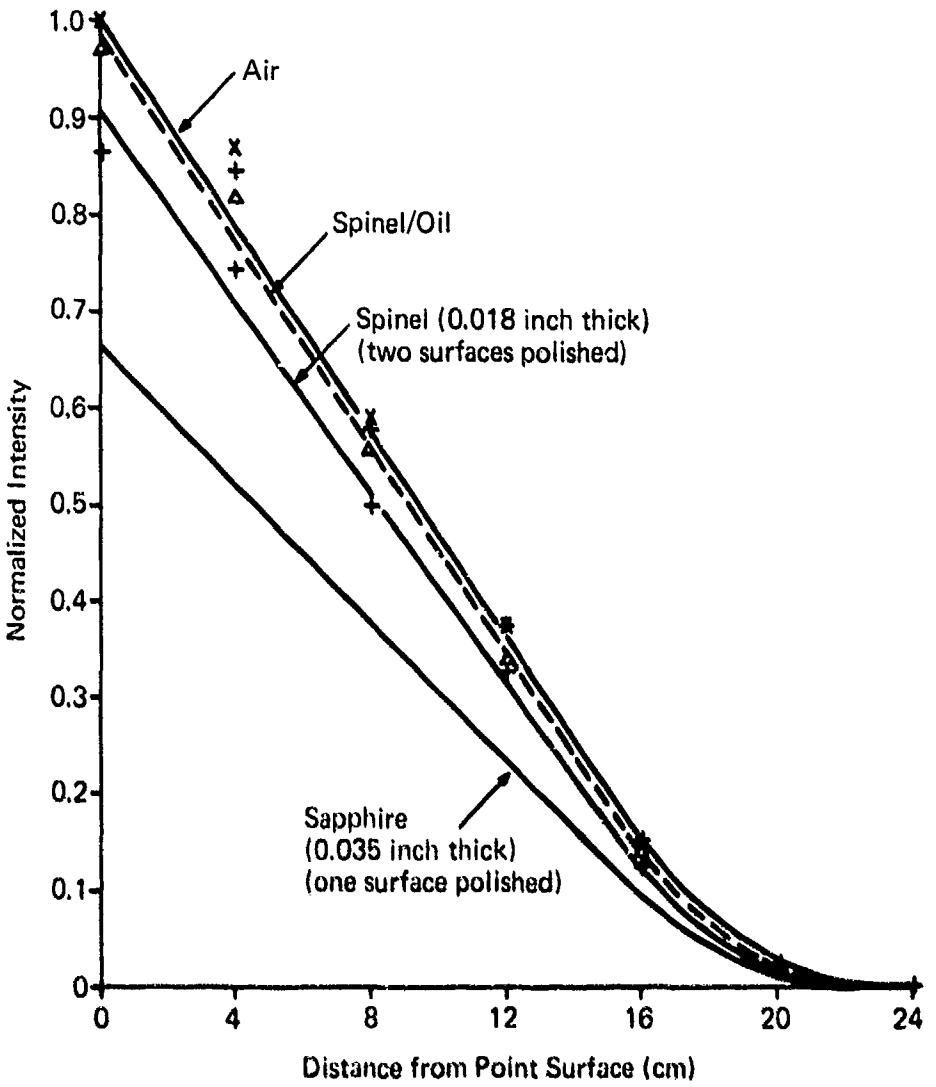


Figure 3-9. Normalized Light Distribution through Spinel and Sapphire

3.2.2 OPTICAL INTERFACES

Another problem inherent with the on-wafer approach is the many interfaces, and the indirect path required to get the LED energy out to the unit side panels.

The first approach is to provide a hole in the silicon directly under the diode and mount the silicon wafer onto a synthetic crystal substrate such as spinel or sapphire. This would replace the existing Al_2O_3 substrate (see Figure 3-7a). However, the problem that arises with this design is that the output from the diode passes through an air-gap (hole in the silicon) that has an index of 1.000 compared to spinel which has a refractive (n) index of 1.768.

In accordance with Snell's law we can see that the refractive index mismatch at the GaAs diode and air interface (3.589 to 1.000) and the air/spinel interface (1.00 to 1.77) would cause significant losses in the incident light output obtained from the LED through to the reflective plane in the light guide strip.

These losses can be reduced somewhat by utilizing better index matching materials at these interfaces such as shown in Figure 3-7b or by relocating the source/detector chip onto the bottom side of the wafer as shown in Figure 3-7c.

The latter technique not only eliminates one of the interfaces but more significantly reduces the distance between the source/detector active surface and the reflective surface in the light guide. This greatly enhances light output. This technique, however, would demand development of new mounting/bonding techniques since chips are now mounted on both sides of the wafer. It would also require holes in the silicon to electrically interconnect both sides. This is not common state-of-the-art practice employed with silicon wafers.

A fourth approach 3-7d is different from the others in that it would replace the silicon wafer rather than the alumina substrate with a spinel or possibly a sapphire wafer. Here again, a reflective surface on the light guide would be used to guide the beam at right angles out to the edge of the module. In this example the light guide material shown both normal to, and parallel to, the wafer is a crown glass. The glass was substituted to show that either glass or acrylics may be used for this purpose. This is important if the module operating or processing requirements dictate exposure to relatively high temperatures (greater than 150° C). The total transmission efficiency in this example is essentially the same with either material.

Table 3-1

COMPARISON OF PROPERTIES OF SPINEL AND SAPPHIRE WITH OTHER ASSOCIATED MATERIALS

Characteristic	Alumina 96%	Spinel	Sapphire	Silicon	Glass (Crown)	Galium Arsenide
Chemical Formula	Al_2O_3	$MgO\ Al_2O_3$	Al_2O_3	Si		GaAs
Expansion Coefficient (10^{-6}/°C)	7.3	7.45	8.4	3.5	9.5	5.93
Index of Refraction	0.578a	1.727a	1.77a	1.4b	1.586	3.30
Transmission Range (μm)	0.17 to 6.5c	0.3 to 5.0d	0.3 to 5.0d	1.2 to 15.0c	0.35 to 3.0e	
Thermal Conductivity Cal/cm-s/°C @ 25°C	0.088	0.068g	0.10	0.30	0.002	
Melting Point °C	2072	2135	2040	1412	~730	1238
Dielectric Constant	9.6	8.4f	9.4 to 11.4f	13.0	~4.0	11.1f

a. at 0.58 μm
b. at 1.4 μm
c. > 10%
d. 82%
e. 95%
f. 1 MHz @ 25°C
g. 0.035 @ 100°C

Although the LED in these examples is shown as a discrete device, it is possible that a suitable device could be generated directly onto the epi-spinel surface along with the associated circuits.

Other approaches very similar to the above were considered. The exception being that the light guide would be located on the top side (wafer side) of the substrate rather than the bottom. However, the combination of material expansion rates and the cost to achieve a good flat surface, such that a good reliable seal could be maintained between the cover and the substrate, was considered an overriding factor against this approach.

3.2.2.1 Analytical Evaluation — Optical Losses

An analytical assessment of the optical losses inherent with each configuration a, b, c, and d was made to allow selection of the most efficient design and appropriate optical materials for an on-wafer design. The analytical data also includes information on the off-wafer design to allow comparison.

To make the comparison, sources of losses were considered as well as the size of the bundle of light which is reflected by the 45° mirror surface on the light guide rod. Although the light guide rod may not be circular, bundle comparisons were made for circular apertures. The following three comparisons were made.

1) Fresnel reflection losses at material interfaces
2) Cone of light accepted by 45° mirror
3) Transmission of light through light guide rod.

Fresnel reflection losses at normal incidence are given by

$$R = \frac{(n_1 - n)^2}{(n_1 + n)^2}$$

where n_1 and n are the indices of the materials at the interface. The results using the above formula, on the transmission through the four configurations as well as the straight through off-wafer design are tabulated in Table 3-2.

The size of the bundle of light which enters the acrylic rod is governed by the geometrical configuration of material between the LED and the 45° reflector. The amount of light collected from a Lambertian LED is proportional to the square of the numerical aperture of the beam transmitted by the system. This is not a symmetrical beam, and the minimum and maximum angular acceptance angle by the 45° reflector have been determined. The average of these two values has been used to determine the amount of light within the cone. The results are given in Table 3-3. Table 3-4 gives the combined result of comparisons Tables 3-2 and 3-3. From this we may conclude that the off-wafer design is, from an optical transmission standpoint, approximately 50% more efficient than the on-wafer approach.

Table 3-2

TRANSMISSION THROUGH INTERFACES (%)

Interface	Configuration				
	a	b	c	d	Off Wafer
LED/Air	75	-	-	-	-
LED/Epoxy	-	90	90	-	90
LED/Spinel	-	-	-	93	-
Air/Spinel	93	-	-	-	-
Epoxy/Acrylic	-	-	100	-	100
Epoxy/Spinel	-	100	-	-	-
Spinel/Acrylic	100	100	-	-	-
Spinel/Glass	-	-	-	100	-
Acrylic/Air	95	95	95	-	95
Glass/Air	-	-	-	95	-
Total Transmission (%)	66	85	85	88	85

Note: The off-wafer configuration would realize an additional 5 to 10% more light output since it does not employ a 45° mirror in the system

Table 3-3

TRANSMISSION AS A FUNCTION OF GEOMETRY

Configuration	Cone of Light Half Angle			Average	
	Max.	Min.	Avg.	NA	$(NA)^2$
a.	16.3°	10.3°	13.3°	0.365	0.13
b.	19.4°	11.7°	15.6°	0.427	0.18
c.	45°	18°	31.5°	0.829	0.69
d.	19.1°	11.5°	15.3°	0.414	0.17
Off-Wafer				1.000	1.000

Table 3-4

LED LIGHT COLLECTION FOR EACH CONFIGURATION

Configuration	(Geometry) Transmission	(Fresnel Losses) Transmission	(% of LED Lambertian Emittance) Relative Total into Acrylic
a.	13%	66%	8.6%
b.	18%	85%	15.3%
c.	69%	85%	58.7%
d.	17%	88%	15.0%
Off-Wafer	100%	85%	85.0%

In order for all the light reflected off the 45° reflector to go through the light guide rod by total internal reflection, it must have a numerical aperture greater than the maximum NA of the bundle as given in Table 3-3. For the sides of the rod surrounded by air, there is no problem. However, at the guide rod-spinel interface, if a cement is used, the index of refraction of the cement used must be considerably lower than that of the guide rod material. For example, using a cement index of 1.5 gives an NA of 0.515 which will satisfy configurations a, b, and d, but not c. Three possible methods may be considered for this transmission medium.

1) Acrylic rod using low index cement.
2) Cladded rod with high NA (glass)
3) Reflective coating between the rod and spinel.

Total internal reflection is preferred, if possible, since it is highly efficient if surfaces are kept extremely clean.

3.2.3 MATERIALS COMPATIBILITY — OPTICAL/ENVIRONMENTAL

As previously stated, materials, particularly for the light guide section of the module assembly, must be selected primarily for their total internal reflecting properties. Also, their ability to withstand moderately high temperatures, their processability, and their resistance to abrasion, particularly at the exit interface, is important. When these factors are considered, clad glass appears to be the

ideal candidate. The glass rod selected should have a sufficiently high refractive index (1.7) to ensure good internal reflection since the cladding and, more important, the bonding materials used to hold the rod in place may have an index as high as 1.56. Certain plastic materials do have fairly desirable optical and processing properties. However, they are not stable at high temperatures (130°C); and they have very high thermal expansion coefficients (140 x 10^{-6}/°C) which is not compatible with either a spinel or alumina substrate (7.37 x 10^{-6}/°C) in either a low or high temperature (200°C) environment. This compares with a coefficient (α) of 9.0 x 10^{-6}/°C for a glass rod.

The thermal mismatch between a plastic (typically allyl diglycol) rod and the substrate would cause severe stress at the bonded interface which would ultimately result in a fracture or failure of the bond or the plastic. For this same reason, it might also be very difficult to hold a fixed optical airgap between the module and the side panel light guide using plastics.

The availability and use of a suitable high temperature epoxy bonding system to retain the light guide components is feasible, however, proper sequencing of the various processing and assembly operations associated with fabrication of the module precludes its use. Optical grade epoxies capable of performing in 175°C ambients are available. Nonoptical grades are good to 235°C. The ultimate use of epoxies in this system would depend primarily on the module thermal design characteristics.

Utilization of spinel or sapphire for either the wafer or substrate in the on-wafer design should present no problem. Both materials are well suited to high temperature and other environments as specified in MIL-E-5400L. Both spinel and sapphire have higher melting temperatures than does silicon (refer to Table 3-1), therefore, they are very suitable for most applicable bonding or sealing techniques.

3.2.4 THERMAL CONSTRAINTS

The placement of the LEDs and the necessary driver and receiver circuits onto the module imposes an additional thermal load on the wafer. This might limit

the extent to which the remaining area of the wafer may be utilized for other circuit functions. To examine this the following analysis was made, based on these assumptions:

1) Evaluate a worse case condition which assumes that all 32 TX/RX channels will be used at the same time
2) Assume that all heat is dissipated uniformly across the wafer
3) Assume that the wafer population for LIT will utilize both planar and hybrid devices/techniques
4) Assume the transmitter LED and driver circuits will dissipate approximately 70 mW and be contained on a chip/surface measuring 0.062 by 0.125 inch total area
5) Assume the receiver LED and driver circuits will dissipate approximately 190 mW and be contained on a chip/surface area measuring 0.125 by 0.125 inch.

A cursory analysis of the impact this would have on thermal density based on the proposed specifications (ref. AADC report Contract No. N001970-C-0504 dated 3 December 1971) is as follows:

For the transmitter function the thermal density is:

$$\frac{P}{A} = \frac{(70)(10)^{-3}\ W}{(8)(10)^{-3}\ in^2} = 8.7\ W/in^2$$

Since this exceeds the thermal density specification of 3 W/in^2 set forth for the AADC wafer, then the minimum free area required for this function is:

$$\frac{\text{Power Required}}{\text{Thermal Density Limit}} = \frac{(70)(10)^{-3}\ W}{3\ W/in^2} = 0.023\ in^2 \text{ (0.125 by 0.188 area)}$$

Therefore if the designated TX functions are spaced on 0.188 inch centers along both axes then a favorable thermal density that is well below the specified 3 W/in^2 limit can be achieved.

$$\frac{P}{A} = \frac{(70)(10)^{-3}\ W}{(0.188)(0.188)\ in^2} = \frac{(70)(10)^{-3}}{(353)(10)^{-4}} = 2\ W/in^2$$

For the receiver function the thermal density is:

$$\frac{P}{A} = \frac{(14)(10)^{-2}}{(156)(10)^{-4}} = 9 \text{ W/in}^2$$

The mounting area required for this circuit to meet the 3 W power density limit is

$$\left(\frac{0.14 \text{ W}}{1}\right)\left(\frac{1 \text{ in}^2}{3 \text{ W}}\right) = 0.047 \text{ in}^2 \text{ minimum}$$

This is equivalent to an area 0.188 by 0.250 inch. Therefore, the receiver circuits may be mounted along a vertical axis on the wafer that is similar to the transmitter circuits, however additional free area (0.250 inch rather than 0.188 inch) must be provided along the horizontal axis to accommodate the higher dissipation. Figure 3-10 depicts one possible layout for these circuit/LED combinations on a 3.00 inch wafer.

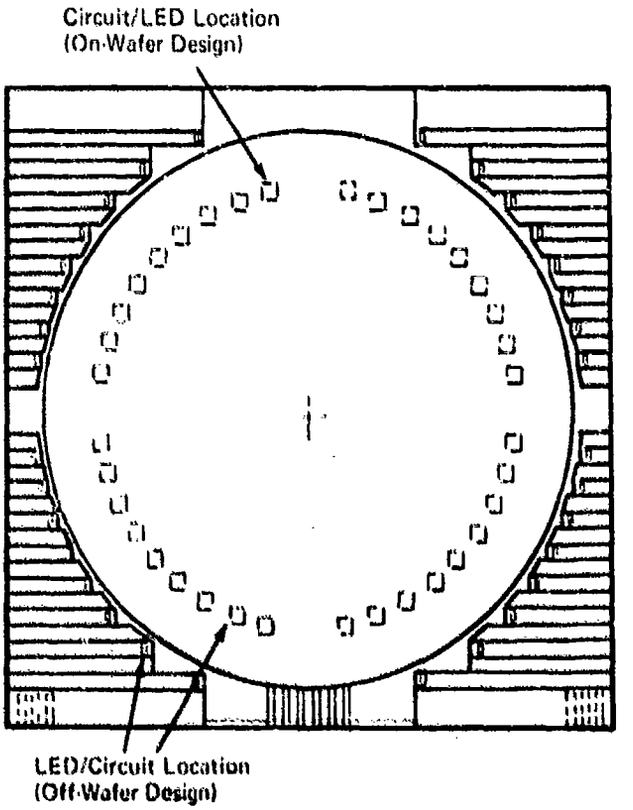


Figure 3-10. Typical LED/Circuit Layout on Module

A breakdown of the typical total dissipation required for optical interconnection in both the on-and off-wafer approach is shown below:

	TX	RX	Total
LED (mW)	10	1	11
Circuits (mW)	60	119	179

or 190 mW per TX/RX pair

Assuming a duty cycle of 100% for a module, the total dissipation of the interconnection function for the on-wafer design is .190 (16) or 3.04 W. In the off-wafer configuration the dissipation on the wafer itself is (.179) (16) or 2.864 W, with the remaining 0.176 W dissipated along the outer edges of the substrate.

3.2.5 DATA RATES

When high data rates are required, the packaging design for a high-speed optical data link becomes particularly critical in terms of placement of, and interconnection between, transmitter/receiver devices and their associated drive circuits. In this application, the on-wafer concept does not present a problem because it allows very close proximity of the appropriate LED to the drive circuits. Using both monolithic and hybrid circuit technology, the physical separation between the two is insignificant taking up a total area of less than 0.0156 in^2. Therefore, it is the off-wafer design approach that must be given serious consideration both in terms of mechanical placement of the chips, and in the design of the microstrip line connecting the TX/RX device to the circuits. Parameters such as impedance matching, cross coupling and isolation can seriously affect the data transfer rate independent of the device (LED/PD) performance. An in-depth study of these parameters was investigated specifically with regard to the proposed off-wafer design and is discussed in detail in Subsection 3.3 of this report.

3.2.6 MECHANICAL OPTICAL ALIGNMENT

The optical alignment of the modules to the light guides in the side panels of the proposed concept are permanently fixed into the design. This is true of either

the on-wafer or the off-wafer approach. Standard design tolerances and machining techniques can be employed to achieve this, such that no initial, routine alignment, or adjustments are necessary.

Depending upon the diameter and distance between mating optical interfaces, a certain amount of misalignment is tolerable. Therefore, with proper manufacturing tolerances very little degradation in coupling efficiency will occur.

3.2.6.1 Transmission vs Displacement

The transmission of light through a junction of light pipes or optical fibers is a function of the alignment of one pipe relative to another. Considering displacement as the only variable, the amount of light being transmitted is a function of the amount of displacement of one pipe relative to the other.

It is assumed in this consideration that the pipes have the same diameter, that there is zero distances between the ends of the two pipes, that the pipes at the point of contact have perpendicular end faces, and the axes are aligned. Also, it is assumed that the distribution of light is uniform within the core of the light pipe, and that the core diameter is the diameter to be used. Under the above assumptions, it is reasonable to expect that the amount of light transmitted through the junction is proportional to the common area of the intersection of the two circles representing the adjacent ends of the two pipes. The coupling efficiency is expressed by the ratio of the areas A to B as illustrated in Figure 3-11.

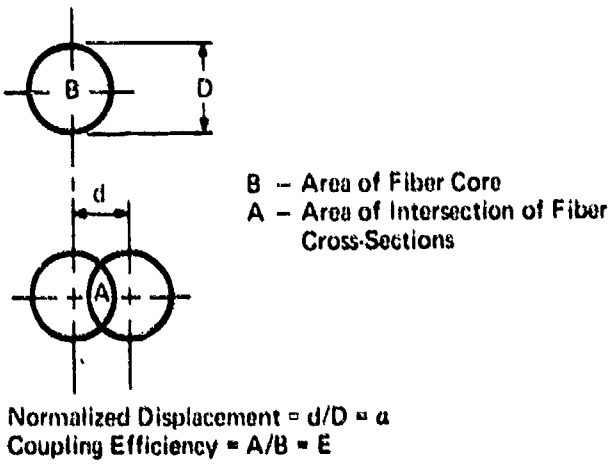


Figure 3-11. Fiber Core-to-Displacement Area Relationship

$$A = \frac{D^2}{2} (\text{Cos}^{-1} \alpha - \alpha \sqrt{1 - \alpha^2})$$

$$B = \frac{\pi D^2}{4}$$

$$E = \frac{A}{B} = \frac{2}{\pi} (\text{Cos}^{-1} \alpha - \alpha \sqrt{1 - \alpha^2})$$

This analysis is used to produce a curve of relative transmission as a function of normalized displacement (Figure 3-12). Experimental results are plotted on the same curve to show how well practice conforms to theory.

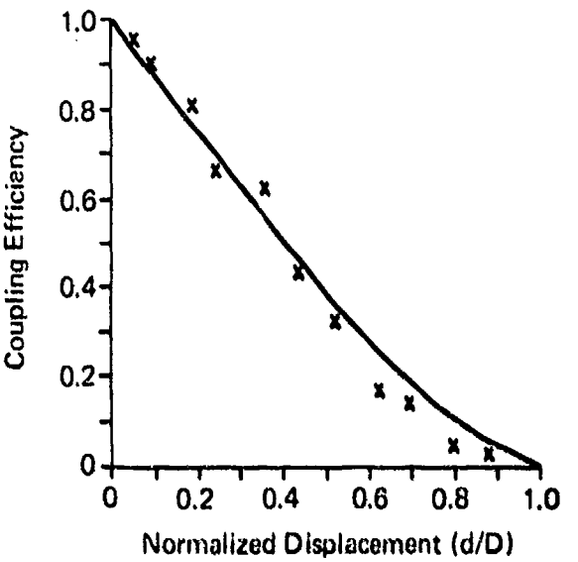


Figure 3-12. Fiber-to-Fiber Coupling Efficiency vs Normalized Displacement

3.2.7 SUMMARY AND CONCLUSIONS

Here again, the detailed evaluation of specific problem areas associated with the on-wafer approach demonstrate that this is a viable, but less efficient and more costly scheme. The off-wafer design offers a 50% increase in coupling efficiency. The use of IR transparent substrates such as spinel, or sapphire, to implement the on-wafer concept is optically acceptable; and processing these materials for microelectronics applications is currently feasible and practical. From a thermal consideration, the low-dissipation circuits associated with the optical

interconnection function, when properly spaced and bonded to the module wafer, impose a negligable thermal load on the module. Also, the area required for these circuits and LED devices on the module is insignificant (approximately 0.28 in^2 out of 7.1 in^2 total area) and should not effect the total useful area of the wafer for other functions. Good design practice and normal high-quality fabrication tolerance limits can be used to obtain an acceptable optically aligned package with no periodic adjustments required.

In summarizing, this section considered several important mechanical design aspects associated with performance and cost for both the on-wafer and the off-wafer approach. A decision to pursue one design over the other will depend primarily on the functional performance required (data rate and number of lines) and secondly, the development schedules and costs involved.

3.3 ELECTRICAL CONSIDERATIONS

The electrical considerations relative to the AADC relate to the choice of on-wafer and off-wafer approaches. The applicability of these to the AADC and the merits and problems of these approaches on an electrical basis are discussed in this subsection.

3.3.1 ON-WAFER APPROACH

The on-wafer approach, as far as electrical considerations are concerned, would be the best approach. Speed limiting interconnections would be eliminated, since the electro-optic conversion devices could be placed at the site of the circuit. Circuit design would also be somewhat simplified since only the parameters of the conversion devices themselves would have to be considered. Although this approach is the superior electrical approach and would yield the highest speed of operation it must be tempered by the optical, thermal, and space requirements on the substrate.

The optical requirements placed on the substrate material would impact the present design and higher level packaging of the wafer. Materials which are optically compatible do exist and were tested within the scope of this program. A feasible approach to the packaging utilizing these materials has been described in this report

but a fabricated model of this type could not be approached within the scope of the program.

Space requirements of the LED and the photodetector would also reduce the usable substrate area due to their required physical size. Although this may be acceptable, it must be a consideration since 32 devices equal in size to the diameter of the transmission medium are being considered for the AADC program.

3.3.2 OFF-WAFER APPROACH

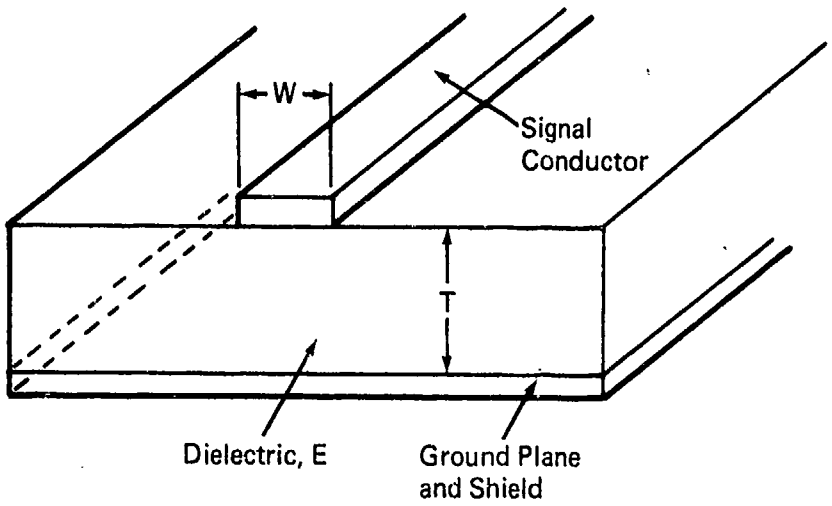
There are two considerations which were addressed during the electrical analysis of this approach, impedance matching and shielding. The performance of these parameters is almost entirely dependent upon the physical configuration, therefore generation of an optimum design required investigation of appropriate techniques.

In the off-wafer approach, the high speed digital signal is transferred outside of the hermetically-sealed package via some form of printed circuit conductor. This conductor is a transmission line, and, as such, must be configured using the constraints of transmission line design. An ideal transmission line allows current and voltage signals of various frequencies to travel to the load at the same phase velocity, with the same attenuation, and with no reflections occurring any place along the line. Reflections and re-reflections of a pulse on the transmission line can cause erroneous results in the digital processing circuitry.

Some techniques for carrying signals throughout a system are shown in Figure 3-13, which depicts "strip line," "printed circuit" techniques which can easily be fabricated on a substrate.

Figure 3-13a shows an open system where the narrow conductor carries the signal and the ground plane provides the shield. Figure 3-13b shows a semishielded system called "tri-plate" or "strip line."

a. Open System



b. Triplate System

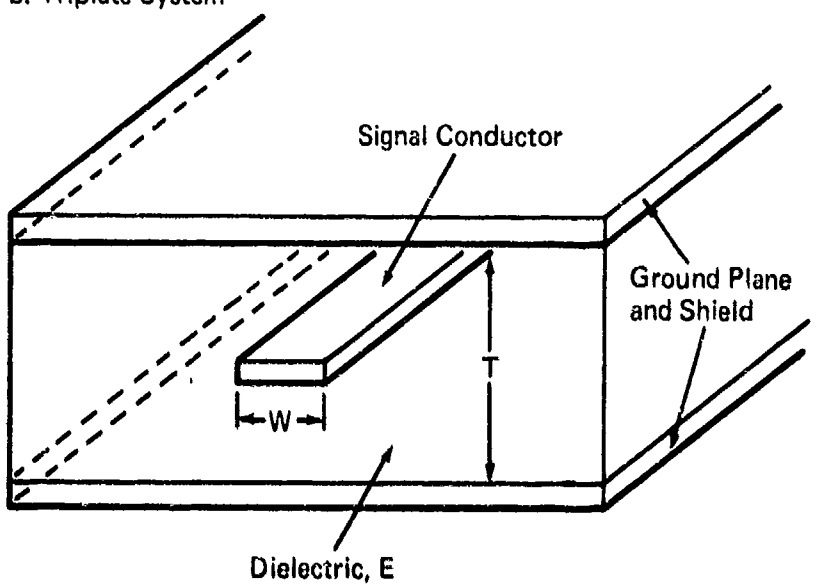


Figure 3-13. Transmission Line Systems

3.3.2.1 Shielding and Impedance Matching

There are two primary considerations to examine when high frequency digital signals are transmitted over printed circuit, wire, or coax systems. These are shielding and impedance matching.

1) Shielding — **Prevents the land, or conductor, from picking up spurious signals from outside source radiation.**

2) Impedance Matching — Allows a more efficient energy transfer of electrical signals and eliminates reflections on the signal line. Reflected signals act as additional digital data causing erroneous results in the computing systems.

Shielding and impedance matching are interrelated since they are determined by common physical parameters such as conductor spacings, dielectric material type and thickness, and conductor width. Much has been written describing the coupling between different line configurations at high frequencies and extensive theoretical analysis of cross talk and coupling between adjacent lines has been performed, (References 2 and 8). Based on these theoretical and empirical works, a design can be formulated and order of magnitude numbers for characteristic impedance, isolation, and other system parameters can be determined.

In the following subsections, data will be presented to give an idea of the relative order of magnitudes of impedance matching and isolation encountered in carrying a proposed 200 MHz signal to and from a LED mounted external to the LSI wafer. These numbers will then be related to signal-to-noise ratio (SNR), gain requirements, and various high speed AADC applications.

3.3.2.2 Characteristic Impedance

The electrical version of the off-wafer approach to the AADC package is shown in Figure 3-14. In the analysis of this package, we will first consider characteristic impedance of the line pattern. To eliminate signal reflections the characteristic impedance Zc of the line pattern must equal the input (Zi) and output (Zo) circuit impedances. The impedance of the conductor is a function of the conductor width, the spacing between the conductor and the ground plane, and the dielectric material.

The triplate configuration, that of a conductor buried in a dielectric covered by two conducting ground planes, is the preferred configuration because it offers more isolation between closely-spaced lines; also lines adjacent to the signal line can be made ground. The triplate pattern allows mounting of external supports, etc., (such as the wafer cover) without electrically affecting the characteristics of the signal line.

Figure 3-15 is a curve which represents the conductor's characteristic impedance for an open and triplate geometry as a function of conductor width for T = 0.70 inch (Reference 6).

The significant conclusion from Figure 3-16 is that lines of the proper characteristic impedance can be built that have the low characteristic impedance of an LED and a receiver load resistor. When the line is terminated in its characteristic impedance, there are no reflections. The goal then is to design the transmission line so that its characteristic impedance matches the load presented by the transmitter/receiver diodes circuitry.

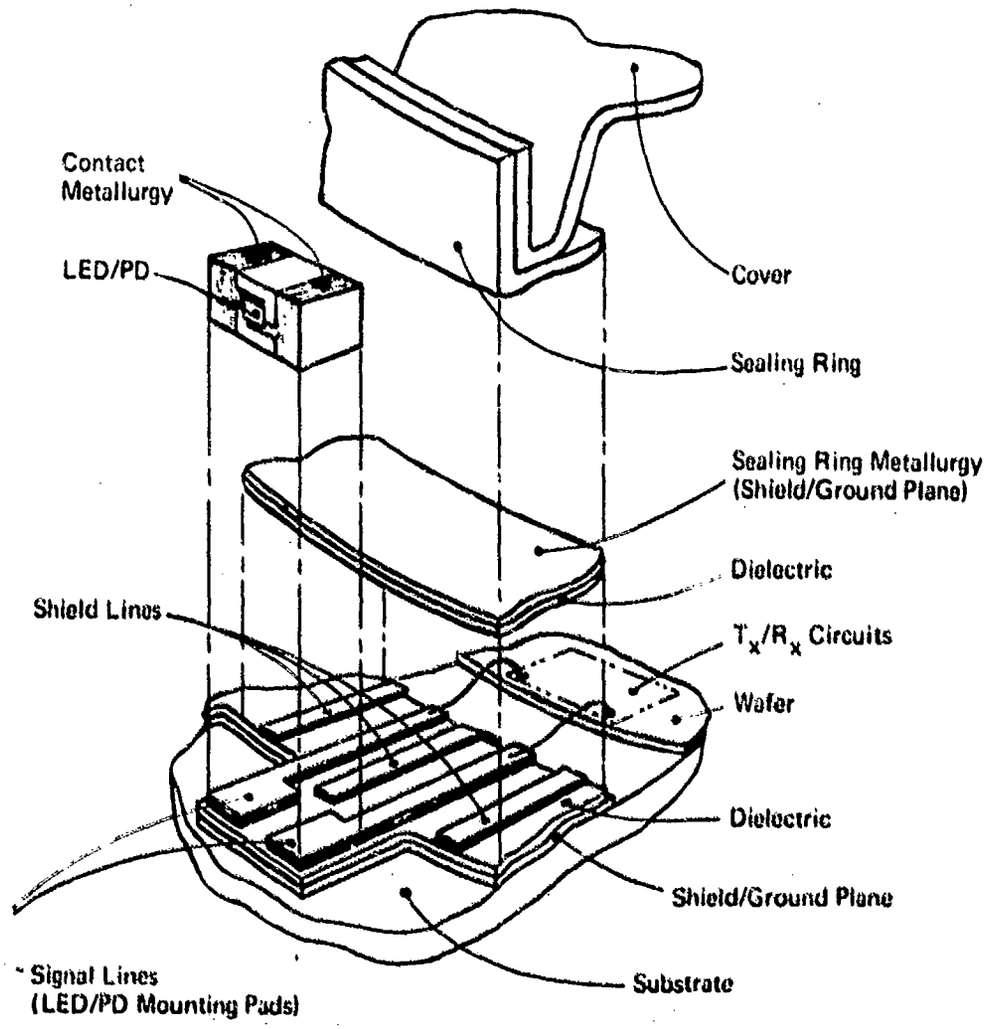


Figure 3-14. Electrical Transmission Line Configuration, Off-Wafer Design

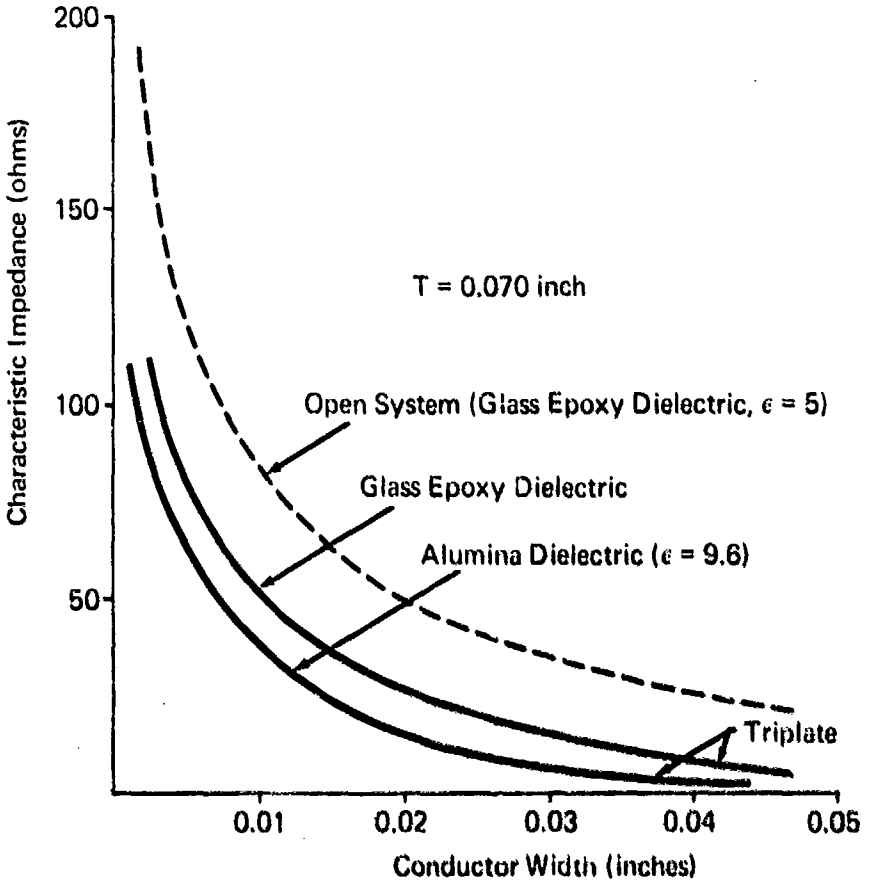
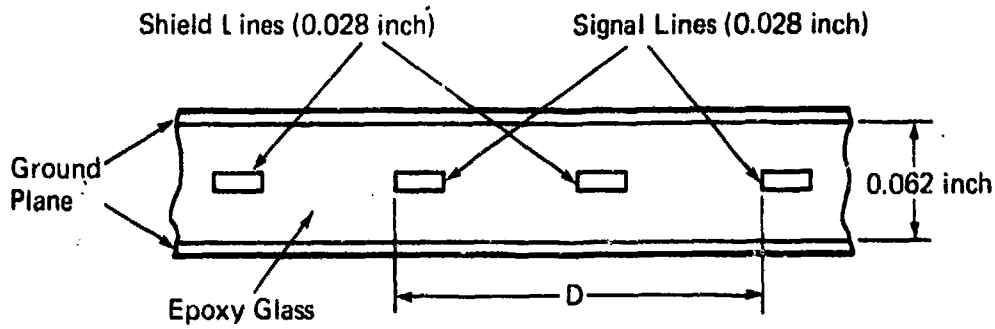


Figure 3-15. Typical Characteristic Impedance as a Function of Conductor Width



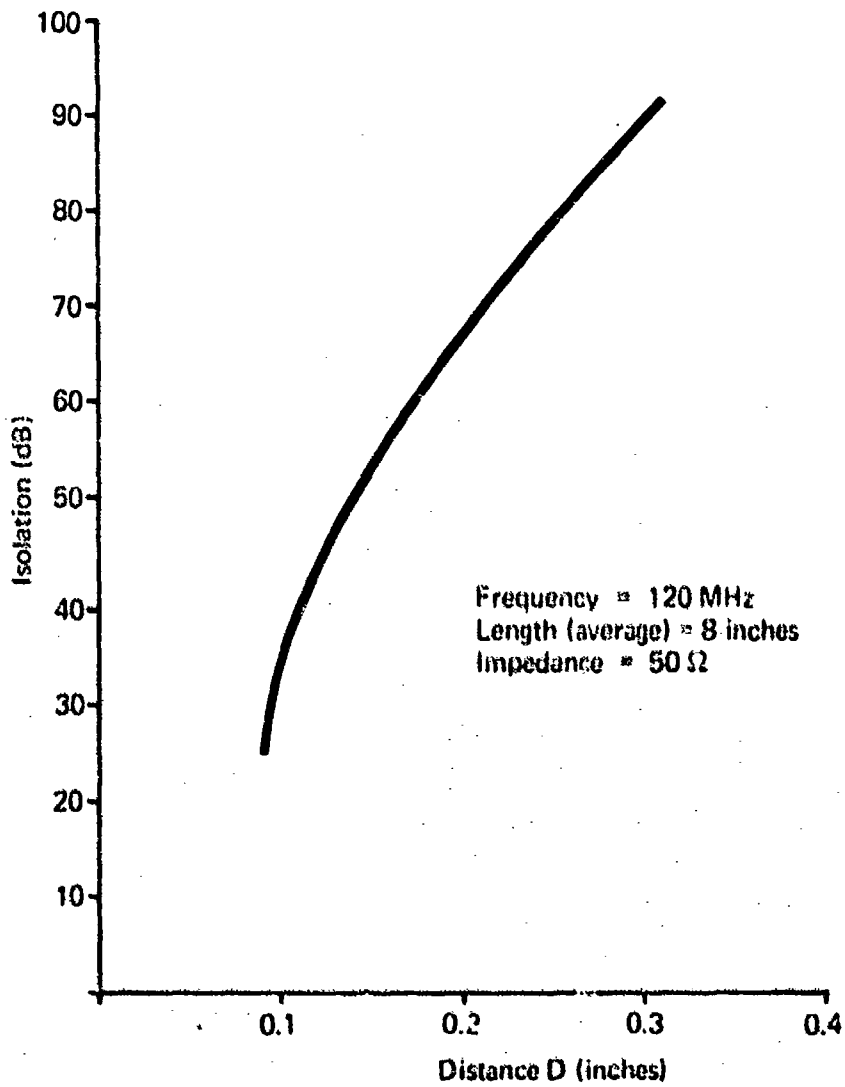


Figure 3-16. Isolation vs Line Spacing for a Triplate Shield Arrangement

3.3.2.3 Crosstalk and Isolation

Another factor to consider is shielding of the signal lines, to prevent cross-coupling and crosstalk. The shielding provided by a signal transmission scheme, such as triplate techniques, depends on several factors; among them, the length of the line, line capacitances, line inductances, the dielectric of the mediums or medium between conductors and ground plane, and the physical separation of the signal lines. It is difficult to accurately determine by analysis the crosstalk or isolation between adjacent channels on the AADC chip because it is difficult to specifically define the physical characteristics of the model. Variables, such as the length and the characteristic of the connecting member between the wafer and the conductor line, will involve dependent technologies such as bonding to silicon, line patterns, sizes, and locations which are not immediately available. What can be done is to determine what isolation is required for the AADC application based on signal levels, probability of false alarm, driver/receiver characteristics, and signal-to-noise ratios. This value can then be compared to measured isolation values for a triplate configuration.

A SNR of 16 dB yields 0.9999 probability of detection and 10^{-6} probability of false alarm (Reference 7). The worst case configuration for crosstalk in the data channels on the alumina substrate would be a transmitter driver line adjacent to a receiver diode line. Spacing between these channels would be small, 0.25 inch, and the difference in signal level would be large. Typical values for such an arrangement follow.

The exercise below was conducted to determine if the off-wafer approach provided adequate shielding for the isolation required.

Model — SNR = 16 dB

Transmitter light = 0.3 mW @ 10 mA

System light losses = 10 dB

Light Energy at detector = 0.03 mW

Signal current in receiver line

(assume 0.35 A/W responsivity) = 0.0105×10^{-3} A

Assuming a 50Ω system, yields power levels of:

Receiver signal power = $(1.05 \times 10^{-5})^2$ (50) = 5.5×10^{-9} W

Transmitter signal power = $(10 \times 10^{-3})^2$ (50) = 5×10^{-3} W

A ratio of 16 dB SNR at the output of the receiver amplifier requires that the receiver signal power be ~ 40 times higher than any noise. (This noise would consist of noise already on signal, thermal noise in the load resistor, and noise generated in the receiver amplifier.)

$$\frac{5.5 \times 10^{-9}}{40} = 0.137 \times 10^{-9} \text{ W tolerable noise}$$

If we assume that the majority of the noise is due to crosstalk from the adjacent signal line, then the minimum isolation required is

$$\frac{5 \times 10^{-3} \text{ (W transmitter)}}{0.137 \times 10^{-9} \text{ (W tolerable noise)}} = 3.65 \times 10^{7}$$

or approximately 76 dB isolation.

The requirement for a 76 dB isolation can be readily achieved by noting the measured values for the system illustrated in Figure 3-16. The data was taken by injecting a 120 MHz signal into a signal line and measuring the percentage of signal that appears in an adjacent terminated signal line. It is noticed that 76 dB isolation can be achieved by a signal line separation of 0.2 inch. Considering that the average line length in Figure 3-16 is 8 inches and the maximum length for the off-wafer approach is 0.5 inch, the isolation should be far better. No crosstalk problems are anticipated in the off-wafer technique.

Section 4

LIGHT SYSTEM LOSSES - PROPOSED AADC CONFIGURATION

As mentioned in Subsections 2.1, 3.1, and 3.2, the optical losses in the system are dependent on device packaging considerations, interface losses, alignment, etc. All of these parameters must be optimized to yield an optical interconnection with minimum loss. The optical path for the AADC module-to-module interconnection is illustrated in Figure 4-1. Since the lengths of fiber optic are very small light attenuation in the fiber can be neglected. The major optical losses will occur at the interfaces and numerical aperture limiting of the fiber rods.

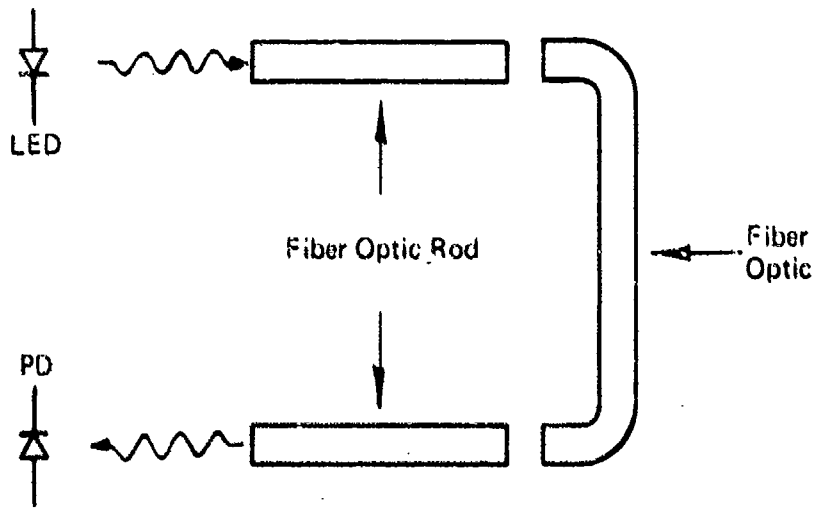


Figure 4-1. Module-to-Module Optical Interconnection

Subsections 4.1 and 4.2 will discuss these losses and Subsection 4.3 will establish an overall optical efficiency for the interconnection system.

4.1 NUMERICAL APERTURE

Light propagates through a fiber optic by total internal reflection at the core/cladding interface. In order for a ray of light to meet this requirement, it must be incident upon the fiber within an acceptance angle given by the relation,

$$\theta = \text{arcsine} \frac{(n_2^2 - n_1^2)^{1/2}}{n_3}$$

where: θ = acceptance angle

n_1 = core refractive index = 1.62

n_2 = cladding refractive index = 1.52

n_3 = air refractive index = 1

The numerical aperture is defined as the sine of θ. Figure 4-2 illustrates the path of a ray (Ray 1) bound by the core/cladding interface, and, for the parameters illustrated, has an acceptance angle of 34°. For short lengths, however, consideration should be given to that light which is confined within the fiber by the cladding/air interface. The cladding/air interface yields a theoretical acceptance angle of greater than 90°. Physically, the acceptance angle is limited to 90°. Ray 2 in Figure 4-2 depicts a light ray bounded by the cladding/air interface.

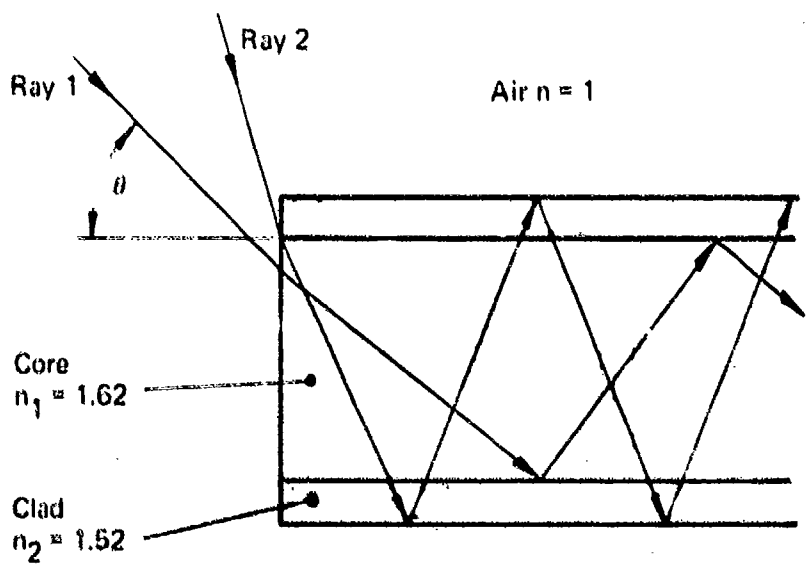


Figure 4-2. Light Transmission in an Optical Fiber

Matching a Lambertian light emitting diode (small compared to fiber rod size) to this particular light pipe results in the following relative distribution of light:

1) Reflected off front surfaces of rod - 11% (both ends)

2) Contained in core - 28%

3) Bound by cladding - 61%

In practice, oil on the cladding, dirt, touching of adjacent fibers, etc., all cause an irregular surface condition which results in the loss of the light bounded by the cladding/air interface. A single piece of masking tape (1 inch) on a 3-inch glass rod has been seen to cause a 50% reduction in the light output through the rod. Some of this occurs normally in all fiber optic cables due to epoxy in terminations, touching fibers, cable shield, etc., and is observable and defined as coupling loss. However, only 28% of the light from the LED will be transmitted by the fiber optic rod unless precautions are taken to ensure a clean cladding/air interface. If this is done, 61% of the light will be transmitted through the rod.

4.2 FIBER-TO-FIBER COUPLING EFFICIENCY

It is desirable to predict the amount of light collected when two light pipes or (fibers) are separated by some distance, with alignment being maintained. This section will describe approximate relationships which can be used to predict this effect. The results of the calculation will be compared with experimental values. It is not intended to obtain exact formulation, but only approximation methods to give usable results.

The following factors are used to compare experimental and analytical results:

1) Source - LEDs — The distribution of the radiations from different LEDs can be approximated by a $\cos^n \theta$ function. A plot of the distribution where n=1, n=7, and n=13 is shown in Figure 4-3. A Lambertian source has a distribution of $\cos \theta$. The measure output of a light emitting diode source is compared with the $\cos \theta$ function in Figure 4-4.

2) Light Rod or Fiber — The light rod or fiber to be compared with analytical computation is one with a cladding. Such a rod or fiber transmits light through the core dependent upon the numerical aperture (NA) of the rod or fiber. It is assumed for this analysis that the output end of a fiber has the same distribution as the input

to the fiber. The two light pipes separated by a distance (d) have the same diameter (D). The distance is normalized as a function of fiber diameter (d/D).

The following subsections give the theory of illumination received from finite sources with different distributions:

1) From a Lambertian source into a hemisphere
2) From a source of distribution $\cos^n \theta$ into a hemisphere
3) From a Lambertian disc source to a point on a parallel surface
4) From a Lambertian disc to a parallel coaxial disc.

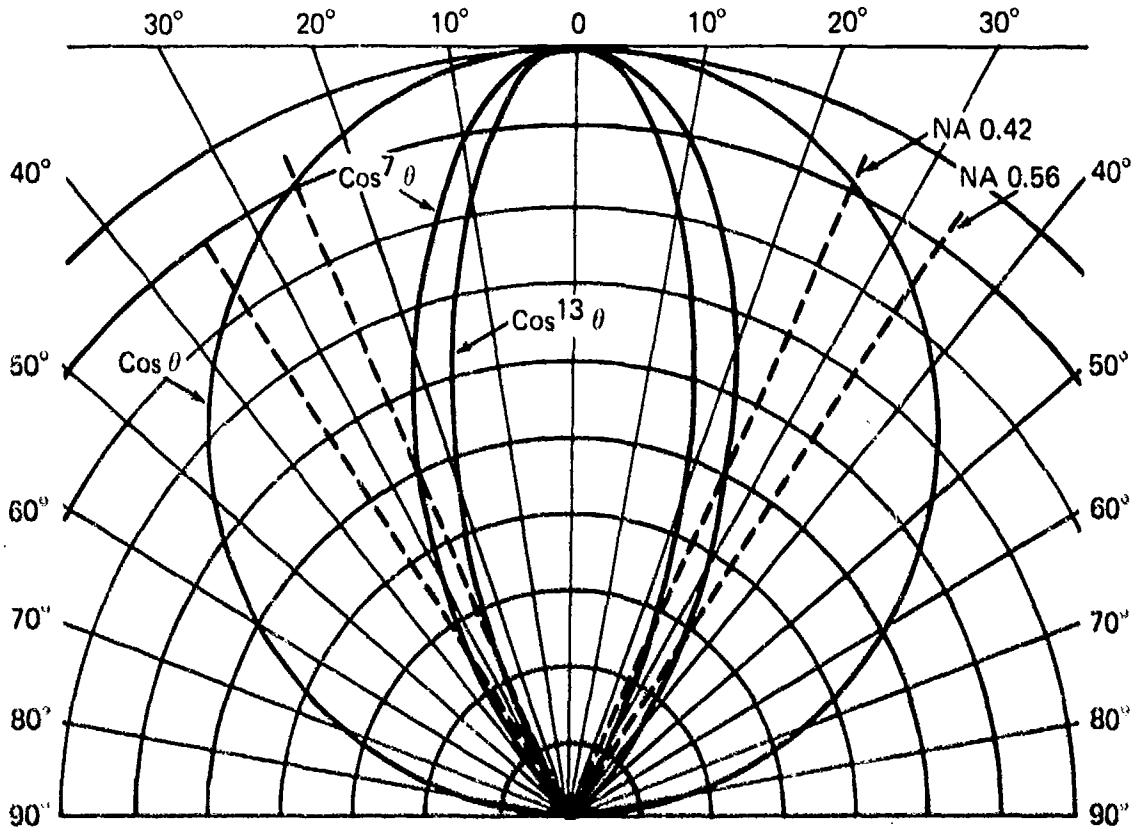


Figure 4-3. $\cos^n \theta$ Source Light Distribution

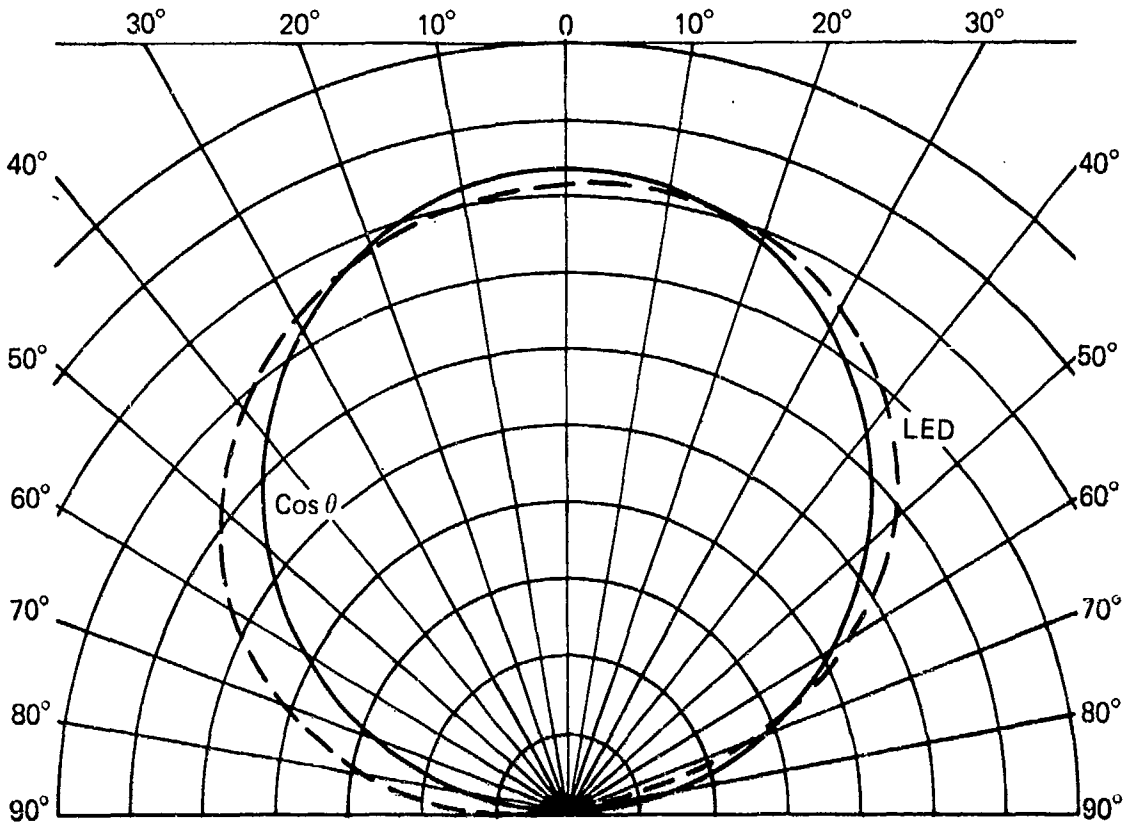


Figure 4-4. LED - Approximate Lambertian Light Distribution

4.2.1 FROM A LAMBERTIAN SOURCE INTO A HEMISPHERE

The light emitted into a hemisphere by a Lambertian source (Figure 4-5) can be obtained by utilizing the following groundrules:

1) Small area of source at center of hemisphere - a
2) Intensity in direction making an angle θ with the normal to the source area - $Ba \cos \theta$
3) Solid angle subtended by a narrow angular ring making angle θ with the normal - $2 \pi \sin \theta \, d \theta$

   The flux (dF) emitted within the ring defined above is the product of the intensity and the solid angle

$$dF = 2 \pi Ba \sin \theta \cos \theta \, d \theta \qquad (4-1)$$

Integrating to obtain the total flux emitted into the hemisphere gives

$$F = \int_0^{\frac{\pi}{2}} 2\pi \, Ba \sin\theta \cos\theta \, d\theta \qquad (4\text{-}2)$$

$$= \pi \, Ba$$

The total flux radiating from a disc of radius r is

$$F = \pi^2 r^2 B \qquad (4\text{-}3)$$

The flux emitted within a cone defined by a given numerical aperture can be found by changing the limits of integration of Equation 4-2.

$$F = \pi^2 r^2 B \left[\sin^2\theta\right]_0^{\theta_o} \quad (NA = n \sin\theta_o) \qquad (4\text{-}4)$$

$$= \pi^2 r^2 B \sin^2\theta_o$$

The fraction (R) of the total flux which is accepted within a cone of half angle α is given by

$$R = \sin^2\alpha \qquad (4\text{-}5)$$

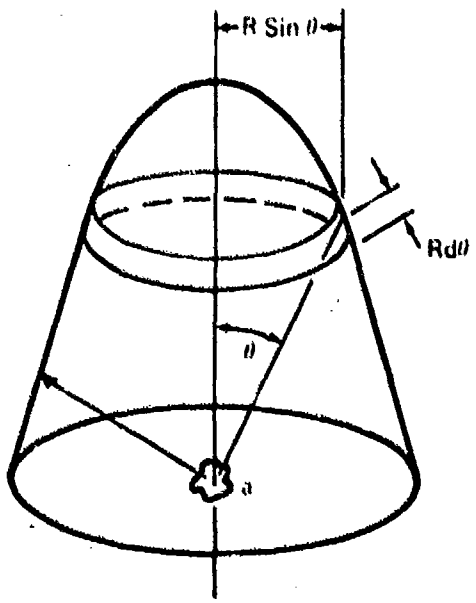


Figure 4-5. Lambertian Source Radiating into a Hemisphere

4.2.2 FROM A SOURCE OF DISTRIBUTION $\cos^n \theta$ INTO A HEMISPHERE

Consider a distribution given by the n'th power of the cosine,

$$Ba \cos^n \theta$$

Integrating to obtain total flux in a hemisphere gives

$$F = \int_0^{\pi/2} 2\pi \, Ba \sin \theta \cos^n \theta \, d\theta$$

$$= \frac{2\pi \, Ba}{n+1} \tag{4-6}$$

The total flux radiating from a disc of radius r is

$$F = \frac{2\pi^2 r^2 B}{n+1} \tag{4-7}$$

The flux within a half angle (α) cone is

$$F = \frac{2\pi^2 r^2 B}{n+1} (1 - \cos^{(n+1)} \alpha) \tag{4-8}$$

The fraction of the total flux accepted within a cone of half angle α is

$$R = (1 - \cos^{n+1} \alpha) \tag{4-9}$$

Equation 4-5 is a special case of formula 4-9 with n=1.

4.2.3 FROM A LAMBERTIAN DISC SOURCE TO A POINT ON A PARALLEL DISC

Figure 4-6 shows the geometry and defines the angles for this discussion. By the inverse square law, the illumination of the surface at P having a normal of angle ϕ with PQ being radiated by a Lambertian source at Q having a normal of angle θ with PQ (see Figure 4-6) is given by

$$(Ba \cos \theta)(b \cos \phi)/s^2$$

where:

a is a small area at P

and

b is a small area at Q.

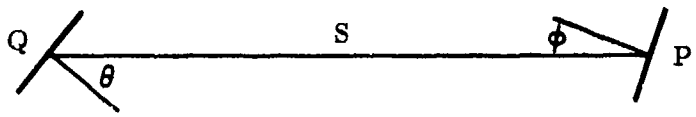


Figure 4-6. Lambertian Disc Source to Parallel Disc

This expression reduces to the following when $\theta = \phi$.

$$B\ a\ b\ \cos^2\theta/s^2$$

When the source becomes larger, the above expression must be integrated over the source area to obtain the illumination at P.

The illumination at P (Figure 4-6) by an anulus of radius x and width dx is given by

$$bd^2 = 2\pi x\ dx/(d^2 + x^2)^2$$

where $a = 2\pi x\ dx$

$$\cos^2\theta = \frac{d^2}{(d^2 + x^2)}$$

$$s^2 = (d^2 + x^2)$$

The total illumination at P from the disc of radius r is given by integrating the above expression.

$$I = 2\pi\ Bd^2 \int_0^r x(d^2 + x^2)^{-2}\,dx$$

$$= \pi B r^2/d^2 + r^2 \qquad (4\text{-}10)$$

$$= \pi B \sin^2\theta$$

Note the similarity of the above result to the results obtained in Subsection 4.2.1. In a similar manner, when the source is not Lambertian but has $\cos^n\theta$ distribution the result is

$$I = \pi\ B\ \frac{2}{n+1}\ (1 - \cos^{n+1}\theta)$$

When the receiving element is not on the axis of the radiating disc, but a distance ρ from the axis, the illumination becomes

$$I = \frac{\pi}{2} B \left[1 - \frac{d^2 - r^2 + \rho^2}{\sqrt{(d^2 + r^2 + \rho^2)^2 - 4r^2 \rho^2}} \right]$$

4.2.4 FROM A LAMBERTIAN DISC TO A PARALLEL COAXIAL DISC

By integration over the area of a receiving disc, the flux which reaches any disc from another parallel disc radiating according to the cosine law is

$$F = \frac{\pi^2 B}{2} (r_1^2 + r_2^2 + d^2) - \sqrt{(r_1^2 + r_2^2 + d^2)^2 - 4r_1^2 r_2^2} \qquad (4\text{-}11)$$

Equation 4-11 is an exact formula, however, it cannot be used as given for the coupling between two fibers because of the numerical aperture constraint imposed by the fibers. Consequently, approximate formulae are developed below as they apply to the coupling efficiency between fibers. The above theory is used as the basis for the approximate formulae.

The formulations given in the previous subsections can be used to predict the amount of light transmitted from the end of one light pipe to another light pipe of the same diameter at a distance (d) from it. See Figure 4-7.

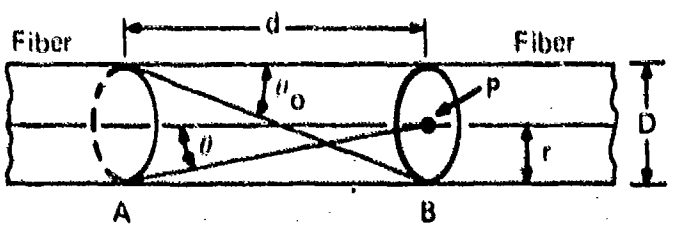


Figure 4-7. Light Pipe Interface

When d is such that sin θ_0 is less than the numerical aperture of the fiber, then every point at B receives light from the entire aperture at A. At separations greater than the above distance Equation 4-10 can be used to give an appropriate value of the light received at B.

For a Lambertian source, the intensity of a point at B is

$$I(\text{at P}) = \pi B \sin^2 \theta$$

The flux which can be received by the fiber at B is

$$F \text{ (at B)} = \pi^2 B r^2 \sin^2 \theta$$

(r = radius of fiber)

The total flux which is radiated at A is given by

$$F \text{ (radiated at A)} = \pi^2 B r^2 \sin^2 \theta_o \tag{4-12}$$

where $\sin \theta_o$ = NA of the fiber

For d > do the normalized light (NO) received by the fiber at B is given by the ratio of Equation 4-11 divided by Formula 4-12

$$NO = \frac{\sin^2 \theta}{\sin^2 \theta_o} \tag{4-13}$$

where $\tan \theta = r/d$

$\tan \theta_o = D/do$

For distances less than do, that is, when every point on the aperture at B does not receive light from the entire aperture at A, the approximation is made that the light received decreases linearly with distance.

This is expressed by the following equation for d < do.

$$NO = 1 = \frac{d}{do} \left[1 - (NO)x\right] \tag{4-14}$$

where $(NO)x = \frac{\sin^2 \theta x}{\sin^2 \theta_o}$

$\tan \theta x = r/do$

Relationships 4-13 and 4-14 for a Lambertian source are plotted in Figure 4-8. The solid line is the analytical curve; the points marked x are the experimental points. The calculations were made for a fiber of 0.56 numerical aperture (NA). The curve changes with NA as is shown in Figure 4-9.

For a source with distribution of the form $\cos^n \theta$, relationships similar to 4-13 and 4-14 can be derived. These are given by

for $d \geq do$

$$NO = \frac{(1 - \cos^{n+1}\theta)}{(1 - \cos^{n+1}\theta_o)} \tag{4-15}$$

and

for $d < do$

$$NO = 1 - \frac{d}{do} \left[1 - (NO)x\right]$$

where

$$(NO)x = \frac{(1 - \cos^{n+1}\theta x)}{(1 - \cos^{n+1}\theta_o)} \tag{4-16}$$

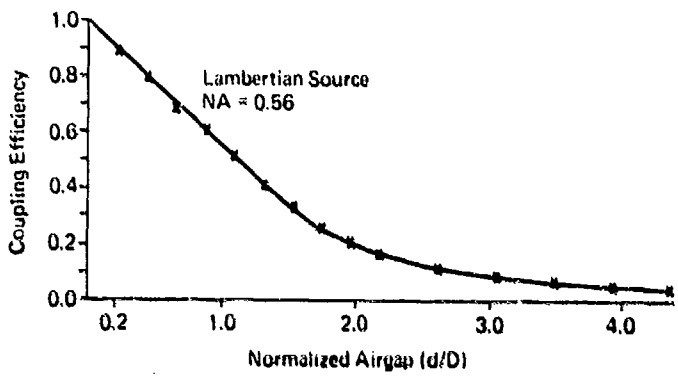


Figure 4-8. Fiber-to-Fiber Coupling Efficiency vs Air Gap

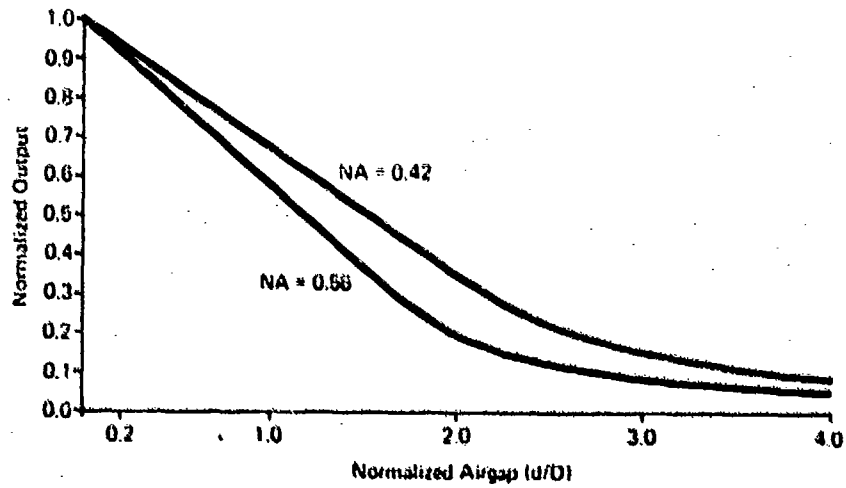


Figure 4-9. Fiber-to-Fiber Coupling Efficiency for Different NAs

Figure 4-10 shows how the curves change as the source distribution is different. Analytical curves are plotted for $\cos\theta$, $\cos^7\theta$, $\cos^{11}\theta$ and $\cos^{13}\theta$ distributions of the source.

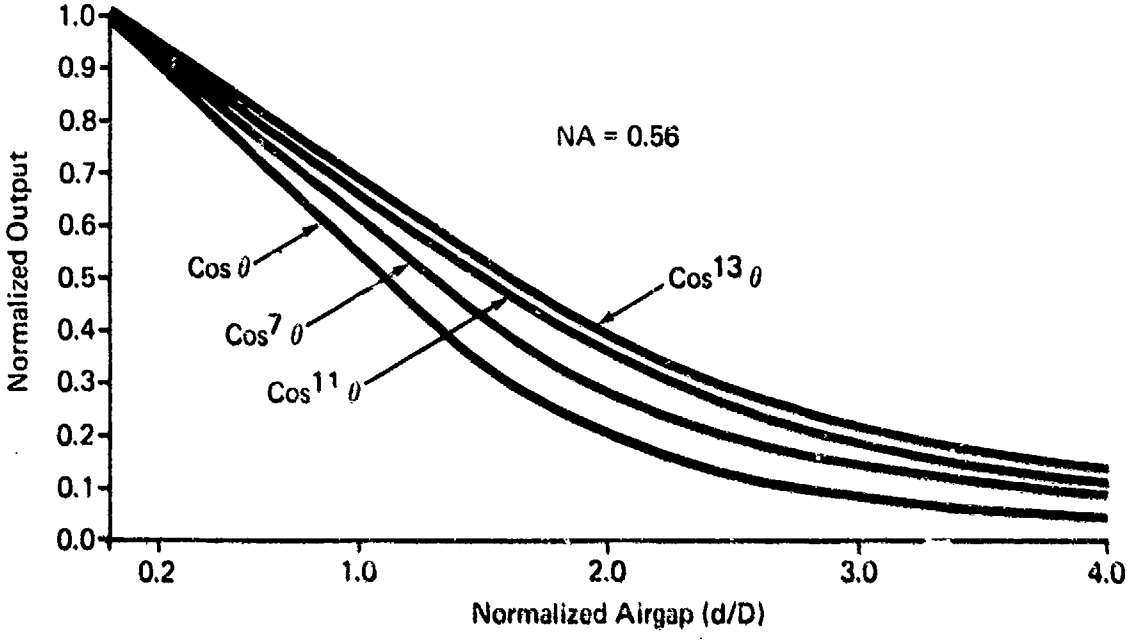


Figure 4-10. Output vs Air Gap for Different Source Distributions

Again, it should be pointed out that the analytical curves are only approximations. It is possible to do much more precise calculations, but the time involved is not warranted since the source distributions are not precise mathematical functions. It is surprising that the results were as good as shown in the curves. Better results should be possible by numerical techniques.

Only meridional (not skew) rays were used in the analytical methods. The normalization of the output into the second fiber eliminated the loss due to Fresnel reflection at the surfaces and also provided a better comparison of analytical and experimental results. It is assumed that source distribution is maintained within the core of the fiber within its NA.

4.2.5 SUMMARY

Analytical results on coupling efficiency as a function of spacing between fiber rods show that the efficiency can be expressed linearly for small separations (less

than the fiber rod diameter). For separations less than the diameter, more than 50% of the light is coupled between the fiber rods. For 90% efficiency the spacing should be about one-fifth of the fiber rod diameter. The efficiency is somewhat better for lower numerical aperture fibers and for source distributions which give more peaked outputs than Lambertian sources.

4.3 OPTICAL INTERCONNECTION EFFICIENCY

The optical efficiency of the interconnection in the off-wafer configuration is approximated by the relation,

$$E = (NA)^2 \cdot \rho^6 \cdot PF \cdot C_o \cdot (D_L A_L)^2 \qquad (4\text{-}17)$$

where

NA = Fiber rod NA = 0.56

ρ = Fresnel transmission coefficient = 0.95

PF = Fiber bundle packing fraction = 0.75

C_o = Fiber rod to photodiode Coupling efficiency = 0.85

D_L = Displacement efficiency = 0.90

A_L = Airgap efficiency = 0.90

This relation considers the pertinent areas of optical loss for the configuration illustrated in Figure 4-1.

As discussed in Subsection 4.2 the percentage of light collected by a fiber rod from a Lambertian source is equivalent to the square of the NA (neglecting Fresnel reflection losses). For an NA of 0.56 only 31.4% of the light is collected. For a typical fiber rod with a core refractive index of 1.62, the Fresnel transmission coefficient is 0.94. Since there are six surfaces (see Figure 4-1) the sixth power of the Fresnel transmission coefficient is used. The fiber optic bundle, which is used in the side panels has a typical packing fraction of 75% (core area/total area). A typical coupling coefficient for a fiber rod/photodiode interface is 85% provided the photodiode is placed very close to the fiber. This can be achieved in the off-wafer configuration. If a 10% alignment tolerance is placed on the fiber-to-fiber inter-

face at the edge of the module, a 90% coupling efficiency can be achieved (see Figure 3-12). Also, allowing an airgap of 20% of the fiber diameter will yield a coupling efficiency of 90% (see Figure 4-8). The quantity $D_L A_L$ is squared in Equation 4-17 because there are two airgaps in the off-wafer configuration (Figure 4-1).

Putting the appropriate values for the parameter in Equation 4-17 and performing the indicated operation yields an optical coupling efficiency of 9.5% (~10 dB). Consequently, with a minimum of caution and without using any optical techniques to improve the efficiency an optical loss of approximately 10 dB can be expected. By using a large NA fiber and refractive index matching techniques this value can be improved substantially.

This same coupling efficiency may be achieved with the on-wafer approach if a one piece light pipe with no losses at the right angle bend is developed for that approach.

Section 5

OPTICAL MODEL – AADC

The latter portion, or phase, of this program effort was devoted to designing, building, and testing a representative LIT intercommunicating mockup.

5.1 PURPOSE AND GROUNDRULES

The purpose of the mockup was to demonstrate light channeling capability for this application and evaluate potential problems associated with the concept as proposed. The basic groundrules required that the model incorporate a minimum of two LSI type modules and that it demonstrate operation of at least one duplex data link.

5.2 DESIGN AND DESCRIPTION

The high-speed LIT model was designed to simulate a small five-module LSI type AADC machine. It is equipped to accept three active and two passive modules. The modules are configured to approximate the size and shape of the actual proposed AADC modules. A standard backpanel type arrangement is provided in the base of the unit into which printed circuit board type receptacles are mounted to allow the modules to be plugged into common power and ground terminations. The receptacles also provide mechanical polarization for each of the active modules. The passive modules are positioned between each active module to increase the distance between intercommunicating modules, thus simplifying fabrication of the unit side panels and the fiber optic cables. Data input, enable and load switches, as well as a power input receptacle are mounted into the front cover of the unit. The rear cover has the eight LED displays mounted into it. Figure 5-1 illustrates the unit with one module removed. Transparent plastic covers are fastened over each of the fiber optic cable wells provided in each side panel. A clear cover is also fastened to the top of the unit to allow viewing of the principal of operation.

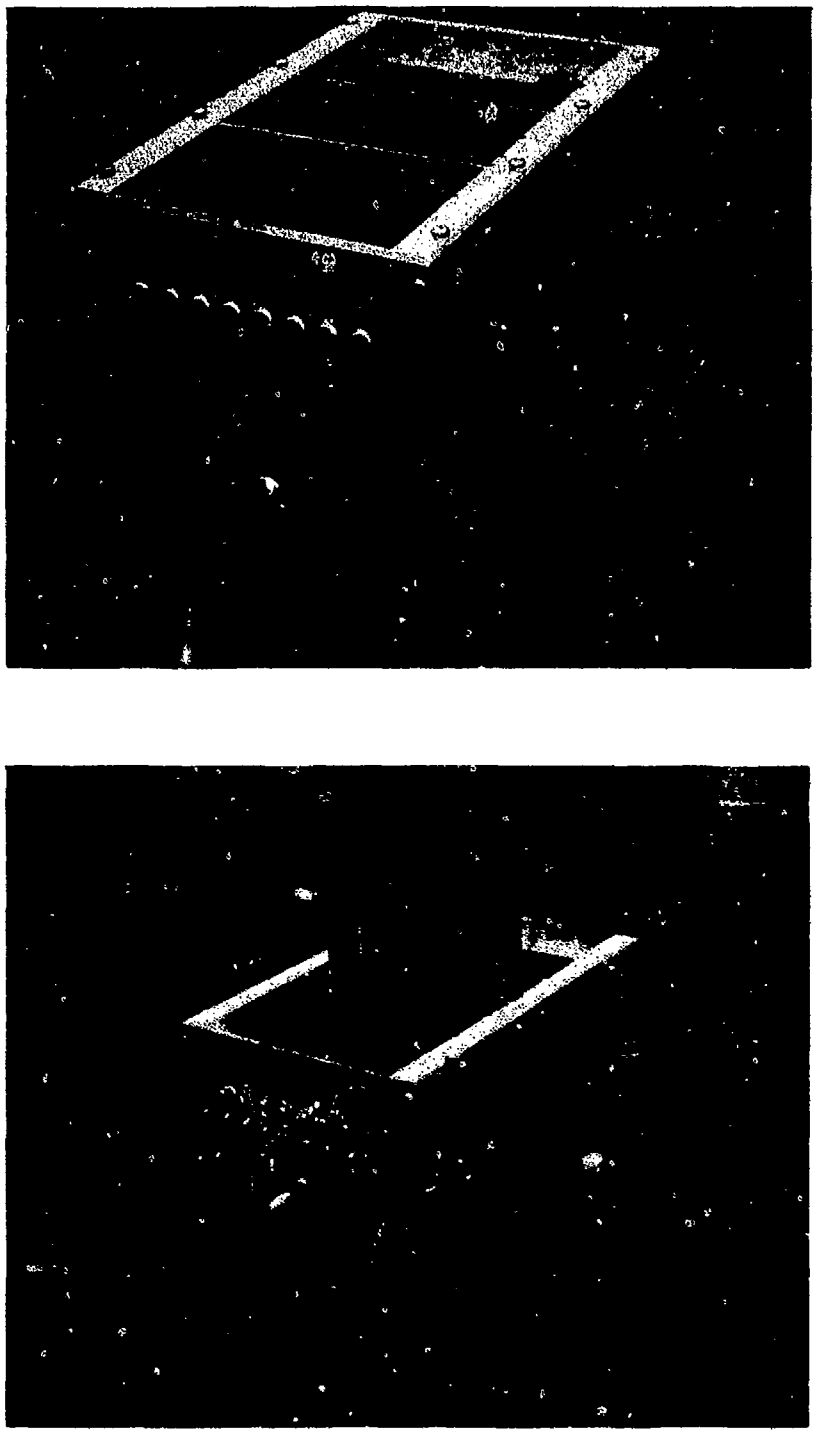


Figure 5-1. High-Speed LIT Model — AADC

5.2.1 MECHANICAL AND OPTICAL DETAIL

The basis of the optical intercommunication concept between modules is in the design of the side panels and the respective diode blocks that are mounted on each module. The design closely parallels the off-wafer concept discussed earlier in this report.

The inside surfaces of the side panels have vertical slots machined on 0.938-inch centers to accept a 0.062-inch wide printed circuit card. The circuit card (in simplified form) represents the module substrate. It also provides the mounting for all associated discrete circuit components and the diode blocks. The grooves maintain spacing between modules, but more important, they provide for the horizontal alignment between the TX and RX LEDs and appropriate optical cables that are plugged into the outside of each side panel. Each optical cable is the same length and is terminated at each end with a shouldered ferrule. Hence, the cables can be plugged into any set of holes within the drilled hole matrix provided in each side panel. This was done to demonstrate both the building block and common parts features that can be built into this type of machine. Vertical alignment of the LED cable interface is provided automatically by appropriate registration of the diode block to the backpanel support plate whenever a module is inserted and seated into the unit.

The three active modules are equipped with appropriate transmitter and receiver LEDs mounted in special holders attached along both vertical edges of the module. All associated drive, logic, and timing circuit components are mounted onto each individual card along with their appropriate LEDs such that each module is electrically a stand-alone assembly. The modules are approximately 4.00 in^2 excluding the projecting power tab. A close-up view of a module is shown in Figure 5-2. The overall unit package size measures 6.0 inches wide by 5.1 inches high by 7.0 inches long.

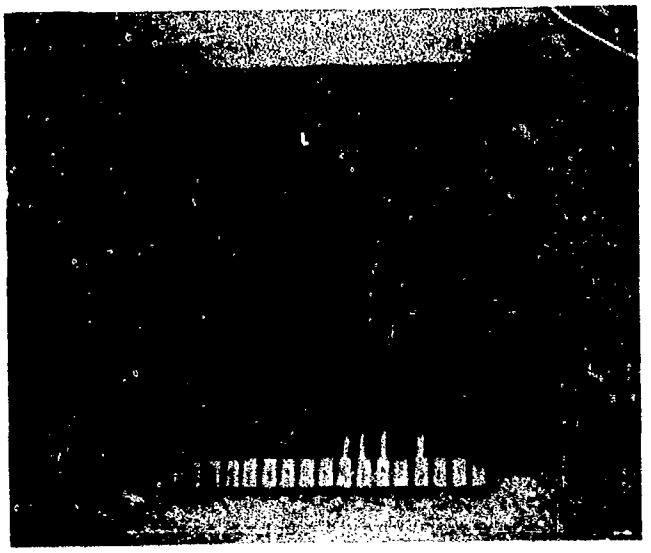


Figure 5-2. Module— High-Speed LIT Model, AADC

5.2.2 ELECTRICAL SYSTEM

The electrical system consists of three active modules which interface with each other via fiberoptic data links. Each module contains a single printed circuit card and all components associated with a module are mounted on their own cards. No electrical wires carrying data or clock signals run between the three cards. The three modules comprising the electrical system are the input module, the clock module, and the output module. Configuration of the system is shown in Figure 5-3. In Figure 5-3 the three horizontal, close-spaced lines running between the light transmitter and receiver blocks represent the fiberoptic links.

The input module contains a parallel-to-serial eight-bit shift register in which data is entered via the eight data switches mounted on the from panel. The transmitter and receiver circuits used throughout the system convert logic signals to light pulses (T blocks) and light pulses to logic signals (R blocks).

Control of the data transfer from the input module to the output module is accomplished by the clock module. This module contains a 20-MHz clock oscillator and two sets of control logic. The control logic circuits are used to generate two series, or bursts, of eight clock pulses for operating the input and output shift registers. The timing between the start of the two series of pulses is critical, and is dependent

on the propagation delay in the data between the input and output shift registers. Propagation delay times will vary between components and therefore cannot be accurately established during the design phase. However, provisions are built into the circuits to set the timing between the start of the two clock bursts.

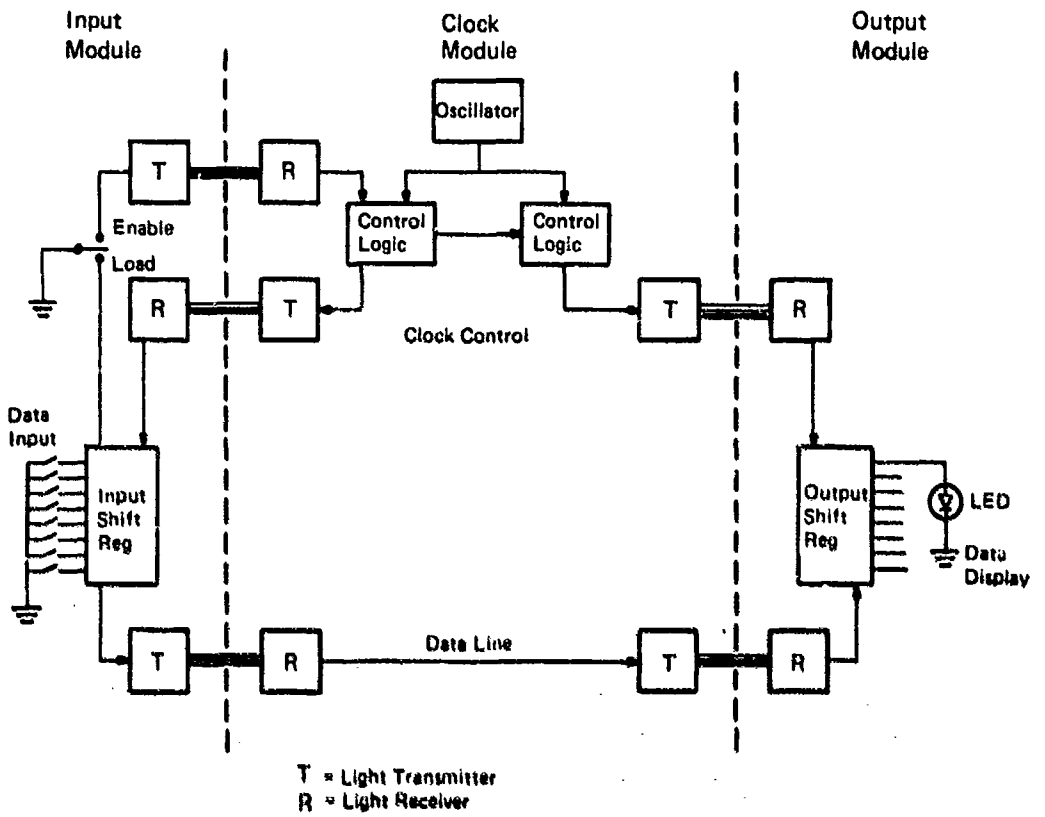


Figure 5-3. System Logic and Data Flow

The output module contains a serial-to-parallel shift register for reconstructing the data word to its original form. Eight light emitting diodes are mounted on the back panel for display of the data word.

5.2.3 SYSTEM OPERATION

A data word is entered into the system by placing the eight data input switches in their appropriate 1 or 0 position and then depressing the enable/load switch to the load position. This inserts the eight-bit parallel word into the input shift register. When the enable/load switch is depressed to the enable position a pulse is generated and transmitted to the clock module. The control logic takes over and the first series

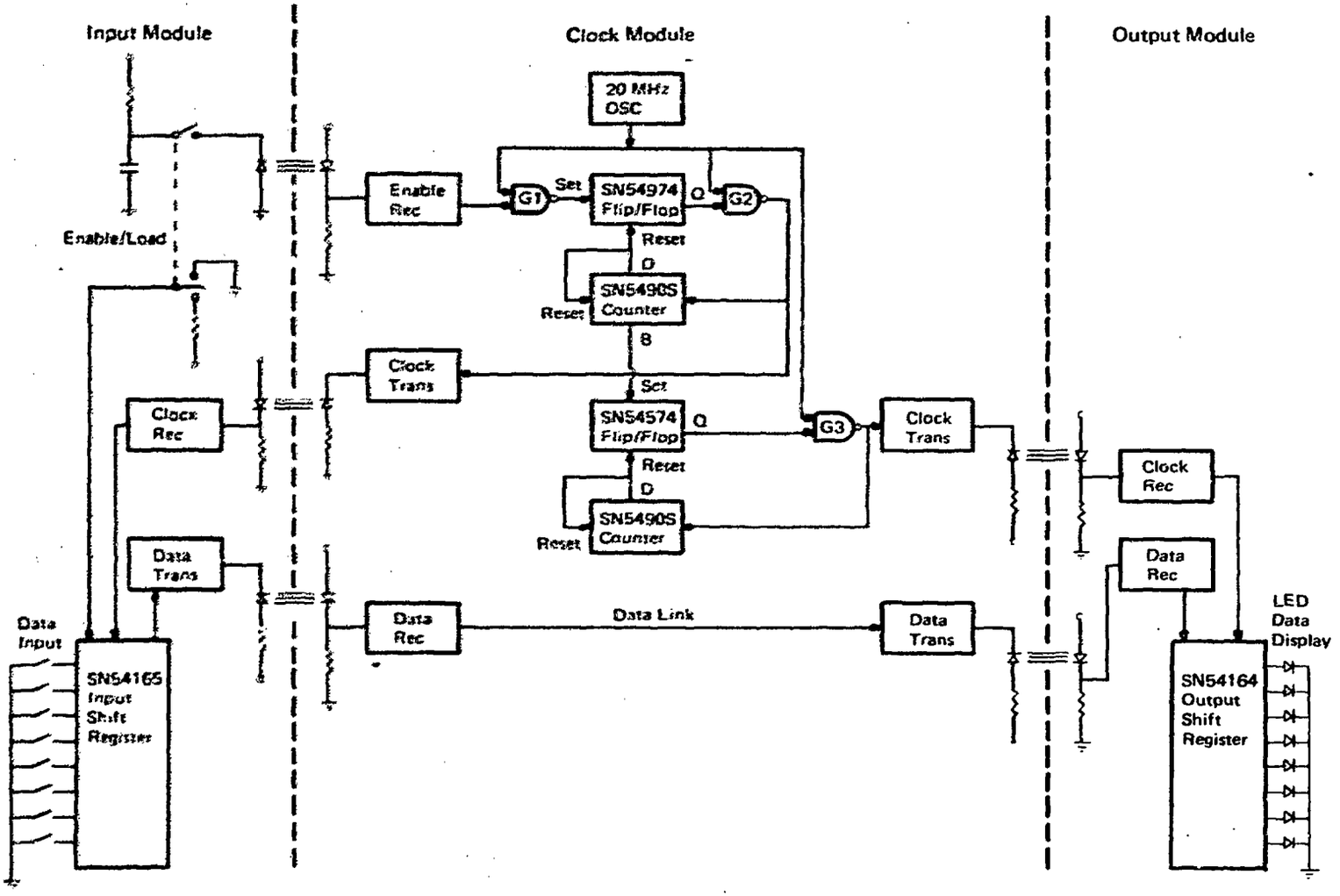


Figure 5-4. Simplified Logic and Data Flow

of clock pulses is generated and transmitted back to the input module. The clock pulses, as they enter the input shift register, shift the stored data word out in serial form. The data is then transmitted over the data line to the output shift register. Here the data must be shifted out as soon as it arrives. This is done by the proper timing of the second set of clock pulses transmitted to the output shift register. After the input data has been shifted out, the data is now stored by the register and can be read by the light-emitting diode word display.

5.2.4 CIRCUIT DESCRIPTION

5.2.4.1 Clock Control Circuits

A simplified logic and data flow diagram is shown in Figure 5-4. This figure will be used to describe the system logic.

When the enable/load switch is depressed to the enable position a capacitor discharge circuit generates a short-duration light pulse which is transmitted to the clock module. At the clock module this pulse is detected and converted to a 50-ns wide logic level pulse by the clock enable receiver circuit. This pulse is used to start the clock control logic into its sequence of operation.

The output of the enable receiver is fed to one input of the nand gate, G1. When a pulse from the 20-MHz clock oscillator is coincident with the enable pulse at G1, a pulse appears at the output of G1. This pulse is used to set the Q output of the SN54S74 flip/flop to an up level state. As long as the Q output is in an up level, clock pulses are gated through the nand gate, G2. The clock pulses leaving G2 are transmitted back to the input module where they shift out the data stored in the input shift register. The Q output of the SN54S74 flip/flop remains in the up level only long enough for eight pulses to be transmitted, otherwise the data stored in the input register would be shifted out repeatedly. Return of the Q output to a low level is accomplished by resetting the flip/flop with a pulse that occurs just after the 8th clock pulse is transmitted through G2. The SN5490S decade counter is used to provide the required reset pulse. The count sequence of the SN5490S is given in Figure 5-5a. The D output, at which a pulse occurs after the 8th count, is used to reset

the flip/flop. Timing of the reset pulse can be obtained from Figure 5-5b. The same pulse used to reset the flip/flop is used to reset the counter, making it ready to receive a new series of pulses.

A second set of eight pulses is generated in a manner similar to the set just described. This group of pulses is transmitted to the output shift register, but is delayed by an amount approximately equal to the propagation delays incurred through the data link circuits. This delay is necessary because the data must appear at the output register just before the clock signals arrive. On breadboarding these circuits a delay in the order of 100 ns was found to be needed.

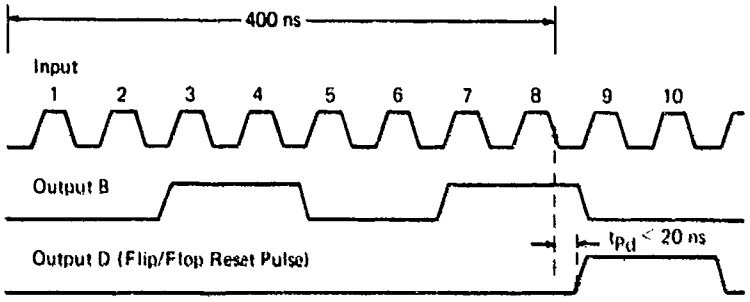
The delay in generating the second group of clock pulses is accomplished by selecting one of the decade counter outputs to set the Q output of a second flip/flop circuit. This flip/flop is used to control the gate time of G3. A second decade counter is then used to reset the second flip/flop back to its initial state after the 8th pulse has been gated over G3.

The count sequence given in Figure 5-5a shows the various outputs that can be used (either singularly, or in combination) to start the second group of clock pulses. Since the counter operates at the 20-MHz clock rate, each successive count provides a delay in 50-ns steps. An additional 18 to 20 ns delay results from the propagation time between the input and the desired output pulse. Thus, from output B we can obtain a delay of approximately 120 ns, which provides the required delay time. From output B we note that two pulses are generated before the counter is reset (Figure 5-5b). This does not cause any problem since only the first pulse received by the SN54S74 triggers the flip/flop. Additional inputs are inhibited until the flip/flop has been reset.

A chart showing the overall system timing sequence is shown in Figure 5-6.

Count	Output			
	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	1
9	1	0	0	1

a. SN5490S Count Sequence



b. SN5490S Input-Output Switching

Figure 5-5. Count Sequence and I/O Switching

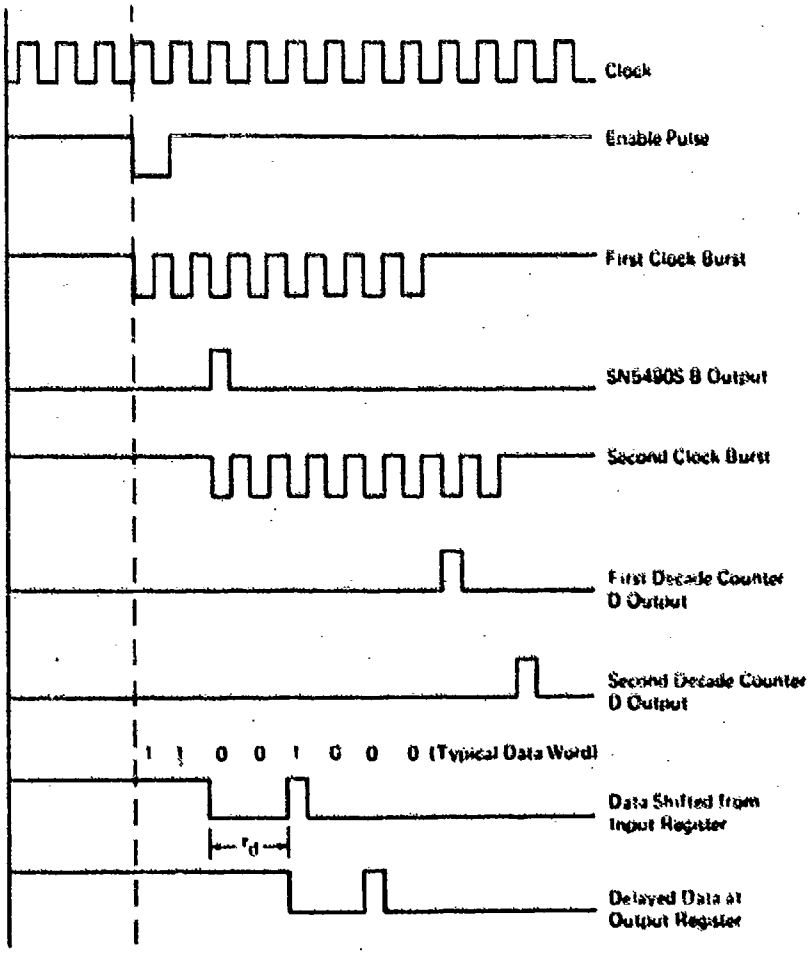


Figure 5-6. Logic Timing Sequence

5.2.5 POWER REQUIREMENTS

The AADC requires three power supplies for operation. The power requirements and special precautions are as follows:

Connector Pin	Voltage	Current	Cable Color
A	+5 ±0.2 V	1 A	Yellow
B	+5 return*		White
C	-5 V	50 mA	Blue
D	-5 return*		Brown
E	-50 V return*		Red
F	-50 V	10 mA	Black
G	do not use		Green

*Do not connect together or apply an external ground to the AADC unit.

Section 6

SUMMARY

6.1 SIGNIFICANT RESULTS

A summary of the significant items discussed in this paper are as follows:

1. A survey and evaluation of state-of-the-art LED light sources indicates that diode structures, specifically the type used for laser operation produce faster risetimes than do conventional LED structures. This appears during operation of the laser in a spontaneous emission mode where the risetime improves as a function of increased current density. Conventional LED structures do not appear to exhibit this same improvement with increases in current density. The results of this evaluation indicate that, with further materials and device development, the fabrication of very short risetime LEDs for use in high data rate communication systems is possible.

2. A current evaluation of PIN diode applicability to optical data links indicates that state-of-the-art PIN diodes exist that meet the requirements of spectral response, spectral sensitivity, and risetime to allow speeds up to 200 MHz in the AADC application. The devices are compatible with circuit load resistor requirements and can be used with amplifiers suitable for use in a digital computer environment.

3. A study of optical device packaging and interconnection concepts established development of a feasible optical/mechanical systems approach. The system utilizes a one-receiver for one-transmitter concept on the module, with communication between modules accomplished via fiber optic cables located along both sides of the modules. Further development of the module configuration suggested a trade-off

study of both an on-wafer LED and off-wafer LED design. The trade-off results indicate that the off-wafer concept is the most efficient and cost effective approach. However, selection of either concept is primarily dependent upon the data rate required and prevailing economic considerations.

4. An operating 20-MHz optical data link model was constructed. The model simulates a small five-module LSI type AADC machine. The model employs off-the-shelf integrated circuits in logic-in logic-out interface and allows manually selected inputs to be transmitted through the modules via the light guiding techniques proposed in this report.

6.2 RECOMMENDATIONS

Based on the results of the work reported here, it is recommended that future development be done in the following areas:

1) Preliminary results of the risetime data taken on heterostructure LEDs indicate that risetimes of less than 2 ns can be achieved. Further work however, must be done in device development and characterization. The work must also concentrate on optimizing the device optical power output as well as speed.

2) Dual mode operation (same diode can be dynamically switched from emission to detector operation by appropriate electronic circuit control) of the GaAs diode will significantly reduce optical complexity and allow for more flexibility. Considerable development work on this type of device is still required. Feasibility has been demonstrated (Reference 2) at reduced speeds.

3) The packaging and mounting of the diode itself should be considered in more detail. Emphasis should be given to optical efficiency, thermal design, interconnection techniques, device mounting, etc. This effort will yield a device suitable for the AADC module optical interconnection.

4) The design and development of a second level package (AADC module) incorporating the off-wafer optical communication technique. This will allow development of prototype hardware which can be used for evaluation of performance and potential problem areas.

5) Further consideration and design should be accomplished in the final (unit) level of packaging. This includes design of the overall structure with cooling provision, optical fiber interconnection, and fixed alignment features, etc.

The above list of recommendations is intended to take the optical communication technique proposed for the AADC, from a laboratory feasibility stage to a prototype model. The intent of the model will be for exploratory evaluation in a military environment.

Section 7

REFERENCES

1. "High Speed Optical Data Links - Final Report" - Contract No. N00019-71-C-0345, Dated 13 March 1972.

2. Mohr, R.J., "Coupling Between Lines at High Frequencies", IEEE Transactions on EMC, Vol EMC-9 No 3, Dec 1967, pg 127.

3. Catt, I., "Cross Talk (Noise) in Digital Systems", IEEE Transactions on Electronic Computers, Vol EC-16 No 6, Dec 1967, pg 743.

4. Mohr, R.J., "Coupling Between Open and Shielded Wire Lines Over a Ground Plane", IEEE Transactions on EMC, Vol EMC-9 No 2, Sept 1967, pg 34.

5. Dettloff, T.N., "Multilayer Interconnection Boards for VHF Circuitry", IBM Federal Systems Division, Electronic Systems Center, Owego, New York, 1972 Electronics Components Conference, Washington, DC, pg 252.

6. Sear, P.E., "Packaging for High Frequency", The Electronic Engineer, July 1972, pg 20.

7. Mohr, R.J., "Interference Coupling - Attack It Early", EDN, 1 July 1969, pg 33.

8. Skolnik, Introduction to Radar Systems, pg 34.

9. Kreidl, N.J. and Rood, J.L., Optical Materials and Coatings.

10. Crystal Products Bulletin - Union Carbide Corp., Bedford, Mass.

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R.L. Williams Texas Instruments Co. 13500 N. Central Expsy. P.O. Box 5474, M.S. 262 Dallas, Texas 75222	1
C. Yea University of California Los Angeles Los Angeles, California 90024	1

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Armand D. Damari, Roy C. Clapper
Harold H. Bloem, Henry C. Farrell
Daniel J. Stigliani, Jr.

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13. ABSTRACT

An investigation of the use of optical communications for interconnecting AADC modules is performed. Both system and optoelectronic device studies are performed. An investigation of various light sources (primarily light emitting diodes (LEDs) and injection laser diodes) and photodetectors (silicon and germanium photodiodes (PDs), phototransistors, etc.) is performed, and the properties of these devices are analyzed. The most appropriate light emitters for near term applications are GaAs LEDs and heterostructure (or Large Optical Cavity) injection lasers for future applications. Silicon PIN photodiodes meet the present photodetectors' requirements for the AADC, or avalanche photodiodes can be used where photocurrent gain and/or larger bandwidths are required. A study of mounting techniques for the LEDs and PDs is performed with respect to the mechanical and optical properties of the devices. This investigation yielded two general configurations, on-wafer and off-wafer. Even though the on-wafer approach may result in somewhat higher speed capability, the mechanical and optical complexity involved indicates that the off-wafer mounting of the optoelectronic devices is presently a more feasible and economical approach. Various conceptual designs of optically interconnecting the AADC modules are investigated. A candidate configuration is established where the optical path extends from the optoelectronic devices to the edge of the module via a light guide and is routed to another module via fiber optics which is located in the side panels. A theoretical analysis of the light coupling losses at the fiber/fiber interface is performed and experimental data taken. The light coupling losses as a function of air gap and misalignment indicate that reasonable tolerances will not substantially affect the coupling efficiency. A prototype model of a five module AADC was fabricated and tested. The model contains three optically active modules, and data is transferred at a 20-MHz rate. The model is discussed

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