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HIGH SLEW RATE OPERATIONAL AMPLIFIER

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Texas Instruments Incorporated

TECHNICAL REPORT AFAL-TR-73-144
May 1973

Air Force Avionics Laboratory
Air Force Systems Command
Wright-Patterson AFB, Ohio 45433

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HIGH SLEW RATE OPERATIONAL AMPLIFIER

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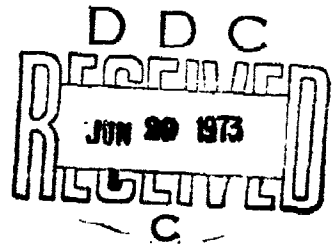

FOREWORD

The technical effort discussed in this report was accomplished under the sponsorship of the Air Force Avionics Laboratory, Contract No. F33615-72-C-1246, Project No. 6096, Task No. 609601, with Mr. James J. Enright, AFAL/TEA, as the Technical Monitor for the Air Force.

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The authors wish to express their appreciation for the excellent technical support given this program within Texas Instruments. Special recognition is particularly due the efforts by Mr. Farris Malone of Special Circuits and by Mr. Jack Ellis of Semiconductor Research and Development Laboratories. Their work was most important to the successful completion of this program.

ROBERT D. LARSON
Chief, Advanced Electronic Devices Branch
Electronic Technology Division
Air Force Avionics Laboratory

ABSTRACT

A high-performance, monolithic operational amplifier has been designed and developed. It incorporates the latest state-of-the-art circuit design techniques and fabrication technology to achieve the best performance available with current production processes. Special attention was placed on achieveing high slew rate and fast settling time. Unity gain slew rates of over 2500 V/μsec and settling times of under 50 ns were achieved at power dissipation levels of approximately 100 mW. The design was kept as simple as possible to eliminate excess parasitic capacitances and to be operated at the optimum power-speed condition for a given application.

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SECTION I
INTRODUCTION

The objective of this program has been to develop a fast operational amplifier for use in high-speed, data-handling systems. Operational amplifiers are often used as buffer amplifiers or voltage followers in such systems and are a major factor in limiting system speed. An operational amplifier with very high slewing rates and fast settling time has been developed using the best available technology in both circuit-design procedures and monolithic-fabrication processing. The performance achieved will allow areas of research to be determined which will result in further improvements in circuit performance.

The amplifier developed at Texas Instruments is of monolithic construction, fabricated with a complementary bipolar, dielectric-isolation process which allows the formation of vertical NPN and PNP transistor structures. The dielectric isolation is used to minimize parasitic capacitances which contribute to propagation delays and increased transition time.

The circuit was designed to be as efficient as possible in order to maximize performance with the smallest number of components. The circuit uses only one gain stage plus input and output stages, which results in both high speed and low-power consumption.

Achieved performance was unity gain slew rates in both positive and negative directions of over 2500 V/μs at a power dissipation of 100 mW. The unity gain bandwidth was greater than 50 MHz and was unity gain stable with no internal or external capacitors. The d-c gain was above 70 dB.

The design and fabrication of the X776 operational amplifier has achieved slew rates obtainable only in hybrid form up to this time. Hybrid amplifiers are bulky, expensive, and consume high power. The X776 is of monolithic construction and has all the reliability and economic advantages attributed to this technology. This amplifier should enhance data-processing systems that require high-speed operational amplifiers.

SECTION II
TECHNICAL DISCUSSION

A. DESIGN PROBLEM

The increased use of operational amplifiers to handle data in digital computers demands an amplifier that has high-speed switching characteristics. A typical application is the introduction of a rapidly changing signal to a buffer amplifier which must faithfully reproduce the input with a high degree of accuracy within a time frame of nanoseconds. Applications requiring fast settling time and slew rate to a high degree of accuracy are typified by Sample-Hold circuits, Multipliers, and Analog-to-Digital (A/D) and Digital-to-Analog (D/A) converters. The speed of the amplifiers used in these circuits determines the maximum data or information-transfer rate for a given accuracy. The buffer amplifier is, in many cases, the major limitation for over-all system speed.

Commercially available circuits up to this time having high slew rates and fast settling time were in hybrid form. The major disadvantages of these circuits are power, size, costs, and reliability. The objective of this program was to exceed the performance of these hybrid circuits by using a high degree of monolithic integration. Inherent in monolithic integration is improved cost, reliability, and size. Power and speed were an optimized trade-off.

The utilization of operational amplifiers in high-speed D/A and A/D converters implies that the basic amplifier must be fast compared to the conversion speed. The amplifier essentially determines the maximum data or information rate for a given accuracy. The amplifier in this system application is generally used for impedance buffering. This is one of the most demanding applications because the amplifier operates with 100% feedback, and the input stage must operate with its rated common-mode voltage without loss of linearity. The buffer amplifier is shown in Figure 1. The gain accuracy and linearity of such a unity-gain buffer are limited by the open-loop gain and the common-mode rejection of the amplifier.

The objective of this program was the design, development, fabrication, characterization, and evaluation of a high slew rate, fast settling operational amplifier. The amplifier was designed to be versatile and have wide system appeal, but the emphasis was on operating speed.

The amplifier was designed to have inverting and noninverting inputs. The design objectives for the operational amplifier were:

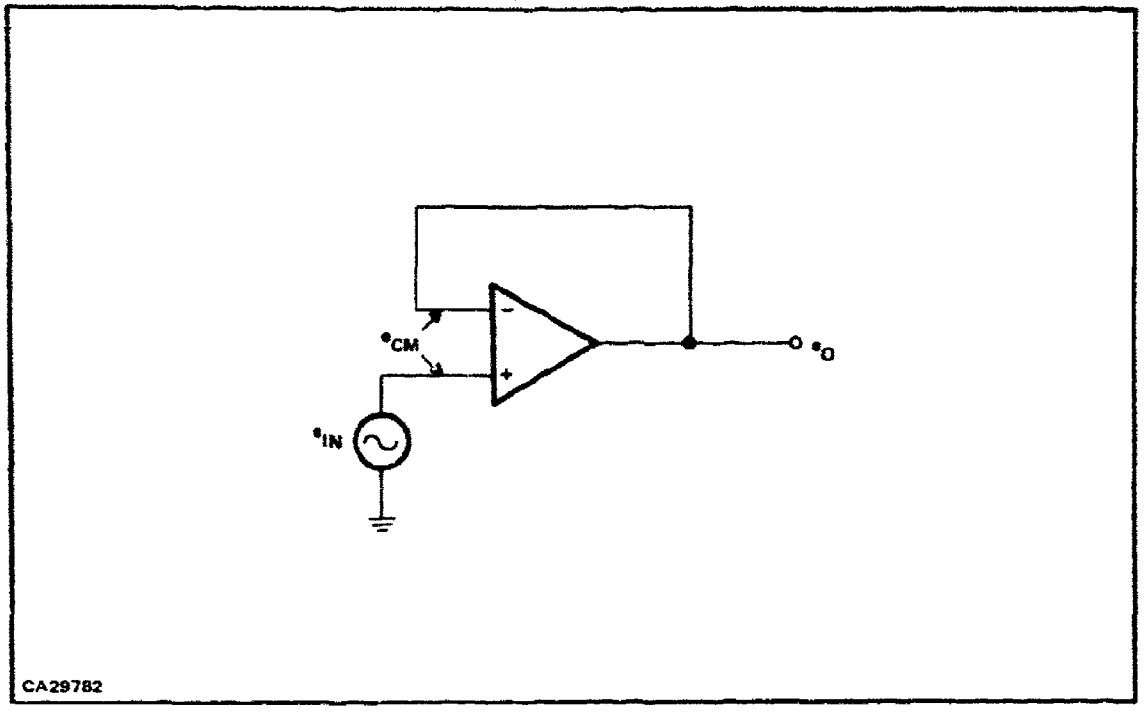


Figure 1. Buffer Amplifier

- Open-loop voltage gain: 84 dB min
- Settling time to 0.1%: 50 ns max
- Slew rate: 2500 volts/μs
- Input voltage range: ±10 volts min
- Output voltage swing: ±8 volts min
- Output current: 50 mA min
- Gain rolloff: 6 dB/octave (linear)
- Supply voltage: ±15 volts
- Operating temp. range: −55°C to +125°C
- Input Offset Drift –
  Current: 0.1 nA °C max
  Voltage: 1 μV/°C max

To achieve a low-cost, high-reliability, optimized operational amplifier, a total monolithic construction was chosen. Most commercially available monolithic integrated circuits use construction techniques that result in vertical NPN transistors and lateral PNP transistors. Lateral PNPs suffer in the area of high-frequency performance. Therefore, a bipolar complementary process (vertical NPN and PNP) was chosen. The resulting transistors allow maximum circuit performance from simple circuitry, the key to high-speed performance.

The normal monolithic integrated circuit also uses junction isolation with the resulting high parasitic capacitance. To eliminate parasitic capacitance, a dielectric (SiO_2) isolation process was selected. The combination of dielectrically isolated and complementary bipolar transistors yields a high-performance structure discussed in a later section. This structure has opened areas of circuit design not available to integrated-circuit designers until recently.

The design philosophy used in designing a high-performance operational amplifier is simplicity itself. A minimum number of stages should be used to eliminate propagation delays. The open-loop gain was somewhat sacrificed to use a single amplification stage. The amplification stage should have one dominant pole so that a unity gain stable circuit results without compensation capacitors. The compensation capacitors needed in other amplifier designs limit the attainable slewing rate. If a relatively high-gain (> 60 dB) amplifier stage can be designed that is unity gain stable without compensation capacitors, the unity gain slew rate is the same as the open-loop slew rate.

B. CIRCUIT DESIGN

The block diagram of such a design is shown in Figure 2. The design includes input buffer stages, a single-gain stage, and an output buffer stage. The input buffer stage should provide high-input impedance and low-input current. The gain stage should have moderate gain (> 60 dB) and a single high-frequency pole. The output stage should buffer the load so that it does not affect the voltage gain of the gain stage.

The design of the input buffer stage must incorporate the following design trade-offs. The stage must have large quiescent currents to charge and discharge circuit and parasitic capacitances. The input bias current should be as low as possible (< 1 μA). The Junction Field-Effect Transistor (JFET) has such qualities. The gate current (input bias current) is basically independent of source to drain current since it is the reverse bias junction leakage current. This device is the basic input stage of high-speed hybrid circuits.

The JFET has several disadvantages. High-performance JFETs are not easily obtained in monolithic construction. In addition, voltage offsets in the millivolt range are also not obtainable in high-yield circuitry. The input current, although low at room temperature, increases rapidly at high temperature; that is, it doubles approximately every 8°C. Alternatives to the JFET approach were investigated.

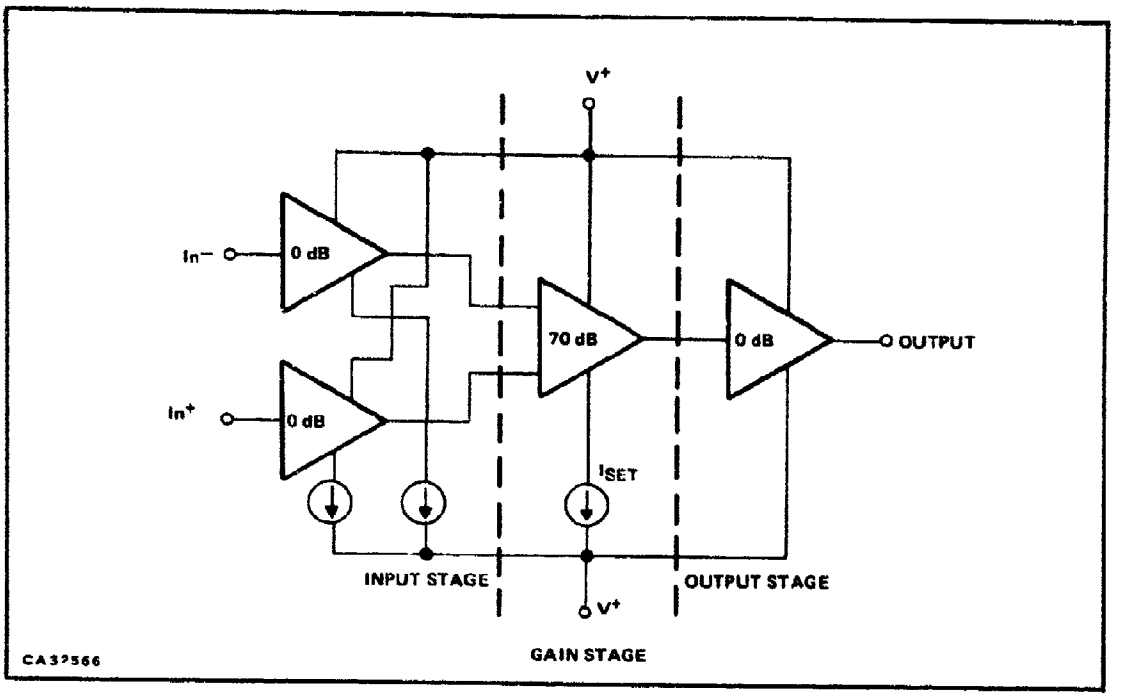


Figure 2. Block Diagram of High Speed Operational Amplifier

An approach that uses only bipolar transistors was investigated. This structure is called a composite transistor in this report. The composite transistor schematic is shown in Figure 3. The basic assumption is that the NPN transistors' current gains (betas) are matched and the PNP transistors' betas are matched. There is no need to require that the NPN and PNP current gains be matched. The operation of the circuit, using the above assumptions, can be explained as follows. The input transistor's (Q1) base current and the sense transistor's (Q2) base currents are equal if we assume matched betas and $I_C \approx I_E$, that is if the betas are high. Since the transistor bases of Q2 and Q3 are connected, the base current of Q3 is equal to the base current of Q2. Using the same assumption for Q3 and Q4, we can equate the base currents of Q3 and Q4. Therefore, the net result is that base current of Q1 is equal to, but in the opposite sense of Q4. The input current (I_{B1} -I_{B4}) is zero and does not depend on the emitter current (I_E) of the device. It approaches the same condition obtainable from a JFET.

The composite transistor circuit was evaluated as the input transistors for various gain stages. The circuits of Figure 4 and Figure 5, were breadboarded. The results are summarized in Figure 6 and Figure 7 with the constant current (I_O) as the variable. The unusual result is that an apparent zero causes the gain to level off or, in some cases, increase after the normal 6 dB/octave initial decrease. This basic effect was also predicted using computer aided design programs. The circuits of Figures 8 through 11 were simulated. The results are summarized in Figure 12.

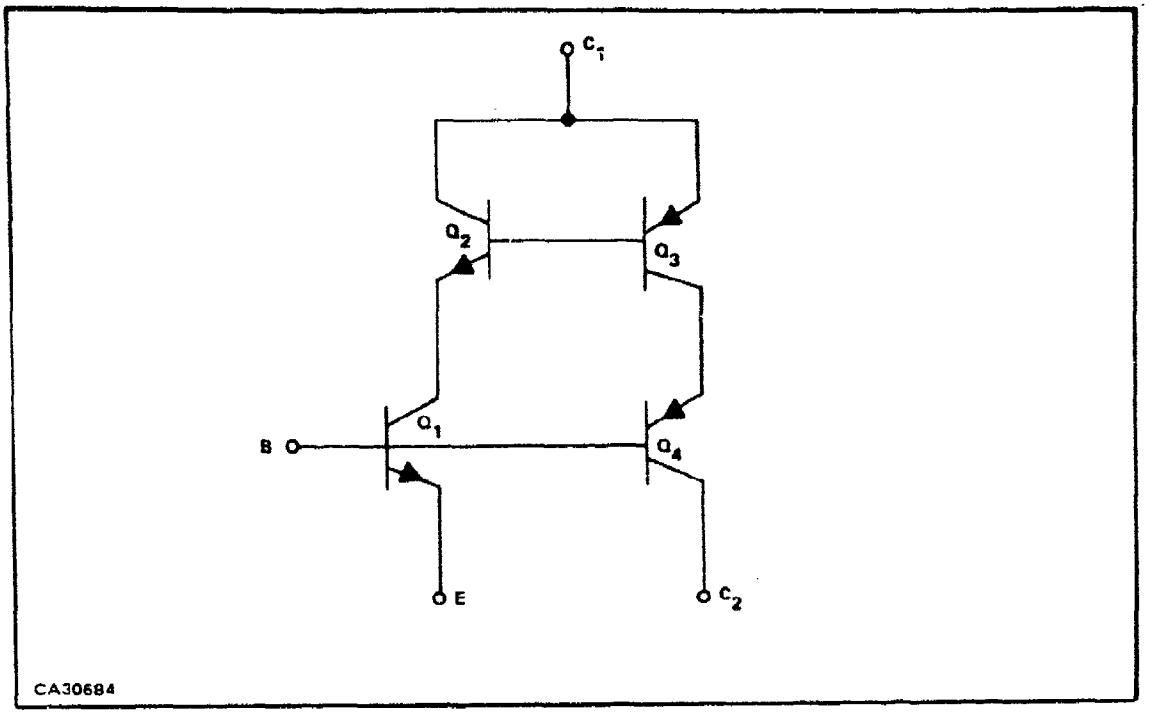


Figure 3. Composite Transistor Circuitry

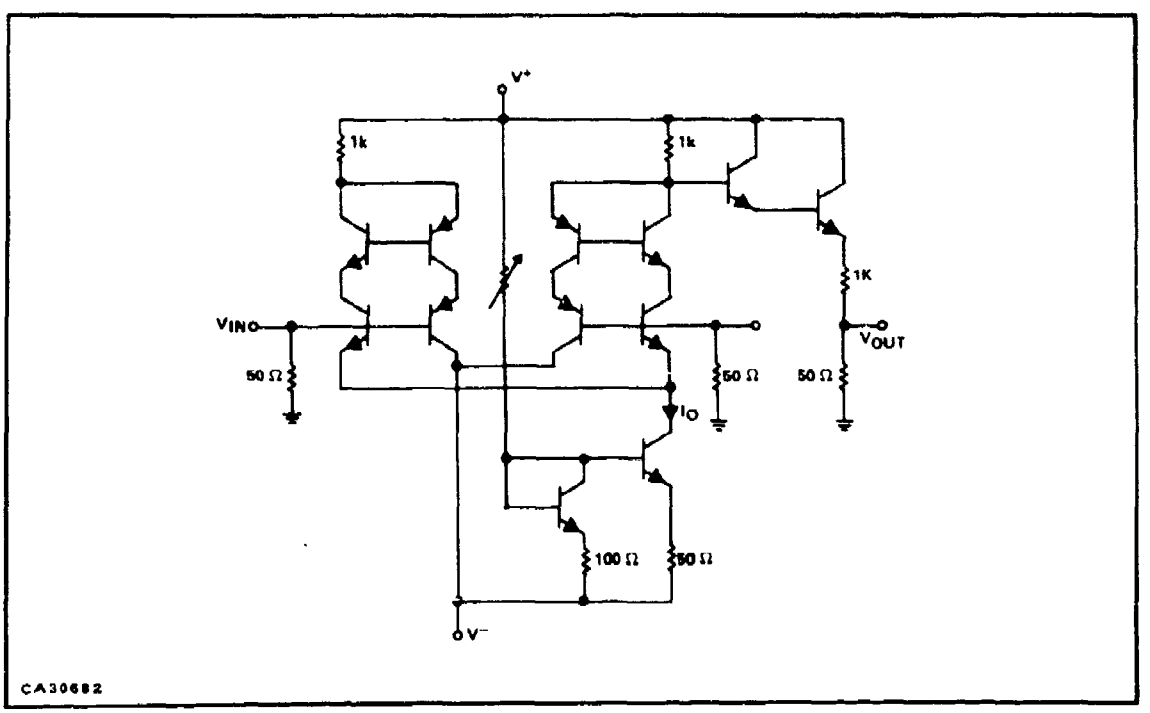


Figure 4. Differential Amplifier Using Composite Transistors and Resistive Loads

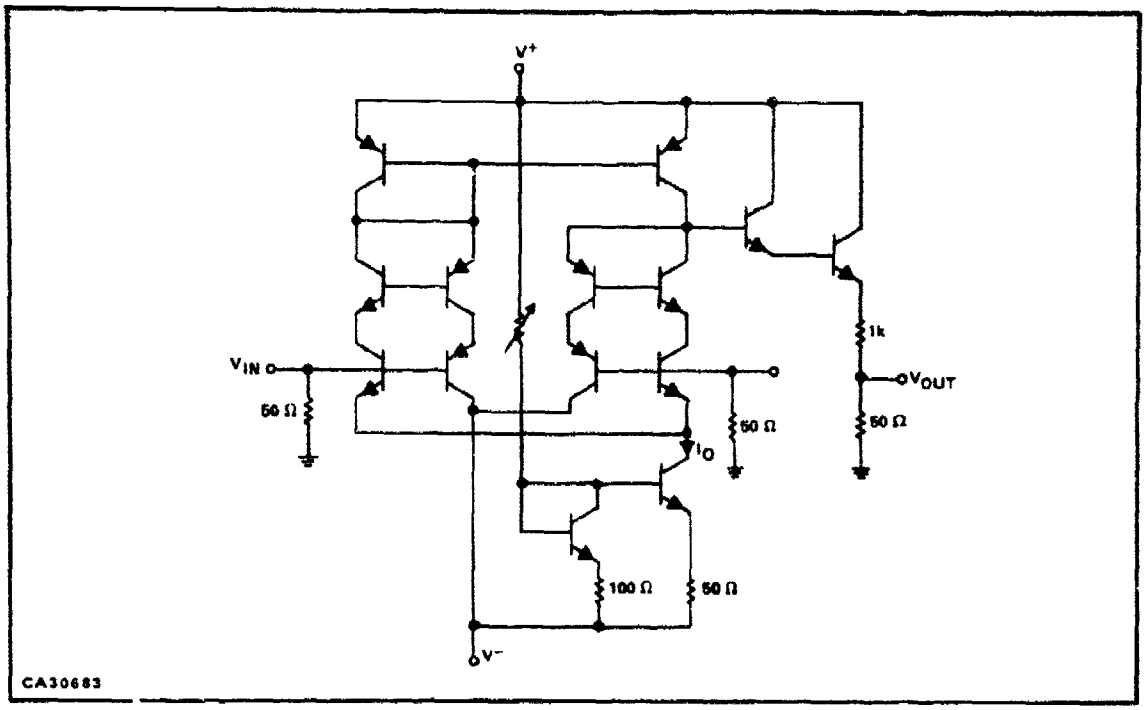


Figure 5. Differential Amplifier using Composite Transistor and Active Loads

The final approach was to use the composite transistor not in the gain stage but in the input buffer stage. The input buffer stage is shown in Figure 13. The nominal emitter current was set at 0.5 mA, as determined by the breadboard analysis. The input current and power dissipation may be improved if it can be determined that this bias current can be reduced. The reduced parasitic capacitance of the integrated circuit may make possible this improvement. The resistor R1 provides short-circuit protection for the input stage, and resistor R3 is used in the offset adjust scheme.

The basic gain-stage design is shown schematically in Figure 14. The design uses vertical PNPs to advantage. Advantages of this circuit are wide common-mode input voltage range (within 2 V_{BE}'s of the plus and minus voltage supplies), high single-stage voltage gain (70 dB), and a large voltage output swing (within 1.0 volt of the power supplies). The circuit also converts the differential input into a single-ended output without any loss in voltage gain.

The a-c frequency response of this circuit is very interesting. The response is represented in Figure 15. As the constant current (I_O) is increased, the voltage gain remains essentially constant, but the bandwidth is increased. This property of the gain stage influenced the design so that a programmable slew rate operational amplifier was built. One pin was brought out of the package so that the user could pick the operating bandwidth and power.

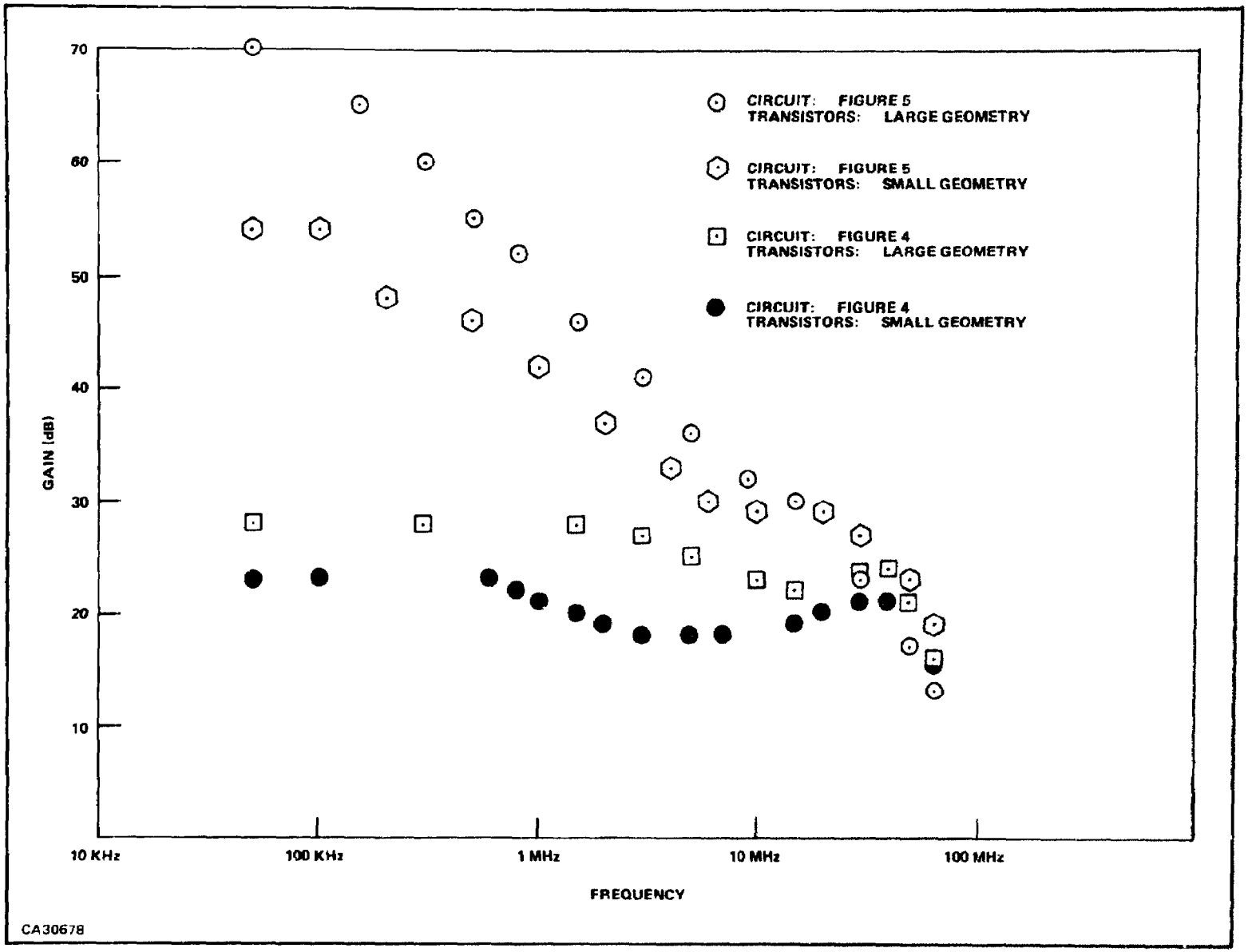


Figure 6. Gain versus Frequency (I_0 = 1 mA)

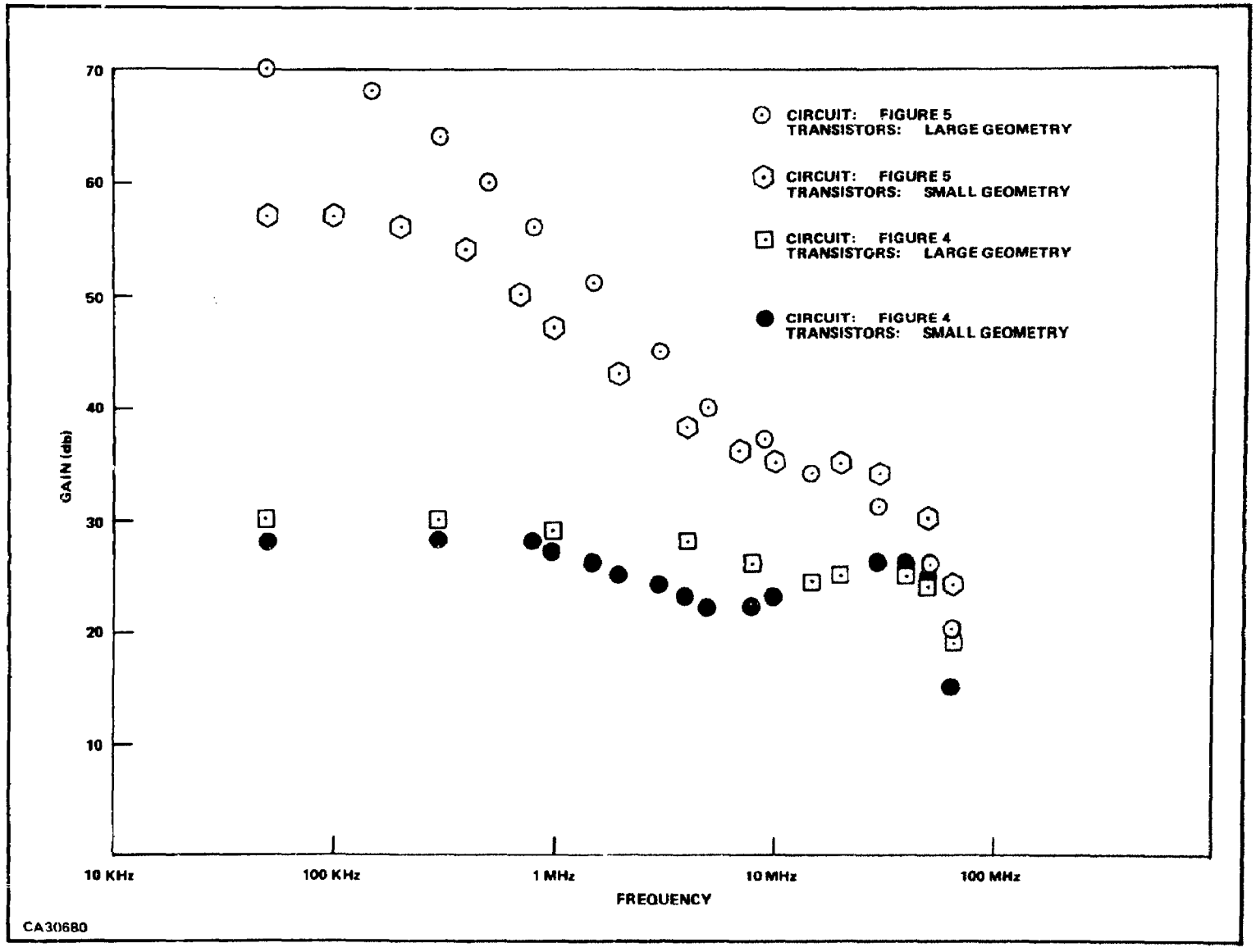


Figure 7. Gain versus Frequency (I_0 = 2 mA)

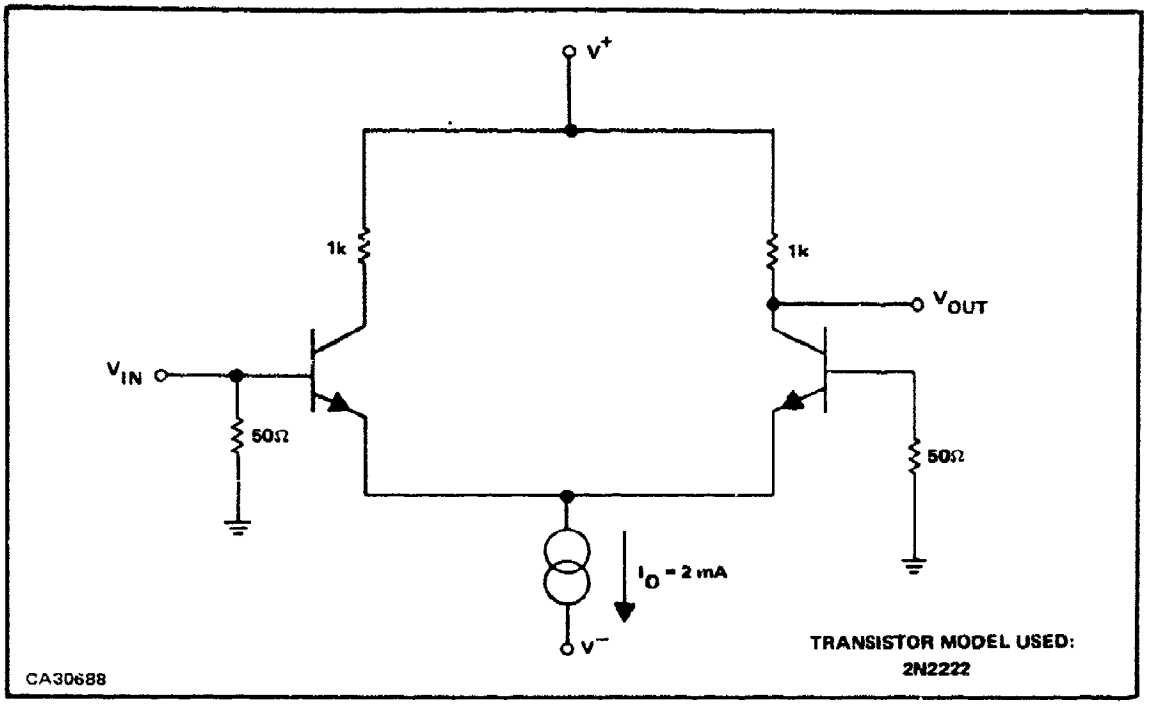


Figure 8. Circuit for Computer Modeling of a Differential Amplifier using Single Input Transistor and Resistive Loads

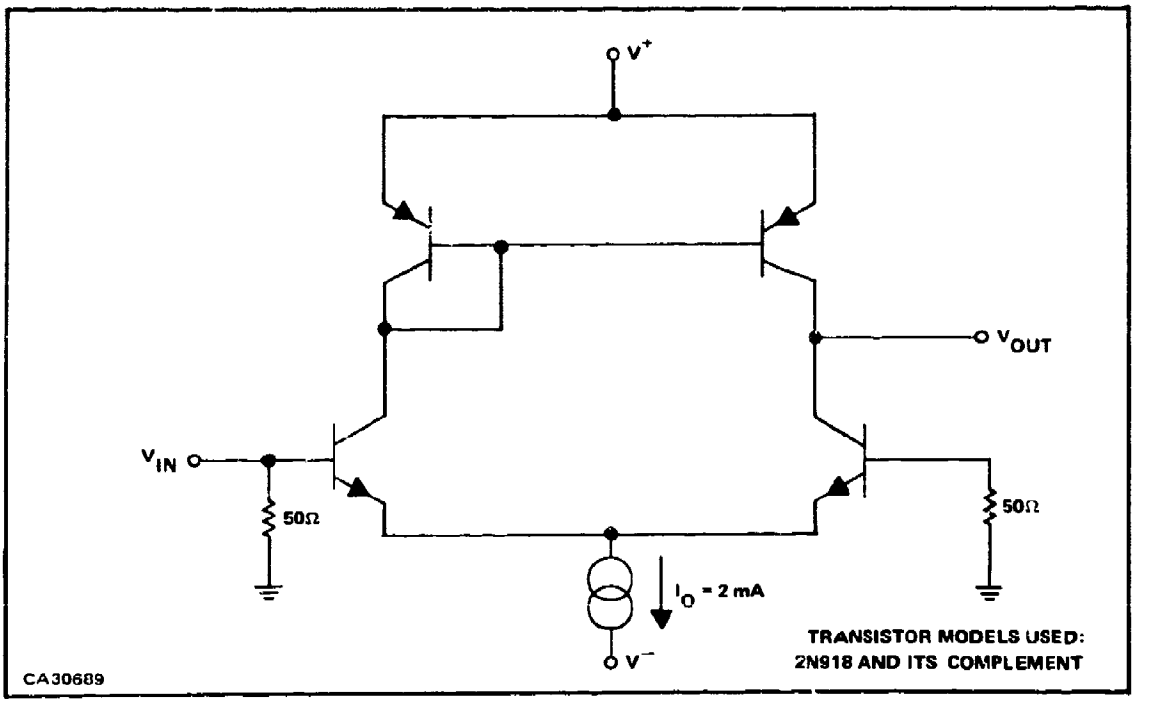


Figure 9. Circuit for Computer Modeling of a Differential Amplifier using Single Input Transistors and Active Loads

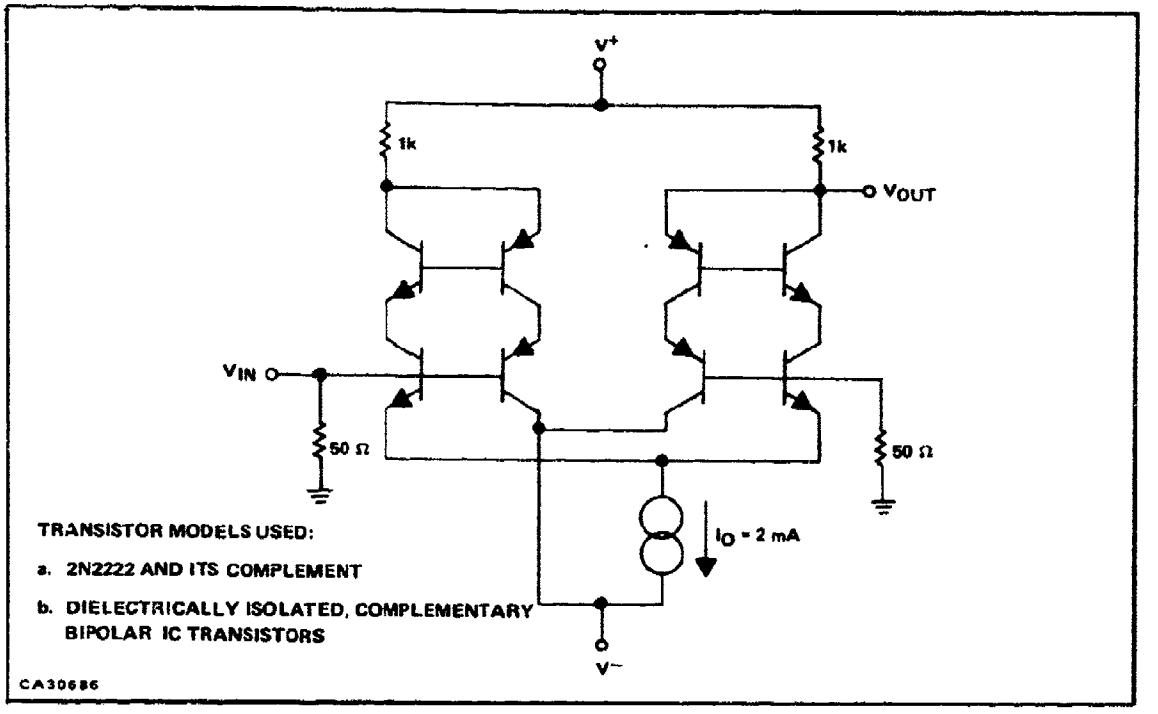


Figure 10. Circuit for Computer Modeling of a Differential Amplifier with Composite Transistors and Resistive Loads

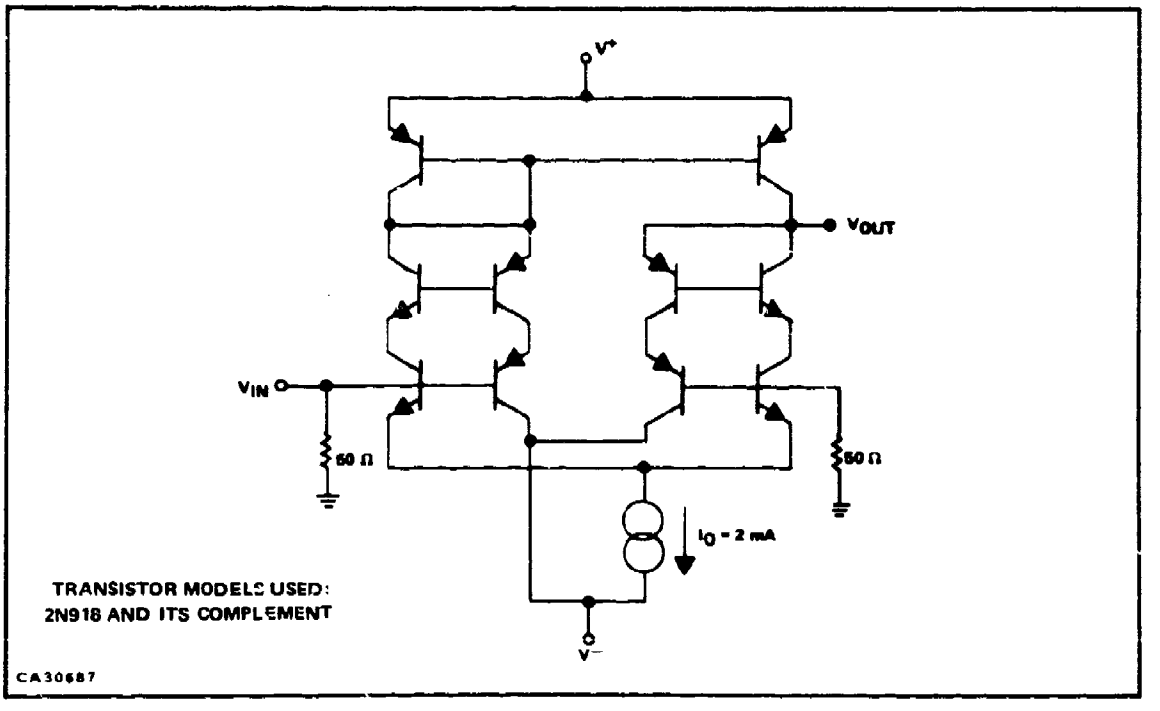


Figure 11. Circuit for Computer Modeling of a Differential Amplifier with Composite Transistors and Active Loads

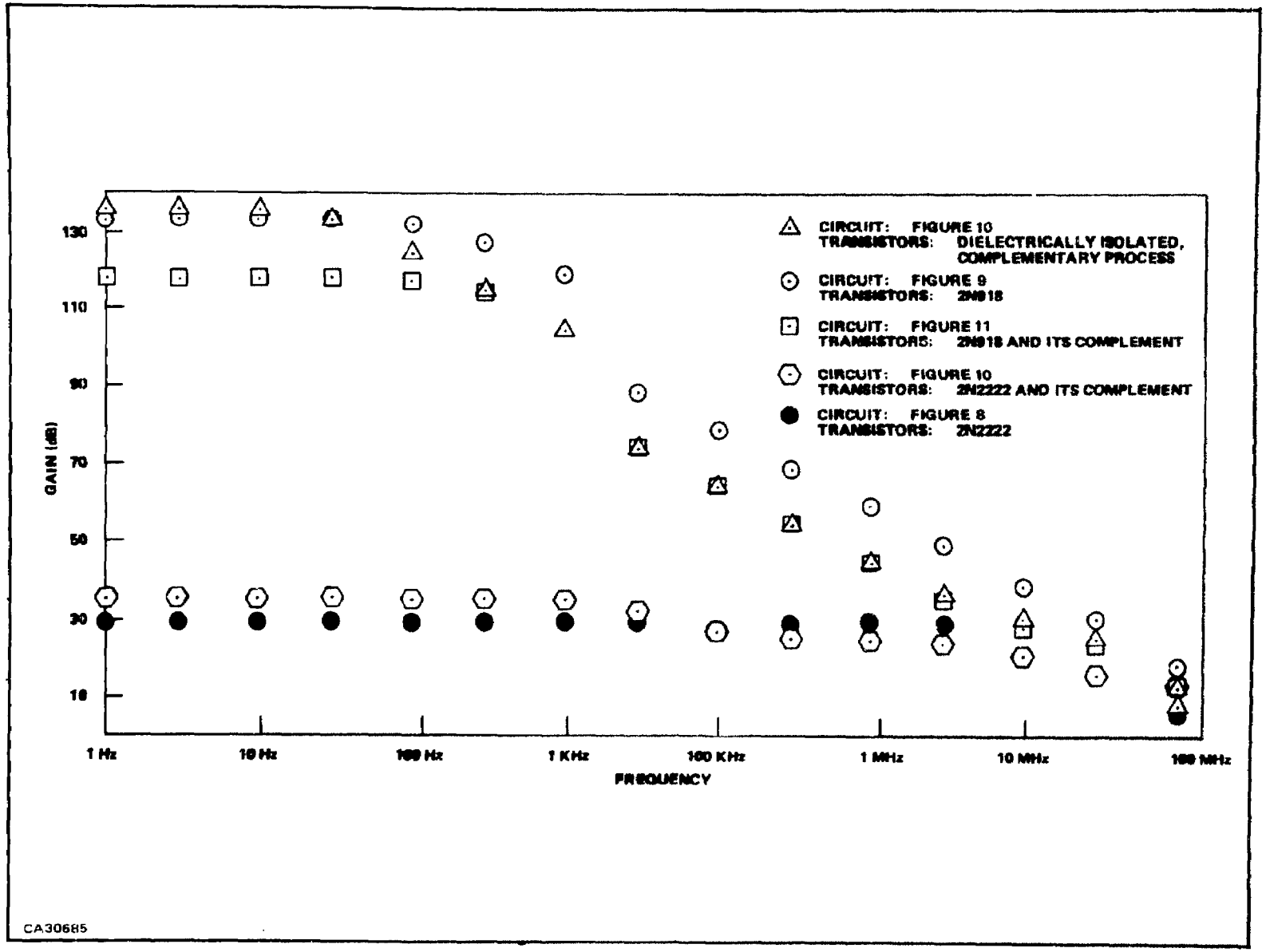


Figure 12 Computer Results of Gain versus Frequency (I_o = 2 nA)

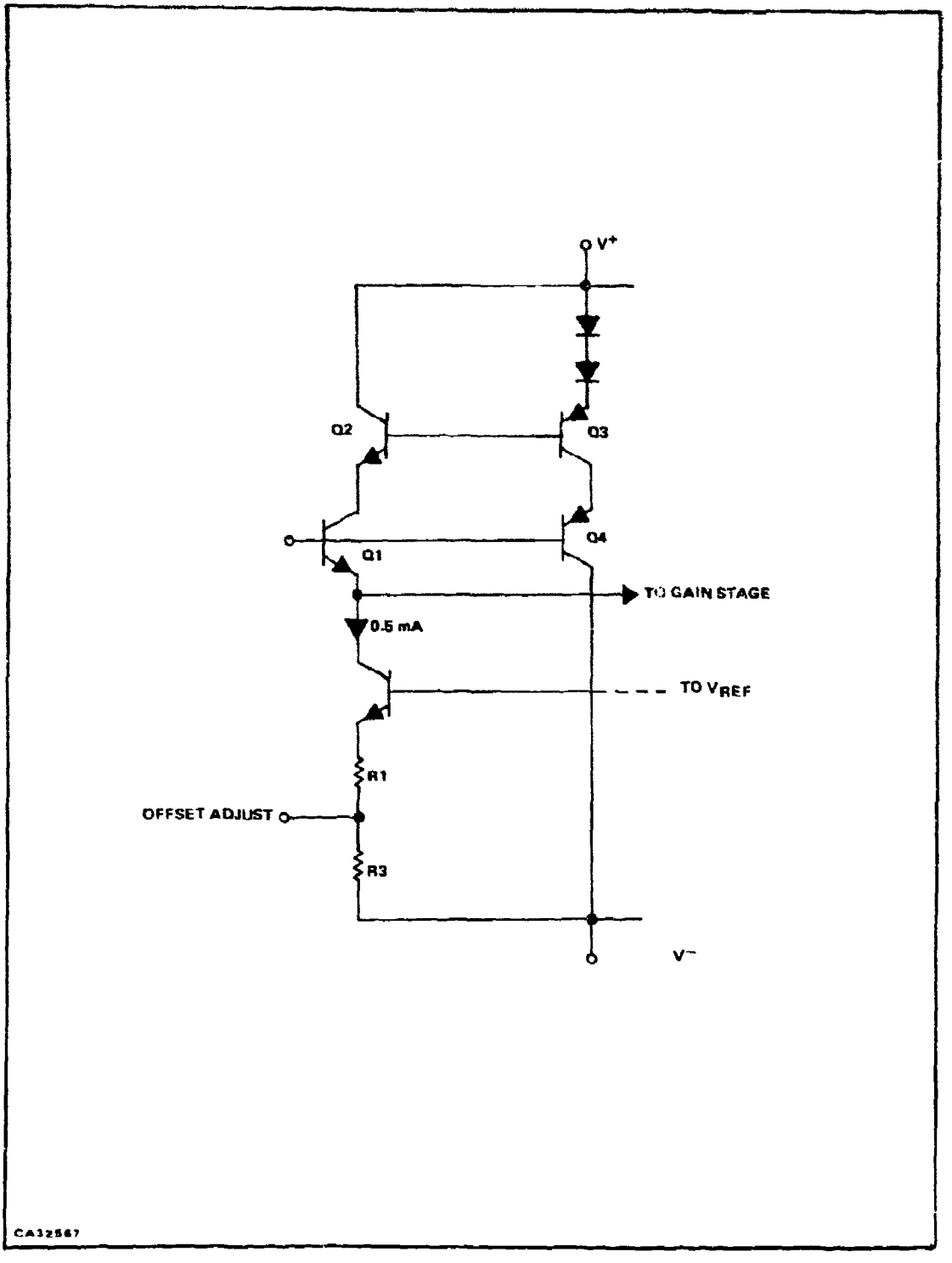


Figure 13. Input Buffer Stage

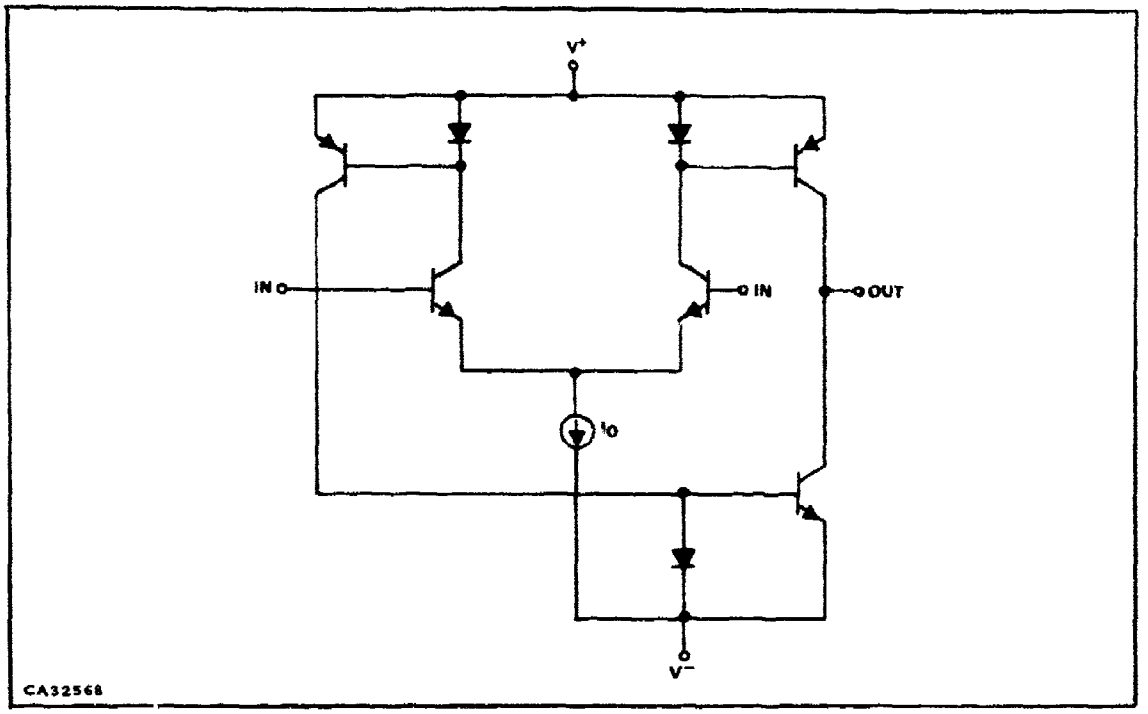


Figure 14. Basic Gain Stage

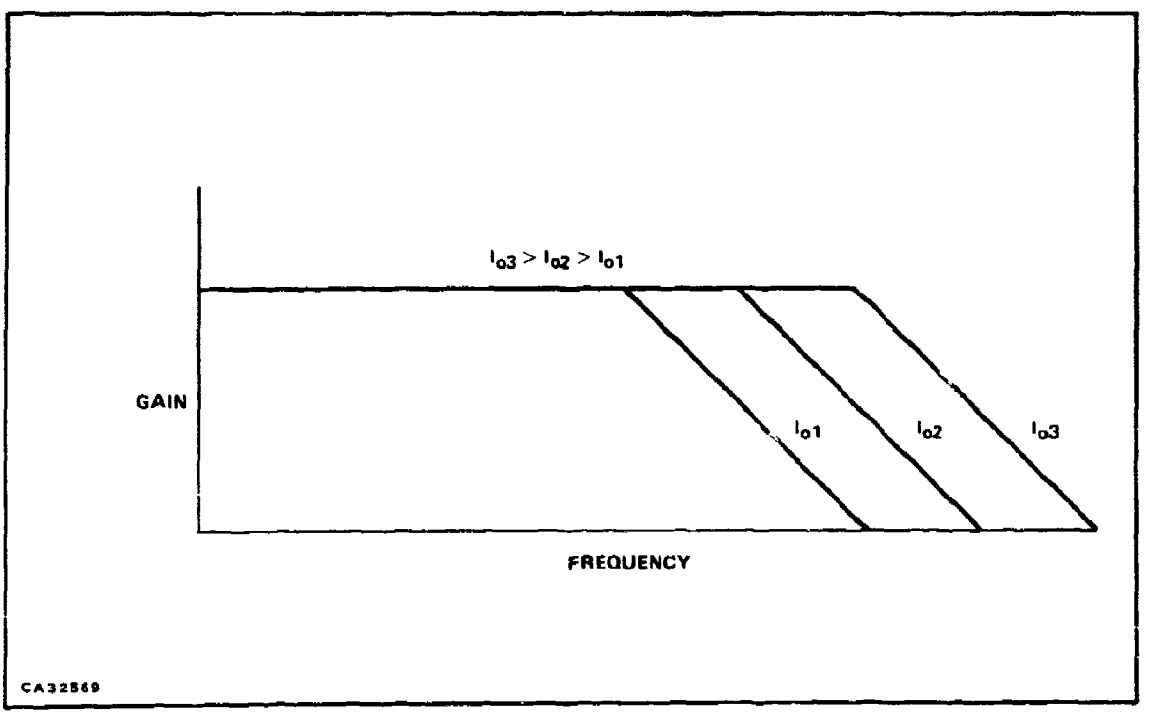


Figure 15. Frequency Response Characteristics of the Basic Gain Stage

The output stage is of conventional design. The NPN and PNP transistors were designed to handle 75 to 100 mA of output current without affecting the gain stage.

The final circuit schematic of the high slew rate amplifier is shown in Figure 16. The design uses the principles previously discussed. The input stages were set at a nominal emitter current of 0.5 mA by the voltage reference of Q16, R5, and R6. The transistors Q1, Q2, Q3, Q4, and Q15 plus the resistors R1 and R3 make up the positive input buffer amplifier. The negative input buffer amplifier is made from transistors Q5, Q6, Q7, Q8, and Q17 and resistors R2 and R4.

The current set node is used to determine the power level of the circuit, except for the input circuitry. The current is set by connecting a resistor from the current set node to the positive supply voltage.

The gain stage consists of transistors Q9, Q10, Q11, Q12, Q13, Q14, Q22, Q26, Q27, and Q28. The resistor R8, R9, R10, R11, R12, and R3 are set to vary the currents in the various branches of the gain stage in proportion to the set current. Resistor R14 is a bleed resistor for the Darlington-connected transistors Q27 and Q28.

The output transistors are Q33 and Q34. The resistors R17 and R18 reduce the idle current in the output stage to save power. This will cause some crossover distortion, which is not an important parameter in buffer amplifiers.

The combination of Q29, Q30, Q31, and Q32 provided additional current gain and biasing of the output transistors. The diode-connected transistors Q23, Q24, and Q25 are directly in the gain stage's output path and bias the output stage.

Short circuit current is sensed by the resistors R16 and R17 and turn on either Q20 or Q21, respectively.

The circuit is also provided with a compensation node. This node is used for a-c frequency shaping when desired.

The circuit of Figure 16 was breadboarded using available complementary bipolar transistors. The breadboard data taken on this circuit is shown in Figures 17 through 20. All data was taken at a set current (I_{SET}) of 0.5 mA. The open-loop slew rate data for the breadboard is summarized in Table I.

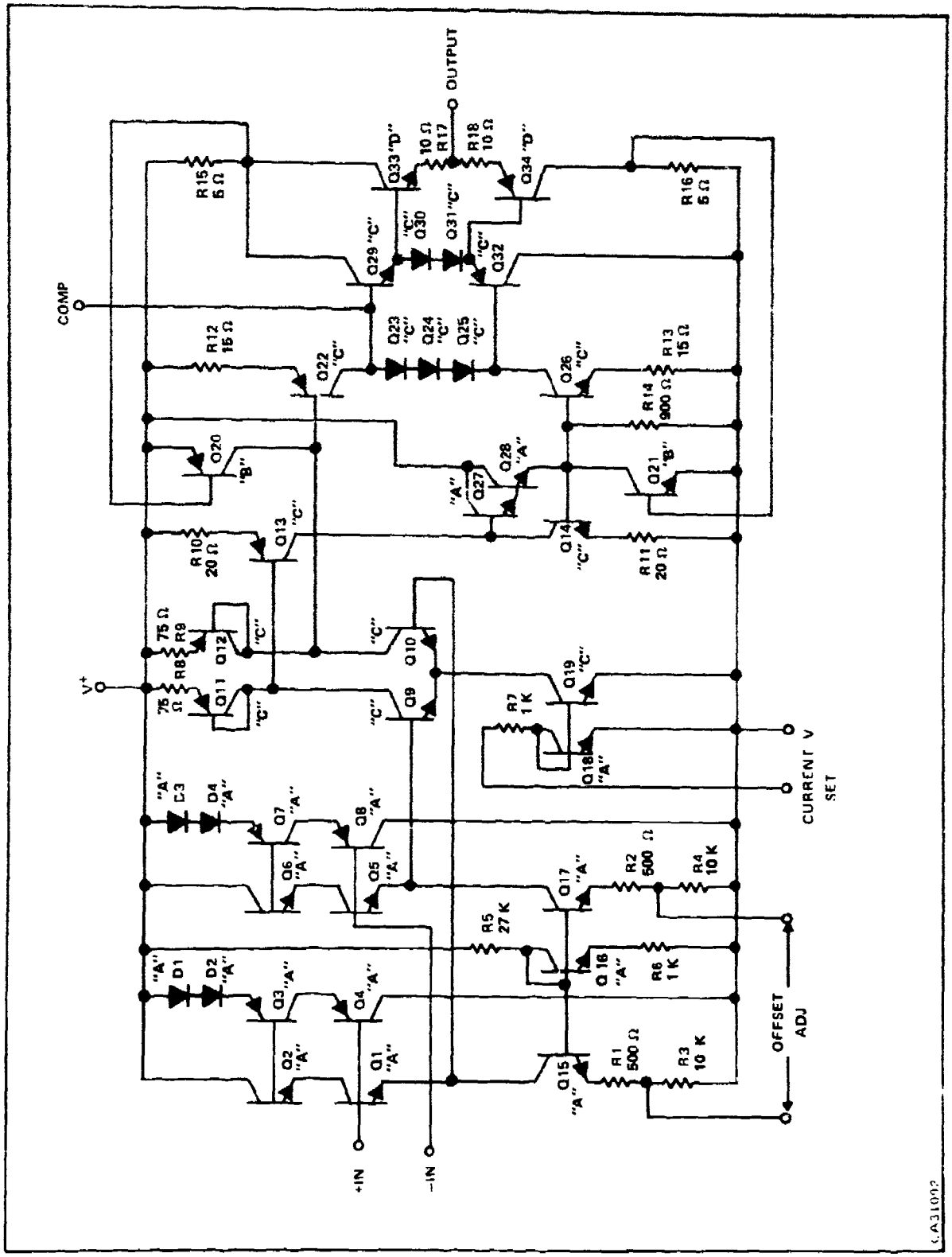


Figure 16. Integrated Circuit Configuration for High Slew Rate Operational Amplifier

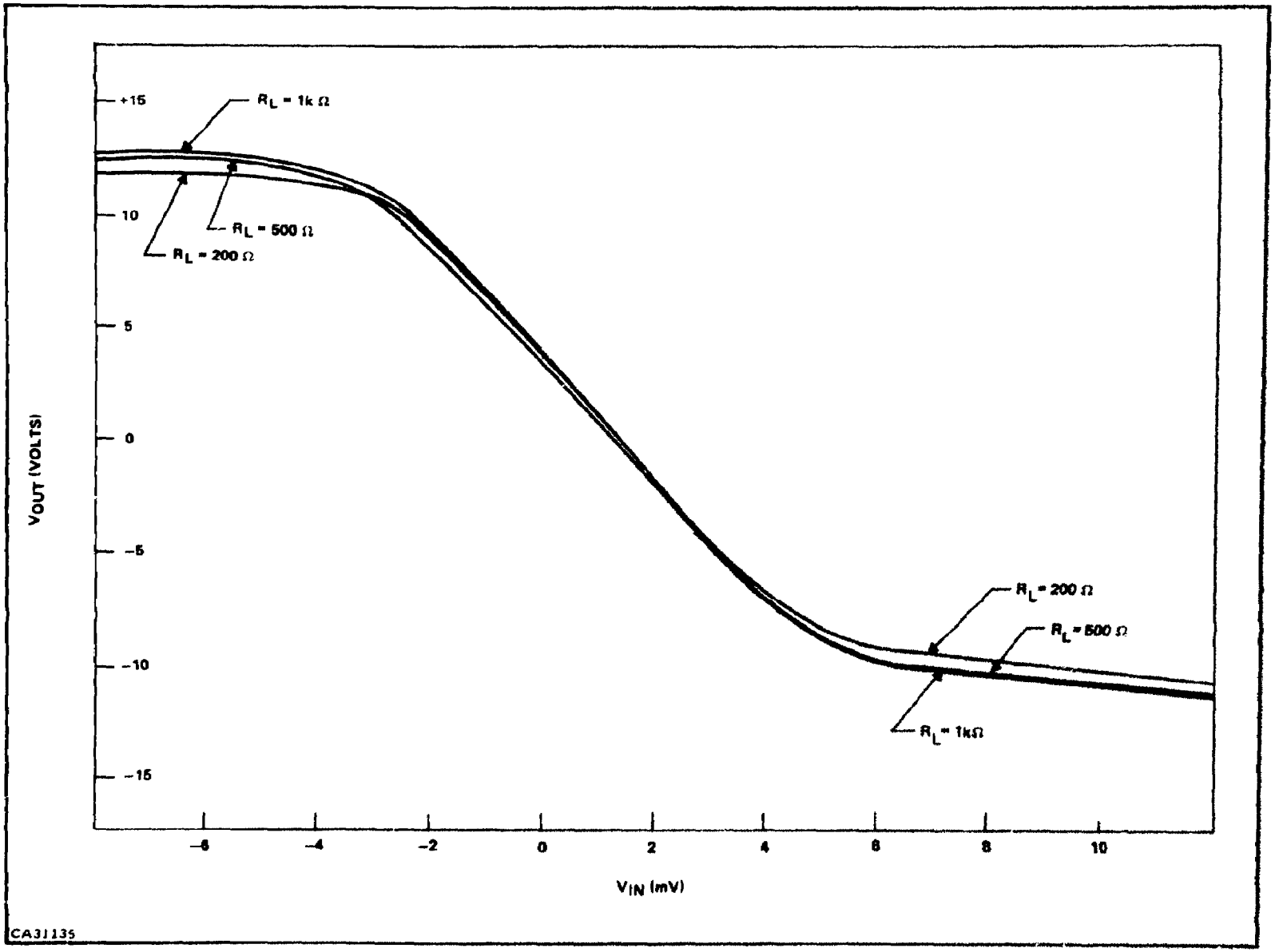


Figure 17. Breadboard Open-Loop Transfer Characteristics as a Function of Load

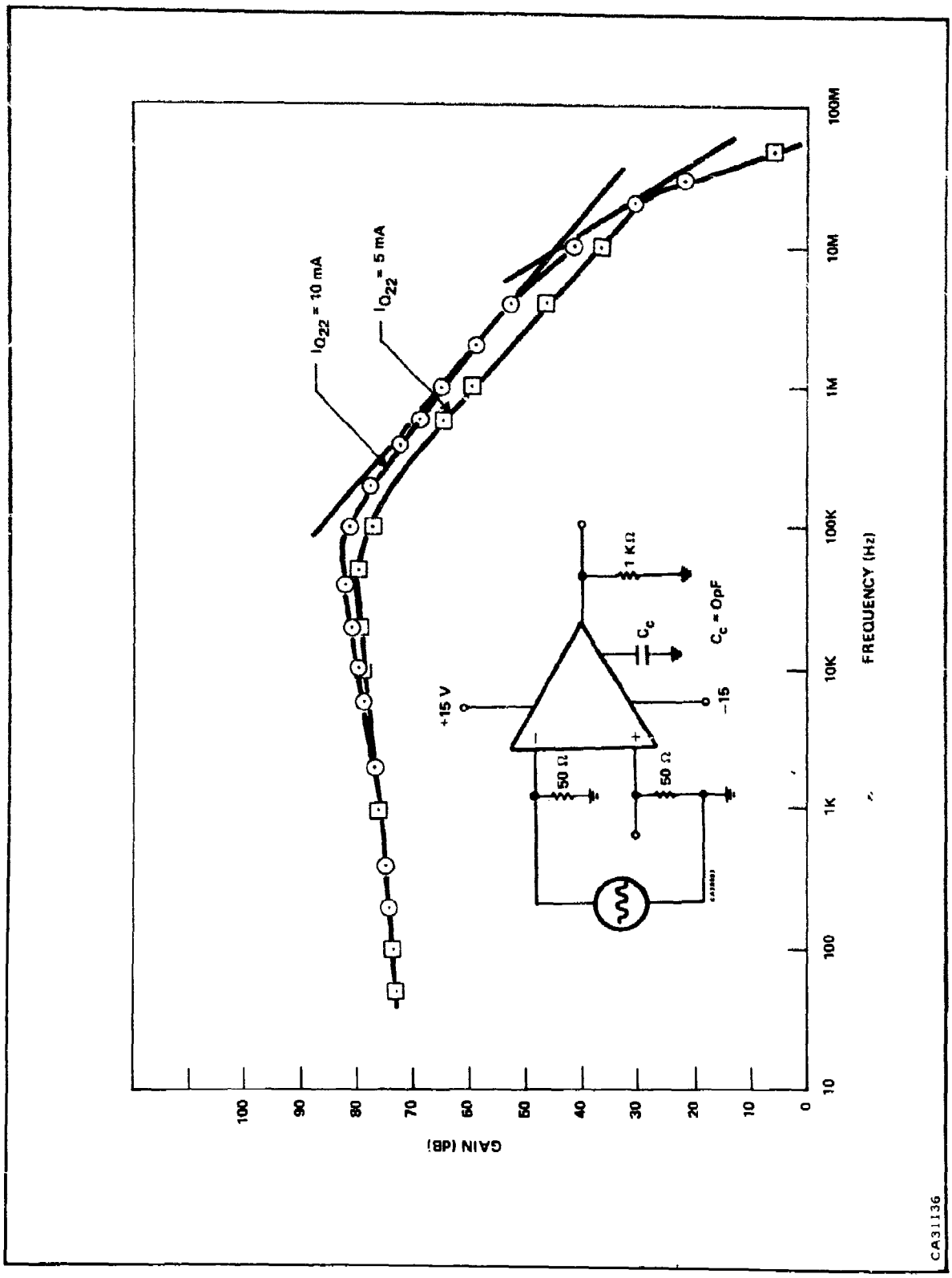


Figure 18. Breadboard Open-Loop Frequency Response

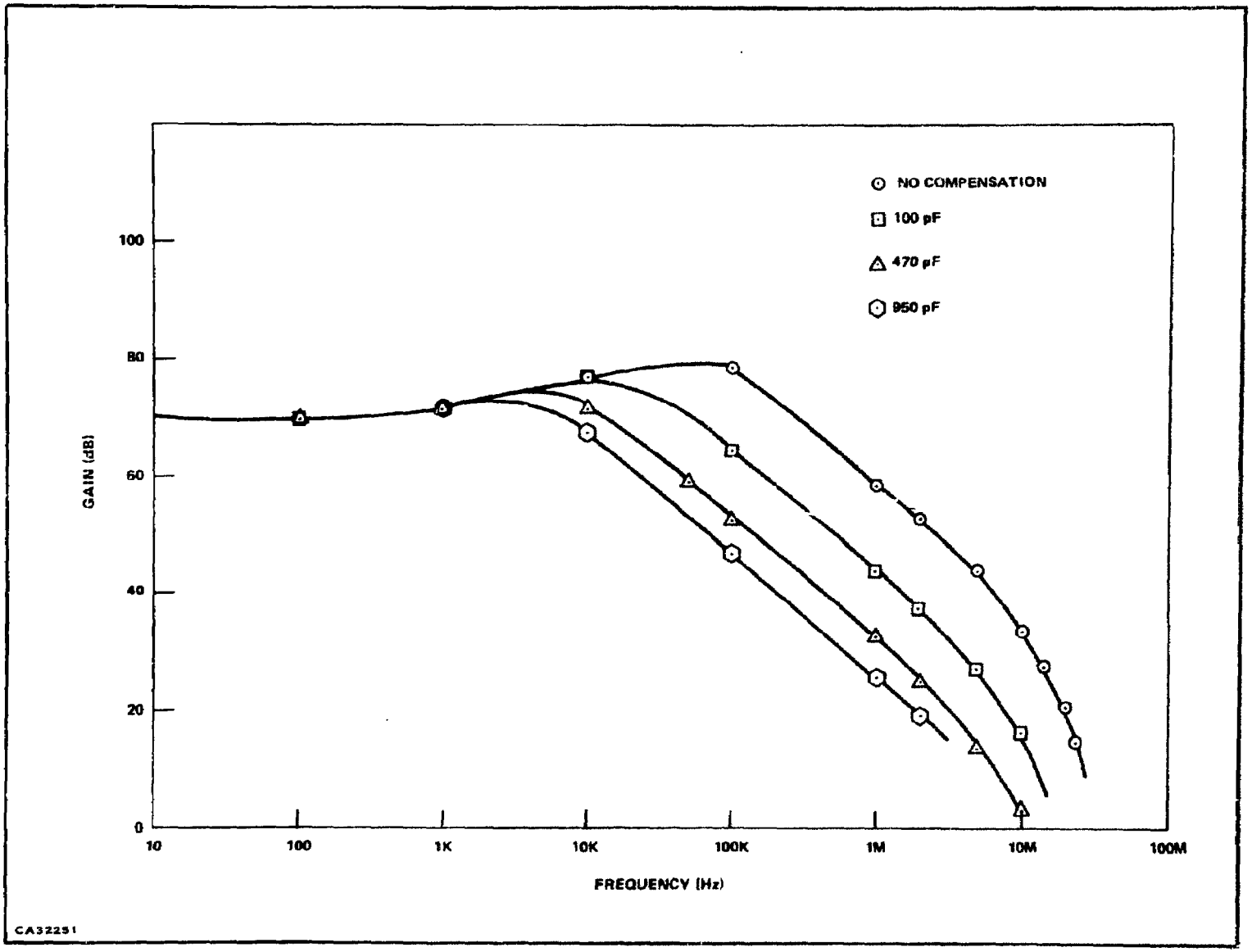


Figure 19. Breadboard Open-Loop Frequency Response for Various Compensating Capacitors

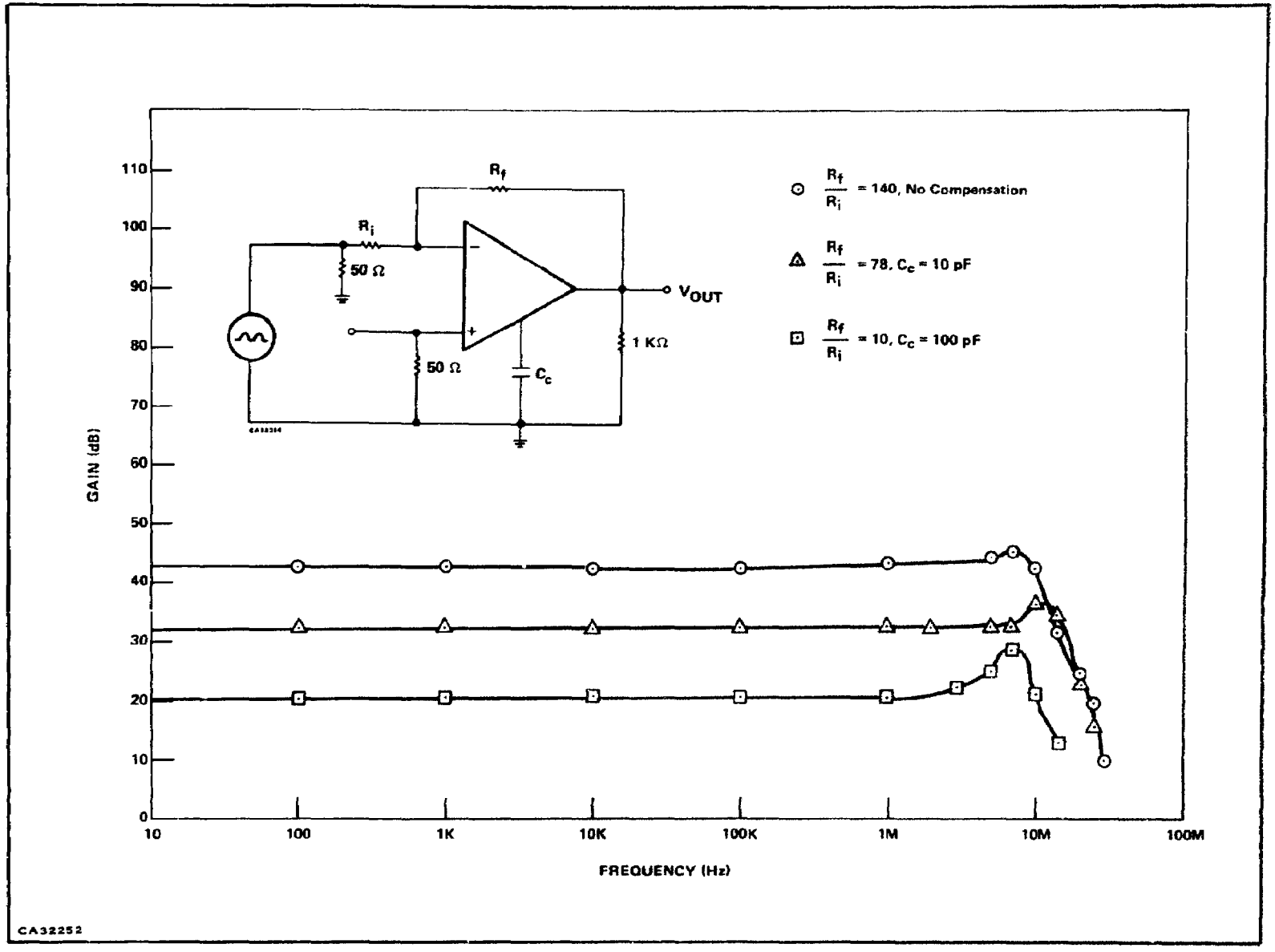


Figure 20. Breadboard Closed-Loop Frequency Response

Table I. Amplifier Open-Loop Slew Rate of Breadboard Circuit

	POSITIVE INPUT		NEGATIVE INPUT	
	Positive-Going Output	Negative-Going Output	Positive-Going Output	Negative-Going Output
Slew Rate (V/μsec)	1800	1400	400	2000

C. FABRICATION

Two possible fabrication approaches were considered for the high slew rate amplifier. These approaches included a monolithic/hybrid circuit with three chips and a monolithic design which uses complementary vertical bipolar transistors.

The hybrid design approach considered utilized a single silicon bipolar chip as the main portion of the circuit. The input stage of the circuit would use two outboard FET chips to obtain very high input impedance. The main advantage of this approach is the ability to select pairs of FET devices which are matched by a computer. These devices would have low-input bias currents and extremely low-input offset currents.

There are several disadvantages to the outboard FET approach. First, the high offset-voltage and input drift current are undesirable. The hybrid circuit is more complex and is, therefore, more expensive to assemble than a monolithic circuit. Reliability was also considered to be affected by the increased number of bond wires required in this process. After all of these factors were considered collectively, the monolithic circuit was chosen as the more desirable approach.

The monolithic approach considered used a dielectrically isolated, complementary bipolar process for implementation of the complete circuit in a single chip. Advantages of this approach include lower fabrication cost, improved reliability, and less processing time. A new circuit technique for improving input characteristics with bipolar transistors offered a reasonable alternative to the FET input. In addition, if the input characteristics of the monolithic circuit were not acceptable, the hybrid FET input devices could be added at a later time by making a simple lead pattern change.

The process used for the fabrication of the single-chip bipolar structure is a dielectrically isolated complementary bipolar process. The dielectrically isolated structure was selected because the isolation capacitances are much smaller than those associated with the collector-substrate junction capacitances of junction-isolated structures.

Several approaches to complementary processing exist. The incorporation of both NPN and PNP transistors in the same integrated circuit introduces considerable complexity into the circuit processing. Typically, in common processing, bases and emitters are selectively deposited and then diffused. In a complementary process; however, both a p-type and an n-type base and an n-type and p-type emitter must be included.

Simple techniques utilize a base deposition and diffusion as the collector of one polarity device and an emitter deposition and diffusion as the base of the opposite polarity device. While these processes are simpler because of fewer processing steps, the two polarities of transistors differ greatly in their characteristics. In a better approach, both bases can be deposited separately and diffused simultaneously; the emitters are done similarly. This introduces two extra selective oxide etching steps and two extra deposition steps. In this manner, the opposite polarity transistor types are similar in performance and have approximately equal diffusion depths.

The process now in use at Texas Instruments for the fabrication of oxide-isolated structures is the "Single-Poly" ("Precision Grind, Lap, and Polish") method. Of the several fabrication processes available, this has proven to be the best compromise in terms of fabrication cost (yields and complexity of process steps) and device performance (control of critical component parameters). Devices are presently being fabricated in volume quantities in the Special Circuits department at Texas Instruments using this process. The process steps are described below and illustrated in Figure 21.

- Starting material is N-type silicon.
- Dopant is diffused to give N^+ and P regions of controlled thickness and resistivity.
- Moats for isolation, lap stops, and bar scribing are etched into the back side using preferential-etching techniques.
- Isolation oxide is grown on the back side, followed by polycrystalline silicon for mechanical support.
- The front side is lapped down to provide isolated regions completely surrounded by silicon dioxide and then a surface oxide is grown.

Following these steps, the slices are ready for normal integrated-circuit processing to diffuse the bases and emitters, open oxide for contacts, and apply the metallization for interconnects. The doping on the bottom of the pockets and the pocket thickness are critical factors in the process. The completed structure, with metallization, is shown in Figure 22. Only the NPN transistor structure is shown. The PNP structure is exactly the same with one exception. The PNP transistor has a P^+ guard ring around the base region to prevent surface inversion.

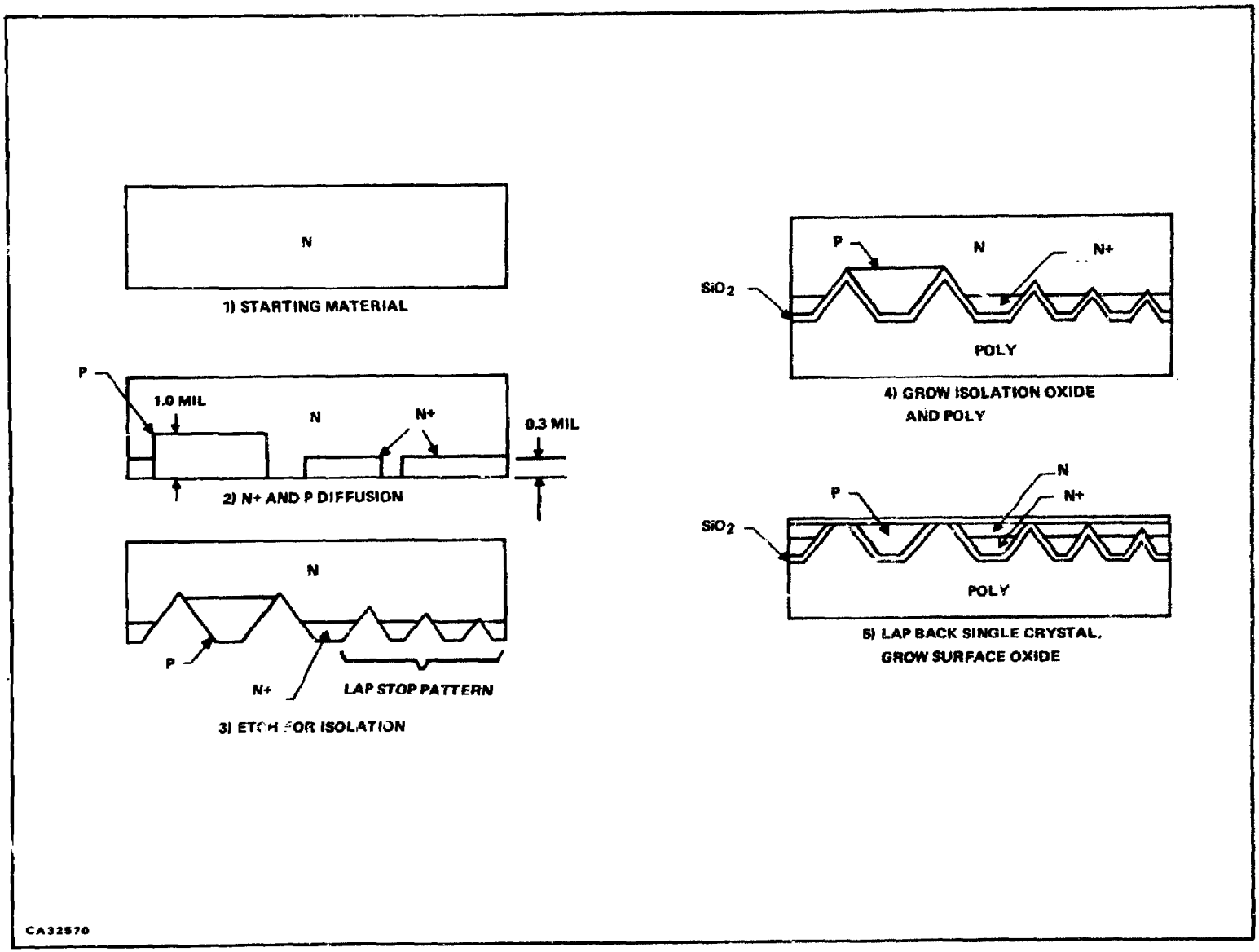


Figure 21. Complementary Dielectric Isolation Process

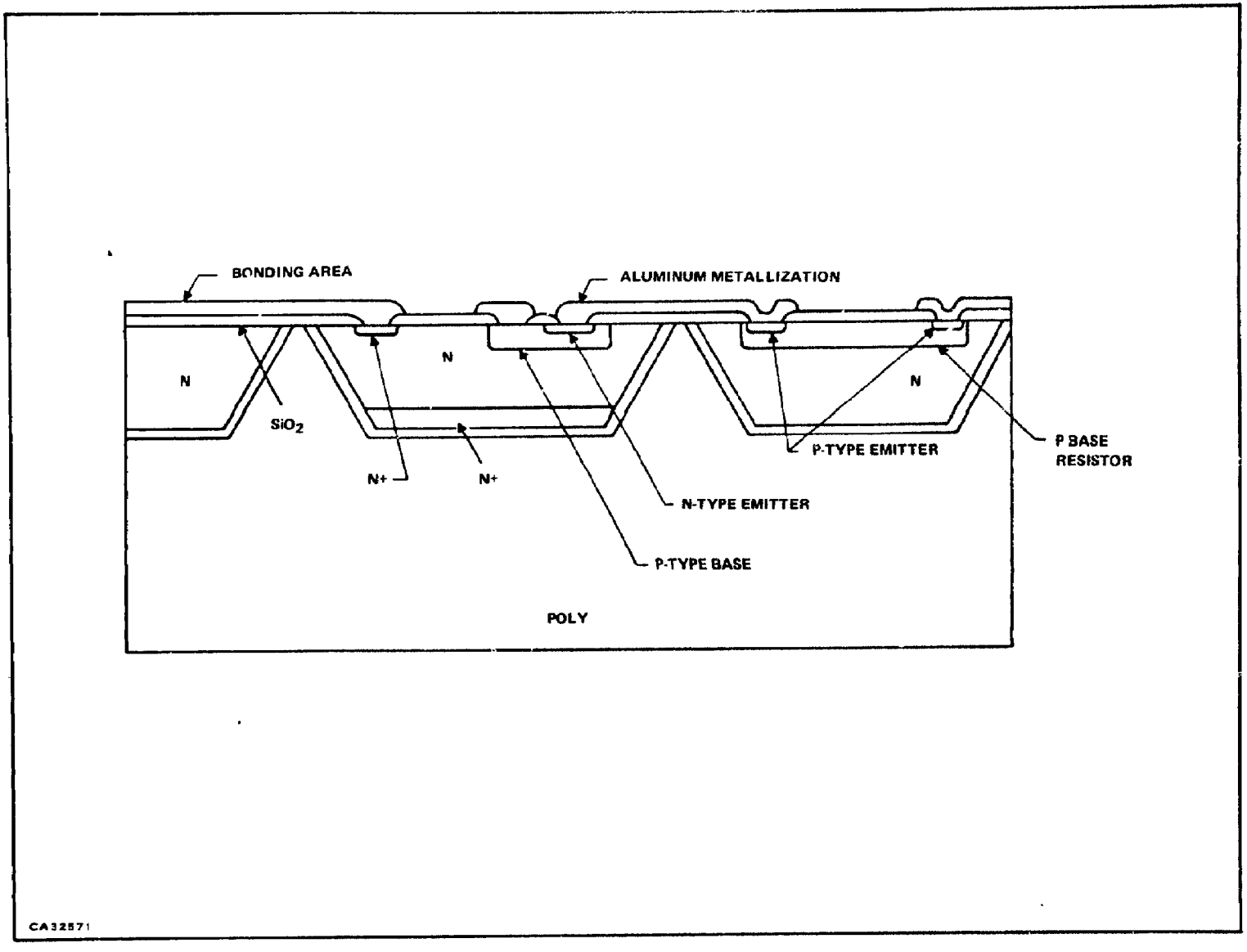


Figure 22. Dielectrically Isolated Transistor and Resistor Structures

It is important that the thickness of the transistor pockets be accurately controlled, since it is primarily this thickness that determines the saturation collector resistance of the transistor. A system of visual indicators is used at Texas Instruments to stop the lap-back operation at a known thickness. The visual indicators are based on the preferential-etch technique wherein the sidewalls of the etched moats are at a known fixed angle to the surface. The depth of the etched moat can be controlled by controlling the width of the isolation oxide opening. In practice, several stripes of graduated width are opened up and etched during normal etch, forming short moats of known graduated depth. Then, during lap-back, it is only necessary to count the number of stripes visible at the surface to determine the thickness of the transistor pockets.

It is desirable that the surface area of the monolithic circuit chip be used as efficiently as possible. This results in a minimum chip size which improves manufacturing yields and presents a lower total exposed volume in a radiation environment. Chip size is minimized by reducing the geometries of the active elements and increasing their packing density.

The resistors used in the circuit are diffused resistors made with either the P-base or the N-emitter diffusion. The P-base resistors are used where high sheet resistances are required to obtain large resistor values. Small resistors of a few ohms are fabricated with the N-emitter diffusion.

Aluminum interconnects are tailored to meet maximum worst-case, current-density requirements. Each interconnect is considered individually on the basis of the maximum current it would be required to carry for any worst-case condition, and its width is then adjusted to ensure a safe current density (based on a known minimum thickness). This current density is defined for three conditions:

- $J = 2 \times 10^5$ amp/cm^2 for continuous operation, maximum operating conditions.
- $J = 5 \times 10^5$ amp/cm^2 for intermittent operation, such as the short-circuit output condition with maximum operating supply voltage.
- $J = 10 \times 10^5$ amp/cm^2 for surge current conditions, such as transisent radiation-recovery levels.

D. DISCRETE DEVICE CHARACTERISTICS

The integrated-circuit-device requirements for the high slew rate operational amplifier were determined by the breadboard and computer-aided circuit design. Optimum operating points and currents for each device were defined. In addition, a 100% worst-case design margin was allowed in current-carrying capabilities since it was believed that higher power levels (approximately one watt quiescent power) might be required for optimum slewing. Since the power level for optimum slewing is actually about an order of magnitude lower in the integrated circuit than in the

breadboard, the device geometries are somewhat oversize and could be significantly reduced without adversely affecting circuit capabilities. In fact, the smaller geometries would have lower parasitic capacitances and, hence, better frequency performance capabilities.

The basic transistor structure is defined by the fabrication process chosen. A profile view of the transistors formed by the complementary bipolar dielectric isolation process is shown in Figure 22. It was recognized that a major problem would be the saturation voltage due to high-output current requirements of the output transistors. The design of the output transistors involved a trade-off between high resistivity of the collector material required for breakdown voltages in excess of 30 volts and low resistivity required for low saturation voltage. Two approaches were used to solve the problem. First, a highly doped layer was formed by a diffusion on the bottom of each transistor pocket. This diffusion serves two purposes – it forms a low-resistivity, buried layer under the device which lowers the parasitic resistance associated with the collector region of the transistor and it also forms a retrograde doping profile for the transistors. The retrograde doping is especially beneficial to the transistors in the gain stage, since the gain of the amplifier is determined by the output impedance of these transistors. The gain of the amplifier is increased by the retrograde doping of the collector regions due to the buried layer diffusion. However, this diffusion causes a breakdown problem due to its up diffusion toward the device surface during the dielectric isolation process and subsequent high-temperature processing. The second approach used to reduce the saturation voltage of the output transistors was to provide a large enough geometry to meet the high current requirement with a relatively deep collector pocket, even if the additional doping on the reverse side could not be used.

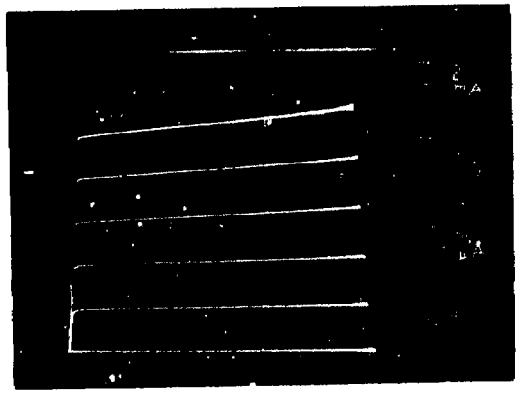
The resulting device characteristics are shown in Figures 23 and 24. The transistor characteristics are identified as geometry "A", "B", "C", or "D". These identifying letters are the same as those which appear in Figure 16 so that the corresponding characteristics may be identified for each device.

The other significant area of device design involves the use of junction area ratios in the current sources to set operating points of high-current paths without dissipating unnecessary amounts of power. A low current is set in the reference device, which causes a higher current to flow in the device being controlled. The savings in power occurs because the power in the voltage reference path can be made lower than if both devices were dissipating equal amounts of power.

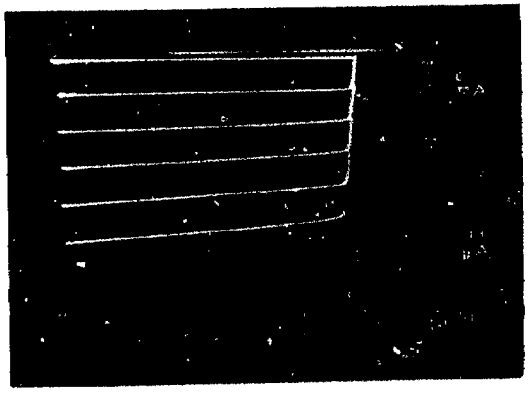
E. DEVICE RESULTS

1. Circuit and Packaging

This section describes the results of monolithic fabrication of the high slew rate amplifier. The device has been designated the X776 operational amplifier. The circuit of Figure 16 was fabricated

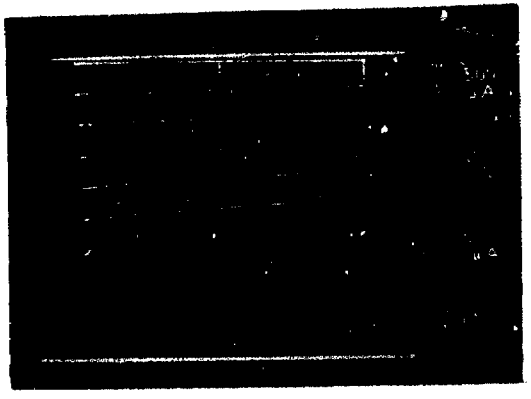


8.0 MIL EMITTER NPN
GEOMETRY "C"



8.0 MIL EMITTER PNP
GEOMETRY "C"

1.0 MIL EMITTER NPN
GEOMETRY "A"



2.0 MIL EMITTER PNP
GEOMETRY "B"

CA32572

Figure 23. Complementary Bipolar, Dielectrically Isolated Transistor Characteristics

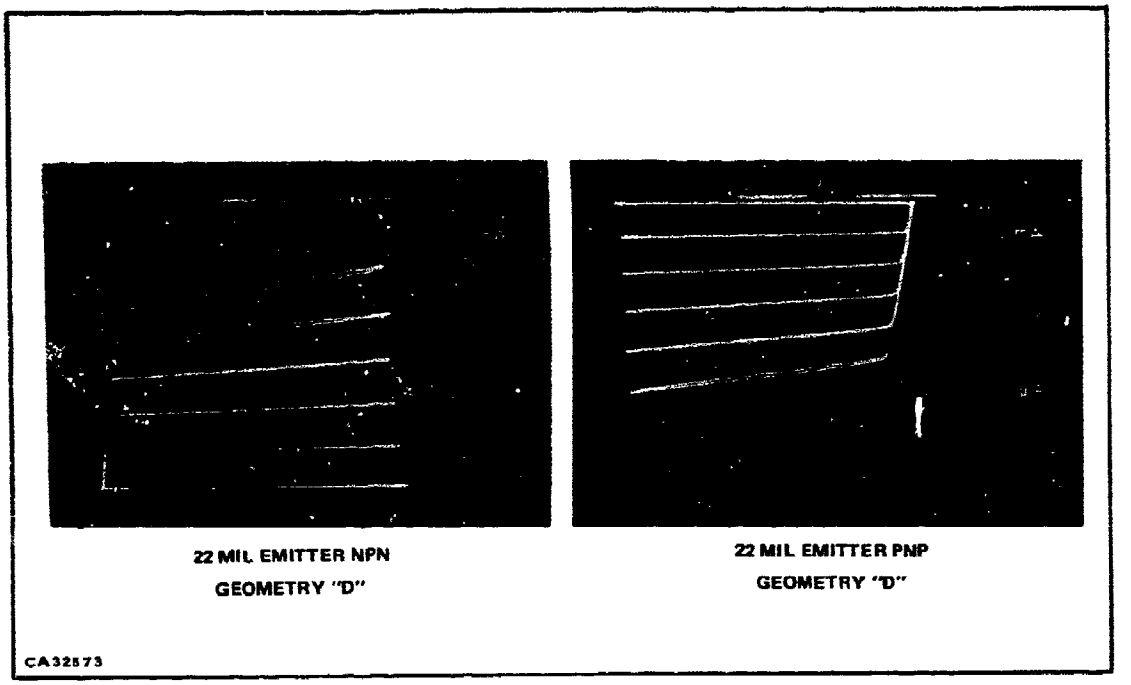


Figure 24. Complementary Output Transistor Characteristics

using the complementary bipolar dielectric isolation structure previously described. A photograph of the X776 bar is shown in Figure 25. The device was packaged in a nine-pin power package for high output current use and in a TO-5 package for lower-power applications.

The nine-pin power package is shown in Figure 26. The package was not developed on this program and was the best power package available at the time of fabrication. The nine pin bonding diagram is shown in Figure 27 and the TO-5 configuration is shown in Figure 28. A typical configuration showing the connection for the offset adjust and current set for the power package configuration is shown in Figure 29.

2. Electrical Characteristics

The open-loop frequency response is shown in Figure 30 for various power levels. The power is varied by changing the set current (I_{SET}). The open-loop characteristic of Figure 30 shows an interesting trend. As the set current (I_{SET}) is decreased, the circuit becomes more stable without sacrificing bandwidth. The breadboard required 600 mW to obtain high open-loop slew rates but it was not unity gain stable. The X776 also was not unity gain stable at high powers but becomes more stable as the power is decreased. This trend continues in Figure 31. The remaining data will be shown at two power levels. They are a set current of 0.5 mA ($P_D \approx$ 600 mW) and a set current of

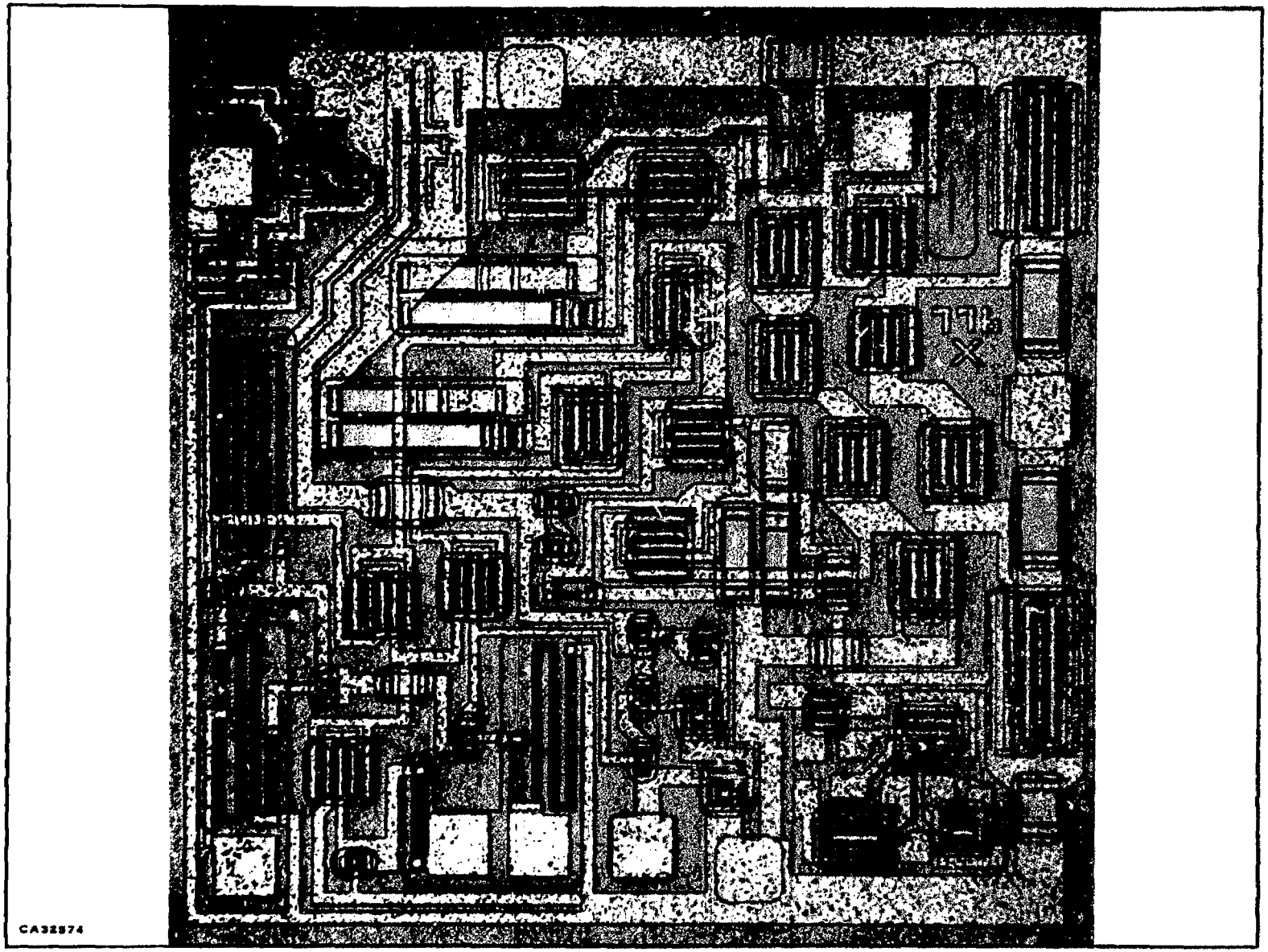


Figure 25. Photograph of the X776 Bar

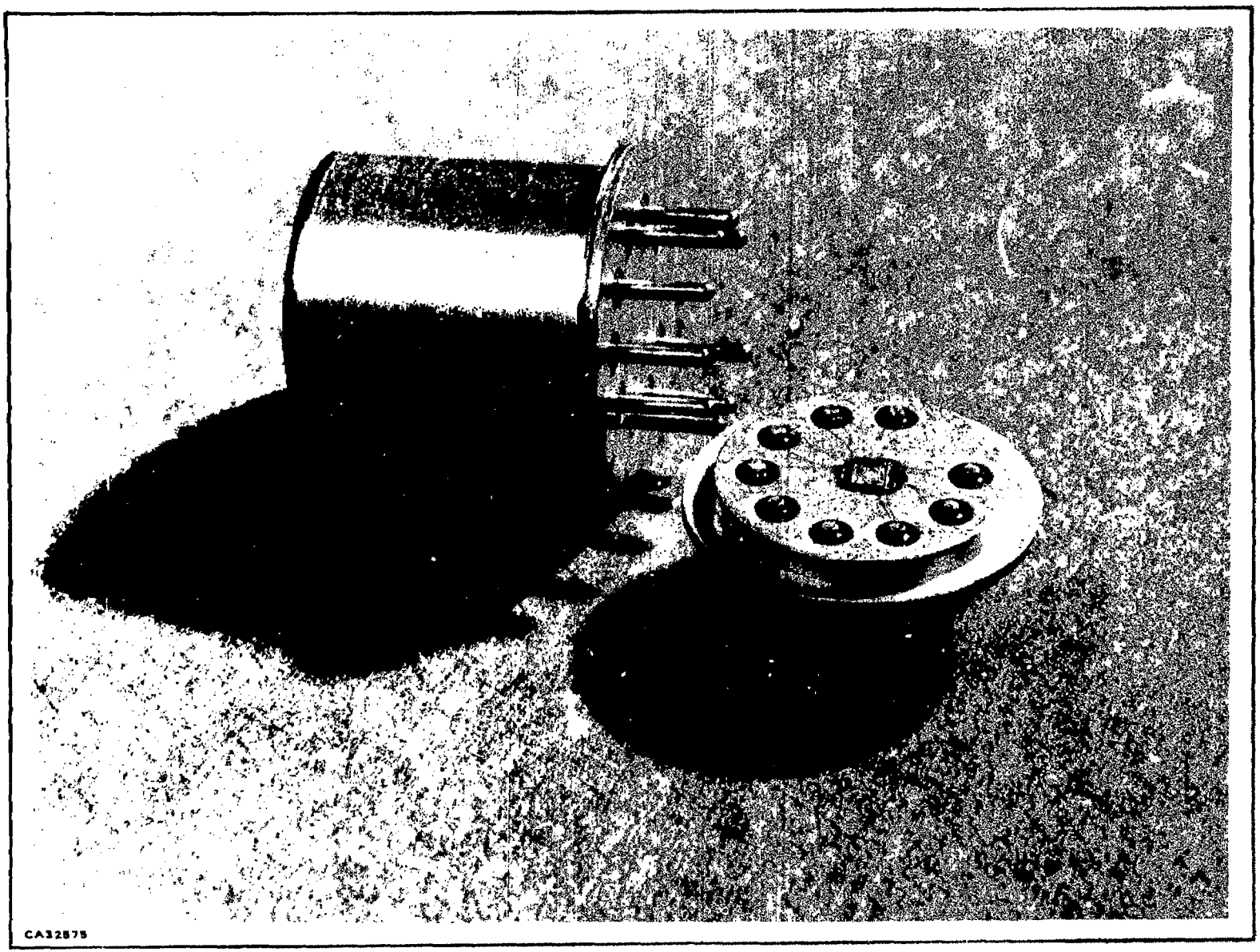


Figure 26. Photograph of the Nine Pin Package

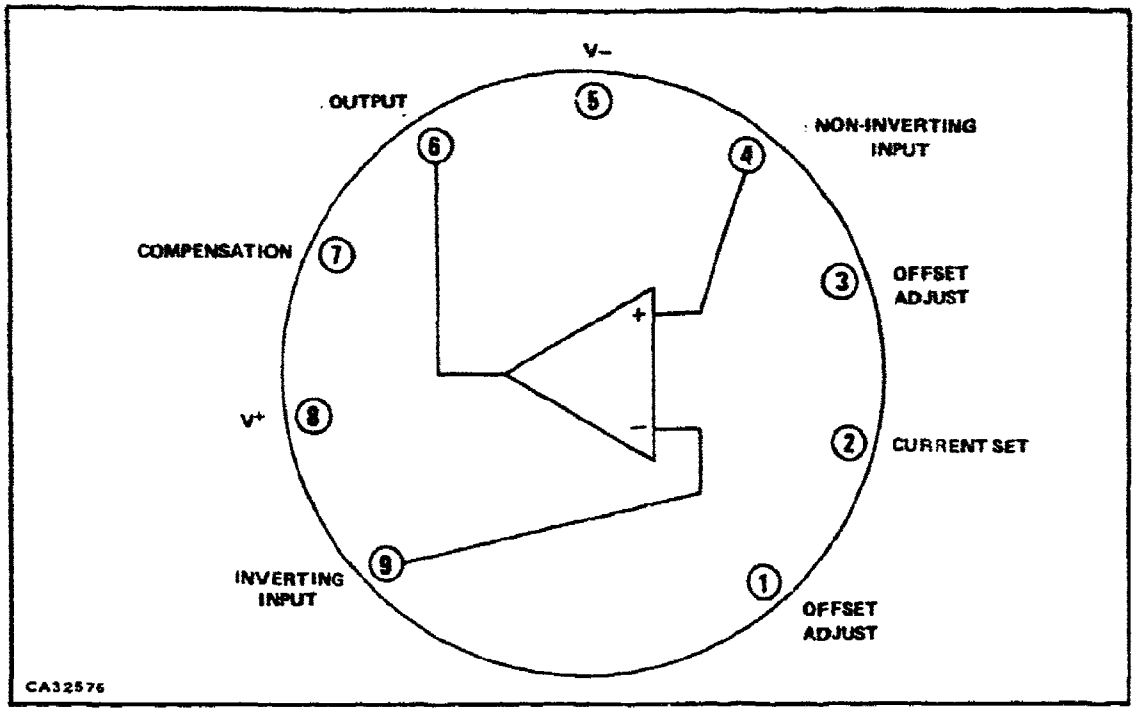


Figure 27. Nine Pin Power Package Pin Configuration (Top View)

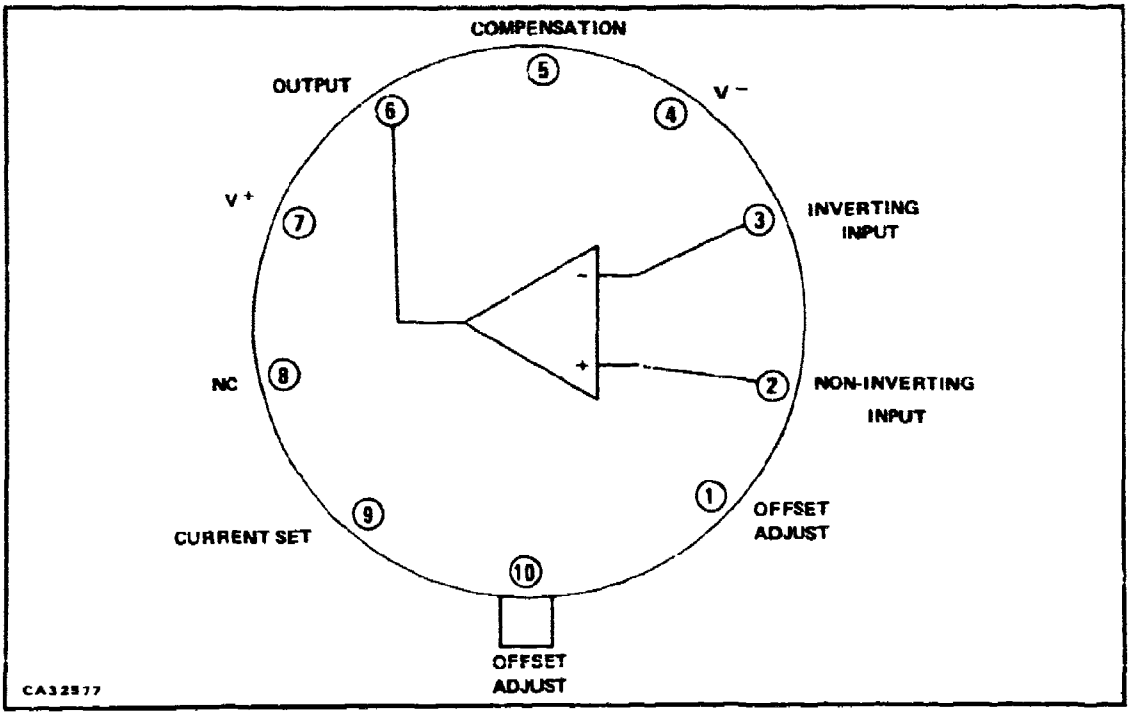


Figure 28. TO-5 Package Pin Configuration (Top View)

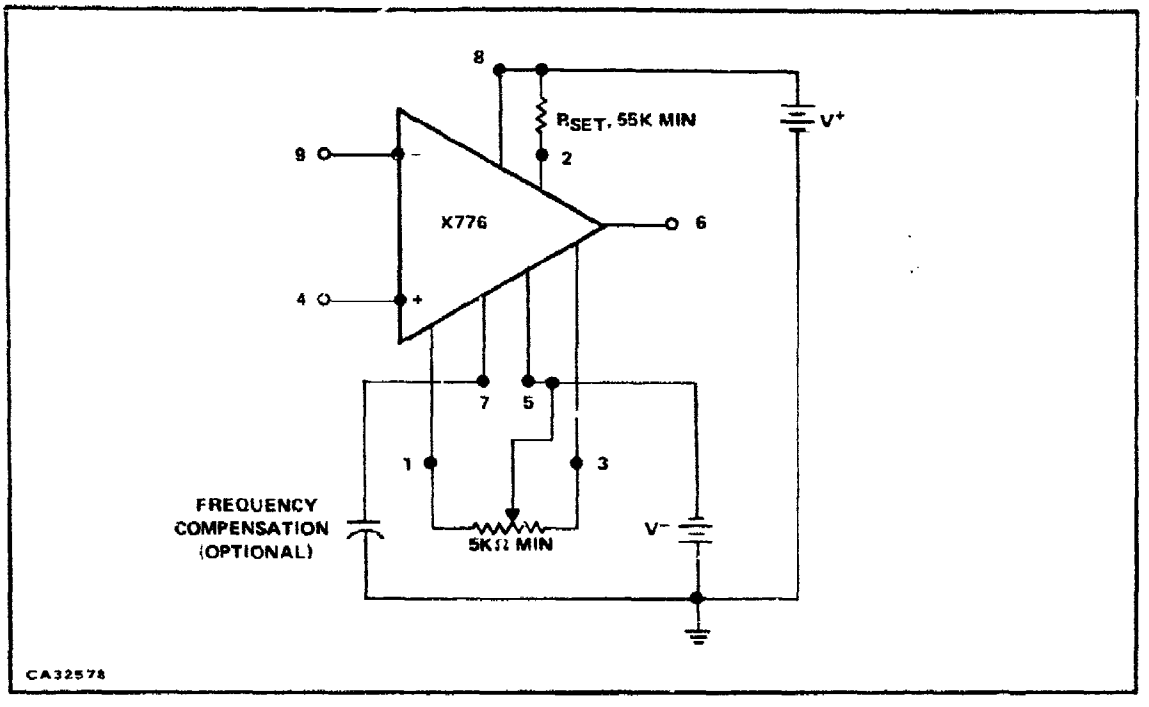


Figure 29. Typical Circuit Connection of the X776 for the Nine Pin Power Package

0.05 mA ($P_D \approx 100$ mW). The higher bias level was not stable when connected in a unity gain configuration and required large compensating capacitances. This seriously lowered slew rates as will be seen later. The lower bias level was unity gain stable and required no external capacitor for compensation, thus the amplifier was able to achieve very fast slew rates at unity gain.

The open-loop frequency response for various temperatures at high power level is shown in Figure 32. The lower power level temperature characteristics for two units are shown in Figures 33 and 34. Since the X776 is not unconditionally stable at high power levels, the device requires compensation capacitors in certain closed-loop configurations. The open-loop frequency characteristic for various compensation capacitors are shown in Figure 35. The closed loop characteristics at high power levels are shown in Figure 36. The X776 is stable for all closed loop configurations at lower power; therefore, no compensating capacitor is required.

The d-c open-loop transfer characteristics are shown for the high-power case in Figure 37. The transfer characteristics for the lower bias case, as shown in Figures 38 and 39, show some crossover distortion. The crossover distortion is a result of designing the output stage to conserve power. This distortion does not appear at higher power levels.

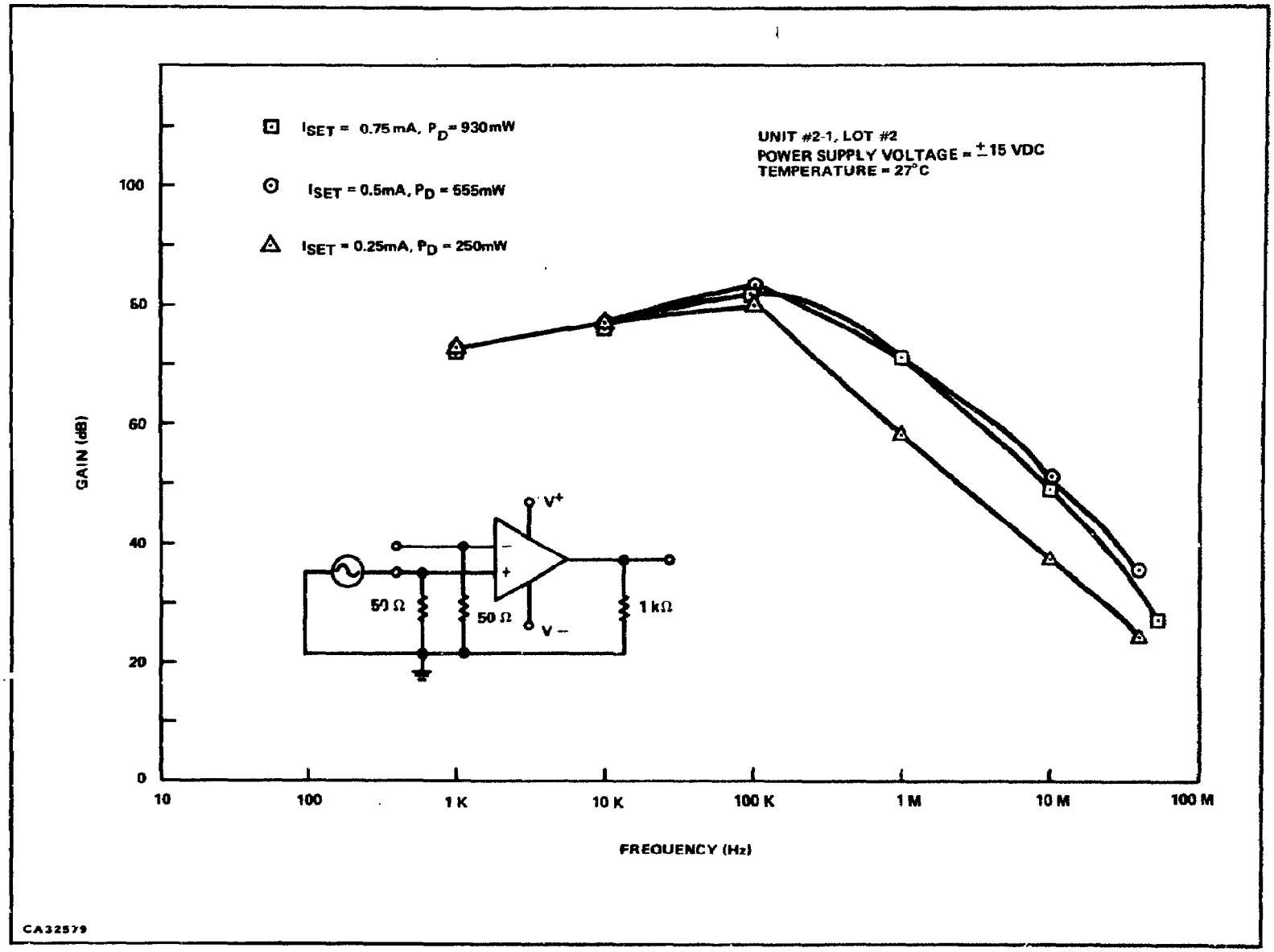


Figure 30. Open-Loop Frequency Response as a Function of Power Dissipation for High Power Levels

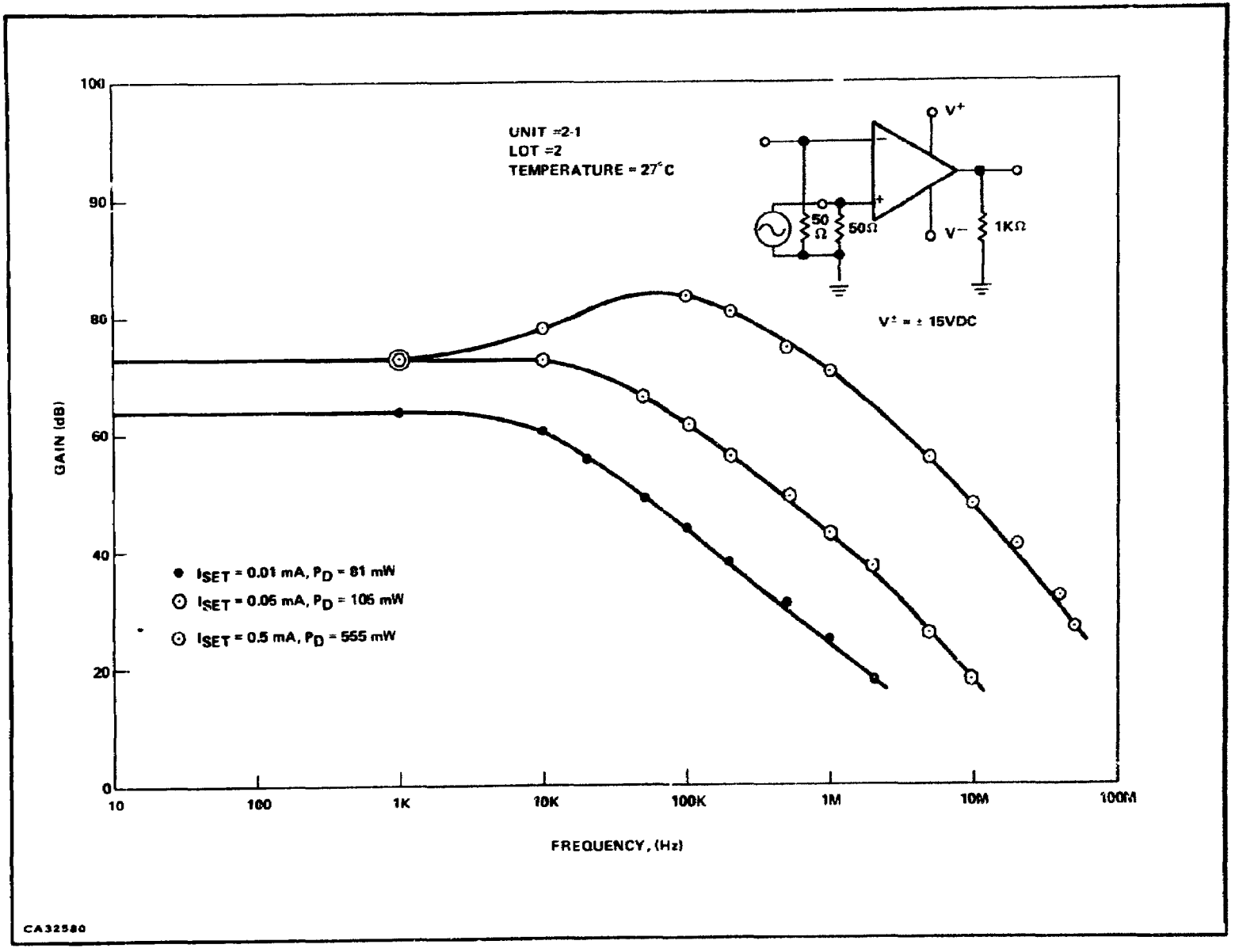


Figure 31. Open-Loop Frequency Response as a Function of Power Dissipation for Low Power Levels

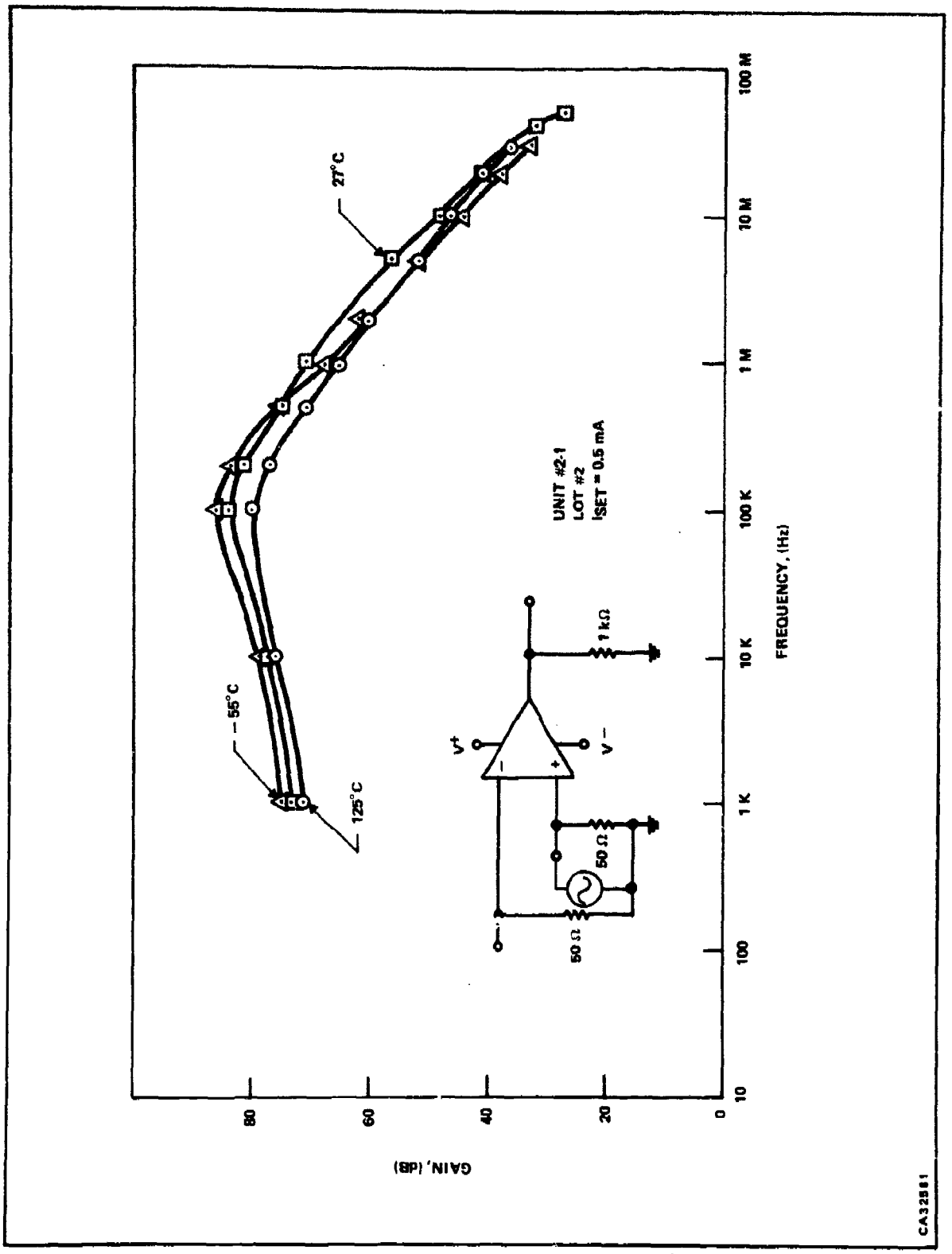


Figure 32. Open-Loop Frequency Response as a Function of Temperature at High Power Levels

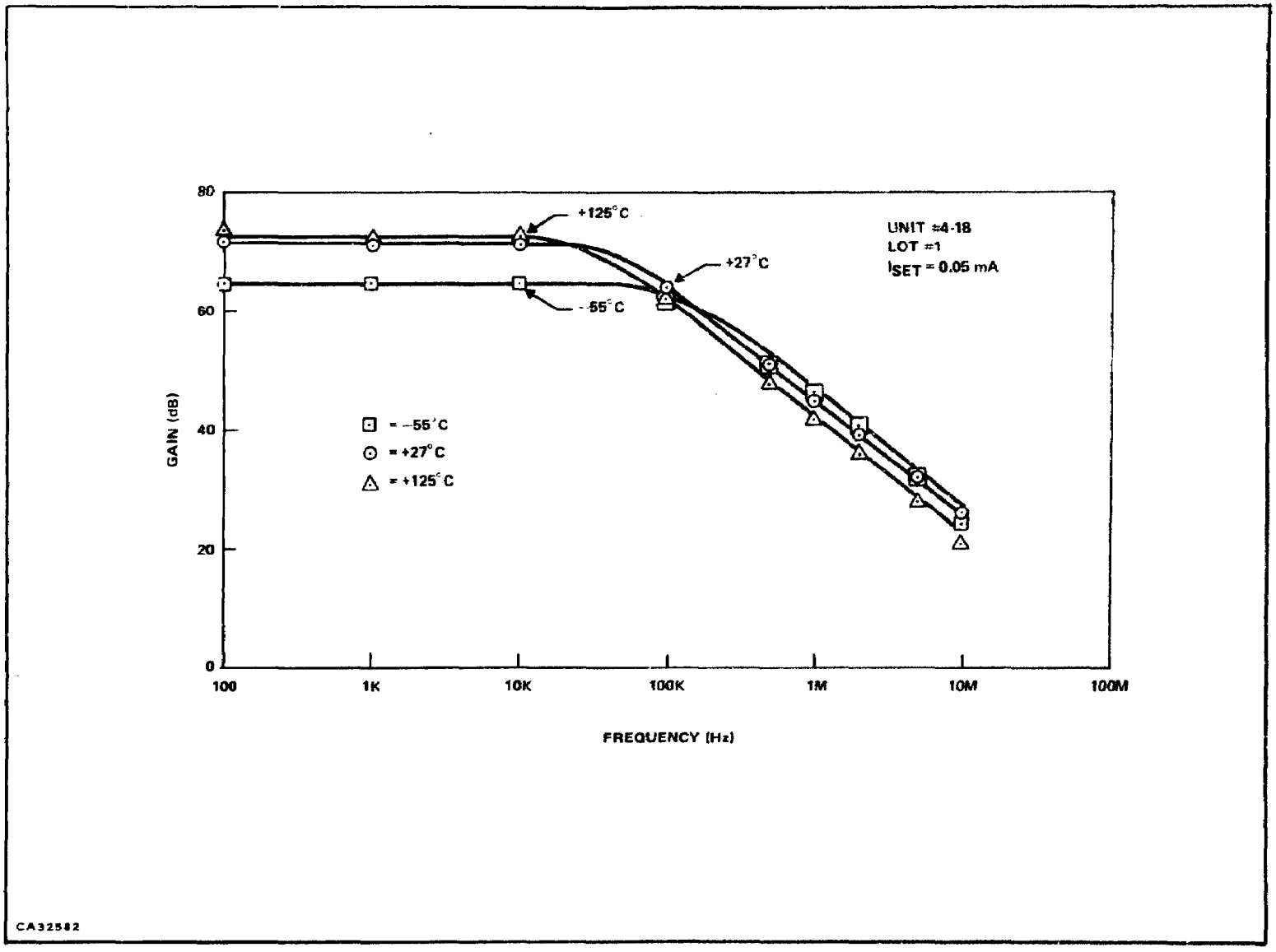


Figure 33. Open-Loop Frequency Response as a Function of Temperature at Low Power Levels (Unit 4-18)

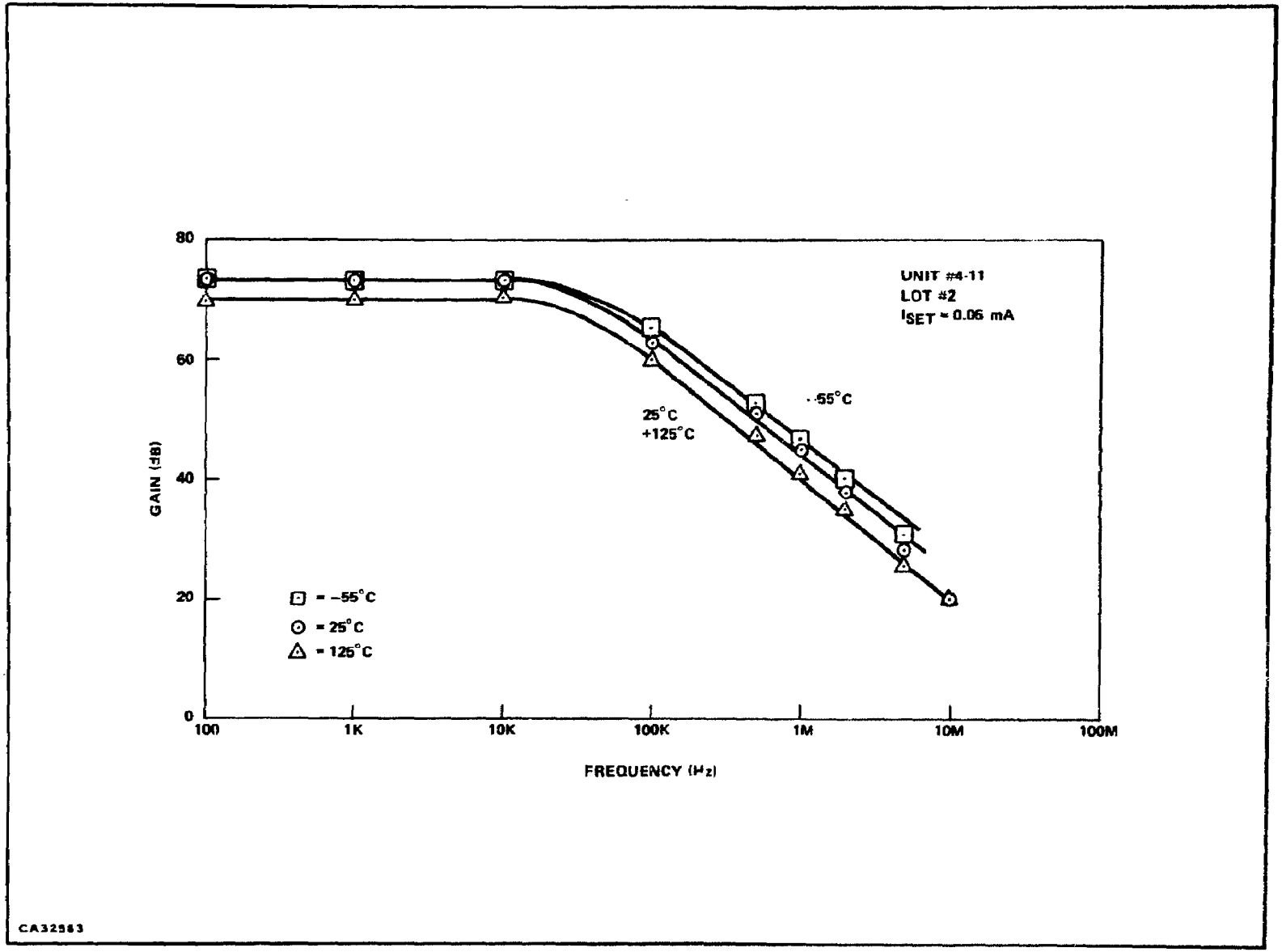


Figure 34. Open-Loop Frequency Response as a Function of Temperature at Low Power Levels (Unit 4-11)

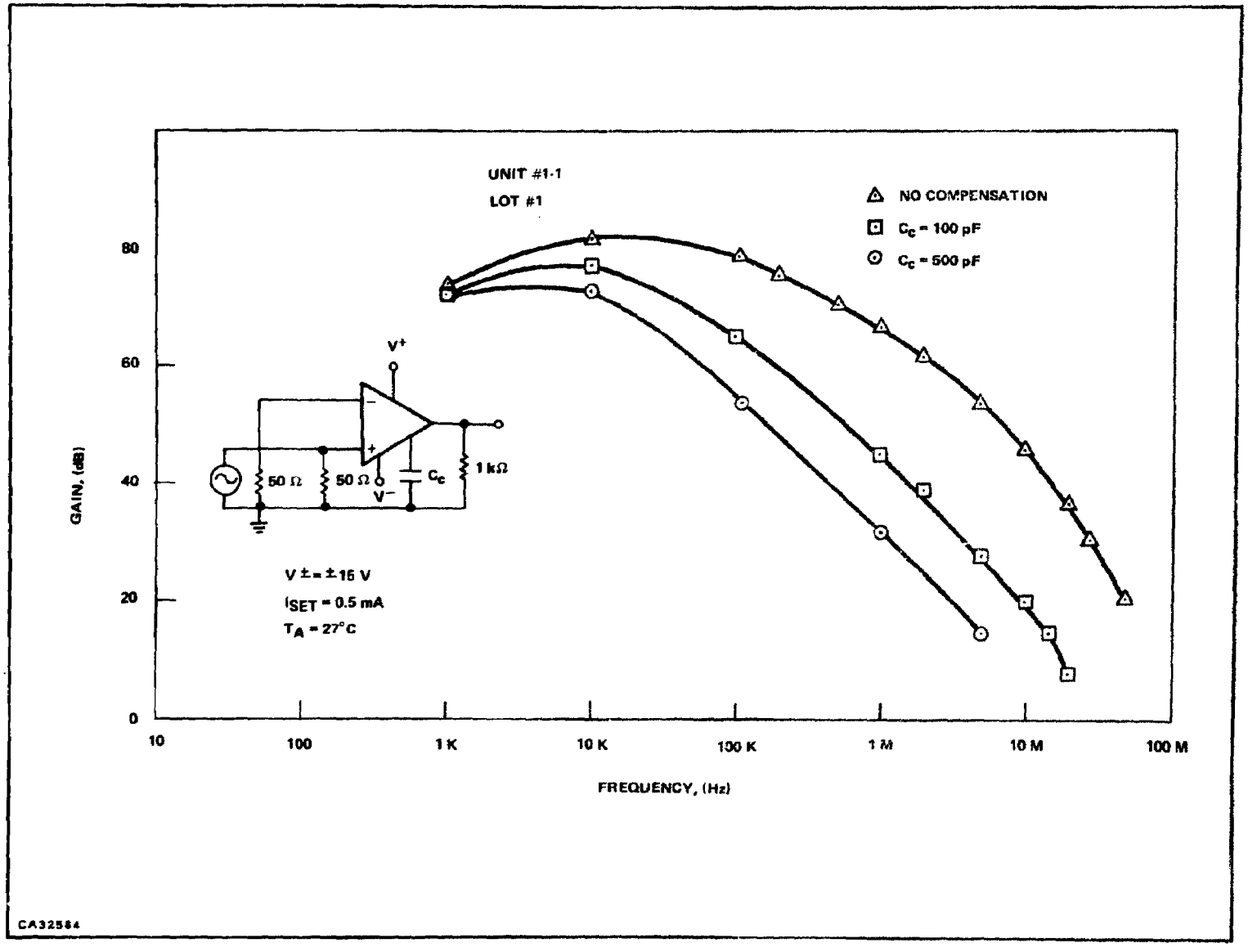


Figure 35. Open-Loop Frequency Response as a Function of Compensation Capacitance at High Power Levels

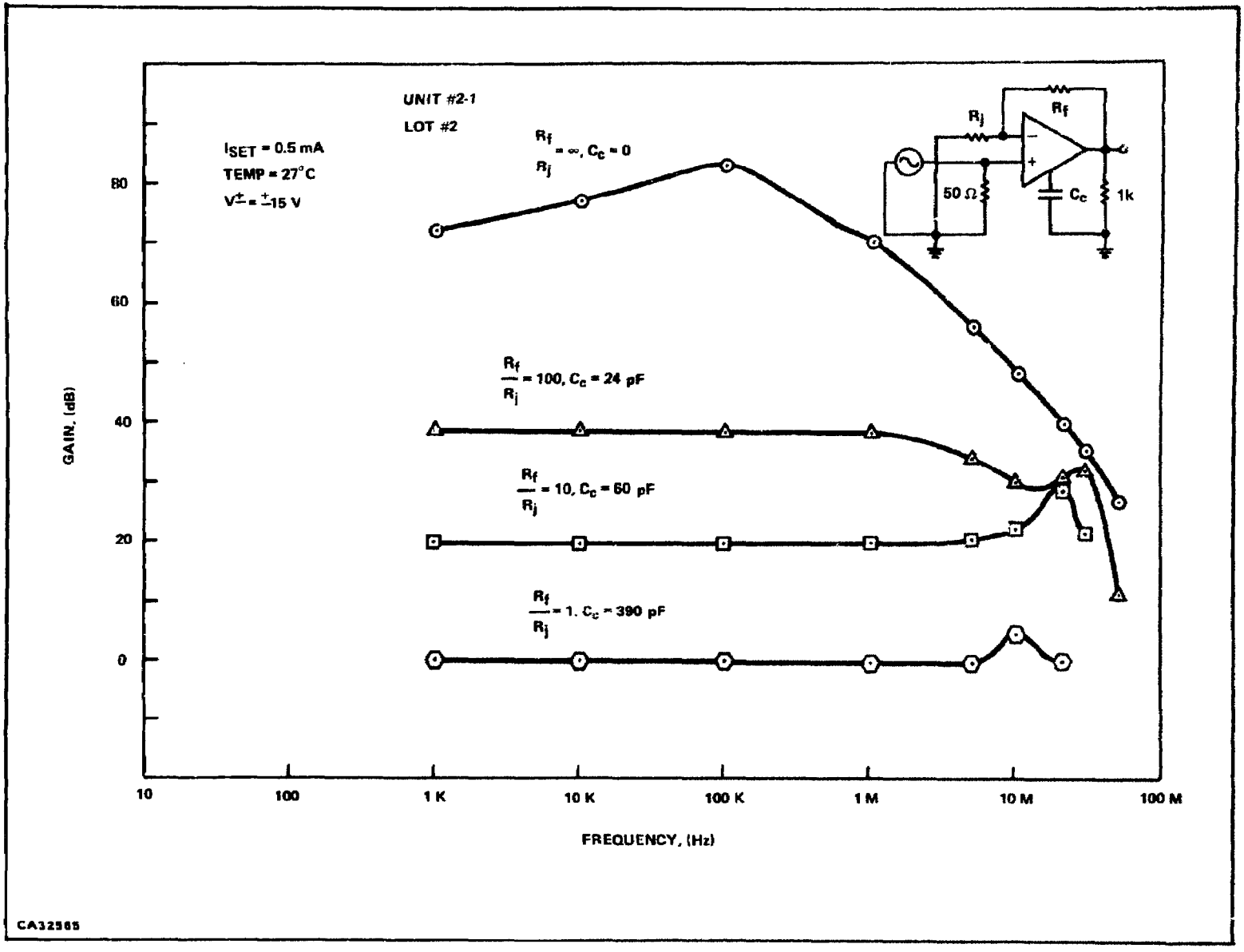


Figure 36. Open-Loop Frequency Response as a Function of Closed-Loop Gain at High Power Levels

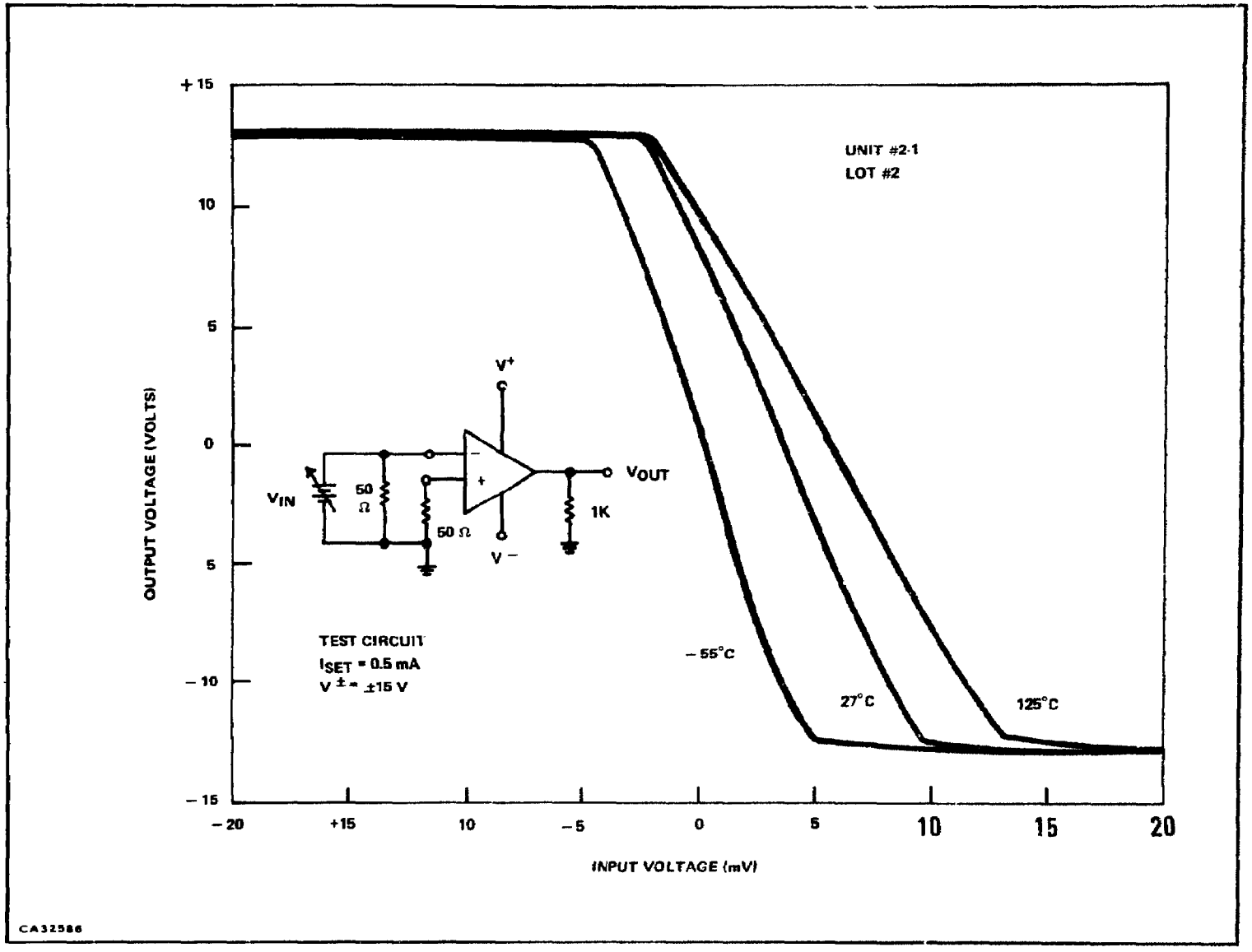


Figure 37. DC Open-Loop Transfer Characteristics at High Power Levels (Unit 2-1)

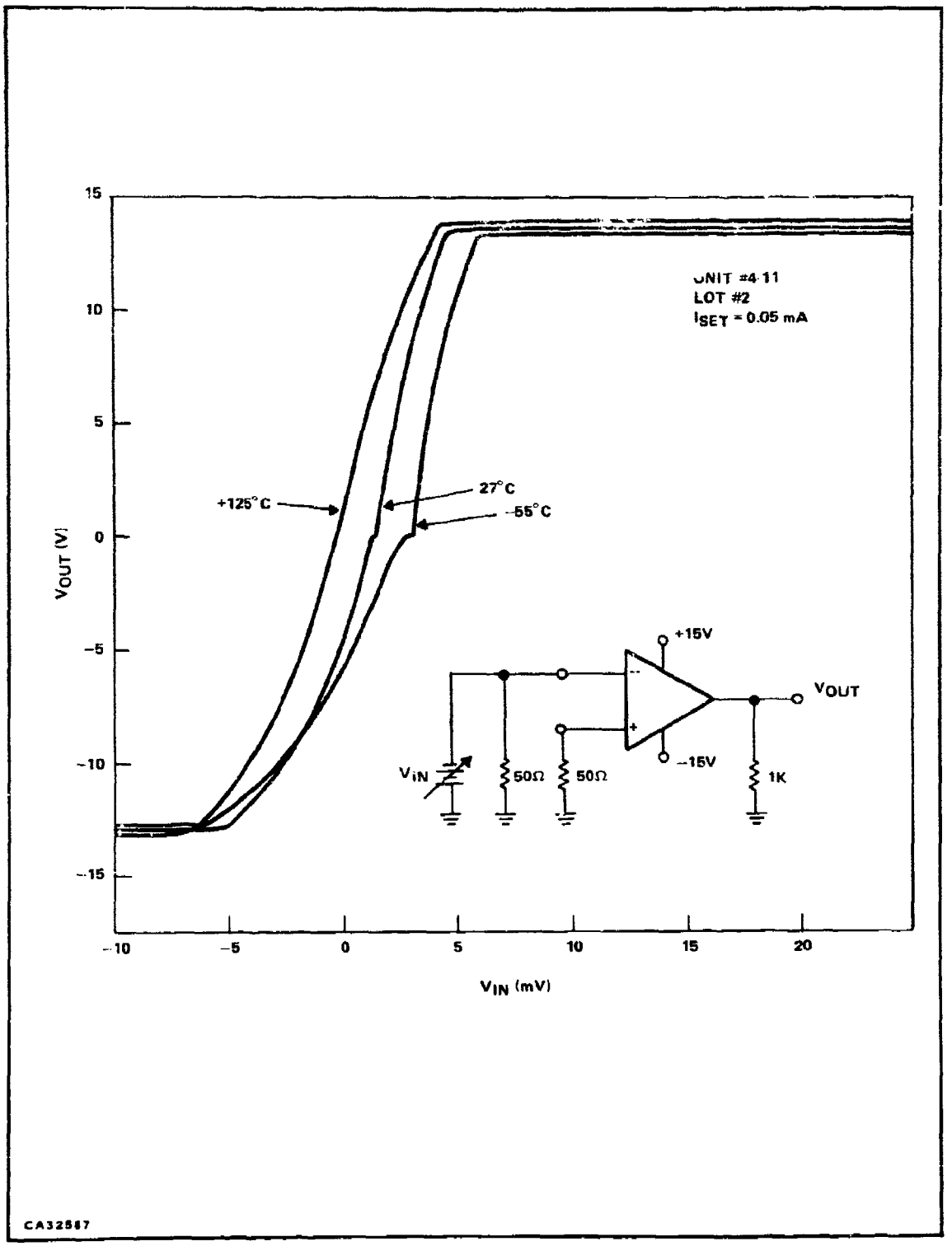


Figure 38. DC Open-Loop Transfer Characteristics at Low Power Levels (Unit 4-11)

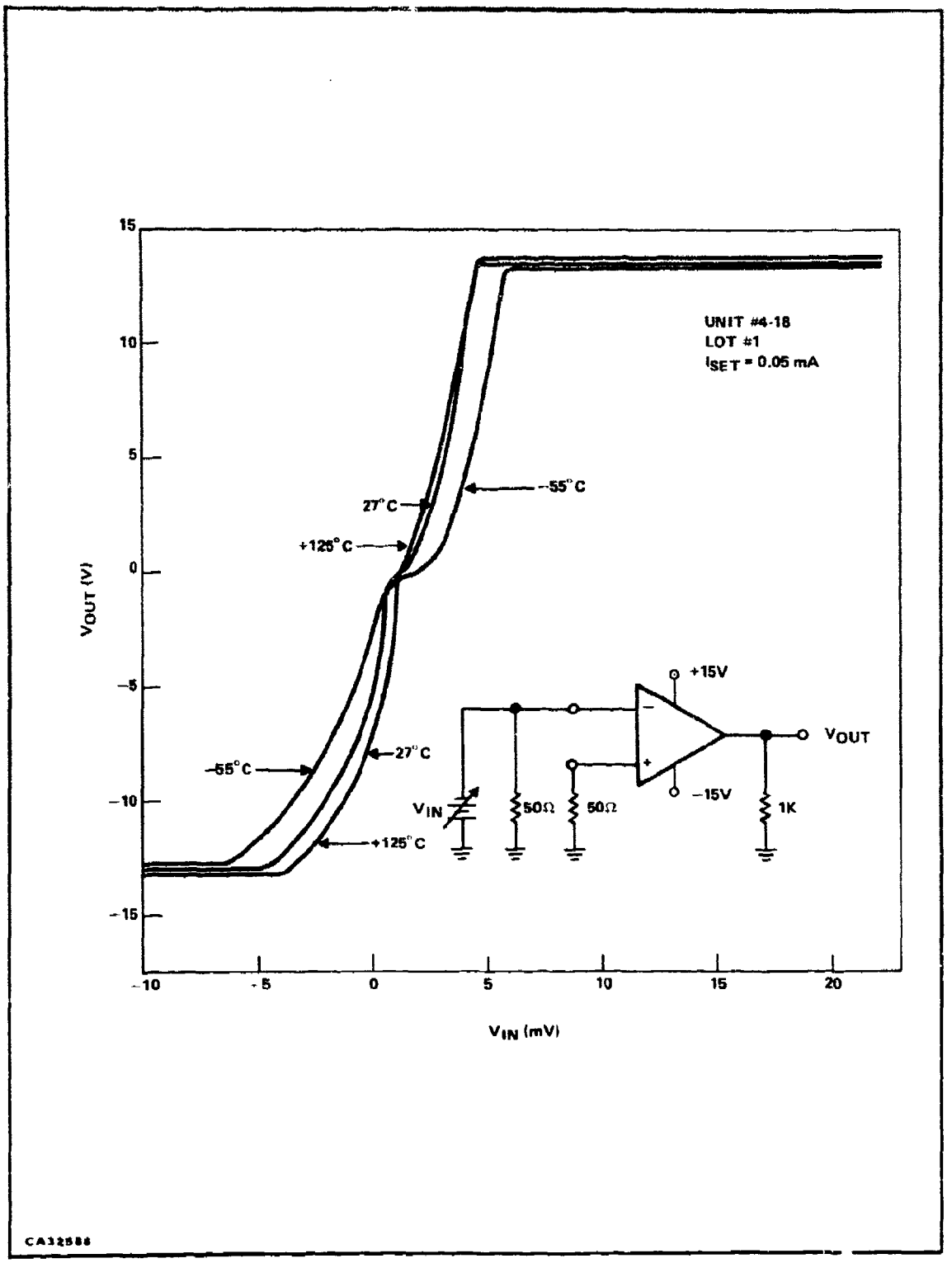


Figure 39. DC Open-Loop Transfer Characteristics at Low Power Levels (Unit 4-18)

The slew rate has been the parameter of most interest. Figure 40 demonstrates the fact that as the power dissipation is descreased, the open loop slew rate is not drastically affected. Since the open loop frequency response is becoming more stable at lower power, it would appear that the optimum power-speed trade off would be to decrease the power until the device is just unity gain stable. Notice that open loop slew rates in excess of 5000 V/μsec have been achieved.

The X776 was connected in a unity gain, voltage buffer configuration as shown in Figure 41. The compensating capacitor (C_C) was optimized at each power level. The device is becoming more stable as the power is decreased and therefore the capacitor can be decreased. At a set current of approximately 0.05 mA (P_D = 105 mW), the capacitor is not needed and the slew rate is essentially the open loop slew rate. A minimum slew rate of 2700 V/μsec at a power of 105 mW is achieved. As the set current is reduced even further (I_{SET} = 0.01 mA), the power does not decrease proportionally because the set current does not control the bias current and the power of the input stage. The input stage power is internally controlled and therefore the minimum power dissipation in the circuit is determined by the input stage.

The large-signal, open-loop slew characteristics for the four possible conditions are shown in Figure 42. These photographs were taken at a power dissipation of 555 mW (I_{SET} = 0.5 mA). The results of various devices are presented in Table II for various closed loop configurations. This data was taken at high power levels (approximately 600 mW). The unity gain slew responses for these units using the test circuit shown in Figure 43 are presented in Figures 44, 45, and 46. All slew rates are over 2500 V/μs at power dissipations of approximately 100 mW.

The device also has a minimum of overshoot. The large signal pulse response (nonslewing condition) is shown in Figure 47.

Typical screening data at a set current of 0.5 mA is shown in Table III and additional screening data taken at a set current of 0.05 mA is shown in Table IV. The input bias currents and offset voltage versus temperature for three units are summarized in Table V. The input offset voltage as a function of temperature is plotted for one of the devices in Figure 48.

The output characteristics are plotted in Figures 49 and 50. The short circuit currents are somewhat unbalanced but they do meet the 50 mA minimum output current requirement.

The input common mode rejection ratio for several devices is summarized in Table VI. The power supply rejection ratios are shown in Figure 51. Typical values of 50 to 80 dB were observed.

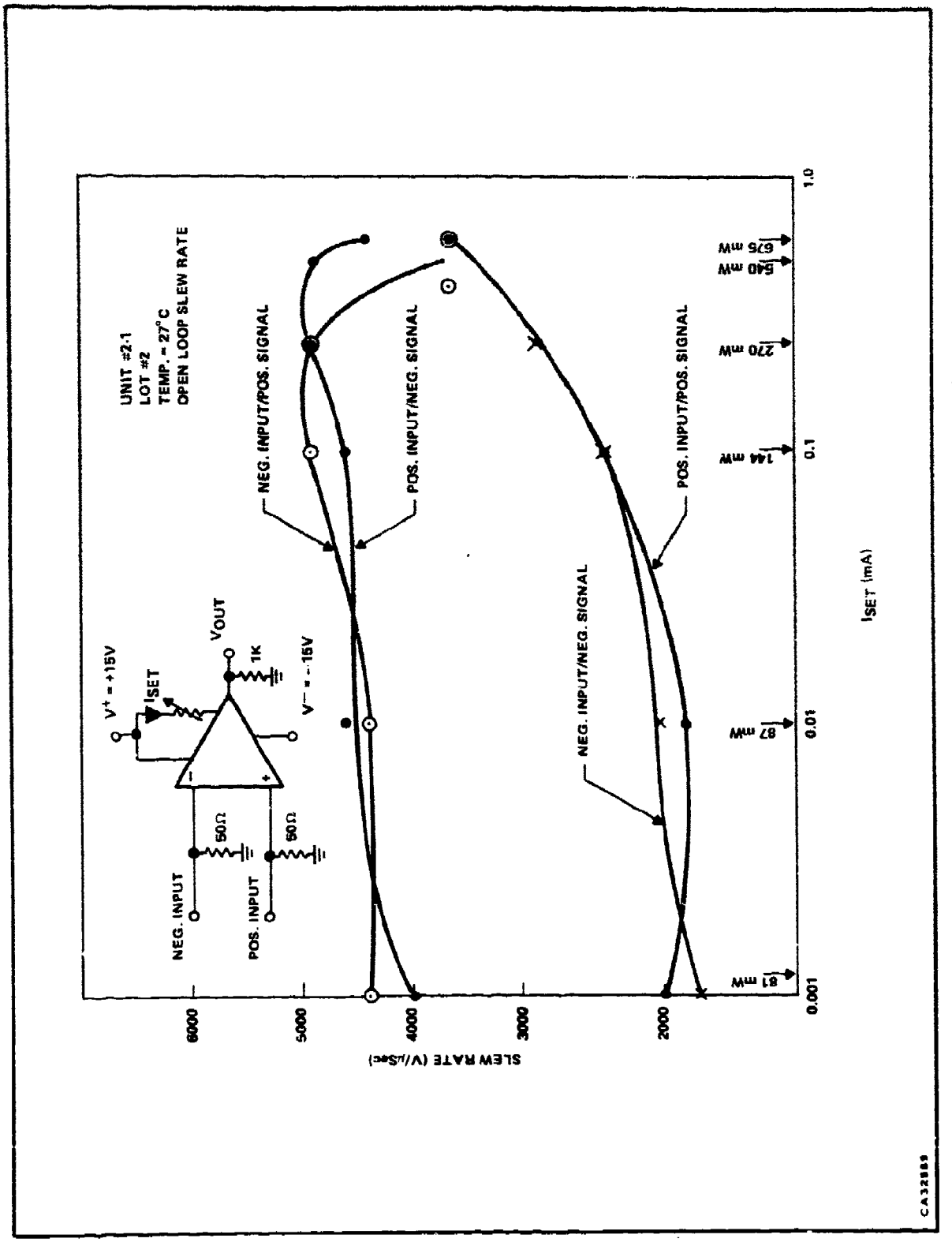


Figure 40. Open-Loop Slew Rate versus Power Dissipation

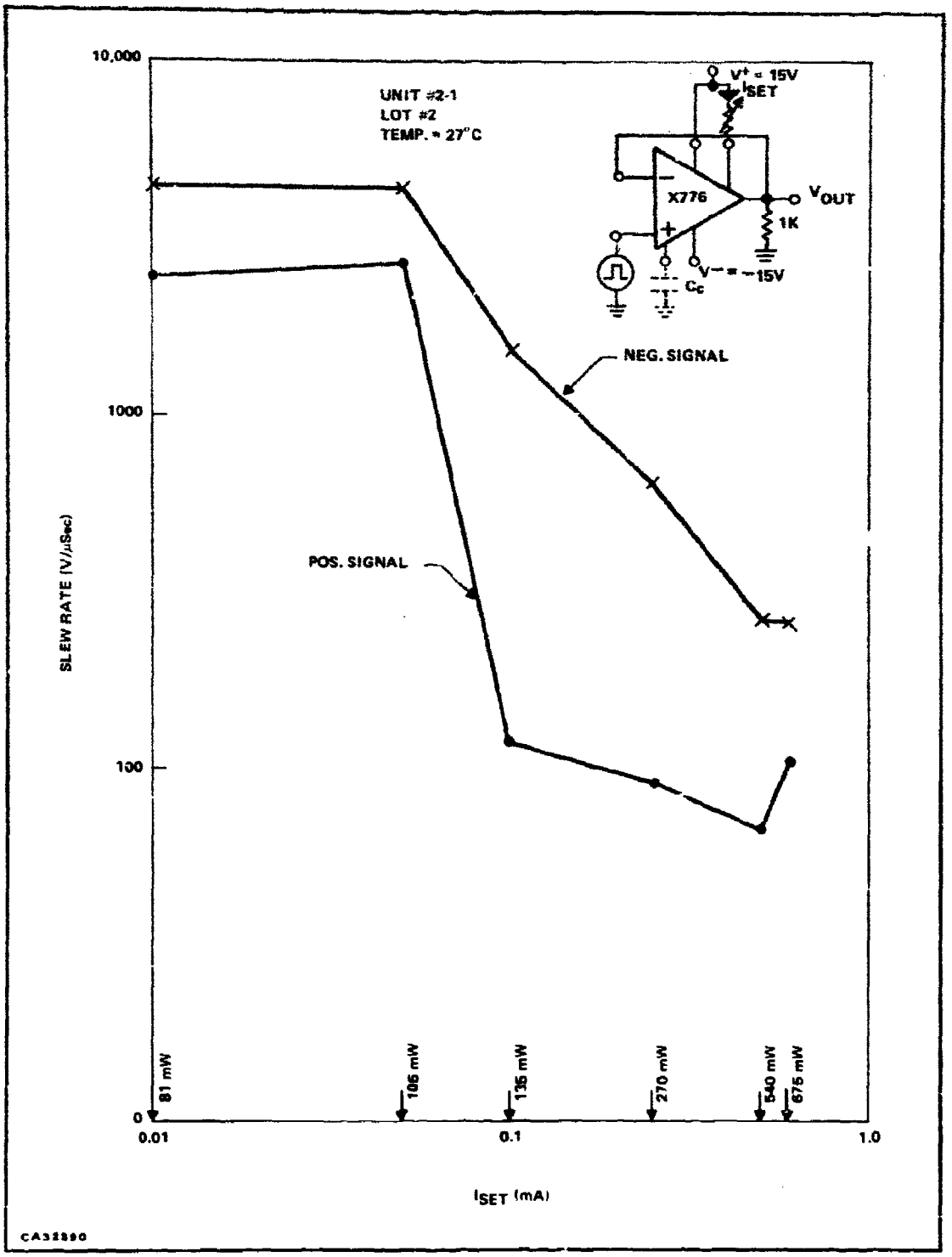


Figure 41. Unity Gain Slew Rate versus Power Dissipation

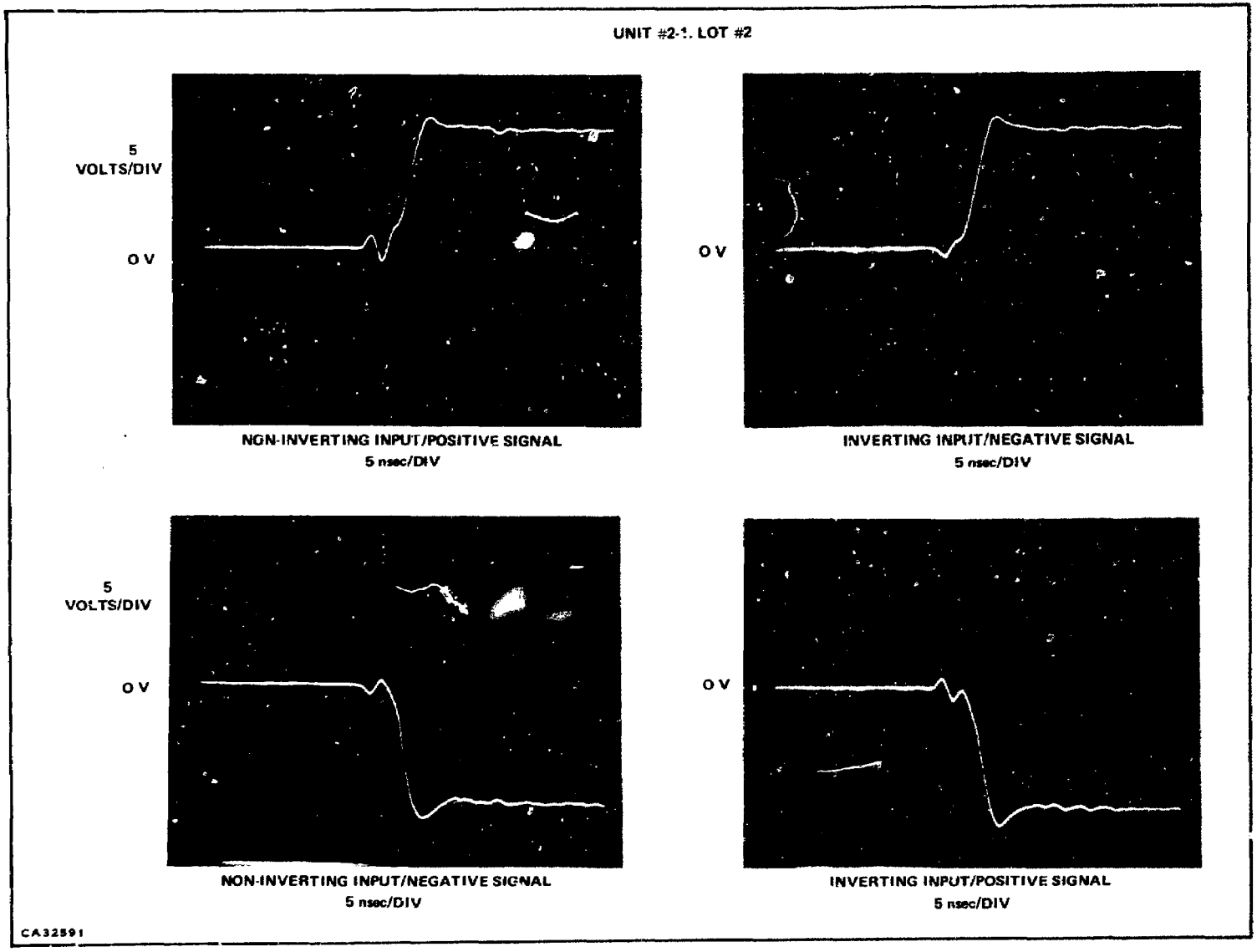
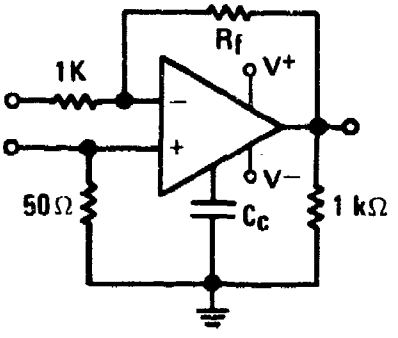


Figure 42. Open-Loop Slew Responses (I_{SET} = 0.5 mA)

Table II. Closed Loop Slew Rate Measurements Using Internal Node Compensation for High Power Dissipation

Unit Number	R_f kΩ	C_C pF	Positive Input		Negative Input	
			Pos. Signal	Neg. Signal	Pos. Signal	Neg. Signal
1-7	100	24	775	2330	1750	360
2-1	100	24	890	1970	1850	375
6-11	100	24	560	2100	1480	300
1-1	100	10	1410	3250	2950	465
1-7	10	50	340	770	650	230
2-1	10	50	405	720	720	260
6-11	10	50	285	680	540	215
1-1	10	50	260	700	540	205
1-7	1	390	32	38	34	32
2-1	1	390	35	55	32	33
6-11	1	390	27	30	27	25
1-1	1	390	26	28	27	24

CLOSED LOOP SLEW RATE (V/μsec)



I_{SET} = 0.5 mA
POWER SUPPLIES = ±15 VDC

TEST CONFIGURATION

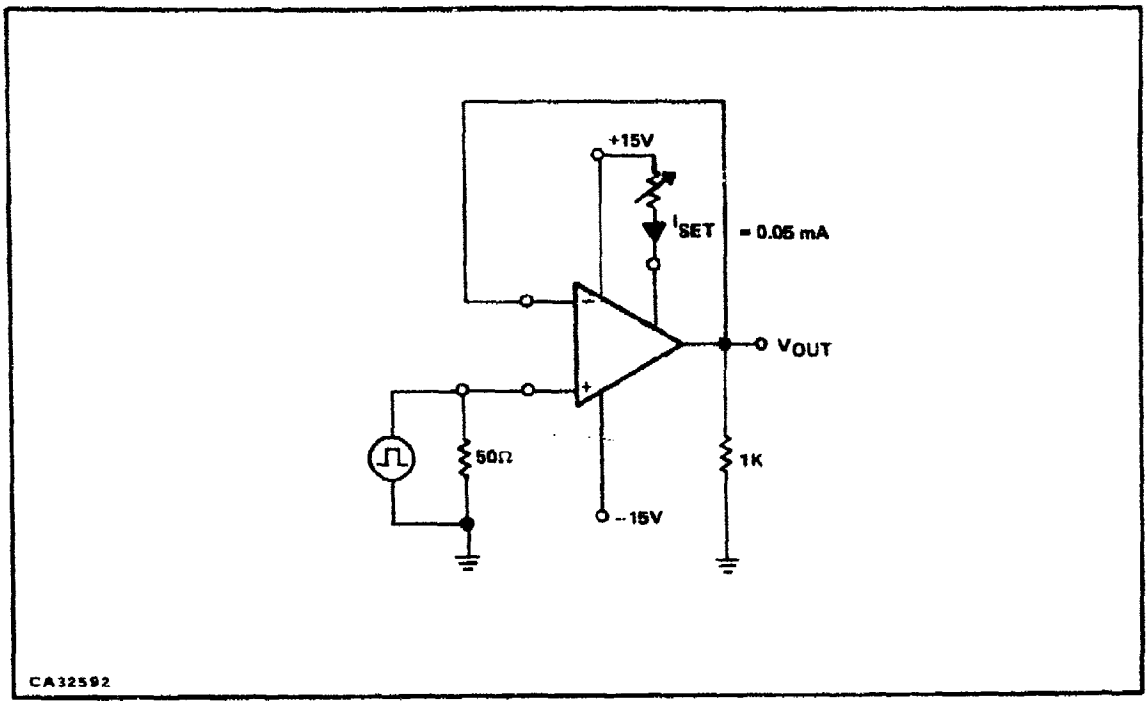


Figure 43. Unity Gain Test Circuit

The data for the X776 are summarized in the next two tables. Table VII summarizes the amplifier performance at a set current of 0.5 mA. Table VIII summarizes the amplier performance at a set current of 0.05 mA. The performance indicated in Table VIII meets the major requirements of this program.

Tables IX and X give a detailed specification covering the important parameters and the conditons under which they apply for the X776 operational amplifier. Table IX gives the operating conditons and maximum device ratings and Table X gives performance limits of the amplifier.

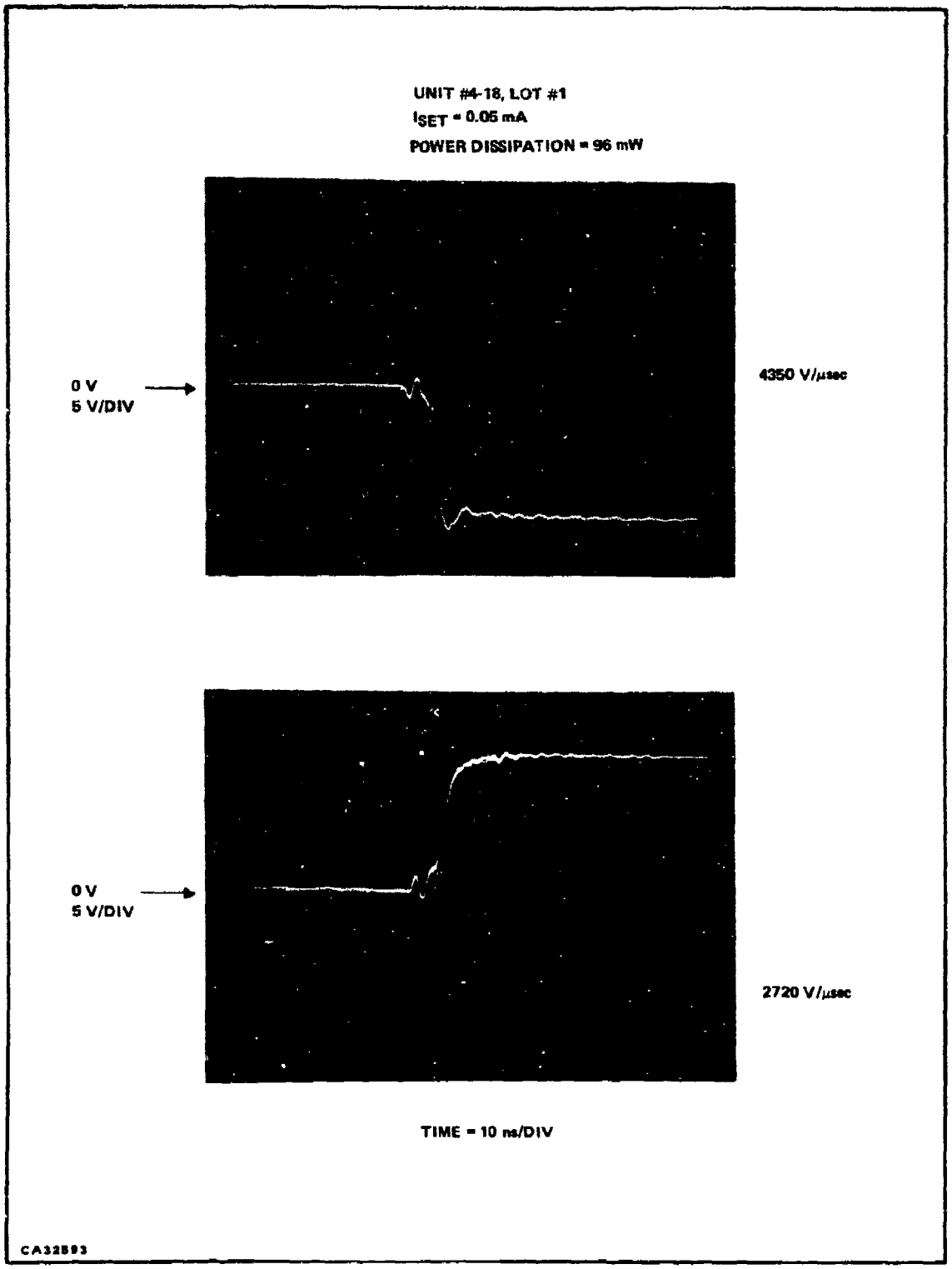


Figure 44. Unity Gain Slew Rate for Unit 4-18

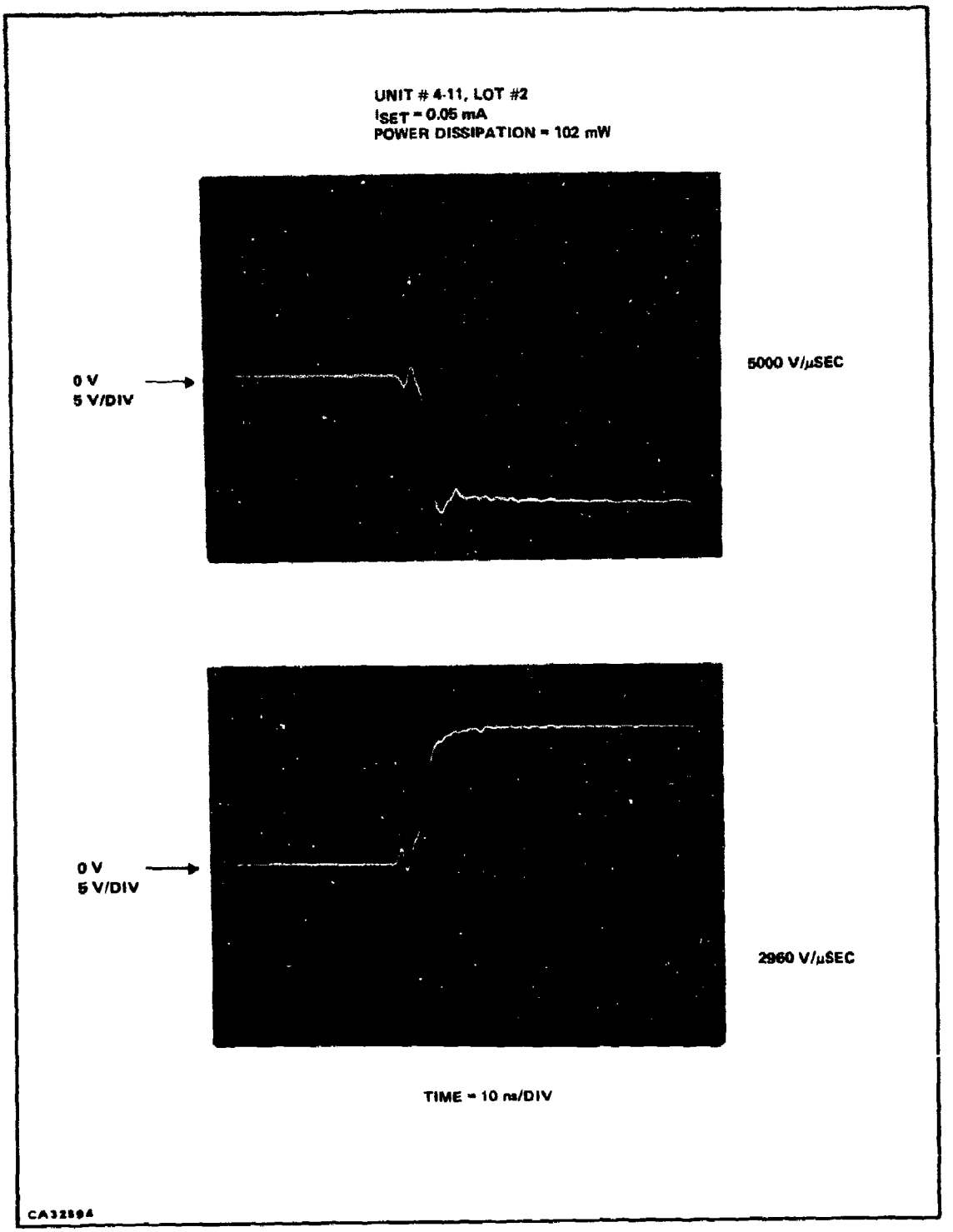


Figure 45. Unity Gain Slew Rate for Unit 4-11

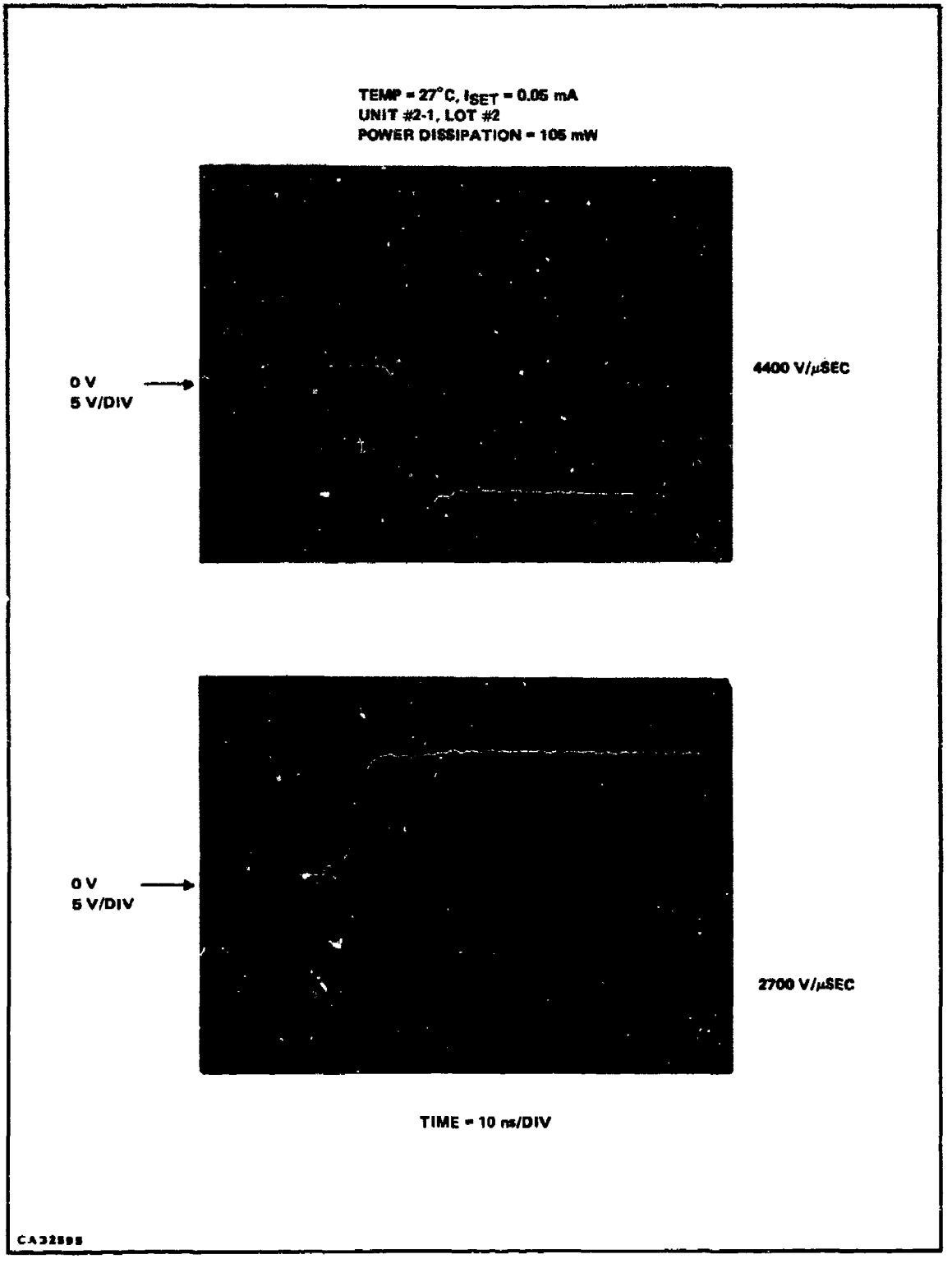


Figure 46. Unity Gain Slew Rate for Unit 2-1

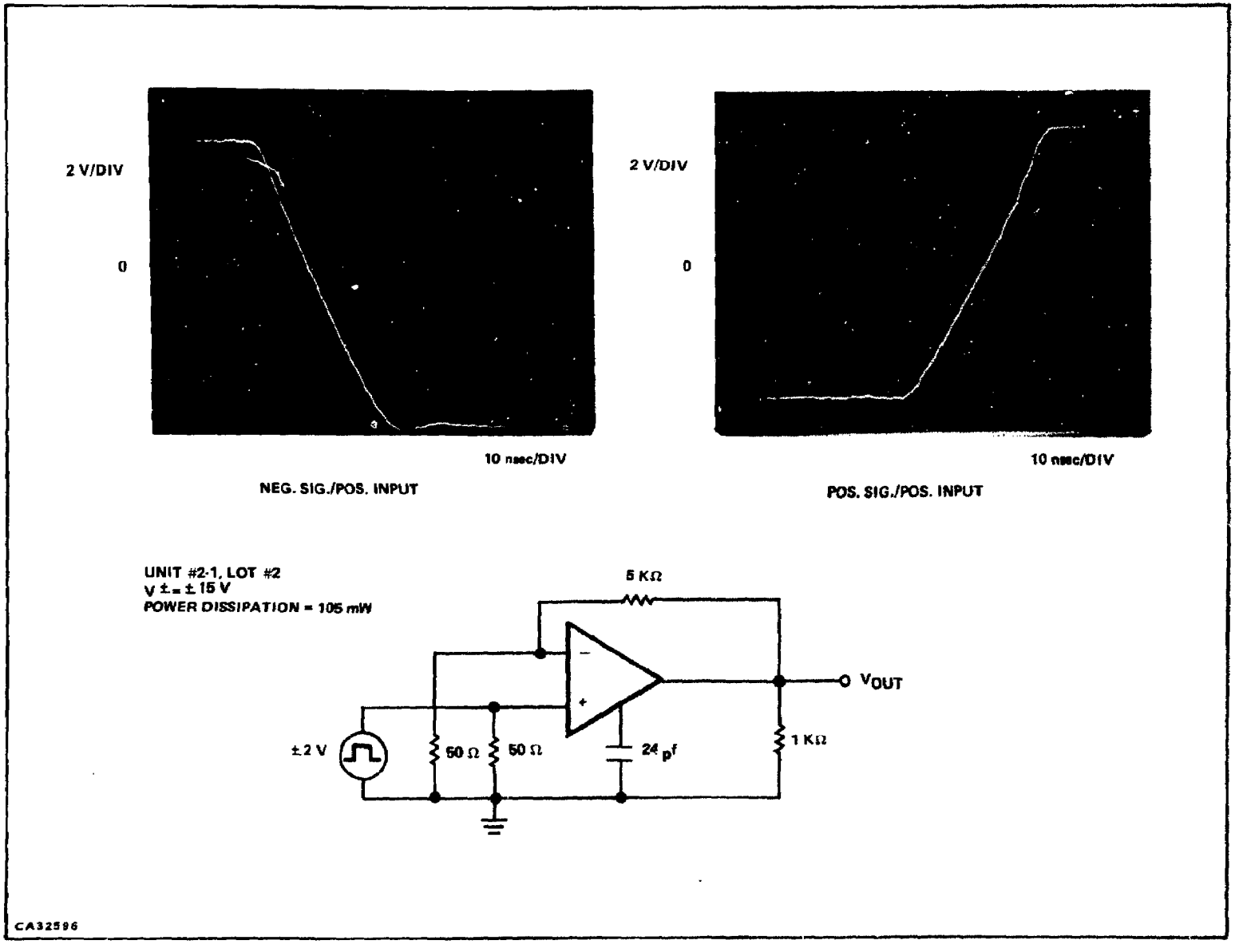


Figure 47. Large Signal Pulse Response

Table III. Typical Screening Data (I_{SET} = 0.5 mA)

Unit No.	Quiescent Power (mW)	Input Bias Current		Input Offset Current (μA)
		Pos. In. (μA)	Neg. In (μA)	
1-1	435	1.0	0.8	0.2
1-2	570	2.0	4.8	2.8
2-1	555	<0.1	<0.1	<0.1
2-3	630	1.0	1.8	0.8
6-2	600	2.0	1.0	1.0

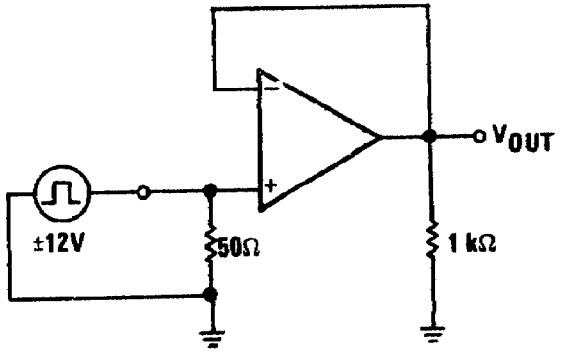
Unit No.	Short Circuit Current		Gain At 1 kHz (dB)	Open-Loop Slew Rate (V/μs)			
	V_{IN} = +1 V (mA)	V_{IN} = −1 V (mA)		Positive Input		Negative Input	
				Pos. Signal	Neg. Signal	Neg. Signal	Pos. Signal
1-1	260	100	72	3420	5420	3095	5000
1-2	250	67	71	3820	5420	3250	5000
2-1	280	73	73	4060	5420	3820	4640
2-3	220	70	72	4060	5420	3820	4330
6-2	130	140	71	3610	5910	3420	5000

Table IV. Screening Data Taken on Operable Units (I_{SET} = 0.05 mA)

Unit No.	Quiescent Power (mW)	Input Bias Current Pos. In. (μA)	Input Bias Current Neg. In. (μA)	Input Offset Current (μA)	Input Offset Voltage (mV)	Unity Gain Slew Rate (V/μSec) Pos. Signal	Unity Gain Slew Rate (V/μSec) Neg. Signal
1-4-1	90	0.3	0.3	< 0.1	4.0	2350	3450
1-4-14	90	1.1	1.2	0.1	4.0	2550	3450
1-4-18	96	0.4	0.5	0.1	1.0	2300	3250
2-4-11	102	0.6	0.5	0.1	1.0	2700	3650
2-6-15	117	0.6	0.8	0.2	< 1.0	1750	3450

TEST CONDITIONS:

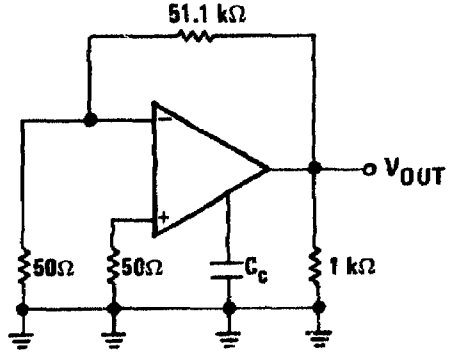
I_{SET} = 0.05 mA
R_L = 1 kΩ
$V^{\pm}$ = ± 15 VOLTS
T_A = 27°C



TEST CIRCUIT FOR UNITY GAIN SLEW RATE MEASUREMENTS

Table V. Input Bias Current and Offset Voltage Temperature Characteristics

Ambient Temperature (°C)	Unit #4-11, Lot #2, I_{SET} = 0.05 mA			Unit #4-18, Lot #1, I_{SET} = 0.05 mA			Unit #2-1, Lot #2, I_{SET} = 0.5 mA		
	Input Bias Current		Input Offset	Input Bias Current		Input Offset	Input Bias Current		Input Offset
	Pos. In. (μA)	Neg. In. (μA)	Voltage (mV)	Pos. In. (μA)	Neg. In. (μA)	Voltage (mV)	Pos. In. (μA)	Neg. In. (μA)	Voltage (mV)
−55	0.2	1.8	−1.8	0.2	0.6	−0.7	1.0	1.3	−0.1
−35	0.1	1.3	−1.7	0.2	0.2	−0.8	0.6	1.3	+0.7
−15	0.1	1.0	−1.5	0.3	0.3	−0.9	0.4	1.0	+1.4
+5	0.3	0.5	−1.2	0.2	0.2	−0.9	0.4	1.2	+1.9
+25	0.4	1.2	−1.0	0.4	0.6	−0.9	0.4	1.4	+2.3
+45	0.6	1.1	−0.7	0.4	0.4	−0.9	0.3	0.8	+2.7
+65	0.4	0.8	−0.4	0.3	0.4	−0.9	0.2	0.5	+3.0
+85	1.0	0.3	−0.2	0.4	0.8	−1.0	0.2	0.3	+3.2
+105	1.3	0.2	+0.1	0.2	0.1	−1.0	0.1	0.9	+3.4
+125	1.6	0.1	+0.2	0.2	0.2	−1.0	0.1	1.6	+3.5



$V^{\pm}$ = ± 15 V
C_c = 1000 pF

TEST CONFIGURATION

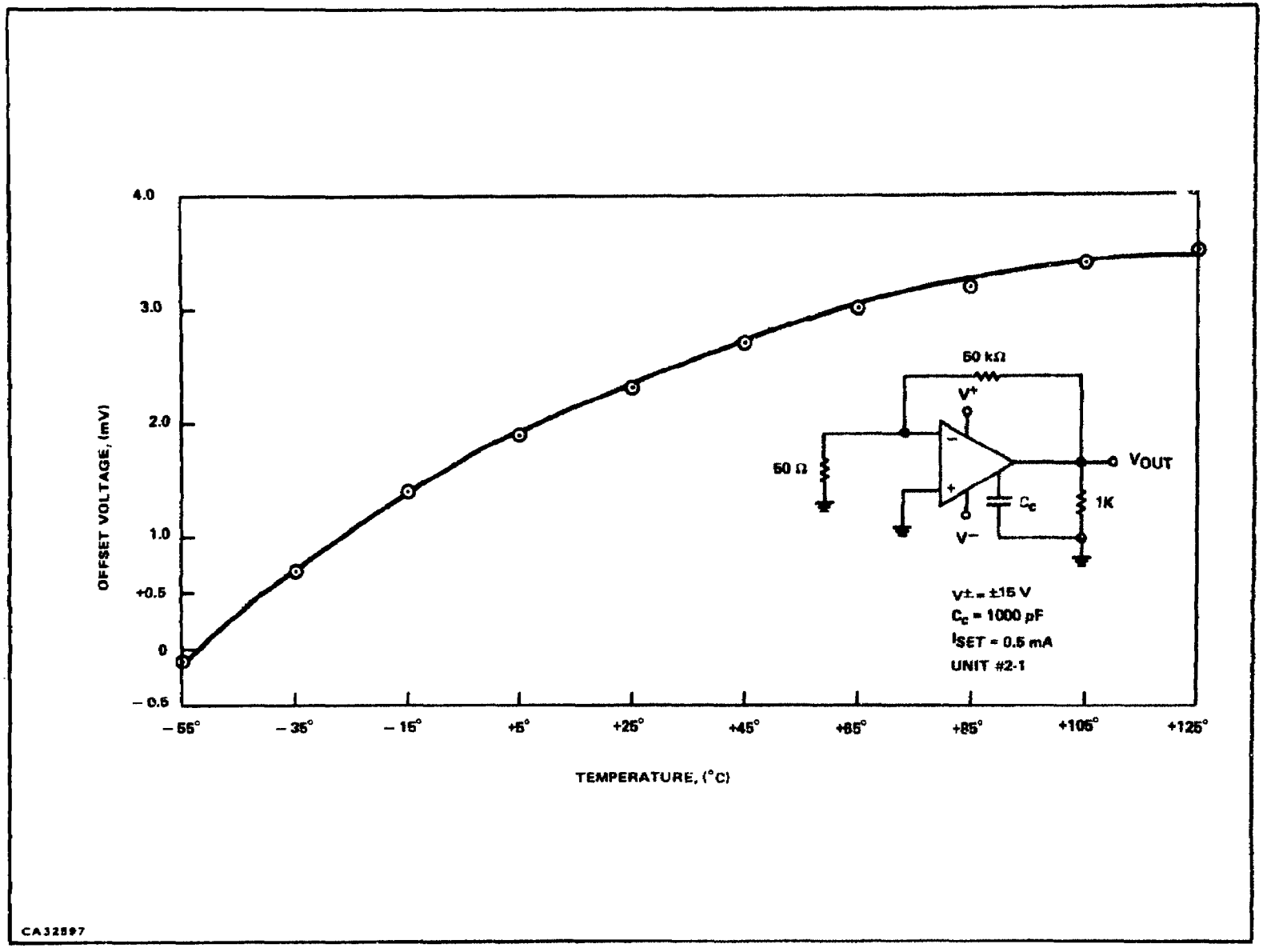


Figure 48. Input Offset Voltage as a Function of Temperature

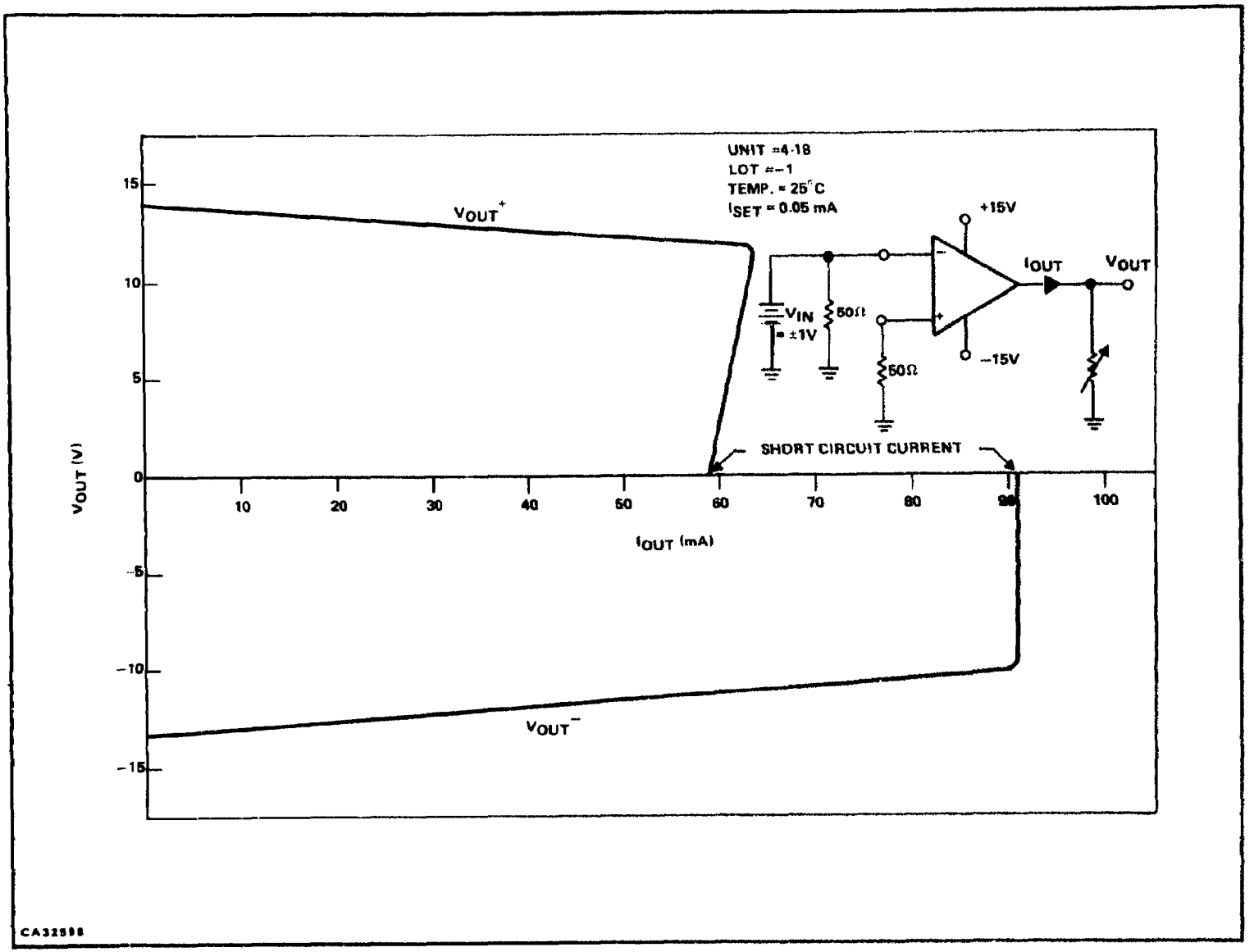


Figure 49. Output Characteristics for Unit 4-18

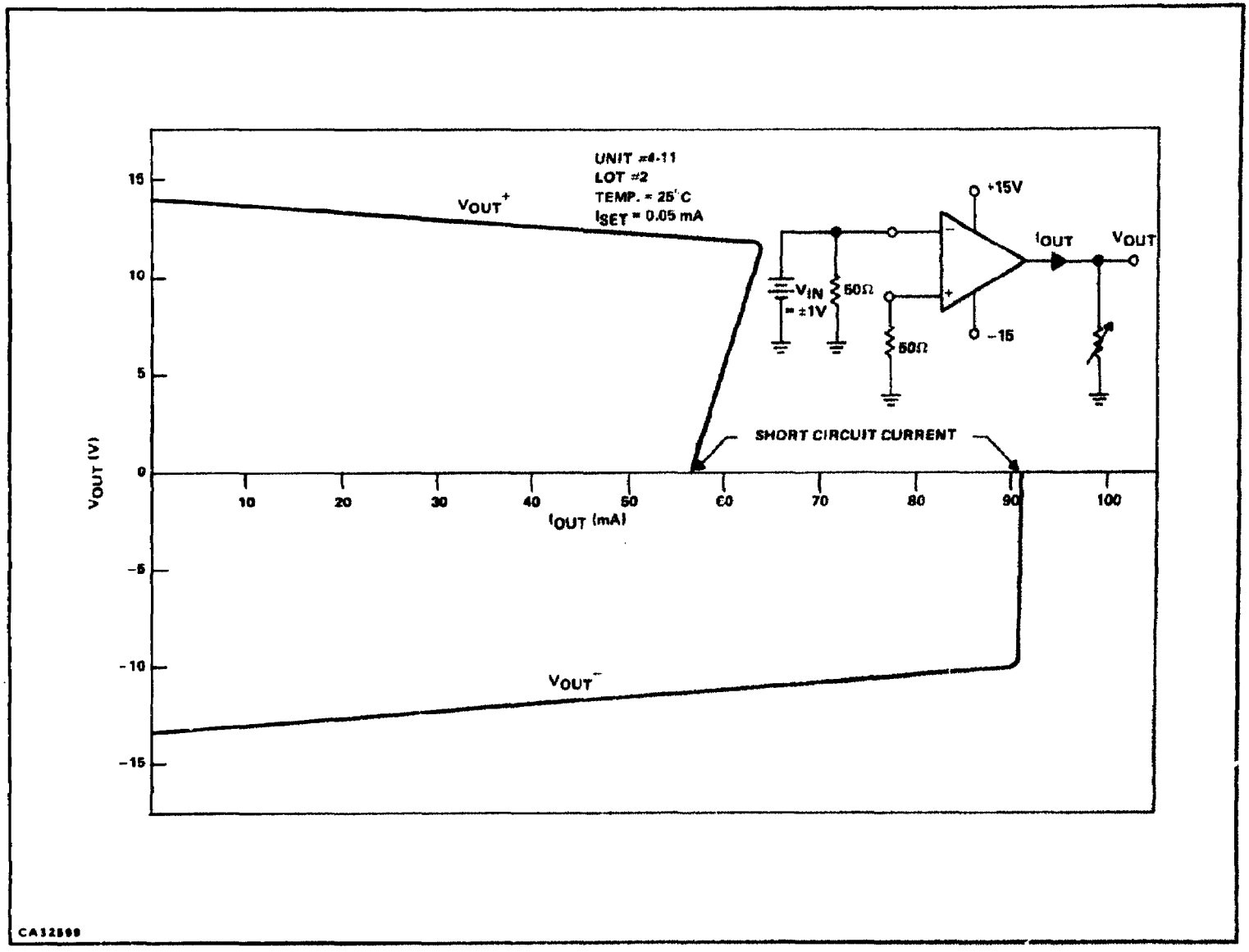
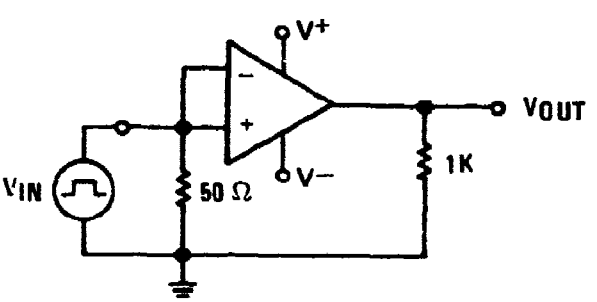


Figure 50. Output Characteristics for Unit 4-11

Table VI. Input Common Mode Rejection Ratio

Unit Number	CMRR, dB	
	Positive	Negative
1-1	75.7	73.4
1-7	73.4	70.4
2-1	68.0	71.6
6-11	70.4	66.0
9-11	62.8	62.4
9-17	70.0	63.8

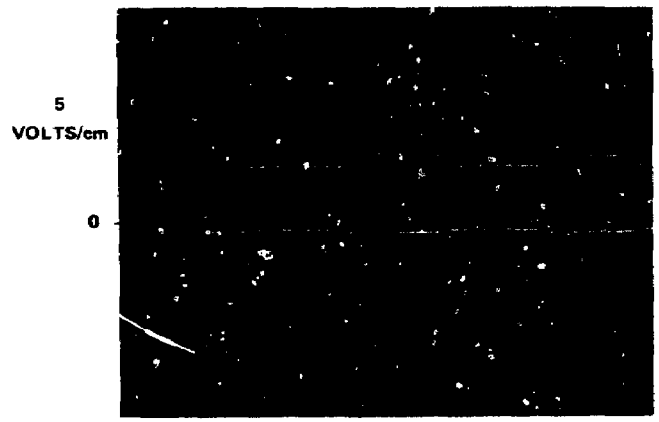
TYPICAL COMMON MODE REJECTION RATIO VALUES

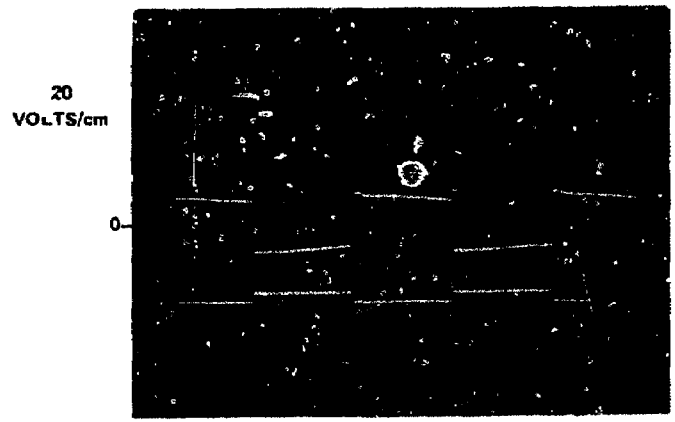


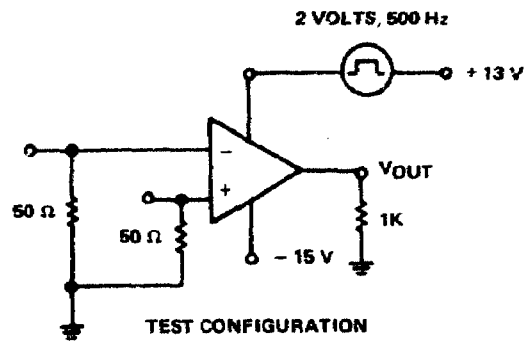
POWER SUPPLY = ±15 V

V_{IN} = ±2 V

I_{SET} = 0.5 mA







CA32600

Figure 51. Power Supply Rejection Response

Table VII. X776 High Slew Rate Operational Amplifier Performance
(I_{SET} = 0.5 mA)

	Goals	Typical Perf. @ I_{SET} = 0.5 mA
Open Loop Voltage Gain	84 dB Min	70 dB Min
Setting Time to .1%	50 nS Max	25 nS
Slew Rate (Open Loop)	2500 Volts/μSec	> 3000 V/μSec
Input Voltage Range	± 10 Volts Min	± 10 Volts
Output Voltage Swing	± 8 Volts Min	± 12 Volts
Output Current	50 mA Min	75 mA
Gain Roll Off	6 dB/Octave	2 Slopes
Supply Voltage	± 15 Volts	± 15 Volts Max
Operating Temperature Range	–55°C to +125°C	–55°C to +125°C
Input Offset Drift		
Current	0.1 nA/°C Max	7 nA/°C
Voltage	1 μV/°C	20 μV/°C
Positive Power Supply Voltage Rejection Ratio	–	80 dB
Negative Power Supply Voltage Rejection Ratio	–	50 dB
Input Offset Voltage	–	± 5 mV
Input Bias Current	–	< 10 μA
Input Offset Current	–	< 10 μA
Power Consumption	–	600 mW
Unity Gain Bandwidth	–	50 MHz

Table VIII. X776 High Slew Rate Operational Amplifier Performance
(I_{SET} = 0.05 mA)

	Goals	Typical Perf. @ i_{SET} = 0.05 mA
Open Loop Voltage Gain	84 dB Min	70 dB Min
Setting Time to .1%	50 nS Max	25 nS
Slew Rate (Unity Gain)	2500 Volts/μSec	>2500 V/μSec
Input Voltage Range	± 10 Volts Min	± 10 Volts
Output Voltage Swing	± 8 Volts Min	± 12 Volts
Output Current	50 mA Min	50 mA
Gain Roll Off	6 dB/Octave	6 dB/Octave
Supply Voltage	± 15 Volts	± 15 Volts Max
Operating Temperature Range	–55°C to +125°C	–55°C to +125°C
Input Offset Drift		
Current	0.1 nA/°C Max	7 nA/°C
Voltage	1 μV/°C	20 μV/°C
Positive Power Supply Voltage Rejection Ratio	–	80 dB
Negative Power Supply Voltage Rejection Ratio	–	50 dB
Input Offset Voltage	–	± 5 mV
Input Bias Current	–	< 10 μA
Input Offset Current	–	< 10 μA
Power Consumption	–	105 mW
Unity Gain Bandwidth	–	50 MHz

Table IX. Operating Conditions and Absolute Maximum Rating

Operating conditions.	
Supply voltage range	±5 to ±15 Vdc
Ambient temperature range	–55° to +125°C
Absolute maximum ratings.	
Supply voltage range	±18 Vdc
Input common-mode voltage range	±12 Vdc 1/
Differential input voltage range	±10 Vdc
Storage temperature range	–65° to +150°C
Output short-circuit duration	Unlimited 2/
Lead temperature (soldering, 60 sec)	300°C
Junction temperature	T_J = 150°C 3/

1/ For supply voltages less than ±15 Vdc, the maximum input common mode voltage is equal to the supply voltage minus ±3 volts.

2/ Short circuit is applied to ground. Rating applies to +125°C case temperature or +75°C ambient temperature. I_{SET} = 0.05 mA.

3/ For short term test (168 hours, maximum) T_J = 275°C.

Table X. Electrical Performance Characteristics

Characteristic	Symbol	Conditions	Limits Min	Limits Max	Units
Input offset voltage	V_{IO}	$V\pm = \pm 15$ V $T_A = 25^\circ C$		±10	mV
		$-55^\circ C \leq T_A \leq 125^\circ C$		±12	mV
		Test Circuit: See Fig. 48			
Input offset voltage temperature sensitivity	$\frac{\Delta V_{IO}}{\Delta T}$	Test Circuit: See Fig. 48		±20	μV/°C
Input offset current	I_{IO}	$V\pm = \pm 15$ $T_A = 25^\circ C$		±5.0	μA
		$-55^\circ C < T_A < 125^\circ C$		±7.0	μA
		Test Circuit: See Table V			
Input offset current temperature sensitivity	$\frac{\Delta I_{IO}}{\Delta T}$	$-55^\circ C \leq T_A \leq 125^\circ C$ Test Circuit: See Table V		20	nA/°C
Input bias current	I_{IB}	$V\pm = \pm 15$ V $T_A = 25^\circ C$		5.0	μA
		$-55^\circ C \leq T_A \leq 125^\circ C$		7.0	μA
		Test Circuit: See Table V			
Power supply rejection ratio	+PSRR	$V\pm = \pm 15$ V $T_A = 25^\circ C$ Test Circuit: See Fig. 51	−70		dB
Power supply rejection ratio	−PSRR	$V\pm = \pm 15$ V $T_A = 25^\circ C$ Test Circuit: See Fig. 51	−50		dB
Input voltage common mode rejection	CMRR	$V\pm = 15$ V $V_{IN} = \pm 2$ V Test Circuit: See Table VI	60		dB
Adjustment for input offset voltage	V_{IO} ADJ	$V\pm = \pm 15$ V	±12		mV

Table X. Electrical Performance Characteristics (Continued)

Characteristic	Symbol	Conditions	Limits Min	Limits Max	Units
Output short circuit current (for positive output)	$I_{OS(+)}$	Test Circuit: See Fig. 49	50	150	mA
Output short circuit current (for negative output)	$I_{OS(-)}$	Test Circuit: See Fig. 49	50	150	mA
DC power dissipation per amplifier	P_D	$-55°C < T_A < 125°C$ $I_{SET} = 0.05$ mA $V_{OUT} = 0$		150	mW
Output voltage swing (maximum peak to peak)	$V_{O:PP}$	$\pm V_{CC} = 15$ V, $R_L = 2$ KΩ	20		V
Open loop voltage gain	$A_{VS(\pm)}$	$\pm Vcc = 15$ V $T_A = 25°C$ $R_L = 2K\Omega$ $-55°C < T_A < 125°C$ $V_{OUT} = \pm 2.0$ V Test Circuit: See Fig. 38	70 65		dB dB
Slew rate	SR	$\pm Vcc = 15$ V Closed loop $V_{IN} = \pm 10$ V voltage gain = 1 See Fig. 43	2000		$\frac{V}{usec}$
Settling time	TS	$\pm Vcc = 15$ V ±0.1% See Fig. 43	50		nsec
Overshoot		Test Circuit: See Fig. 43	20		%
Bandwidth 1/	BW		50		MHz

1/ Calculated value from: $BW\ (MHz) = \frac{0.35}{\text{Rise time (usec)}}$

Note: These electrical performance characteristics apply over the full operating ambient temperature range of −55°C to 125°C and for supply voltages of ±5 Vdc to ±15 Vdc, unless otherwise specified.

SECTION III
ASSESSMENT OF CURRENT TECHNOLOGY

The present design has utilized the best available technology to achieve a high speed monolithic operational amplifier.

The use of a dielectrically isolated structure allowed complementary transistor structures with low parasitic capacitance values to be fabricated. Improvements in speed can be achieved by using better isolation structures which would result in lower parasitic capacitances. Further improvements could be achieved through the use of high frequency transistors with shallow junctions and reduced geometries. A junction field effect transistor compatible with the complementary bipolar technology would yield improvements in input characteristics.

The circuit was designed to achieve the maximum slew rate attainable with a single stage in order to avoid the need for compensating capacitances. Higher voltage gain per stage can be achieved with an improved current source design. Improved input bias compensation configurations have been demonstrated that can be used to lower the input bias current of this circuit. Other areas where performance could be enhanced by improvements in circuit design include optimizing current levels, improving output short circuit current limiting, and providing slew detection circuitry.

SECTION IV
SUMMARY

The X776 high-performance operational amplifier has been designed and developed. Its performance has been characterized and the results are detailed in this report.

The amplifier was designed with special emphasis placed on attaining high slew rate and fast settling time. Both of these objectives were met; the amplifier is extremely fast and is stable in a unity gain configuration – an important feature for system applications.

There are two areas where the amplifier does not meet the design goals: input characteristics and open-loop gain. The input bias currents obtained are not as low as might have been attained using an FET input stage; however, the input characteristics are more stable with variations in temperature than an FET input stage would be. The open-loop gain – typically 72 dB – is also less than the design goal of 84 dB, but is sufficient for most system applications for amplifiers of this type.

Twenty-two units were delivered to AFAL on 9 March 1973, in partial fulfillment of the contract requirements. An additional 13 units, mounted in special headers, were also delivered at the request of AFAL.

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13. ABSTRACT

A high-performance, monolithic operational amplifier has been designed and developed. It incorporates the latest state-of-the-art circuit design techniques and fabrication technology to achieve the best performance available with current production processes. Special attention was placed on achieveing high slew rate and fast settling time. Unity gain slew rates of over 2500 V/μsec and settling times of under 50 ns were achieved at power dissipation levels of approximately 100 mW. The design was kept as simple as possible to eliminate excess parasitic capacitances and to be operated at the optimum power-speed condition for a given application.

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Unity Gain Slew Rate						
Settling Time						
Bandwidth, Amplifier						