Technical Report No. 170

SACLANT ASW
RESEARCH CENTRE

A HIGH-DENSITY DIGITAL RECORDING SYSTEM FOR UNDERWATER SOUND STUDIES

by

ALESSANDRO BARBAGELATA, ALAIN CASTANET,
ROBERT LAVAL and MARIO PAZZINI

15 JULY 1970

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APPROVED FOR DISTRIBUTION

Ir M.W. van Batenburg
Director

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A HIGH-DENSITY DIGITAL RECORDING SYSTEM FOR UNDERWATER SOUND STUDIES

By

Alessandro Barbagelata, Alain Castanet,
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ABSTRACT

A high-density digital recording system is described that allows the conversion from analogue to digital form of up to twenty input analogue channels, their recording on magnetic tape, their readback from tape, and their transfer to a digital computer. The heart of the system is a standard 14-track analogue instrumentation tape-recorder, of the wide-band type, working in direct-recording mode at a speed of 30 in/s and used for digital recording at a density of about 12 kilobits per inch and per track. A total data recording rate of 2 880 kilobits per second is achieved with ten magnetic tracks. The system has been successfully tested during various sea trials and is now fully operational.

INTRODUCTION

Data collected during sound propagation trials at sea are normally stored on magnetic tape before analysis. Analogue instrumentation tape-recorders in FM mode have so far been used for this purpose but the technique has many disadvantages:

a) A frequency band ranging from a few hertz up to 15 kHz to 20 kHz is normally needed in our investigations. For such a frequency band, a maximum dynamic range of 40 dB can be achieved, so that a precise adjustment of the gain of the receiving system becomes critical. Furthermore our sea trials are mainly based on the use of explosive charges, i.e. on the study of the impulse response of the medium. Thus the signals dealt with require the highest possible dynamic range.

b) The tape-recorder's time base is not precise because tape speed is not constant. This introduces errors in the measurement of power-spectra when high frequency resolution is required. Angular movement of the tape (skew) introduces relative time fluctuations between the various channels and prevents precise cross-correlation measurements.

Analogue signal-analysis techniques have many limitations. In general, the accuracy of the results is rather poor. The risk of errors is great because human intervention is necessary at each stage of the operation. Each time a new type of analysis has to be undertaken, a new measurement set-up is necessary. Furthermore, numerous problems connected with the treatment of random functions are almost impossible to solve by means of analogue signal-processing.

The use of digital techniques both for recording and for analysis allows all these limitations to be overcome. Signals are digitized during the experiment and recorded on magnetic tape in digital form. The digitally recorded data can be edited and processed in the laboratory, and data can be transferred to a digital computer for analysis.

Standard, computer-type, digital tape-recorders cannot be used for our purposes as their information recording rate is still one order of magnitude lower than our needs.

For this reason a high-density digital recording system has been developed and built. The system employs a standard 14-track analogue instrumentation tape-recorder, of the wide-band type, working in direct recording mode.

The complete system allows the conversion from analogue to digital form of up to twenty analogue channels, their recording on magnetic tape, their read-back from tape, and their transfer to a digital computer. The digital recording system is now fully operational and has been successfully employed in various sea trials.

1. GENERAL DESCRIPTION OF THE SYSTEM

1.1 Summary of the Main Characteristics

The main features of the digital recording system are the following.

1.1.1 Analogue Input

a) Number of channels: up to 20 simultaneous data inputs.

b) Channel bandwidth:

50 Hz to 16 kHz (6 dB freq.) for up to 5 input channels.
50 Hz to 8 kHz (6 dB freq.) for up to 10 input channels.
50 Hz to 4 kHz (6 dB freq.) for up to 20 input channels.

c) Input signal level: given by ±10 volts peak divided by the voltage gain of the input amplifier.

d) Voltage gain: from 0 dB to 72 dB (divided in two overlapping ranges of from 0 to 48 dB and from 24 to 72 dB).

e) Input impedance: 1.0 MΩ shunted by 100 pF for each input amplifier.

f) Low-pass filters: inserted between input amplifiers and A/D converters for folding-effect reduction. Filters are plug-in type, with cut-off frequencies of 16 kHz, 8 kHz, or 4 kHz (6 dB points). The filter configuration has to be varied according to channel configuration.

g) Filter, main characteristics:

- Group delay is constant in the pass-band within 1%.

-Overshoot in the step response is less than 1%.

1.1.2 Analogue Multiplexers

Each of the five A/D converters employed is provided with an input multiplexer allowing up to four analogue inputs to be sequentially sampled.

1.1.3 A/D Converters

a) Resolution: 15 binary bits including sign.

b) Sample-and-hold aperture time: less than 100 ns.

c) Sampling rate: 48 000 conversions per second.

1.1.4 Data Channel Sampling Rate

48 000 conversions/second for 16 kHz channels
24 000 conversions/second for 8 kHz channels
12 000 conversions/second for 4 kHz channels

1.1.5 Floating-Point Conversion

The 15-bit data-words issued by the A/D converters are converted to 12-bit floating-point words that incorporate the binary-coded gain of the corresponding input amplifier.

1.1.6 Recording Dynamic Range

128 dB total recording range
80 dB min. for each gain setting

Accuracy allowed by the floating-point format: Relative accuracy of between 0.8% and 1.6% constant within the upper 42 dB of the dynamic range.

1.1.7 Tape Recording

a) Tape Recorder:

Wide-band (IRIG Group II) instrumentation tape-recorder with 1.0 inch tape, 14-track record and reproduce heads and

standard record electronics for direct recording.

b) Tape speed:

30 in/s both in record and reproduce modes
(240 in/s in fast forward and rewind modes)

c) Recording format:

modified NRZ-Mark.

d) Recording density:

12.133 kilobits per inch per track.

e) Recording rate:

364 kilobits per second per track.

f) Total effective data recording rate:

2.880 megabits per second for ten tracks.
(excluding parity words and synchronization words).

g) Error rate:

about 1×10^{-7} bits.

h) Continuous recording time:

one hour with a 9200 foot reel of tape.

i) Track organization:

each A/D converter feeds one track-pair so that ten tracks are used for data recording.

j) Error detection:

horizontal and vertical parity-words are recorded in order to allow error detection and location. Vertical parity words are recorded on Track 11.

k) Event location:

a sequence of binary coded decimal (BCD) numbers is recorded on Track 12 for event location and data transfer control. A new number is issued at each millisecond. Range: from zero to 7 999 999.

1.1.8 System Output

Information-carrying words and both horizontal and vertical parity words are available at the outputs of eleven shift-registers, whence they can be parallel-transferred to a digital computer or to a D/A converter. The event-location BCD numbers are available at the outputs of a 27-bit shift register and are also displayed on a set of nixie tubes.

1.2 General Description of the Record Section

A simplified block-diagram of the record section is shown in Fig. 1. The input analogue signals are amplified by variable-gain amplifiers (VGA) that are manually set according to the expected input levels. Gains can be varied in 6 dB steps; no continuous gain adjustment is provided. Each VGA sends a binary-coded gain value to the following blocks. The amplified signals are band-limited by special low-pass filters (LPF) that reduce to pre-determined limits the folding effect due to the sampling process taking place in the A/D converters. The above analogue devices are described in detail in Refs. 1 and 2. The outputs of the filters are sent to five A/D converters with input multiplexer and sample-and-hold units. Each multiplexer can handle up to four analogue inputs.

The A/D converters are clock-driven at a constant sampling rate of 48 000 conversions per second, each sample being defined by 15 binary bits, including the sign.

The multiplexers allow the choice of one to four input analogue channels to each A/D converter, according to the needs of the

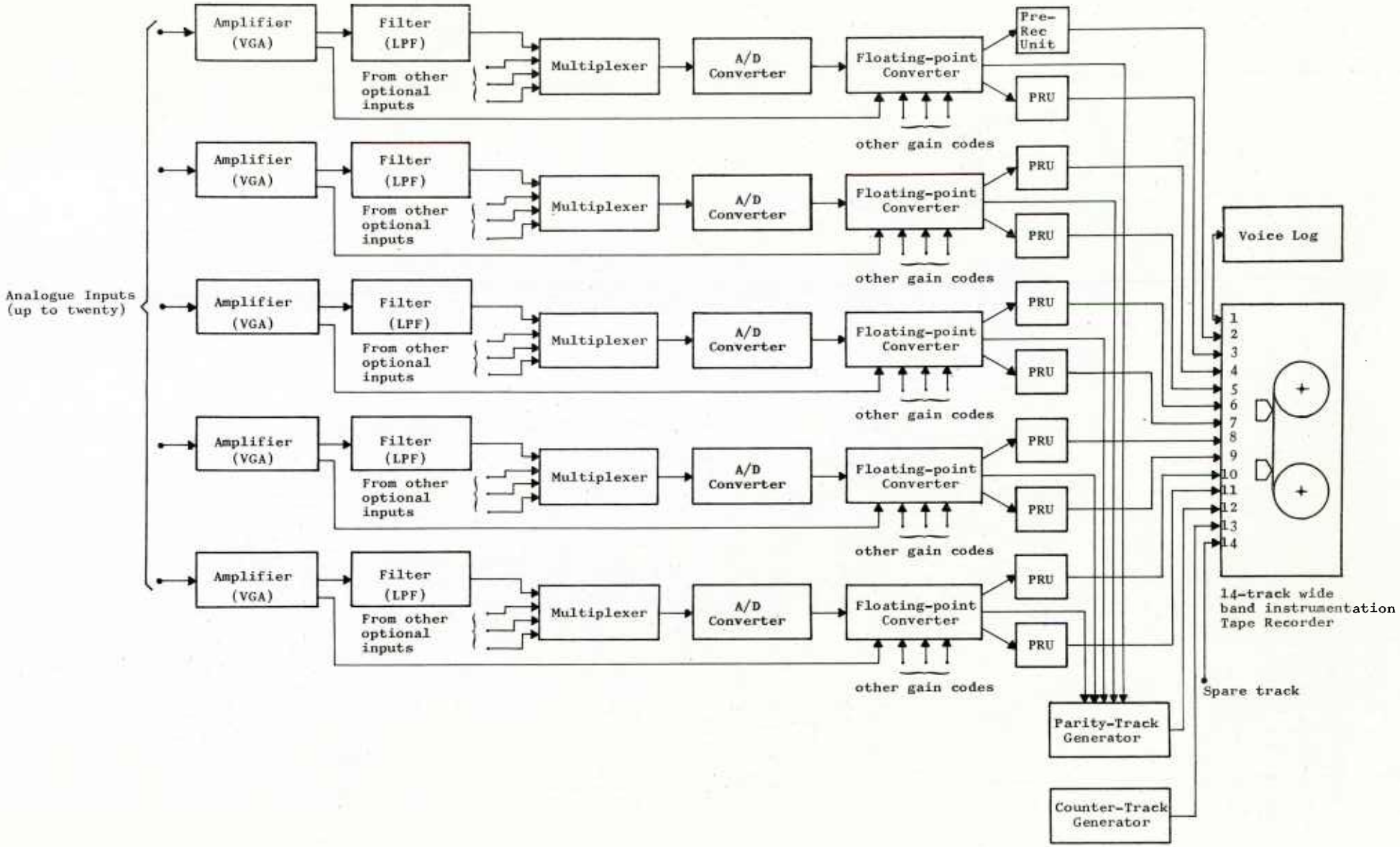


FIG. 1 DIGITAL RECORDING SYSTEM : RECORD SECTION

particular experiment. Thus the sampling rate of a given analogue channel depends on the configuration at the corresponding multiplexer and is 48 000, 24 000, or 12 000 samples per second.

Hence the whole system allows the recording of:

either 1 to 5 signals, each one represented by 48 000 samples/second,

or 1 to 10 signals, each one represented by 24 000 samples/second,

or 1 to 20 signals, each one represented by 12 000 samples/second,

or a combination, such as:
1 signal sampled at 48 000 samples/second
plus 4 signals sampled at 24 000 samples/second
plus 8 signals sampled at 12 000 samples/second.

The allowed useful bandwidth for each input channel will of course depend on the corresponding low-pass filter (LPF) and on the corresponding sampling frequency.

The allowed input bandwidth is:

16 kHz for a sampling frequency of 48 000 samples/second
8 kHz for a sampling frequency of 24 000 samples/second
4 kHz for a sampling frequency of 12 000 samples/second

The appropriate filters have to be inserted according to the chosen configuration. The 15-bit words issued by the A/D converters are sent to the floating-point converters (FPC) where they are processed together with the gain codes coming from the input VGA's to produce 12-bit words giving a pseudo-logarithmic representation of the samples.

The 12-bit words produced by each FPC are shared between two tracks of the tape recorder. For this reason the words are alternately

sent to two pre-recording units (PRU) each of which feeds one tape-track. In the PRU, parity words and synchronization words are added to the information-carrying words and a transformation of the sequences of "ones" and "zeros" to a suitable recording format is made. The adopted format is a modification of NRZ-Mark. Thus ten tracks (Tracks 2 to 11) are used for the five A/D converters. Track 12 is fed by a parity track generator (PTG) that receives the full outputs of the five FPC's and generates a sequence of vertical-parity words that serve for error detection, location, and eventual correction.

Finally, a counter-track generator (CTG) issues a sequence of BCD numbers that are recorded on Track 13 and label each millisecond of recording time. Track 1 is used for the recording operator's comments.

A standard 14-track wide-band instrumentation tape recorder working in direct-recording mode is employed. The bit-packing density is 12.133 kilobits/inch on each of Tracks 2 to 12. A lower density is used for the counter track. The tape runs at a speed of 30 in/s, so that a recording time of one hour can be obtained by using 9200 ft of tape.

1.3 General Description of the Reproduce Section

The block diagram of the reproduce section of the system is shown in Fig. 2. The tape is read again at a speed of 30 in/s. The signal recovered from each track is first processed by a bit-restorer (BR). This unit compensates phase and amplitude distortions introduced by the recording and reading processes and discriminates the recorded "ones" against the background noise and the signal drop-out due to tape imperfections. One BR is used for each of the twelve useful tracks (including parity track and counter track). The restored signals need further processing to become usable.

First of all, the timing of the bit sequence read from each track is not constant, owing to tape-speed fluctuations both in the

recording and reading phases. The timing is also different from track to track, owing to tape angular movements (skew). For these reasons each track is processed by a bit synchronizer (BS) that compensates for tape-speed fluctuation by generating a clock-signal that exactly follows the fluctuations themselves. This is followed by a word synchronizer (WS) that discriminates the information-carrying words and the parity words against the synchronization words. Information-carrying words and parity words are thus transferred to the output registers (OR) where they are available for transfer to a digital computer or simply to a D/A converter followed by a display unit. The vertical parity track is processed in an identical way, while the counting track undergoes a somewhat different processing. This will be described later in more detail.

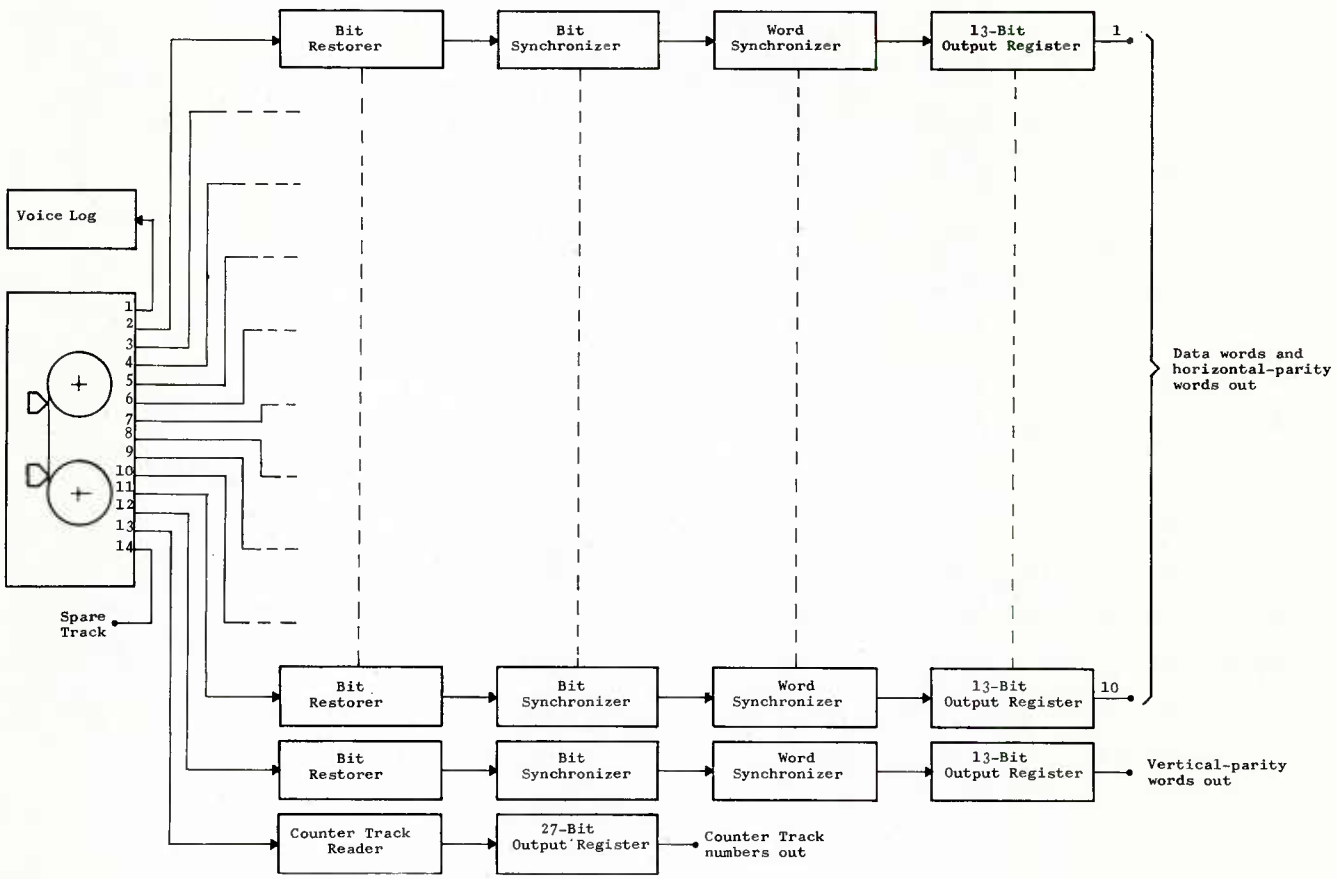


FIG. 2 DIGITAL RECORDING SYSTEM : REPRODUCE SECTION

2. SIGNAL PROCESSING BEFORE RECORDING

2.1 Input Filtering and Analogue-to-Digital Conversion

The range of measurements currently carried out in underwater acoustic investigations covers a dynamic range that can exceed 120 dB. Even for a single experiment the required dynamic range is often larger than 60 dB. Another point that leads to the requirement for a high dynamic range is the need to avoid critical gain adjustments of the receiving chain in order to reduce data losses due to saturations or to exceedingly low signal-to-noise ratios. These arguments led to the requirement for the highest available resolution for the analogue-to-digital conversion process. Accordingly it was decided to use 15-bit A/D converters.

A very elegant and trouble-free solution would have been achieved by means of a single A/D converter with such a speed as to be able to handle all the information to be recorded. A 15-bit multiplexer and A/D converter combination capable of at least 250 000 conversions per second for up to twenty input analogue channels would thus have been required. However, at the time this project was started, the fastest 15-bit A/D converters available allowed a sampling rate of about 50 000 conversions per second. Consequently we could not adopt the single-converter approach and were forced to use five A/D converters, one for each full-bandwidth input channel. Each of these converters is operated at a sampling rate of 48 000 conversions per second and includes a sample-and-hold unit and a multiplexer for up to four input channels. The general specifications for the input low-pass filters to be inserted before the A/D converters were established by combining the above speed rating with the requirement for a relative measurement error of about 1%. In fact a relative error of about 1% can be allowed for most underwater acoustic investigations.

Therefore the useful input frequency-band now depended on the amount of frequency folding allowed by the input low-pass filter. A special design of these filters finally allowed a useful bandwidth from a few hertz up to one third the sampling frequency f_s, i.e. at a frequency of $1/3\ f_s$ the amplitude of the folded spectrum due to the sampling process reaches a value of less than 1% of the amplitude of the input spectrum at the same frequency.

Of course the multiplexers allow the selection of one, two, or four analogue channels to be fed into each A/D converter, each time with a corresponding halving of the useful bandwidth for each input.

2.2 Floating Point Conversion

Because a constant relative error and a high dynamic range were required, the use of a floating-point converter was considered as a convenient means of reducing the number of bits required for each sample to a minimum.

For example, a logarithmic A/D converter, in which the output digital numbers would be proportional to the logarithm of the sample amplitudes, would allow a 200 dB dynamic range to be covered by 0.1 dB steps with 12-bit words. This solution, however, would be technically difficult to achieve and would require a computer or a hardware unit to extract the antilog of all the sample values before performing any linear operation.

Consider also that we had to record not only the A/D converter output data words but also the digital values of the gains of the input amplifiers. Thus it appeared more convenient to use a floating-point representation that combines the advantages of both the linear and the logarithmic representations. For this purpose each sample value is coded by means of a 12-bit word having the following structure:

a) The first bit (MSB + 1 position) gives the sign of the sample.

b) The four following bits define in binary form the exponent of a power of two that represents the "scale" of the sample.

c) The last seven bits give the value of the sample, to be multiplied by the above scale factor when reconverting to the linear representation.

This is equivalent to expressing each sample value in the form:

$$S = \pm a\, 2^{b}$$

where "a" is given by seven bits and "b" by four bits.

Now consider how the words "a" and "b" are determined in the floating point converter. The FPC receives both the 15-bit binary word coming from the A/D converter and the 4-bit word coming from the input amplifier (VGA) and representing its gain as a certain number of 6 dB steps. The basic operation performed by the FPC consists of a sequence of shifts of the 15-bit word towards the MSB position while at the same time leaving the sign bit unaltered. The shift operation is stopped as soon as the first "one" has reached the MSB position or as soon as a maximum of seven shifts have been totalled.

Note that each shift is equivalent to doubling the value of the sample. The word "a" is given by the first seven bits, starting from the MSB. The word "b" gives in binary form the value of the expression:

$$15 - g - n$$

where "n" is the above defined number of shifts and "g" is the gain of the input amplifier expressed as a number of 6 dB steps. We note that "b" can reach a maximum value of 15 and that "g" is allowed to reach a maximum value of 8 (48 dB gain). Since "b" is not allowed to become negative, the maximum value of "n" must be limited to 7, as we have already pointed out. The operating

principle of the FPC is further illustrated in Fig. 3. As a conclusion, for each value of "g", i.e. for each gain setting, "b" can assume eight different values, thus providing a 42 dB dynamic range that can be added to the 42 dB given by "a" and to the 6 dB given by the sign bit. Hence we have a total dynamic range of 90 dB for each gain setting. It is, however, important to note that nine different gain settings (from 0 dB to 48 dB) are possible: since the gain setting is also recorded through "b", we can say that the recording system allows a dynamic range of 138 dB when we refer to the VGA's input. In practice A/D Converter noise limits the above figures to about 80 dB and 128 dB, respectively.

The block-diagram of the FPC is shown in Fig. 4. Note that an overflow indicator has been included to allow the best adjustment of the VGA's gains.

2.3 Word Organization on the Tape

48 kilowords/second are produced by each A/D converter: this corresponds, after the floating point conversion, to a bit-rate of $48 \times 10^3 \times 12 = 576$ kilobits/second for each full channel. If we now include a necessary 20% increase in this rate in order to introduce parity words and synchronization words, we reach a rate of about 700 kilobits/second. The bit-recording density we have achieved on tape with an acceptably low error-rate is about 12 kilobits/inch for each track. The recording of the above bit-rate on a single track would thus require a tape speed of 60 in/s. Since a 14-track tape recorder was available, we decided to double the recording time by splitting the information coming from each A/D converter between two tracks. This has allowed a recording speed of 30 in/s, thus giving recording times of up to one hour with a single reel of tape and better utilizing the available storage.

The organization of the words on each pair of tracks is shown in Fig. 5. One can notice that two successive words from the FPC are not always written on two different tracks: a somewhat more complex pattern has been adopted in order to allow the insertion, at each half millsecond, of a parity word or of a synchronization

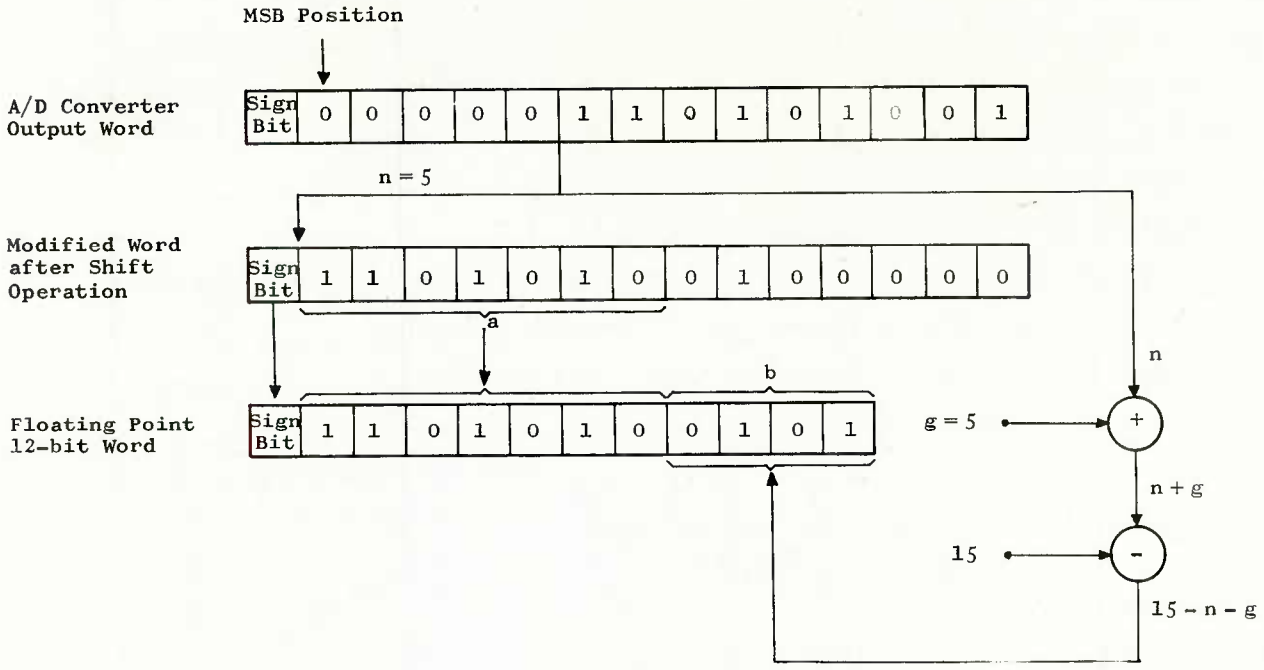


FIG. 3 EXAMPLE OF FLOATING-POINT CONVERSION (GAIN: 30 dB)

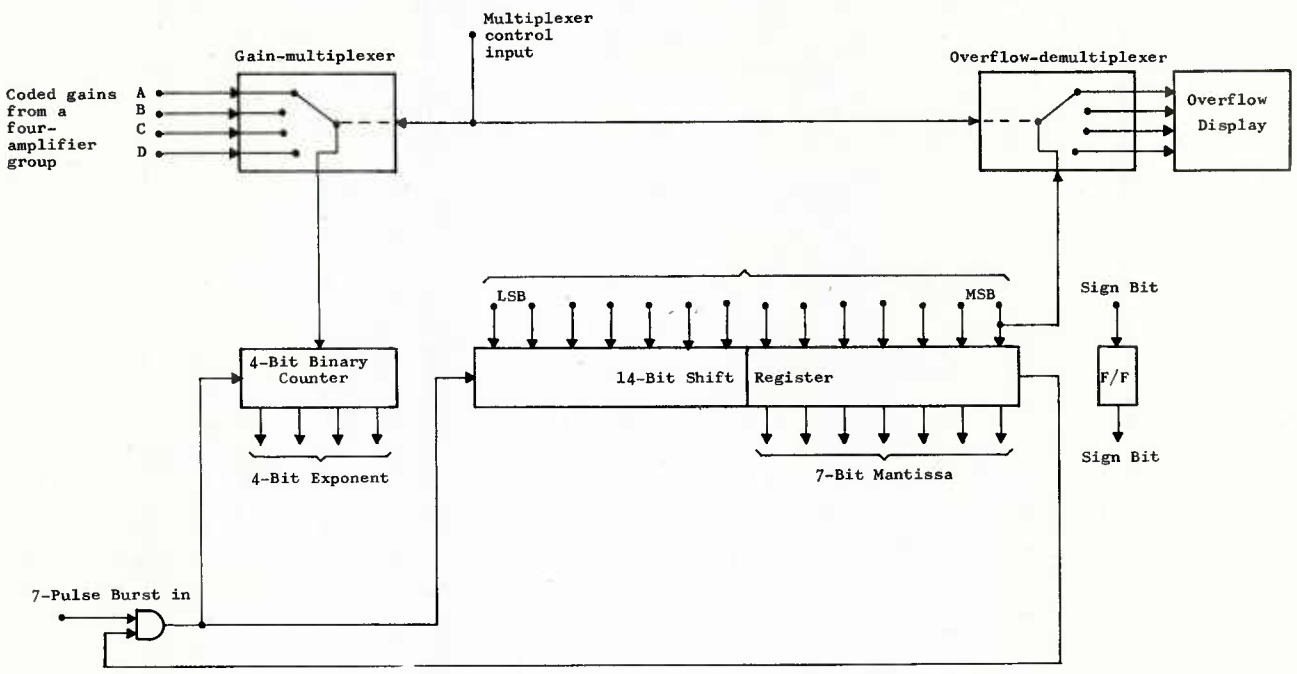
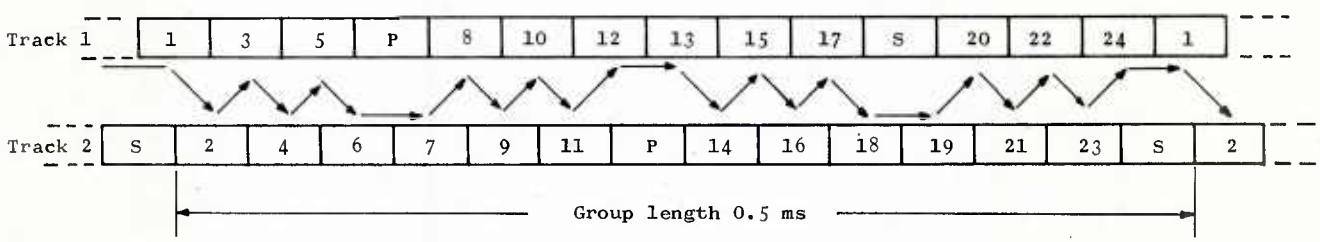


FIG. 4 FLOATING-POINT CONVERTER

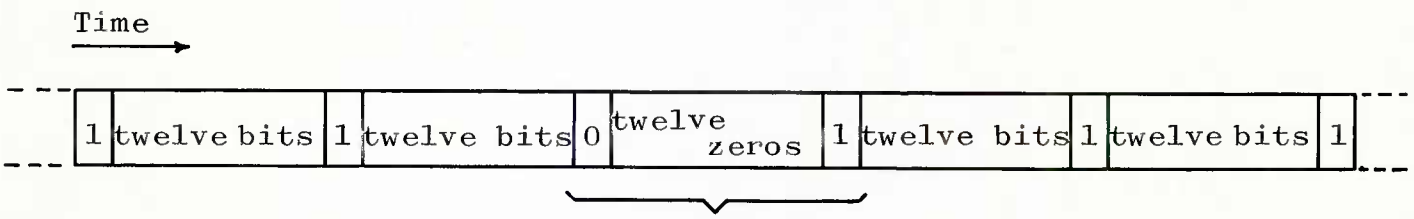


Track-pairs 3-4, 5-6, 7-8, 9-10 have the same organization

FIG. 5 WORD ORGANIZATION ON A TRACK-PAIR

word. The parity word is composed of twelve bits where the n^{th} bit gives the parity of the n^{th} bits of the twelve preceding information-carrying words of the same track. The synchronization word is composed of twelve "zeros".

To be able to identify the synchronization words, a 13^{th} bit has been added to each word. In particular, a fixed "one" is added at the beginning of each information-carrying word and of each parity word, while an additional "zero" is added at the beginning of each synchronization word. Therefore a synchronization word is unambiguously identified by a sequence of thirteen "zeros" followed by a "one". This is further illustrated in Fig. 6.



thirteen "zeros" followed by a "one" identify a synchronization word

FIG. 6 SYNCHRONIZATION WORD IDENTIFICATION

All of the above processing is executed in the pre-recording units (PRU) shown in Fig. 1. As explained in Sect. 1.1.7, ten tracks are used for recording the data issued by the five A/D converters and Track 11 is used for recording a "vertical-parity" track that is built up in the parity-track generator (PTG) of Fig. 1. This track has the same organization as the preceding ones, the only difference being that its "information-carrying" words are obtained by making the parity (bit per bit) of the ten words recorded at the same time on the other tracks.

We have thus established on the tape a sort of orthogonal system of parities that can be used for error location and correction. The whole parity system is schematically shown in Fig. 7.

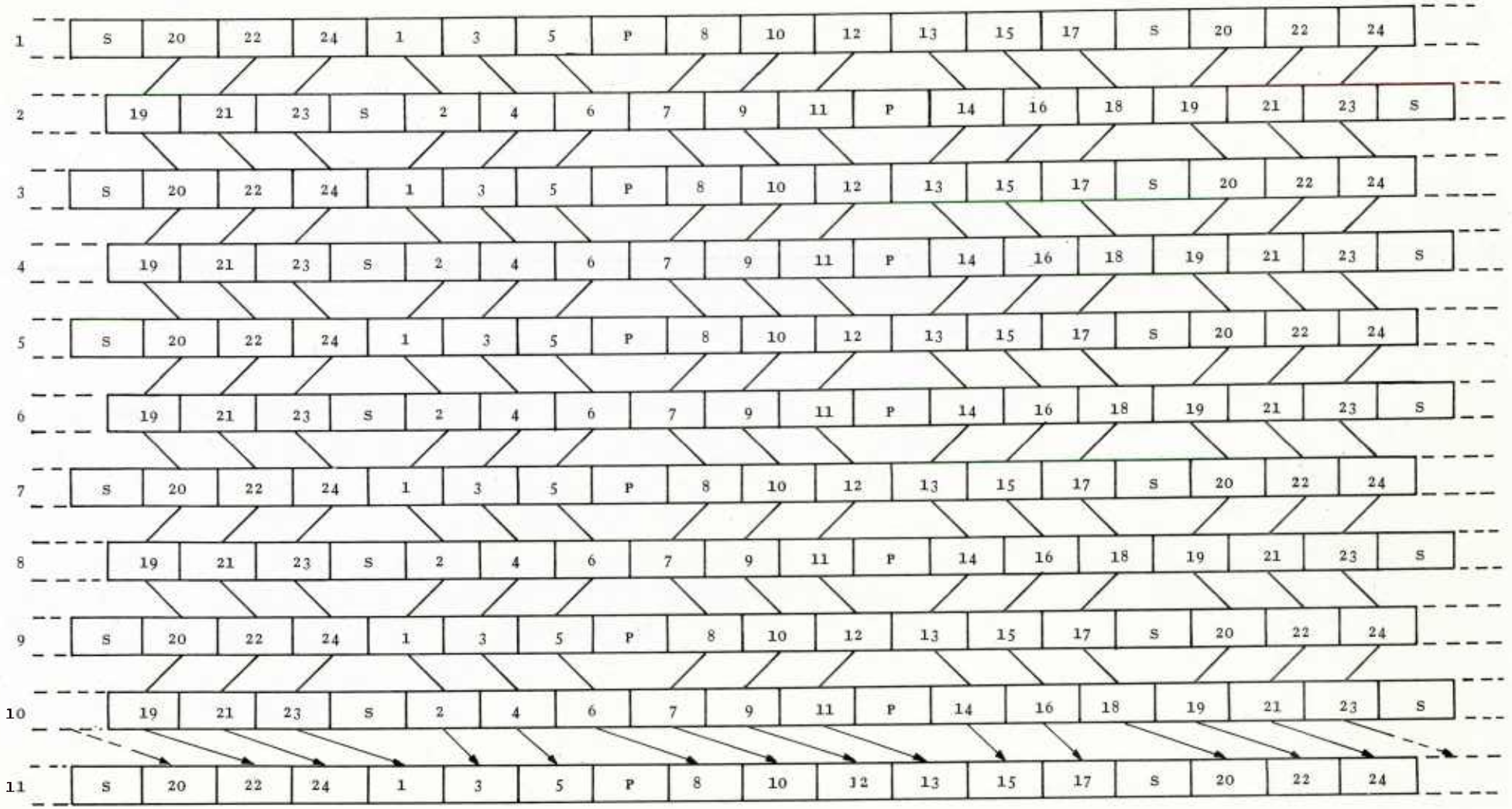


FIG. 7 WORD ORGANIZATION ON THE TAPE SHOWING THE CONSTRUCTION OF 'VERTICAL–PARITY' TRACK

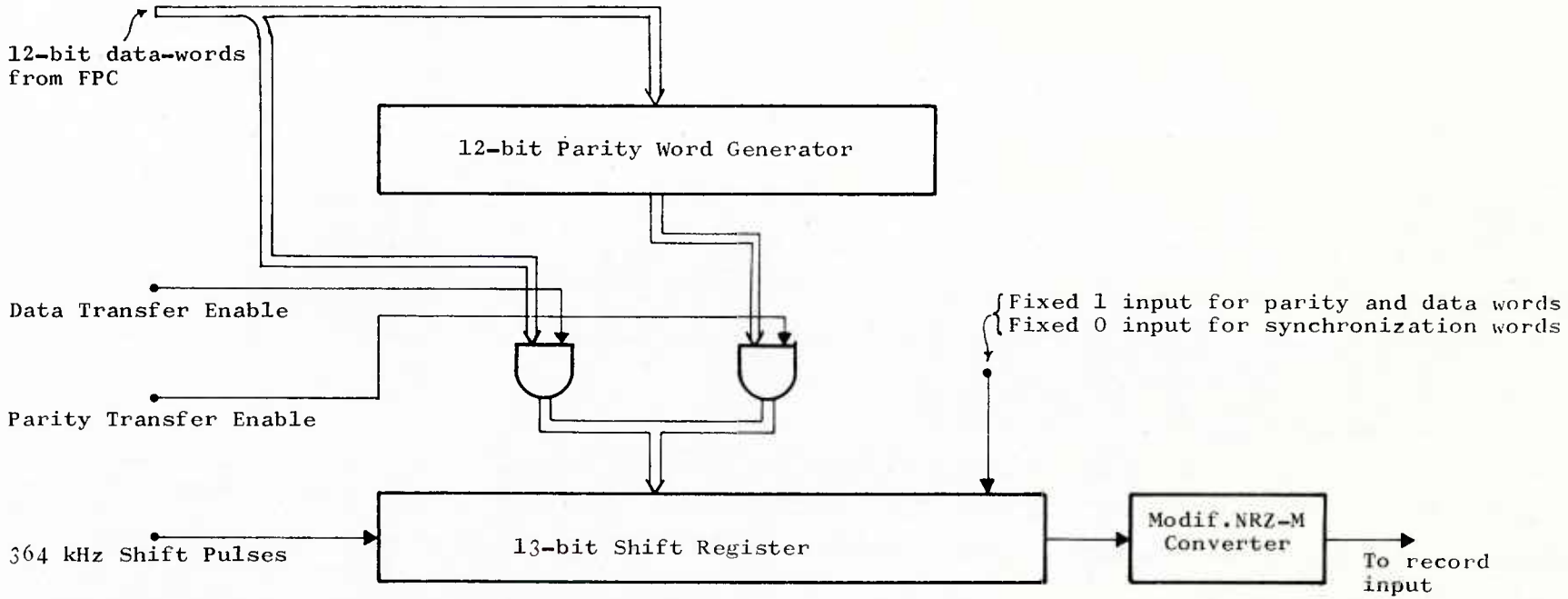


FIG. 8 SIMPLIFIED BLOCK DIAGRAM OF PRE-RECORDING UNIT

The block-diagram of the pre-recording unit (PRU) is shown in Fig. 8.

2.4 High-Density Recording

2.4.1 Choice of the Tape Recorder

The information-recording rates of digital tape recorders available on the market fall far short of our requirements for the five-channel system. Considering for example a 9-track digital tape-recorder working at a speed of 75 in/s and at a density of 800 bits/inch and storing one 13-bit word from the pre-recording unit by means of two 8-bit characters, we reach a word recording rate of 30 kilowords/second, which is not sufficient for recording a single full channel from our data sources. Although it may seem strange, it is possible to record a much higher bit density on an analogue instrumentation tape-recorder than on a digital one. This is mainly due to the following reasons:

a) Non-saturated linear recording can be used in the instrumentation machine by means of high frequency bias (ac bias): this minimizes non-linearities and extends the resolution available for given write and read head gaps. The non-saturated recording also minimizes the crosstalk between adjacent tracks.

b) The tape-transport system of an instrumentation tape-recorder is much more refined and precise than that of a digital recorder, thus minimizing tape-speed fluctuations and tape angular movements (skew). The stability of the tape-speed is extremely important in that it greatly facilitates the generation of a synchronizing clock from the recorded data. The difficulties involved in the use of an instrumentation machine must also be mentioned:

1) The tape transport is rather delicate and needs continuous maintenance.

2) Especially for a wide-band machine, the write and read heads wear rapidly, causing continuous change of frequency

response and thereby necessitating frequent adjustments in the record and reproduce electronics.

3) The reproduce electronics are much more sophisticated than those of a low-density digital recorder.

4) No incremental recording is possible.

2.4.2 Density Limitations

For non-saturated digital recording the capacity limitation of one track can be expressed by replacing cycles per second (hertz) with cycles per inch in the well-known Shannon-Hartley equation:

$$C = BW \lg_2 (1 + S/N)$$

where C = capacity in bits per linear inch
BW = bandwidth in cycles per linear inch
S/N = rms signal-to-noise power ratio

In our case, the wide-band instrumentation tape-recorder employed allows a frequency band of from 400 Hz up to 500 kHz in direct recording mode with an S/N ratio of 20 dB at a tape speed of 30 in/s. This corresponds to a bandwidth (BW) of about 16 kilocyles per linear inch and to a theoretical capacity C of about 50 kilobits per linear inch. In practice many factors limit the above capacity. These depend both on the nature of the magnetic recording process itself and on the adopted coding method.

Capacity losses are caused by imperfect equalization and lack of dc response of the reading process. Further on, the noise distribution is not Gaussian as implicitly assumed in the Shannon equation. The departure from the Gaussian distribution is normally due to "dropouts", i.e. temporary losses of the read signal strength, caused by transient increases in head-to-tape spacing.

The noise energy in dropouts is small, because they are relatively infrequent, but a dropout can be expected to reduce the instantaneous S/N ratio by as much as 10 dB to 15 dB. For this reason we think

that our 12 kilobit/inch density with a mean error rate of less than 1 error out of 10^7 bits represents a good approach to the Shannon limit.

2.4.3 Coding Method

We can now state the bit-rate and density requirements for each track of the tape recorder. In each second, 48 kilowords are produced for each full channel. Each word is defined by 13 bits. A parity word or a synchronization word are alternately added for each group of six information-carrying words, so that each full channel gives us a total rate of 56 kilowords/second and a corresponding bit-rate of 728 kilobits/second. By splitting each full channel on two tracks, we reach a bit-rate of 364 kilobits/second per track. Finally, by using a tape speed of 30 in/s we have a recording density of 12.133 kilobits/inch on each track. The above values are valid for each information-carrying track and for the parity track; a lower density is required for the counting track.

A modified form of NRZ encoding has been employed for the recording process. Two different methods of NRZ encoding are commonly used in digital recording. These are schematically shown in Fig. 9 as

a) NRZ-C or "non-return to zero change" and

b) NRZ-M or "non-return to zero mark".

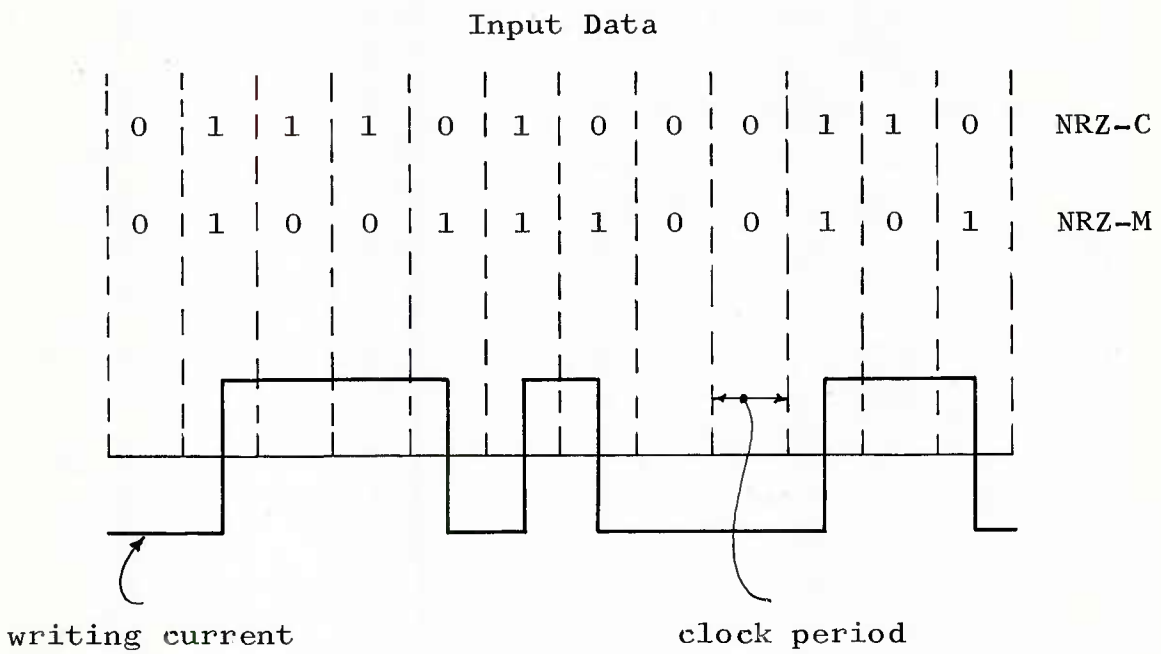
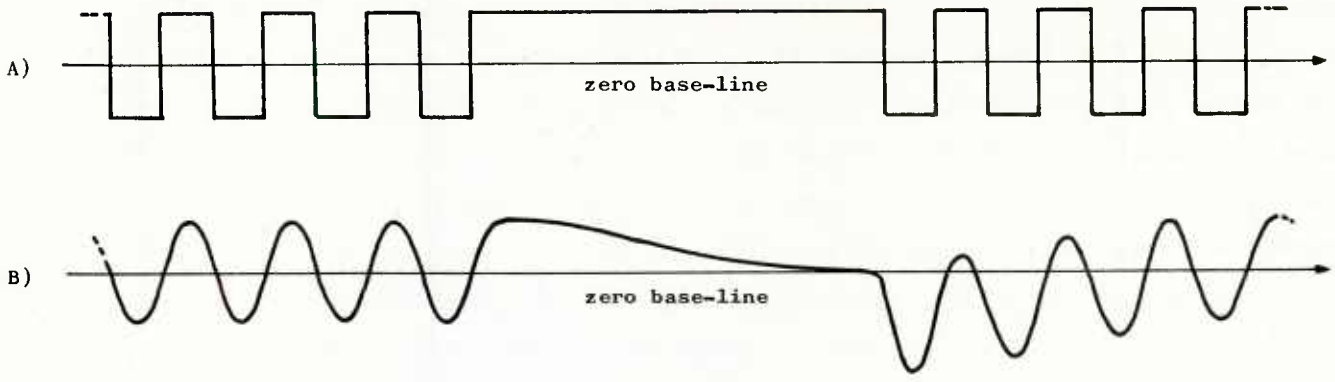


FIG. 9 NRZ ENCODING FORMATS

In the NRZ-C method, the direction of the writing current is reversed for every change in the binary sequence to be recorded, so that one direction of surface magnetization corresponds to a "one", while the opposite direction corresponds to a "zero". In the NRZ-M method, the current is reversed every time a "one" is to be recorded. With this method, if a bit is misread only that bit is in error, while in the NRZ-C method, if a bit is in error, all succeeding bits will be erroneously read until the next current reversal is encountered. Another advantage of the NRZ-M method lies in the fact that the polarity of the signal is not significant in defining the readback sequence. For both the above reasons we based our coding format on the NRZ-M method.

It must be mentioned that the NRZ encoding provides no redundancy in the waveform of the recorded signal; the density of the magnetization reversals is just equal to the recorded bit density. Thus NRZ encoding provides a minimization of the recording density for a given bit-rate at the expense of a complete lack of redundancy. For this reason parity words and a vertical-parity track are normally used with NRZ, as in our case.

At this point we must enter into some detail about the reading process. The operation of the magnetic reading head is based on the rate of change of flux, so that the head response is ideally given by a straight line with 6 dB/octave positive slope. In other words, the reading process ideally corresponds to a differentiation of the recorded signal. This accounts for the lack of dc and low frequencies in the reproduced signal. In practice the response of the reading head does not rise continuously at 6 dB/octave but in the upper half of the reproduce band it first flattens out and then drops to "zero" at the wavelength of the head's gaps. For the above reasons we have a return to the signal base-line after a given time period and an apparent dc offset with non-symmetrical digital data, which is the case with standard NRZ encoding. A typical example of base-line shift is illustrated in Fig. 10. It appears from this example that the base-line shift also limits the number of consecutive "zeros" that may be recorded by the NRZ-M method.



TRACE A - NRZ-coded recording signal
TRACE B - Corresponding output at the reading head

FIG. 10 AN EXAMPLE OF BASE-LINE SHIFT DUE TO NON-SYMMETRICAL ENCODING

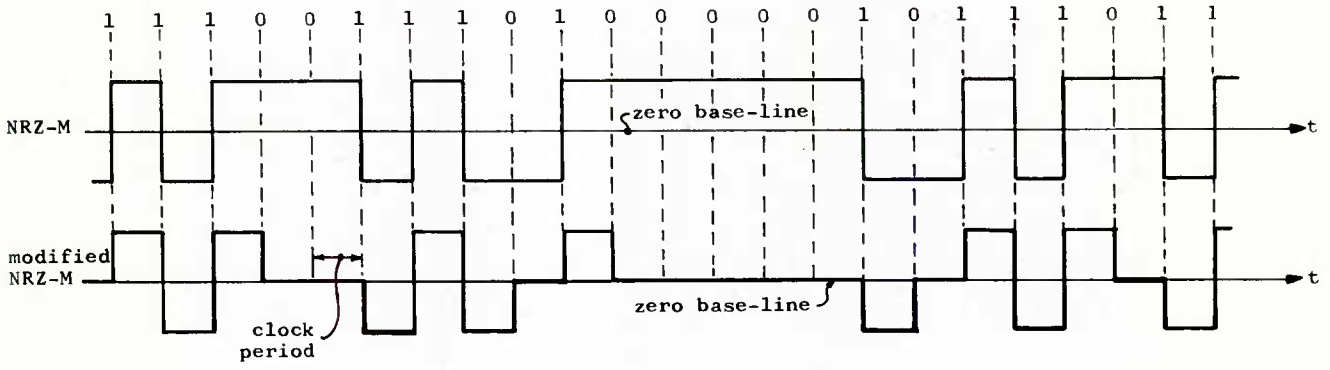


FIG. 11 EXAMPLE OF MODIFIED NRZ-M ENCODING FORMAT

To avoid such difficulties, we have adopted a modified coding format: this is shown in Fig. 11, where it is compared with an equivalent NRZ-M code. One can notice that the new code is a sort of "digital derivative" of the NRZ-M code. In fact it nearly eliminates the base-line shift problem by suppressing departures from the zero base-line that may last for more than one clock-period and by continuously alternating pulses of opposite polarities. One may object that the adoption of a three-level code causes a loss of 6 dB in the dynamic range of the recorded signal but we think that the suppression of the base-line shift is well worth this loss. It is important to note that the two codes of Fig. 11 become identical when representing a continuous series of "ones", so that there is no increase in the maximum density of magnetization reversals over that of the NRZ encoding.

3. SIGNAL PROCESSING IN THE REPRODUCE PHASE

3.1 The Equalization Problem

The signal recovered at the reading head output is affected by a considerable amount of phase and amplitude distortion. Phase distortion is caused by a 90° phase shift at the so-called "thickness loss breakpoint" and also by a recording point shift in the record gap field at the shorter wavelengths. Amplitude distortion is due to the unequalized system response at the reading head output. This is shown in Fig. 12 for a wide-band instrumentation tape recorder working at a speed of 30 in/s.

Amplitude and phase distortion are of course not important in themselves but only to the extent that they impair the detection of "ones" in the reproduced signal. For this reason we made no attempt to restore all the original shape of the recorded signal, but only tried to minimize the really unwanted effects, i.e. base-line shift, overshoot, and pulse-crowding effects.

Since we made use of a standard analogue tape recorder, we could have also used the standard direct-reproduce equalizers that are always available with such machines. These would have produced a flat amplitude vs frequency response but have also given a strong overshoot in the pulse response, due to the sharp cut-off of the amplitude response itself. Furthermore, no good phase equalization is normally allowed by standard direct-reproduce equalizers. For the above reasons we preferred to correct only the rising portion of the unequalized response, thus having to deal with a very simple phase equalizer and minimizing overshoot and noise contributions from the high frequency portion of the reproduced signal spectrum. The adopted equalization and the resultant amplitude response are

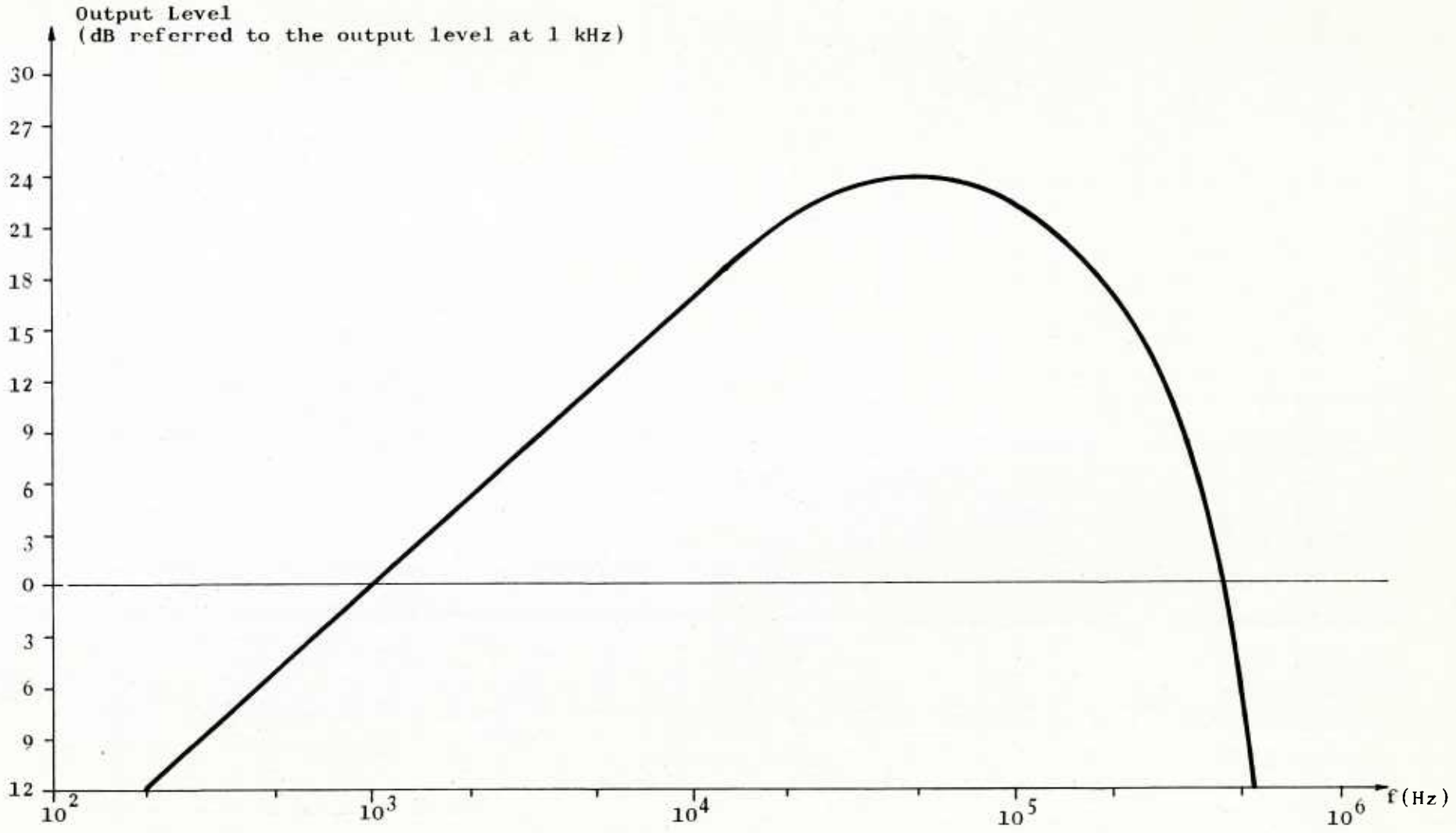


FIG. 12 UNEQUALIZED AMPLITUDE RESPONSE AT 30 in/s

shown in Fig. 13a; 13b shows a typical standard equalization. Figures 14a and 14b respectively show the amplitude and phase equalizers built by using high-speed operational amplifiers.

3.2 Detection and Positioning of "Ones"

After amplitude and phase equalization, the reproduced signal is as schematically represented in Fig. 15. It is still very similar to the recorded signal, except for a rounding of the pulses and a certain amount of pulse-crowding effect.

Since each "one" is represented by a pulse of either positive or negative polarity, the first following operation is a full-wave rectification, as shown in the second trace of Fig. 15.

The signal now takes two different paths: the first leads to a threshold detector that decides the eventual presence of a "one", the second leads to a differentiator followed by a clipper. The output of the clipper is gated by the threshold detector output, so that its transitions due to clipped noise are cut away. So we can say that the threshold detector is capable of finding the "ones" but cannot precisely position them because of the amplitude distortions due to the crowding effect. On the other hand the differentiator-clipper is capable of precisely locating the position of the pulse maxima (less influenced from the crowding effect) by means of the zero crosses of the signal derivative. Unfortunately it does the same job for the noise peaks contained in the reproduced signal. Hence the importance of the gating operation and of a correct threshold value, which must be high enough to avoid the noise peaks but also as low as possible compared to the signal drop-outs. A good compromise threshold value must be experimentally found, depending on the noise distribution in the reproduced signal and the particular brand of tape used. The output of the gating stage triggers a monostable multivibrator that provides fixed-length pulses and an additional noise immunity because of its intentional insensitivity to the very narrow clipped noise pulses that may cross the gate at the edges of the threshold signal. All of the

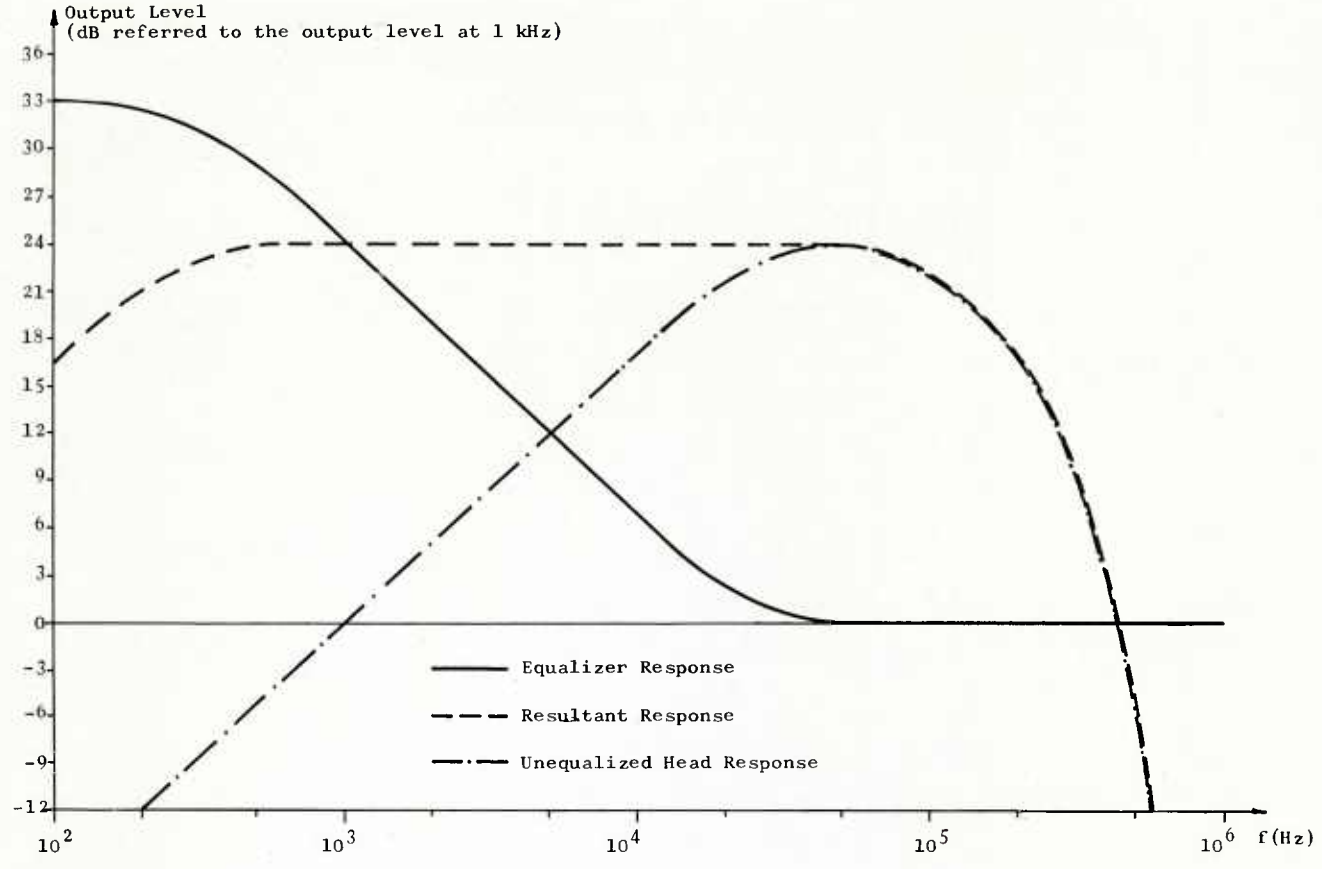


FIG. 13a ADOPTED EQUALIZATION

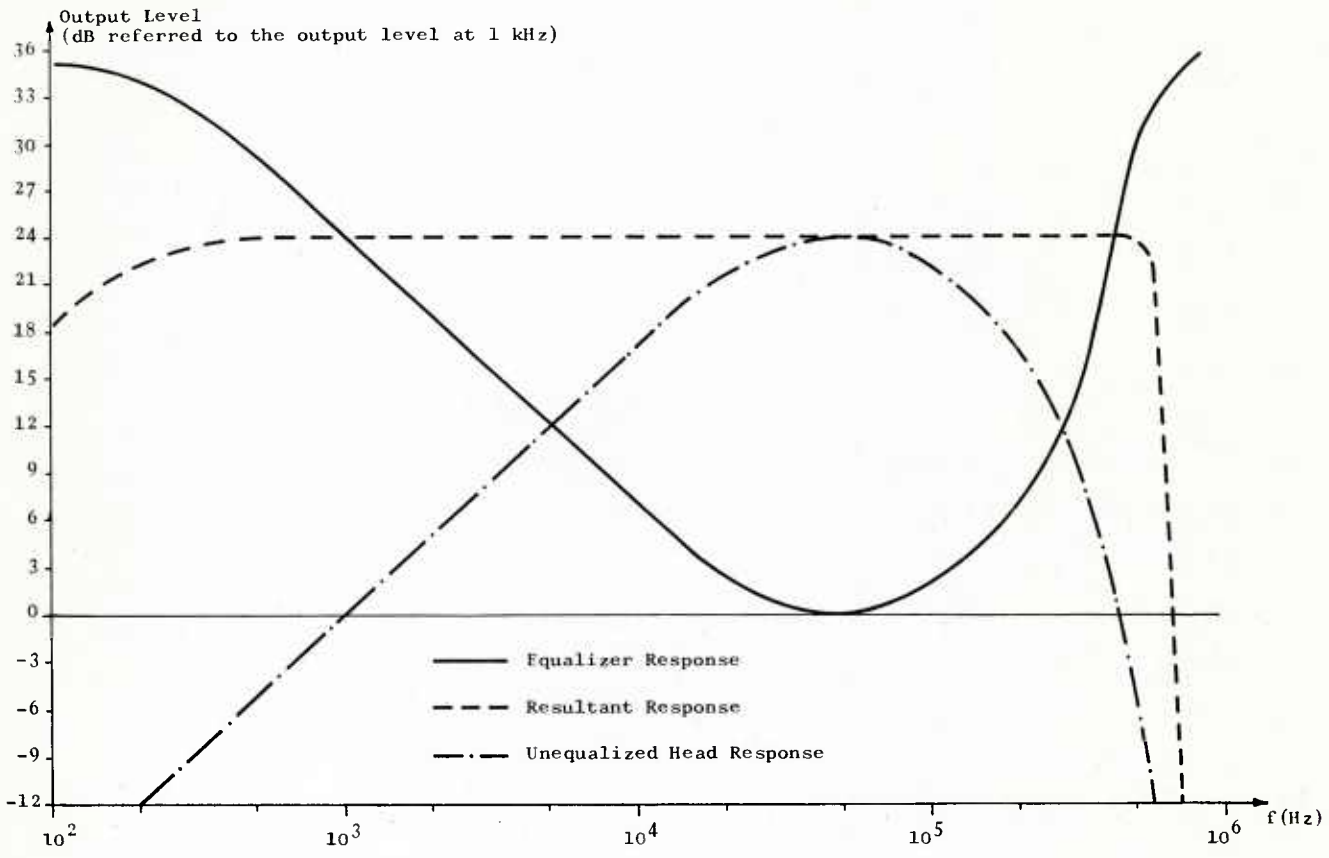
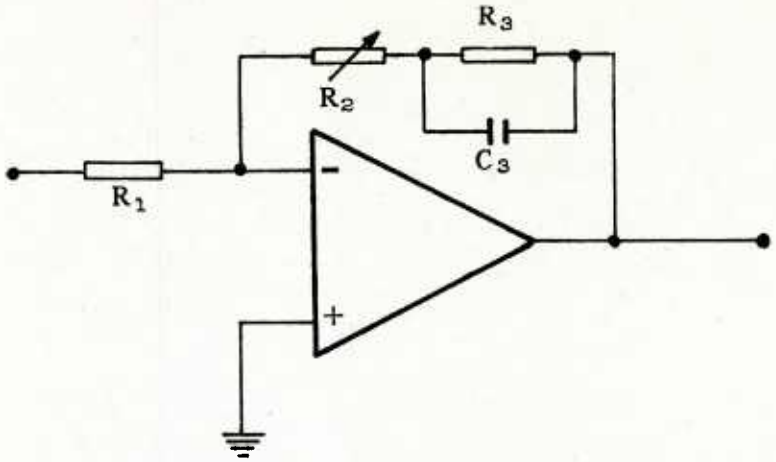


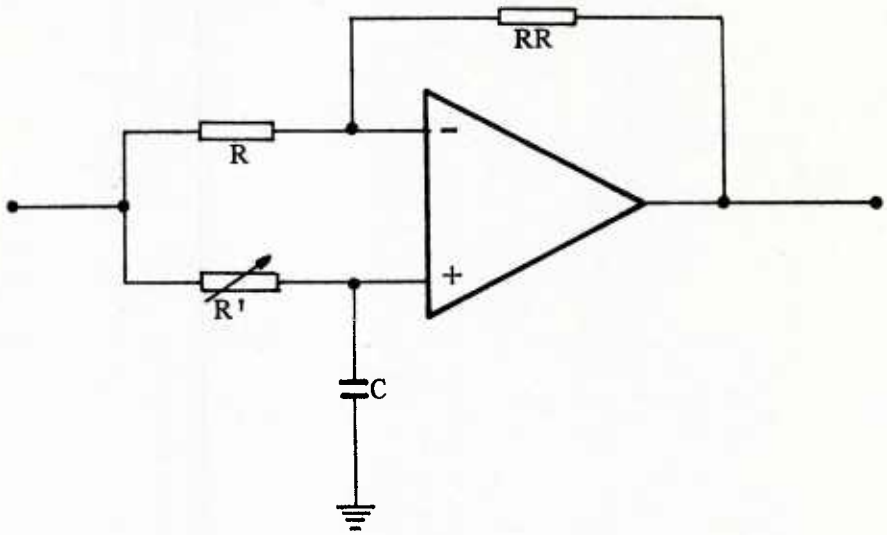
FIG. 13b TYPICAL STANDARD EQUALIZATION



$$G(s) = \frac{R_2}{R_1} + \frac{R_3}{R_1}\,\frac{1}{1+s\,\tau_3}$$

where $\tau_3 = R_3\,C_3$

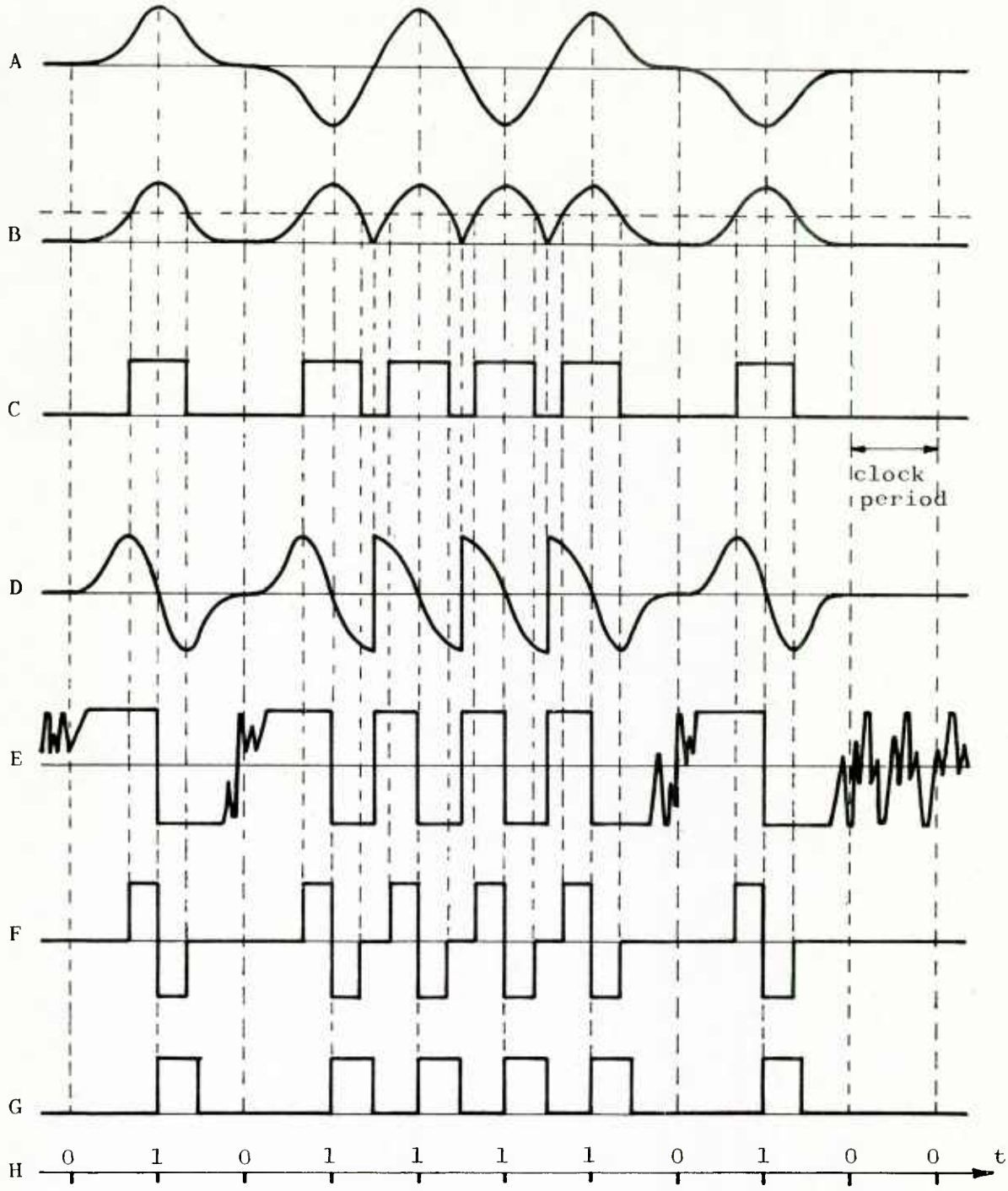
FIG. 14a AMPLITUDE EQUALIZER



$$G(s) = \frac{1 - s\,\tau'}{1 + s\,\tau'}$$

where $\tau' = R'C$

FIG. 14b PHASE EQUALIZER



TRACE A - Readback signal after equalization
TRACE B - Full-wave rectified readback signal
TRACE C - Threshold detector output
TRACE D - 1st derivative of full wave rectified signal
TRACE E - Clipper output
TRACE F - Gate output
TRACE G - Monostable multivibrator output
TRACE H - Recorded/Reproduced bit sequence

FIG. 15 BIT DETECTION AND POSITIONING

above processing is schematically shown in Fig. 15. The simplified block diagram of the bit-restorer is shown in Fig. 16.

3.3 Bit Synchronization

The recovered sequence of "ones" (trace G of Fig. 15, referred to hereafter as the "G-signal") is affected by a considerable amount of short-term and long-term rate fluctuation, due to the non-constant tape speed both in the recording and reading processes. Furthermore, the short-term fluctuation is also different from track to track, due to angular movements of the tape. To be able to interpret the recovered data words, it is necessary to build up a timing clock for each track that can be used for sampling the G-signal and for timing all of the following logics. A simplified block diagram of the timing-clock generator or bit-synchronizer (BS) is shown in Fig. 17.

A crystal-controlled oscillator supplies pulses at a 4.368 MHz repetition rate to a divider-by-twelve whose output, in absence of any rate fluctuation, provides the required 364 kHz timing frequency. This frequency can be varied by means of the adder/subtractor interposed between the crystal oscillator and the divider in such a way as to precisely follow the rate fluctuations. For such a purpose, pulses are subtracted or additional pulses are inserted at the divider input, depending on the relative position of the pulses in the G-signal and of the rising fronts in the divider output. The divider output and the G-signal are fed into a phase comparator whose output provides a suitable control signal to the pulse adder/subtractor. More clearly, the rising front of a pulse in the G-signal can correspond either with a "zero" level or with a "one" level of the divider output. In the first case it is decided that the divider output has to be anticipated and an additional pulse is added at the divider input; in the second case it is decided that the divider output has to be delayed and a pulse is subtracted from the divider input. Consequently the position of the rising fronts in the divider output will nearly coincide with that of the "ones" and "zeros" in the G-signal. Of course there is no feedback on the

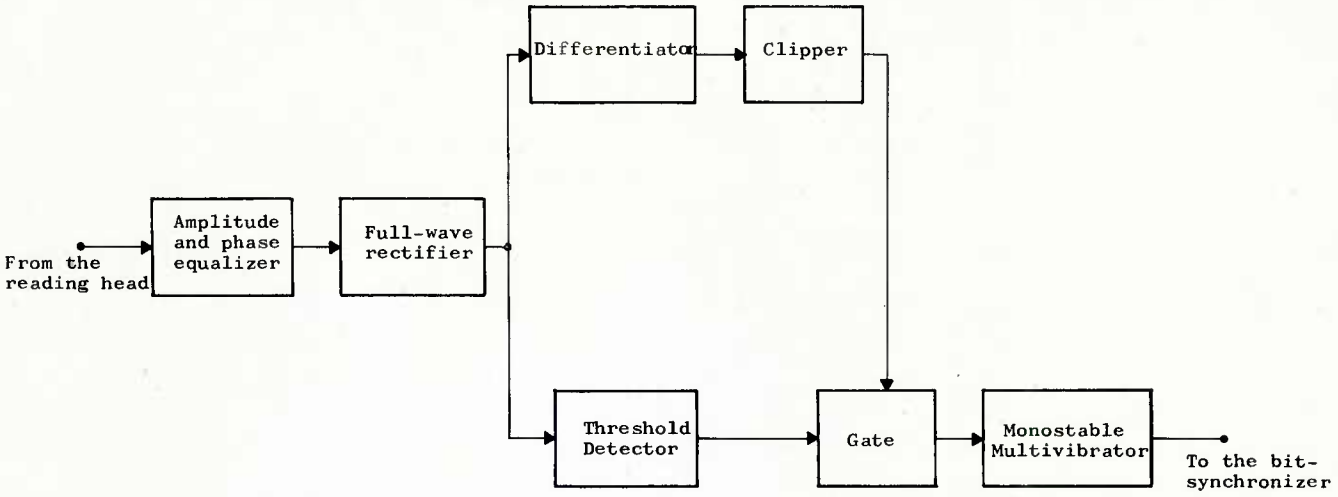


FIG. 16 SIMPLIFIED BLOCK DIAGRAM OF A SINGLE-TRACK BIT RESTORER

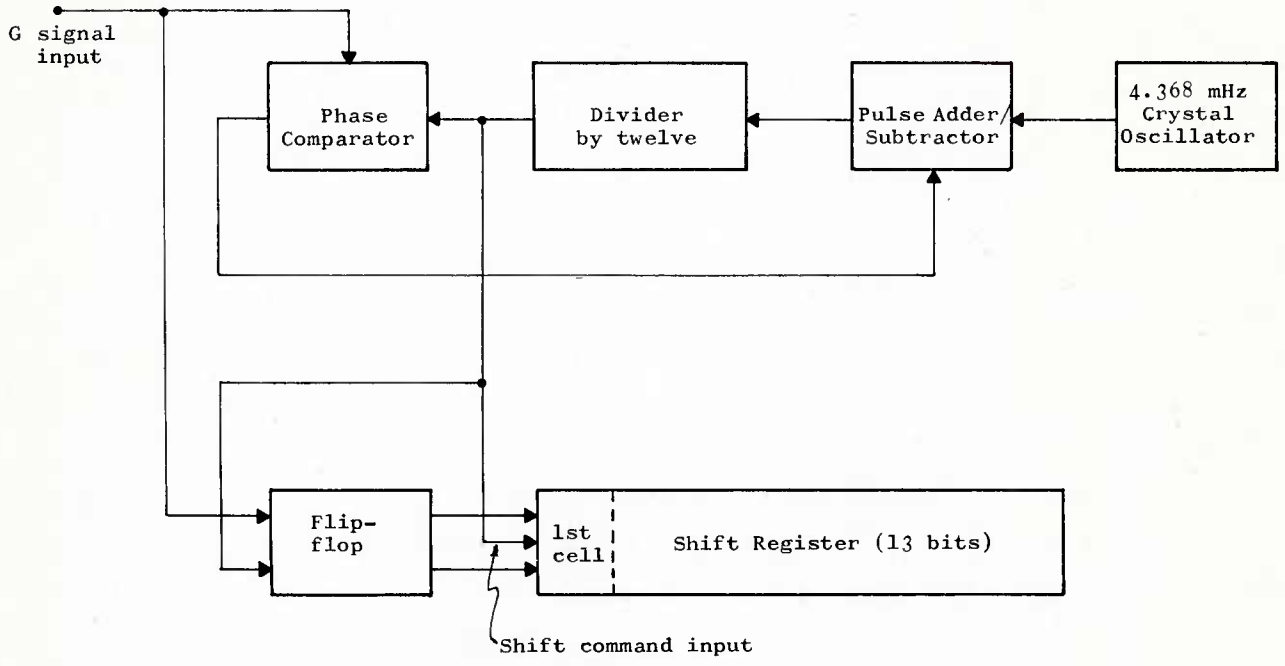


FIG. 17 SIMPLIFIED BLOCK DIAGRAM OF BIT SYNCHRONIZER

divider when a "zero" occurs; this would lead to a loss of synchronism for a long series of consecutive "zeros" if it were not for the fact that in our recording format the maximum number of consecutive "zeros" is restricted to thirteen.

The maximum rate at which pulses are added or subtracted at the divider input is one pulse in twelve supplied by the crystal oscillator, thus providing a maximum frequency deviation of about ±8% at the divider output. Owing to the presence of zeros, this maximum deviation is never statically attained; which is why it is purposely designed as much higher than the allowed rate fluctuation caused by tape-speed error and unstability. A big advantage of the adopted synchronization scheme lies in the fact that it is completely digital, stable, and self-locking.

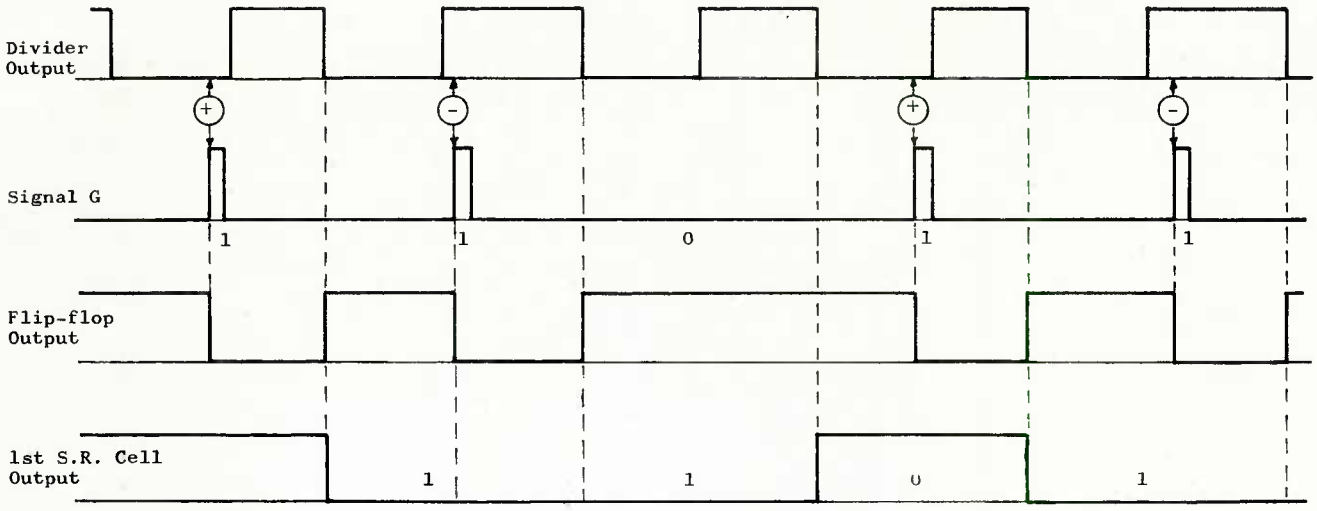
The G-signal and divider output are fed to a flip-flop set by the rising fronts of the G-pulses and reset by the descending fronts of the divider output. Flip-flop outputs feed a shift-register whose first cell successively contains the recorded sequence of "zeros" and "ones".

All of the above processing is illustrated in Fig. 18. The operation of the shift register will be explained in the next section.

3.4 Word Synchronization

The binary sequence recovered from each track of the tape recorder is fed to a shift register (already shown in Fig. 15) whose shift command is given by the output of the divider-by-twelve. Each binary sequence is also fed to a serial-parity checker that compares the bits in each group of twelve successive words with the following parity word.

Each time a twelve-bit data-word is present in the shift register, a timing circuit enables the parallel transfer of the word to an output register from which the word can be transferred to an external storage device or to a digital computer. The parallel-transfer



Rate fluctuations have been exaggerated for clarity: ⊕ indicates that one pulse is added at the divider input; ⊖ indicates that one pulse is subtracted from it.

FIG. 18 BIT SYNCHRONIZER OPERATION

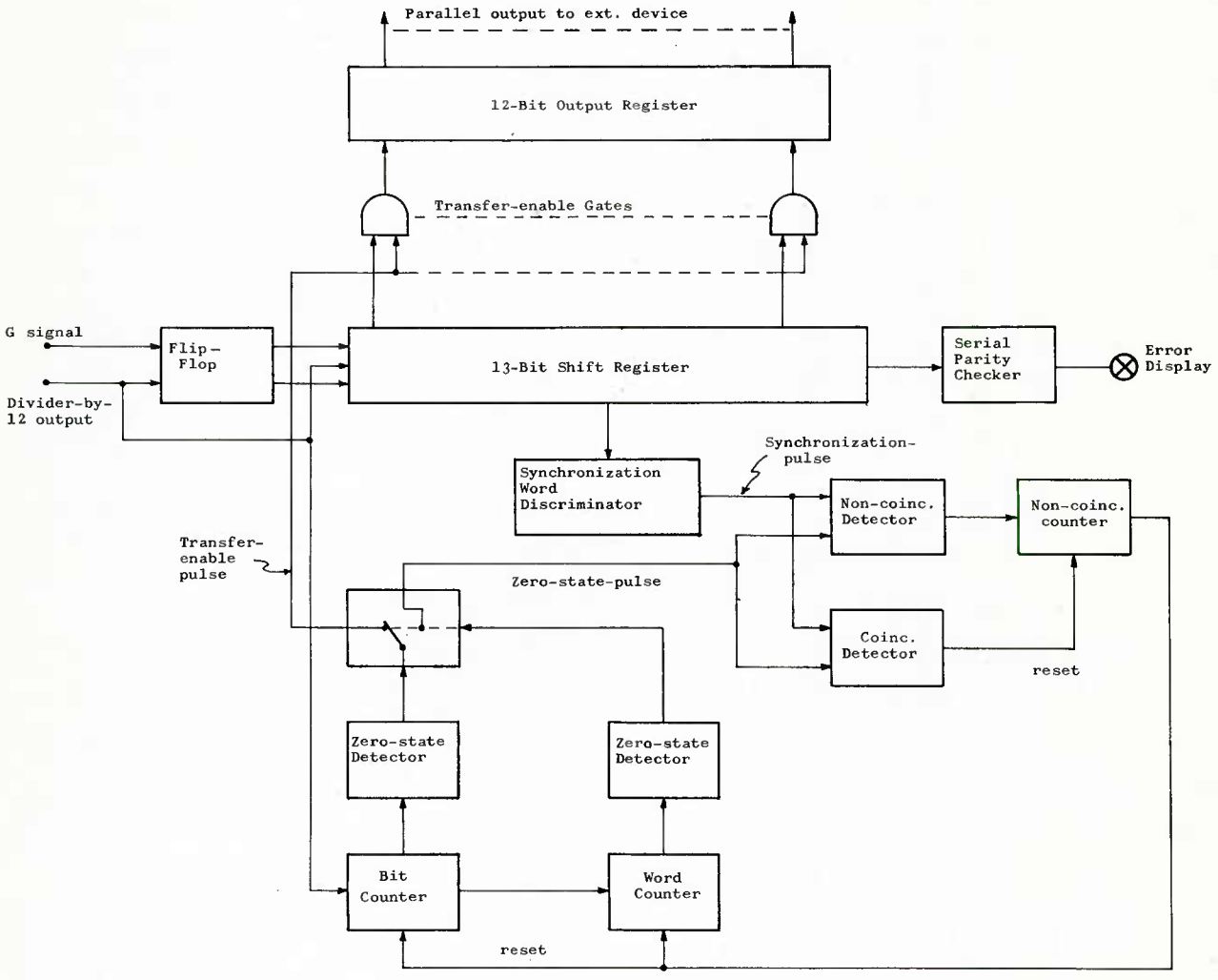


FIG. 19 SIMPLIFIED BLOCK DIAGRAM OF THE WORD SYNCHRONIZER

order to the output-register must be given at the instant when each word is exactly contained in the shift-register. Furthermore, the thirteenth bit of each word and the synchronization word must not be transferred. This requires the precise recognition of the moment at which each word is exactly positioned into the shift-register and the discrimination of the synchronization words against data words and parity words. Both the above results are achieved by means of a "bit-counter" and a "word-counter". The first produces a transfer-enable pulse at each thirteenth bit in the input bit sequence; the second inhibits this transfer-enable pulse once for each fourteen words i.e. when the synchronization word is contained in the shift-register.

Of course such a system requires a perfect synchronism between the counters and the succession of the incoming words; this is obtained in the following way. If we suppose the counters to be synchronized, we can define as "zero state" the state of the two counters just after the shift order that has brought the synchronization word exactly into the shift register. If we now identify the presence of the synchronization word in the shift register and the "zero state" of the counters by correspondingly generating a "synchronization-pulse" and a "zero-state-pulse", the system will be kept synchronized if these two pulses are kept coincident. For this purpose a "non-coincidence counter" is used that counts every non-coincidence of the above pulses and is reset to "zero" at each coincidence. If three consecutive synchronization words are found not to coincide with the zero state pulse, the last of the three is used for resetting the "bit-counter" and the "word-counter", thus providing the required synchronization. The non-coincidence counter is not strictly necessary, but has been included in the system to avoid synchronization losses due to the possible detection of spurious synchronization words. These are likely to correspond with long dropouts in the reading process.

The word synchronizer unit is illustrated in Fig. 19; one such unit is used for each of the twelve magnetic tracks.

4. COUNTER TRACK

4.1 Counter-Track Generation and Recording

Any editing or analysis operation to be performed on the recorded data requires the precise location on tape of each event or portion of it. When the analysis operation is performed in digital form, e.g. by means of a digital computer, the useful data sequence must be localized to the precision of a single sample.

Since, for each track pair, a complete group of twenty-four information-carrying words is produced exactly at each half millisecond, we decided to label each millisecond of recording time and to leave the sample-selection to the computer performing the analysis. Thus we record on Track 12 of the tape a binary-coded decimal number that increases by one at each millisecond, i.e. for each pair of 24-word groups. The one millisecond time interval between two successive numbers is produced by the same clock that governs all the recording system, thus providing a constant synchronism between counting-track numbers and data words.

A simplified block diagram of the counter-track recording system is shown in Fig. 20.

A twenty-seven bit, seven-digit, BCD counter counts an input pulse train with a repetition rate of 1 kHz. After each increment, the content of the counter is parallel-transferred to a shift register where a fixed pattern of nine bits is also transferred. Four of these nine bits are placed at the MSB side of the 27-bit word, while the remaining five are intermixed with the 27 bits. The fixed pattern serves for synchronization purposes in the reading phase. The 36-bit

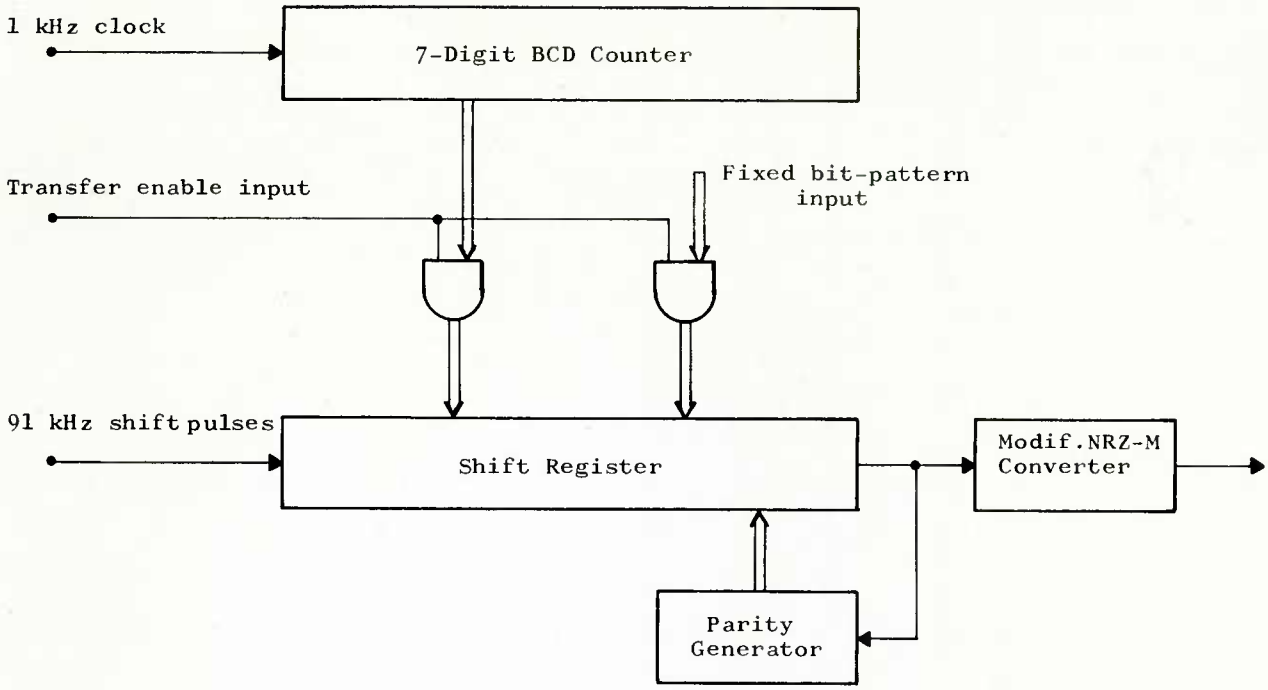


FIG. 20 SIMPLIFIED BLOCK DIAGRAM OF THE COUNTER TRACK GENERATOR

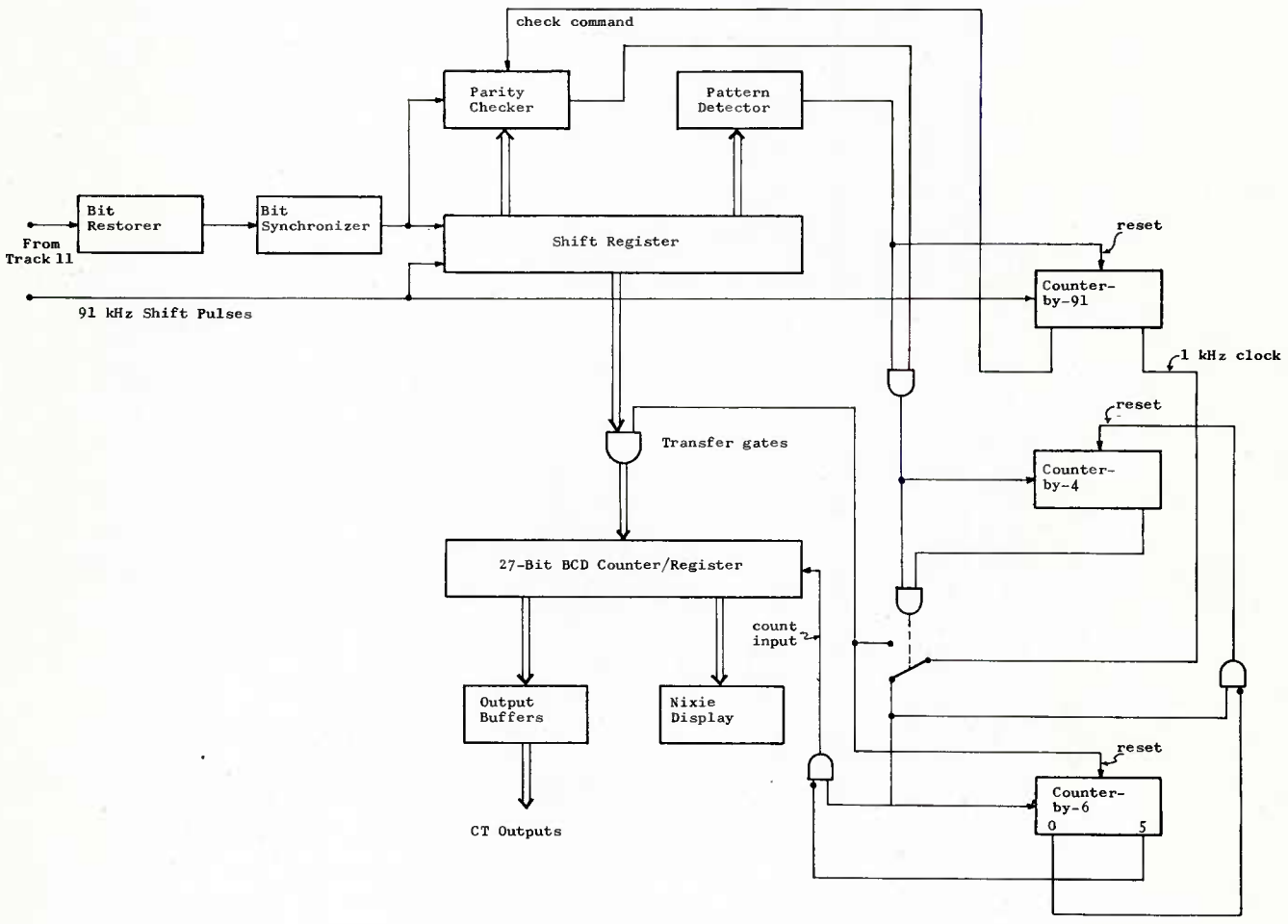


FIG. 21 SIMPLIFIED BLOCK DIAGRAM OF THE COUNTER TRACK READER UNIT

word contained in the shift register is taken out in series: during the shift operation a four-bit parity word is generated, where each bit gives the parity of a corresponding group of eight bits starting from the MSB of the 27-bit word and including the five intermixed bits of the fixed pattern. The four parity bits plus a fixed "zero" are added in series after the LSB of the 27-bit word. We thus generate a 41-bit word at each millisecond. The gap between two successive 41-bit words is filled by 50 "ones" in order to allow continuous synchronization during the reading phase. Hence we generate 91 kilobits per second: these, after transformation to our modified NRZ-C format, are recorded on Track 12 of the tape.

The 27-bit counter can be reset or preset to any number between zero and 7 999 999 by means of a set of digiswitches and its content is displayed by means of a set of seven nixie tubes. Remote control of the counter is also possible, e.g. it can be started when the tape recorder is in record mode and stopped when it is in reproduce mode or when the tape is stopped.

4.2 Counter-Track Reading

A simplified block diagram of the counter-track reading unit is shown in Fig. 21. The counter-track signal read from the tape must be restored in digital form and used for synchronizing the counter-track reading unit. For this purpose a bit restorer and a bit synchronizer are used that differ from those used for the other tracks only because of the lower clock frequency (91 kHz instead of 364 kHz). The restored digital signal is thus sent to a shift-register driven at a clock frequency of 91 kHz.

A decoder identifies the ten-bit fixed pattern and as soon as the first incoming pattern is recognized a counter-by-91 is reset to zero. This counter provides the one-millisecond timing for the system.

Once the counter is reset, thus synchronizing its output with the incoming sequence, the parity check of the sequence itself can be

started. Four parity bits are generated and compared with the recorded parity bits. If the fixed 10-bit pattern and the parity bits are found correct (we call this "condition S") for four consecutive times, we decide that no false pattern or parity recognition occurred. Accordingly, a counter-by-four allows the one-millisecond clock from the counter-by-91 to open the transfer gates from the shift register to a 27-bit counter/register. In other words, starting from the moment when four consecutive "conditions S" have been detected, the counter-by-four enables the parallel transfer of the 27 significant bits from the shift-register to an output register that is wired as a seven-digit BCD counter. If no errors are detected, the counter-by-four stays set at full content.

Whenever a wrong parity is detected or the fixed pattern is not recognized, the one-millisecond clock is switched to the counter input of the counter/register so that its content is correctly increased: no parallel transfer from the shift register occurs in this case. The same pulse that increases the content of the counter register also increases the content of a counter-by-six that is reset from the one-millisecond clock itself whenever the "condition S" is detected. After the detection of a first parity or pattern error we have two possibilities: either the following word is correct or it is wrong again. In the first case the 27 significant bits are transferred and the counter-by-six is reset to zero, while in the second case a second increment is given to the counter/register and to the counter-by-six. This second increment to the counter-by-six also resets the counter-by-four to zero: because of this the following four words are not transferred in any case and the counter/register is incremented by the one-millisecond clock another four times.

After these four increments the content of the counter register is increased, and words are transferred, only if four consecutive conditions S have been detected in the meantime, i.e. if the counter-by-four has reached full content; otherwise no increase or transfer takes place until full content of the counter-by-four is again reached.

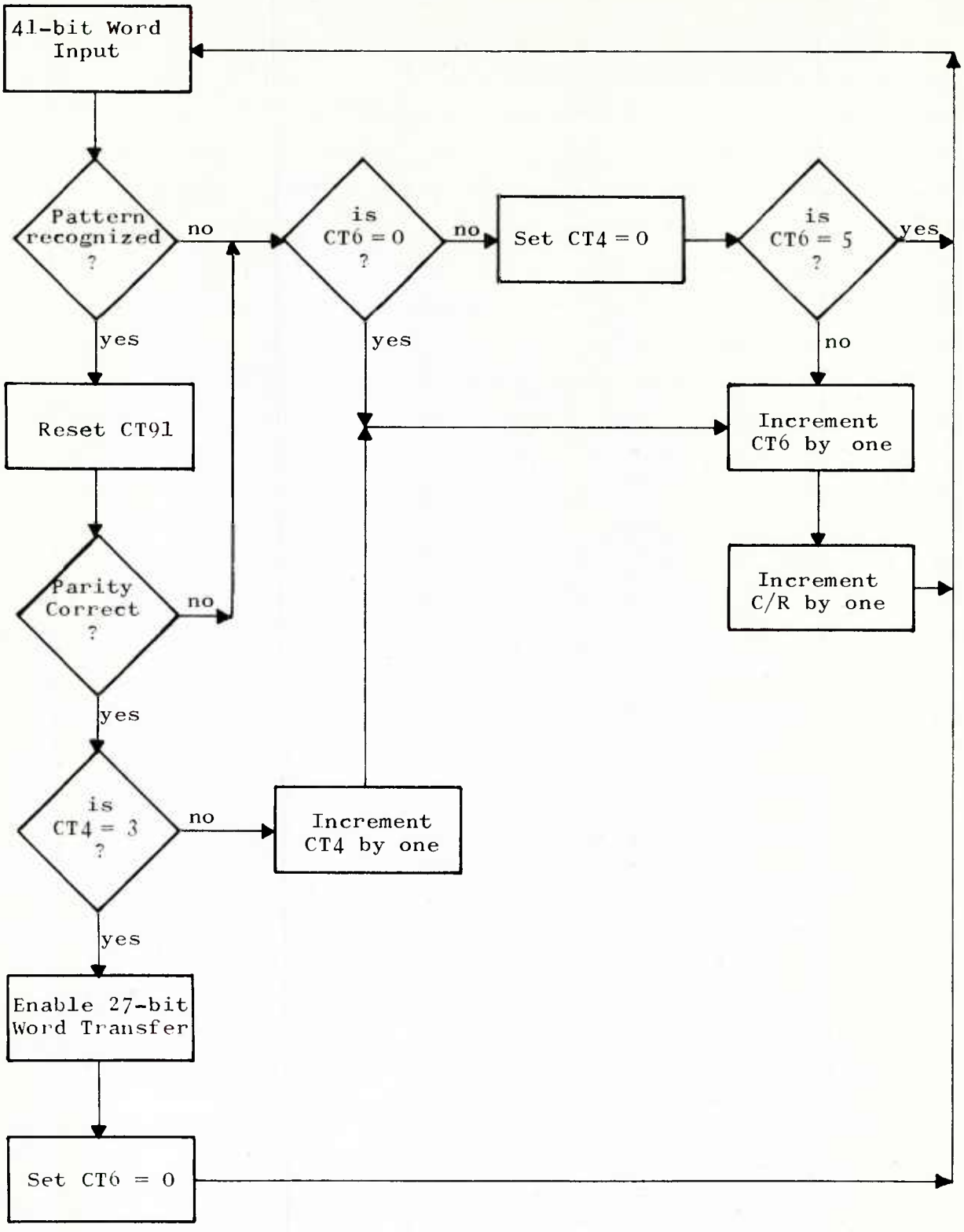


FIG. 22 OPERATION OF COUNTER TRACK READING UNIT

The system has been designed in this way for the following reason: considering that the counter-track reading process features an extremely low error rate (since the counter-track recording density is one-fourth the density used on other tracks), the detection of two consecutive errors nearly always means that the tape has been stopped or that it is in the fast rewind or fast forward modes. Thus the content of the counter/register must not increase any more in order to provide a useful indication about the last correctly read number. Another important case is when a recording gap occurs between two successive events on the tape: also in this case the counter/register has to be stopped during the recording gap. This is the typical case when data blocks are being transferred into a digital computer: the computer continuously reads the counter track, comparing it with a preset transfer-start number. Obviously a wrong transfer-start can occur if the counter/register continues to advance during a recording gap.

The operation of the counter track reading unit is further illustrated in the flow chart of Fig. 22 where all the possible operating sequences have been taken into account. The following abbreviations have been used:

CT 91	=	counter-by-91
CT 4	=	counter-by-4
CT 6	=	counter-by-6
C/R	=	counter/register.

It is recalled that, since "state zero" is included between the possible ones, the maximum content of CT 4 is three and that of CT 6 is five.

5. CONSTRUCTION DETAILS

The digital recording system has been completely built at SACLANTCEN, with the exception of the tape recorder and of the A/D converters. It consists of the following units:

1. The Receiving System, which occupies a complete rack and includes the variable-gain amplifiers and the low-pass filters with the relative power supplies.

2. The A/D Converters, which occupy a special rack-unit in which particular precautions have been taken with the wiring in order to minimize ground loops and crosstalk.

3. The Writing System, which is contained in a rack-mountable chassis and includes the floating-point converters (FPC), the pre-recording units (PRU), the vertical parity track generator (PTG) and the counter-track generator (CTG).

4. The Ampex AR1600 Tape Recorder, which is mounted on shock absorbers in a standard rack that includes the associated power supply and air-cooling system.

5. The Bit Restoring System, which occupies a rack-mountable chassis and includes the twelve bit-restorers and the voice-log.

6. The Reading System, which also occupies a rack-mountable chassis and includes bit-synchronizers, word-synchronizers, output registers and counter-track reader.

To make the construction work as easy and fast as possible, modular circuitry has been employed wherever possible.

Honeywell-3C μ-Pac micrologic cards have been used to build the digital circuitry. The wire-wrap technique has been extensively

used for the interconnections of the logic cards. Figure 23, which shows the underneath of the Reading System, demonstrates the wiring technique. A typical micrologic card is also shown in the lower right of the picture.

The bit-restorers have been built with modular operational amplifiers and hybrid thick-film voltage regulators; discrete components have also been used. The bit-restoring system is shown in Fig. 24; a typical card is shown on the left of the picture.

Figure 25 shows the front panel of the writing system, on which can be seen the overflow indicators, a set of nixie tubes displaying the counter-track numbers, and various controls for presetting and driving the counter-track generator. Figure 26 shows the front panel of the reading system, with the counter-track display and the parity-error indicators for odd tracks(1_O, 2_O, 3_O, 4_O, 5_O), even tracks (1_E, 2_E, 3_E, 4_E, 5_E), parity track (P), and counter track (C).

Figure 27 shows the transport side of the coaxial-wheel wide-band tape recorder employed.

The complete system mounted aboard SACLANTCEN's MARIA PAOLINA G. during a sea-trial is shown in Fig. 28.

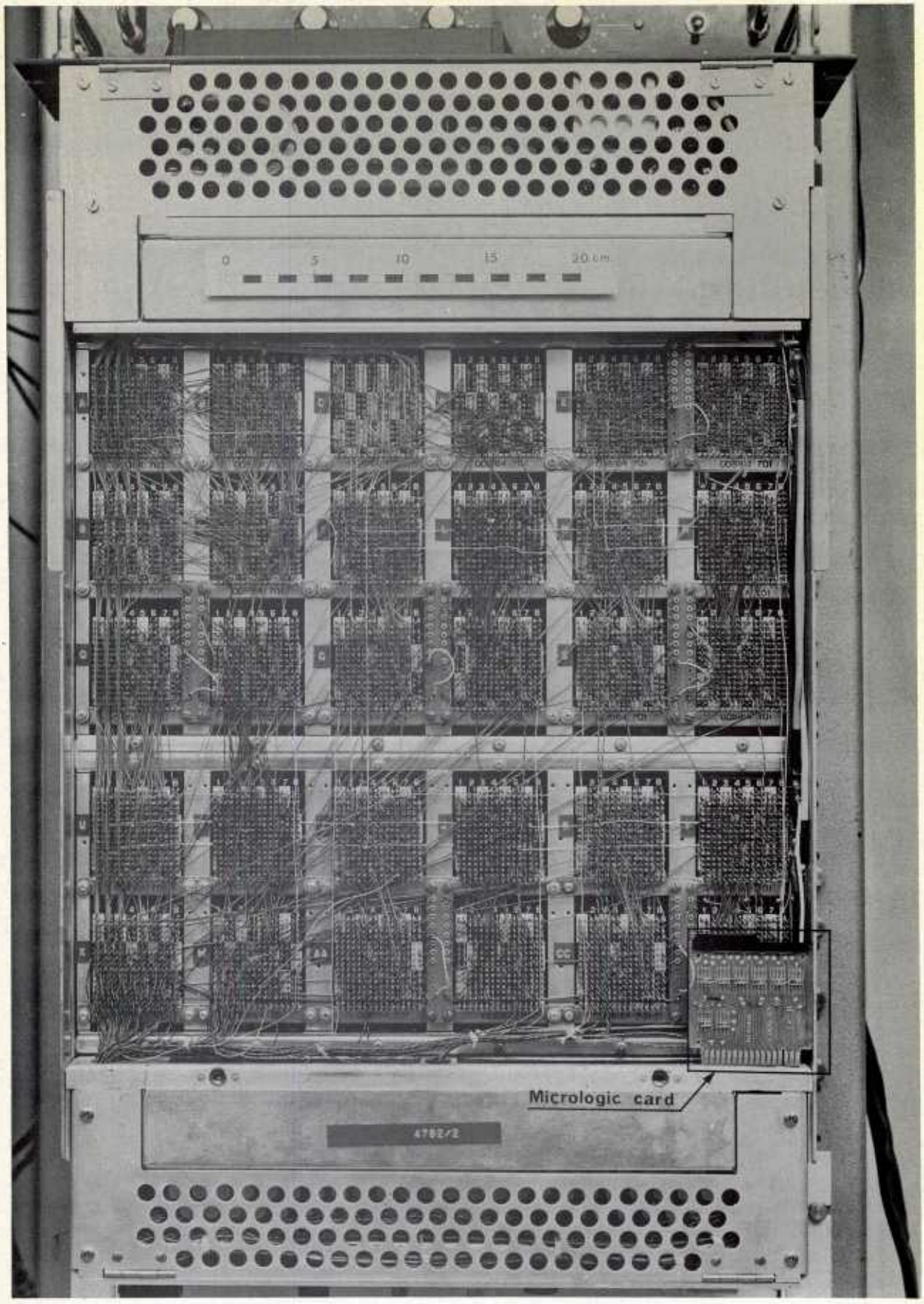


FIG. 23 BOTTOM OF THE READING SYSTEM

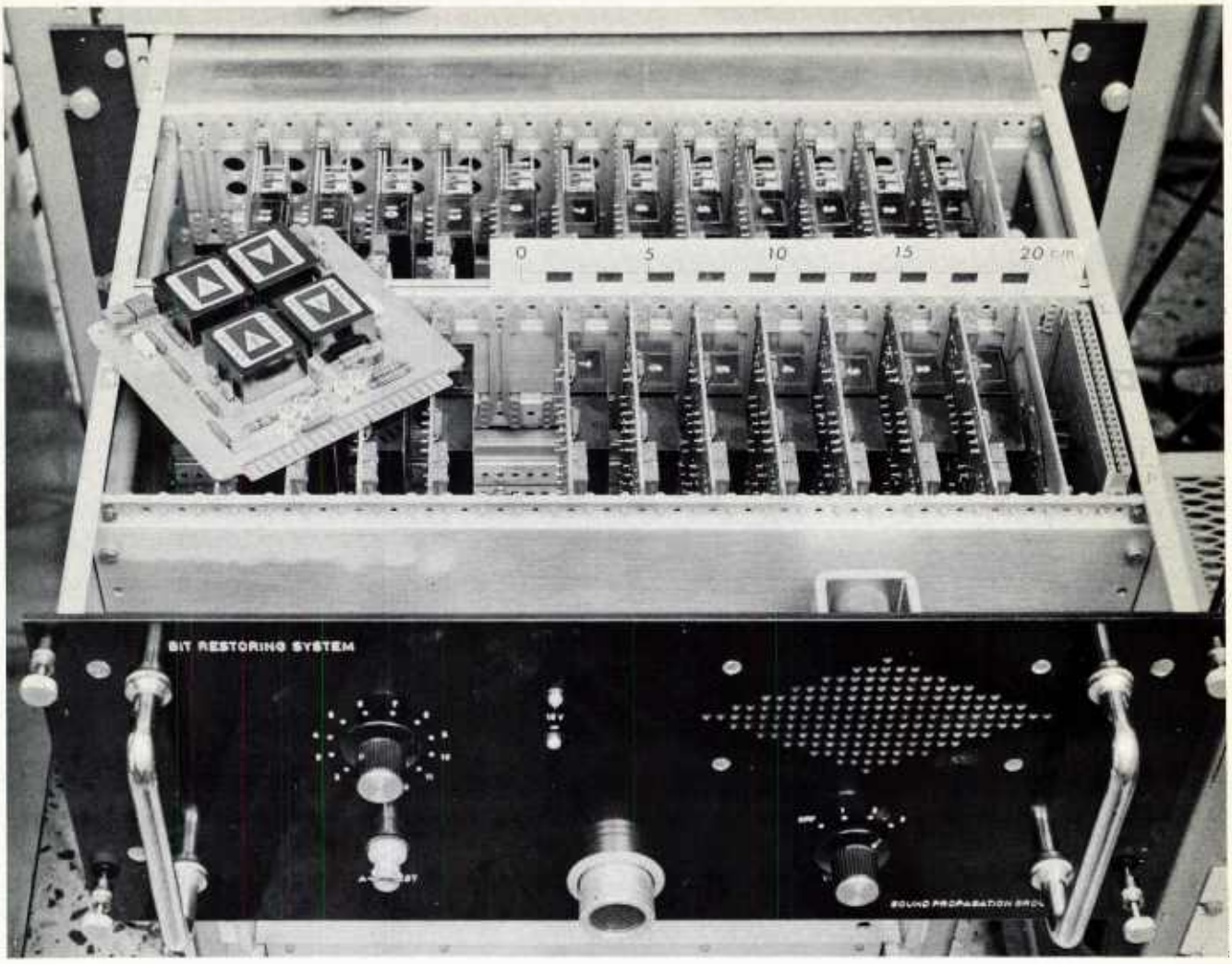


FIG. 24 BIT RESTORING SYSTEM

FIG. 25 FRONT PANEL OF THE WRITING SYSTEM

FIG. 26 FRONT PANEL OF THE READING SYSTEM

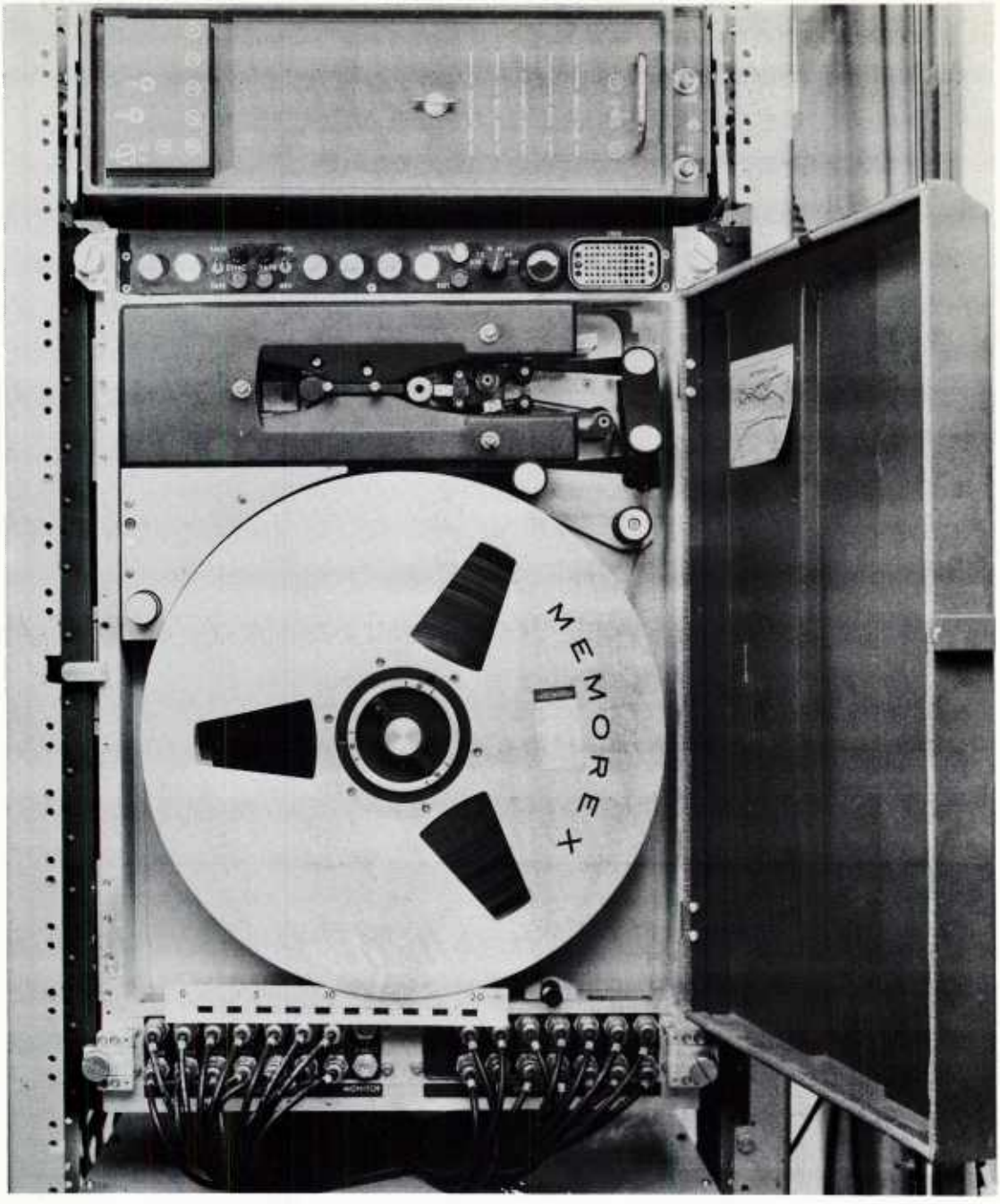


FIG. 27 WIDE-BAND TAPE RECORDER

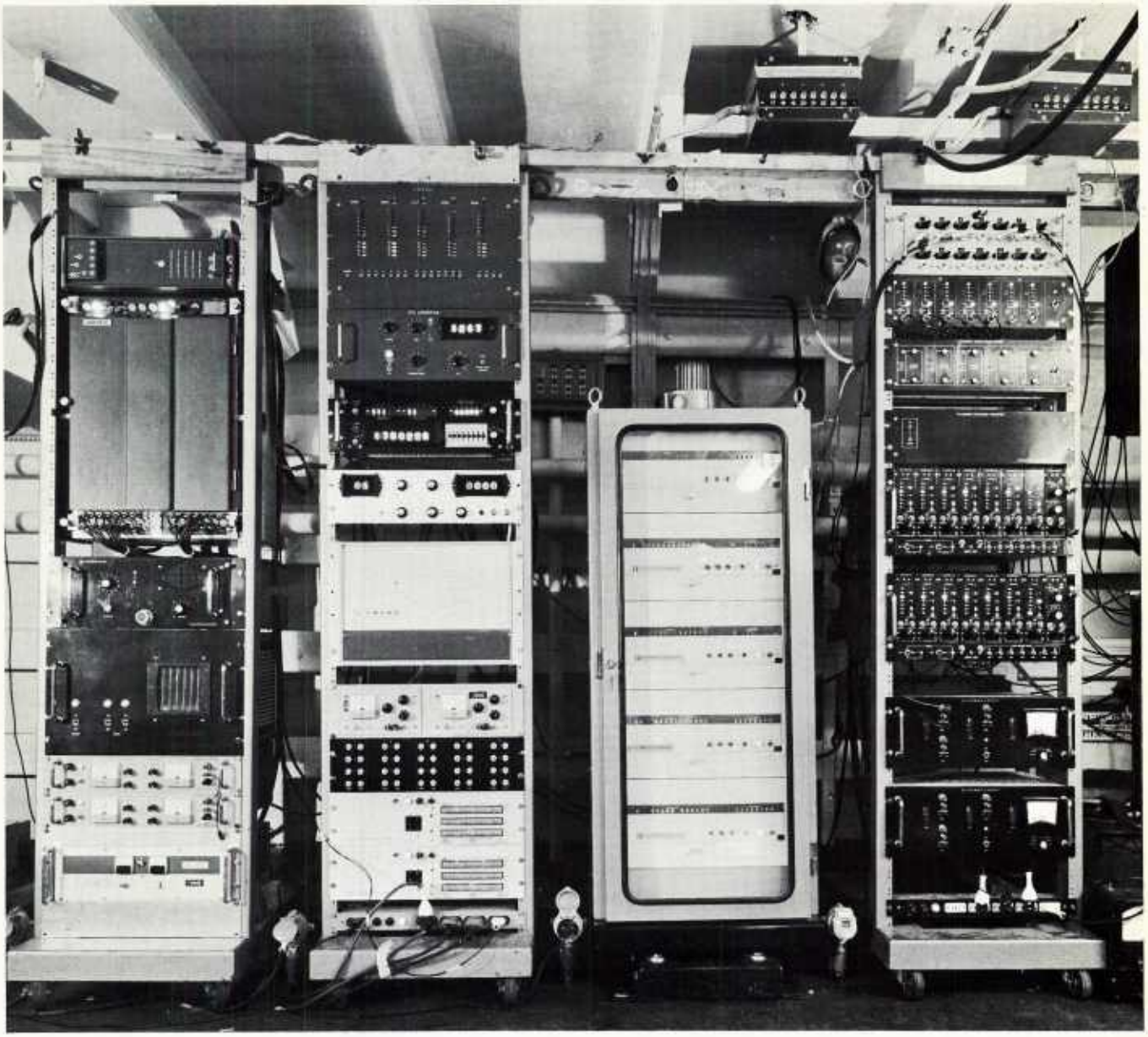


FIG. 28 THE DIGITAL RECORDING SYSTEM ON BOARD THE MARIA PAOLINA DURING A SEA TRIAL

6. OPERATING RESULTS

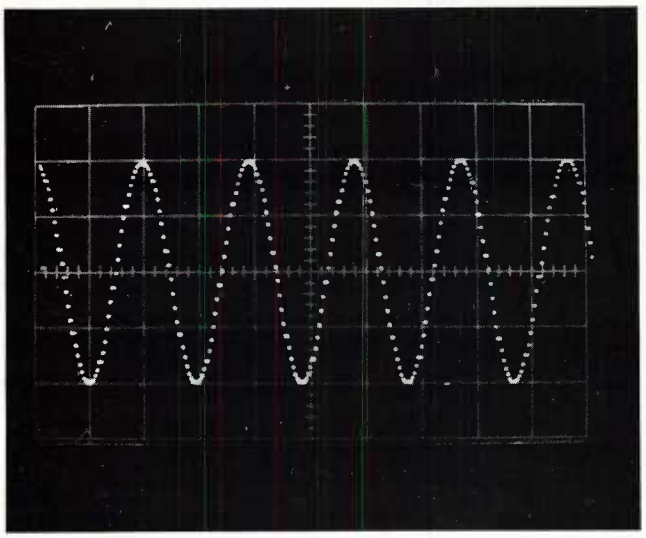
Figure 29 shows the results of a test in which 1 kHz sinusoidal signals of various amplitudes taken from an a.c. calibrator were recorded on a full channel of the system, i.e. at a sampling frequency of 48 000 samples/second. The signals were then reproduced from the tape and reconverted in analogue form using a special D/A converter built to be capable of handling the floating-point data-words and allowing the insertion in digital form of a gain that can be varied in 6 dB steps.

Figure 29a shows the D/A converter output for a voltage of 6.880 V rms applied at the A/D converter input. Figures 29b, c, d, e, and f show the same for input voltages of 0.855 V, 0.121 V, 15 mV, 2.1 mV, and 1.1 mV rms, respectively.

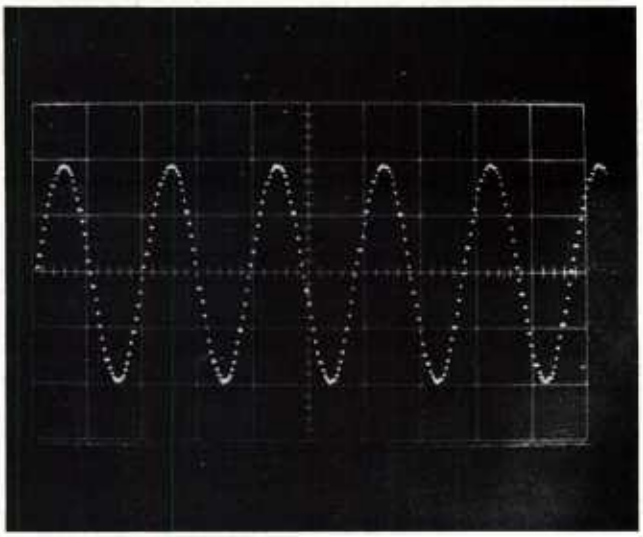
The signal of Fig. 29a is very near to the maximum allowed input for the A/D converter. Thus the dynamic range of the system appears to be of the order of 80 dB; this holds for a single input-gain setting since the variable-gain amplifiers were kept at zero dB gain.

Figure 30 shows the output of the D/A converter with four signals applied to the same A/D converter by means of the multiplexer; each signal is here being sampled at 12 000 samples/second.

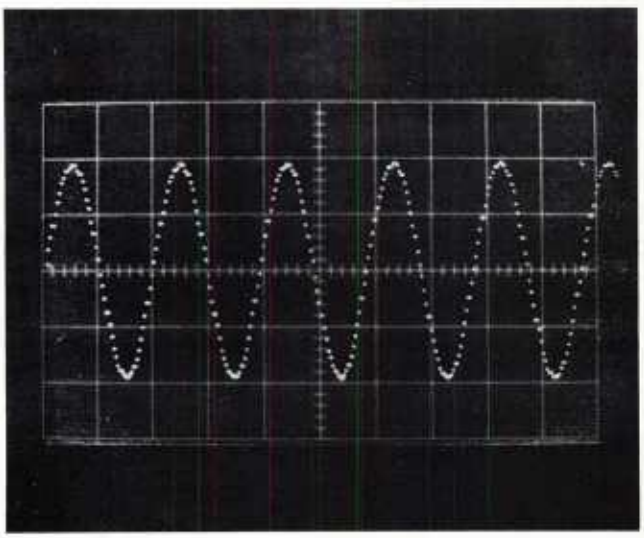
Figure 31 shows plots of a signal collected at sea during an experiment with explosive sound sources. These were made by a CALCOMP plotter after transfer of the digitally-recorded data to the digital computer. The same event is shown using four different vertical scales given as computer instructions by a special software package (SACLANTCEN Computer Program No. 77.) Scales, counter track numbers, event code and hydrophone number are automatically written on the plots.



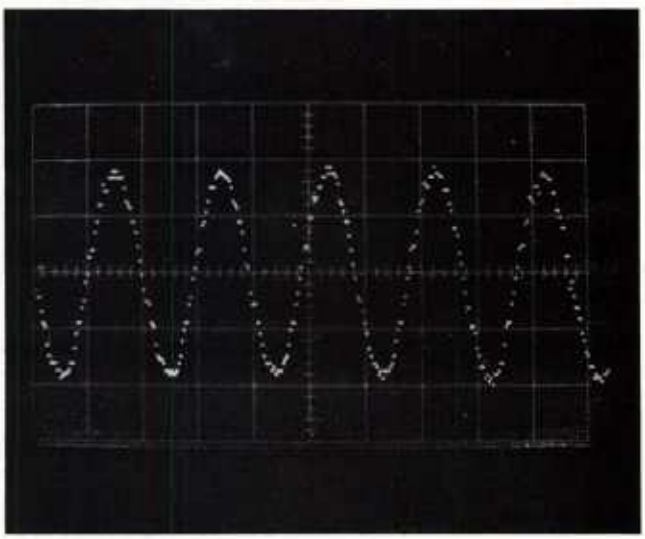
a



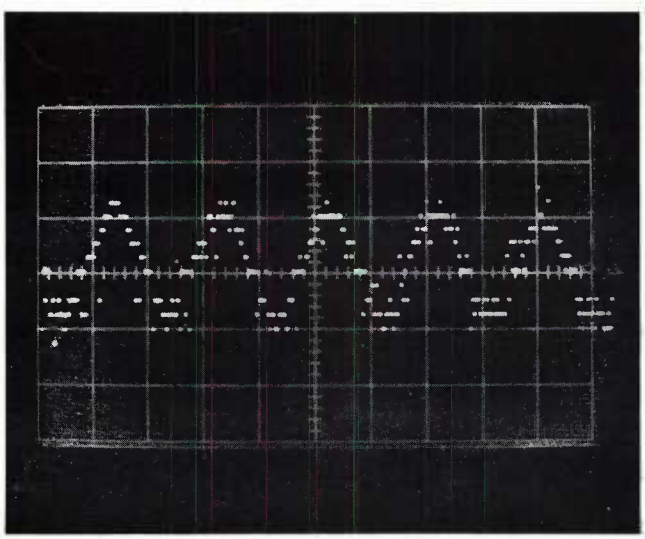
b



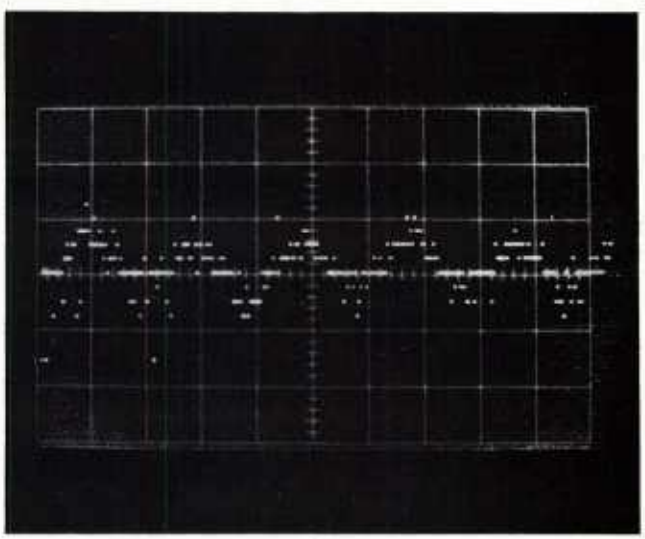
c



d



e



f

FIG. 29 DYNAMIC RANGE D/A Converter outputs for inputs of
(a) 6880 mV, (b) 855 mV, (c) 121 mV, (d) 15 mV, (e) 2.1 mV, (f) 1.1 mV rms

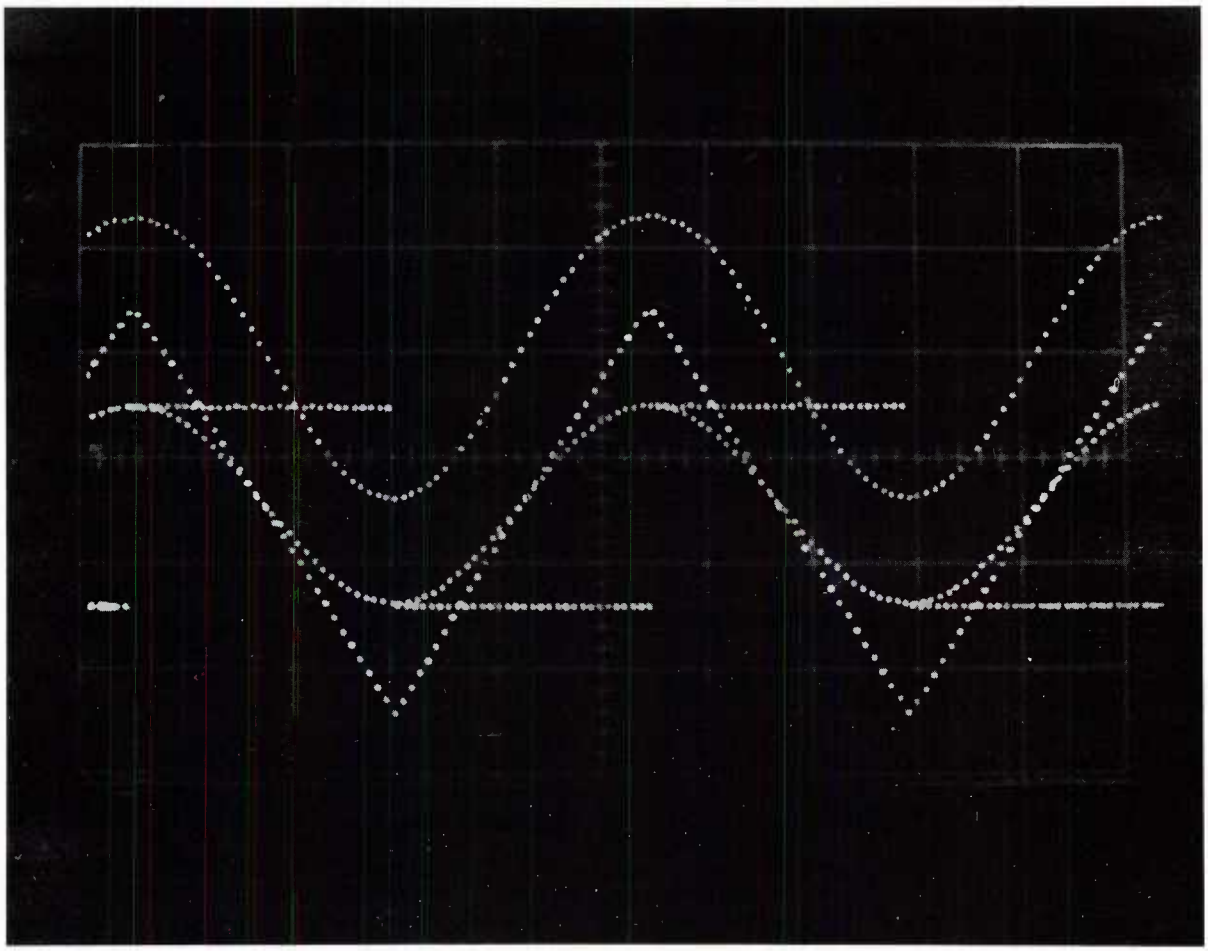


FIG. 30 MULTIPLEXER PERFORMANCE D/A Converter output with four signals applied to same A/D Converter by the Multiplexer. Sampling rate: 12000 samples/second

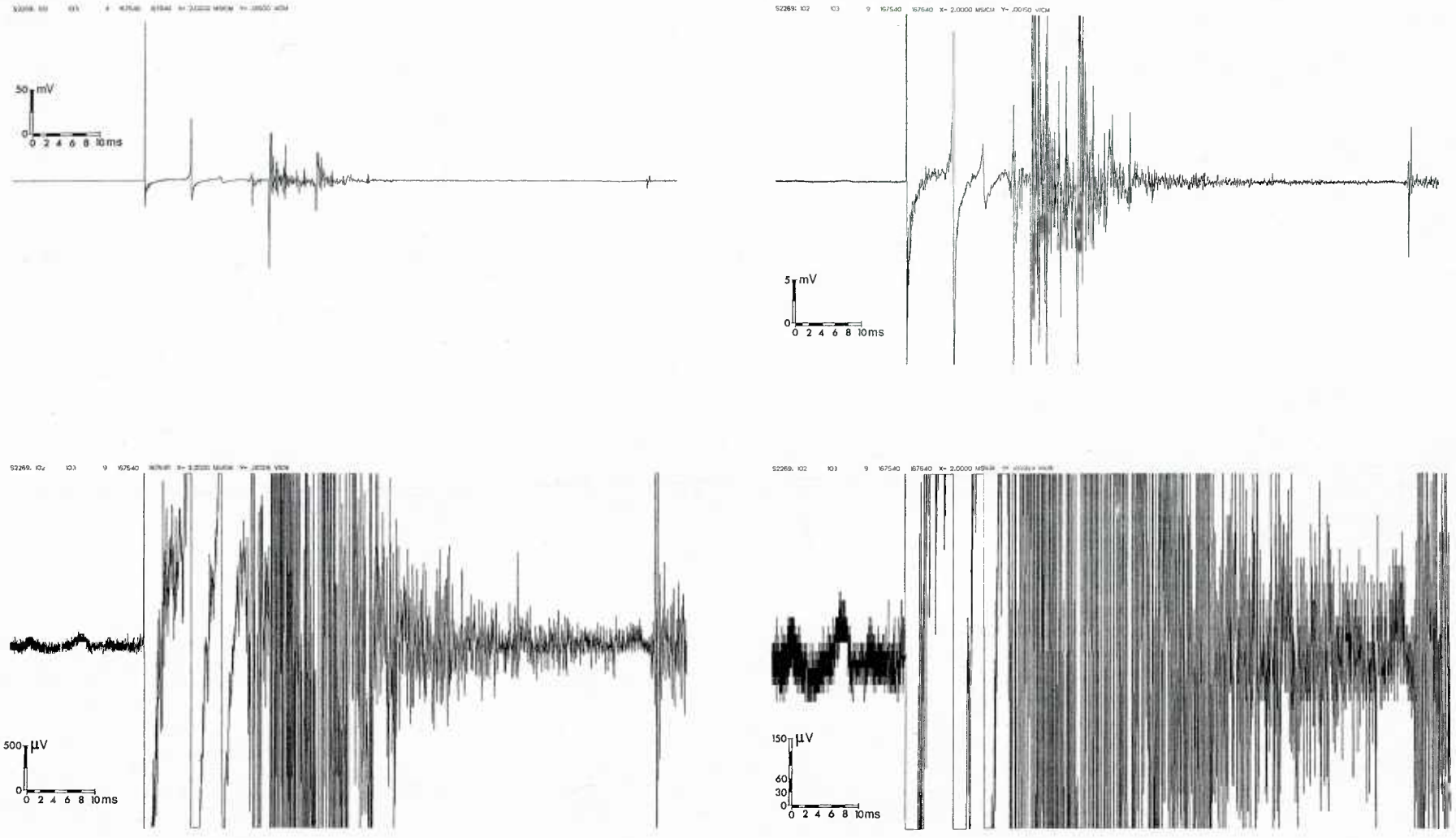


FIG. 31 COMPUTER PLOTS OF A SIGNAL COLLECTED AT SEA DURING AN EXPERIMENT WITH EXPLOSIVE SOUND SOURCES, four different vertical scales are used

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