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RADC USAF LTR, 17 SEP 1971

RADC-TR-69-350
Final Technical Report
October 1969

FAILURE RATE PREDICTION FOR COMPLEX BIPOLAR MICROCIRCUITS

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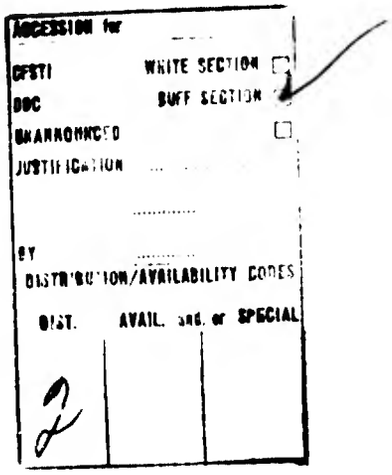

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FAILURE RATE PREDICTION FOR COMPLEX BIPOLAR MICROCIRCUITS

Peter F. Manno

FOREWORD

This technical report was prepared by Mr. Peter F. Manno under project 5519.

This report has been reviewed and is approved.

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ABSTRACT

The intent of this report is to provide a reliability prediction technique for complex bipolar microcircuits, commonly referred to as small-, medium- and large-scale integration. Failure mode distributions for complex microcircuits are projected from failure mode data on standard integrated circuits. This is done by the use of failure mode multipliers which are determined by linear extrapolations from a representative breakdown of composite industry-wide failure mode data on current state-of-the-art integrated circuits.

The RADC failure rate prediction model for standard integrated circuits is extended to cover these new complex circuits. To achieve this, an additional term, to account for the variations in processing and fabrication of complex microcircuit arrays, is introduced into the standard model along with the standard multipliers (which have been extended or altered) according to the number of gates, packaging configuration, and increased silicon chip area. The base failure rate for standard circuits will also be used as the basis of the new prediction technique. Optimum failure rates are calculated for some typical complex circuits and compared to the failure rate of their discrete integrated circuit equivalent.

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1.0 INTRODUCTION

During the last decade, the electronic industry has progressed from solid state discrete devices to the present silicon monolithic microcircuits. Today, the present state of the art is moving toward a new era of multi-integrated circuit arrays commonly known as LSI (large scale integration). In some ways, this technology has already arrived and will soon be proposed for military use. In anticipation of the early introduction of LSI devices in Air Force systems/equipment, RADC is attempting to develop, under contract[1], procedural guidelines which can be used for the reliability assessment of complex arrays. This effort will result in qualitative definitions of the critical parameters that must be considered in LSI reliability evaluations, effective screening procedures, and qualification and acceptance testing techniques for LSI devices. The problems associated with failure analysis will also be considered. However, in the interim, with the arrival of more complex microcircuits, such as shift registers and 30-gate configurations, there is a need to provide Air Force project engineers with a preliminary technique for assessing their reliability when used in an equipment or system. Since limited life test or use data exist on these types of devices, only ballpark figures for predicting failure rates can be provided. These ballpark figures will be based solely on engineering judgment, experience, and previous reliability data on standard integrated circuits (ICs) and not on testing and demonstration. As more reliability data on the complex devices become available, the models and adjustment factors, presented herein, will be altered or changed to improve accuracy.

2.0 DEFINITIONS

For the purpose of this report, complex microcircuits are placed in three categories of complexity: small scale integrated circuit arrays (SSI), medium scale integrated circuit arrays (MSI), and large scale integrated circuit arrays (LSI). SSI is considered to contain from 16 to 32 gates or circuits on a chip; MSI from 33 to 64 gates or circuits per chip; and LSI over 64 gates or circuits per chip. A circuit is considered to be the smallest group of elements which are required to perform an individual function. A simple flip-flop would, therefore, consist of two gates. A complex circuit, such as a shift register, which is specified in total bits, will be considered on a flip-flop-per-bit basis. However, any circuit containing more than one layer of metallization on the silicon chip, regardless of the number of gates, is considered in the MSI or LSI category and will be treated as such in this report. This is attributable to the increase and variations in processing, and a decrease in the tolerance of such problems as pinholes. In all likelihood, however, any circuit employing more than one layer of metallization will contain a sufficient number of gates to be numerically placed into the MSI or LSI category.

3.0 DEVELOPMENT OF RELIABILITY RELATIONSHIPS

In order to establish the reliability relationship between standard integrated circuits and the aforementioned complex integrated circuits, multipliers have been developed to predict the failure mode distributions, and adjustment factors have been developed to project the failure rates from one to the other. This is justifiable in that the same materials and processes are used, the only real variables being the extent and magnitude of usage and processing configuration.

3.1 FAILURE MODE BREAKDOWN

A contractual effort[2], currently in progress at Philco-Ford, has resulted in the classification of quality defects observed in standard integrated circuits in terms of their frequency of occurrence as causes of failure (see Table I). This failure mode breakdown resulted from the analysis and categorization of failures at initial acceptance and from rated stress levels of life and environmental testing. The data are not restricted to a specific circuit type or process and were collected over a three-year period.

In addition, this breakdown is representative of the composite industry-wide failure mode data on current state-of-the-art integrated circuits as can be seen in references 2 and 3.

TABLE I

FAILURE MODE DISTRIBUTIONS FOR STANDARD INTEGRATED CIRCUITS IN PERCENTAGES

FAILURE MODE	DISTRIBUTION FOR STANDARD ICs
Open metal at oxide steps	25.1
Hermeticity	10.4
Bond failures	19.0
Photolithographic defects	18.6
Contact cut resistance	12.5
Wire defects	5.1
Channeling	4.4
Foreign material	3.5
Miscellaneous	1.4
	100.0%

3.2 FAILURE MODE MULTIPLIERS

The failure mode multipliers for complex devices are determined by linear extrapolations of each failure mode listed in Table I, on a per gate, per bond, and total area basis. To establish a base for the multipliers, a three-gate circuit with a 14-lead package is considered. The data are on Philco-Ford circuits PL969, PL962, PL929, and PA702[2]. This circuit was chosen because it is a simple circuit, has a high usage, and its failure mode distribution is identical to the one listed in Table I. This triple nand gate has three inputs per gate and has a total chip area of 2000 square mils. The multipliers to project the percent contribution of each failure mode on a per gate, per bond, etc., basis are given in Table II.

TABLE II

FAILURE MODE DISTRIBUTION BREAKDOWN

FAILURE MODE	MULTIPLIER (%)
Metallization	8.4 per gate
Hermeticity	0.74 per pin or 0.0052 per square mil if circuit dim. are given
Bond Failures	1.4 per bond
Photolithographic Defects	6.2 per gate
Contact Cut Resistance	4.2 per gate
Wire Defects	0.36 per wire
Channeling	1.5 per gate
Foreign Material	0.00175 per square mil
Miscellaneous	0.0007 per square mil

3.2.1 EXAMPLES OF CALCULATION OF MULTIPLIERS

These multipliers were calculated using the data contained in Table I and the characteristics of the three-gate integrated circuits. The following are example calculations:

a. Example 1:

25.1% of the quality defects were due to metallization problems.

$\frac{25.1\%}{3 \text{ Gates}} = 8.4\%$ per gate

This is the multiplier for metallization.

b. Example 2:

19% of the quality defects were due to bonding problems.

$\frac{19\%}{14 \text{ Bonds}} = 1.4\%$ per bond

This is the multiplier for bonds.

The failure mode percentage contributed by hermeticity, foreign material, and miscellaneous are considered on a total area basis. That is, if the die area increases then the percentage contribution of each one to the failure mode distribution also increases. Hermeticity can also be treated on a per bond basis, and justly, for as the number of pins and package size increases, the probability of poor sealing occurring also increases. This is done because there may be some complex microcircuits with only 14 leads; conversely there may be comparatively small, complex circuits with large numbers of leads.

3.3 EXPECTED FAILURE MODE DISTRIBUTION FOR COMPLEX MICROCIRCUITS

Using the data contained in Table II, the expected failure mode

distribution for any complex microcircuit can be predicted assuming linear extrapolation in accordance with the criteria specified in paragraph five. The only required information on the complex circuits is the number of pins, number of bonds, chip area, and number of gates or circuits per chip. In Tables III-A and III-B an example for the prediction of the failure mode distribution of a commercially available complex microcircuit, a four-bit binary full adder, is presented. This circuit contains 36 gates, 16 pins, and 16 bonds, and is classified in the MSI category.

Other examples of expected failure distribution for complex microcircuits are given in Appendix A.

TABLE III-A

PREDICTED FAILURE MODE DISTRIBUTIONS
FOR COMPLEX CIRCUITS

Metallization	36 x 8.4% per gate =	301.20%
Hermeticity	16 x .74% per pin =	11.84%
Bonds	16 x 1.4% per bond =	22.40%
Photolithographic Defects	36 x 6.2% per gate =	223.20%
Contact Cut Resistance	36 x 4.2% per gate =	150.00%
Wire Defects	16 x .36% per bond =	5.76%
Channeling	36 x 1.5% per gate =	54.00%
Foreign Material		3.50%
Miscellaneous		1.40%
		773.30% Total

TABLE III-B

NORMALIZATION OF PREDICTED FAILURE MODE DISTRIBUTIONS
FOR COMPLEX CIRCUITS

Metallization	38.96%
Hermeticity	1.53%
Bonds	2.90%
Photolithographic Defects	28.86%
Contact Cut Resistance	19.40%
Wire Defects	.74%
Channeling	6.98%
Foreign Material	.45%
Miscellaneous	.18%
	100.00% Total

3.3.1 DISCUSSION OF REPORTED FAILURE MODES

This predicted failure mode distribution agrees closely with the reported[4] expected failure modes for complex circuit arrays which are:

a. Metallization problems

b. Surface effects

c. Bond and package failures

d. Dielectric integrity.

3.3.2 BONDING CONTRADICTION

However, as can be seen in the normalized failure mode distribution chart, the percent contribution due to bond problems is greatly reduced in comparison to standard monolithic ICs. This implies that bonds are not going to present a problem, relative to the other failure modes, but as a larger number of pins are used, for example in LSI (40 pins), the failure mode distribution will change drastically. Later in this report factors to account for the contribution of bond failures to the overall device failure rate will be presented.

4.0 RADC FAILURE RATE PREDICTION MODEL FOR STANDARD ICs

In the latest version of the RADC Reliability Notebook[5] the mathematical model used to predict the failure rate, λ_M, of double and triple diffused silicon and single layer metallization planar monolithic microcircuits is given as:

$$\lambda_M = \lambda_b \pi_C \pi_Q \pi_E \pi_P$$

where:

λ_M = microcircuit failure rate in %/1000 hours

λ_b = a base failure rate (function of junction temperature)

π_C = a complexity adjustment factor

π_Q = a factor based on achieved reliability

π_E = an environmental adjustment factor

π_P = adjustment for package type factor

4.0.1 DIFFERENCE BETWEEN STANDARD AND COMPLEX PREDICTION MODELS

Present and future complex circuits will differ from today's microcircuits mainly in the total number of gates per chip, package size, number of pins, and number of layers of metallization. The mathematical model for standard circuits can be modified, to consider these expected differences, by the addition of a new term and adjusting the magnitude of the values for the other factors given in the RADC Reliability Notebook.

4.1 COMPLEX CIRCUIT PREDICTION MODEL

The model for predicting the failure rate, λ_{MC}, of complex

microcircuits would then be given as:

$$\lambda_{MC_x} = \lambda_b \left[\left(\pi_C \pi_{P_C} \pi_E \pi_Q \right) + \pi_{M_x} \right]$$

where :

λ_{MC_x} = complex microcircuit failure rate at any specified temperature - x, and the new term on the righthand side of the equation is:

$$\pi_{M_x} = \frac{\sum_M}{\lambda_b}$$

where:

M = 0.0023%/1000 hours for each layer of metallization in the circuit under consideration,

λ_b = base failure rate of circuit at the temperature x.

Metallization increases are also treated in the complexity factor, π_C, due to the increased number of gates and also as a separate entity π_M. Circuits containing larger numbers of gates with the accompanying increase in metallization will have higher complexity factors which are independent of temperature. The additional term, π_M, will take into account interactions between layers which may or may not be a function of temperature. This method allows for uniformity of the multipliers and allows for future expansion and simplified corrections.

4.1.1 ENVIRONMENTAL AND QUALITY FACTORS, π_E AND π_Q

The environmental factor, π_E, and the quality factor, π_Q, given in Tables IV and V, respectively,should not differ from those given for standard ICs. These are valid assumptions, in that the military use environments will not change, and the relative effectiveness of reliability screening

TABLE IV

ENVIRONMENTAL ADJUSTMENT FACTOR, π_E

Environment	π_E
Laboratory	1.0
Satellite, Orbit	1.5
Ground, Fixed	2.0
Ground, Portable	5.0
Ground, Mobile	7.0
Airborne, Inhabited	5.0
Airborne, Uninhabited	7.0
Satellite, Launch	8.0
Missile	10

TABLE V

ADJUSTMENT FACTOR, π_Q

π_Q	Quality Grade
1	Optimum Screen which includes: (a) Vendor, line and product qualifications. (b) Line discipline on an interference basis. (c) Failure feedback (tight loop) with continuous corrective action similar to Minuteman procedures. (d) Screens and burn-in. (e) Traceability of test data.
2	Upper Grade which includes: (a) Screens and burn-in comparable to MIL-STD-883 based on limit testing (sample subjected to destructive tests to establish absolute limits of stresses which devices can withstand) to identify major failure modes and mechanisms to which screens are tailored. (b) Feedback from screening results only.
15	Average Grade which includes: (a) Normal production grade and lot acceptance testing on a sampling basis. (b) No 100% screening beyond routine vendor procedure for electrical parameters and hermeticity.
30	Lower Grade which includes routine vendor procedures which are applied to all production devices on a 100% basis.

and quality control will not be reduced in the manufacture of complex microcircuits. However, the remaining adjustment factors and additional terms will vary and thus a discussion of each is needed.

4.1.2 COMPLEXITY FACTOR, π_C

The complexity factor, π_C, for standard microcircuits is based on the number of oxide steps and contact cuts, and is presented in the RADC Reliability Notebook as a numeric according to circuit type. As circuits become more complex, the number of oxide steps and contact cuts will approximately increase in direct proportion to the increase in the number of gates. In the RADC Reliability Notebook the value of the complexity factor for standard microcircuits varies from one for a simple gate to four for a dual J-K flip-flop. It will be assumed that the number of contact cuts and oxide steps will increase linearly as complexity increases. Therefore, the complexity factors, given in Table VI for SSI, MSI, and LSI, are extrapolated by considering an increase of one in the complexity factor as the number of gates doubles.

TABLE VI

COMPLEXITY FACTORS FOR
STANDARD AND COMPLEX MICROCIRCUITS

Complexity Factor π_C	Logic	Input Description (per function) or Number of Leads (per package)
1	Basic Single Gate	up to 4 inputs
	Buffer	1 input
	Single Gate	4 to 8 inputs
	Dual Gate	up to 4 inputs
	Expander	up to 5 inputs
	NAND/NOR Gate	up to 5 inputs
	AND/OR Gate	up to 5 inputs
	Dual Inverter	any
2	Triple Gate	up to 4 inputs
	Exclusive OR Gate	up to 4 inputs
	Triple NAND Gate	up to 3 inputs
	Triple NAND/NOR Gate	up to 3 inputs
	NAND/NOR with Emitter Follower	up to 6 inputs
	Adder	any
	Quad Gate	up to 4 inputs
	Dual Expander	up to 4 inputs
	Dual NAND/NOR Gate	up to 5 inputs
	Quad Inverter Driver	any
	Triple NAND/NOR with Emitter Follower	up to 4 inputs
	Simple Flip-flop	2 inputs
	Pulse Exclusive-OR	any
3	JK Flip-flop with Preset AND/OR Clear	any
	Dual Exclusive-OR Gate	up to 4 inputs
	One Shot Multivibrator	
	JK/R-S Flip-flop	
	Quad NAND/NOR	any
4	Dual Simple Flip-flop	2 inputs
	RS Flip-flop/counter	any
	Ripple Counters	any
	Dual JK Flip-flop with Preset AND/OR Clear	any

TABLE VI continued

Complexity Factor π_C	Logic	Input Description (per function) or Number of Leads (per package)
5	16-32 Gates (SSI)	up to 20 leads
6	32-64 Gates (MSI)	up to 30 leads
7	64 Gates or Greater (LSI)	greater than 30 leads

These complexity factors appear to be reasonable at this time and vary according to the criteria established for standard IC's.

4.1.3 PACKAGING FACTOR, π_{P_C}

The packaging factor, π_P, for standard microcircuits varies depending on the type of package and method of die bonding. For an average chip area of 2500 square mils, 14 leads, and with a flat pack configuration, the standard microcircuit packaging factor is two. As the package size increases, the packaging factor should also increase. However, the most critical consideration in determining the packaging factor is the quality of the "seal." Therefore, the effect on the packaging factor due to the increased perimeter will not be as great or as important as the hermeticity problems due to an increased number of external leads over the standard fourteen. Also, failures due to poor bonds will continue to be a reliability problem as in standard ICs. Therefore, the increase in the failure rate due to bonding problems will also be accounted for in the packaging factor. The new packaging factor will consider an increase of .04 for each lead over the standard fourteen in the circuit under consideration. This number was empirically derived using the expected percent contributions in the predicted failure mode distribution (Table II) along with failure rate data on standard integrated circuits[3]. This new factor also takes into account package deficiencies and the increased hermeticity problems. The packaging factor, π_{P_C}, for complex microcircuits can be determined by the following equation:

$$\pi_{P_C} = 2 + (N - 14)\ (.04)$$

where:

π_{P_C} = packaging factor for complex microcircuits,

N = number of leads of circuits under consideration.

The use of new materials such as plastics, and methods such as flip-chip and beam-lead bonding, will be evaluated as information becomes available.

4.1.4 THE NEW ADDITIONAL TERM π_M

The complexity factors for standard integrated circuits are based on circuits using single-layer metallization and 14-lead packages. However, for most complex circuits in the MSI and LSI category, multi-level metallization is required to provide the associated intraconnections. Presently, multilevel metallization is a potential trouble area for complex circuits as reported in the literature[6] and as predicted by the expected failure mode distribution (see Table II). To account for this in the model, π_M is provided which considers the contribution to the failure rate for the increased number of layers of metallization in addition to the first level. The term is determined in the following manner:

$$\pi_{M_x} = \frac{\sum M}{\lambda_b}$$

where:

π_M is the metallization factor at the temperature (x) under consideration,

M = .0023%/1000 hours (for each layer),

λ_b is the base failure rate (see Figure 1) at temperature x.

For each layer of metallization add .0023%/1000 hours*. This number

*Note: The increased metallization of the complex circuit may cause this figure to be altered.

w_{ps} empirically derived using the expected percent contributions in the predicted failure mode distribution (Table II) along with failure rate data on standard integrated circuits[3]. This is based on an average chip area of 2,500 sq. mils. It is expected that future complex microcircuits will approximately utilize the following chip areas:

SSI	6,000 sq. mils.
MSI	8,000 sq. mils.
LSI	10,000 sq. mils. or greater

5.0 BASE FAILURE RATE

The remaining item in the model, the base failure rate, λ_b, will be considered over the temperature range of 25°C to 125°C, with no electrical stress applied. This is the same curve that is presented in the RADC Reliability Notebook, Vol II[5].

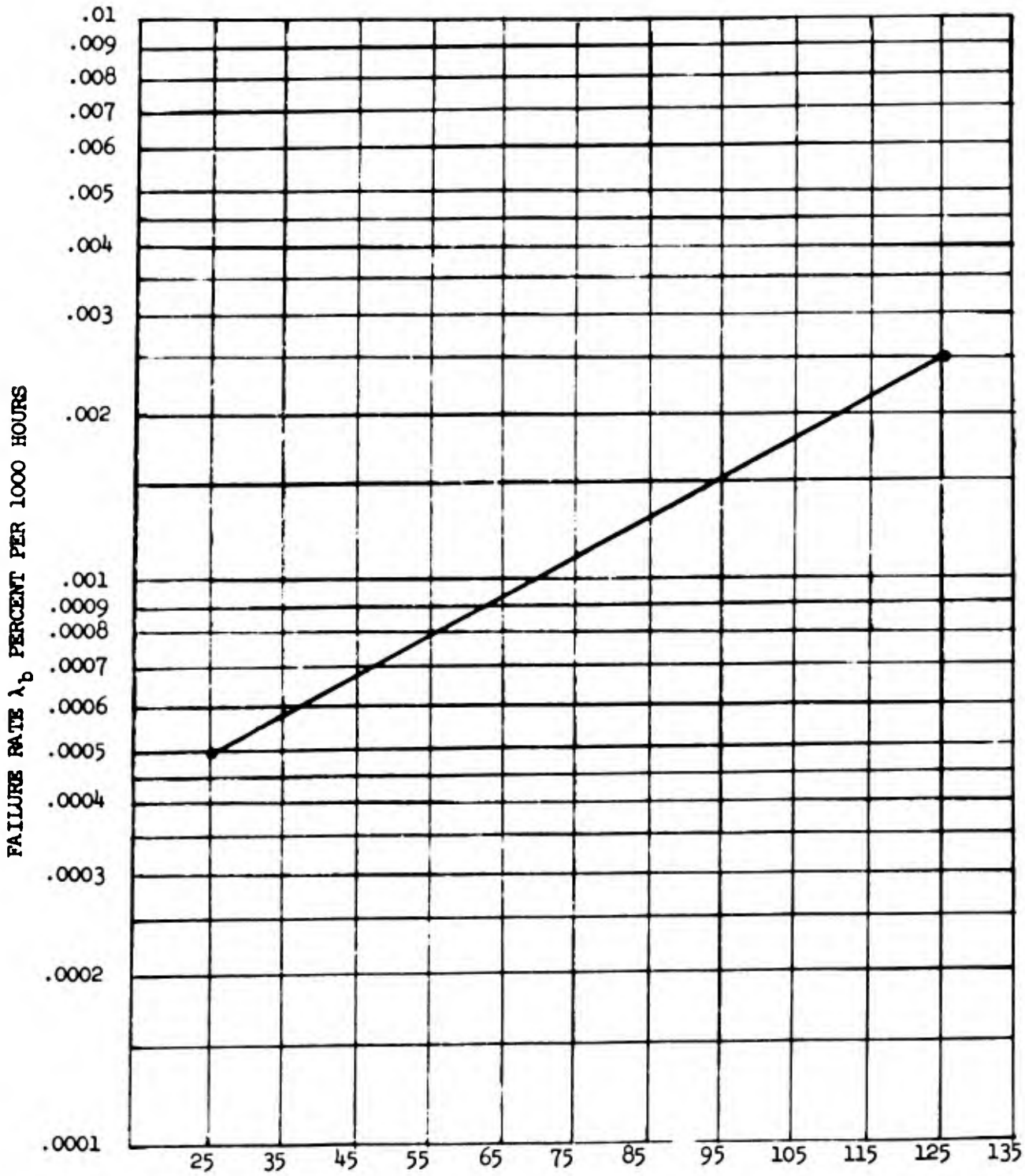
The "law" of thermal degradation should hold for all circuits regardless of complexity. Therefore, the Arrhenius Model which has been shown to be appropriate for use with integrated circuits will also be used as the basis for the failure rates of complex microcircuits. This base failure rate must be multiplied by the various adjustment factors given in this report to arrive at λ_{MC} which is typical of the complex microcircuits in actual use.

Later it may prove out that different approaches to LSI (i.e. discretionary wiring, 100% yield, and cell approaches) or that specific processing may result in different λ_b curves.

The predicted optimum failure rates for the existing complex microcircuits are presented in Appendix B.

FIGURE 1

5.1 MICROCIRCUITS BASE FAILURE RATE*



* Zero Stress

6.0 PREDICTED OPTIMUM FAILURE RATES FOR COMPLEX MICROCIRCUITS

Using the base failure rate curve given in Figure 1, along with the adjustments and additional factors as presented in Appendix C, the optimum failure rates for present complex microcircuits can be predicted using the new model. These failure rates are presented in Table VII and the associated calculations are presented in Appendix C.

TABLE VII

OPTIMUM FAILURE RATES FOR STANDARD AND COMPLEX MICROCIRCUITS

AT 25° and 125°C IN %/1000 HOURS

TEMPERATURE	STANDARD	SSI	MSI	LSI
25°C	0.001	0.008	0.012	0.020
125°C	0.005	0.030	0.044	0.073

The standard microcircuit is considered to have 14 leads and only one layer of metallization.

The SSI circuits are considered to also have a single layer of metallization but utilize a 20-lead package. The packaging factor π_{P_C} is 2.2, π_C is 5, and $\sum_M$ equals .0023.

The failure rate for MSI circuitry is based on two layers of metallization and 30 leads. The packaging factor π_{P_C} is 2.6, π_C is 6, and $\sum_M$ is .0046.

The LSI failure rate prediction is based on devices using three layers of metallization and 60 leads. The packaging factor π_{P_C} is 3.8, π_C is 7, and $\sum_M$ is .0069.

7.0 COMPARISON OF OPTIMUM FAILURE RATES OF COMPLEX CIRCUITS VERSUS THEIR EQUIVALENT IN STANDARD ICs

The standard IC gate will serve as the basis for this prediction. The projected failure rates for complex circuits will be compared to the failure rate of an equivalent number of standard IC gates. It is assumed that the failure rate of the equivalent number of basic gates, corresponding to a single complex circuit, will be a direct multiple of the number of gates times the failure rate of the standard circuit basic gate. The comparisons are now given in Table VIII.

TABLE VIII

COMPARISON OF OPTIMUM FAILURE RATES OF COMPLEX MICROCIRCUITS VERSUS THEIR EQUIVALENT IN STANDARD CIRCUITS AT 25°C

COMPLEXITY	NUMBER OF GATES	FAILURE RATE %/1000 HOURS	APPLICATION IMPROVEMENT FACTOR
Standard IC	1	0.001	
	32	0.032	
	64	0.064	
	128	0.128	
SSI	32	0.008	4
MSI	64	0.012	5.3
LSI	128	0.020	6.4

These improvement factors do not reflect the total improvement in system reliability or design. For example, the number of interconnections eliminated in system fabrication is not considered. However, these factors appear to be realistic and do reflect the actual improvement rate in processing and the results of reliability physics studies in reducing the contributions of certain failure mechanisms. Proponents of complex microcircuits are predicting a 10:1 improvement in overall system reliability[7].

8.0 CONCLUSIONS

Complex microcircuits promise improved reliability, increased performance, reductions in size, and lower costs per function. There are many different approaches to complex circuit fabrication being investigated. Some devices with two layers of metallization are already on the market. At the time of this writing two vendors currently have in production 96- and 120-gate TTL bipolar arrays, respectively. Another vendor has delivered TTL bipolar arrays with 174 equivalent gates interconnected with three layers of metallization and claims he can deliver similar customized arrays on a two-months notice[8]. In line with these developments, this report provides a preliminary approach for assessing the associated reliability problems. The adjustment factors and predictions presented in this report are to serve as interim guidelines. As more information becomes available these figures will be modified or the model changed to reflect state-of-the-art developments.

APPENDIX A

PREDICTED FAILURE MODE DISTRIBUTIONS FOR COMPLEX CIRCUITS

Using the multipliers listed in Table II, the predicted failure mode distributions for the following commercially available complex circuits were determined:

1. Decade Counter - 14 pins - 46 gates
2. Binary Counter - 14 pins - 45 gates
3. BCD-to-Decimal Decoder - 16 pins - 9 gates
4. 2 Bit Binary Full Adder - 14 pins - 18 gates
5. 4 Bit Binary Full Adder - 16 pins - 36 gates
6. Divide-by-Twelve Counter - 14 pins - 33 gates
7. 4 Bit Binary Counter - 14 pins - 33 gates

The predicted failure mode distributions for these complex microcircuits are listed in Table A-1, and the predicted optimum failure rates are presented in Appendix B.

PREDICTED FAILURE MODE DISTRIBUTIONS FOR COMPLEX MICROCIRCUITS

TABLE A-1

FAILURE MODE / CIRCUIT	1	2	3	4	5	6	7
METALLIZATION	39.64%	39.64%	33.17%	37.32%	38.96%	39.05%	39.05%
HERMETICITY	1.07%	1.09%	5.21%	2.58%	1.53%	1.47%	1.47%
BONDS	1.96%	2.00%	9.87%	4.70%	2.90%	2.68%	2.68%
PHOTOLITHOGRAPHIC DEFECTS	29.44%	29.37%	24.58%	27.66%	28.86%	28.93%	28.93%
CONTACT CUT RESISTANCE	19.74%	19.74%	16.52%	18.59%	19.40%	19.45%	19.45%
WIRE DEFECTS	.53%	.54%	2.54%	1.25%	.74%	.72%	.72%
CHANNELING	7.12%	7.10%	5.95%	6.68%	6.98%	7.00%	7.00%
FOREIGN MATERIAL	.36%	.37%	1.54%	.87%	.45%	.50%	.50%
MISCELLANEOUS	.14%	.15%	.62%	.35%	.18%	.20%	.20%
TOTAL	100%	100%	100%	100%	100%	100%	100%

APPENDIX B

OPTIMUM FAILURE RATES FOR EXISTING COMPLEX FUNCTION INTEGRATED CIRCUITS

(Failure Rates in %/1000 Hours @ 25°C)

CIRCUIT	NO. OF GATES	NO. OF PINS	π_M	π_C	π_{P_C}	π_Q and π_E	λ_b	$\lambda_{MC_{25°}}$
1	46	14	$\frac{.0023}{.0005}$	6	2.0	1	.0005	.0083%/ 1000 Hrs
2	45	14	"	6	2.0	"	"	.0083%/ 1000 Hrs
3	9	16	"	4	2.1	"	"	.0065%/ 1000 Hrs
4	18	14	"	5	2.0	"	"	.0073%/ 1000 Hrs
5	36	16	"	6	2.1	"	"	.0085%/ 1000 Hrs
6	33	14	"	6	2	"	"	.0083%/ 1000 Hrs
7	33	14	"	6	2	"	"	.0083%/ 1000 Hrs

$$\pi_{M_x} = \frac{\sum M}{\lambda_b}$$

$$\lambda_{MC_x} = \lambda_b \left[(\pi_{P_C} \pi_Q \pi_C \pi_E) + \pi_{M_x} \right]$$

APPENDIX C

CALCULATION OF OPTIMUM FAILURE RATES FOR STANDARD AND COMPLEX MICROCIRCUITS

The base failure rates at 25°C and 125°C for a basic single gate as given in RADC Reliability Notebook and Figure 1 are:

$$\lambda_{b_{25^\circ C}} = 0.0005\%/1000 \text{ Hours}$$

$$\lambda_{b_{125^\circ C}} = 0.0025\%/1000 \text{ Hours}$$

The values of the adjustment factors are:

$$\pi_C = 1$$

$$\pi_P = 2$$

$$\pi_E = 1$$

$$\pi_Q = 1$$

Using the standard microcircuit prediction model:

$$\lambda_M = \lambda_b \pi_C \pi_P \pi_Q \pi_E$$

We obtain the optimum failure rates at 25°C and 125°C:

$$\lambda_{M_{25^\circ C}} = (0.0005\%/1000 \text{ Hours}) \cdot (2)$$

$$\lambda_{M_{25^\circ C}} = 0.001\%/1000 \text{ Hours}$$

$$\lambda_{M_{125^\circ C}} = (0.0025\%/1000 \text{ Hours}) \cdot (2)$$

$$\lambda_{M_{125^\circ C}} = 0.005\%/1000 \text{ Hours}$$

Appendix C, Cont'd

CALCULATION OF OPTIMUM FAILURE RATES FOR SSI CIRCUIT ARRAYS

The base failure rates are, again:

$$\lambda_{b_{25^\circ C}} = 0.0005\%/1000 \text{ Hours}$$

$$\lambda_{b_{125^\circ C}} = 0.0025\%/1000 \text{ Hours}$$

$$\pi_C = 5$$

$$\pi_{P_C} = 2.2$$

$$\pi_E = 1$$

$$\pi_Q = 1$$

$$\pi_{M_{25^\circ C}} = \frac{0.0023\%/1000 \text{ Hours}}{0.0005\%/1000 \text{ Hours}}$$

$$\pi_{M_{125^\circ C}} = \frac{0.0023\%/1000 \text{ Hours}}{0.0025\%/1000 \text{ Hours}}$$

Using the postulated complex microcircuit prediction model:

$$\lambda_{SSI} = \lambda_b \left[(\pi_{P_C} \pi_C \pi_Q \pi_E) + \pi_M \right]$$

We obtain the optimum failure rates at 25°C and 125°C.

$$\lambda_{SSI_{25^\circ C}} = 0.0005 \left[(2.2)\ (5) + \frac{0.0023}{0.0005} \right]$$

$$\lambda_{SSI_{25^\circ C}} = 0.008\%/1000 \text{ Hours}$$

$$\lambda_{SSI_{125^\circ C}} = .0025\%/1000 \text{ Hours} \left[(2.2)\ (5) + \frac{0.0023}{0.0025} \right]$$

$$\lambda_{SSI_{125^\circ C}} = 0.03\%/1000 \text{ Hours}$$

Appendix C, Cont'd

CALCULATION OF OPTIMUM FAILURE RATES FOR MSI CIRCUIT ARRAYS

The base failure rates are, again:

$\lambda_{b_{25^\circ C}}$ = 0.0005%/1000 Hours

$\lambda_{b_{125^\circ C}}$ = 0.0025%/1000 Hours

The values of the adjustment factors are:

$\pi_C = 6$

$\pi_{P_C} = 2.6$

$\pi_E = 1$

$\pi_Q = 1$

$$\pi_{M_{25^\circ C}} = \frac{0.0046\%/1000 \text{ Hours}}{0.0005\%/1000 \text{ Hours}}$$

$$\pi_{M_{125^\circ C}} = \frac{0.0046\%/1000 \text{ Hours}}{0.0025\%/1000 \text{ Hours}}$$

Using the complex microcircuit model.

$$\lambda_{MSI} = \lambda_b \left[(\pi_{P_C} \pi_C \pi_Q \pi_E) + \pi_M\right]$$

We obtain the optimum failure rates at 25°C and 125°C.

$$\lambda_{MSI_{25^\circ C}} = 0.0005 \left[(2.6)(6) + \frac{0.0046}{0.0005}\right]$$

$\lambda_{MSI_{25^\circ C}}$ = 0.012%/1000 Hours

$$\lambda_{MSI_{125^\circ C}} = 0.0025 \left[(2.6)(6) + \frac{0.0046}{0.0025}\right]$$

$\lambda_{MSI_{125^\circ C}}$ = 0.044%/1000 Hours

Appendix C, Cont'd

CALCULATION OF OPTIMUM FAILURE RATES FOR LSI CIRCUIT ARRAYS

The base failures are, again:

$\lambda_{b_{25^\circ C}}$ = 0.0005%/1000 Hours

$\lambda_{b_{125^\circ C}}$ = 0.0025%/1000 Hours

The values of the adjustment factors are:

$\pi_C = 7$

$\pi_{P_C} = 3.8$

$\pi_Q = 1$

$\pi_E = 1$

$\pi_{M_{25^\circ C}} = \frac{0.0069\%/1000 \text{ Hours}}{0.0005\%/1000 \text{ Hours}}$

$\pi_{M_{125^\circ C}} = \frac{0.0069\%/1000 \text{ Hours}}{0.0025\%/1000 \text{ Hours}}$

Using the complex microcircuit prediction model:

$$\lambda_{LSI} = \lambda_b \left[(\pi_{P_C} \pi_C \pi_Q \pi_E) + \pi_M\right]$$

We obtain the optimum failure rates at 25°C and 125°C:

$$\lambda_{LSI_{25^\circ C}} = 0.0005 \left[(3.8)\ (7) + \frac{0.0069}{0.0005}\right]$$

$\lambda_{LSI_{25^\circ C}}$ = 0.02%/1000 Hours

$$\lambda_{LSI_{125^\circ C}} = 0.0025 \left[(3.8)\ (7) + \frac{0.0069}{0.0025}\right]$$

$\lambda_{LSI_{125^\circ C}}$ = 0.073%/1000 Hours

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UNCLASSIFIED
Security Classification

DOCUMENT CONTROL DATA - R & D

(Security classification of title, body of abstract and indexing annotation must be entered when the overall report is classified)

1 ORIGINATING ACTIVITY (Corporate author)	2a. REPORT SECURITY CLASSIFICATION
Rome Air Development Center (EMNRR/Mr. Peter Manno) Griffiss AFB NY 13440	Unclassified
	2b. GROUP

3 REPORT TITLE

FAILURE RATE PREDICTION FOR COMPLEX BIPOLAR MICROCIRCUITS

4 DESCRIPTIVE NOTES *(Type of report and inclusive dates)*

Technical Report (May 1968 - May 1969) In-house

5 AUTHOR(S) *(First name, middle initial, last name)*

Peter F. Manno

6 REPORT DATE	7a. TOTAL NO OF PAGES	7b. NO OF REFS
October 1969	34	8

8a. CONTRACT OR GRANT NO	9a. ORIGINATOR'S REPORT NUMBER(S)
b. PROJECT NO 5519 Task No. 551902 d.	RADC-TR-69-350
	9b. OTHER REPORT NO(S) *(Any other numbers that may be assigned this report)*

10 DISTRIBUTION STATEMENT

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11 SUPPLEMENTARY NOTES	12 SPONSORING MILITARY ACTIVITY
	Rome Air Development Center (EMNRR) Griffiss Air Force Base, New York 13440.

13 ABSTRACT

The intent of this report is to provide a reliability prediction technique for complex bipolar microcircuits, commonly referred to as small-, medium-, and large-scale integration. Failure mode distributions for complex microcircuits are projected from failure mode data on standard integrated circuits. This is done by the use of failure mode multipliers which are determined by linear extrapolations from a representative breakdown of composite industry-wide failure mode data on current state-of-the-art integrated circuits.

The RADC failure rate prediction model for standard integrated circuits is extended to cover these new complex circuits. To achieve this, an additional term, to account for the variations in processing and fabrication of complex microcircuit arrays, is introduced into the standard model along with the standard multipliers (which have been extended or altered) according to the number of gates, packaging configuration, and increased silicon chip area. The base failure rate for standard circuits will also be used as the basis of the new prediction technique. Optimum failure rates are calculated for some typical complex circuits and compared to the failure rate of their discrete integrated circuit equivalent.

DD FORM 1 NOV 68 1473

UNCLASSIFIED
Security Classification

14 KEY WORDS	LINK A		LINK B		LINK C	
	ROLE	WT	ROLE	WT	ROLE	WT
Reliability Large Scale Integration (LSI) Failure Modes						

AFLC—Griffiss AFB NY