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RADC-TR-68-339, Volume II
Final Report

DEVELOPMENT AND IMPLEMENTATION OF A RELIABILITY ANALYSIS CENTER

Volume II, Sections 8-10

G. T. Jacobi
H. A. Lauffenburger
P. A. Llewellen
et al

IIT Research Institute

TECHNICAL REPORT NO. RADC-TR-68-339
October 1968

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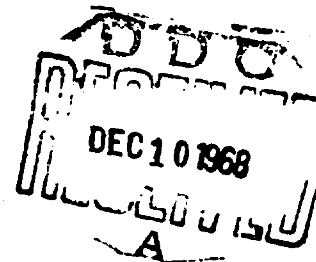

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8.0 STRUCTURED TERM LIST

The structured term list has the terms grouped into logical categories. The arrangement of the terms into categories is equivalent to including roles in the vocabulary. The majority of the terms in this list are applicable to only one category. However, certain terms, identified by having the Termatrex card code printed to the right of the term, are applicable to more than one category; for example, Compound Formation SDI (02). Reference to the alphabetical listing shows this term can be interpreted as part of Subsection 8.6, Failure Analysis Studies, or as part of Subsection 8.5, Microelectronic Design and Development.

a) 8.6 P.O. Failure Phenomena SDI (78)

P.O. Failure Analysis Studies PI (00)

b) 8.5 P.O. Chemical Phenomena SDI (01)

P.O. Circuit/Device Theory SDI (00)

Unqualified Terms (page 28) are terms which may be related to many categories. These are to be indexed whenever any of the qualified forms of the terms are indexed <u>or</u> whenever no further qualifications of the concept is given in the document.

Asterisk (*) terms are not represented by Termatrex cards. Digit Codes have been set up for Manufacturer's names (page 6), Part Numbers (page 9), Report Dates (page 29), Device Manufacturers (page 30), and Device User (page 32).

8.1 Generic Class Descriptors

Red I

Microelectronic Category*

RDI(00) Composite IC, NOC (Synonyms: Compatible Monolithic*, Monobrid*, Active Substrate IC*)

RDI(01) Composite IC, Diffused

RDI(02) Composite IC, Epitaxial

RDI(03) Hybrid Microcircuit (Synonyms: Hybrid Integrated Circuit*)

RDI(04) Monolithic, Diffused

RDI(05) Monolithic, Epitaxial

RDI(06) Monolithic IGFET (MOS, MNS, MTOS, SOS)

RDI(07) Monolithic, NOC (Not otherwise classified. Synonyms: Mono*, Fully IC*, Semiconductor IC*)

RDI(08) Multichip Microcircuit (Synonyms: Multichip Hybrid IC*)

RDI(09) Thick Film - Pure IC (Synonyms: Passive Substrate IC*)

RDI(10) Thin Film - Pure IC (Synonyms: TFIC*, Passive Substrate IC*)

Functional Category*

RDI(11) Digital

RDI(12) Linear (Analog*)

* Term not represented by a Termatrex card.

Package Configuration*

RDI(52) Can, Hermetically Sealed

RDI(53) Dual In-Line, Hermetically Sealed

RDI(54) Dual In-Line, Plastic (DIP)

RDI(55) Flat Pack, Ceramic

RDI(56) Flat Pack, Glass

RDI(57) Module

RDI(58) Plastic Encapsulated (Non-DIP Plastic Cap)

Operational Type*

RDI(13) (Digital Logic)

- RDI(14) CML (ECL*, ECCSL*, MECL*)
- RDI(15) CTL
- RDI(16) DCTL
- RDI(17) DTL
- RDI(18) MOSTL
- RDI(19) RCTL
- RDI(20) RTL
- RDI(21) TTL (T^2L*)
- RDI(22) Digital Logic NOC

RDI(23) (Linear Device)

- RDI(24) Differential
- RDI(25) Single Ended
- RDI(86) Linear Device NOC

Qualification Class*

RDI(59) Consumer

RDI(60) High Reliability Certification (Hi-Rel Certification)

RDI(61) Industrial/Commercial

RDI(62) Military

RDI(63) Military Upgraded

RDI(26) Interconnection System

RDI(27) Aluminum-to-Aluminum, Direct

RDI(28) Aluminum-to-Aluminum, Wire bond

RDI(29) Gold-to-Aluminum, Direct

RDI(30) Gold-to-Aluminum, Wire bond

RDI(31) Gold-to-Gold, Direct (Gold-to-Gold, inverted chip; Gold-to-Gold, flip chip

RDI(32) Gold-to-Gold, Wire bond

RDI(33) Gold-to-Silicon-to-Aluminum, Wire bond

RDI(34) Isolation Method

RDI(35) Dielectric, Air (Beam Lead*)

RDI(36) Dielectric, Ceramic

RDI(37) Dielectric, Glass

RDI(38) Dielectric, Nitride

RDI(39) Dielectric, Oxide

RDI(40) Dielectric, NOC

RDI(41) Junction

RDI(42) Resistive

Circuit Complexity*

RDI(43) Arithmetic Functional Unit

RDI(44) Audio Amp

RDI(45) Differential Amplifier

RDI(46) Cate (Logic Gate)

RDI(47) Multivibrator

RDI(48) RF-IF Amp

RDI(49) Storage Element

RDI(50) Video (wideband) Amp

RDI(51) Special NOC

8.2 Manufacturer Descriptor

Manufacturer

DIGIT CODE

Tens	Units
RDI (83) 0-	RDI (64) -0
RDI (74) 1-	RDI (65) -1
RDI (75) 2-	RDI (66) -2
RDI (76) 3-	RDI (67) -3
RDI (77) 4-	RDI (68) -4
RDI (78) 5-	RDI (69) -5
RDI (79) 6-	RDI (70) -6
RDI (80) 7-	RDI (71) -7
RDI (81) 8-	RDI (72) -8
RDI (82) 9-	RDI (73) -9

Code	Manufacturer
RDI (83) RDI (65)	Amelco Semiconductor (1)
RDI (83) RDI (66)	Amperex Electronic Corp. (2)
RDI (83) RDI (67)	Bunker-Ramo Corp. (3)
RDI (83) RDI (68)	Fairchild Semiconductor (4)
RDI (83) RDI (69)	General Instrument Corp. (5)
RDI (83) RDI (70)	ITT Semiconductor (6)
RDI (83) RDI (71)	Motorola Semiconductor Products, Inc. (7)
RDI (83) RDI (72)	National Semiconductor Corp. (8)

Manufacturer (cont'd)

RDI (83) Philco-Ford Corp. (9)
RDI (73)

Philco-Ford Bipolar IC's

Philco-Ford MOS IC's

RDI (74) Radiation, Inc. (10)
RDI (64)

RDI (74) Radio Corporation of America (11)
RDI (65)

RDI (74) Raytheon Company (12)
RDI (66)

RDI (74) Signetics Corp. (13)
RDI (67)

RDI (74) Siliconix, Inc. (14)
RDI (68)

RDI (74) Sperry Semiconductor (15)
RDI (69)

RDI (74) Sprague Electric Co. (16)
RDI (70)

RDI (74) Sylvania Electric Products, Inc. (17)
RDI (71)

RDI (74) Texas Instruments Incorporated (18)
RDI (72)

RDI (74) Transitron Electronic Corp. (19)
RDI (73)

RDI (75) Union Carbide Electronics (20)

RDI (75) Westinghouse Electric Corp. (21)
RDI (65)

GYI(79) <u>Manufacturing Date</u>

GYI(62) 1962

GYI(63) 1963

GYI(64) 1964

GYI(65) 1965

GYI(66) 1966

GYI(73) January - June

GYI(74) July - December

GYI(67) 1967

GYI(68) 1968

GYI(69) 1969

GYI(70) 1970

GYI(71) 1971

GYI(72) 1972

GYI(75) January - March

GYI(76) April - June

GYI(77) July - September

GYI(78) October - December

Part Numbers

Part Number Code	Termatrex Card Numbers
Thousand	
0---	WI (62)
1---	WI (63)
Hundred	
-0--	WI (64)
-1--	WI (65)
-2--	WI (66)
-3--	WI (67)
-4--	WI (68)
-5--	WI (69)
-6--	WI (70)
-7--	WI (71)
-8--	WI (72)
-9--	WI (73)
Tens	
--0-	WI (40)
--1-	WI (41)
--2-	WI (42)
--3-	WI (43)
--4-	WI (44)
--5-	WI (45)
--6-	WI (46)
--7-	WI (47)
--8-	WI (48)
--9-	WI (49)
Units	
---0	WI (90)
---1	WI (91)
---2	WI (92)
---3	WI (93)
---4	WI (94)
---5	WI (95)
---6	WI (96)
---7	WI (97)
---8	WI (98)
---9	WI (99)

8.3 Item Descriptors (Terms which describe a microelectronic device or device element.)

Black I

Electrical Properties*

Output Impedance (Typical)

BKI(00) Less than 10 K Ohms

BKI(01) 10 K thru 100 K Ohms

BKI(02) Greater than 100 K Ohms

Maximum Fan-Out (Rating per equivalent gate circuit)

BKI(03) Less than 5

BKI(04) 5 thru 10

BKI(05) Excess of 10

Maximum Frequency of Operation

BKI(06) Less than 10 Hz

BKI(07) 10 Hz to less than 10 kHz

BKI(08) 10 kHz to less than 10 MHz

BKI(09) 10 MHz to less than 300 MHz

BKI(10) 300 MHz to 300 GHz

BKI(11) Greater than 300 GHz

Maximum Power Dissipation (per equivalent circuit input)(gate)

BKI(12) Less than 10 mw

BKI(13) 10 thru 30 mw

BKI(14) Greater than 30 mw

Electrical Properties* (cont')

Propagation Delay (Maximum)

- BKI(15) Less than 10 Nanoseconds
- BKI(16) 10 thru 30 Nanoseconds
- BKI(17) Greater than 30 Nanoseconds

Gain (Typical)

- BKI(18) Less than 40 db
- BKI(19) 40 thru 80 db
- BKI(20) Greater than 80 db

Maximum Output Power

- BKI(21) Less than 10 mw
- BKI(22) 10 thru 100 mw
- BKI(23) 101 mw thru 1 Watt
- BKI(24) Greater than 1 Watt

Environmental Capabilities*

Maximum Operating Temperature

- BKI(25) ≥202.5°C
- BKI(26) 172.5°C to <202.5°C
- BKI(27) 152.5°C to <172.5°C
- BKI(28) 102.5°C to <152.5°C
- BKI(29) <102.5°C

Environmental Capabilities* (cont')

Minimum Operating Temperature

BKI(30) ≥-42.5°C

BKI(31) -62.5°C to <-42.5°C

BKI(32) -82.5°C to <-62.5°C

BKI(33) <-82.5°C

Maximum Storage Temperature

BKI(34) ≥302.5°C

BKI(35) 252.5°C to <302.5°C

BKI(36) 202.5°C to <252.5°C

BKI(37) 152.5°C to <202.5°C

BKI(38) 102.5°C to <152.5°C

BKI(39) <102.5°C

Minimum Storage Temperature

BKI(40) ≥-42.5°C

BKI(41) -62.5°C to <-42.5°C

BKI(42) -82.5°C to <-62.5°C

BKI(43) -102.5°C to <-82.5°C

BKI(44) <-102.5°C

Reliability Rating (Max. Failure Rate)

BKI(45) Less than 0.001% per 1000 hours

BKI(46) 0.001% to less than 0.01% per 1000 hours

BKI(47) 0.01% to less than 0.1% per 1000 hours

BKI(48) Greater than 0.1% per 1000 hours

BKI (49) Circuit Functions

BKI (50) A/D Converter

BKI (51) Adders

BKI (52) AND Gate (AND/OR Gate*)

BKI (53) Astable Multivibrators

Audio Amplifier RDI (44)

BKI (54) Bistable Multivibrators (flip-flops*)

BKI (55) Counters

BKI (56) D/A Converter

Differential Amplifier RDI (45)

BKI (57) Gate Expanders

BKI (58) IF Amplifier

BKI (71) Inverter

BKI (59) Magnetic Film Storage Elements

BKI (60) Molecular Electronic Function

BKI (61) Monostable Multivibrators

BKI (62) NAND Gate (NAND/NOR Gate*)

BKI (63) NOR Gate (NOR/NAND Gate*)

BKI (64) Operational Amplifier

BKI (65) OR Gate (OR/AND Gate*)

BKI (66) Power Amplifier

BKI (67) RF Amplifier

Circuit Functions (cont')

BKI(68) Servo Amplifier

BKI(69) Superconducting Storage Elements

Video Amplifier RDI(50)

BKI(70) Voltage Regulator

Special NOC RDI(51)

Scale of Integration*

BKI(83) LSI

BKI(84) MSI

BKI(85) SSI

Number of Major Process Steps*

BKI(73) 3

BKI(74) 4

BKI(75) 5

BKI(76) 6

BKI(77) 7

BKI(78) 8

BKI(79) 9

BKI(80) 10

BKI(81) 11

BKI(82) 12

BKI(72) Other

MEL Device Element Descriptor*

- GNI(00) Circuit Component
  - GNI(01) PNPN Devices
    - GNI(02) DIAC
    - GNI(03) GTO
    - GNI(04) LASCR
    - GNI(05) SCR
    - GNI(06) SCS
    - GNI(07) Shockley 4-Layer Diode
    - GNI(08) TRIAC
  - GNI(09) Transistors
    - GNI(10) Bipolar
    - GNI(11) Complementary
    - GNI(12) FET
      - GNI(13) IGFET
        - GNI(14) N-Channel IGFET
        - GNI(15) P-Channel IGFET
        - GNI(28) MOS
        - GNI(46) MNS
        - GNI(47) MTOS
        - GNI(81) SOS
        - GNI(82) Thin Film
      - GNI(16) JFET

Mel Device Element Descriptor* (cont')

Circuit Component (cont')

Transistors (cont')

GNI(17) Multiple Emitter

GNI(18) NPN

GNI(19) PNP

GNI(20) PNP Lateral

GNI(21) Power

GNI(22) Small Signal

GNI(23) Unijunction

GNI(24) Capacitors

GNI(25) Diffused Junction

GNI(26) Discrete Capacitor

GNI(27) Film

GNI(28) MOS

GNI(29) Variable

GNI(30) Diode

GNI(31) Avalanche Diode

GNI(32) General Purpose Diode-Junction

GNI(33) Gunn Effect Diode

GNI(34) Micro-Diode-Discrete

GNI(35) Schottkey Barrier Diode

Mel Device Element Descriptor* (cont')

- Circuit Component (cont')
  - Diode (cont')
    - GNI(36) Tunnel Diode
      - Voltage Regulator BKI(70)
  - GNI(37) Distributed Passive Devices
    - GNI(38) Strip Line Filters
    - GNI(39) Terminators
  - GNI(40) Inductor
      - Film GNI(27)
    - GNI(41) Simulated (i.e. Gyrator)
  - GNI(42) Resistors
    - GNI(43) Diffused Resistor
    - GNI(44) Discrete Resistor
      - Film GNI(27)
      - Variable GNI(29)
  - GNI(48) Special Active Devices NOC
    - GNI(49) Acoustical Transducer
    - GNI(50) Cryotron
    - GNI(51) Resonant Gate FET
  - GNI(52) Discrete Microcomponent

MEL Device Element Descriptor* (cont')

Circuit Component Regions*

GNI(53) Alloy Junction

GNI(54) Anode

GNI(55) Base

GNI(56) Buried Layer

GNI(57) Cathode

GNI(58) Channel

GNI(59) Collector

GNI(60) Contact Area

GNI(61) Crossover

Diffused Junction GNI(25)

GNI(63) Drain

GNI(64) Electrodes

GNI(65) Emitter

GNI(66) Epitaxial Junction

GNI(67) Epitaxial Layer

GNI(68) Gate (IGFET Type)

GNI(69) Isolation Region

GNI(70) Planar Junction

GNI(71) Source (FET)

GNI(72) Terminals

Mel Device Element Descriptor* (cont')

Die Size

GNI(73)	<30 mils/side (<900 sq. mils)
GNI(74)	31-42 mils/side (900-1800 sq. mils)
GNI(75)	43-60 mils/side (1800-3600 sq. mils)
GNI(76)	61-85 mils/side (3600-7200 sq. mils)
GNI(77)	86-120 mils/side (7200-14,400 sq. mils)
GNI(78)	121-170 mils/side (14,400-28,800 sq. mils)
GNI(79)	171-240 mils/side (28,800-57,680 sq. mils)
GNI(80)	>240 mils/side (>57,680 sq. mils)

BK II (26) Device Element Materials

Functional Elements*

BK II (00) Circuit Metallization Materials

BK II (01) Aluminum

BK II (02) Chromium

BK II (03) Copper

BK II (04) Gold

BK II (05) Nickel

BK II (06) Silver

BK II (07) Circuit Metallization Materials NOC

BK II (08) Dielectrics and Insulating Materials

BK II (09) Air

Alumina BK II (47)

BK II (11) Hafnium Dioxide

BK II (12) Silicon Carbide

Silicon Nitride BK II (55)

Silicon Oxide (SiO or SiO_2) BK II (56)

BK II (15) Tantalum Oxide

BK II (16) Titanium Dioxide

BK II (17) Dielectrics and Insulating Materials NOC

Device Element Materials (cont')

Functional Elements* (cont')

BK II (18) Dopant Materials

BK II (19) Aluminum

BK II (20) Antimony

BK II (21) Arsenic

BK II (22) Boron

BK II (10) Gallium

BK II (23) Gold

BK II (24) Phosphorous

BK II (25) Dopant Materials NOC

BK II (27) Wire Material

BK II (28) Aluminum

BK II (29) Gold

BK II (30) Wire Material NOC

BK II (13) Materials NOC

BK II (31) Cermets and Glazes (all compositions)

BK II (32) II-VI Compounds (BeO, MgO, ZnO, BaO, HgS, BaS, ZnS, CdS, CdSe, ZnSe, BaSe, HgSe, CdTe, ZnTe, BaTe, HgTe)

BK II (33) III-V Compounds (BN, BP, AlAs, AlSb, GaN. GaP. GaAs, GaSb, InP, InAs, InSb)

BK II (34) IV-VI Compounds (SiO, SiO_2, TiO_2, ZrO_2, SnO_2, HfO_2, PbO, PbS. PbSe, PbTe)

Device Element Materials (cont')

Functional Elements* (cont')

Materials NOC (cont')

BK II (35) IV-IV Compounds (Silicon Carbide)

BK II (98) III-VI Compounds (Al_2O_3, Ga_2O_3, In_2O_3)

BK II (36) Ferrites

BK II (14) Hafnium

BK II (37) Ferroelectrics

BK II (38) Indium

BK II (39) Iron

BK II (40) Lead

BK II (41) Molybdenum

BK II (42) Nichrome (alloy)

BK II (43) Platinum

BK II (44) Tantalum

BK II (45) Tin

BK II (13) Materials NOC

Non Functional Elements*

BK II (46) Substrate Materials

BK II (47) Alumina

BK II (48) Ceramics

BK II (49) Germanium

Glass RDI (89)

BK II (50) Sapphire

BK II (51) Silicon

BK II (52) Substrate Materials NOC

Device Element Materials (cont')

Non Functional Elements* (cont')

BK II (53) Surface Protection

Glass RDI(89)

BK II (55) Silicon Nitride

BK II (56) Silicon Oxide (SiO or SiO_2)

BK II (57) Passivated NOC

BK II (58) Die Bond Material

BK II (59) Glass Frit

BK II (60) Gold Germanium Eutectic

BK II (61) Gold Silicon Eutectic

Solder GNI(96)

BK II (63) Die Bond Material NOC

BK II (64) Package Terminal Material

BK II (65) Aluminum

BK II (66) Copper

BK II (67) Gold

BK II (68) Kovar

BK II (69) Package Terminal Material NOC

Device Element Materials (cont')

Non Functional Elements* (cont')

RDI(87) Package Material (Primary)

RDI(88) Ceramics

RDI(89) Glass

RDI(90) Metal

RDI(91) Plastic, Silicon Resin

RDI(92) Plastic, NOC

BK II (81) Package Type

BK II (82) TO-5

BK II (70) TO-70

BK II (71) TO-71

BK II (72) TO-72

BK II (73) TO-73

BK II (74) TO-74

BK II (75) TO-75

BK II (76) TO-76

BK II (77) TO-77

BK II (78) TO-78

BK II (79) TO-79

BK II (80) TO-80

BK II (84) TO-84

BK II (85) TO-85

Package Type (cont')

BK II (86) TO-86

BK II (87) TO-87

BK II (88) TO-88

BK II (89) TO-89

BK II (90) TO-90

BK II (91) TO-91

BK II (95) TO-95

BK II (96) TO-96

BK II (99) TO-99

BK II (83) TO-100

BK II (92) Dual In-Line, 10-Lead

BK II (93) Dual In-Line, 14-Lead

BK II (94) Dual In-Line, NOC

RDI (93) Internal Connection Mode

RDI(94) Beam Lead

RDI(95) Inverted, Face Down (Lid, Flip Chip)

RDI(96) Flush (Metallized)

RDI(97) Flying Leads

RDI(98) Internal Connection Mode NOC

GNI (83) Lead Attachment Modes (External Leads)

GNI(84) Microcable

GNI(85) Modules

GNI(86) Multi Layer Board

GNI(87) Pressure Connector

GNI(88) Printed Circuit Board

GNI(89) Soldered

GNI(90) Stacked Arrays

GNI(91) Welded

GNI (92) Lead/Terminal Bond Mode

GNI(93) Ball TC Bond

GNI(94) Plated

GNI(95) Resistance Weld

GNI(96) Solder

GNI(97) Stitch TC Bond

GNI(98) Ultrasonic Bond

GNI(99) Wedge TC Bond

BKI (90) Package Seal

BKI(91) Glass-to-Glass Seal

BKI(92) Glass-to-Metal Seal

BKI(93) Molded

BKI(94) Seam Weld

BKI(95) Package Seal NOC

Item Status*

BKI(96) Developmental

BKI(97) Experimental

BKI(98) Pilot Production

BKI(99) Production

Major System*

GYI(53) Minuteman II

GYI(54) F-111

GYI(55)

GYI(56)

GYI(57)

GYI(58)

GYI(59)

GYI(60)

GYI (86) Circuit Parameters

GYI(87) Bandwidth

GYI(88) Common Mode Rejection Ratio

GYI(89) Gain

GYI(90) Noise Figure

GYI(91) Noise Margin

GYI(92) Power Dissipation

GYI (93) <u>Device Parameters</u>

GYI(94) Capacitance

GYI(95) Current Transfer Ratio (Beta)

GYI(96) Inductance

GYI(97) Resistivity

GYI(98) Transconductance

<u>Unqualified Terms</u>

These are unqualified terms which are to be indexed whenever any of the qualified forms of the terms are indexed or whenever no further qualification of the concept is given in the document being indexed.

Aluminum (all)	GYI (80)
Ceramics (all)	GYI (81)
Copper (all)	GYI (82)
Current (all)	GYI (83)
Gold (all)	GYI (84)
Nickel (all)	GYI (85)
Power (all)	GYI (99)
Voltage (all)	GYI (61)

8.4 Document Descriptors

Report Date*

BLI(00) Prior to 1960

BLI(10) 1960

BLI(11) 1970

BLI(12) 1980

BLI(51) 00

BLI(01) 1

BLI(02) 2

BLI(03) 3

BLI(04) 4

BLI(05) 5

BLI(06) 6

BLI(07) 7

BLI(08) 8

BLI(09) 9

Report Security Classification*

BLI(13) Classified (see also Limited and/or Proprietary Information)

BLI(14) Confidential

BLI(15) Secret

BLI(16) Unclassified (see also Limited, and/or Proprietary Information)

BLI(17) Limited

BLI(18) Proprietary Information

Report Source*

- BLI(19) Military and Space
  - BLI(20) Air Force
  - BLI(21) Army
  - BLI(22) DOD
  - BLI(23) NASA
  - BLI(24) Navy
- BLI(25) Device Manufacturer

DIGIT CODE

Tens	Units
RDI (83) 0-	RDI (64) -0
RDI (74) 1-	RDI (65) -1
RDI (75) 2-	RDI (66) -2
RDI (76) 3-	RDI (67) -3
RDI (77) 4-	RDI (68) -4
RDI (78) 5-	RDI (69) -5
RDI (79) 6-	RDI (70) -6
RDI (80) 7-	RDI (71) -7
RDI (81) 8-	RDI (72) -8
RDI (82) 9-	RDI (73) -9

Report Source* (cont')

Device Manufacturer (cont')

RDI (83) Amelco Semiconductor (1)
RDI (65)

RDI (83) Amperex Electronic Corp. (2)
RDI (66)

RDI (83) Bunker-Ramo Corp. (3)
RDI (67)

RDI (83) Fairchild Semiconductor (4)
RDI (68)

RDI (83) General Instrument Corp. (5)
RDI (69)

RDI (83) ITT Semiconductor (6)
RDI (70)

RDI (83) Motorola Semiconductor Products, Inc. (7)
RDI (71)

RDI (83) National Semiconductor Corp. (8)
RDI (72)

RDI (83) Philco-Ford Corp. (9)
RDI (73)

Philco-Ford Bipolar IC's

Philco-Ford MOS IC's

RDI (64) Radiation, Inc. (10)
RDI (74)

RDI (74) Radio Corporation of America (11)
RDI (65)

RDI (74) Raytheon Company (12)
RDI (66)

RDI (74) Signetics Corp. (13)
RDI (67)

RDI (74) Siliconix, Inc. (14)
RDI (68)

RDI (74) Sperry Semiconductor (15)
RDI (69)

RDI (74) Sprague Electric Co. (16)
RDI (70)

Report Source* (cont')

Device Manufacturer (cont')

RDI (74) Sylvania Electric Products, Inc. (17)
RDI (71)

RDI (74) Texas Instruments Incorporated (18)
RDI (72)

RDI (74) Transitron Electronic Corp. (19)
RDI (73)

RDI (75) Union Carbide Electronics (20)

RDI (75) Westinghouse Electric Corp. (21)
RDI (65)

BLI(26) Device User (Equipment Mfgr/Systems Contractors)

DIGIT CODE

Tens	Units
SDI(58) 0-	SDI(05) -0
SDI(59) 1-	SDI(91) -1
SDI(68) 2-	SDI(92) -2
SDI(80) 3-	SDI(93) -3
SDI(84) 4-	SDI(94) -4
	SDI(95) -5
	SDI(96) -6
	SDI(97) -7
	SDI(98) -8
	SDI(99) -9

Report Source* (cont')

Device User (cont')

SDI(58) A.C. Electronics (1)
SDI(91)

SDI(58) Autonetics (2)
SDI(92)

SDI(58) Avco (3)
SDI(93)

SDI(58) Bendix (4)
SDI(94)

SDI(58) Boeing (5)
SDI(95)

SDI(58) Burroughs (6)
SDI(96)

SDI(58) General Electric (7)
SDI(97)

SDI(58) Honeywell (8)
SDI(98)

SDI(58) Martin-Marietta (9)
SDI(99)

SDI(59) Motorola (10)
SDI(05)

SDI(59) Norden (11)
SDI(91)

SDI(59) Sanders (12)
SDI(92)

SDI(59) Sperry Gyroscope (13)
SDI(93)

SDI(59) Sylvania (14)
SDI(94)

SDI(59) Teledyne (15)
SDI(95)

BLI(27) Industry Associations (ASTM, IEEE)

BLI(28) Non-Military Government Agency (other than NASA)

BLI(29) R&D and Test Laboratories (Includes University Labs.)

Sponsoring Organization*

BLI(30) Military and Space

BLI(31) Air Force

BLI(32) Army

BLI(33) DOD

BLI(34) NASA

BLI(35) Navy

BLI(36) Device Manufacturer

BLI(37) Device User (Equipment Mfgr/Systems Contractors)

BLI(38) Industry Associations (ASTM, IEEE)

BLI(39) Non-Military Government Agency (other than NASA)

BLI(40) R&D and Test Laboratories (Includes University Labs.)

Data Validation*

BLI(41) Not Certified

BLI(42) Certified

BLI(43) Activity Monitored by Source-Sponsor Representative

BLI(44) Activity Witnessed and Report Countersigned by Source-Sponsor

BLI(45) Countersigned by Responsible Report-Source Official

BLI(46) Facility Approved by Source-Sponsor Representative

BLI(47) Procedure Approved by Source-Sponsor

BLI(48) Test Equipment Procedures Approved by Non-resident Source-Sponsor Representative

BLI(49) Test Equipment Procedures Approved by Resident Source-Sponsor Agent

Report Type*

- BLI(50) Bibliography
  - Case Study ORI(80)
- BLI(52) Drawings
- BLI(53) IITRI Generated Device Description
- BLI(54) IITRI Generated Data Summary
- BLI(55) Journal Article
- BLI(56) Proceedings, Symposia, Conference
- BLI(57) R/D Report
- BLI(58) Specifications
- BLI(59) Survey and Review
  - BLI(60) Application
  - BLI(61) Available Devices/Circuits/Functions
  - BLI(62) Equipment
  - BLI(63) Packaging
  - BLI(64) Processing
- BLI(65) Technical Report
- BLI(66) Test Data
- BLI(67) Vendor
  - BLI(68) General Catalog
  - BLI(69) Specific Information

Document Format*

BLI(70) Audio-Video Tape Recording

BLI(71) Hard Copy Document

BLI(72) Machine Printout

BLI(73) Machine Sensible Format

BLI(74) Microfiche

BLI(75) Microfilm

BLI(76) Slide

File Entry Date

BLI(83) 1968

BLI(84) 1969

BLI(85) 1970

BLI(86) 1971

BLI(87) 1972

BLI(88) January

BLI(89) February

BLI(90) March

BLI(91) April

BLI(92) May

BLI(93) June

BLI(94) July

BLI(95) August

File Entry Date (cont')

BLI(96)	September
BLI(97)	October
BLI(98)	November
BLI(99)	December

8.5 Microelectronic Design and Development

SDI (00) Circuit/Device Theory

SDI(23) Physical Phenomena

- SDI(24) Carrier Diffusion
- SDI(25) Carrier Generation
- SDI(26) Carrier Injection
- SDI(27) Carrier Recombination
- SDI(28) Carrier Saturation
- SDI(29) Depletion
- SDI(30) Electrical Conduction
- SDI(31) Electrical Noise Generation
- SDI(32) Electron Spin
- SDI(33) Enhancement
- SDI(34) Faults and Dislocations
- SDI(35) Ferroelectricity
- SDI(36) Field Effect
- SDI(37) Hall Effect
- SDI(38) Impurity Diffusion
- SDI(39) Inversion and Channeling
- SDI(40) Ion Migration
- SDI(41) Magnetism
- SDI(42) Mechanical Propagation
- SDI(43) Negative Resistance/Gunn Effect
- SDI(44) Photoconductivity

Circuit/Device Theory (cont')

Physical Phenomena (cont')

SDI(45) Pinch Off

SDI(46) Radiation Emission/Electroluminesence

SDI(47) Resonance

SDI(48) Reverse Breakdown

SDI(49) Superconductivity

SDI(50) Thermal Conduction

SDI(51) Thermoelectric Effects

SDI(07) Physical Parameters

SDI(08) Carrier Concentration

SDI(09) Carrier Lifetime

SDI(10) Carrier Mobility

SDI(11) Carrier Velocity

SDI(12) Contact Potential

SDI(13) Diffusion Coefficient

SDI(14) Diffusion Length

SDI(15) Energy Gap

SDI(16) Energy Level

SDI(17) Fermi Level

SDI(18) Heat Capacity

SDI(19) Storage Time

Circuit/Device Theory (cont')

Physical Parameters (cont')

SDI(20) Thermal Conductivity

SDI(21) Thermal Diffusivity

SDI(22) Work Function

SDI(01) Chemical Phenomena

SDI(02) Compound Formation

SDI(03) Decomposition

Etching WI(20)

Oxidation WI(13)

SDI(06) Polymerization

SDI(53) Metallurgical Phenomena

Alloying WI(10)

Crystal Growth WI(02)

SDI(54) Fatigue

SDI(55) Shear Modules

SDI(56) Work Hardening

SDI(57) Young's Modules

SDI(52) Mathematical Modeling

SDI (60) Circuit/Device Implementation

SDI(61) Breadboarding

SDI(62) Circuit Layout

SDI(63) Computer Aids

SDI(64) Layout

SDI(65) LSI Interconnection Design

SDI(66) Mask Design

SDI(67) Device Geometry

Mask Design SDI(66)

SDI(69) Modification

SDI(70) Testing

Electrical characterization PI (05)

SDI (71) Functional/Circuit Design and Optimization

SDI(72) Computer Analysis

SDI(73) Design Considerations

SDI(74) Functional Synthesis

SDI(75) Test Pattern

SDI(76) Tolerances

SDI(77) Trade-Offs

8.6 Failure Analysis Studies

PI (01) Failure Analysis Techniques

PI(02) Chemical Analysis

PI(03) Conventional Microscopic Examination

PI(04) Dissection and Sectioning

PI(05) Electrical Characterization

PI(06) Electron Microprobe

PI(07) Electron Microscopic Examination

PI(08) Holographic Examination (use of Holograms)

PI(09) IR Thermal Mapping

PI(10) Non-Destructive Evaluation

PI(11) Photochromic Paints

PI(12) Photoresponse Mapping

PI(13) Spectrographic Analysis

PI(14) Sub-Optical Electromagnetic Energization (NON-IR)

PI(15) Ultrasonic Inspection

PI(16) Visual Inspection

PI(17) X-Ray Evaluation

PI (18) Failure Environment

PI(19) Application Tests, Inplant

PI(20) Application Tests, Onsite

PI(21) Assembly/Installation

PI(22) Field Use

Failure Environment (cont')

PI(23) Laboratory Environmental Test

PI(24) Laboratory Life Test

PI(25) Post Production Screen/Burn-In

PI(26) Product Inspection

PI (27) Failure Modes

PI(28) Functional Degradation

PI(29) Inspection Specification Deviation

PI(30) Open Circuit

PI(31) Package Failure

PI(32) Short Circuit

PI (33) Failure Stress Domain

PI(34) Acceleration. Constant

PI(35) Liquid Immersion

PI(36) Mechanical Shock

PI(37) Moisture or Humidity

PI(38) Noise. Acoustical

PI(39) Pressure - Gas

PI(40) Radiation. Electromagnetic

PI(41) Radiation Exposure (Particle)

Failure Stress Domain (cont')

PI(42) Salt Atmosphere/Spray

PI(43) Sand and Dust

PI(44) Temperature >102.5°C

PI(45) Temperature <-42.5°C

PI(46) Thermal Shock

PI(47) Vacuum

PI(48) Vibration

PI (49) Causes of Failure

PI(50) Inherent Material Flaws

PI(51) Misapplication

PI(52) Device Mishandling

PI(53) Erroneous Lead Positioning

PI(54) Overstressed Devices

PI(55) Poor Design

Circuit Layout SDI(62)

Device Geometry SDI(67)

PI(56) Process Design

PI(57) Process Equipment Design

PI(60) Process Errors

Causes of Failures (cont')

PI(61) Workmanship Defects

PI(62) Excessive Lead Length

PI(63) Improper Component Alignment

PI(64) Improper Mask Alignment

PI(65) Improper Package Marking

PI(66) Improper Wire Bonding

PI(67) Loose Material in Package

PI(68) Scratches

PI(69) Workmanship Defects NOC

PI (70) Physical Defects

PI(71) Broken Lead

PI(72) Contamination

PI(73) Cracked Die

PI(74) Cracked Package

PI(75) Crystal Defects

PI(76) Defective Bond

PI(77) Diffusion Defects

PI(78) Epitaxy Defects

PI(79) Film Thickness Defect

PI(80) Foreign Material

PI(81) Improper Etch

Physical Defects (cont')

PI(82) Mask Misalignment

PI(83) Metallization Discontinuity

PI(84) Oxidation Defect

PI(85) Pin Holes in Metallization

PI(86) Pin Holes in Oxide

PI(87) Poor Metallization Adhesion

PI(88) Seal Leak

SDI (78) Failure Phenomena

SDI (79) Carrier Generation Through Radiation

Compound Formation SDI(02)

SDI (81) Crystal Degradation by Radiation

SDI (82) Disappearance of Metallization

SDI (83) Electrolytic Corrosion

Inversion and Channeling SDI(39)

Ion Migration SDI(40)

SDI (86) Lead Fatigue

SDI (87) Metallurgical Diffusion

SDI (88) Plague Formation

SDI (89) PNPN Latch-Up

SDI (90) Secondary Breakdown

ORI (89) Corrective Measures

ORI(90) Final Inspection

ORI(91) Inprocess Inspection Procedures

ORI(92) Materials Control

ORI(93) Post-Production Screens

ORI(94) Process Control

ORI(95) Process Equipment Improvement

ORI(96) Process Improvement

ORI(97) Procurement Specification

ORI(98) Quality Assurance Measures

ORI(99) Redesign

SDI (85) Failure Analysis Facilities

8.7 WI(00) Fabrication Techniques and Equipment

WI(01) Material Preparation

- WI(02) Crystal Growth
- WI(03) Purification and Refinement

WI(04) Wafer Preparation

- WI(05) Wafer Cutting
- WI(06) Wafer Etching
- WI(07) Wafer Lapping
- WI(08) Wafer Polishing

WI(09) Junction Formation

- WI(10) Alloying
- WI(11) Diffusion
- WI(12) Epitaxy

WI(13) Oxidation

WI(14) Photolithography

- WI(15) Developing
- WI(16) Exposure
- WI(17) Masking
- WI(18) Photoresist
- WI(19) Washing

WI(20) <u>Etching</u>

WI(21) <u>Surface Passivation</u>

WI(22) <u>Deposition</u>

- WI(23) Thick Film
  - WI(24) Metal Screen
  - WI(25) Silk Screen
- WI(26) Thin Film
  - WI(27) Sputtering
  - WI(28) Vacuum Deposition
  - WI(29) Vapor Plating

WI(30) <u>Assembly</u>

- WI(31) Breaking (Dicing*)
- WI(32) Die Bonding
  - WI(33) Eutectic Braze
    - Glass Frit BK II (59)
    - Solder GNI (96)
  - WI(36) Die Bonding NOC

Assembly (cont')

WI(37) Lead/Terminal Bonding (Wire Bonding*)

WI(38) Thermo Compression Bonding

Ball TC Bond GNI(93)

Stitch TC Bond GNI(97)

Wedge TC Bond GNI(99)

Ultrasonic Bond GNI(98)

WI(35) Scribing

WI(34) Washing

WI (39) Encapsulation/Package Sealing

Glass-to-Glass Seal BKI(91)

Glass-to-Metal Seal BKI(92)

Molded BKI(93)

Seam Weld BKI(94)

WI (50) Lead Attachment Processes and Equipment (External Leads)

WI(51) Cold Welding

Resistance Weld GNI(95)

Soldered GNI(89)

WI(52) Lead Attachment Processes and Equipment NOC

WI (55) Process Control Techniques

- WI(56) Beveling
- WI(57) Deposition Rate Monitoring
- WI(58) Probing
- WI(59) Residual Gas Analysis
- WI(60) Use of Test Patterns

WI (53) Process Effectiveness

- WI(54) Yield

WI (61) MOS Processes NOC

8.8 Specifications (Content Descriptors)

WI (75) Data System Specifications

WI (76) Equipment System Level Specifications

WI (77) Material Control (RAW) Specifications

WI (78) Packaging and Delivery Specifications

WI (79) Process Control Specifications

WI (80) Quality Assurance Specifications

- WI(81) Government Agency QA Specifications
- WI(82) Quality Control Manuals
- WI(83) Reliability and Environmental Test Methods
- WI(84) User Proprietary Screening and Burn-In Specifications
- WI(85) Vendor QA Plans and Specifications (Performance Spec)
- WI(86) Vendor Screening and Burn-In Specifications

8.9 ORI (00) Reliability Technology

ORI (01) General Methodology

ORI (02) Prediction and Modeling

ORI (03) Test Techniques and Procedures

- ORI(04) Accelerated Testing
- ORI(05) Agree Test
- ORI(06) Atmospheric Stress Testing
- ORI(07) Burn-In Procedures
- ORI(08) Mechanical Stress Testing
- ORI(09) Operating Tests
- ORI(10) Radiation Environments
- ORI(11) Screening Procedures
- ORI(12) Step Stress Testing
- ORI(13) Thermal Stress Testing
- ORI(14) Test Techniques and Procedures NOC

ORI (15) Statistical Tools

- ORI(16) Acceleration Factors
- ORI(17) Attributes Data Analysis
- ORI(18) Design of Experiments
- ORI(19) Exponential Distribution
- ORI(20) Machine Processing
- ORI(21) Variables Data Analysis
- ORI(22) Weibull Analysis

ORI (23) Data Collection and Reduction

ORI(24) Automated Systems

ORI(25) Data Merging

ORI(26) Manual Systems

ORI (27) Facilities

ORI(28) Inspection

ORI(29) Performance Measurement

ORI(30) Reliability and Environmental Test

8.10 Y(00) Part Level Data

Test Type*

Developmental (Experimental*) BKI(96)

YI(02) Performance

YI(03) Quality Assurance (Device Test Oriented)

YI(04) Burn-In Test

YI(05) Lot Acceptance

YI(06) Product Line Audit

YI(07) Qualification (Procurement)

Reliability Demonstration ORI(71)

YI(09) Screening (Processing Control*)

YI(10) Special Reliability Study

Specification Reference*

YI(11) MIL-M-23700

YI(12) MIL-S-19500

YI(13) MIL-STD-202

YI(14) MIL-STD-750

YI(15) NASA

YI(16) RADC Spec. #2867

YI(17) User Procurement

YI(18) Vendor

YI(19) Special Military

YI (26) <u>Operational Static Life Test</u>

YI(27) <-82.5°C

YI(28) -82.5°C to <-42.5°C

YI(29) -42.5°C to <21°C

YI(30) 21°C to <31°C

YI(31) 31°C to <102.5°C

YI(32) 102.5°C to <152.5°C

YI(33) 152.5°C to <202.5°C

YI(34) 202.5°C to <302.5°C

YI(35) ≥302.5°C

<u>Operational Static Test Supply Voltage</u>

YI(36) <95% Rated

YI(37) 95% to <105% Rated

YI(38) 105% to <155% Rated

YI(39) ≥155% Rated

<u>Operational Static Test Load Power</u>

YI(40) <95% Rated

YI(41) 95% to <105% Rated

YI(42) 105% to <155% Rated

YI(43) ≥155% Rated

Storage Life Test Temperature

YI(44) <21°C

YI(45) 21°C to <102.5°C

YI(46) 102.5°C to <152.5°C

YI(47) 152.5°C to <202.5°C

YI(48) 202.5°C to <302.5°C

YI(49) ≥302.5°C

YI (50) Intermittent Life Test

Intermittent Stress Domain*

YI(51) Current

YI(52) Power

YI(53) Temperature

YI(54) Voltage

YI(55) Combination with Environment Stresses

Intermittent Life Test Temperature

YI(56) <-82.5°C

YI(57) -82.5°C to <-42.5°C

YI(58) -42.5°C to <21°C

YI(59) 21°C to <31°C

YI(60) 31°C to <102.5°C

Intermittent Life Test Temperature (cont')

YI(61) 102.5°C to <152.5°C

YI(62) 152.5°C to <202.5°C

YI(63) 202.5°C to <302.5°C

YI(64) ≥302.5°C

Intermittent Life Test Supply Voltage

YI(65) <95% Rated

YI(66) 95% to <105% Rated

YI(67) 105% to <155% Rated

YI(68) ≥155% Rated

Intermittent Life Test Load Power

YI(69) <95% Rated

YI(70) 95% to <105% Rated

YI(71) 105% to <155% Rated

YI(72) ≥155% Rated

YI (73) Step Stress Test

Step Stress Test Domain*

YI(74) Atmospheric Environments

YI(75) Current

YI(76) High Temperature

Step Stress Test Domain* (cont')

YI(77) Mechanical Environments

YI(78) Power

YI(79) Thermal Environments

YI(80) Voltage

YI(81) Combination

Step Stress Test Maximum Temperature

YI(82) <21°C

YI(83) 21°C to <102.5°C

YI(84) 102.5°C to <202.5°C

YI(85) 202.5°C to <302.5°C

YI(86) ≥302.5°C

YI (87) Accelerated Life Test

Accelerated Life Test Domain*

YI(88) Atmospheric Environments

YI(89) Current

YI(90) High Temperature

YI(91) Mechanical Environments

YI(92) Power

YI(93) Thermal Environments

YI(94) Voltage

YI(95) Combination

Accelerated Life Test Maximum Temperature*

GYI(00) <21°C

GYI(01) 21°C to <102.5°C

GYI(02) 102.5°C to <202.5°C

GYI(03) 202.5°C to <302.5°C

GYI(04) ≥302.5°C

GYI (05) Operational Dynamic Life Test

Operational Dynamic Test Maximum Temperature

GYI(06) <-82.5°C

GYI(07) -82.5°C to <-42.5°C

GYI(08) -42.5°C to <21°C

GYI(09) 21°C to <31°C

GYI(10) 31°C to <102.5°C

GYI(11) 102.5°C to <152.5°C

GYI(12) 152.5°C to <202.5°C

GYI(13) 202.5°C to <302.5°C

GYI(14) ≥302.5°C

Operational Dynamic Maximum Supply Voltage

GYI(15) <95% Rated

GYI(16) 95% to <105% Rated

GYI(17) 105% to <155% Rated

GYI(18) ≥155% Rated

Operational Dynamic Maximum Load Power

GYI(19) <95% Rated

GYI(20) 95% to <105% Rated

GYI(21) 105% to <155% Rated

GYI(22) ≥155% Rated

Agree Test ORI(05)

GYI (24) Environmental Condition

GYI(25) Acoustic Noise

GYI(26) Constant Acceleration (Centrifuge*)

GYI(27) Electromagnetic and Particle Radiation

GYI(28) Humidity

GYI(29) Immersion

GYI(30) Low Barometric Pressure

GYI(31) Mechanical Shock

GYI(32) Moisture Resistance

GYI(33) RF Interference

Salt Atmosphere/Spray PI(42)

GYI(36) Soldering Heat

GYI(37) Temperature Cycling

GYI(38) Terminal Strength (Lead Pull)

Thermal Shock PI(46)

Environmental Condition (cont')

GYI(40) Vibration, Fatigue

GYI(41) Vibration, Random

GYI(42) Vibration, Variable Frequency

GYI (43) Test Results

Acceleration Factors ORI(16)

GYI(45) Attributes, Summary

GYI(46) Failure Analysis Results

GYI(47) Performance Curves

GYI(48) Raw Variables Data

GYI(49) Reliability Attributes Summary

GYI(50) Variables Analysis Summaries

8.11 Applications

ORI (35) <u>Application Environment</u>

- ORI(36) <u>Aircraft Environment</u>
  - ORI(37) Airborne Manned
  - ORI(38) Airborne Unmanned
  - ORI(39) Ground Checkout
- ORI(40) <u>Ground Environment</u>
  - ORI(41) Ground Fixed
  - ORI(42) Ground Laboratory
  - ORI(43) Ground Mobile
  - ORI(44) Ground Portable
- ORI(45) <u>Missile Environment</u>
  - ORI(46) Ground Checkout
  - ORI(47) Launch and Flight
- ORI(48) <u>Shipboard Environment</u>
  - ORI(49) Shipboard Submarine
  - ORI(50) Shipboard Surface
- ORI(51) <u>Spacecraft Environment</u>
  - ORI(52) Ground Checkout
  - ORI(53) Satellite Launch
  - ORI(54) Satellite Orbit (Flight)
- ORI(55) <u>Unspecified Environment</u>

Equipment Class*

OR I(56) Combination and NOC

OR I(57) Communications

OR I(58) Computation (Digital Processers)

OR I(59) Control

OR I(60) Instrumentation and Display

OR I(61) Navigation

OR I(62) Power (Power Supplies)

OR I(63) Radar

OR I(64) Signal Processing (Buffers, Convertors, Amplifiers)

OR I(65) Unspecified Equipment Class

Application Status*

Developmental BK I(96)

OR I(67) Factory Checkout

OR I(68) Field Operations

OR I(69) Field Testing (e.g. Category II and III)

OR I(70) Production Test and Inspection

OR I(71) Reliability Demonstration

ORI (72) <u>Reliability Data</u>

ORI(73) Application Stress and Parts Counts

ORI(74) Failure Modes

ORI(75) Failure Rate Statistics

ORI(76) Malfunction Reports

ORI(77) Test Reports

ORI(78) Reliability Data NOC

ORI (79) <u>Application Design Techniques and Considerations</u>

ORI(80) Case Study

ORI(81) Comparison with Discrete

ORI(82) Economic Factors

ORI(83) Environmental

ORI(84) Equipment Application

ORI(85) Packaging

ORI(86) System Application

ORI (87) <u>Vendor Application Notes</u>

8.12 Other NOC

(Do not set up Termatrex cards in this group until information is available)

Value Engineering

Systems Effectiveness

Availability

Information Systems

Economics

Maintainability

9.0 ALPHABETICAL TERM LIST

The alphabetical term list includes all the concept terms of the structured term list. Asterisk (*) terms are not represented on Termatrex cards. The Termatrex code is given for all terms represented by Termatrex cards. The major categories into which these terms are organized will be represented as follows:

- 8.1 Generic Class Descriptors
- 8.2 Manufacturer Descriptors
- 8.3 Item Descriptors
- 8.4 Document Descriptors
- 8.5 Microelectronic Design and Development
- 8.6 Failure Analysis Studies
- 8.7 Fabrication Techniques and Equipment
- 8.8 Specifications
- 8.9 Reliability Technology
- 8.10 Part Level Data
- 8.11 Applications
- 8.12 Other

Category numbers listed above refer to Section 8.0.

P.O. Terms = post on - requires that these terms be considered for indexing wherever applicable; for example, an accelerated life test - maximum temperature of <21°C should be indexed and coded as

Accelerated Life Test-Maximum Temperature		
<21°C	GYI (00)	
Accelerated Life Test	YI (87)	P.O.
Part Level Data	YI (00)	P.O.

"See" terms such as Accelerated Life Test Domain* are not represented by Termatrex cards. However, the concepts they encompass are represented by Termatrex cards. It is necessary to review each of the terms listed following "see" to determine how the

concept is handled in the system. For example, Accelerated Life Test Domain*

See: Atmospheric Environments - Accelerated Life

Test Domain YI (88)

Current - Accelerated Life Test Domain YI (89)

High Temperature - Accelerated Life Test

Domain YI (90)

Mechanical Environments - Accelerated Life Test

Domain YI (91)

Power - Accelerated Life Test Domain YI (92)

Thermal Environments - Accelerated Life Test

Domain YI (93)

Voltage - Accelerated Life Test Domain YI (94)

Combination - Accelerated Life Test Domain YI (95)

<u>"See" terms</u> also covers common synonyms and near-synonyms identified in the alphabetical listing. Actual concept terms used for this system are identified; for example, Active Substrate IC* see Composite IC, NOC RDI (00).

<u>Includes</u>: Application Environment is represented by a Termatrex card. Concepts covered by this are listed as includes: - - - To locate additional concept breakdowns it is necessary to locate these terms in the listing Application Environment ORI (35)

Includes:

→ Aircraft Environment ORI (36)

Ground Environment ORI (40)

Missile Environment ORI (45)

→ Aircraft Environment ORI (36)

Includes:

Airborne Manned ORI (37)

Airborne Unmanned ORI (38)

Ground Checkout ORI (39)

Considered under: indicates higher concept to which the concept is related; i.e., Aircraft Environment ORI (36) considered under Applications BLI (60).

Digit Coding: Digit coding has been used to conserve the number of cards used by the system. Digit coding has been used for Manufacturer's Names, Part Numbers, Report Dates, Device Manufacturers and Device Users. Explanation of the use of this coding is to be found in Section 2.4.2. An example of the use of this coding follows: AC Electronics - code #01: Termatrex cards SD I (58), SD I (91).

<u>Alphabetical Term List</u>

Accelerated Life Test Y I(87)

P.O. Part Level Data Y I(00)

Includes:

- Accelerated Life Test Domain*
- Accelerated Life Test Maximum Temperature

Accelerated Life Test Domain*

P.O. Accelerated Life Test Y I(87)

P.O. Part Level Data Y I(00)

See:

- Atmospheric Environments Y I(88)
- Current Y I(89)
- High Temperature Y I(90)
- Mechanical Environments Y I(91)
- Power Y I(92)
- Thermal Environments Y I(93)
- Voltage Y I(94)
- Combination Y I(95)

Accelerated Life Test Maximum Temperature

P.O. Accelerated Life Test Y I(87)

P.O. Part Level Data Y I(00)

GY I(00) < 21°C

GY I(01) 21°C to < 102.5°C

GY I(02) 102.5°C to < 202.5°C

GY I(03) 202.5°C to < 302.5°C

GY I(04) ≥ 302.5°C

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*Concept not represented by a Termatrex Card.

Accelerated Testing	OR I(04)	8.9	P.O. Test Techniques and Procedures OR I(03)
			P.O. Reliability Technology OR I(00)
Acceleration, Constant	P I(34)	8.6	P.O. Failure Stress Domain P I(33)
			P.O. Failure Analysis Studies P I(00)
Acceleration Factors	OR I(16)	a) 8.10	P.O. Test Results GY I(4[illegible])
			P.O. Part Level Data Y I(00)
		b) 8.9	P.O. Statistical Tools OR I(15)
			P.O. Reliability Technology OR I(00)
			or neither
A.C. Electronics (01)	SD I(58) SD I(91)	8.4	P.O. Device User BL I(26)
			Considered under Report Source*
Acoustic Noise	GY I(25)	8.10	P.O. Environmental Condition GY I(24)
			P.O. Part Level Data Y I(00)
Acoustical Transducer	GN I(49)	8.3	P.O. Special Active Devices NOC GN I(48)
			P.O. Circuit Component GN I(00)
			Considered under MEL Device Element Descriptor*
Active Substrate IC*			See Composite IC, NOC
Activity Monitored by Source-Sponsor Representative	BL I(43)	8.4	Considered under Data Validation*
Activity Witnessed and Report Countersigned by Source-Sponsor Agent	BL I(44)	8.4	Considered under Data Validation*
A/D Converter	BK I(50)	8.3	P.O. Circuit Functions BK I(49)
Adders	BK I(51)	8.3	P.O. Circuit Functions BK I(49)

Agree Test	OR I(05)	a) 8.10	P.O. Part Level Data Y I(00)
		b) 8.9	P.O. Test Techniques and Procedures OR I(03)
			P.O. Reliability Technology OR I(00)
Air	BK II(09)	8.3	P.O. Dielectrics and Insulating Materials BK II(08)
			Considered under Functional Elements*
			P.O. Device Element Materials BK II(26)
Airborne Manned	OR I(37)	8.11	P.O. Aircraft Environment OR I(36)
			P.O. Application Environment OR I(35)
			Considered under Applications
Airborne Unmanned	OR I(38)	8.11	P.O. Aircraft Environment OR I(36)
			P.O. Application Environment OR I(35)
			Considered under Applications
Aircraft Environment	OR I(36)	8.11	P.O. Application Environment OR I(35)
			Considered under Applications
			Includes:
			Airborne Manned OR I(37)
			Airborne Unmanned OR I(38)
			Ground Checkout OR I(39)
Air Dielectric			See Dielectric, Air
Air Force	BL I(20)	8.4	P.O. Military and Space BL I(19)
			Considered under Report Source*
Air Force	BL I(31)	8.4	P.O. Military and Space BL I(30)
			Considered under Sponsoring Organization*

Alloy Junction	GN I(53)		8.3	Considered under Circuit Component Regions*
				Considered under MEL Device Element Descriptor*
Alloying	W I(10)	a)	8.5	P.O. Metallurgical Phenomena SD I(53)
				P.O. Circuit/Device Theory SD I(00)
		b)	8.7	P.O. Junction Formation W I(09)
				P.O. Fabrication Techniques and Equipment W I(00)
Alumina	BK II(47)	a)	8.3	P.O. Dielectrics and Insulating Materials BK II(08)
				Considered under Functional Elements*
				P.O. Device Element Materials BK II(26)
		b)	8.3	P.O. Substrate Materials BK II(46)
				Considered under Non-Functional Elements*
				P.O. Device Element Materials BK II(26)
Aluminum	BK II(19)		8.3	P.O. Dopant Materials BK II(18)
				Considered under Functional Elements*
				P.O. Device Element Materials BK II(26)
				P.O. Aluminum (All) GY I(80)
Aluminum	BK II(01)		8.3	P.O. Circuit Metallization Materials BK II(00)
				Considered under Functional Elements*
				P.O. Device Element Materials BK II(26)
				P.O. Aluminum (All) GY I(80)
Aluminum	BK II(28)		8.3	P.O. Wire Materials BK II(27)
				Considered under Functional Elements*

Term	Reference			Disposition
Aluminum (cont'd)				P.O. Device Element Material BK II(26) P.O. Aluminum (All) GY I(80)
Aluminum	BK II(65)		8.3	P.O. Package Terminal Material BK II(64) Considered under Non-Functional Elements* P.O. Device Element Materials BK II(26) P.O. Aluminum (All) GY I(80)
Aluminum (All)	GY I(80)		8.3	Unqualified terms
Aluminum-to-Aluminum, Direct	RD I(27)		8.1	P.O. Interconnection System RD I(26)
Aluminum-to-Aluminum, wire bond	RD I(28)		8.1	P.O. Interconnection System RD I(26)
Amelco Semiconductor (01)	RD I(83) RD I(65)	a) b)	8.2 8.4	Considered under Manufacturer P.O. Device Manufacturer BL I(25) Considered under Report Source*
Amperex Electronic Corp. (02)	RD I(83) RD I(66)	a) b)	8.2 8.4	Considered under Manufacturer P.O. Device Manufacturer BK I(25) Considered under Report Source*
Amplifier*				See Audio or Differential, or RF-IF or Video, or IF, or RF, or Operational or Power or Servo Amplifier
Analog*				See Linear
AND Gate (AND/OR Gate*)	BK I(52)		8.3	P.O. Circuit Functions BK I(49)
AND/OR Gate*				See AND Gate
Anode	GN I(54)		8.3	Considered under Circuit Component Regions* Considered under MEL Device Element Descriptor*

Term	Code		Related
Antimony	BK II(20)	8.3	P.O. Dopant Materials BK II(18) Considered under Functional Elements* P.O. Device Element Materials BK II(26)
Application (See also Applications)	BL I(60)	8.4	P.O. Survey and Review BL I(59) Considered under Report Type*
Application, Design Techniques and Considerations	OR I(79)	8.11	Considered under Applications Includes: Case Study OR I(80) Comparison with Discrete OR I(81) Economic Factors OR I(82) Environmental OR I(83) Equipment Application OR I(84) Packaging OR I(85) System Application OR I(86)
Application Environment	OR I(35)	8.11	Considered under Applications Includes: Aircraft Environment OR I(36) Ground Environment OR I(40) Missile Environment OR I(45) Shipboard Environment OR I(48) Spacecraft Environment OR I(51) Unspecified Environment OR I(55)
Applications		8.11	Includes: Application Design Techniques and Considerations OR I(79) Application Environment OR I(35) Application Status*

Term	Code		Cross-reference
Applications (cont'd)			Equipment Class* Reliability Data OR I(72) Vendor Application Notes OR I(87)
Application Status*		8.11	Considered under Applications See: Developmental BK I(96) Factory Checkout OR I(67) Field Operations OR I(68) Field Testing (e.g. Category II & III) OR I(69) Production Test and Inspection OR I(70) Reliability Demonstration OR I(71)
Application Stress and Parts Count	OR I(73)	8.11	P.O. Reliability Data OR I(72) Considered under Applications
Application Tests, Inplant	P I(19)	8.6	P.O. Failure Environment P I(18) P.O. Failure Analysis Studies P I(00)
Application Tests, Onsite	P I(20)	8.6	P.O. Failure Environment P I(18) P.O. Failure Analysis Studies P I(00)
Arithmetic Functional Unit	RD I(43)	8.1	Considered under Circuit Complexity*
Army	BL I(21)	8.3	P.O. Military and Space BL I(19) Considered under Report Source*
Army	BL I(32)	8.4	P.O. Military and Space BL I(30) Considered under Sponsoring Organization*
Arsenic	BK II(21)	8.5	P.O. Dopant Materials BK II(18) Considered under Functional Elements* P.O. Device Element Materials BK II(26)
Assembly	W I(30)	8.7	P.O. Fabrication Techniques and Equipment W I(00)

Term	Code			Relationship
Assembly (cont'd)				Includes:
				Breaking (dicing*) W I(31)
				Die Bonding W I(32)
				Lead/Terminal Bonding W I(37)
				Scribing W I(35)
				Washing W I(34)
Assembly/Installation	P I(21)		8.4	P.O. Failure Environment P I(18)
				P.O. Failure Analysis Studies P I(00)
Astable Multivibrator	BK I(53)		8.3	P.O. Circuit Functions BK I(49)
Atmospheric Environments	Y I(88)		8.12	Considered under Accelerated Life Test Domain*
				P.O. Accelerated Life Test Y I(87)
				P.O. Part Level Data Y I(00)
Atmospheric Environments	Y I(74)		8.10	Considered under Step Stress Test Domain*
				P.O. Step Stress Test Y I(73)
				P.O. Part Level Data Y I(00)
Atmospheric Stress Testing	OR I(06)		8.9	P.O. Test Techniques and Procedures OR I(03)
				P.O. Reliability Technology OR I(00)
Attributes Data Analysis	OR I(17)		8.9	P.O. Statistical Tools OR I(15)
				P.O. Reliability Technology OR I(00)
Attributes, Summary	GY I(45)		8.12	P.O. Test Results GY I(43)
				P.O. Part Level Data Y I(00)
Audio Amplifier	RD I(44)	a)	8.1	Considered under Circuit Complexity*
		b)	8.3	P.O. Circuit Functions BK I(49)
Audio-Video Tape Recording	BL I(70)		8.4	Considered under Document Format*
Automated Systems	OR I(24)		8.9	P.O. Data Collection and Reduction OR I(23)
				P.O. Reliability Technology OR I(00)

Autonetics (02)	SD I(58) SD I(92)	8.4	P.O. Device User BL I(26)
			Considered under Report Source*
Available Devices/ Circuits/ Functions	BL I(61)	8.4	P.O. Survey and Review BL I(59)
			Considered under Report Type*
Availability*		8.12	Other NOC
Avalanche Diode	GN I(31)	8.3	P.O. Diode GN I(30)
			P.O. Circuit Component GN I(00)
			Considered under MEL Device Element Descriptor*
Avco (03)	SD I(58) SD I(93)	8.4	P.O. Device User BL I(26)
			Considered under Report Source*
Ball TC Bond	GN I(93)	a) 8.7	P.O. Thermo Compression Bonding W I(38)
			P.O. Lead/Terminals Bonding W I(37)
			P.O. Assembly W I(30)
			P.O. Fabrication Techniques and Equipment W I(00)
		b) 8.3	P.O. Lead/Terminal Bond Mode GN I(92)
Bandwidth	GY I(87)	8.3	P.O. Circuit Parameters GY I(86)
Base	GN I(55)	8.3	Considered under Circuit Component Regions*
			Considered under MEL Device Element Descriptors*
Beam Lead*		8.1	See Dielectric, air
Beam Lead	RD I(94)	8.3	P.O. Internal Connection Mode RD I(93)
Bendix (04)	SD I(58) SD I(94)	8.4	P.O. Device User BL I(26)
			Considered under Report Source*
Beveling	W I(56)	8.7	P.O. Process Control Techniques W I(55)
			P.O. Fabrication Technique and Equipment W I(00)

Term	Code		Relationship
Bibliography	BL I(50)	8.4	Considered under Report Type*
Bipolar Transistors	GN I(10)	8.3	P.O. Transistors GN I(09)
			P.O. Circuit Component GN I(00)
			Considered under MEL Device Element Descriptors*
Bistable Multi-vibrator	BK I(54)	8.3	P.O. Circuit Function BK I(49)
Boeing (05)	SD I(58) SD I(95)	8.4	Device User BL I(26)
			Considered under Report Source*
Bonding			See Lead/Terminal Bonding or Die Bonding
Boron	BK II(22)	8.3	P.O. Dopant Materials BK II(18)
			Considered under Functional Elements*
			P.O. Device Element Materials BK II(26)
Breaking (Dicing*)	W I(31)	8.7	P.O. Assembly W I(30)
			P.O. Fabrication Techniques and Equipment W I(00)
Broken Lead	P I(71)	8.6	P.O. Physical Defects P I(70)
			P.O. Failure Analysis Studies P I(00)
Breadboarding	SD I(61)	8.5	P.O. Circuit/Device Implementation SD I(60)
Bulk Defect*			See Crystal, Epitaxy, and/or Diffusion Defects
Bunker-Ramo Corp. (03)	RD I(83) RD I(67)	a) 8.2	Considered under Manufacturer
		b) 8.4	P.O. Device Manufacturer BL I(25)
			Considered under Report Source*
Buried Layer	GN I(56)	8.3	Considered under Circuit Component Regions*
			Considered under MEL Device Element Descriptor*
Burn-In Procedures	OR I(07)	8.9	P.O. Test Techniques and Procedures OR I(03)
			P.O. Reliability Techniques OR I(00)

Burn-In Spec			See Quality Assurance Specs
Burn-In Test	Y I(04)	8.10	P.O. Quality Assurance Y I(03)
			Considered under Test Type*
			P.O. Part Level Data Y I(00)
Burroughs (06)	SD I(58) SD I(96)	8.4	P.O. Device User BL I(26)
			Considered under Report Source*
Can, Hermetically Sealed	RD I(52)	8.1	Considered under Package Configuration*
Capacitance	GY I(94)	8.3	P.O. Device Parameters GY I(93)
Capacitors	GN I(24)	8.3	P.O. Circuit Component GN I(00)
			Considered under MEL Device Element Descriptor*
			Includes:
			Diffused Junction GN I(25)
			Discrete Capacitor GN I(26)
			Film GN I(27)
			MOS GN I(28)
			Variable GN I(29)
Carrier Concentration	SD I(08)	8.5	P.O. Physical Parameters SD I(07)
			P.O. Circuit/Device Theory SD I(00)
Carrier Diffusion	SD I(24)	8.5	P.O. Physical Phenomena SD I(23)
			P.O. Circuit/Device Theory SD I(00)
Carrier Generation	SD I(25)	8.5	P.O. Physical Phenomena SD I(23)
			P.O. Circuit/Device Theory SD I(00)
Carrier Generation through Radiation	SD I(79)	8.4	P.O. Failure Phenomena SD I(78)
			P.O. Failure Analysis Studies P I(00)
Carrier Injection	SD I(26)	8.5	P.O. Physical Phenomena SD I(23)
			P.O. Circuit/Device Theory SD I(00)

Term	Code			Relation
Carrier Lifetime	SD I(09)		3.5	P.O. Physical Parameters SD I(07)
				P.O. Circuit/Device Theory SD I(00)
Carrier Mobility	SD I(10)		3.5	P.O. Physical Parameters SD I(07)
				P.O. Circuit/Device Theory SD I(00)
Carrier Recombination	SD I(27)		3.5	P.O. Physical Phenomena SD I(23)
				P.O. Circuit/Device Theory SD I(00)
Carrier Saturation	SD I(28)		3.5	P.O. Physical Phenomena SD I(23)
				P.O. Circuit/Device Theory SD I(00)
Carrier Velocity	SD I(11)		3.5	P.O. Physical Parameters SD I(07)
				P.O. Circuit/Device Theory SD I(00)
Case Study	OR I(80)	a)	3.4	Considered under Report Type*
		b)	3.11	P.O. Application Design Techniques and Considerations OR I(79)
				Considered under Applications
Cathode	GN I(57)		3.3	Considered under Circuit Component Regions*
				Considered under MEL Device Element Descriptor*
Causes of Failure	P I(49)		3.6	P.O. Failure Analysis Studies P I(00)
				Includes:
				Inherent Material Flaws P I(50)
				Misapplication P I(51)
				Poor Design P I(55)
				Process Errors P I(60)
				Workmanship Defects P I(61)
Ceramic Dielectric				See Dielectric, Ceramic
Ceramic Flat Pack				See Flat Pack, Ceramic
Ceramics (ALL)	GY I(81)		3.3	Unqualified terms

Ceramics	BK II(48)	8.3	P.O. Substrate Materials BK II(46) Considered under Non-Functional Materials* P.O. Device Element Material BK II(26) P.O. Ceramics (All) GY I(81)
Ceramics	RD I(88)	8.3	P.O. Package Material (Primary) RD I(87) Considered under Non-Functional Materials* P.O. Device Element Material BK II(26) P.O. Ceramics (All) GY I(81)
Cermets & Glazes (all compositions)	BK II(31)	8.3	P.O. Materials NOC BK II(13) Considered under Functional Elements* P.O. Device Element Materials BK II(26)
Certification, High Reliability			See High Reliability Certification
Certified	BL I(42)	8.4	Considered under Data Validation*
Channel	GN I(58)	8.3	Considered under Circuit Component Regions* Considered under MEL Device Element Descriptor*
Checkout			See Ground, Aircraft, Missile or Spacecraft Checkout
Chem. Analysis	P I(02)	8.6	P.O. Failure Analysis Techniques P I(01) P.O. Failure Analysis Studies P I(00)
Chemical Phenomena	SD I(01)	8.5	P.O. Circuit/Device Theory SD I(00) Includes: Compound Formation SD I(02) Decomposition SD I(03)

Chemical Phenomena (cont'd)			Includes (cont'd) Etching W I(20) Oxidation W I(13) Polymerization SD I(06)
Chromium	BK II(02)	X,3	P.O. Circuit Metallization Materials BK II(00) Considered under Functional Elements* P.O. Device Element Materials BK II(26)
Circuit Complexity*		T.1	See: Arithmetic Functional Unit RD I(43) Audio Amplifier RD I(44) Differential Amplifier RD I(45) Gate (Logic Gate) RD I(46) Multivibrator RD I(47) RF-IF Amplifier RD I(48) Storage Element RD I(49) Video (wideband) Amplifier RD I(50) Special NOC RD I(51)
Circuit Component	GN I(00)	X,3	Considered under MEL Device Element Descriptors* Includes: Capacitors GN I(24) Diode GN I(30) Discrete Microcomponent GN I(52) Distributed Passive Devices GN I(37) Inductor GN I(40) PNPN Devices GN I(01)

Circuit Component (cont'd)

Includes (cont'd)

Resistors GN I(42)

Transistors GN I(09)

Special Active Devices NOC GN I(48)

Circuit Component Regions*

8.3 Considered under MEL Device Element Descriptor*

See:

Alloy Junction GN I(53)

Anode GN I(54)

Base GN I(55)

Buried Layer GN I(56)

Cathode GN I(57)

Channel GN I(58)

Collector GN I(59)

Contact Area GN I(60)

Crossover GN I(61)

Diffused Junction GN I(25)

Drain GN I(63)

Electrodes GN I(64)

Emitter GN I(65)

Epitaxial Junction GN I(66)

Epitaxial Layer GN I(67)

Gate (IGFET Type) GN I(68)

Isolation Region GN I(69)

Planar Junction GN I(70)

Source (FET) GN I(71)

Terminals GN I(72)

Circuit/Device Implementation	SD I(60)	8.5	Includes:
			Breadboarding SD I(61)
			Circuit Layout SD I(62)
			Computer Aids SD I(63)
			Device Geometry SD I(67)
			Mask Design SD I(66)
			Modification SD I(69)
			Testing SD I(70)
Circuit/Device Theory	SD I(00)	8.5	Includes:
			Chemical Phenomena SD I(01)
			Mathematical Modeling SD I(52)
			Metallurgical Phenomena SD I(53)
			Physical Parameters SD I(07)
			Physical Phenomena SD I(23)
Circuit Functions	BK I(49)	8.3	Includes:
			A/D Converter BK I(50)
			Adders BK I(51)
			AND Gate (AND/OR Gate*) BK I(52)
			Astable Multivibrators BK I(53)
			Audio Amplifier RD I(44)
			Bistable Multivibrator BK I(54)
			Counters BK I(55)
			D/A Converter BK I(56)
			Differential Amplifier RD I(45)
			Gate Expanders BK I(57)
			IF Amplifier BK I(58)
			Magnetic Film Storage Elements BK I(59)

Term	Code		Relationships
Circuit Metalliza-tion Materials (cont'd)			Includes (cont'd) Silver BK II(06) Circuit Metallization Material NOC BK II(07)
Circuit Metalliza-tion Materials NOC	BK II(07)	8.3	P.O. Circuit Metallization Materials BK II(00) Considered under Functional Elements* P.O. Device Element Materials BK II(26)
Circuit Parameters	GY I(86)	8.3	Includes: Bandwidth GY I(87) Common Mode Rejection Ratio GY I(88) Gain GY I(89) Noise Figure GY I(90) Noise Margin GY I(91) Power Dissipation GY I(92)
Classified	BL I(13)	8.4	Considered under Report Security Classification* Includes: Confidential BL I(14) Secret BL I(15) Limited BL I(17) and/or Proprietary Information BL I(18)
CML (ECL*, MECL*, ECCSL*)	RD I(14)	8.1	P.O. Digital Logic RD I(13) Considered under Operational Type*
Cold Welding	W I(51)	8.7	P.O. Lead Attachment Processes and Equipment W I(50) P.O. Fabrication Techniques and Equipment W I(00)
Collector	GN I(59)	8.3	Considered under Circuit Component Regions* Considered under MEL Device Element Descriptor*

Circuit Functions (cont'd)			Includes (cont'd)
			Molecular Electronic Function BK I(60)
			Monostable Multivibrators BK I(61)
			NAND Gate (NAND/NOR Gate*) BK I(62)
			NOR Gate (NOR/NAND Gate*) BK I(63)
			Operational Amplifier BK I(64)
			OR Gate (OR/AND Gate*) BK I(65)
			Power Amplifier BK I(66)
			RF Amplifier BK I(67)
			Servo Amplifier BK I(68)
			Superconducting Storage Elements BK I(69)
			Video Amplifier RD I(50)
			Voltage Regulator BK I(70)
			Special NOC RD I(51)
Circuit Layout	SD I(62)	a) 8.5	P.O. Circuit/Device Implementation SD I(60)
		b) 8.4	P.O. Poor Design P I(55)
			P.O. Causes of Failure P I(49)
			P.O. Failure Analysis Studies P I(00)
Circuit Metalliza-tion Materials	BK II(00)	8.3	Considered under Functional Elements*
			P.O. Device Element Materials BK II(26)
			Includes:
			Aluminum BK II(01)
			Chromium BK II(02)
			Copper BK II(03)
			Gold BK II(04)
			Nickel BK II(05)

Combination	Y I(95)	8.10	Considered under Accelerated Life Test Domain*
			P.O. Accelerated Life Test Y I(87)
			P.O. Part Level Data Y I(00)
Combination	Y I(81)	8.10	Considered under Step Stress Test Domain*
			P.O. Step Stress Test Y I(73)
			P.O. Part Level Data Y I(00)
Combination and NOC	OR I(56)	8.11	Considered under Equipment Class*
			Considered under Applications
Combination with Environment Stress	Y I(55)	8.10	Considered under Intermittent Stress Domain*
			P.O. Intermittent Life Test Y I(50)
			P.O. Part Level Data Y I(00)
Commercial/Industrial			See Industrial/Commercial
Common Mode Rejection Ratio	GY I(88)	8.3	P.O. Circuit Parameters GY I(86)
Communications	OR I(57)	8.10	Considered under Equipment Class*
			Considered under Applications
Comparison with Discrete	OR I(81)	8.10	P.O. Application Design Techniques and Considerations OR I(79)
			Considered under Applications
Compatible Monolithic*			See Composite IC NOC
Complementary Transistor	GN I(11)	8.3	P.O. Transistors GN I(09)
			P.O. Circuit Component GN I(00)
			Considered under MEL Device Element Descriptor*
Composite IC, NOC (Compatible Monolithic*, Monobrid*, Active Substrate IC*)	RD I(00)	8.1	Considered under Microelectronic Category*

Composite IC, Diffused	RD I(01)		8.1	Considered under Microelectronic Category*
Composite IC, Epitaxial	RD I(02)		8.1	Considered under Microelectronic Category*
Compounds III-VI (Al_2O_3, Ga_2O_3, In_2O_3)	BK II(98)		8.3	Considered under Materials NOC* Considered under Functional Elements* P.O. Device Element Materials BK II(26)
Compounds II-VI (BeO, MgO, ZnO, BaO, HgS, BaS, ZnS, CdS, CdSe, ZnSe, BaSe, HgSe, CdTe, ZnTe, BaTe, HgTe)	BK II(32)		8.3	P.O. Materials NOC BK II (13) Considered under Functional Element* P.O. Device Element Materials BK II(26)
Compounds III-V (BN, BP, AlAs, AlSb, GaN, GaP, GaAs, GaSb, InP, InAs, InSb)	BK II(33)		8.3	P.O. Materials NOC BK II(13) Considered under Functional Elements* P.O. Device Element Materials BK II(26)
Compounds IV-VI (SiO, SiO_2, TiO_2, ZrO_2, SnO_2, HfO_2, PbO, PbS, PbSe, PbTe)	BK II(34)		8.3	P.O. Materials NOC BK II(13) Considered under Functional Elements* P.O. Device Element Materials BK II(26)
Compounds IV-IV (Silicon Carbide)	BK II(35)		8.3	P.O. Materials NOC BK II(13) Considered under Functional Elements* P.O. Device Element Materials BK II(26)
Compound Formation	SD I(02)	a)	8.4	P.O. Failure Phenomena SD I(78) P.O. Failure Analysis Studies P I(00)
		b)	8.5	P.O. Chemical Phenomena SD I(01) P.O. Circuit Device Theory SD I(00)
Computation (Digital Processors)	OR I(58)		8.11	Considered under Equipment Class* Considered under Applications

Computer Aids	SD I(63)	8.5	P.O. Circuit/Device Implementation SD I(60) Includes: Layout SD I(64) LSI Interconnection Design SD I(65) Mask Design SD I(66)
Computer Analysis	SD I(72)	8.5	P.O. Functional/Circuit Design and Optimization SD I(71)
Confidential	BL I(14)	8.4	P.O. Classified BL I(13) Considered under Report Security Classification*
Constant Acceleration (Centrifuge*)	GY I(26)	8.10	P.O. Environmental Condition GY I(24) P.O. Part Level Data Y (00)
Consumer	RD I(59)	8.1	Considered under Qualification Class*
Contact Area	GN I(60)	8.3	Considered under Circuit Component Regions* Considered under MEL Device Element Descriptor*
Contact Potential	SD I(12)	8.5	P.O. Physical Parameters SD I(07) P.O. Circuit/Device Theory SD I(00)
Contamination	P I(72)	8.6	P.O. Physical Defects P I(70) P.O. Failure Analysis Studies P I(00)
Control	OR I(59)	8.11	Considered under Equipment Class* Considered under Applications
Conventional Microscopic Examination	P I(03)	8.6	P.O. Failure Analysis Techniques P I(01) P.O. Failure Analysis Studies P I(00)
Converter	P I(03)		See A/D, or D/A converter

Copper	BK II(66)	8.3	P.O. Package Terminal Material BK II(64) Considered under Non-Functional Element* P.O. Device Element Materials BK II(26) P.O. Copper (All) GY I(82)
Copper	BK II(03)	8.3	P.O. Circuit Metallization Materials BK II(00) Considered under Non-Functional Elements* P.O. Device Element Materials BK II(26) P.O. Copper (All) GY I(82)
Copper (All)	GY I(82)	8.3	Unqualified terms
Corrective Measures	OR I(89)	8.6	P.O. Failure Analysis Studies P I(00) Includes: Final Inspection OR I(90) Inprocess Inspection Procedures OR I(91) Materials Control OR I(92) Post-Production Screens OR I(93) Process Control OR I(94) Process Equipment Improvement OR I(95) Process Improvement OR I(96) Procurement Specification OR I(97) Quality Assurance Measures OR I(98) Redesign OR I(99)
Counters	BK I(55)	8.3	P.O. Circuit Functions BK I(49)
Countersigned by Responsible Report Source Official	BL I(45)	8.4	Considered under Data Validation*

Term	Code			Relation
Cracked Die	P I(73)		8.6	P.O. Physical Defects P I(70)
				P.O. Failure Analysis Studies P I(00)
Cracked Package	P I(74)		8.6	P.O. Physical Defects P I(70)
				P.O. Failure Analysis Studies P I(00)
Crossover	GN I(61)		8.3	Considered under Circuit Component Regions*
				Considered under MEL Device Element Descriptor*
Cryotron	GN I(50)		8.3	P.O. Special Active Devices NOC GN I(48)
				P.O. Circuit Component GN I(00)
				Considered under MEL Device Element Descriptor*
Crystal Defects	P I(75)		8.6	P.O. Physical Defects P I(70)
				P.O. Failure Analysis Studies P I(00)
Crystal Degradation by Radiation	SD I(81)		8.6	P.O. Failure Phenomena SD I(78)
				P.O. Failure Analysis Studies P I(00)
Crystal Growth	W I(02)	a)	8.7	P.O. Material Preparation W I(01)
				P.O. Fabrication Techniques and Equipment W I(00)
		b)	8.5	P.O. Metallurgical Phenomena SD I(53)
				P.O. Circuit/Device Theory SD I(00)
CTL	RD I(15)		8.1	P.O. Digital Logic RD I(13)
				Considered under Operational Type*
Current (All)	GY I(83)		8.8	Unqualified terms
Current	Y I(89)		8.10	Considered under Accelerated Life Test Domain*
				P.O. Accelerated Life Test Y I(87)
				P.O. Part Level Data Y I(00)
				P.O. Current (All) GY I(83)

Current	Y I(51)	8.10	Considered under Intermittent Stress Domain* P.O. Intermittent Life Test Y I(50) P.O. Part Level Data Y I(00) P.O. Current (All) GY I(83)
Current	Y I(75)	8.10	Considered under Step Stress Test Domain* P.O. Step Stress Test Y I(73) P.O. Part Level Data Y I(00) P.O. Current (All) GY I(83)
Current Transfer Ratio (Beta)	GY I(95)	8.3	P.O. Device Parameters GY I(93)
D/A Converter	BK I(56)	8.3	P.O. Circuit Functions BK I(49)
Data Collection and Reduction	OR I(23)	8.9	P.O. Reliability Technology OR I(00) Includes: Automated Systems OR I(24) Data Merging OR I(25) Manual Systems OR I(26)
Data Merging	OR I(25)	8.9	P.O. Data Collection and Reduction OR I(23) P.O. Reliability Technology OR I(00)
Data Systems Specifications	W I(75)	8.8	Specifications
Data Validation*		8.4	See: Certified BL I(42) Not Certified BL I(41) Activity Monitored by Source-Sponsor Representative BL I(43) Activity Witnessed and Report Countersigned by Source-Sponsor Agent BL I(44) Countersigned by Responsible Report-Source Official BL I(45)

Term	Code		Cross-reference
Data Validation (cont'd)			See (cont'd)
			Facility Approved by Source-Sponsor Representative BL I(46)
			Procedure Approved by Source-Sponsor BL I(47)
			Test Equipment/Procedures Approved by Non-Resident Source-Sponsor Representative BL I(48)
			Test Equipment/Procedures Approved by Resident Source-Sponsor Agent BL I(49)
DCTL	RD I(16)	8.1	P.O. Digital Logic RD I(13)
			Considered under Operational Type*
Decomposition	SD I(03)	8.5	P.O. Chemical Phenomena SD I(01)
			P.O. Circuit/Device Theory SD I(00)
Defective Bond	P I(76)	8.6	P.O. Physical Defects P I(70)
			P.O. Failure Analysis Studies P I(00)
Defects			See Physical Defects
Depletion	SD I(29)	8.5	P.O. Physical Phenomena SD I(23)
			P.O. Circuit/Device Theory SD I(00)
Deposition	W I(22)	8.7	P.O. Fabrication Techniques and Equipment W I(00)
			Includes:
			Thick Film W I(23)
			Thin Film W I(26)
Deposition Rate Monitoring	W I(57)	8.7	P.O. Process Control Technique W I(55)
			P.O. Fabrication Techniques and Equipment W I(00)
Design Considerations	SD I(73)	8.5	P.O. Functional/Circuit Design and Optimization SD I(71)
Design of Experiments	OR I(18)	8.9	P.O. Statistical Tools OR I(15)
			P.O. Reliability Technology OR I(00)

Developing	W I(15)		8.7	P.O. Photolithography W I(14)
				P.O. Fabrication Techniques and Equipment W I(00)
Developmental	BK I(96)	a)	8.11	Considered under Application Status*
				Considered under Applications
		b)	8.3	Considered under Item Status*
		c)	8.10	Considered under Test Type*
				P.O. Part Level Data Y I(00)
Device Element Material	BK II(26)		8.3	Includes:
				Functional Elements*
				Non-Functional Elements*
Device Geometry	SD I(67)	a)	8.6	P.O. Poor Design P I(55)
				P.O. Causes of Failure P I(49)
				P.O. Failure Analysis Studies P I(00)
		b)	8.5	P.O. Circuit/Device Implementation SD I(60)
Device Manufacturer	BL I(36)		8.4	Considered under Sponsoring Organization*
Device Manufacturer	BL I(25)		8.4	Considered under Report Source*
				See Manufacturer for listing and codes
Device Mishandling	P I(52)		8.6	P.O. Misapplication P I(51)
				P.O. Causes of Failures P I(49)
				P.O. Failure Analysis Studies P I(00)
Device Parameters	GY I(93)		8.3	Includes:
				Capacitance GY I(94)
				Current Transfer Ratio (Beta) GY I(95)
				Inductance GY I(96)
				Resistivity GY I(97)
				Transconductance GY I(98)

Device User	BL I(37)	8.4	Considered under Sponsoring Organization*
Device User	BL I(26)	8.4	Considered under Report Source*

Includes:

A.C. Electronics (01) SD I(58)
SD I(91)

Autonetics (02) SD I(58)
SD I(92)

Avco (03) SD I(58)
SD I(93)

Bendix (04) SD I(58)
SD I(94)

Boeing (05) SD I(58)
SD I(95)

Burroughs (06) SD I(58)
SD I(96)

General Electric (07) SD I(58)
SD I(97)

Honeywell (08) SD I(58)
SD I(98)

Martin-Marietta (09) SD I(58)
SD I(99)

Motorola (10) SD I(59)
SD I(05)

Norden (11) SD I(59)
SD I(91)

Sanders (12) SD I(59)
SD I(92)

Sperry Gyroscope (13) SD I(59)
SD I(93)

Sylvania (14) SD I(59)
SD I(94)

Teledyne (15) SD I(59)
SD I(95)

DIAC (Bilateral Diode Switch*)	GN I(02)	8.3	P.O. PNPN Devices GN I(01) P.O. Circuit Component GN I(00) Considered under MEL Device Element Descriptors*
Dicing*			See Breaking
Die Bonding	W I(32)	8.7	P.O. Assembly W I(30) P.O. Fabrication Techniques and Equipment W I(00) Includes: Eutectic Braze W I(33) Glass Frit BK II(59) Solder GN I(96) Die Bonding NOC W I(36)
Die Bonding NOC	W I(36)	8.7	P.O. Die Bonding W I(32) P.O. Assembly W I(30) P.O. Fabrication Techniques and Equipment W I(00)
Die Bond Material	BK II(58)	8.3	Considered under Non-Functional Elements* P.O. Device Element Materials BK II(26) Includes: Glass Frit BK II(59) Gold Germanium Eutectic BK II(60) Gold Silicon Eutectic BK II(61) Solder GN I(96) Die Bond Material NOC BK II(63)
Die Bond Material NOC	BK II(63)	8.3	P.O. Die Bond Material BK II(58) Considered under Non-Functional Elements* P.O. Device Element Material BK II(26)

Term	Code		Reference
Dielectric, Air (Beam Lead*)	RD I(35)	8.1	P.O. Isolation Method RD I(34)
Dielectric, Ceramic	RD I(36)	8.1	P.O. Isolation Method RD I(34)
Dielectric, Glass	RD I(37)	8.1	P.O. Isolation Method RD I(34)
Dielectric, Nitride	RD I(38)	8.1	P.O. Isolation Method RD I(34)
Dielectric, Oxide	RD I(39)	8.1	P.O. Isolation Method RD I(34)
Dielectric, NOC	RD I(40)	8.1	P.O. Isolation Method RD I(34)
Dielectric and Insulating Materials	BK II(08)	8.3	Considered under Functional Elements* P.O. Device Element Materials BK II(26) Includes: Air BK II(09) Alumina BK II(47) Hafnium Dioxide BK II(11) Silicon Carbide BK II(12) Silicon Nitride BK II(55) Silicon Oxide (SiO or SiO_2) BK II(56) Tantalum Oxide BK II(15) Titanium Dioxide BK II(16) Dielectrics and Insulating Material NOC BK II(17)
Dielectric and Insulating Materials NOC	BK II(17)	8.3	P.O. Dielectric and Insulating Materials BK II(08) Considered under Functional Element* P.O. Device Element Materials BK II(26)

Die Size		8.3	Considered under MEL Device Element Descriptor* Includes: GN I(73) <30 mils/side (<900 sq. mils) GN I(74) 31-42 mils/side (900-1800 sq. mils) GN I(75) 43-60 mils/side (1800-3600 sq. mils) GN I(76) 61-85 mils/side (3600-7200 sq. mils) GN I(77) 86-120 mils/side (7200-14,400 sq. mils) GN I(78) 121-170 mils/side (14,400-28,800 sq. mils) GN I(79) 171-240 mils/side (28,800-57,680 sq. mils) GN I(80) >240 mils/side (57,680 sq. mils)
Differential	RD I(24)	8.1	P.O. Linear Device RD I(23) Considered under Operational Type*
Differential Amplifier	RD I(45)	8.[illegible]	Considered under Circuit Complexity*
		8.3	P.O. Circuit Functions BK I(49)
Diffused Composite IC			See Composite IC, Diffused
Diffused Junction	GN I(25)	a) 8.3	Considered under Circuit Component Regions* Considered under MEL Device Element Descriptor*
		b) 8.3	P.O. Capacitor GN I(24) P.O. Circuit Component GN I(00) Considered under MEL Device Element Descriptor*
Diffused Monolithic			See Composite, Monolithic

Diffused Resistor	GN I(43)	8.3	P.O. Resistor GN I(42) P.O. Circuit Component GN I(00) Considered under MEL Device Element Descriptor*
Diffusion	W I(11)	8.7	P.O. Junction Formation W I(09) P.O. Fabrication Techniques and Equipment W I(00)
Diffusion Coefficient	SD I(13)	8.5	P.O. Physical Parameters SD I(07) P.O. Circuit/Device Theory SD I(00)
Diffusion Defects	P I(77)	8.6	P.O. Physical Defects P I(70) P.O. Failure Analysis Studies P I(00)
Diffusion Length	SD I(14)	8.5	P.O. Physical Parameters SD I(07) P.O. Circuit/Device Theory SD I(00)
Digital	RD I(11)	8.1	Considered under Functional Category*
Digital Logic	RD I(13)	8.1	Considered under Operational Type* Includes: CML (ECL*, MECL*, ECCSL*) RD I(14) CTL RD I(15) DCTL RD I(16) DTL RD I(17) MOSTL RD I(18) RCTL RD I(19) RTL RD I(20) TTL (T^2L*) RD I(21) Digital Logic NOC RD I(22)
Digital Logic NOC	RD I(22)	8.1	P.O. Digital Logic RD I(13) Considered under Operational Type*

Diode	GN I(30)	8 3	P.O. Circuit Component GN I(00) Considered under MEL Device Element Descriptor* Includes: Avalanche Diode GN I(31) General Purpose Diode - Junction GN I(32) Gunn Effect Diode GN I(33) Micro-Diode, Discrete GN I(34) Schottkey Barrier Diode GN I(35) Tunnel Diode GN I(36) Voltage Regulator BK I(70)
Disappearance of Metallization	SD I(82)	8 6	P.O. Failure Phenomena SD I(78) P.O. Failure Analysis Studies P I(00)
Discrete Capacitor	GN I(26)	8 3	P.O. Capacitor GN I(24) P.O. Circuit Component GN I(00) Considered under MEL Device Element Descriptor*
Discrete Microcomponent	GN I(52)	8 3	P.O. Circuit Component GN I(00) Considered under MEL Device Element Descriptor*
Discrete Resistor	GN I(44)	8.3	P.O. Resistor GN I(42) P.O. Circuit Component GN I(00) Considered under MEL Device Element Descriptor*
Dissection and Sectioning	P I(04)	8.4	P.O. Failure Analysis Techniques P I(01) P.O. Failure Analysis Studies P I(00)

Distributed Passive Devices	GN I(37)	8.3	P.O. Circuit Component GN I(00)
			Considered under MEL Device Element Descriptor*
			Includes:
			Strip Line Filters GN I(38)
			Terminators GN I(39)
Document Format*		8.4	See:
			Audio-Video Tape Recording BL I(70)
			Hard Copy Document BL I(71)
			Machine Printout BL I(72)
			Machine Sensible Format BL I(73)
			Microfiche BL I(74)
			Microfilm BL I(75)
			Slide BL I(76)
DOD	BL I(22)	7.4	P.O. Military and Space BL I(19)
			Considered under Report Source*
DOD	BL I(33)	8.4	P.O. Military and Space BL I(30)
			Considered under Sponsoring Organization*
Dopant Materials	BK II(18)	83	Considered under Functional Elements*
			P.O. Device Element Materials BK II(26)
			Includes:
			Aluminum BK II(19)
			Antimony BK II(20)
			Arsenic BK II(21)
			Boron BK II(22)
			Gallium BK II(10)
			Gold BK II(23)
			Phosphorous BK II(24)
			Dopant Materials NOC BK II(25)

Dopant Materials NOC	BK II(25)	8.3	P.O. Dopant Materials BK II(18) Considered under Functional Elements* [illegible] O. Device Element Materials [illegible] II(26)
Drain	GN I(63)	8.3	Considered under Circuit Component Regions* Considered under MEL Device Element Descriptors*
Drawings	BL I(52)	8.4	Considered under Report Type*
DTL	RD I(17)	8.1	P.O. Digital Logic RD I(13) Considered under Operational Type*
Dual Inline, 10 lead	BK II(92)	8.3	P.O. Package Type BK II(81)
Dual Inline, 14 l[illegible]d	BK II(93)	8.3	P.O. Package Type BK II(81)
Dual Inline, Hermetically Sealed	RD I(53)	8.1	Considered under Package Configuration*
Dual Inline, Plastic (DIP*)	RD I(54)	8.1	Considered under Package Configuration*
Dual Inline, NOC	BK II(94)	8.3	P.O. Package Type BK II(81)
ECCSL*			See CML
ECL*			See CML
Economic Factors	OR I(82)	8.11	P.O. Application Design Techniques and Considerations OR I(79) Considered under Applications
Economics*		8.12	Other NOC
Electrical Characterization	P I(05)	8.4	P.O. Failure Analysis Techniques P I(01) P.O. Failure Analysis Studies P I(00)
		8.5	P.O. Testing SD I(70) P.O. Circuit/Device Implementation SD I(60)

Term	Code	Section	Relationships
Electrical Conduction	SD I(30)	8.5	P.O. Physical Phenomena SD I(23) P.O. Circuit/Device Theory SD I(00)
Electrical Noise Generation	SD I(31)	8.5	P.O. Physical Phenomena SD I(23) P.O. Circuit/Device Theory SD I(00)
Electrical Properties*		8.3	See: Gain (Typical) Maximum Fan-Out Maximum Frequency of Operation Maximum Output Power Maximum Power Dissipation Output Impedance (Typical) Propagation Delay (Max.)
Electrodes	GN I(64)	8.3	Considered under Circuit Component Regions* Considered under MEL Device Element Descriptors*
Electroluminesence/ Radiation Emission			See Radiation Emission/Electroluminesence
Electrolytic Corrosion	SD I(83)	8.4	P.O. Failure Phenomena SD I(78) P.O. Failure Analysis Studies P I(00)
Electromagnetic and Particle Radiation	GY I(27)	8.10	P.O. Environmental Condition GY I(24) P.O. Part Level Data Y I(00)
Electron Microprobe	P I(06)	8.6	P.O. Failure Analysis Techniques P I(01) P.O. Failure Analysis Studies P I(00)
Electron Microscopic Examination	P I(07)	8.6	P.O. Failure Analysis Techniques P I(01) P.O. Failure Analysis Studies P I(00)
Electron Spin	SD I(32)	8.5	P.O. Physical Phenomena SD I(23) P.O. Circuit/Device Theory SD I(00)

Emitter	GN I(65)	8.3	Considered under Circuit Component Regions*
			Considered under MEL Device Element Descriptors*
Emitter, Multiple			See Multiple Emitter
Encapsulated Plastic			See Plastic Encapsulated
Encapsulation/ Package Sealing	W I(39)	8.7	P.O. Fabrication Techniques and Equipment W I(00)
			Includes:
			Glass-to-Glass Seal BK I(91)
			Glass-to-Metal Seal BK I(92)
			Molded BK I(93)
			Seam Weld BK I(94)
Energy Gap	SD I(15)	8.5	P.O. Physical Parameters SD I(07)
			P.O. Circuit/Device Theory SD I(00)
Energy Level	SD I(16)	8.5	P.O. Physical Parameters SD I(07)
			P.O. Circuit/Device Theory SD I(00)
Enhancement	SD I(33)	8.5	P.O. Physical Phenomena SD I(23)
			P.O. Circuit/Device Theory SD I(00)
Environmental	OR I(83)	8.11	P.O. Application Design Techniques and Considerations OR I(79)
			Considered under Applications
Environmental Capabilities*		8.3	See:
			Maximum Operating Temperature
			Minimum Operating Temperature
			Maximum Storage Temperature
			Minimum Storage Temperature
			Reliability Rating

Environmental Condition	GY I(24)	8.10	P.O. Part Level Data Y I(00) Includes: Acoustic Noise GY I(25) Constant Acceleration (Centrifuge*) GY I(26) Electromagnetic & Particle Radiation GY I(27) Humidity GY I(28) Immersion GY I(29) Low Barometric Pressure GY I(30) Mechanical Shock GY I(31) Moisture Resistance GY I(32) RF Interference GY I(33) Salt Atmosphere/Spray P I(42) Soldering Heat GY I(36) Temperature Cycling GY I(37) Terminal Strength (Lead Pull) GY I(38) Thermal Shock P I(46) Vibration, Fatigue GY I(40) Vibration, Random GY I(41) Vibration, Variable Frequency GY I(42)
Epitaxial Composite IC			See Composite IC, Epitaxial
Epitaxial Junction	GN I(66)	8.3	Considered under Circuit Component Region* Considered under MEL Device Element Descriptors*
Epitaxial Layer	GN I(67)	8.3	Considered under Circuit Component Region* Considered under MEL Device Element Descriptors*

Epitaxial, Monolithic			See Monolithic, Epitaxial
Epitaxy	W I(12)	8.7	P.O. Junction Formation W I(09)
			P.O. Fabrication Techniques and Equipment W I(00)
Epitaxy Defects	P I(78)	8.4	P.O. Physical Defects P I(70)
			P.O. Failure Analysis Studies P I(00)
Equipment	BL I(62)	8.4	P.O. Survey and Review BL I(59)
			Considered under Report Type*
Equipment Application	OR I(84)	8.11	P.O. Application Design Techniques and Considerations OR I(79)
			Considered under Applications
Equipment Class*		8.11	Considered under Applications
			See:
			Communications OR I(57)
			Computation (Digital Processors) OR I(58)
			Control OR I(59)
			Instrumentation and Display OR I(60)
			Navigation OR I(61)
			Power (Power Supplies) OR I(62)
			Radar OR I(63)
			Signal Processing (Buffers, Converters, Amplifiers) OR I(64)
			Unspecified OR I(65)
			Combination and NOC OR I(56)
Equipment System Level Specifications	W I(76)	8.8	Considered under Specifications

Term	Code			Relationship
Erroneous Lead Positioning	P I(53)		8.6	P.O. Misapplication P I(51)
				P.O. Causes of Failures P I(49)
				P.O. Failure Analysis Studies P I(00)
Etching	W I(20)	a	8.5	P.O. Chemical Phenomena SD I(01)
				P.O. Circuit/Device Theory SD I(00)
		b	8.7	P.O. Fabrication Techniques and Equipment W I(00)
Eutectic Braze	W I(33)		8.7	P.O. Die Bonding W I(32)
				P.O. Assembly W I(30)
				P.O. Fabrication Techniques and Equipment W I(00)
Excessive Lead Length	P I(62)		8.6	P.O. Workmanship Defects P I(61)
				P.O. Causes of Failures P I(49)
				P.O. Failure Analysis Studies P I(00)
Experimental	BK I(97)		8.3	Considered under Item Status*
Experimental				See Developmental Test Type
Exponential Distribution	OR I(19)		8.9	P.O. Statistical Tools OR I(15)
				P.O. Reliability Technology OR I(00)
Exposure	W I(16)		8.7	P.O. Photolithography W I(14)
				P.O. Fabrication Techniques and Equipment W I(00)
F-111	GY I(53)		8.3	Considered under Major Systems*
Fabrication Technique and Equipment	W I(00)		8.7	Includes:
				Assembly W I(30)
				Deposition W I(22)
				Encapsulation/Package Sealing W I(39)
				Etching W I(20)
				Junction Formation W I(09)

Fabrication Technique and Equipment (cont'd)			Includes: (cont'd) Lead Attachment Processes and Equipment W I(50) Material Preparation W I(01) Oxidation W I(13) Photolithography W I(14) Process Control Techniques W I(55) Process Effectiveness W I(53) Surface Passivation W I(21) Wafer Preparation W I(04) MOS Processes NOC W I(61)
Facilities	OR I(27)	8.9	P.O. Reliability Technology OR I(00) Includes: Inspection OR I(28) Performance Measurement OR I(29) Reliability and Environmental Test OR I(30)
Facility Approved by Source-Sponsor Representative	BL I(46)	8.4	Considered under Data Validation*
Factory Checkout	OR I(67)	8.11	Considered under Application Status* Considered under Applications
Failure Analysis Facilities	SD I(85)	8.6	P.O. Failure Analysis Studies P I(00)
Failure Analysis Results	GY I(46)	8.16	P.O. Test Results GY I(43) P.O. Part Level Data Y I(00)
Failure Analysis Studies	P I(00)	8.6	Includes: Causes of Failure P I(49) Corrective Measures OR I(89) Failure Analysis Facilities SD I(85)

Failure Analysis Studies (cont'd)

Includes (cont'd)

- Failure Analysis Techniques P I(01)
- Failure Environment P I(18)
- Failure Mode P I(27)
- Failure Phenomena SD I(78)
- Failure Stress Domain P I(33)
- Physical Defects P I(70)

Failure Analysis Techniques P I(01)

P.O. Failure Analysis Studies P I(00)

Includes:

- Chemical Analysis P I(02)
- Conventional Microscopic Examination P I(03)
- Dissection and Sectioning P I(04)
- Electrical Characterization P I(05)
- Electron Microprobe P I(06)
- Electron Microscopic Examination P I(07)
- Holographic Examination (use of Holograms) P I(08)
- IR Thermal Mapping P I(09)
- Non-Destructive Evaluation P I(10)
- Photochromic Paints P I(11)
- Photoresponse Mapping P I(12)
- Spectrographic Analysis P I(13)
- Sub-Optical Electromagnetic Energization (Non-IR) P I(14)
- Ultrasonic Inspection P I(15)
- Visual Inspection P I(16)
- X-Ray Evaluation P I(17)

Term	Code		Category
Failure Environment	P I(18)	8.6	P.O. Failure Analysis Studies P I(00)
			Includes:
			Application Tests, Inplant P I(19)
			Application Tests, Onsite P I(20)
			Assembly/Installation P I(21)
			Field Use P I(22)
			Laboratory Environmental Test P I(23)
			Laboratory Life Test P I(24)
			Post Production Screen/Burn-In P I(25)
			Product Inspection P I(26)
Failure Modes	OR I(74)	8.11	P.O. Reliability Data OR I(72)
			Considered under Applications
Failure Mode	P I(27)	86	P.O. Failure Analysis Studies P I(00)
			Includes:
			Functional Degradation P I(28)
			Inspection Specification Deviation P I(29)
			Open Circuit P I(30)
			Package Failure P I(31)
			Short Circuit P I(32)
Failure Phenomena	SD I(78)	86	P.O. Failure Analysis Studies P I(00)
			Includes:
			Carrier Generation through Radiation SD I(79)
			Compound Formation SD I(02)
			Crystal Degradation by Radiation SD I(81)
			Disappearance of Metallization SD I(82)

Term	Code		Related Terms
Failure Phenomena (cont'd)			Includes (cont'd)
			Electrolytic Corrosion SD I(83)
			Inversion and Channeling SD I(39)
			Ion Migration SD I(40)
			Lead Fatigue SD I(86)
			Metallurgical Diffusion SD I(87)
			Plague Formation SD I(88)
			PNPN Latch-up SD I(89)
			Secondary Breakdown SD I(90)
Failure Rate			See Reliability Rating (Max./Min/ Failure Rate)
Failure Rate Statistics	OR I(75)	4,11	P.O. Reliability Data OR I(72)
			Considered under Applications
Failure Stress Domain	P I(33)	7,8	P.O. Failure Analysis Studies P I(00)
			Includes:
			Acceleration, Constant P I(34)
			Liquid Immersion P I(35)
			Mechanical Shock P I(36)
			Moisture or Humidity P I(37)
			Noise, Accoustical P I(38)
			Pressure - Gas P I(39)
			Radiation, Electromagnetic P I(40)
			Radiation Exposure (particle) P I(41)
			Salt Atmosphere/Spray P I(42)
			Sand and Dust P I(43)
			Temperature $\leq$-42.5°C P I(45)
			Temperature $\geq$102.5°C P I(44)
			Thermal Shock P I(45)

Term	Code		Relationship
Failure Stress Domain (cont'd			Includes (cont'd)
			Vacuum P I(47)
			Vibration P I(48)
Fairchild Semiconductor	RD I(63)	a) 8.2	Considered under Manufacturer
	RD I(68)	b) 8.4	
		b) 8.4	P.O. Device Manufacturer BL I(25)
			Considered under Report Source*
Fatigue	SD I(54)	8.5	P.O. Metallurgical Phenomena SD I(53)
			P.O. Circuit/Device Theory SD I(00)
Faults and Dislocations	SD I(34)	8.5	P.O. Physical Phenomena SD I(23)
			P.O. Circuit/Device Theory SD I(00)
Fermi Level	SD I(17)	8.5	P.O. Physical Parameters SD I(07)
			P.O. Circuit/Device Theory SD I(00)
Ferrites	BK II(36)	8.3	P.O. Materials NOC BK II(13)
			Considered under Functional Elements*
			P.O. Device Element Materials BK II(26)
Ferroelectricity	SD I(35)	8.5	P.O. Physical Phenomena SD I(23)
			P.O. Circuit/Device Theory SD I(00)
Ferroelectrics	BK II(37)	8.3	P.O. Materials NOC BK II(13)
			Considered under Functional Elements*
			P.O. Device Element Materials BK II(26)
FET (Field Effect Transistor*)	GN I(12)	8.3	P.O. Transistors GN I(09)
			P.O. Circuit Components GN I(00)
			Considered under MEL Device Element Descriptors*
			Includes:
			IGFET (insulated Gate Field Transistor*) GN I(13)
			JFET (Junction Field Effect Transistor*) GN I(16)

Field Effect	SD I(36)	8.5	P.O. Physical Phenomena SD I(23)
			P.O. Circuit/Device Theory SD I(00)
Field Effect Transistor*			See FET
Field Operations	OR I(68)	8.11	Considered under Application Status*
			Considered under Applications
Field Testing (e.g. Category II & III)	OR I(69)	8.11	Considered under Application Status*
			Considered under Applications
Field Use	P I(22)	8.6	P.O. Failure Environment P I(18)
			P.O. Failure Analysis Studies P I(00)
File Entry Date		8.4	Includes:

BL I(83) 1968

BL I(84) 1969

BL I(85)

BL I(86)

BL I(87)

BL I(88) Jan.

BL I(89) Feb.

BL I(90) Mar.

BL I(91) Apr.

BL I(92) May

BL I(93) June

BL I(94) July

BL I(95) Aug.

BL I(96) Sept.

BL I(97) Oct.

BL I(98) Nov.

BL I(99) Dec.

Term	Code			Entry
Film	GN I(27)	a)	8.3	P.O. Capacitor GN I(24)
				P.O. Circuit Component GN I(00)
				Considered under MEL Device Element Descriptors*
		b)	8.3	P.O. Inductor GN I(40)
				P.O. Circuit Component GN I(00)
				Considered under MEL Device Element Descriptors*
		c)	8.3	P.O. Resistor GN I(42)
				P.O. Circuit Component GN I(00)
				Considered under MEL Device Element Descriptors*
		8.3		P.O. either Thin Film W I(26) or Thick Film W I(23
				P.O. Deposition W I(22)
				P.O. Fabrication Techniques and Equipment W I(00)
Film Thickness Defect	P I(73)		8.6	P.O. Physical Defects P I(70)
				P.O. Failure Analysis Studies P I(00)
Final Inspection	OR I(90)		8.6	P.O. Corrective Measures OR I(89)
				P.O. Failure Analysis Studies P I(00)
Fixed Ground Environment				See Ground, fixed
Flat Pack, Ceramic	RD I(55)		8.1	Considered under Package Configuration*
Flat Pack, Glass	RD I(56)		8.1	Considered under Package Configuration*
Flip-Chip*				See Inverted, Face Down
Flip-Chip, gold-to-gold				See Gold-to-Gold Direct
Flip-Flops*			8.3	See Bistable Multivibrators BK II(54)

Term	Code		Relations
Flush (metallized)	RD I(96)	8.3	P.O. Internal Connection Mode RD I(93)
Flying Leads	RD I(97)	8.3	P.O. Internal Connection Mode RD I(93)
Foreign Material	P I(80)	8.4	P.O. Physical Defects P I(70) P.O. Failure Analysis Studies P I(00)
Fully IC*			See Monclithic NOC
Functional Category*		8.1	See: Digital RD I(11) Linear (Analog*) RD I(12)
Functional/Circuit Design & Optimization	SD I(71)	8.5	Includes: Computer Analysis SD I(72) Design Considerations SD I(73) Functional Synthesis SD I(74) Test Pattern SD I(75) Toierances SD I(76) Trade-Offs SD I(77)
Functional Degradation	P I(28)	8.4	P.O. Failure Mode P I(27) P.O. Failure Analysis Studies P I(00)
Functional Elements*		8.3	P.O. Device Element Material BK II(26) Includes: Circuit Metallization Materials BK II(30) Dielectric and Insulating Materials BK II(08) Dopant Materials BK II(18) Wire Material BK II(27) Materials NOC BK II(13)
Functional Synthesis	SD I(74)	8.5	P.O. Functional/Dircuit Design & Optimization SD I(71)

Term	Code		Notes
Gain (Typical)		8.3	Considered under Electrical Properties*
			BK I(18) Less than 40 db
			BK I(19) 40 thru 80 db
			BK I(20) Greater than 80 db
Gain	GY I(89)	8.3	P.O. Circuit Parameters GY I(86)
Gallium	BK II(10)	8.3	P.O. Dopant Materials BK II(18)
			Considered under Functional Elements*
			P.O. Device Element Materials BK II(26)
Gate			See AND Gate, NAND Gate, NOR Gate, OR Gate
Gate (Logic Gate)	RD I(46)	8.1	Considered under Circuit Complexity*
Gate (IGFET Type)	GN I(63)	8.3	Considered under Circuit Component Regions* (the Gate of an IGFET)
			Considered under MEL Device Element Descriptors*
Gate Expanders	BK I(57)	8.3	P.O. Circuit Functions BK I(49)
General Catalog	BL I(68)	8.4	P.O. Vendor Report BL I(67)
			Considered under Report Type*
General Electric (07)	SD I(58) SD I(97)	8.4	P.O. Device User BL I(26)
			Considered under Report Source*
General Instrument Corp. (05)	RD I(83) RD I(69)	a) 8.2	Considered under Manufacturer
		b) 8.4	P.O. Device Manufacturer BL I(25)
			Considered under Report Source*
General Methodology	OR I(01)	8.4	P.O. Reliability Technology OR I(00)
General Purpose Diode - Junction	GN I(32)	8.3	P.O. Diode GN I(30)
			P.O. Circuit Component GN I(00)
			Considered under MEL Device Element Descriptor*

Germanium	BK II(49)	a)	8.3	P.O. Substrate Materials BK II(46)
				Considered under Non-Functional Elements*
				P.O. Device Element Materials BK II(26)
Glass	RD I(89)	a)	8.3	P.O. Package Material (primary), RD I(87)
				Considered under Non-Functional Element*
				P.O. Device Element Materials BK II(26)
		b)	8.3	P.O. Substrate Materials BK II(46)
				Considered under Non-Functional Element*
				P.O. Device Element Materials BK II(26)
		c)	8.3	P.O. Surface Protection BK II(53)
				Considered under Non-Functional Element*
				P.O. Device Element Materials BK II(26)
Glass Dielectric				See Dielectric, Glass
Glass Flat Pack				See Flat Pack, Glass
Glass Frit	BK II(59)	a)	8.7	P.O. Die Bonding W I(32)
				P.O. Assembly W I(30)
				P.O. Fabrication Techniques and Equipment W I(00)
		b)	8.3	P.O. Die Bond Material BK II(58)
				Considered under Non-Functional Element*
				P.O. Device Element Materials BK II(26)
Glass-to-Glass Seal	BK I(91)	a)	8.3	P.O. Package Seal BK I(90)

Glass-to-Glass Seal (cont'd)		b)	8.7	P.O. Encapsulation/Package Sealing W I(39)
				P.O. Fabrication Techniques and Equipment W I(00)
Glass-to-Metal Seal	BK I(92)	a)	8.3	P.O. Package Seal BK I(90)
		b)	8.7	P.O. Encapsulation/Package Sealing W I(39)
				P.O. Fabrication Techniques and Equipment W I(00)
Gold (All)	GY I(84)		8.5	Unqualified term
Gold	BK II(23)		8.5	P.O. Dopant Materials BK II(18)
				Considered under Functional Element*
				P.O. Device Element Materials BK II(26)
				P.O. Gold (All) GY I(84)
Gold	BK II(04)		8.5	P.O. Circuit Metallization Materials BK II(00)
				Considered under Functional Element*
				P.O. Device Element Materials BK II(26)
				P.O. Gold (All) GY I(84)
Gold	BK II(29)		8.5	P.O. Wire Materials BK II(27)
				Considered under Functional Element*
				P.O. Device Element Materials BK II(26)
				P.O. Gold (All) GY I(84)
Gold	BK II(67)		8.5	P.O. Package Terminal Material BK II(64)
				Considered under Non-Functional Element*
				P.O. Device Element Materials BK II(26)
				P.O. Gold (All) GY I(84)

Term	Reference		Related
Gold-to-Aluminum, Direct	RD I(29)	8.1	P.O. Interconnection System RD I(26)
Gold-to-Aluminum, Wire Bond	RD I(30)	8.1	P.O. Interconnection System RD I(26)
Gold-to-Gold, Direct (gold-to-gold, inverted chip, gold-to-gold, flip chip	RD I(31)	8.1	P.O. Interconnection System RD I(26)
Gold-to-Gold, Wire Bond	RD I(32)	8.1	P.O. Interconnection System RD I(26)
Gold-to-Silicon-to Aluminum, Wire Bond		8.1	P.O. Interconnection System RD I(26)
Gold Germanium Eutectic	BK II(60)	8.3	P.O. Die Bond Material BK II(58)
			Considered under Non-Functional Element*
			P.O. Device Element Material BK II(26)
Gold Silicon Eutectic	BK II(61)	8.3	P.O. Die Bond Material BK II(58)
			Considered under Non-Functional Element*
			P.O. Device Element Material BK II(26)
Government Agency QA Specifications	W I(81)	8.8	P.O. Quality Assurance Specifications W I(80)
Ground Checkout	OR I(39)	8.11	P.O. Aircraft Environment OR I(36)
			P.O. Application Environment OR I(35)
			Considered under Applications
Ground Checkout	OR I(46)	8.11	P.O. Missile Environment OR I(45)
			P.O. Application Environment OR I(35)
			Considered under Applications
Ground Checkout	OR I(52)	8.11	P.O. Spacecraft Environment OR I(51)
			P.O. Application Environment OR I(35)
			Considered under Applications

Ground Environment	OR I(40)	P.O. Application Environment OR I(35)
		Considered under Applications
		Includes:
		Ground Fixed OR I(41)
		Ground Laboratory OR I(42)
		Ground Mobile OR I(43)
		Ground Portable OR I(44)
Ground Fixed	OR I(41)	P.O. Ground Environment OR I(40)
		P.O. Application Environment OR I(35)
		Considered under Applications
Ground Laboratory	OR I(42)	P.O. Ground Environment OR I(40)
		P.O. Application Environment OR I(35)
		Considered under Applications
Ground Mobile	OR I(43)	P.O. Ground Environment OR I(40)
		P.O. Application Environment OR I(35)
		Considered under Applications
Ground Portable	OR I(44)	P.O. Ground Environment OR I(40)
		P.O. Application Environment OR I(35)
		Considered under Applications
GTO (Gate Turn Off Switch*)	GN I(03)	P.O. PNPN Devices GN I(01)
		P.O. Circuit Component GN I(00)
		Considered under MEL Device Element Descriptor*
Gunn Effect Diode	GN I(33)	P.O. Diode GN I(30)
		P.O. Circuit Component GN I(00)
		Considered under MEL Device Element Descriptor*
Gunn Effect/Negative Resistance		See Negative Resistance/Gunn Effect

Hafnium	BK II(14)	8.3	P.O. Materials NOC BK II(13) P.O. Device Element Materials BL II(26)
Hafnium Dioxide	BK II(11)	8.3	P.O. Dielectrics and Insulating Materials BK II(08) Considered under Functional Element* P.O. Device Element Material BK II(26)
Hall Effect	SD I(37)	8.5	P.O. Physical Phenomena SD I(23) P.O. Circuit/Device Theory SD I(00)
Hard Copy Document	BL I(71)	8.4	Considered under Document Format*
Heat Capacity	SD I(18)	8.5	P.O. Physical Parameters SD I(07) P.O. Circuit/Device Theory SD I(00)
Hermetically Sealed			See Can or Dual in-line, Hermetically Sealed
High Reliability Certification (Hi-Rel Certification)	RD I(60)	8.1	Considered under Qualification Class*
High Temperature	Y I(90)	8.10	Considered under Accelerated Life Test Domain* P.O. Accelerated Life Test Y I(87) P.O. Part Level Data Y I(00)
High Temperature	Y I(76)	8.10	Considered under Step Stress Test Domain* P.O. Step Stress Test Y I(73) P.O. Part Level Data Y I(00)
Holographic Examination (use of Holograms)	P I(08)	8.6	P.O. Failure Analysis Techniques P I(01) P.O. Failure Analysis Studies P I(00)
Honeywell (08)	SD I(58 SD I(98)	8.4	P.O. Device User BL I(26) Considered under Report Source*

Humidity	GY I(28)	8.10	P.O. Environmental Conditions GY I(24)
			P.O. Part Level Data Y I(00)
Humidity			See Moisture Failure Stress Domain
Hybrid Integrated Circuit*			See Hybrid Microcircuit
Hybrid Microcircuit (Hybrid Integrated Circuit*)	RD I(03)	8.1	Considered under Microelectronic Category*
IF Amplifier	BK I(58)	8.3	P.O. Circuit Functions BK I(49)
IGFET (Insulated Gate Field Effect Transistor)	GN I(13)	8.3	P.O. Field Effect Transistor GN I(12)
			P.O. Transistors GN I(09)
			P.O. Circuit Component GN I(00)
			Considered under MEL Device Element Descriptors*
			Includes:
			MNS GN I(46)
			MOS GN I(28)
			MTOS GN I(47)
			N-Channel IGFET GN I(14)
			P-Channel IGFET GN I(15)
			SOS GN I(81)
			Thin Film GN I(82)
IITRI Generated Data Summary	BL I(54)	8.4	Considered under Report Type*
IITRI Generated Device Descriptions	BL I(53)	8.4	Considered under Report Type*
Immersion	GY I(29)	8.10	P.O. Environmental Conditions GY I(24)
			P.O. Part Level Data Y I(00)
Improper Component Alignment	P I(63)	8.6	P.O. Workmanship Defects P I(61)
			P.O. Causes of Failures P I(49)
			P.O. Failure Analysis Studies P I(00)

Term	Code		Related
Improper Etch	P I(81)	86	P.O. Physical Defect P I(70)
			P.O. Failure Analysis Studies P I(00)
Improper Mask Alignment	P I(64)	86	P.O. Workmanship Defects P I(61)
			P.O. Causes of Failures P I(49)
			P.O. Failure Analysis Studies P I(00)
Improper Package Marking	P I(65)	86	P.O. Workmanship Defects P I(61)
			P.O. Causes of Failures P I(49)
			P.O. Failure Analysis Studies P I(00)
Improper Wire Bonding	P I(66)	86	P.O. Workmanship Defects P I(61)
			P.O. Cause of Failures P I(49)
			P.O. Failure Analysis Studies P I(00)
Impurity Diffusion	SD I(38)	8.5	P.O. Physical Phenomena SD I(23)
			P.O. Circuit/Device Theory SD I(00)
Indium	BK II(38)	8.3	P.O. Materials NOC BK II(13)
			Considered under Functional Elements*
			P.O. Device Element Material BK II(26)
Inductance	GY I(96)	8.3	P.O. Device Parameters GY I(93)
Inductor	GN I(40)	83	P.O. Circuit Components GN I(00)
			Considered under MEL Device Element Descriptor*
			Includes:
			Film GN I(27)
			Simulated (i.e. gyrator) GN I(41)
Industrial/ Commercial	RD I(61)	81	Considered under Qualification Class*
Industry Associations (ASTM, IEEE)	BL I(27)	8.4	Considered under Report Source*

Term	Code		Disposition
Industry Associations (ASTM, IEEE)	BL I(38)	8.4	Considered under Sponsoring Organization*
Information Systems*		8.12	Other NOC
Inherent Material Flaws	P I(50)	8.6	P.O. Causes of Failure P I(49)
			P.O. Failure Analysis Studies P I(00)
Inprocess Inspection Procedures	OR I(91)	8.6	P.O. Corrective Measures OR I(89)
			P.O. Failure Analysis Studies P I(00)
Inspection	OR I(28)	8.9	P.O. Facilities OR I(27)
			P.O. Reliability Technology OR I(00)
Inspection Specification Deviation	P I(29)	8.6	P.O. Failure Mode P I(27)
			P.O. Failure Analysis Studies P I(00)
Insulating Materials			See Dielectrics and Insulating Materials
Instrumentation and Display	OR I(60)	8.11	Considered under Equipment Class*
			Considered under Applications
Interconnection System	RD I(26)	8.1	Includes:
			Aluminum-to-Aluminum, direct RD I(27)
			Aluminum-to-Aluminum, wire bond RD I(28)
			Gold-to-Aluminum, direct RD I(29)
			Gold-to-Aluminum, wire bond RD I(30)
			Gold-to-Gold, direct (Gold-to-Gold, inverted chip; Gold-to-Gold, flip chip) RD I(31)
			Gold-to-Gold, wire bond RD I(32)
			Gold-to-Silicon-to-Aluminum, wire bond RD I(33)

Intermittent Life Test — Y I(50)

8.1c P.O. Part Level Data Y I(00)

Includes:

- Intermittent Life Test Load Power
- Intermittent Life Test Supply Voltage
- Intermittent Life Test Temperature
- Intermittent Stress Domain*

Intermittent Life Test Load Power

8.1c P.O. Intermittent Life Test Y I(50)

P.O. Part Level Data Y I(00)

Includes:

I(69) $<$ 95% Rated

I(70) 95% to $<$ 105% Rated

I(71) 105% to $<$ 155% Rated

I(72) $\geq$ 155% Rated

Intermittent Life Test Supply Voltage

8.1c P.O. Intermittent Life Test Y I(50)

P.O. Part Level Data Y I(00)

Includes:

I(65) $<$ 95% Rated

I(66) 95% to $<$ 105% Rated

I(67) 105% to $<$ 155% Rated

I(68) $\geq$ 155% Rated

Intermittent Life Test Temperature

8.1c P.O. Intermittent Life Test Y I(50)

P.O. Part Level Data Y I(00)

Includes:

Y I(56) $<$ -82.5°C

Y I(57) -82.5°C to $<$ -42.5°C

Y I(58) -42.5°C to $<$ 21°C

Y I(59) 21°C to $<$ 31°C

Term	Code			Entries
Intermittent Life Test Temperature (cont'd)				Includes (cont'd) Y I(60 31°C to < 102.5°C Y I(61) 102.5°C to < 152.5°C Y I(62) 152.5°C to < 202.5°C Y I(63) 202.5°C to < 302.5°C Y I(64) ≥302.5°C
Intermittent Stress Domain*			8.10	P.O. Intermittent Life Test Y I(50) P.O. Part Level Data Y I(00) See: Current Y I(51) Power Y I(52) Temperature Y I(53) Voltage Y I(54) Combination with Environment Stresses Y I(55)
Internal Connection Mode	RD I(98)		8.3	Includes: Beam Lead RD I(94) Flush (metallized) RD I(96) Flying Leads RD I(97) Inverted, Face Down (lid, flip chip) RD I(95) Internal Connection Mode NOC RD I(98)
Internal Connection Mode NOC	RD I(98)		8.3	P.O. Internal Connection Mode RD I(93)
Inversion and Channeling	SD I(39)	a)	8.5	P.O. Physical Phenomena SD I(23) P.O. Circuit/Device Theory SD I(00)
		b)	8.6	P.O. Failure Phenomena SD I(78) P.O. Failure Analysis Studies P I(00)

Term	Code			Relation
Inverted Chip, Gold-to-Gold				See Gold-to-Gold
Inverted, Face Down (Lid, Flip Chip)	RD I(95)		8.3	P.O. Internal Connection Mode RD I(93)
Inverter	BK I(71)		8.3	P.O. Circuit Functions BK I(49)
Ion Migration	SD I(40)	a)	8.5	P.O. Physical Phenomena SD I(23)
				P.O. Circuit/Device Theory SD I(00)
		b)	8.6	P.O. Failure Phenomena SD I(78)
				P.O. Failure Analysis Studies P I(00)
IR Thermal Mapping	P I(09)		8.6	P.O. Failure Analysis Techniques P I(01)
				P.O. Failure Analysis Studies P I(00)
Iron	BK II(39)		8.3	P.O. Materials NOC BK II(13)
				Considered under Functional Elements*
				P.O. Device Element Materials BK II(26)
Isolation Method	RD I(34)		8.1	Includes:
				Dielectric, Air (Beam Lead*) RD I(35)
				Dielectric, Ceramic RD I(36)
				Dielectric, Glass RD I(37)
				Dielectric, Nitride RD I(38)
				Dielectric, Oxide RD I(39)
				Junction RD I(41)
				Resistive RD I(42)
				Dielectric, NOC RD I(40)
Isolation Region	GN I(69)		8.3	Considered under Circuit Component Regions*
				Considered under MEL Device Element Descriptors*

Term	Code		Relationships
Item Status*			See: Developmental BK I(96) Experimental BK I(97) Pilot Production BK I(98) Production BK I(99)
ITT Semiconductor (06)	RD I(83) RD I(70)	a)	Considered under Manufacturer
		b)	P.O. Device Manufacturer BL I(25) Considered under Report Source*
JFET (Junction Field Effect Transistor)	GN I(16)		P.O. FET GN I(12) P.O. Transistor GN I(09) P.O. Circuit Component GN I(00) Considered under MEL Device Element Descriptors*
Journal Article	BL I(55)		Considered under Report Type*
Junction	RD I(41)		P.O. Isolation Method RD I(34)
Junction Formation	W I(09)		P.O. Fabrication Techniques and Equipment W I(00) Includes: Alloying W I(10) Diffusion W I(11) Epitaxy W I(12)
Kovar	BK II(68)		P.O. Package Terminal Material BK II(64) Considered under Non-Functional Element* P.O. Device Element Materials BK II(26)
Laboratory Environmental Test	P I(23)		P.O. Failure Environment P I(18) P.O. Failure Analysis Studies P I(00)
Laboratory Ground Environment			See Ground, Laboratory Environment

Laboratory Life Test	P I(24)	8.6	P.O. Failure Environment P I(18) P.O. Failure Analysis Studies P I(00)
LASCR (Light Activated Silicon Controlled Rectifier)	GN I(04)	8.3	P.O. PNPN Devices GN I(01) P.O. Circuit Component GN I(00) Considered under MEL Device Element Descriptors*
Launch and Flight	OR I(47)	8.11	P.O. Missile Environment OR I(45) P.O. Application Environment OR I(35) Considered under Applications
Layout	SD I(64)	8.5	P.O. Computer Aids SD I(63) P.O. Circuit/Device Implementation SD I(60)
Lead	BK II(40	8.3	P.O. Materials NOC BK II(13) Considered under Functional Elements* P.O. Device Element Materials BK II(26)
Lead Attachment Modes (external leads)	GN I(83)	8.3	Includes: Microcable GN I(84) Modules GN I(85) Multilayer Board GN I(86) Pressure Connector GN I(87) Printed Circuit Board GN I(88) Soldered GN I(89) Stacked Arrays GN I(90) Welded GN I(91)
Lead Attachment Processes and Equipment (external leads)	W I(50)	8.7	P.O. Fabrication Techniques and Equipment W I(60)

Term	Code		Scope
Lead Attachment Processes etc. (cont'd)			Includes: Cold Welding W I(51); Resistance Weld GN I(95); Soldered GN I(89); Lead Attachment Processes and Equipment NOC W I(52)
Lead Attachment Processes and Equipment NOC	W I(52)	8.7	P.O. Lead Attachment Processes and Equipment W I(50) P.O. Fabrication Techniques and Equipment W I(00)
Lead Fatigue	SD I(86)	8.6	P.O. Failure Phenomena SD I(78) P.O. Failure Analysis Studies P I(00)
Lead/Terminal Bond Mode	GN I(92)	8.3	Includes: Ball TC Bond GN I(93); Plated GN I(94); Resistance Weld GN I(95); Solder GN I(96); Switch TC Bond GN I(97); Ultrasonic Bond GN I(98); Wedge TC Bond GN I(99)
Lead/Terminal Bonding (wire bonding*)	W I(37)	8.7	P.O. Assembly W I(30) P.O. Fabrication Techniques and Equipment W I(00) Includes: Thermocompression bonding W I(38); Ultrasonic Bond GN I(98)
LID* (leadless inverted device*)			See Inverted, Face Down
Limited	BL I(17)	8.4	Considered under Report Security Classification* P.O. Classified BL I(13) or Unclassified BL I(16)

Linear (Analog*)	RD I(12)	8.1	Considered under Functional Category*
Linear Device	RD I(23)	8.1	Considered under Operational Type*
			Includes:
			Differential RD I(24)
			Single Ended RD I(25)
			Linear Device NOC RD I(86)
Linear Device NOC	RD I(86)	8.1	P.O. Linear Device RD I(23)
Liquid Immersion	P I(35)	8.6	P.O. Failure Stress Domain P I(33)
			P.O. Failure Analysis Studies P I(00)
Loose Material in Package	P I(67)	8.6	P.O. Workmanship Defects P I(61)
			P.O. Causes of Failures P I(49)
			P.O. Failure Analysis Studies P I(00)
Lot Acceptance	YI(05)	8.10	P.O. Quality Assurance Y I(03)
			Considered under Test Type*
			P.O. Part Level Data Y I(00)
Low Barometric Pressure	GY I(30)	8.10	P.O. Environmental Conditions GY I(24)
			P.O. Part Level Data Y I(00)
LSI Interconnection Design	SD I(65)	8.5	P.O. Computer Aids SD I(63)
			P.O. Circuit/Device Implementation SD I(60)
LSI (Large Scale Integration*)	BK I(83)	8.3	Considered under Scale of Integration*
Machine Printout	BL I(72)	8.4	Considered under Document Format*
Machine Processing	OR I(20)	8.9	P.O. Statistical Tools OR I(15)
			P.O. Reliability Technology OR I(00)
Machine Sensible Format	BL I(73)	8.4	Considered under Document Format*

Magnetism SD I(41) 8.5 P.O. Physical Phenomena SD I(23)

P.O. Circuit/Device Theory SD I(00)

Magnetic Film Storage Elements BK I(59) 8.3 P.O. Circuit Functions BK I(49)

Major System* 8 3 See:

F-111 GY I(53)

Minuteman II GY I(54)

Malfunction Reports OR I(76) 8.11 P.O. Reliability Data OR I(72)

Considered under Applications

Manual Systems OR I(26) 8.9 P.O. Data Collection and Reduction OR I(23)

P.O. Reliability Technology OR I(00)

Manufacturer 8.2 DIGIT CODE

	Tens		Units
RD I(83)	0-	RD I(64)	-0
RD I(74)	1-	RD I(65)	-1
RD I(75)	2-	RD I(66)	-2
RD I(76)	3-	RD I(67)	-3
RD I(77)	4-	RD I(68)	-4
RD I(78)	5-	RD I(69)	-5
RD I(79)	6-	RD I(70)	-6
RD I(80)	7-	RD I(71)	-7
RD I(81)	8-	RD I(72)	-8
RD I(82)	9-	RD I(73)	-9

Manufacturer (cont'd)	RD I(83) RD I(65)	Amelco Semiconductor (01)
	RD I(83) RD I(66)	Amperex Electronic Corp. (02)
	RD I(83) RD I(67)	Bunker-Ramo Corp. (03)
	RD I(83) RD I(68)	Fairchild Semiconductor (04)
	RD I(83) RD I(69)	General Instrument Corp. (05)
	RD I(83) RD I(70)	ITT Semiconductor (06)
	RD I(83) RD I(71)	Motorola Semiconductor Products (07)
	RD I(83) RD I(72)	National Semiconductor Corp. (08)
	RD I(83) RD I(73)	Philco-Ford Corp. (09)
		Philco-Ford Bipolar IC's
		Philco-Ford MOS IC's
	RD I(74) RD I(64)	Radiation, Inc. (10)
	RD I(74) RD I(65)	Radio Corporation of America (11)
	RD I(74) RD I(66)	Raytheon Company (12)
	RD I(74) RD I(67)	Signetics Corp. (13)
	RD I(74) RD I(68)	Siliconix, Inc. (14)
	RD I(74) RD I(69)	Sperry Semiconductor (15)
	RD I(74) RD I(70)	Sprague Electric Co. (16)
	RD I(74) RD I(71)	Sylvania Electric Products Inc. (17)

Manufacturer (cont'd)

RD I(74) Texas Instruments Incorporated (18)
RD I(72)

RD I(74) Traneitron Electronic Corp. (19)
RD I(73)

RD I(75) Union Carbide Electronics (20)

RD I(75) Westinghouse Electric Corp. (21)
RD I(65)

a) 8 4 P.O. Device Manufacturer BL I(25)

b) 8.2 Considered under Report Source*

Manufacturing Date GY I(79) 8.2 Includes:

GY I(62) 1962

GY I(63) 1963

GY I(64) 1964

GY I(65) 1965

GY I(66) 1966

GY I(73) Jan.-June

GY I(74) July-Dec.

GY I(67) 1967

GY I(68) 1968

GY I(69) 1969

GY I(70) 1970

GY I(71)

GY I(72)

GY I(75) Jan.-Mar.

GY I(76) Apr.-June

GY I(77) July-Sept.

GY I(78) Oct.-Dec.

Martin-Marietta (OS) SD I(58) SD I(99) 8.4 P.O. Device User BL I(26)

Considered under Report Source*

Term	Code		Section	Related Terms
Masking	W I(17)		8.7	P.O. Photolithography W I(14) P.O. Fabrication Techniques and Equipment W I(00)
Mask Design	SD I(66)	a)	8.5	P.O. Computer Aids SD I(63)
		b)	8.5	P.O. Circuit/Device Implementation SD I(60)
Mask Misalignment	P I(82)		8.6	P.O. Physical Defects P I(75) P.O. Failure Analysis Studies P I(00)
Material Control (RAW) Specifications	W I(77)		8.8	Considered under Specifications
Material Preparation	W I(01)		8.8	P.O. Fabrication Techniques and Equipment W I(00) Includes: Crystal Growth W I(02) Purification and Refinement W I(03)
Materials Control	OR I(92)		8.6	P.O. Corrective Measures OR I(89) P.O. Failure Analysis Studies P I(00)
Materials NOC	BK II(13)		8.3	Considered under Functional Elements* P.O. Device Element Materials BK II(26) Includes: II-VI Compounds[1] BK II(32) III-V Compounds[1] BK II(33) IV-VI Compounds[1] BK II(34) IV-IV Compounds[1] BK II(35) III-VI Compounds[1] BK II(98) Cermets and Glazes (all compositions) BK II (31)

[1]Compound identification page 247

Term	Code		Scope / Includes
Materials NOC (cont'd)			Includes (cont'd)
			Ferrites BK II(36)
			Ferroelectrics BK II(37)
			Hafnium BK II(14)
			Indium BK II(38)
			Iron BK II(39)
			Lead BK II(40)
			Molybdenum BK II(41)
			Nichrome BK II(42)
			Platinum BK II(43)
			Tantalum BK II(44)
			Tin BK II(45)
			Materials NOC BK II(13)
Mathematical Modeling	SD I(52)	8.5	P.O. Circuit/Device Theory SD I(00)
Maximum Fan-Out (Rating per Equivalent Gate Circuit)		8.3	Considered under Electrical Properties*
			BK I(03) Less than 5
			BK I(04) 5 thru 10
			BK I(05) Excess of 10
Maximum Frequency of Operation		8.3	Considered under Electrical Properties*
			BK I(06) Less than 10 Hz
			BK I(07) 10 Hz to less than 10 kHz
			BK I(08) 10 kHz to less than 10 MHz
			BK I(09) 10 MHz to less than 300 MHz
			BK I(10) 300 MHz to 300 GHz
			BK I(11) Greater than 300 GHz

Parameter	Ref.	Criteria
Maximum Operating Temperature	8.3	Considered under Environmental Capabilities*
		BK I(25) ≥202.5°C
		BK I(26) 172.5°C to <202.5°C
		BK I(27) 152.5°C to <172.5°C
		BK I(28) 102.5°C to <152.5°C
		BK I(29) <102.5°C
Maximum Output Power	8.3	Considered under Electrical Properties*
		BK I(21) Less than 10 mw
		BK I(22) 20 - 100 mw
		BK I(23) 101mw - 1 Watt
		BK I(24) Greater than 1 Watt
Maximum Power Dissipation (per Equivalent Circuit Input) (gate)	8.3	Considered under Electrical Properties*
		BK I(12) Less than 10 mw
		BK I(13) 10 thru 30 mw
		BK I(14) Greater than 30 mw
Maximum Storage Temperature	8.3	Considered under Environmental Capabilities*
		BK I(34) ≥302.5°C
		BK I(35) 252.5°C to <302.5°C
		BK I(36) 202.5°C to <252.5°C
		BK I(37) 152.5°C to <202.5°C
		BK I(38) 102.5°C to <152.5°C
		BK I(39) < 102.5°C
Mechanical Environments Y I(77)	8.10	Considered under Step Stress Test Domain*
		P.O. Step Stress Test Y I(73)
		P.O. Part Level Data Y I(00)

Mechanical Environments	Y I(91)	8.10	Considered under Accelerated Life Test Domain* P.O. Accelerated Life Test Y I(87) P.O. Part Level Data Y I(00)
Mechanical Propagation	SD I(42)	8.5	P.O. Physical Phenomena SD I(23) P.O. Circuit/Device Theory SD I(00)
Mechanical Shock	GY I(31)	8.10	P.O. Environmental Condition GY I(24) P.O. Part Level Data Y I(00)
Mechanical Shock	P I(36)	8.6	P.O. Failure Stress Domain P I(33) P.O. Failure Analysis Studies P I(00)
Mechanical Stress Testing	OR I(08)	8.9	P.O. Test Techniques and Procedures OR I(03) P.O. Reliability Technology OR I(00)
MECL*			See CML
MEL Device Element Descriptor*		8.7	Includes: Circuit Component GN I(00) Circuit Component Regions* Die Size
Metal	RD I(90)	8.3	P.O. Package Material (Primary) RD I(87) Considered on Non-Functional Elements* P.O. Device Element Materials BK II(26)
Metallization Discontinuity	P I(83)	8.6	P.O. Physical Defects P I(70) P.O. Failure Analysis Studies P I(00)
Metallization Materials			See Circuit Metallization Materials
Metallurgical Diffusion	SD I(87)	8.6	P.O. Failure Phenomena SD I(78) P.O. Failure Analysis Studies P I(00)
Metallurgical Phenomena	SD I(53)	8.5	P.O. Circuit/Device Theory SD I(00)

Metallurgical Phenomena (cont'd)			Includes:
			Alloying W I(10)
			Crystal Growth W I(02)
			Fatigue SD I(54)
			Shear Modulus SD I(55)
			Work Hardening SD I(56)
			Young's Modulus SD I(57)
Metal Screen	W I(24)	8.7	P.O. Thick Film W I(23)
			P.O. Fabrication Techniques and Equipment W I(00)
			P.O. Deposition W I(22)
Microcable	GN I(84)	8.3	P.O. Lead Attachment Modes GN I(83)
Micro Capacitor Discrete*			See Discrete Micro Capacitor
Microcircuit, Hybrid			See Hybrid Microcircuit
Microcircuit, Multichip			See Multichip Microcircuit
Micro Diode, Discrete	GN I(34)	8.3	P.O. Diode GN I(30)
			P.O. Circuit Component GN I(00)
			Considered under MEL Device Element Descriptors*
Microelectronic Category*		8.1	Includes:
			Composite IC, Diffused RD I(01)
			Composite IC, Epitaxial RD I(02)
			Composite IC, NOC (Synonyms: Compatible Monolithic*, Monobrid*, Active Substrate IC*) RD I(00)
			Hybrid Microcircuit (Synonyms: Hybrid Integrated Circuit*) RD I(03)
			Monolithic, Diffused RD I(04)
			Monolithic, Epitaxial RD I(05)
			Monolithic IGFET RD I(06)

Microelectronic Category* (cont'd)			Includes (cont'd) Monolithic, NOC (not otherwise classified. Synonyms: Mono*, Fully IC*, Semiconductor IC*) RD I(07) Multichip Microcircuit (Synonyms: Multichip Hybrid IC*) RD I(08) Thick Film - Pure IC (Synonyms: Passive Substrate IC*) RD I(09) Thin Film - Pure IC (Synonyms: TFIC*, Passive Substrate IC*) RD I(10)
Microelectronic Device			See MEL Device
Microfiche	BL I(74)	8 4	Considered under Document Format*
Microfilm	BL I(75)	84	Considered under Document Format*
MIL-M-23700	Y I(11)	8.10	Considered under Specification Reference* P.O. Part Level Data Y I(00)
MIL-S-19500	Y I(12)	8.10	Considered under Specification Reference* P.O. Part Level Data Y I(00)
MIL-STD-202	Y I(13)	8.10	Considered under Specification Reference* P.O. Part Level Data Y I(00)
MIL-STD-750	Y I(14)	8.10	Considered under Specification Reference* P.O. Part Level Data Y I(00)
Military	RD I(62)	8.1	Considered under Qualification Class*
Military and Space	BL I(30)	84	Considered under Sponsoring Organization* Includes: Air Force BL I(31) Army BL I(32)

Military and Space (cont'd)			Includes (cont'd)
			DOD BL I(33)
			NASA BL I(34)
			Navy BL I(35)
Military and Space	BL I(19)	8.4	Considered under Report Source*
			Includes:
			Air Force BL I(20)
			Army BL I(21)
			DOD BL I(22)
			NASA BL I(23)
			Navy BL I(24)
Military Upgraded	RD I(63)	8.1	Considered under Qualification Class*
Minimum Operating Temperature		8.3	Considered under Environmental Capabilities*
			BK I(30) ≥-42.5°C
			BK I(31) -62.5°C to <-42.5°C
			BK I(32) -82.5°C to <-62.5°C
			BK I(33) <-82.5°C
Minimum Storage Temperature		8.3	Considered under Environmental Capabilities*
			BK I(40) ≥-42.5°C
			BK I(41) -62.5°C to <-42.5°C
			BK I(42) -82.5°C to <-62.5°C
			BK I(43) -102.5C to <-82.5°C
			BK I(44) <-102.5°C
Minuteman II	GY I(54)	8.3	Considered under Major System*

Misapplication	P I(51)	8.6	P.O. Causes of Failure P I(49) P.O. Failure Analysis Studies P I(00) Includes: Device Mishandling P I(52) Erroneous Lead Positioning P I(53) Overstressed Devices P I(54)
Missile Environment	OR I(45)	8.11	P.O. Application Environment OR I(35) Considered under Applications Includes: Ground checkout OR I(46) Launch and Flight OR I(47)
MNS	GN I(46)	8.3	P.O. IGFET GN I(13) P.O. FET GN I(12) P.O. Transistors GN I(09) P.O. Circuit Component GN I(00) Considered under MEL Device Element Descriptors*
Mobile, Ground Environment			See Ground Mobile Environment
Modification	SD I(69)	8.5	P.O. Circuit/Device Implementation SD I(60)
Module	RD I(57)	8.1	Considered under Package Configuration*
Modules	GN I(85)	8.3	P.O. Lead Attachment Modes GN I(83)
Moisture or Humidity	P I(37)	8.6	P.O. Failure Stress Domain P I(33) P.O. Failure Analysis Studies P I(00)
Moisture Resistance	GY I(32)	8.10	P.O. Environmental Condition GY I(24) P.O. Part Level Data Y I(00)

Molded	BK I(93)	a)	8.3	P.O. Package Seal BK I(90)
		b)	8.7	P.O. Encapsulation/Package Sealing W I(39)
				P.O. Fabrication Techniques and Equipment W I(00)
Molecular Electronic Function	BK I(60)		8.3	P.O. Circuit Functions BK I(49)
Molybdenum	BK II(41)		8.3	P.O. Materials NOC BK II(13)
				Considered under Functional Element*
				P.O. Device Element Materials BK II(26)
Mono*				See Monolithic, NOC
Monobrid*				See Composite IC (NOC)
Monolithic, NOC (Synonyms: Mono*, Fully IC*, Semiconductor IC*)			8.1	Considered under Microelectronic Category*
Monolithic, Diffused	RD I(04)		8.1	Considered under Microelectronic Category*
Monolithic, Epitaxial	RD I(05)		8.1	Considered under Microelectronic Category*
Monolithic IGFET	RD I(06)		8.1	Considered under Microelectronic Category*
Monostable Multivibrators	BK I(61)		8.3	P.O. Circuit Functions BK I(49)
MOS	GN I(28)	a)	8.3	Considered under Capacitor GN I(24)
				P.O. Circuit Component GN I(00)
				Considered under MEL Device Element Descriptors*
		b)	8.3	P.O. IGFET GN I(13)
				P.O. FET GN I(12)
				P.O. Transistors GN I(09)
				P.O. Circuit Component GN I(00)
				Considered under MEL Device Element Descriptors*

MOS Processes NOC	W I(61)		8.7	P.O. Fabrication Techniques and Equipment W I(00)
MOSTL	RD I(18)		8.1	P.O. Digital Logic RD I(13) Considered under Operational Type*
Motorola (10)	SD I(59) SD I(05)		8.4	P.O. Device User BL I(26) Considered under Report Source*
Motorola Semi-conductor Products, Inc. (07)	RD I(83) RD I(71)	a)	8.2	Considered under Manufacturer
		b)	8.4	P.O. Device Manufacturer BL I(25) Considered under Report Source*
MSI (Medium Scale Integration)	BK I(84)		8.3	Considered under Scale of Integration*
MTOS	GN I(47)		8.3	P.O. IGFET GN I(13) P.O. FET GN I(12) P.O. Transistor GN I(09) P.O. Circuit Component GN I(00) Considered under MEL Device Element Descriptors*
Multichip Hybrid IC*				See Multichip Microcircuit
Multichip Micro-circuit (Multi-chip Hybrid IC*)	RD I(08)		8.1	Considered under Microelectronic Category*
Multilayer Board	GN I(86)		8.3	P.O. Lead Attachment Modes GN I(83)
Multiple Emitter	GN I(17)		8.3	P.O. Transistors GN I(09) P.O. Circuit Component GN I(00) Considered under MEL Device Element Descriptors*
Multivibrator	RD I(47)		8.1	Considered under Circuit Complexity*
Multivibrator				See Astable, Bistable, Monostable Multivibrator

NAND Gate (NAND/ NOR Gate*)	BK I(62)	8.3	P.O. Circuit Functions BK I(49)
NAND/NOR, Gate*			See NAND Gate
NASA	BL I(23)	8.4	P.O. Military and Space BL I(19) Considered under Report Source*
NASA	BL I(34)	8.4	P.O. Military and Space BL I(30) Considered under Sponsoring Organization
NASA	Y I(15)	8.10	Considered under Specification Reference* P.O. Part Level Data Y I(00)
National Semiconductor Corp. (08)	RD I(83) RD I(72)	a) 8.2 b) 8.4	Considered under Manufacturer P.O. Device Manufacturer BL I(25) Considered under Report Source*
Navigation	OR I(61)	8.11	Considered under Equipment Class* Considered under Applications
Navy	BL I(24)	8.4	P.O. Military and Space BL I(19) Considered under Report Source*
Navy	BL I(35)	8.4	P.O. Military and Space BL I(30) Considered under Sponsoring Organization*
N-Channel IGFET	GN I(14)	8.3	P.O. IGFET GN I(13) P.O. FET GN I(12) P.O. Transistors GN I(09) P.O. Circuit Component GN I(00) Considered under MEL Device Element Descriptors*
Negative Resistance/Gunn Effect	SD I(43)	8.5	P.O. Physical Phenomena SD I(23) P.O. Circuit/Device Theory SD I(00)

Nichrome	BK II(42)	8.3	P.O. Materials NOC BK II(13) Considered under Functional Elements* P.O. Device Element Material BK II(26)
Nickel (All)	GY I(85)	8.3	Unqualified terms
Nickel	BK II(05)	8.3	P.O. Circuit Metallization Material BK II(00) Considered under Functional Elements* P.O. Device Element Material BK II(26) P.O. Nickel (All) GY I(85)
Nitride Dielectric			See Dielectric, Nitride
Noise, Acoustical	P I(38)	8.4	P.O. Failure Stress Domain P I(33) P.O. Failure Analysis Studies P I(00)
Noise Figure	GY I(90)	8.5	P.O. Circuit Parameters GY I(86)
Noise Margin	GY I(91)	8.5	P.O. Circuit Parameters GY I(86)
Non-Destructive Evaluation	P I(10)	8.6	P.O. Failure Analysis Techniques P I(01) P.O. Failure Analysis Studies P I(00)
Non-Functional Elements*		8.3	P.O. Device Element Material BK II(26) See: Die Bond Material BK II(58) Package Material (Primary) RD I(87) Package Terminal Material BK II(64) Substrate Materials BK II(46) Surface Protection BK II(53)
Non-Military Government Agency	BL I(39)	8.4	Considered under Sponsoring Organization*

Term	Code		Relations
Non-Military Government Agency	BL I(28)	8.4	Considered under Report Source*
Norden (11)	SD I(59) SD I(91)	8.4	P.O. Device User BL I(26)
			Considered under Report Source*
NOR Gate (NOR/NAND Gate*)	BK I(63)	8.3	P.O. Circuit Functions BK I(49)
NOR/NAND Gate*			See NOR Gate
Not Certified	BL I(41)	8.4	Considered under Data Validation*
NPN	GN I(18)	8.3	P.O. Transistors GN I(09)
			P.O. Circuit Component GN I(00)
			Considered under MEL Device Element Descriptors*
Number of Major Process Steps*		8.3	BK I(73) 3
			BK I(74) 4
			BK I(75) 5
			BK I(76) 6
			BK I(77) 7
			BK I(78) 8
			BK I(79) 9
			BK I(80) 10
			BK I(81) 11
			BK I(82) 12
			BK I(72) Other
Open Circuit	P I(30)	8.4	P.O. Failure Mode P I(27)
			P.O. Failure Analysis Studies P I(00)
Operating Tests	OR I(09)	8.9	P.O. Test Techniques and Procedures OR I(03)
			P.O. Reliability Technology OR I(00)
Operational Amplifier	BK I(64)	8.3	P.O. Circuit Functions BK I(49)

Operational Dynamic Life Test	GY I(05)	8.10	P.O. Part Level Data Y I(00) Includes: Operational Dynamic Test Maximum Load Power Operational Dynamic Test Maximum Supply Voltage Operational Dynamic Test Maximum Temperature
Operational Dynamic Test Maximum Load Power		8.10	P.O. Operational Dynamic Life Test GY I(05) P.O. Part Level Data Y I(00) Includes: GY I(19) < 95% Rated GY I(20) 95% to < 105% Rated GY I(21) 105% to < 155% Rated GY I(22) ≥155% Rated
Operational Dynamic Test Maximum Supply Voltage		8.10	P.O. Operational Dynamic Life Test GY I(05) P.O. Part Level Data Y I(00) Includes: GY I(15) < 95% Rated GY I(16) 95% to < 105% Rated GY I(17) 105% to < 155% Rated GY I(18) ≥155% Rated
Operational Dynamic Test Maximum Temperature		8.10	P.O. Operational Dynamic Life Test GY I(05) P.O. Part Level Data Y I(00) Includes: GY I(06) < -82.5°C GY I(07) -82.5°C to < -42.5°C GY I(03) -42.5°C to < 21°C GY I(09) 21°C to < 31°C

Operational Dynamic Test Maximum Temperature (cont'd)			Includes (cont'd) GY I(10) 31°C to < 102.5°C GY I(11) 102.5°C to 152.5°C GY I(12) 152.5°C to 202.5°C GY I(13) 202.5°C to < 302.5°C GY I(14) ≥302.5°C
Operational Static Life Tests	Y I(26)	8.10	P.O. Part Level Data Y I(00) Includes: Operational Static Test Load Power Operational Static Test Supply Voltage Operational Static Test Temperature
Operational Static Test Load Power		8.10	P.O. Operational Static Life Test Y I(26) P.O. Part Level Data Y I(00) Includes: Y I(40) < 95% Rated Y I(41) 95% to < 105% Rated Y I(42) 105% to < 155% Rated Y I(43) ≥155% Rated
Operational Static Test Supply Voltage		8.10	P.O. Operational Static Life Test Y I(26) P.O. Part Level Data Y I(00) Includes: Y I(36) < 95% Rated Y I(37) 95% to < 105% Rated Y I(38) 105% to < 155% Rated Y I(39) ≥155% Rated

Term	Code		Cross-reference
Operational Static Test Temperature		8.16	P.O. Operational Static Life Test Y I(26)
			P.O. Part Level Data Y I(00)
			Includes:
			Y I(27) $< -82.5°C$
			Y I(28) -82.5°C to $<$ -42.5°C
			Y I(29) -42.5°C to $<$ 21°C
			Y I(30) 21°C to $<$ 31°C
			Y I(31) 31°C to $<$ 102.5°C
			Y I(32) 102.5°C to $<$ 152.5°C
			Y I(33) 152.5°C to $<$ 202.5°C
			Y I(34) 202.5°C to $<$ 302.5°C
			Y I(35) $\geq$302.5°C
Operational Type*		8.1	See:
			Digital Logic RD I(13)
			Linear Device RD I(23)
OR/AND Gate*			See OR Gate
OR Gate (OR/AND Gate*)	BK I(65)	8.3	P.O. Circuit Functions BK I(49)
Output Impedance (Typical)		8.3	Considered under Electrical Properties*
			Includes:
			BK I(00) Less than 10 K Ohms
			BK I(01) 10 K thru 100 K Ohms
			BK I(02) Greater than 100 K Ohms
Overstressed Devices	P I(54)	8.6	P.O. Misapplication P I(51)
			P.O. Causes of Failure P I(49)
			P.O. Failure Analysis Studies P I(00)

Oxidation	W I(13)	a) 8.5	P.O. Chemical Phenomena SD I(01)
			P.O. Circuit/Device Theory SD I(00)
		b) 8.7	P.O. Fabrication Techniques and Equipment W I(00)
Oxidation Defects	P I(84)	8.4	P.O. Physical Defects P I(70)
			P.O. Failure Analysis Studies P I(00)
Oxide, Dielectric			See Dielectric, Oxide
Package Configuration*		8.1	See:
			Can, Hermetic Sealed RD I(52)
			Dual In-Line, Hermetic Sealed RD I(53)
			Dual In-Line, Plastic (DIP) RD I(54)
			Flat Pack, Ceramic RD I(55)
			Flat Pack, Glass RD I(56)
			Module RD I(57)
			Plastic Encapsulated (Non-DIP Plastic Cap) RD I(58)
Package Failure	P I(31)	8.4	P.O. Failure Modes P I(27)
			P.O. Failure Analysis Studies P I(00)
Package Material (Primary)	RD I(87)	8.3	Considered under Non-Functional Elements*
			P.O. Device Element Materials BK II(26)
			Includes:
			Ceramics RD I(88)
			Glass RD I(89)
			Metal RD I(90)
			Plastic Silicon Resin RD I(91)
			Plastic, NOC RD I(92)

Package Seal	BK I(90)	8.3	Includes: Glass-to-Glass Seal BK I(91) Glass-to-Metal Seal BK I(92) Molded BK I(93) Seam Weld BK I(94) Package Seal NOC BK I(95)
Package Seal NOC	BK I(95)	8.3	P.O. Package Seal BK I(90)
Package Terminal Material	BK II(64)	8.3	Considered under Non-Functional Elements* P.O. Device Element Material BK II(26) Includes: Aluminum BK II(65) Copper BK II(66) Gold BK II(67) Kovar BK II(68) Package Terminal Material NOC BK II(69)
Package Terminal Material NOC	BK II(69)	8.3	P.O. Package Terminal Material BK II(64) Considered under Non-Functional Elements* P.O. Device Element Materials BK II(26)
Package Type	BK II(81)	8.3	Includes: BK II(82) TO-5 BK II(70) TO-70 BK II(71) TO-71 BK II(72) TO-72 BK II(73) TO-73

Package Type (cont'd)			Includes (cont'd)
			BK II(74) TO-74
			BK II(75) TO-75
			BK II(76) TO-76
			BK II(77) TO-77
			BK II(78) TO-78
			BK II(79) TO-79
			BK II(80) TO-80
			BK II(84) TO-84
			BK II(85) TO-85
			BK II(86) TO-86
			BK II(87) TO-87
			BK II(88) TO-88
			BK II(89) TO-89
			BK II(90) TO-90
			BK II(91) TO-91
			BK II(95) TO-95
			BK II(96) TO-96
			BK II(99) TO-99
			BK II(83) TO-100
			Dual In-Line, 10 Lead BK II(92)
			Dual In-Line, 14 Lead BK II(93)
			Dual In-Line, NOC BK II(94)
Packaging	OR I(85)	8.11	P.O. Application Design Techniques and Considerations OR I(79)
			Considered under Applications

Packaging	BL I(63)	8.4	P.O. Survey and Review BL I(59)
			Considered under Report Type*
Packaging and Delivery Specifications	W I(78)	8.8	Specifications
Part Level Data	Y I(00)	8.10	Includes:
			Accelerated Life Test Y I(87)
			Agree Test OR I(05)
			Environmental Condition GY I(24)
			Intermittent Life Test Y I(50)
			Operational Dynamic Life Test GY I(05)
			Operational State Life Test Y I(26)
			Specification Reference*
			Step Stress Test Y I(73)
			Storage Life Test Temperature
			Test Results GY I(43)
			Test Type*
Part Number		5.2	

Part Number Code	Termatrex Card Numbers
Thousand	
0 _ _ _	W I(62)
1 _ _ _	W I(63)
Hundred	
_ 0 _ _	W I(64)
_ 1 _ _	W I(65)
_ 2 _ _	W I(66)
_ 3 _ _	W I(67)
_ 4 _ _	W I(68)
_ 5 _ _	W I(69)
_ 6 _ _	W I(70)
_ 7 _ _	W I(71)
_ 8 _ _	W I(72)
_ 9 _ _	W I(73)

Part Number (cont'd)

Part Number Code	Termatrex Card Numbers
Tens	
_ _0_	W I(40)
_ _1_	W I(41)
_ _2_	W I(42)
_ _3_	W I(43)
_ _4_	W I(44)
_ _5_	W I(45)
_ _6_	W I(46)
_ _7_	W I(47)
_ _8_	W I(48)
_ _9_	W I(49)
Units	
_ _ _0	W I(90)
_ _ _1	W I(91)
_ _ _2	W I(92)
_ _ _3	W I(93)
_ _ _4	W I(94)
_ _ _5	W I(95)
_ _ _6	W I(96)
_ _ _7	W I(97)
_ _ _8	W I(98)
_ _ _9	W I(99)

Term	Card		Cross-reference
Passive Substrate IC*			See Thin Film Pure IC or Thick Film Pure IC
Passivated NOC	BK II(57)	8.8	P.O. Surface Protection BK II(53)
			Considered under Non-Functional Element*
			P.O. Device Element Material BK II(26)
P-Channel IGFET	GN I(15)	8.3	P.O. IGFET GN I(13)
			P.O. FET GN I(12)
			P.O. Transistor GN I(09)
			P.O. Circuit Component GN I(00)
			Considered under MEL Device Element Descriptor*
Performance	Y I(02)	8.10	Considered under Test Type*
			P.O. Part Level Data Y I(00)
Performance Curves	GY I(47)	8.10	P.O. Test Results GY I(43)
			P.O. Part Level Data Y I(00)

Term	Code			Related entries
Performance Measurement	OR I(29)		8.9	P.O. Facilities OR I(27)
				P.O. Reliability Technology OR I(00)
Philco-Ford Corp. (09)	RD I(83) RD I(73)	a)	8.2	Considered under Manufacturer
		b)	8.4	P.O. Device Manufacturer BL I(25)
				Considered under Report Source*
Phosphorous	BK II(24)		8.3	P.O. Dopant Materials BK II(18)
				Considered under Functional Element*
				P.O. Device Element Material BK II(26)
Photochromic Paints	P I(11)		8.6	P.O. Failure Analysis Techniques P I(01)
				P.O. Failure Analysis Studies P I(00)
Photoconductivity	SD I(44)		8.5	P.O. Physical Phenomena SD I(23)
				P.O. Circuit/Device Theory SD I(00)
Photolithography	W I(14)		8.7	P.O. Fabrication Techniques and Equipment W I(00)
				Includes:
				Developing W I(15)
				Exposure W I(16)
				Masking W I(17)
				Photoresist W I(18)
				Washing W I(19)
Photoresist	W I(18)		8.7	P.O. Photolithography W I(14)
				P.O. Fabrication Techniques and Equipment W I(00)
Photoresponse Mapping	P I(12)		8.6	P.O. Failure Analysis Techniques P I(01)
				P.O. Failure Analysis Studies P I(00)

Physical Defects	P I(70)	8.4	P.O. Failure Analysis Studies P I(00)
			Includes:
			Broken Lead P I(71)
			Contamination P I(72)
			Cracked Die P I(73)
			Cracked Package P I(74)
			Crystal Defects P I(75)
			Defective Bond P I(76)
			Diffusion Defects P I(77)
			Epitaxy Defects P I(78)
			Film Thickness Defect P I(79)
			Foreign Material P I(80)
			Improper Etch P I(81)
			Mask Misalignment P I(82)
			Metallization Discontinuity P I(83)
			Oxidation Defect P I(84)
			Pin Holes in Metallization P I(85)
			Pin Holes in Oxide P I(86)
			Poor Metallization Adhesion P I(87)
			Seal Leak P I(88)
Physical Parameters	SD I(07)	8.5	P.O. Circuit/Device Theory SD I(00)
			Includes:
			Carrier Concentration SD I(08)
			Carrier Lifetime SD I(09)
			Carrier Mobility SD I(10)
			Carrier Velocity SD I(11)

Term	Code		Related Terms
Physical Parameters (cont'd)			Includes (cont'd) Contact Potential SD I(12) Diffusion Coefficient SD I(13) Diffusion Length SD I(14) Energy Gap SD I(15) Energy Level SD I(16) Fermi Level SD I(17) Heat Capacity SD I(18) Storage Time SD I(19) Thermal Conductivity SD I(20) Thermal Diffusivity SD I(21) Work Function SD I(22)
Physical Phenomena	SD I(23)	8.5	P.O. Circuit/Device Theory SD I(00) Includes: Carrier Diffusion SD I(24) Carrier Generation SD I(25) Carrier Injection SD I(26) Carrier Recombination SD I(27) Carrier Saturation SD I(28) Depletion SD I(29) Electrical Conduction SD I(30) Electrical Noise Generation SD I(31) Electron Spin SD I(32) Enhancement SD I(33) Faults and Dislocations SD I(34) Ferroelectricity SD I(35) Field Effect SD I(36)

Term	Code		Notes
Physical Phenomena (cont'd)			Includes (cont'd)
			Hall Effect SD I(37)
			Impurity Diffusion SD I(38)
			Inversion and Channeling SD I(39)
			Ion Migration SD I(40)
			Magnetism SD I(41)
			Mechanical Propagation SD I(42)
			Negative Resistance/Gunn Effect SD I(43)
			Photoconductivity SD I(44)
			Pinch Off SD I(45)
			Radiation Emission/Electroluminescence SD I(46)
			Resonance SD I(47)
			Reverse Breakdown SD I(48)
			Superconductivity SD I(49)
			Thermal Conduction SD I(50)
			Thermoelectric Effects SD I(51)
Pilot Production	BK I(98)	8.3	Considered under Item Status*
Pinch Off	SD I(45)	8.5	P.O. Physical Phenomena SD I(23)
			P.O. Circuit/Device Theory SD I(00)
Pin Holes in Metallization	P I(85)	8.6	P.O. Physical Defects P I(70)
			P.O. Failure Analysis Studies P I(00)
Pin Holes in Oxide	P I(86)	8.4	P.O. Physical Defects P I(70)
			P.O. Failure Analysis Studies P I(00)
Plaque Formation	SD I(88)	8.6	P.O. Failure Phenomena SD I(78)
			P.O. Failure Analysis Studies P I(00)
Planar Junction	GN I(70)	8.3	Considered under Circuit Component Regions*
			Considered under MEL Device Element Descriptor*

Plastic, Dual In-Line			See Dual In-Line Plastic
Plastic Encapsulated (Non-DIP Plastic Cap)	RD I(58)	8.1	Considered under Package Configuration*
Plastic, Silicon Resin	RD I(91)	8.3	P.O. Package Material (Primary) RD I(87) Considered under Non-Functional Elements* P.O. Device Element Descriptor BK II(26)
Plastics, NOC	RD I(92)	8.3	P.O. Package Material (Primary) RD I(87) Considered under Non-Functional Elements* P.O. Device Element Descriptor BK II(26)
Plated	GN I(94)	8.3	P.O. Lead/Terminal Bond Mode GN I(92)
Platinum	BK II(43)	8.3	P.O. Materials NOC BK II(13) Considered under Functional Elements* P.O. Device Element Materials BK II(26)
PNP	GN I(19)	8.3	P.O. Transistors GN I(09) P.O. Circuit Component GN I(00) Considered under MEL Device Element Descriptor*
PNP-lateral	GN I(20)	8.3	P.O. Transistors GN I(09) P.O. Circuit Component GN I(00) Considered under MEL Device Element Descriptor*
PNPN Devices	GN I(01)	8.3	P.O. Circuit Components GN I(00) Considered under MEL Device Element Descriptor*

PNPN Devices (cont'd)			Includes:
			DIAC GN I(02)
			GTO GN I(03)
			LASCR GN I(04)
			SCR GN I(05)
			SCS GN I(06)
			Shockley 4-Layer Diode GN I(07)
			TRIAC GN I(08)
PNPN Latch-up	SD I(89)	8.6	P.O. Failure Phenomena SD I(78)
			P.O. Failure Analysis Studies P I(00)
Polymerization	SD I(06)	8.5	P.O. Chemical Phenomena SD I(01)
			P.O. Circuit/Device Theory SD I(00)
Poor Design	P I(55)	8.6	P.O. Causes of Failure P I(49)
			P.O. Failure Analysis Studies P I(00)
			Includes:
			Circuit Layout SD I(62)
			Device Geometry SD I(67)
			Process Design P I(56)
			Process Equipment Design P I(57)
Poor Metallization Adhesion	P I(87)	8.6	P.O. Physical Defects P I(70)
			P.O. Failure Analysis Studies P I(00)
Portable Ground Environment			See Ground Portable Environment
Post-Production Screens	OR I(93)	8.6	P.O. Corrective Measures OR I(89)
			P.O. Failure Analysis Studies P I(00)
Post-Production Screen/Burn-In	P I(25)	8.6	P.O. Failure Environment P I(18)
			P.O. Failure Analysis Studies P I(00)
Power	Y I(52)	8.10	Considered under Intermittent Stress Domain*

Power (cont'd)			P.O. Intermittent Life Test Y I(50)
			P.O. Part Level Data Y I(00)
			P.O. Power (All) GY I(99)
Power	Y I(92)	8.10	Considered under Accelerated Life Test Domain*
			P.O. Accelerated Life Test Y I(87)
			P.O. Part Level Data Y I(00)
			P.O. Power (All) GY I(99)
Power	Y I(78)	8.10	Considered under Step Stress Test Domain*
			P.O. Step Stress Test Y I(73)
			P.O. Part Level Data Y I(00)
			P.O. Power (All) GY I(99)
Power	GN I(21)	8.5	P.O. Transistors GN I(09)
			P.O. Circuit Component GN I(00)
			Considered under MEL Device Element Descriptor*
			P.O. Power (All) GY I(99)
Power (All)		8.3	Unqualified terms
Power Amplifier	BK I(66)	8.3	P.O. Circuit Functions BK I(49)
Power Dissipation	GY I(92)	8.5	P.O. Circuit Parameters GY I(86)
Power (Power Supplies)	OR I(62)	8.11	Considered under Equipment Class*
			Considered under Applications
Prediction and Modeling	OR I(02)	8.9	P.O. Reliability Technology OR I(00)
Pressure Connector	GN I(87)	8.3	P.O. Lead Attachment Modes GN I(83)
Pressure-Gas	P I(39)	8.6	P.O. Failure Stress Domain P I(33)
			P.O. Failure Analysis Studies P I(00)
Printed Circuit Board	GN I(88)	8.5	P.O. Lead Attachment Modes GN I(83)

Term	Code		Relations
Probing	W I(58)	8.7	P.O. Process Control Techniques W I(55)
			P.O. Fabrication Techniques and Equipment W I(00)
Procedure Approved by Source-Sponsor	BL I(47)	8.4	Considered under Data Validation*
Proceedings, Symposia, Conference	BL I(56)	8.4	Considered under Report Type*
Process Control	OR I(94)	8.6	P.O. Corrective Measures OR I(89)
			P.O. Failure Analysis Studies P I(00)
Process Control Specifications	W I(79)	8.8	Specifications
Process Control Techniques	W I(55)	8.7	P.O. Fabrication Techniques and Equipment W I(00)
			Includes:
			Beveling W I(56)
			Deposition Rate Monitoring W I(57)
			Probing W I(58)
			Residual Gas Analysis W I(59)
			Use of Test Patterns W I(60)
Process Design	P I(56)	8.6	P.O. Poor Design P I(55)
			P.O. Causes of Failures P I(49)
			P.O. Failure Analysis Studies P I(00)
Process Effectiveness	W I(53)	8.7	P.O. Fabrication Techniques and Equipment W I(00)
			Includes:
			Yield W I(54)
Process Equipment Design	P I(57)	8.6	P.O. Poor Design P I(55)
			P.O. Causes of Failures P I(49)
			P.O. Failure Analysis Studies P I(00)

Term	Code	Section	Cross-reference
Process Equipment Improvement	OR I(95)	8.6	P.O. Corrective Measures OR I(89)
			P.O. Failure Analysis Studies P I(00)
Process Errors	P I(60)	8.6	P.O. Causes of Failure P I(49)
			P.O. Failure Analysis Studies P I(00)
Process Improvement	OR I(96)	8.6	P.O. Corrective Measures OR I(89)
			P.O. Failure Analysis Studies P I(00)
Processing	BL I(64)	8.4	P.O. Survey and Review BL I(59)
			Considered under Report Type*
Processing Control			See Screening
Process Steps			See Number of Process Steps
Procurement			See Qualification - Part Level Data
Procurement Specification	OR I(97)	8.6	P.O. Corrective Measures OR I(89)
			P.O. Failure Analysis Studies P I(00)
Product Inspection	P I(26)	8.6	P.O. Failure Environment P I(18)
			P.O. Failure Analysis Studies P I(00)
Product Line Audit	Y I(06)	8.10	P.O. Quality Assurance Y I(03)
			Considered under Test Type*
			P.O. Part Level Data Y I(00)
Production	BR I(99)	8.3	Considered under Item Status*
Production Test and Inspection	OR I(70)	8.11	Considered under Application Status*
			Considered under Applications
Propagation Delay (Maximum)		8.3	Considered under Electrical Properties*
	BL I(15)		Less than 10 Nanoseconds
	BK I(16)		10 thru 30 Nanoseconds
	BK I(17)		Greater than 30 Nanoseconds
Proprietary Information	BL I(18)	8.4	Considered under Report Security Classification*
			P.O. Classified BL I(13) or Unclassified BL I(16))

Term	Code		Related Terms
Purification and Refinement	W I(03)	8.7	P.O. Material Preparation W I(01) P.O. Fabrication Techniques and Equipment W I(00)
Qualification (Procurement)	Y I(07)	8.10	P.O. Quality Assurance Data Y I(03) Considered under Test Type* P.O. Part Level Data Y I(00)
Qualification Class*		8.1	See: Consumer RD I(59) High Reliability Certification (Hi-Rel Certification) RD I(60) Industrial/Commercial RD I(61) Military RD I(62) Military Upgraded RD I(63)
Quality Assurance (Device Test Oriented)	Y I(03)	8.16	Considered under Test Type* P.O. Part Level Data Y I(00) Includes: Burn-In Test Y I(04) Lot Acceptance Y I(05) Product Line Audit Y I(06) Qualification (Procurement) Y I(07) Reliability Demonstration OR I(71) Screening (Processing Control) Y I(09)
Quality Assurance Measures	OR I(98)	8.6	P.O. Corrective Measures OR I(89) P.O. Failure Analysis Studies P I(00)
Quality Assurance Specifications	W I(80)	8.8	Includes: Government Agency QA Specifications W I(81) Quality Control Manuals W I(82)

Term	Code		Section	Related Terms
Quality Assurance Specifications (cont'd)				Includes (cont'd)
				Reliability and Environmental Test Methods W I(83)
				User Proprietary Screening and Burn-In Specifications W I(84)
				Vendor QA Plans and Specifications (Performance Specifications) W I(85)
				Vendor Screening and Burn-In Specifications W I(86)
Quality Control Manuals	W I(8[illegible])		8.8	P.O. Quality Assurance Specifications W I(80)
Radar	OR I(05)		8.11	Considered under Equipment Class*
				Considered under Applications
RADC Spec [illegible]	Y I(16)		8.10	Considered under Specification Reference*
				P.O. Part Level Data Y I(00)
Radiation, Electromagnetic	P I(40)		8.6	P.O. Failure Stress Domain P I(33)
				P.O. Failure Analysis Studies P I(00)
Radiation Emission/Electroluminescence	SD I([illegible])		8.5	P.O. Physical Phenomena SD I(23)
				P.O. Circuit/Device Theory SD I(00)
Radiation Environments	OR I(10)		8.9	P.O. Test Techniques and Procedures OR I(03)
				P.O. Reliability Technology OR I(00)
Radiation Exposure (Particle)	P I(41)		8.6	P.O. Failure Stress Domain P I(33)
				P.O. Failure Analysis Studies P I(00)
Radiation, Inc. (18)	PD I(71)	a)	8.2	Considered under Manufacturer
	PD I(64)	b)	8.4	P.O. Device Manufacturer BL I(25)
				Considered under Report Source*
Radio Corporation of America ([illegible])	RD I(71)	a)	8.2	Considered under Manufacturer
	RD I(6[illegible])	b)	8.4	P.O. Device Manufacturer BL I(25)
				Considered under Report Source*

Term	Code		Section	Disposition
Random Vibration*				See Vibration, Random
Raw Variables Data	GY I(48)		8.10	P.O. Test Results GY I(43)
				P.O. Part Level Data Y I(00)
Raytheon Company (12)	RD I(74), RD I(66)	a)	8.2	Considered under Manufacturer
		b)	8.4	P.O. Device Manufacturer BL I(25)
				Considered under Report Source*
RCTL	RD I(19)		8.1	P.O. Digital Logic RD I(13)
				Considered under Operational Type*
R/D Report	BL I(57)		8.4	Considered under Report Type*
R&D and Test Laboratories (Includes University Labs.)	BL I(40)		8.4	Considered under Sponsoring Organization*
R&D and Test Laboratories (Includes University Labs.)	BL I(29)		8.4	Considered under Report Source*
Redesign	OR I(99)		8.6	P.O. Corrective Measures OR I(89)
				P.O. Failure Analysis Studies P I(00)
Reliability and Environmental Test	OR I(30)		8.9	P.O. Facilities OR I(27)
				P.O. Reliability Technology OR I(00)
Reliability and Environmental Test Methods	W I(83)		8.8	P.O. Quality Assurance Specifications W I(80)
Reliability Attributes Summary	GY I(49)		8.10	P.O. Test Results GY I(43)
				P.O. Part Level Data Y I(00)
Reliability Data	OR I(72)		8.11	Considered under Applications
				Includes:
				Application Stress and Parts Counts OR I(73)
				Failure Modes OR I(74)
				Failure Rate Statistics OR I(75)

Reliability Data (cont'd)				Includes (cont'd)
				Malfunction Reports OR I(76)
				Test Reports OR I(77)
				Reliability Data NOC OR I(78)
Reliability Data NOC	OR I(78)		8.11	P.O. Reliability Data OR I(72)
				Considered under Applications
Reliability Demonstration	OR I(71)	a)	8.10	P.O. Quality Assurance Y I(03)
				Considered under Test Type*
				P.O. Part Level Data Y I(00)
		b)	8.11	Considered under Application Status*
				Considered under Applications
Reliability Rating (Maximum Failure Rate)			8.3	Considered under Environmental Capabilities*
				BK I(45) Less than 0.001% per 1000 hours
				BK I(46) 0.001 to less than 0.01% per 1000 hours
				BK I(47) 0.01 to less than 0.1% per 1000 hours
				BK I(48) Greater than 0.1% per 1000 hours
Reliability Technology	OR I(00)		8.9	Includes:
				Data Collection and Reduction OR I(23)
				Facilities OR I(27)
				General Methodology OR I(01)
				Prediction and Modeling OR I(02)
				Statistical Tools OR I(15)
				Test Techniques and Procedures OR I(03)

Report Date* 8.4 Includes:

BL I(00)	Prior to 1960
BL I(10)	1960
BL I(11)	1970
BL I(12)	1980
BL I(01)	1
BL I(02)	2
BL I(03)	3
BL I(04)	4
BL I(05)	5
BL I(06)	6
BL I(07)	7
BL I(08)	8
BL I(09)	9
BL I(51)	0

Report Security Classification* 8.4 See:

BL I(13)	Classified (see also Limited and/or Proprietary Information)
BL I(16)	Unclassified (see also Limited, and/or Proprietary Information)
BL I(17)	Limited
BL I(18)	Proprietary Infor ion

Report Source* 8.4 See:

Device Manufacturer BL I(25)

Device User (Equipment Mfgr/ Systems Contractors) BL I(26)

Industry Associations (ASTM, IEEE) BL I(27)

Military and Space BL I(19)

Report Source* (cont'd) — 8.4 See (cont'd)

- Non-Military Government Agency (Other than NASA) BL I(28)
- R&D and Test Laboratories (Includes University Labs.) BL I(29)

Report Type* — 8.4 See:

- Bibliography BL I(50)
- Case Study OR I(80)
- Drawings BL I(52)
- IITRI Generated Device Descriptors BL I(53)
- IITRI Generated Document Summary BL I(54)
- Journal Article BL I(55)
- Proceedings, Symposia, Conference BL I(56)
- R/D Report BL I(57)
- Specifications BL I(58)
- Survey and Review BL I(59)
- Technical Report BL I(65)
- Test Data BL I(66)
- Vendor Report BL I(67)

Residual Gas Analysis — W I(59) — 8.7

- P.O. Process Control Techniques W I(55)
- P.O. Fabrication Techniques and Equipment W I(00)

Resistance Weld — GN I(9[illegible])

a) 8.7

- P.O. Lead Attachment Processes and Equipment W I(50)
- P.O. Fabrication Techniques and Equipment W I(00)

b) 8.3 P.O. Lead Terminal Bond Mode GN I(92)

Resistive	RD I(42)		8.1	P.O. Isolation Method RD I(34)
Resistivity	GY I(97)		8.3	P.O. Device Parameters GY I(93)
Resistor	GN I(42)		8.3	P.O. Circuit Component GN I(00)
				Considered under MEL Device Element Descriptor*
				Includes:
				Diffused Resistor GN I(43)
				Discrete Resistor GN I(44)
				Film GN I(27)
				Variable GN I(29)
Resonance	SD I(47)		8.5	P.O. Physical Phenomena SD I(23)
				P.O. Circuit/Device Theory SD I(00)
Resonant Gate FET	GN I(51)		8.3	P.O. Special Active Devices NOC GN I(48)
				P.O. Circuit Component GN I(00)
				Considered under MEL Device Element Descriptor*
Reverse Break-down	SD I(48)		8.5	P.O. Physical Phenomena SD I(23)
				P.O. Circuit/Device Theory SD I(00)
RF Amplifier	BK I(67)		8.3	P.O. Circuit Functions BK I(49)
RF-IF Amplifier	RD I(48)		8.1	Considered under Circuit Complexity*.
RF Interference	GY I(33)		8.10	P.O. Environmental Conditions GY I(24)
				P.O. Part Level Data Y I(00)
RTL	RD I(20)		8.1	P.O. Digital Logic RD I(13)
				Considered under Operational Type*
Salt Atmosphere/ Spray	P I(42)	a)	8.4	P.O. Failure Stress Domain P I(33)
				P.O. Failure Analysis Studies P I(00)
		b)	8.10	P.O. Environmental Conditions GY I(24)
				P.O. Part Level Data Y I(00)

Term	Code		Related Terms
Sand and Dust	P I(43)	8.4	P.O. Failure Stress Domain P I(33) P.O. Failure Analysis Studies P I(00)
Sanders (12)	SD I(59) SD I(92)	8.4	P.O. Device User BL I(26) Considered under Report Source*
Sapphire	BK II(50)	8.3	P.O. Substrate Materials BK II(46) Considered under Non-Functional Elements* P.O. Device Element Materials BK II(26)
Satellite Launch	OR I(53)	8.11	P.O. Spacecraft Environment OR I(51) P.O. Application Environment OR I(35) Considered under Applications
Satellite Orbit (Flight)	OR I(54)	8.11	P.O. Spacecraft Environment OR I(51) P.O. Application Environment OR I(35) Considered under Applications
Scale of Integration*		8.3	See: LSI BK I(83) MSI BK I(84) SSI BK I(85)
Schottkey Barrier Diode	GN I(35)	8.3	P.O. Diode GN I(30) P.O. Circuit Component GN I(00) Considered under MEL Device Element Descriptors*
SCR (Silicon Controlled Rectifier*)	GN I(05)	8.3	P.O. PNPN Devices GN I(01) P.O. Circuit Component GN I(00) Considered under MEL Device Element Descriptors*
Scratches	P I(68)	8.6	P.O. Workmanship Defects P I(61) P.O. Causes of Failures P I(49) P.O. Failure Analysis Studies P I(00)

Term	Code	Section	Related Entries
Screening (Processing Control*)	Y I(09)	8.10	P.O. Quality Assurance Y I(03)
			Considered under Test Type*
			P.O. Part Level Data Y I(00)
Screening Procedures	OR I(11)	8.9	P.O. Test Techniques and Procedures OR I(03)
			P.O. Reliability Technology OR I(00)
Scribing	W I(35)	8.7	P.O. Assembly W I(30)
			P.O. Fabrication Techniques and Equipment W I(00)
SCS	GN I(06)	8.3	P.O. PNPN Devices GN I(01)
			P.O. Circuit Component GN I(00)
			Considered under MEL Device Element Descriptors*
Seal Leak	P I(88)	8.6	P.O. Physical Defects P I(70)
			P.O. Failure Analysis Studies P I(00)
Seam Weld	BK I(94)	a) 8.3	P.O. Package Seal BK I(90)
		b) 8.7	P.O. Encapsulation/Package Sealing W I(39)
			P.O. Fabrication Techniques and Equipment W I(00)
Secondary Breakdown	SD I(90)	8.6	P.O. Failure Phenomena SD I(78)
			P.O. Failure Analysis Studies P I(00)
Secret	BL I(15)	8.4	P.O. Classified BL I(13)
			Considered under Report Security Classification*
Semiconductor IC*			See Monolithic, NOC
Servo Amplifier	BK I(68)	8.3	P.O. Circuit Functions BK I(49)
Shear Modulus	SD I(55)	8.5	P.O. Metallurgical Phenomena SD I(53)
			P.O. Circuit/Device Theory SD I(00)

Term	Code		Section	Relations
Shipboard Environment	OR I(48)		8.11	P.O. Application Environment OR I(35)
				Considered under Applications
				Includes:
				Shipboard Submarine OR I(49)
				Shipboard Surface OR I(50)
Shipboard Submarine	OR I(49)		8.11	P.O. Shipboard Environment OR I(48)
				P.O. Application Environment OR I(35)
				Considered under Applications
Shipboard Surface	OR I(50)		8.11	P.O. Shipboard Environment OR I(48)
				P.O. Application Environment OR I(35)
				Considered under Applications
Shock				See Mechanical or Thermal Shock
Shockley 4-Layer Diode	GN I(07)		8.3	P.O. PNPN Devices GN I(01)
				P.O. Circuit Component GN I(00)
				Considered under MEL Device Element Descriptors*
Short Circuit	P I(52)		8.6	P.O. Failure Mode P I(27)
				P.O. Failure Analysis Studies P I(00)
Signal Processing (Buffers, Converters, Amplifiers)	OR I(64)		8.11	Considered under Equipment Class*
				Considered under Applications
Signetics Corp. (13)	RD I(74) RD I(67)	a)	8.4	P.O. Device Manufacturer BL I(25)
				Considered under Report Source*
		b)	8.2	Considered under Manufacturer
Silicon	BK II(51)		8.3	P.O. Substrate Materials BK II(46)
				Considered under Non-Functional Elements*
				P.O. Device Element Materials BK II(26)

Silicon Carbide	BK II(12)		8.3	P.O. Dielectrics and Insulating Materials BK II(08) Considered under Functional Elements* P.O. Device Element Materials BK II(26)
Silicon Nitride	BK II(55)	a)	8.3	P.O. Dielectrics and Insulating Materials BK II(08) Considered under Functional Elements* P.O. Device Element Materials BK II(26)
		b)	8.3	P.O. Surface Protection BK II(53) Considered under Non-Functional Elements* P.O. Device Element Materials BK II(26)
Silicon Oxide (SiO or SiO_2)	BK II(56)	a)	8.3	P.O. Dielectrics and Insulating Materials BK II(08) Considered under Functional Elements* P.O. Device Element Materials BK II(26)
		b)	8.3	P.O. Surface Protection BK II(53) Considered under Non-Functional Elements* P.O. Device Element Material BK II(26)
Siliconix, Inc. (14)	RD I(74) RD I(68)	a)	8.2	Considered under Manufacturer
		b)	8.4	P.O. Device Manufacturer BL I(25) Considered under Report Source*
Silk Screen	W I(25)		8.7	P.O. Thick Film W I(23) P.O. Deposition W I(22) P.O. Fabrication Techniques and Equipment W I(00)

Term	Code		Section	Reference
Silver	BK II(06)		8.3	P.O. Circuit Metallization Material BK II(00)
				Considered under Functional Element*
				P.O. Device Element Material BK II(26)
Simulated (i.e. gyrator)	GN I(41)		8.3	P.O. Inductor GN I(40)
				P.O. Circuit Component GN I(00)
				Considered under MEL Device Element Descriptors*
Single Ended	RD I(25)		8.1	P.O. Linear Device RD I(23)
				Considered under Operational Type*
Slide	BL I(76)		8.4	Considered under Document Format*
Small Signal	GN I(22)		8.3	P.O. Transistors GN I(09)
				P.O. Circuit Component GN I(00)
				Considered under MEL Device Element Descriptors*
Solder	GN I(96)	a)	8.7	P.O. Die Bonding W I(32)
				P.O. Assembly W I(30)
				P.O. Fabrication Techniques and Equipment W I(00)
		b)	8.3	P.O. Die Bonding Material BK II(58)
				Considered under Non Functional Elements*
				P.O. Device Element Material BK II(26)
		c)	8.3	P.O. Lead/Terminal Bond Mode GN I(92)
Soldered	GN I(89)	a)	8.3	P.O. Lead Attachment Modes GN I(83)
		b)	8.7	P.O. Lead Attachment Processes and Equipment W I(50)
				P.O. Fabrication Techniques and Equipment W I(00)

Term	Code	Section	Reference
Soldering Heat	GY I(36)	8.10	P.O. Environmental Conditions CY I(24)
			P.O. Part Level Data Y I(00)
SOS	GN I(81)	8.3	P.O. IGFET GN I(13)
			P.O. FET GN I(12)
			P.O. Transistors GN I(09)
			P.O. Circuit Component GN I(00)
			Considered under MEL Device Element Descriptors*
Source (FET)	GN I(71)	8.3	Considered under Circuit Component Regions*
			Considered under MEL Device Element Descriptors*
Spacecraft Environment	OR I(51)	8.11	P.O. Application Environment OR I(55)
			Considered under Applications
			Includes:
			Ground Checkout OR I(52)
			Satellite Launch OR I(53)
			Satellite Orbit (Flight) OR I(54)
Special NOC	RD I(51)	a) 8.1	Considered under Circuit Complexity*
		b) 8.3	P.O. Circuit Functions BK I(49)
Special Active Devices NOC	GN I(48)	8.3	P.O. Circuit Component GN I(00)
			Considered under MEL Device Element Descriptors*
			Includes:
			Acoustical Transducer GN I(49)
			Cryotron GN I(50)
			Resonant Gate FET GN I(51)
Special Military	Y I(19)	8.10	Considered under Specification Reference*
			P.O. Part Level Data Y I(00)

Term	Code			Entry
Special Reliability Study	Y I(10)		8.10	Considered under Test Type*
				P.O. Part Level Data Y I(00)
Specific Information	BL I(69)		8.4	P.O. Vendor Report BL I(67)
				Considered under Report Type*
Specification Reference*			8.10	P.O. Part Level Data Y I(00)
				See:
				MIL-M-23700 Y I(11)
				MIL-S-19500 Y I(12)
				MIL-STD-202 Y I(13)
				MIL-STD-750 Y I(14)
				NASA Y I(15)
				RADC Spec. #2867 Y I(16)
				User Procurement Y I(17)
				Vendor Y I(18)
				Special Military Y I(19)
Specifications	BL I(58)		8.4	Considered under Report Type*
Spectrographic Analysis	P I(13)		8.6	P.O. Failure Analysis Techniques P I(01)
				P.O. Failure Analysis Studies P I(00)
Sperry Gyroscope (13)	SD I(59) SD I(93)		8.4	P.O. Device User BL I(26)
				Considered under Report Source*
Sperry Semiconductor (15)	RD I(74) RD I(69)	a)	8.2	Considered under Manufacturer
		b)	8.4	P.O. Device Manufacturer BL I(25)
				Considered under Report Source*
Sponsoring Organization*			8.4	See:
				Device Manufacturer BL I(36)
				Device User (Equipment Mfgr/ Systems Contractors) BL I(37)

Sponsoring Organization (cont'd)				See (cont'd)
				Industry Associations (ASTM, IEEE) BL I(38)
				Military and Space BL I(30)
				Non-Military Government Agency (Other than NASA) BL I(39)
				R&D and Test Laboratories (Includes University Labs.) BL I(40)
Sprague Electric Co. (16)	RD I(74)	a)	8.2	Considered under Manufacturer
	RD I(70)	b)	8.4	P.O. Device Manufacturer BL I(25)
				Considered under Report Source*
Sputtering	W I(27)		8.7	P.O. Thin Film W I(26)
				P.O. Deposition W I(22)
				P.O. Fabrication Techniques and Equipment W I(00)
SSI (Small Scale Integration*)	BK I(85)		8.3	Considered under Scale of Integration*
Stacked-Arrays	GN I(90)		8.3	P.O. Lead Attachment Modes GN I(93)
Statistical Tools	OR I(15)		8.9	P.O. Reliability Technology OR I(00)
				Includes:
				Acceleration Factors OR I(16)
				Attributes Data Analysis OR I(17)
				Design of Experiments OR I(18)
				Exponential Distribution OR I(19)
				Machine Processing OR I(20)
				Variables Data Analysis OR I(21)
				Weibull Analysis OR I(22)
Step Stress Test	Y I(73)		8.10	P.O. Part Level Data Y I(00)
				Includes:
				Step Stress Domain*
				Step Stress Maximum Temperature

Step Stress Test Domain*

8.10 P.O. Step Stress Test Y I(73)

P.O. Part Level Data Y I(00)

See:

Atmospheric Environments Y I(74)

Current Y I(75)

High Temperature Y I(76)

Mechanical Environments Y I(77)

Power Y I(78)

Thermal Environments Y I(79)

Voltage Y I(80)

Combination Y I(81)

Step Stress Test Maximum Temperature

8.10 P.O. Step Stress Test Y I(73)

P.O. Part Level Data Y I(00)

Y I(82) < 21 C

Y I(83) 21°C to $<$ 102.5°C

Y I(84) 102.5°C to $<$ 202.5°C

Y I(85) 202.5°C to $<$ 302.5°C

Y I(86) $\geq$302.5°C

Step Stress Testing OR I(12)

8.9 P.O. Test Techniques and Procedures OR I(03)

P.O. Reliability Technology OR I(00)

Stitch TC Bond GN I(97)

a) 8.7 P.O. Thermo Compression Bonding W I(38)

P.O. Lead/Terminal Bonding W I(37)

P.O. Assembly W I(30)

P.O. Fabrication Techniques and Equipment W I(00)

b) 8.3 P.O. Lead Terminal Bond Mode GN I(92)

Storage Element	RD I(49)	8.1	Considered under Circuit Complexity*
Storage Element			See: Magnetic Film Superconducting Storage Element
Storage Life Test Temperature		8.10	P.O. Part Level Data Y I(00) Y I(44) < 21°C Y I(45) 21°C to < 102.5°C Y I(46) 102.5°C to < 152.5°C Y I(47) 152.5°C to < 202.5°C Y I(48) 202.5 C to < 302.5°C Y I(49) ≥302.5°C
Storage Time	SD I(19)	8.5	P.O. Physical Parameters SD I(07) P.O. Circuit/Device Theory SD I(00)
Strip Line Filters	GN I(38)	8.3	P.O. Distributed Passive Device GN I(37) P.O. Circuit Component GN I(00) Considered under MEL Device Element Descriptors*
Submarine			See Shipboard Submarine
Sub-Optical Electromagnetic Energization (Non-IR)	P I(14)	8.6	P.O. Failure Analysis Techniques P I(01) P.O. Failure Analysis Studies P I(00)
Substrate Materials	BK II(46)	8.3	Considered under Non-Functional Elements* P.O. Device Element Materials BK II(26) Includes: Alumina BK II(47) Ceramics BK II(48) Germanium BK II(49)

Substrate Materials (cont'd)			Includes (cont'd) Glass RD I(89) Sapphire BK II(50) Silicon BK II(51) Substrate Materials NOC BK II(52)
Substrate Materials NOC	BK II(52)	8.3	P.O. Substrate Materials BK II(46) Considered under Non-Functional Elements* P.O. Device Element Materials BK II(26)
Superconductivity	SD I(49)	8.5	P.O. Physical Phenomena SD I(23) P.O. Circuit/Device Theory SD I(00)
Surface Environment			See Shipboard Surface
Surface Passivation	W I(21)	87	P.O. Fabrication Techniques and Equipment W I(00)
Surface Protection	BK II(53)	8.3	Considered under Non-Functional Elements* P.O. Device Element Materials BK II(26) Includes: Glass RD I(89) Silicon Nitride BK II(55) Silicon Oxide (SiO or SiO_2) BK II(56) Passivated NOC BK II(57)
Survey and Review	BL I(59	8.4	Considered under Report Type* Includes: Application BL I(60) Available Devices/Circuits/Functions BL I(61) Equipment BL I(62) Packaging BL I(63)

Survey and Review (cont'd)				Includes (cont'd)
				Processing BL I(64)
Sylvania (14)	SD I(59) SD I(94)		8.4	P.O. Device User BL I(26)
				Considered under Report Source*
Sylvania Electric Products, Inc. (17)	RD I(74) RD I(71)	a)	8.2	Considered under Manufacturer
		b)	8.4	P.O. Device Manufacturer BL I(25)
				Considered under Report Source*
Systems Effect-iveness*			8.11	Other NOC
System Applica-tion	OR I(86)		8.1c	P.O. Application Design Techniques and Considerations OR I(79)
				Considered under Applications
Tantalum	BK II(44)		8.3	P.O. Materials NOC BK II(13)
				Considered under Functional Elements*
				P.O. Device Element Materials BK II(26)
Tantalum Oxide	BK II(15)		8.3	P.O. Dielectrics and Insulating Materials BK II(08)
				Considered under Functional Elements*
				P.O. Device Element Materials BK II(26)
Technical Report	BL I(65)		8.4	Considered under Report Type*
Teledyne (15)	SD I(59) SD I(95)		8.4	P.O. Device User BL I(26)
				Considered under Report Source*
Temperature	Y I(53)		8.10	Considered under Intermittent Stress Domain*
				P.O. Intermittent Life Test Y I(50)
				P.O. Part Level Data Y I(00)

Temperature (cont'd)			See also:
			Environmental Capabilities*
			Operational Static Life Test Temperature
			Storage Life Test Temperature
			Intermittent Life Test Temperature
			Step Stress Test Maximum Temperature
			Accelerated Life Test Maximum Temperature
			Operational Dynamic Test Maximum Temperature
Temperature ≥102.5°C	P I(44)	8.6	P.O. Failure Stress Domain P I(33)
			P.O. Failure Analysis Studies P I(00)
Temperature ≤-42.5°C	P I(45)	8.6	P.O. Failure Stress Domain P I(33)
			P.O. Failure Analysis Studies P I(00)
Temperature Cycling	GY I(37)	8.10	P.O. Environmental Conditions GY I(24)
			P.O. Part Level Data Y I(00)
Terminals	GN I(72)	8.9	Considered under Circuit Components Regions*
			Considered under MEL Device Element Descriptors*
Terminal Strength (Lead Pull)	GY I(38)	8.10	P.O. Environmental Conditions GY I(24)
			P.O. Part Level Data Y I(00)
Terminators	GN I(39)	8.3	P.O. Distributed Passive Device GN I(37)
			P.O. Circuit Component GN I(00)
			Considered under MEL Device Element Descriptors*

Test Data	BL I(66)	8.4	Considered under Report Type*
Test Equipment/ Procedures Approved by Non-Resident Source-Sponsor Representative	BL I(48)	8.4	Considered under Data Validation*
Test Equipment/ Procedures Approved by Resident Source-Sponsor Agent	BL I(49)	8.4	Considered under Data Validation*
Test Pattern	SD I(75)	8.5	P.O. Functional/Circuit Design and Optimization SD I(71)
Test Pattern, Use of			See Use of Test Pattern W I(60)
Test Reports	OR I(77)	8.11	P.O. Reliability Data OR I(72) Considered under Applications
Test Results	GY I(43)	8.10	P.O. Part Level Data Y I(00) Includes: Acceleration Factors OR I(16) Attributes, Summary GY I(45) Failure Analysis Results GY I(46) Performance Curves GY I(47) Raw Variables Data GY I(48) Reliability Attributes Summary GY I(49) Variable Analysis Summaries GY I(50)
Test Techniques and Procedures	OR I(03)	8.9	P.O. Reliability Technology OR I(00) Includes: Accelerated Testing OR I(04)

Term	Code		Mapping
Test Techniques and Procedures (cont'd)			Includes (cont'd) Agree Testing OR I(05) Atmospheric Stress Testing OR I(06) Burn-In Procedures OR I(07) Mechanical Stress Testing OR I(08) Operating Tests OR I(09) Radiation Environments OR I(10) Screening Procedures OR I(11) Step Stress Testing OR I(12) Thermal Stress Testing OR I(13) Test Techniques and Procedures NOC OR I(14)
Test Techniques and Procedures NOC	OR I(14)	8.9	Test Techniques and Procedures OR I(03) P.O. Reliability Technology OR I(00)
Test Type*		8.10	P.O. Part Level Data Y I(00) See: Developmental (Experimental*) OR I(96) Performance Y I(02) Quality Assurance (Device Test Oriented*) Y I(03) Special Reliability Study Y I(10)
Testing	SD I(70)	8.5	P.O. Circuit, Device Implementation SD I(60) See Electrical Characterization E I(05)

Term	Code			Disposition
Texas Instruments Inc. (18)	RD I(74) RD I(72)	a)	8.2	Considered under Manufacturer
		b)	8.4	P.O. Device Manufacturer BL I(25)
				Considered under Report Source*
TFIC*				See Thin Film - Pure IC
Thermal Conduction	SD I(50)		8.5	P.O. Physical Phenomena SD I(23)
				P.O. Circuit/Device Theory SD I(00)
Thermal Conductivity	SD I(20)		8.5	P.O. Physical Parameters SD I(07)
				P.O. Circuit/Device Theory SD I(00)
Thermal Diffusivity	SD I(21)		8.5	P.O. Physical Parameters SD I(07)
				P.O. Circuit/Device Theory SD I(00)
Thermal Environments	Y I(79)		8.10	Considered under Step Stress Test Domain*
				P.O. Step Stress Test Y I(73)
				P.O. Part Level Data Y I(00)
Thermal Environments	Y I(93)		8.10	Considered under Accelerated Life Test Domain*
				P.O. Accelerated Life Test Y I(87)
				P.O. Part Level Data Y I(00)
Thermal Shock	P I(46)	a)	8.6	P.O. Failure Stress Domain P I(33)
				P.O. Failure Analysis Studies P I(00)
		b)	8.10	P.O. Environmental Conditions GY I(24)
				P.O. Part Level Data Y I(00)

Term	Code			Related Terms
Thermal Stress Testing	OR I(13)		79	P.O. Test Techniques and Procedures OR I(03)
				P.O. Reliability Technology OR I(00)
Thermo Compression Bonding	W I(38)		8.7	P.O. Lead/Terminal Bonding W I(37)
				P.O. Assembly W I(30)
				P.O. Fabrication Techniques and Equipment W I(00)
				Includes:
				Ball TC Bond GN I(93)
				Stitch TC Bond GN I(97)
				Wedge TC Bond GN I(99)
Thermoelectric Effects	SD I(51)		8.5	P.O. Physical Phenomena SD I(23)
				P.O. Circuit/Device Theory SD I(00)
Thick Film	W I(23)	a)	8.7	P.O. Deposition W I(22)
				P.O. Fabrication Techniques and Equipment W I(00)
				Includes:
				Metal Screen W I(24)
				Silk Screen W I(25)
		b)	8.3	P.O. Film GN I(27)
Thick Film Pure IC (Passive Substrate IC*)	RD I(09)		8/	Considered under Microelectronic Category*
Thin Film	W I(26)	a)	87	P.O. Deposition W I(22)
				P.O. Fabrication Techniques and Equipment W I(00)
				Includes:
				Sputtering W I(27)
				Vacuum Deposition W I(28)
				Vapor Plating W I(29)
		b)	8.3	P.O. Film GN I(27)

Thin Film	GN I(82)	8.3	P.O. IGFET GN I(13) P.O. FET GN I(12) P.O. Transistor GN I(09) P.O. Circuit Component GN I(00) Considered under MEL Device Element Descriptors*
Thin Film - Pure IC (TFIC*, Passive Substrate IC*)	RD I(10)	8.1	Considered under Microelectronic Category*
Tin	BK II(45)	8.3	P.O. Materials NOC BK II(13) Considered under Functional Elements* P.O. Device Element Material BK II(26)
Titanium Dioxide	BK II(16)	8.3	P.O. Dielectrics and Insulating Materials BK II(08) Considered under Functional Elements* P.O. Device Element Material BK II(26)
T^2L*			See TTL
TO-			See Package Type
Tolerances	SD I(76)	8.5	P.O. Functional Circuit Design and Optimization SD I(71)
Trade-Offs	SD I(77)	8.5	P.O. Functional/Circuit Design and Optimization SD I(71)
Transconductance	GY I(98)	8.3	P.O. Device Parameters GY I(93)
Transistors	GN I(09)	8.3	P.O. Circuit Component GN I(00) Considered under MEL Device Element Descriptors* Includes: Bipolar Transistors GN I(10) Complementary GN I(11)

Term	Code		Relation
Transistors (cont'd)			Includes (cont'd)
			FET (Field Effect Transistor*) GN I(12)
			Multiple Emitter GN I(17)
			NPN GN I(18)
			PNP GN I(19)
			PNP - lateral GN I(20)
			Power GN I(21)
			Small Signal GN I(22)
			Unijunction GN I(23)
Transitron Electronic Corp. (19)	RD I(74) RD I(73)	a) 8.2	Considered under Manufacturer
		b) 84	P.O. Device Manufacturer BL I(25)
			Considered under Report Source*
TRIAC (Bilateral Triode Switch*)	GN I(08)	83	P.O. PNPN Devices GN I(01)
			P.O. Circuit Component GN I(00)
			Considered under MEL Device Element Descriptors*
TTL (T^2L*)	RD I(21)	81	P.O. Digital Logic RD I(13)
			Considered under Operational Type*
Tunnel Diode	GN I(36)	8.3	P.O. Diode GN I(30)
			P.O. Circuit Component GN I(00)
			Considered under MEL Device Element Descriptors*
Ultrasonic Bond	GN I(98)	a) 8.3	P.O. Lead/Terminal Bond Mode GN I(92)
		b) 8.7	P.O. Lead/Terminal Bonding W I(37)
			P.O. Assembly W I(30)
			P.O. Fabrication Techniques and Equipment W I(00)

Ultrasonic Inspection	P I(15)		8.6	P.O. Failure Analysis Techniques P I(01)
				P.O. Failure Analysis Studies P I(00)
Unclassified	BL I(16)		8.4	Considered under Report Security Classification*
				See:
				Limited BL I(17) and/or Proprietary Information BL I(18)
Unijunction	GN I(23)		8.3	P.O. Transistors GN I(09)
				P.O. Circuit Component GN I(00)
				Considered under MEL Device Element Descriptors*
Union Carbide Electronics (20)	RD I(75)	a)	8.2	Considered under Manufacturer
		b)	8.4	P.O. Device Manufacturer BL I(25)
				Considered under Report Source*
Unspecified Equipment Class	OR I(66)		8.11	Considered under Equipment Class*
				Considered under Applications
Unspecified Environment	OR I(55)		8.11	P.O. Application Environment OR I(35)
				Considered under Applications
Use of Test Patterns	W I(60)		8.7	P.O. Process Control Techniques W I(55)
				P.O. Fabrication Techniques and Equipment W I(00)
User Procurement	Y I(17)		8.10	Considered under Specification Reference*
				P.O. Part Level Data Y I(00)
User Proprietary Screening and Burn In Specifications	W I(84)		8.8	P.O. Quality Assurance Specifications W I(80)
Vacuum	P I(47)		8.6	P.O. Failure Stress Domain P I(33)
				P.O. Failure Analysis Studies P I(00)

Term	Code			Disposition
Vacuum Deposition	W I(28)		8.7	P.O. Thin Film W I(26)
				P.O. Deposition W I(22)
				P.O. Fabrication Techniques and Equipment W I(00)
Value Engineering*			8.12	Other NOC
Vapor Plating	W I(29)		8.7	P.O. Thin Film W I(26)
				P.O. Deposition W I(22)
				P.O. Fabrication Techniques and Equipment W I(00)
Variable	GN I(29)	a)	8.3	P.O. Capacitors GN I(24)
				P.O. Circuit Component GN I(00)
				Considered under MEL Device Element Descriptors*
		b)	8.3	P.O. Resistor GN I(42)
				P.O. Circuit Component GN I(00)
				Considered under MEL Device Element Descriptors*
Variables Analysis Summaries	GY I(59)		8.16	P.O. Test Results GY I(43)
				P.O. Part Level Data Y I(00)
Variables Data Analysis	OR I(21)		8.9	P.O. Statistical Tools OR I(15)
				P.O. Reliability Technology OR I(00)
Vendor	Y I(18)		8.10	Considered under Specification Reference*
				P.O. Part Level Data Y I(00)
Vendor Report	BL I(67)		8.4	Considered under Report Type*
				Includes:
				General Catalog BL I(68)
				Specific Information BL I(69)
Vendor Application Notes	OR I(87)		8.11	Considered under Applications

Vendor QA Plans and Specifications (performance specs)	W I(85)		8.8	P.O. Quality Assurance Specifications W I(80)
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				P.O. Failure Analysis Studies P I(00)
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				P.O. Part Level Data Y I(00)
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				P.O Part Level Data Y I(00)
Vibration, Variable Frequency	GY I(42)		8.10	P.O. Environmental Conditions GY I(24)
				P.O. Part Level Data Y I(00)
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		b)	8.1	Considered under Circuit Complexity*
Visual Inspection	P I(16)		8.6	P.O. Failure Analysis Techniques P I(01)
				P.O. Failure Analysis Studies P I(00)
Voltage	Y I(54)		8.10	Considered under Intermittent Stress Domain*
				P.O. Intermittent Life Test Y I(50)
				P.O. Part Level Data Y I(00)
				P.O. Voltage (All) GY I(61)
Voltage	Y I(80)		8.10	Considered under Step Stress Test Domain*
				P.O. Step Stress Test Y I(73)
				P.O. Part Level Data Y I(00)
				P.O. Voltage (All) GY I(61)

Voltage	Y I(94)	8.10	Considered under Accelerated Life Test Domain*
			P.O. Accelerated Life Test Y I(87)
			P.O. Part Level Data Y I(00)
			P.O. Voltage (All) GY I(61)
Voltage (All)	GY I(61)	8.3	Unqualified terms
Voltage Regulator	BK I(70)	a) 8.3	P.O. Circuit Functions BK I(49)
		b) 8.3	P.O. Diode GN I(30)
			P.O. Circuit Component GN I(00)
			Considered under MEL Device Element Descriptors*
Wafer Cutting	W I(05)	8.7	P.O. Wafer Preparation W I(04)
			P.O. Fabrication Techniques and Equipment W I(00)
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			P.O. Fabrication Techniques and Equipment W I(00)
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			P.O. Fabrication Techniques and Equipment W I(00)
Wafer Polishing	W I(08)	8.7	P.O. Wafer Preparation W I(04)
			P.O. Fabrication Techniques and Equipment W I(00)
Wafer Preparation	W I(04)	8.7	P.O. Fabrication Techniques and Equipment W I(00)
			Includes:
			Wafer Cutting W I(05)
			Wafer Etching W I(06)
			Wafer Lapping W I(07)
			Wafer Polishing W I(08)

Washing	W I(19)		8.7	P.O. Photolithography W I(14)
				P.O. Fabrication Techniques and Equipment W I(00)
Washing	W I(34)		8.7	P.O. Assembly W I(30)
				P.O. Fabrication Techniques and Equipment W I(00)
Wedge TC Bond	GN I(99)	a)	8.7	P.O. Thermo Compression Bonding W I(38)
				P.O. Assembly W I(30)
				P.O. Lead/Terminal Bonding W I(37)
				P.O. Fabrication Techniques and Equipment W I(00)
		b)	8.3	P.O. Lead/Terminal Bond Mode GN I(92)
Weibull Analysis	OR I(22)		8.9	P.O. Statistical Tools OR I(15)
				P.O. Reliability Technology OR I(00)
Welded	GN I(91)		8.3	P.O. Lead Attachment Modes GN I(83)
Westinghouse Electric Corp. (21)	RD I(75) RD I(65)	a)	8.2	Considered under Manufacturer
		b)	8.4	P.O. Device Manufacturer BL I(25)
				Considered under Report Source*
Wire Bonding*				See Lead/Terminal Bonding
Wire Material	BK II(27)		8.3	Considered under Functional Elements*
				P.O. Device Element Materials BK II(26)
				Includes:
				Aluminum BK II(28)
				Gold BK II(29)
				Wire Material NOC BK II(30)

Wire Material NOC	BK II(30)	8.3	P.O. Wire Material BK II(27) Considered under Functional Elements* P.O. Device Element Materials BK II(26)
Work Function	SD I(22)	8.5	P.O. Physical Parameters SD I(07) P.O. Circuit/Device Theory SD I(00)
Work Hardening	SD I(56)	8.5	P.O. Metallurgical Phenomena SD I(53) P.O. Circuit/Device Theory SD I(00)
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Young's Modulus	SD 1(57)	8.5	P.O. Metallurgical Phenomena SD 1(05)
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10.0 RAC APPLICABLE TERM DEFINITIONS

The definitions cited here are for use in correlation with the Structured Term List, Section 8.0, and the Alphabetical Term List, Section 9.0. These definitions are intended to explain the technical meaning and system use of the term. The terms have been defined as they pertain to microelectronic usage with the RAC system. If a term has more than one primary usage and each usage was considered important to the RAC system, the term has been defined for each primary usage.

MAJOR CATEGORY headings and MAJOR TERMS within the categories are typed in upper-case letters. Terms related to the major terms are typed in lower-case letters. System related concepts are identified as "see" terms.

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ACCELERATED LIFE MAXIMUM TEST TEMPERATURE:

(Ambient Temperature Condition, Accelerated)

The environmental condition of ambient thermal severity at the maximum level of conducting the "ACCELERATED LIFE TEST".

Accelerated Life Max. Test Temperature <21°C:

Thermal severity level is less than 21 degrees Centigrade.

Accelerated Life Max. Test Temperature 21°C to <102.5°C:

Thermal severity level is in the range from 21 degrees to less than 102.5 degrees Centigrade.

Accelerated Life Max. Test Temperature 102.5°C to <202.5°C:

Thermal severity level is in the range from 102.5 degrees to less than 202.5 degrees Centigrade.

Accelerated Life Max. Test Temperature 202.5°C to <302.5°C:

Thermal severity level is in the range from 202.5 degrees to less than 302.5 degrees Centigrade.

Accelerated Life Max. Test Temperature ≥302.5°C:

Thermal severity level is in the range greater than or equal to 302.5 degrees Centigrade.

ACCELERATED LIFE TEST:

An "Operating Test(s)", environmental test or a test combination of these, which is conducted in accordance with "Accelerated Testing" procedures. (See "Accelerated Testing (TEST TECHNIQUES & PROCEDURES)").

ACCELERATED LIFE TEST DOMAIN:

The specific nature of the externally applied test stress(es) of the "ACCELERATED LIFE TEST".

Accelerated Testing:

Testing in which the applied stress severity level is chosen to exceed that stated in the reference conditions in order to shorten the time required to observe the stress response of the item, or magnify the response in a given time. Purpose of such testing is to achieve these results without altering the basic mechanisms of failure, or their relative prevalence. On this basis, "Accelerated Testing" is usually performed at a fixed level of elevated severity. "Step Stress Testing" is covered by another descriptor.

Acceleration Factors:

(See "Acceleration Factors: STATISTICAL TOOLS").

Acceleration Factors:

Ratios between the times required to obtain given proportions of failures, each for two different sets of stress severity conditions and which involve the same failure mechanisms and/or failure modes.

Acoustic Noise:

(Audio Noise, Sonic Vibration)

Application of or exposure to (of the device or assembly of devices) random fluctuations of energy in the audio range. (See "Failure Stress Domain, Noise, Acoustical").

Acoustical Transducer:

Any device which changes electrical energy to mechanical energy, or vice versa.

Activity Monitored by Source-Sponsor Representative (Data Validation):

Reported testing was witnessed by a representative of the SPONSORING ORGANIZATION, as ascertained by the representative's stamp or seal and signature of the responsible official of the SOURCE organization.

Activity Witnessed and Report Countersigned by Source-Sponsor Agent (Data Validation):

This DATA VALIDATION ranks first among the set of eight descriptors. Reported testing was witnessed by an agent of the SPONSORING ORGANIZATION and the documentation countersigned by this cognizant inspector.

Adder(s):

A Logic circuit the output of which is the sum of two inputs - with carry digit, in the case of a Full Adder, and without carry digit, in the case of a Half Adder.

AGREE TEST:

(See "AGREE Test (TEST TECHNIQUES AND PROCEDURES)").

AGREE Test:

A test procedure which conforms to recommendations set forth in the AGREE report, and in accordance with specifications or standards devised as an outgrowth of that report. (AGREE Report, Reliability of Military Electronic Equipment, DOD Advisory Group on the Reliability of Electronic Equipment, published by U. S. Government Printing Office, June 1957.) Documents based upon the AGREE report include MIL-STD-781 and the Established Reliability (ER) Military Specifications.

Although originally advocated with orientation toward test methods for equipment, essential AGREE concepts have been adopted for evaluations of devices or components. Such is an AGREE life test which requires that microelectronic devices be subjected to a combination of vibration, temperature cycling, and on-off electrical stressing to simulate as closely as possible actual system applications and environments (Method 1007: Military Standard (Proposed), Test Methods and Procedures for Microelectronics, Project 5962-0002: RADC (EMERM), Griffiss AFB, NY, 14 July 1967).

Airborne Manned:

(Airborne Inhabited)

An "Aircraft Environment" in which in-flight personnel must operate the system.

Airborne Unmanned:

(Airborne Uninhabited)

An "Aircraft Environment" in which remote operation of system obviates the need of in-flight personnel.

Aircraft Environment:

Application environment associated with an equipment system for flight through aerodynamic means.

Alloy Junction:

A p-n junction formed by alloying a metallic dopant with the semiconductor material.

Alloying:

The mixing of two or more metallic elements.

Alloying:

The mixing of a metallic material and a semiconductor to form a localized alloy. On solidifying a eutectic alloy precipitates from the mix and constitutes a heavily doped semiconductor region. This region in contact with the unalloyed semiconductor forms a p-n junction.

Alumina:

(Aluminum Oxide)

A dielectric compound of Aluminum from Group III of the Periodic Table and Oxygen from Group VI.

Aluminum:

An element of Group III of the Periodic Table which acts as an acceptor impurity in Si and Ge.

Aluminum:

(Al)

A metallic element of Atomic Number 13.

Aluminum Silicon Eutectic:

An alloy of aluminum and silicon of such composition that its melting point is a minimum in the phase diagram of the alloy system.

Aluminum-to-Aluminum, Direct (Al/Al, Direct; Aluminum-to-Aluminum, Inverted Chip; Aluminum-to-Aluminum, Flip Chip):

Inverted chip bonding with aluminum metallization material bonded to aluminum circuit metallization material. A wetting agent or intermediary material may be used. (See "INTERCONNECTION SYSTEM").

Aluminum-to-Aluminum, Wire Bond (Al/Al, Wire Bond):

An aluminum wire bonded to aluminum circuit metallization material. (See "Interconnection System").

Analog to Digital Converter (A/D Converter):

A circuit which converts a linear, or analog, signal to a train of digital pulses proportional to the properties of the linear signal.

AND Gate:

A logic gate with more than one input which gives an output of a logical "zero" if any of the inputs are a logical "zero", and an output of a logical "one" only if all inputs are a logical "one".

Anode:

The positive electrode in a semiconductor diode.

Antimony:

An element of Group V of the Periodic Table which acts as a donor impurity in Si and Ge.

APPLICATION DESIGN TECHNIQUES AND CONSIDERATIONS:

Major aspects and relations for device design compatibility with requirements of general applications. (See "FUNCTION/CIRCUIT DESIGN & OPTIMIZATION").

APPLICATION ENVIRONMENT:

(SERVICE ENVIRONMENT, APPLICATION USAGE, APPLICATION SEVERITY CLASS, SYSTEMS CATEGORY)

The comprehensive level of environmental conditions as associated with the category of systems application. (See "FAILURE ENVIRONMENT").

APPLICATION STATUS:

The state-of-the-art of applied technology in system service conditions. The maturity of system utilization.

Application Stress and Parts Counts:

(Device/Count Application Stress Summary)

A summary of number of devices by type, and their associated service environments, which are utilized in specific systems/ equipments.

APPLICATIONS:

Information and data concerning assemblies of devices for system service conditions (applications).

Arithmetic Functional Unit:

A digital circuit combining registers (assemblies of bistable multivibrators) and logic gates to perform elementary arithmetical operations. Such units include: adders and counters. (See "Adders, CIRCUIT FUNCTIONS").

Arsenic:

An element of Group V of the Periodic Table which acts as a donor impurity in Si and Ge.

ASSEMBLY:

Fitting together of all elements needed to produce a completed electronic device, e.g., circuit chip, header, hermetic seal, terminals, interconnections.

Astable Multivibrator:

A two stage regenerative circuit which, in the absence of external triggering, makes periodic transitions between two possible states.

Atmospheric Environments, Accelerated Life Test Domain:

Test stress domain consists of an environment as included by the "Atmospheric Stress Testing" descriptor. (See term, as organizationally grouped under "TEST TECHNIQUES AND PROCEDURES").

Atmospheric Environments, Step-Stress Test Domain:

Test stress domain consists of an environment as included by the "Atmospheric Stress Testing" descriptor. (See term, as organizationally grouped under "TEST TECHNIQUES AND PROCEDURES").

Atmospheric Stress Testing:

Environmental testing in which the applied stress domain is a severe condition of the device ambient atmosphere. Such stress domains include: vacuum, gas pressure, salt atmosphere/spray, and sand and dust. (See "Failure Stress Domain, Vacuum").

Attributes Data Analysis:

(Reduced Data Analysis, Summary Data Analysis)

Statistical analysis of reduced or summarized data wherein results are expressed in terms of specimen quality, i.e., "good-bad" and "conforming-defective", and analysis considers sample counts having the specified quality. (See "Attributes, Summary" and "Reliability Attributes Summary").

Attributes, Summary:

Reduced test or inspection data in terms of results which report the device count exhibiting a specified attribute or quality, i.e., "fail", "defective", etc., independent of time (non-stoichastic variable summary). (See "Attributes Data Analysis").

Audio Amp:

Classed as Audio Amplifiers are linear networks that are used primarily to amplify signals in the audio range, viz., DC to approximately 50 KHz, although circuits with gain bandwidth products in the megahertz region are found in the audio category.

Audio Video Tape Recording (Document Format):

RAC Library document is contained on an audio tape recording, a video tape recording, or a video film recording.

Automated Systems:

(Machine Processing)

Machine implemented techniques and provisions for recording, collection, or the summarization of reliability test or application monitored data. IC Testers is a term included by this descriptor.

AVAILABILITY:

Studies, and application of the concept, "Availability", a contributing parameter of systems effectiveness, which attempts to quantify and predict the probability that an equipment or system is operating satisfactorily at any point in time.

Ball TC Bonding:

Thermo-compression bonding in which the end of the wire is melted so as to form a ball. The ball is then flattened by the compressive bonding force to form a large area contact.

Bandwidth:

The frequency range between the one-half power (-3 db) response points of the amplifier.

Base:

In a bipolar transistor, the middle region in which current transfer from a low impedance circuit to a high impedance circuit occurs.

Basic Materials:

Materials from which device elements can be formed through subsequent processing.

Beam Lead:

Cantilivered beam conductors formed as an integral part of a microelectronic device by plating a thick metal film onto the wafer and etching the lead pattern, followed by an etching away of the semiconductor material between devices. (See "INTERNAL CONNECTION MODE: and "Dielectric, Air: ISOLATION METHOD").

Beveling:

Lapping of a semiconductor device on a shallow angle to the surface to expose the cross-section of the device for analysis.

Bibliography (Report Type):

A collection of references to relevant documents.

Bipolar Transistor:

A three-terminal solid state device consisting of alternate N-type and P-type semiconductor material separated by potential barriers. Power gain is achieved through the injection of current into the base region from a low impedance emitter region and transfer of that current to a high impedance collector region. Transistor action relies on the generation and recombination of hole-electron pairs, hence the term "bipolar".

Bistable Multivibrator:

(Flip Flop)

A two stage regenerative circuit capable of existing in either of two stable states and requiring an external trigger signal to switch to the opposite state.

Boron:

An element of Group III of the Periodic Table which acts as an acceptor impurity in Si and Ge.

Breadboarding; Circuit/Device Implementation:

(Pre-Product Simulation, Breadboard Modeling)

Techniques for check out of microelectronic device performance through utilization of basic device elements, such as discrete microcomponents and hybrid assemblies.

Broken Lead:

(Broken Interconnection Wiring, Broken Lead Wire)

A mechanical imperfection due to a break in the device terminal wires or leads.

Buried Layer:

A heavily doped (n+) region placed between substrate and epitaxial collector layer which, because of its high conductivity, is used to reduce the collector resistance of integrated transistors.

Burn-In Procedures:

(Product Conditioning Procedures)

Procedures associated with the post-production operation of devices for the purpose of stabilizing their characteristics and especially isolating unstable and marginal devices. (See "Failure Environment, Post-Production Screen/Burn-In").

Burn-In Test:

(Product Conditioning)

Testing directed toward the stabilization of device characteristics and especially to isolate unstable units and those with marginal life expectancy. (See "Burn-In Procedures").

Can, Hermetically Sealed:

A package which consists of a can, generally metal, with hermetically sealed header and pins, such as for the JEDEC TO-5 can. Other TO numbers which are included in this classification are listed as follows: (See "PACKAGE CONFIGURATION").

TO-5	TO-73	TO-76	TO-80
TO-70	TO-74	TO-77	TO-96
TO-71	TO-75	TO-78	TO-99
TO-72		TO-79	TO-100

Capacitance:

The measure of the ability of a capacitor to store electronic charge.

Carrier Concentration:

A measure of the number of free carriers per unit volume in a material.

Carrier Diffusion:

(Charge Carrier Diffusion)

The passage of charges through a material in the absence of an electrical field and as a result of charge concentration gradients.

Carrier Generation:

The removal of a bound electron from an atom in a crystal such that the electron and its vacated location in the atom (the hole) becomes free to contribute to electrical current in the material.

Carrier Generation Through Radiation:

Absorption of nuclear radiation by semiconductors can result in the ionization of atoms of the semiconductors, thus the generation of carriers which alters the conductivity of the device regions.

Carrier Injection:

The introduction of electronic charge carriers into a medium, such as the base region of a transistor, by application of appropriate bias potential.

Carrier Lifetime:

The time between generation and recombination, or injection and trapping, of charge carriers during which they are available to take part in the conduction process in a device.

Carrier Mobility:

The measure or the ease with which carriers may move within a particular medium or material; expressed as a velocity per unit electric field.

Carrier Recombination:

The uniting of a free electron with an ionized atom in a crystal such that the electron is no longer free to move in the material.

Carrier Velocity:

The velocity with which a carrier moves through a medium under the influence of a given electric field.

Case Study:

(Sample Design, Design Demonstration, Illustrative Design)

An illustration of a design or developmental approach with its documentation in the context of a specific system and device or device element.

Cathode:

The negative electrode in a semiconductor diode.

CAUSES OF FAILURES:

(Failure Activators, Failure Mechanisms)

The key conditions or circumstances to which may be assigned the activation of failure mechanisms. The major activities which contributively induce failure. Such causes are deducted from physical defects in failure analyses.

Ceramics:

An inorganic dielectric material.

Cermets and Glazes:

Mixtures of ceramic materials and metals having high value of resistivity.

Chemical Analysis:

(Stoichiometric Evaluation)

Analysis of the chemical constituents through conventional techniques of the chemical laboratory.

Chemical Phenomena:

Actions or events which occur to change the chemical nature or composition of a material.

Chromium:

A metallic element of Atomic Number 24.

CIRCUIT COMPLEXITY:

A generic index of the complexity of the device circuitry in terms of the relative scope of its function. (Also see "SCALE OF INTEGRATION" and "NUMBER OF MAJOR PROCESS STEPS").

Circuit Component:

An electrical element which, together with other elements, forms a microelectronic circuit.

Circuit Component Regions:

Specific local regions of a solid state device, active or passive, which are essential to the operation or construction of that device.

CIRCUIT/DEVICE IMPLEMENTATION:

(Circuit/Device Development)

Generalized principles entering into the development of microelectronic circuits, devices and device elements.

CIRCUIT/DEVICE THEORY:

Theoretical (generalized) considerations in the design and operation of microelectronic devices, circuits, and device elements.

CIRCUIT FUNCTIONS:

The roles microelectronic devices are designed to perform in electronic systems.

Circuit Layout:

(Circuit Topology)

The graphic delineation of the circuit configuration and the means of implementation upon the wafer surface, such as the associated photomasks.

Circuit Metallization Materials:

Materials used to form the metallic conductor for interconnection of elements of a microelectronic circuit.

CIRCUIT PARAMETERS:

The parameters of a microelectronic circuit which are used in calculating overall circuit performance. (See "ELECTRICAL PROPERTIES").

Classified (Report Security Classification):

RAC document's label, as indicated "Secret" or "Confidential", through authorization by the appropriate government agency.

CML (Digital Logic Type (Current Mode Logic))

A nonsaturating digital logic circuit configuration whose gates are characterized by the use of an individual transistor for each input, a common collector resistor for all input transistors, and a common emitter resistor for all input transistors and a reference transistor - that is, it has "differential type" configuration. This generic logic type includes the type proprietarily designated as MECL. (See "Differential (Linear Device Type)" and "Digital Logic Type").

Cold Welding:

The welding of two metals by the application of pressure only.

Collector:

In a bipolar transistor, the high impedance region into which current from the emitter is transferred through the base.

Combination, Accelerated Life Test Domain:

Stress conditions consist of combination of two or more "ACCELERATED LIFE TEST DOMAIN(S)".

Combination and NOC:

A combination of "EQUIPMENT CLASS(ES)" and/or an equipment class which is not otherwise classified in terms of descriptors in the current glossary. (See "Unspecified Equipment Class").

Combination, Step-Stress Test Domain:

Stress conditions consist of combination of two or more "STEP STRESS TEST DOMAIN(S)".

Combination With Environment Stresses; Intermittent Stress Domain:

Test stress consisting of a combination of electrical and environmental stress domains. (See "INTERMITTENT STRESS DOMAIN").

Common Mode Rejection Ratio:

In a differential amplifier, the ratio of the output voltage (or current) when the two input signals are in phase to the output voltage (or current) when the two input signals are 180° out of phase, but of the same magnitude.

Communications:

(Telecommunications)

A class of equipment which operates to transmit information.

Comparison with Discrete:

Study of the comparative relations in implementing an application with microelectronic devices versus the application of discrete component devices.

Complementary Transistors:

A pair of PNP and NPN bipolar transistors having identical performance characteristics but requiring power supplies of opposite polarity.

Composite IC, Diffused (Compatible Monolithic IC, Diffused; Monobrid, Diffused):

A composite IC in which monolithic diffusion technology is used to form all junctions. (See "Composite IC Microelectronic Category").

Composite IC, Epitaxial (Compatible Monolithic IC, Epitaxial; Monobrid, Epitaxial):

A composite IC in which monolithic epitaxial growth technology is used to form at least one junction. (See "Composite IC Microelectronic Category").

(Composite IC Microelectronic Category (Compatible Monolithic IC, Monobrid, Active Substrate IC))

An integrated circuit composed of a monolithic IC with at least one passive film circuit component deposited on the top surface of the monolithic die after the surface has been passivated. This Microelectronic Category excludes the "Monolithic IGFET" (see term) categories. (See "Integrated Circuit". "Monolithic Microelectronic Category", and "Film IC".)

Composite IC, NOC (Not-Otherwise Classified Compatible IC):

Composite IC microelectronic integrated circuits which cannot be classified within any descriptors of the current glossary. (See "Composite IC Microelectronic Category"; "Composite IC, Diffused"; and "Composite IC, Epitaxial").

Compound Formation:

The mixing of chemical elements in proper proportion to form stoichiometric compounds of those elements, e.g., cadmium and sulfur to form cadmium sulfide.

Computation:

(Digital Processers)

A class of equipment which processes information. Informational output is derived from input information through handling of data by logical processes.

Computer Aids:

(Computer-Aided LSI Design, Computer Simulation of Breadboarding)

General aspects of computer techniques, as utilized to facilitate evaluation and development of microelectronic devices or device elements.

Computer Analysis:

(Computer-Aided Design)

Computer-aided analysis and computer-assisted design, such as in the delineation of microelectronic circuits through "paper studies" with computer-aided approaches.

Confidential (Classified, Report Security Classification):

Unauthorized disclosure of informational content is forbidden, since such release could be prejudicial to the defense of the nation.

Constant Acceleration:

(Centrifuge)

Exposure to a constant rate of change of directed motion or centrifugal force. (See "Failure Stress Domain, Acceleration, Constant").

Consumer:

Devices are qualified for consumer type applications. (See "QUALIFICATION CLASS").

Contact Area:

The region of a device where electrical connection is made to one of its elements.

Contact Potential:

The work required to move a charge carrier from one material into another in contact with it.

Contamination:

(Material Impurity)

A physical defect due to the inadvertent introduction of impurities into combination with the device materials.

Control:

(Regulator)

A class of equipment which operates to regulate the operation of other equipment. Equipment which exercises programming or real-time command over the functions of the complete system. Descriptor is exclusive of "Navigation".

Conventional Microscopic Examination:

(Optical Microscopic Inspection)

Inspection with utilization of a conventional optical microscope, including stereographic adaptations.

Copper:

A metallic element of Atomic Number 29.

CORRECTIVE MEASURES:

(RE-WORK PROCEDURES, RETROFIT)

Procedures taken to eliminate failure mechanisms or quality defects, in response to analyses of failure.

Counter(s):

A chain of series connected binary logic elements capable of counting the number of input pulses.

Cracked Die:

(Cracked or Chipped Die, Broken Wafer)

A mechanical imperfection due to a break discontinuity in the die or wafer.

Cracked Package:

(Cracked or Chipped Package)

A mechanical imperfection due to a break discontinuity in the device package.

Crossover:

The physical crossing of two thin film conductors on the same substrate, embodied by the two metallic films being separated by a thin film of insulation material.

Cryotron:

A solid state device based on the phenomenon of superconductivity. A magnetic field generated by current in a control element causes a gate element to change from the superconducting state to the normally resistive state, thereby affecting the switching of logic signals.

Crystal Defects:

(Monocrystalline Flaws)

Bulk defects due to flaws in the lattice structures of single crystals.

Crystal Growth:

The formation of a relatively large crystal of a substance.

CTL (Digital Logic Type (Complementary Transistor Logic, CTL)):

A digital logic circuit configuration wherein the gates are characterized by the use of both PNP and NPN transistors, with each input connected to a transistor's base. (See "Digital Logic Type").

Current, Accelerated Life Test Domain:

(Electric Current Input)

An accelerated life test where stress domain of interest is input or load current.

Current, Intermittent Stress Domain:

(Electric Current)

Rate of transfer of electrical charge.

Current, Step-Stress Test Domain:

(Electric Current Input)

Step-stress test where the stepped domain is device or input current.

Current Transfer Ratio (Alpha, Beta):

The ratio of transistor output current to transistor input current.

Crystal Degradation by Radiation:

Permanent damage, such as creation of faults and dislocations, in a semiconductor crystal due to the absorption of radiation. (See "Faults and Dislocations (CIRCUIT/DEVICE THEORY)").

Crystal Growth:

The growing of large area single crystals of semiconductor materials.

- D -

DATA COLLECTION AND REDUCTION:

(DATA HANDLING TECHNIQUES, NUMERICAL INFORMATION PROCESSING, DATA PROCESSING)

Techniques for the recording, compilation and collection of test data, and for processing the data into summarized forms. Also, procedures applicable to monitoring device performance during application.

Data Merging:

Procedures and techniques applicable for combining data generated in independent tests but under approximately equivalent conditions into a single common characteristic value or set of values.

DATA SYSTEM SPECS:

(INFORMATION PROCESSING SPECS)

Specifications and standards covering the implementation of data systems or information processing for microelectronic devices.

DATA VALIDATION (DOCUMENT DESCRIPTOR):

The degree of r liance one can attribute to reported results contained in . RAC document. Complete interpretation of this definition depends on the SPONSORING ORGANIZATION and SOURCE descriptors. (The descriptors in this group are applicable to Test Data REPORT TYPE.)

DCTL (Digital Logic Type (Direct Coupled Transistor Logic)):

A digital logic circuit configuration wherein each input of a gate is connected (coupled) directly to the base of the associated transistor and the output(s) of the gate (or flip flop) are connected directly to the associated transistor. That is, there are no passive components between transistors in successive gates and/or flip flops.

Decomposition:

The separating of atoms in a compound into the constituent elements.

Defective Bond:

(Substandard Bond/Pad, Deteriorated Lead/Die Attachment)

A metallurgical defect due to an inadequate wire or die bond. Defective Bond encompasses open bond/pad, lifted bonds, degradation of attachment contact, plague formation, and improper positioning of the bond upon the terminal pad.

Depletion:

In a field effect transistor, a reverse bias applied to the gate (junction or insulated) repels the majority charge carriers, reducing the number of available carriers in the channel. In any p-n junction, the reverse biasing of the junction causes a depletion of carriers in the junction region.

DEPOSITION:

The methods of placing a layer of material on a substrate.

Deposition Rate Monitoring:

Measurement of the rate at which molecules are deposited on a substrate during a thin film fabrication.

Design Considerations; Function/Circuit Design and Optimization:

General aspects of optimized function and circuit quality under performance constraints, such as supply voltage transients, thermal impedances and electromagnetic and cosmic radiation environments. (See "FUNCTION/CIRCUIT DESIGN & OPTIMIZATION" and "APPLICATION DESIGN TECHNIQUES AND CONSIDERATIONS").

Design of Experiments:

A selection of methods of statistical sampling based upon study of test efficiency and related problems. Such methods must result in sampling which is representative of a population of devices, in order that statistical inferences be valid.

Developing:

Dissolution of the unpolymerized photoresist leaving the diffusion pattern on the wafer.

Developmental:

Device status is beyond the experimental stage. Engineering activity is primarily oriented toward design refinemencs and achievement of fabricability. (See "ITEM STATUS").

Developmental (Test Type):

(Experimental)

Testing/inspection performed in connection with the implementation and refinements of pre-production concepts. (See "Developmental (ITEM STATUS)").

DEVICE ELEMENT MATERIALS:

Materials - elements and compounds - used in fabricating elements of microelectronic devices and circuits.

Device Geometry:

(Physical Structure, Device Configuration)

The physical form and its intra-relationships of the microelectronic device.

Device Manufacturer (Source):

Corporate author identified by a specific device vendor. For example:

"Westinghouse Electric Corp. (Device Mfgr. Source)
Molecular Electronics Div."

Device Manufacturer (Sponsoring Organization):

Device vendor supported document's authorship. (Individual manufacturer is not indexed under this grouping).

Device Mishandling:

(Not-Otherwise Classified Misapplication)

Misapplications, such as physical abuses, which are not defined by "Overstressed Device", or "Erroneous Lead Positioning".

DEVICE PARAMETERS:

The parameters of a microelectronic device element which can be used in calculating the electrical performance of the device. (See "Circuit Component").

(Device User (Equipment Mfr./Systems Contractors Sources)):

Corporate author identified by a specific equipment vendor or systems contractor, as in the example for "Device Mfr. Source".

Device User (Sponsoring Organization):

Equipment Mfr. or Systems Contractor supported document's authorship. (Individual firm is not indexed under this group descriptor).

Dicing (Breaking):

After scribing, the separating of the individual chips.

Die Bonding:

The fusing of the solid state device chip, or die, to the support surface of the protective package.

Die Bond Material:

Substance used to bond or adhere the microcircuit chip to its header or package support plane.

Dielectric, Air (Beam Lead Isolation, Air Isolation):

An isolation method associated with use of extra heavy circuit metallization called "beam leads" at the network terminals. With this beam support, the wafer substrate may be entirely removed, leaving the attached semiconductor islands with air separation. (See "Dielectric Isolation Method").

Dielectric and Insulating Materials:

Inter-element compounds having very high electrical resistivity used in electrically isolating conductors from each other and in forming the dielectric media of capacitors. (See "Dielectric Isolation Method: ISOLATION METHOD").

Dielectric, Ceramic:

Isolation accomplished through separation of the device elements with a ceramic insulating barrier, such as with a ceramic substrate used with hybrid microcircuits. (See "ISOLATION METHOD" and "Dielectric Isolation Method").

Dielectric, Glass:

An isolation effected through interposing layers of glass (amorphous SiO_2) insulating barriers between the semiconductor islands. Techniques associated with this method of isolation are also known by the proprietary designations: Waffle Wafer and EPIC. This descriptor identifies a specific form of "Dielectric, Oxide". (See "Dielectric, Oxide" and "Dielectric Isolation Method").

(Dielectric Isolation Method):

Isolation achieved by interposing an insulating or dielectric barrier between the semiconductor islands. Techniques used to accomplish dielectric isolation are also known as: insulated substrate and multi-phase monolithic systems. (See "ISOLATION METHOD").

Dielectric, Nitride (Silicon Nitride):

A method of dielectric isolation which utilizes a nitride compound (generally silicon nitride). (See "ISOLATION METHOD" and "Dielectric Isolation Method").

Dielectric, NOC (Not-Otherwise Classified Dielectric Isolation Method):

A dielectric method of isolation which cannot be classified by any descriptors in the current glossary. (See "ISOLATION METHOD" and "Dielectric Isolation Method").

Dielectric, Oxide (Silicon Dioxide; Dielectric, Dioxide; Dielectric, Monoxide):

An isolation effected through interposing an (di-) oxide insulating barrier between the semiconductor islands. "Dielectric, Glass", other dioxides, oxides and monoxides are included within the scope of this descriptor. (See "Dielectric, Glass", and "Dielectric Isolation Method").

Die Size:

The range of size values of the semiconductor dice used for the microelectronic device. Size values are given in terms of linear dimension for each side, in the interest of universality of designations. Corresponding area dimensions applicable to square dice are shown in parentheses in the listing of value ranges. This listing is as follows:

<30 mils/side (<900 sq. mils)

31-42 mils/side (900-1800 sq. mils)

43-60 mils/side (1800-3600 sq. mils)

61-85 mils/side (3600-7200 sq. mils)

86-120 mils/side (7200-14,400 sq. mils)

121-170 mils/side (14,400-28,800 sq. mils)

171-240 mils/side (28,800-57,680 sq. mils)

>240 mils/side (>57,680 sq. mils)

Differential Amplifier:

A linear electronic circuit consisting of two cathode, or emitter, coupled amplifier devices such that the output is proportional to the difference between the input signals on each device. Such an amplifier is capable of amplifying dc signals with minimum drift.

Differential Amplifier (Difference Amp, Sense Amp):

A linear device type consisting of two matched cathode or emitter coupled amplifier circuit partitions such that the output is proportional to the difference between the input signal on each partition. Such an amplifier is capable of amplifying signals from d-c to r-f with minimum drift.

Differential (Linear Device Type (Symmetrically Balanced Network, Push-Pull Circuit, Balanced Input/Output Network)):

A linear operational type in which each stage has circuit components with intraconnection and matching such as to provide symmetry about an electrical neutral or ground point. Output response depends upon the difference between two opposing input signals. Differential or push-pull amplifiers are included within the scope of this descriptor. (See "Differential Amplifier").

Diffused Junction:

A pn semiconductor junction formed by the diffusion of impurities of a certain polarity into a semiconductor region of opposite polarity.

Diffusion:

The introduction of doping impurities into a semiconductor to form a region of opposite polarity to that of the remainder of the host material, thus creating a p-n junction.

Diffusion Coefficient:

A measure of the rate of diffusion of carriers through a material. Also applied to the diffusion of impurities in a material.

Diffusion Defects:

(Diffusion Irregularity/Flaw, Inadequate Doping Profile)

Semiconductor bulk defects due to diffusant imperfections. Diffusion spikes and incomplete diffusion are terms included in the scope of this descriptor.

Diffusion Length:

A measure of the distance a carrier may move through a material, in the absence of an electric field, during its lifetime.

Digital (Functional Category) (Switching Logic Circuit, Discrete Response Circuit, Quantum Level Output Circuit):

A circuit function where the output varies discretely or discontinuously with input stimulus. Also, the category of circuits designed to perform an auxiliary function to a switching logic circuit, such as gate expanders.

Digital Logic, NOC (Not-Otherwise Classified Digital Operational Type):

A digital network type which cannot be classified by any descriptors of the current glossary. (See "Digital Logic Type").

(<u>Digital Logic Type</u> (Logic Circuit Type, Logic Family, Digital Operational Type, Digital Network Type, Switching Logic Type)):

The operational type of digital circuit, as characterized by its key circuit components and intraconnection pattern. In general, the basic circuit partition which typifies the digital operational type, and which serves as the functional building block of complex networks, may be regarded as the elemental logic gate. Such logic gate implements one of the elemental functions of AND, NAND, OR or NOR. Accordingly, acronyms which are included under this descriptor heading (RTL, RCTL, DCTL, etc.) are defined with reference to the elemental logic NOR gate. (See circuit diagrams in <u>Electronic Design</u>, May 17, 1966, p. 171). (See "OPERATIONAL TYPE" and "Digital (Functional Category")).

<u>Digital to Analog Converter (D/A Converter)</u>:

A circuit which converts digital signals to a linear signal proportional to the characteristics of the digital signal.

<u>Disappearance of Metallization</u>:

(Vanishing Metallization)

The loss of metal from the conducting films as a result of diffusio. migration, or evaporation.

<u>Discrete Microcomponent</u>:

Any solid state device, active or passive, which, because of its small size and geometry, is suitable for incorporation into a multi-chip or hybrid microelectronic circuit.

<u>Dissection and Sectioning</u>:

(Device Autopsy)

Inspection procedures involving appropriate disassembly of devices and the preparation of specimen device elements to facilitate examination, such as through slides and stained cross sections.

(<u>DOCUMENT DESCRIPTORS</u>):

Appropriate set of terms for identifying and classifying the RAC held document.

DOCUMENT FORMAT (DOCUMENT DESCRIPTOR):

Form in which the RAC document is accessible.

Dopant Materials:

Materials added to a semiconductor to alter its resistivity and the type of majority current carrier present.

Drain:

In a field effect transistor, the electrode through which carriers are removed from the conducting channel.

Drawings (Report Type):

"Specifications, Report Type" which is designated as "Drawing" by the document's SOURCE or SPONSORING ORGANIZATION.

DTL (Digital Logic Type (Diode Transistor Logic)):

A digital logic circuit configuration wherein the gates are characterized by a diode in series with each input and with opposite terminals of the input diodes being connected to the base of the associated transistor. Although all diodes must be connected the same, either the anodes or the cathodes can be connected to the transistor base in order to obtain the desired logic function. The generic DTL type includes the modified DTL types such as "UTILOGIC (UTL)" MDTL, VTL, MVTL, LPDTL, HNIL-DTL, DT L, and MOD-DTL. (See "Digital Logic Type").

Dual In-Line, Hermetically Sealed:

A Dual In-Line package with hermetic seals. (See "Dual In-Line, Plastic").

Dual In-Line, Plastic (DIP):

A flat-pack type of plastic package but with the terminal leads bent or projecting at right angle to the package flat, with alignment of the two rows of leads to facilitate insertion contact within a mate socket. (See "PACKAGE CONFIGURATION").

- E -

ECONOMICS:

Considerations of technological alternatives with respect to relative expenditures.

Electrical Characterization:

(Electrical Probing, Electrical Measurement)

Evaluation of device or device element through determination of electrical properties or variation of electrical parameters.

Electrical Conduction:

The transport of electrical energy through the motion of electric charges.

Electrical Noise Generation:

The random fluctuations of electrons in electrical components generated by thermal energy.

ELECTRICAL PROPERTIES:

(DEVICE ELECTRICAL PARAMETER VALUES, RATINGS/CHARACTERISTICS LEVELS)

Value levels of device electrical parameters, in terms of characteristics and maximum ratings.

Electrodes:

(Plates)

The metallic electrodes of a film capacitor.

Electrolytic Corrosion:

Chemical changes in composition and compound formation as a result of electrolysis at the interface between two dissimilar materials.

Electromagnetic and Particle Radiation:

(See "Radiation Environments (TEST TECHNIQUES & PROCEDURES)").

Electron Microprobe:

(Electron Beam Micro-Scanning)

An inspection system utilizing the magnified imaging of electrostatic potential gradients, resulting from exposure of the energized device elements to electron beam scanning.

Electron Microscopic Examination:

Inspection through use of an electron microscope. This technique does not include Electron Microprobe.

Electron Spin:

The electron, in addition to its orbital angular momentum, has associated with it an angular momentum which is attributed to a spinning about an axis which gives rise to a magnetic moment.

Emitter:

The low impedance region of a bipolar transistor from which current is injected into the base region.

ENCAPSULATION/PACKAGE SEALING:

The surrounding of a solid state device with a protective casing.

Energy Gap:

The unallowed energy states in a semiconductor in the region between the lowest of the conduction band of energies and the highest of the valence band of energies.

Energy Level:

A discrete state of energy in which an atom is capable of existing.

Enhancement:

In a p-channel MOS field effect transistor, a negative potential on the gate will attract positive charge (holes) to the surface increasing the number of available majority carriers.

Environmental:

Design approach which is primarily within the context of thermal and other environmental constraints. This descriptor covers considerations of thermal impedance, such as for high-power dissipating circuits; and designed immunities to electromagnetic or cosmic radiation environments. (See "Design Considerations; Function/Circuit Design & Optimization").

ENVIRONMENTAL CAPABILITIES:

Value levels of the ability of the device to satisfactorily respond to environmental requirements.

ENVIRONMENTAL CONDITION:

(AMBIENT STRESS DOMAIN)

The specific nature of ambient stress(es) to which the device or assembly of devices is exposed.

Epitaxy:

The deposition of a layer of semiconductor onto the surface of a single crystal wafer such that the epitaxial layer grows as a single crystal. Junctions are formed at the layer-substrate interface when the semiconductor being deposited is doped to different polarity than the substrate material.

Epitaxial Junction:

A pn junction formed at the interface between a substrate of a certain polarity and an epitaxial layer of opposite polarity.

Epitaxial Layer:

In a solid state device or integrated circuit, a thin layer of semiconductor, usually of opposite polarity to that of the substrate, deposited so as to grow as a single crystal with same orientation as that of substrate. Generally used to obtain sharply defined pn junction to provide isolation between devices, and uniformly doped collector region, affording better control over collector-base capacitance and breakdown voltage.

Epitaxy Defects:

(Epitaxial Flaw)

A surface defect due to an irregularity in the growth of an epitaxial layer onto a substrate material.

Equipment Application:

State-of-the-art capabilities for facilitating equipment design, or, the effects of technological advances in stimulating use of microelectronic designs. This descriptor also includes consideration of novel applications, maue feasible with microelectronic devices.

EQUIPMENT SYSTEM LEVEL SPECS:

(PROCESS EQUIPMENT/APPLICATION USAGE SPECS)

Specifications and standards governing equipment and systems, for fabrication processes and for applications.

Erroneous Lead Positioning:

(Incorrect External Interconnection)

Improperly interconnecting the device to external terminals through incorrectly associating the device lead positions with such terminals.

Etching:

The selective removal of atoms from the surface of a substance.

Eutectic Braze:

The use of a metal which forms a eutectic alloy with the semiconductor material of the chip, especially to form an ohmic contact between header and chip.

Excessive Lead Length:

(Inordinate Wire Length)

Wire or lead section which is made overly long, such as to result in excessive pigtail length at a terminal pad, or, excessive span length connecting two terminal pads.

Experimental:

Device status is beyond the conceptual and preliminary design stages. Effort with device is directed toward investigating promising alternative designs and to finalize the fundamental design and capabilities. (See "ITEM STATUS").

Exponential Distribution:

A one-parameter probability-density function of the form:

$$f(t) = \frac{1}{m} \exp\left(\frac{-t}{m}\right)$$

where "m" is the mean-time-to-failure (MTTF). The exponential distribution is characterized by exhibiting a constant value of the parameter m.

Exposure:

The illumination of a photoresist film for the required time to polymerize the material.

- F -

FABRICATION TECHNIQUES AND EQUIPMENT:

Information on activities concerned with process description, control, fabrication optimization and facilities.

FACILITIES:

(RELIABILITY INSPECTION LABORATORIES/SETUPS)

Provisions in terms of laboratory, test equipment, instrumentation, and failure or performance monitoring measures for reliability inspection.

Facility Approved by Source-Sponsor Representative (Data Validation):

Test results generated with facilities which have undergone inspection by a representative of the SPONSORING ORGANIZATION, as indicated via "Certified by Responsible Report-Source Official" and a countersignature of statement by agent of the SPONSORING ORGANIZATION.

Factory Checkout:

(See "Failure Environment, Assembly/Installation").

FAILURE ANALYSIS FACILITIES:

(FAILURE ANALYSIS LABORATORY SETUPS, DEFECTS ANALYSIS FACILITIES)

Provisions in terms of instrumentation and laboratory facilities for conducting failure analyses of microelectronic devices.

Failure Analysis Results:

(Failure Diagnoses, Failure Mode Summary)

Data obtained from failure analysis studies. (See "FAILURE ANALYSIS STUDIES").

FAILURE ANALYSIS STUDIES:

(PHYSICS OF FAILURE STUDIES, MAJOR TERMATREX CATEGORY V)

Information relating to the procedures and results of analytical investigations of failures.

FAILURE ANALYSIS TECHNIQUES:

(PHYSICS OF FAILURE PROCEDURES)

Methods and procedures to ascertain and substantiate physical defects, failure phenomena, failure stress domains, and causes of failure.

FAILURE ENVIRONMENT:

(PRIMARY ENVIRONMENT OF FAILURE)

General conditions that indicate where and when failure occurred. The generic environment of failure. (See "APPLICATION ENVIRONMENT", "TEST TYPE", "ENVIRONMENTAL CONDITION" and "APPLICATION STATUS").

Failure Environment, Application Tests, In-Plant:

(Simulated Application Tests, In-Plant)

Testing conducted on an assembly or equipment to simulate the conditions of application, within the manufacturer's plant, upon its completion.

Failure Environment, Application Tests, On-Site:

(Simulated Application Tests, On-Site)

Testing conducted to simulate the conditions of application, at the site of application, upon manufacturer's delivery of equipment.

Failure Environment, Assembly/Installation:

(Equipment Checkout Tests)

Pertains to the actual conditions of assembly of micro-electronic devices, or, their installation into equipment or system configuration. Generally, failures are exposed during inspection performed in conjunction with these activities.

Failure Environment, Field Use:

(Field Monitoring)

Observation and inspection of assembled devices under their normal conditions of application.

Failure Environment, Laboratory Environmental Test:

(Environment Testing)

Testing conducted under controlled or laboratory environmental conditions, such as, mechanical, thermal and aqueous exposure environments.

Failure Environment, Laboratory Life Test:

(Operation Life Test, Storage Life Test, Steady State Testing, High Temperature Life Test)

Life testing conducted under controlled or laboratory conditions.

Failure Environment, Post-Production Screen/Burn-In:

(Product Quality Conditioning)

A test or combination of tests designed to identify specimens with quality defects (those likely to exhibit early failures), and tests designed to stabilize the products' characteristics.

Failure Environment, Product Inspection:

(Product Quality Monitoring, Product Line Audit)

General testing conducted during production or procurement phases to insure a product free from quality defects.

FAILURE MODES:

(Failure Manifestations)

The observations or test results, on a pre-analysis of failure level, which identify a defective device. The manifestations of any failed device in terms of generalized reject or failure criteria.

Failure Modes:

(Failure Manifestations)

(See "FAILURE MODES: FAILURE ANALYSIS STUDIES").

FAILURE PHENOMENA:

(FUNDAMENTAL FAILURE MECHANISMS, PHYSICS OF FAILURE)

The underlying facts, events, or processes which give rise to physical defects or failure mechanisms.

Failure Rate Statistics:

(Reliability Attributes Summary)

Summary attributes of the test or inspection data from which the failure rate is obtained. Such attributes include sample size, the number of failures, the associated times to failure, and applicable conditions.

FAILURE STRESS DOMAIN:

(SECONDARY ENVIRONMENT OF FAILURE)

The specific nature of externally applied stresses which may contribute to failure.

Failure Stress Domain, Acceleration, Constant:

Failure activating stress of immersion in a liquid.

Failure Stress Domain, Mechanical Shock:

(Simulated Drop)

Suddenly applied forces or abrupt changes in motion are the failure activating stresses.

Failure Stress Domain, Moisture or Humidity:

Deteriorative effects of high humidity is the failure activating stress.

Failure Stress Domain, Noise, Acoustical:

(Sonic Vibration)

Exposure of device to random sonic energy is the failure activating stress.

Failure Stress Domain, Pressure, Gas:

(High Pressure)

Exposure of device to a high pressure environment or to an explosion shock wave is the failure activating stress.

Failure Stress Domain, Radiation, Electromagnetic:

(Electromagnetic Interference, Electrical Noise)

Failure activating stress is exposure of device to an electromagnetic environment within the sub-optical frequency range.

Failure Stress Domain, Radiation Exposure, Particle:

(Cosmic Radiation)

Failure activating stress is exposure of device to particulate radiation, or, to irradiation within the region of the electromagnetic spectrum of optical and shorter wavelengths.

Failure Stress Domain, Salt Atmosphere/Spray:

(Corrosion, Marine Fog)

Failure activating stress is exposure of device to a fine mist of salt solution or to a sea-coast atmosphere.

Failure Stress Domain, Sand and Dust:

Exposure of device to a sand and dust-laden atmospheric environment is the failure activating stress.

Failure Stress Domain, Temperature <-42.5°C:

Failure activating stress temperature less than -42.5 degrees, Centigrade.

Failure Stress Domain, Temperature ≥ 102.5°C:

Failure activating stress temperature greater than or equal to 102.5 degrees Centigrade.

Failure Stress Domain, Thermal Shock:

(Temperature Cycling, Seal Strain)

A test or application in which failure is activated by a sudden exposure to extreme changes in temperature.

Failure Stress Domain, Vacuum:

(Reduced Barometric Pressure, Altitude Operation, Low Pressure)

Failure activating stress of environmental pressure reduced to the region of a vacuum.

Failure Stress Domain, Vibration:

Contributory cause of failure is mechanical vibration stress. This failure stress domain includes vibration fatigue; vibration, variable frequency; vibration, high frequency; and random vibration environments.

Fatique:

The local strain exceeding the elastic limit of a metal, such that it loses its strength, as a result of stressing the metal repeatedly.

Fermi Level:

A mean value of energy electrons would have if, instead of existing in discrete and preferred states, they were continuously distributed in energy according to Fermi-Dirac statistics.

Ferrite:

A non-metallic compound having two sub-lattices Fe_2O_3 and XO where X may be any of the elements Mn, Mg, Co, Ni, Zn, Cu, or Ba and having the property of ferrimagnetism, i.e., adjacent molecular groups have oppositely oriented magnetic moments but of different magnitude, resulting in a residual magnetization.

Ferroelectricity:

The natural occurrance of oriented electric dipoles in a dielectric material giving rise to large dielectric constant and whose direction of orientation can be reversed by the application of an electric field.

Ferroelectrics:

Oxide compounds which exhibit very high dielectric constant due to polarization of dipole moments.

Field Effect:

The modulation of electrical conductivity of a media by the application of a transverse electric field.

Field Effect Transistor (FET):

A three terminal semiconductor device in which an electric field created by the potential on a gate electrode controls the conductivity of a channel in the semiconductor between source and drain electrodes.

Field Operations:

(Field Use, Field Monitoring)

Observation and inspection of devices, as assembled in equipment, under the normal conditions of application.

Field Testing:

(Simulated Application Field Testing)

See "Failure Environment, Application Tests, On-Site".

Film IC (Passive Substrate IC):

An integrated circuit whose elements (circuit components) are formed from films of conductive, resistive, dielectric, and/or semiconductor materials deposited upon a substrate which is generally passive (non-conductive). Currently, commercially available film IC's are limited to passive components incorporated into hybrid IC's, although much research and development work is presently being done in the area of active film components such as thin film IGFET's.

Film Thickness Defect:

(Inadequate Film Cross-Section)

A mechanical imperfection due to improper profile distribution of film. Metallization and insulative films are included in the scope of this descriptor. Film Thickness Defect includes: thin metal at oxide step, and inadequate oxide protection.

Final Inspection:

(Terminal Product Inspection)

Detail test procedures for verification of adequate fabrication, subsequent to product assembly.

Flat Pack:

A package with a flat near-rectangular or near-square configuration. Terminal leads project from two sides and the encapsulation sealed as in the JEDEC TO-84 flat package. Other TO numbers, which are included in this classification, are listed as follows:

TO-84	TO-87	TO-90
TO-85	TO-88	TO-91
TO-86	TO-89	TO-95

Flat Pack, Ceramic:

A flat package with ceramic encapsulation material. (See "Flat Pack").

Flat Pack, Glass:

A flat package with glass encapsulation material. (See "Flat Pack").

Flush (Metallized):

Interconnection of microelectronic devices in which the devices are embedded in the substrate such that the device surface is flush with the substrate surface. The interconnection pattern is then deposited onto this surface. (See "Inverted" and "INTERNAL CONNECTION MODE").

Flying Leads:

Small diameter wires used as internal connections and being self supported in traversing the space between device and terminal posts. (See "INTERNAL CONNECTION MODE:).

Foreign Material:

(Extraneous Particles, Loose Foreign Material)

A mechanical imperfection due to the incorporation of a foreign substance, in identifiable form, within the device. An extraneous material which may have a deleterious effect upon device performance.

FUNCTIONAL CATEGORY:

The generic classification of circuit function in terms of whether the microelectronic device is designed for digital or linear (analog) functions.

FUNCTION/CIRCUIT DESIGN & OPTIMIZATION:

Approaches to optimize the function and circuit quality with considerations of performance conditions. (See "Design Considerations").

Functional Degradation:

(Performance Loss)

Manifestation of the loss of functional capability of a device through failure to meet performance criteria in a test assembly or within equipment. Failure exhibited in terms of a "NO GO" observation.

Functional Elements:

Elements which take an active role in the function or operation of a microelectronic circuit.

Functional Synthesis:

(Functional Design, Molecular Electronic Design)

Synthesis of circuit functions or device functions, primarily from an approach which considers the network topology (intraconnection pattern) and interactions of basic device elements. These elemental building blocks for functional synthesis need not be fully defined.

- G -

Gain:

The typical increase in signal power voltage or current, usually expressed as a ratio of output to input in decibels (db).

Less than 40 DB

40 thru 80 DB

Greater than 80 DB

Gate Expander(s):

A logic circuit consisting of a multiple of elements identical to the input elements of a logic gate. Used to increase the fan-in of a logic gate circuit.

Gate (Logic Gate):

A switching logic circuit with more than one input but only one output. A discrete output response is contingent upon the presence (or absence) of one or all of several inputs, each with a given discrete value. Thus, a logic gate may implement one of the elementary digital functions: AND, OR, NAND or NOR.

Gate Turn Off Switch (GTO):

A PNPN semiconductor device in which contact is made to three of the four regions and which conduction can be both initiated and terminated by appropriately setting the gate potential.

General Catalog (Vendor Report Type):

A document containing technical data sheets for several vendors, a summary catalog of a vendor, or, technical data sheets and application notes of one vendor.

GENERAL METHODOLOGY:

Techniques (NOC) reported on the as. ssment and implementation of reliability which cannot be classified as: "PREDICTION AND MODELING", "TEST TECHNIQUES AND PROCEDURES", "STATISTICAL TOOLS", "DATA COLLECTION AND REDUCTION", or "FACILITIES". (See definitions of these terms, and "RELIABILITY TECHNOLOGY").

GENERIC CLASS DESCRIPTORS:

The major identifiers of microelectronic devices with regard to their physics-of-failure characteristics. Generic Class Descriptors consist of eight term groupings which identify or describe the properties of microelectronic devices. These are: Microelectronic Category, Functional Category, Package Configuration Operational Type, Qualification Class, Interconnection System, Isolation Method and Circuit Complexity.

Germanium:

(Ge)

An elemental semiconductor of Atomic Number 32.

Glass:

A non-crystalline (amorphous) brittle compound usually containing, as a base, silicon dioxide.

Glass Frit:

A powdered form of low melting glass.

Glass-Glass Seal:

The joining of two glass pieces to form an impervious seal, usually by using a low melting glass frit or solder glass as the bonding agent. (See "Glass-to-Glass Seal: ENCAPSULATION/PACKAGE SEALING").

Glass-Metal Seal:

The bonding of glass to metal to form an impervious seal, usually by oxidizing the metal and then fusing the glass to the oxide (See "Glass-to-Metal Seal: ENCAPSULATION/PACKAGE SEALING").

Glass to Glass Seal:

The joining of glass to glass in a device package so as to form a hermetic seal.

Glass to Metal Seal:

The joining of glass to metal in a device package so as to form a hermetic seal.

Gold:

A metallic element of Group I of the Periodic Table used in silicon devices to reduce carrier lifetimes.

Gold:

(Au)

A nobel metal element of Atomic Number 79.

Gold-to-Aluminum, Direct (Au/Al, Direct; Gold-to-Aluminum, Inverted Chip; Gold-to-Aluminum, Flip Chip):

Inverted chip bonding with gold metallization material bonded to an aluminum circuit metallization material. A wetting agent or intermediary material may be utilized. (See "INTERCONNECTION SYSTEM").

Gold-to-Aluminum, Wire Bond (Au/Al, Wire Bond):

A gold wire bonded to aluminum circuit metallization material. (See "INTERCONNECTION SYSTEM").

Gold-to-Gold, Direct (Au/Au, Direct; Gold-to-Gold, Inverted Chip; Gold-to-Gold, Flip Chip)):

Inverted chip bonding with gold metallization material bonded to a gold circuit metallization material. A wetting agent or intermediary material may be employed. (See "INTERCONNECTION SYSTEM").

Gold-to-Gold, Wire Bond (Au/Au, Wire Bond)):

A gold wire bonded to gold circuit metallization material. (See "INTERCONNECTION SYSTEM").

Gold-to-Silicon-to-Aluminum, Wire Bond (Au/Si/Al, Wire Bond):

A gold wire bonded to a heavily doped silicon terminal region, with an aluminum circuit metallization tab deposited over another portion of this terminal area. (See "INTERCONNECTION SYSTEM").

Gold Silicon Eutectic:

An alloy of gold and silicon of such composition that its melting point is a minimum in the phase diagram for the alloy system.

Government Agency QA Specs:

(Federal Agency Quality Conformance Specs/Standards)

Quality assurance (QA) specifications promulgated by a government agency. (See "QUALITY ASSURANCE SPECS").

Ground Checkout Aircraft Environment:

"Aircraft Environment" associated with the out-of-flight facilities or base provisions for system maintenance and inspection.

Ground Checkout Missile Environment:

"Missile Environment" associated with pre-launch and out-of-flight facilities for missile system maintenance and inspection.

Ground Checkout Spacecraft Environment:

"Spacecraft Environment" associated with pre-launch and non-orbital provisions for satellite maintenance and inspection.

Ground Environment:

Application environment associated with an equipment system designed for normal service on land.

Ground Fixed:

A "Ground Environment" in which the equipment system is bound to stationary operational service facilities.

Ground Laboratory:

A "Ground Environment" associated with facilities for controlled conditions of testing or operation.

Ground Mobile:

A "Ground Environment" in which the system equipment is self propelled or is capable of operation in a transportation mode. A system operating as a land vehicle.

Ground Portable:

A "Ground Environment" in which the system equipment is designed to facilitate its being carried to various operational sites as well as being operational while being so transported.

- H -

Hafnium Dioxide:

A dielectric compound of Hafnium from Group IV of the Periodic Table and Oxygen from Group VI.

Hall Effect:

The development of a voltage across a material which is carrying an electrical current when placed in a magnetic field normal to the direction of the current. The voltage is measured normal to both current and magnetic field and its polarity indicates the type of carrier comprising the current.

Hard Copy Document (Document Format):

RAC Library document is in the form of a bound or filed printed copy.

Heat Capacity:

A measure of the amount of heat energy required to raise the temperature of a unit mass of a material.

High Reliability Certification (Hi-Rel Certification):

Microelectronic device is qualified for service where maintenance and replacement is not reasonable, and reliability is imperative. Production line certification is required. In addition, screen/burn-in and complete Quality Assurance (QA) tests are conducted on 100% of the product. Inspection procedures must meet requirements of a specification, such as the NASA high-rel specs. (See "QUALIFICATION CLASS").

High Temperature, Accelerated Life Test Domain:

(Elevated Temperature, Elevated Ambients)

Accelerated life test where principle domain is elevated temperature (constant). (See "Thermal Environments").

High Temperature, Step-Stress Test Domain:

(Elevated Temperature, Elevated Ambients)

Step stress test in which the stepped domain is temperature. (See "Thermal Environments").

Holographic Examination:

(Laser 3-D Imaging, Hologram Inspection)

Evaluation of a device or device element through preparation and viewing with holograms.

Humidity:

(Moisture, Relative Humidity)

Exposure to an atmospheric stress of ambient moisture. (See "Failure Stress Domain, Moisture or Humidity" and "Atmospheric Stress Testing").

Hybrid Microcircuit (Hybrid Integrated Circuit; Hybrid IC; HIC; Multichip Microcircuit, Hybrid):

A microelectronic device whose circuit elements are fabricated upon two or more substrates and interconnected to form the device substrate assembly, to result in a combination of integrated circuits within two or more MICROELECTRONIC CATEGORIES, or, of a combination of one or more such IC's and discrete microcomponents. (See "MICROELECTRONIC CATEGORY", "Discrete Microcomponent" and "Multichip Microcircuit").

Improper Package Marking:

(Device Mismarking)

Incorrect labeling or misaligned marking on the package of the microelectronic device.

Improper Wire Bonding:

(Substandard Lead Attachment, Poor Wire Bonding)

The preparation of wire bonds with poor adhesion or with improper contact placement.

Impurity Diffusion:

The random passage of impurities into a host material under the influence of a concentration gradient.

Indium:

A metallic element of Atomic Number 49.

Inductance:

The measure of the amount of magnetic flux created in a conducting loop by a current flowing in that loop.

Industrial/Commercial:

Devices are qualified for demanding industrial/commercial service, such as in manufacturing and computer operation. However, requirements are less stringent than those for the "Military" Qualification Class, especially in regard to operating temperature range and environmental stress endurance.

Industry Associations (ASTM, IEEE, Source):

Document sources such as ASTM, IEEE, and EIA. (No specific descriptors are detailed under this group).

Industry Associations (Sponsoring Organization, such as ASTM, and IEEE):

Trade organization supported document's authorship.

Inherent Material Flaws (Bulk Defects, Intrinsic Material Faults, Raw Material Imperfections):

Imperfections in the device element materials to a degree which gives rise to secondary physical defects, and bulk defects other than diffusion defects. An example is the presence of crystalline dislocations in a critical region of a semiconductor which cause the production of diffusion spikes. (See "Diffusion Defects").

In-Process Inspection Procedures:

(Device In-Process Testing/Probing)

Delineation of detail test or wafer probing procedures for in-process control. (See "Failure Environment, Product Inspection").

Inspection:

Provisions and procedures for reliability inspection.

Inspection Specification Deviation:

(Measurement Parameter Deviation)

Deviation of measured parameter to a value outside of specified limits, either of values of the initial distribution or of changes in parameter values.

Instrumentation and Display:

A class of equipment which performs measurement, indication or monitoring, and exhibition functions. Descriptor is exclusive of "Navigation".

Insulated Gate Field Effect Transistor (IGFET):

A field effect transistor in which the gate electrode is separated from the conductive channel by a layer of insulation. The electric field modulates the density of carriers in the channel.

Integrated Circuit (IC, Integral Circuitry, Pure Integrated Circuit)):

A set of intraconnected circuit elements which are inseparably formed upon and associated with a single substrate.

INTERCONNECTION SYSTEM:

Identification of the means used to electrically connect the microelectronic device chip(s) to the package leads. The wire or direct metallization material and the circuit metallization material of the bond are respectively designated. Also, this internal connection mode is classified as to whether wire bonding or direct lead/die attachment is used. Direct lead/die attachment is also known as inverted chip, flip chip, leadless-inverted device (LID), and face down bonding. (See "INTERNAL CONNECTION MODE").

INTERMITTENT LIFE TEST:

(CYCLED STRESS OPERATION LIFE TEST)

"Operating Test(s)" in which a stress domain, generally electrical, is applied with specified on-off cycling of the severity level. (See "Operating Tests (TEST TECHNIQUES AND PROCEDURES)").

INTERMITTENT LIFE TEST LOAD POWER:

Electrical stress condition of relative load power severity level at which the "INTERMITTENT LIFE TEST" is conducted.

Intermittent Life Test Load Power (<95% Rating)

Relative severity level is less than 95 percent of rated load power.

Intermittent Life Test Load Power (95% to <105% Rating)

Relative severity level is in the range from 95 percent to less than 105 percent of rated load power.

Intermittent Life Test Load Power (105% to <155% Rating)

Relative severity level is in the range from 105 percent to less than 155 percent of rated load power.

Intermittent Life Test Load Power (≥155% Rating)

Relative severity level is in the range greater than or equal to 155 percent of rated supply voltage.

INTERMITTENT LIFE TEST SUPPLY VOLTAGE:

Electrical stress condition of relative supply voltage severity level at which the "INTERMITTENT LIFE TEST" is conducted.

Intermittent Life Test Supply Voltage (<95% Rating)

Relative severity level is less than 95 percent of rated supply voltage.

Intermittent Life Test Supply Voltage (95% to <105% Rating)

Relative severity level is in the range from 95 percent to less than 105 percent of rated supply voltage.

Intermittent Life Test Supply Voltage (105% to <155% Rating)

Relative severity level is in the range from 105 percent to less than 155 percent of rated supply voltage.

Intermittent Life Test Supply Voltage (≥155% Rating)

Relative severity level is in the range greater than or equal to 155 percent of rated supply voltage.

INTERMITTENT LIFE TEST TEMPERATURE:

(AMBIENT TEMPERATURE CONDITION, INTERMITTENT LIFE)

The environmental condition of ambient thermal severity level at which the "INTERMITTENT LIFE TEST" is conducted.

Intermittent Life Test Temperature <-82.5°C:

Temperature severity level less than -82.5 degrees Centigrade.

Intermittent Life Test Temperature -82.5°C to <-42.5°C:

Temperature severity level is in the range from -82.5 degrees to less than -42.5 degrees Centigrade.

Intermittent Life Test Temperature -42.5°C to <21°C:

Thermal severity level is in the range from -42.5 degrees to less than 21 degrees Centigrade.

Intermittent Life Test Temperature 21°C to 31°C:

Thermal severity level is in the range from 21 degrees to less than 31 degrees Centigrade.

Intermittent Life Test Temperature 31°C to <102.5°C:

Thermal severity level is in the range from 31 degrees to less than 102.5 degrees Centigrade.

Intermittent Life Test Temperature 102.5°C to <152.5°C:

Thermal severity level is in the range from 102.5 degrees to less than 152.5 degrees Centigrade.

Intermittent Life Test Temperature 152.5°C to <202.5°C:

Thermal severity level is in the range from 152.5°C degrees to less than 202.5 degrees Centigrade.

Intermittent Life Test Temperature 202.5°C to <302.5°C:

Thermal severity level is in the range from 202.5 degrees to less than 302.5 degrees Centigrade.

Intermittent Life Test Temperature ≥302.5°C:

Thermal severity level is in the range greater than or equal to 302.5 degrees Centigrade.

INTERMITTENT STRESS DOMAIN:

The specific nature of the externally applied test stress of the "INTERMITTENT LIFE TEST".

INTERNAL CONNECTION MODE:

The method of interconnecting the terminal points on the microelectronic devices and the internal terminal posts or tabs of the package leads. (See "INTERCONNECTION SYSTEM").

Inversion:

In a MOS field effect transistor (p-channel) when the bias is made positive, the concentration of holes near the surface is depleted. At a certain large value of bias, as the conduction

Inversion (cont'):

band energy in the semiconductor is bent toward the Fermi level, the concentration of minority carriers (electrons) will suddenly increase forming an n-type channel in a narrow region near the surface.

Inversion and Channeling:

The presence of fixed charges in the oxide layer on a semiconductor device may cause attraction or repulsion of majority carriers. In a p-n-p transistor this results in repulsion of holes from the surface of the collector region, inversion of polarity at the surface and creation of an n-type channel. (See "Inversion and Channeling (CIRCUIT/DEVICE THEORY)").

Inverted:

(Face-down, LID, Flip-chip, Direct)

Interconnection of microelectronic devices by a thin film (or printed circuit) network of conductors onto which the devices have been placed face-down such that the device terminals are in contact with terminal pads on the conductor network. (See "INTERNAL CONNECTION MODE" and "INTERCONNECTION SYSTEM").

Ion Migration:

(See "Ion Migration (FAILURE PHENOMENA)").

Ion Migration:

The motion of ions present in a material under the influence of electric fields present in a device resulting in accumulation of these ions in a region containing one of the poles of the field and subsequent contamination of that region. (See "Ion Migration (CIRCUIT/DEVICE THEORY)").

Iron:

A metallic element of Atomic Number 26.

IR Thermal Mapping:

(Infrared Scanning, Isothermal Plotting, Thermal Profile or Contouring)

Use of responses to infrared energy for evaluation, with a system for plotting the isothermal radiation patterns.

ISOLATION METHOD:

Designation of the mode of electrically isolating device elements which are formed (through diffusion or epitaxy) in the same semiconductor chip, or which are mounted upon the same substrate.

Isolation Region:

In integrated circuits the area of a substrate doped to opposite polarity to that of the substrate in which are fabricated some of the components of the circuit. The area, by way of the resultant pn junction which is always reverse-biased, served to electrically isolate these components from others in the circuit.

<u>Journal Article (Report Type)</u>:

A pre-print, reprint, or excerpted paper(s) from a trade journal.

<u>Junction Field Effect Transistor (JFET)</u>:

A field effect transistor in which the gate electrode is separated from the conductive channel by a reverse-biased PN junction. Conductivity control is obtained by varying the width of the depletion region adjacent to the gate-channel junction.

<u>JUNCTION FORMATION</u>:

The creation of p-n junctions in the semiconductor material during device fabrication.

<u>Junction</u> (PN Junction Isolation):

An isolation method which utilizes reverse bias across a specially formed PN junction. Other terms covered by this descriptor are: diffused collector isolation, all-diffused isolation, and diffused isolation in epitaxial layer. (See "ISOLATION METHOD" and "Isolation Region, MEL DEVICE ELEMENT DESCRIPTOR").

- K -

Kovar:

An alloy of iron, nickel and cobalt, having low thermal expansion coefficient.

- L -

Large Scale Integration (LSI):

The inclusion and interconnection of a large number, usually more than 50, of elemental functional units on a single semiconductor chip.

Launch and Flight Missile Environment:

"Missile Environment" in which the system equipment is being thrusted into fractional orbit or is in the actual operational condition.

Layout; Computer Aids:

(Computer-Aided Circuit Topography)

Computer-aided approach to circuit layout. (See "Circuit Layout"). Design of the associated photomasks is not encompassed by this descriptor. (See "Mask Design; Computer Aids").

Lead:

A metallic element of Atomic Number 82.

LEAD ATTACHMENT MODES:

(EXTERNAL LEAD ATTACHMENT)

Lead provisions for mechanical/electrical interface of device package to the external fixtures, such as printed circuit boards or other wiring assemblies. (See "LEAD ATTACHMENT PROCESSES AND EQUIPMENT").

LEAD ATTACHMENT PROCESSES AND EQUIPMENT:

The electrical and mechanical connection of the leads of a microelectronic device package to the wiring of a printed circuit board or other wiring assembly.

Lead Fatigue:

A weakening of the wire metal as a result of flexing.

Lead/Terminal Bonding:

(Wire Bonding)

The interconnecting of the terminal points on the device chip with the electrical leads provided by the device package.

LEAD TERMINAL BOND MODE:

Identification of the method of bonding intraconnecting leads within a microelectronic package to the terminal posts or tabs of the package leads (See "Lead/Terminal Bonding: ASSEMBLY").

Light Activated Silicon Controlled Rectifier (LASCR):

A PNPN semiconductor device in which contact is made to three of the four regions and a window is provided in the device package for illuminating the device with light radiation. Triggering can be accomplished either by raising the gate potential, as in a standard SCR or by application of radiant energy.

Limited (Report Security Classification):

Informational content not to be released to the general public.

(Linear Device Type (Analog Device Type, Linear Operational Type)):

The operational type of analog network as characterized by electrical symmetry or asymmetry with respect to a neutral or ground potential. (See "Single Ended" and "Differential").

Linear (Functional Category) (Analog Circuit, LIC):

The category of circuits in which the output response is a continuous linear or non-linear function of the input value. Such functional category includes a unit where analog signals are sampled or multiplexed.

Loose Material in Package:

(Loose Foreign Particle)

Particles included in and free to move around within the device package. Such particles may be introduced through loss of some device material or from extraneous sources.

Lot Acceptance:

(Quality Conformance Inspection)

Specified testing conducted through sampling of an inspection lot to allow submission of the product (devices) in compliance with procurement stipulations of the user.

Low Barometric Pressure:

(Vacuum, Reduced Barometric Pressure, Altitude Operation)

Exposure to an atmospheric stress (ambient condition) approaching the region of a vacuum or below sea-level standard pressure. (See "Failure Stress Domain, Vacuum").

LSI Interconnection Design; Computer Aids:

(Computer-Aided Discretionary Wiring (DIP), LSI Device Element Selection through Computer Aids)

Provisions for wafer testing, selection of "good" device elements and the associated intraconnections of large scale integrated (LSI) circuits. (See "Testing").

- M -

Machine Printout (Document Format):

RAC Library document is a collection of sheets prepared by printout machine terminal of computer.

Machine Processing:

(Automatic Data Processing, Computer-Aided Data Analysis)

Use of computers in reliability analysis.

Machine Sensible Format (Document Format):

RAC Library document is in a form accessible through direct entry into a computer input terminal. This format includes magnetic tape, punched cards, and paper tape.

Magnetic Film Storage Element:

A digital memory element based on the permanent magnetization properties of thin magnetic films.

Magnetism:

The force generated by moving electrical charges manifesting itself in various forms such as ferro-magnetic materials, interaction between current carrying conductors, etcetra.

MAINTAINABILITY:

Considerations of the facility with which a product may be repaired or kept in a state of operational readiness.

MAJOR SYSTEM:

Identification of principal systems applications in which the applied technology and device maturity is exemplified. Such applications, with large-scale and recurring utilization of relevant devices, are primarily military systems. The terms grouped under this descriptor heading are 'open ended'.

Malfunction Reports:

A log of data at the equipment level of inspection. This data includes the elapsed calendar time and operating hours of equipment use, hours to part failure, the responsible devices and device vendor, number of identical devices per equipment, and the part operating hours. This descriptor includes: Field Failure Reports.

Manual Systems:

Manually implemented techniques and provisions for recording, collection, or the reduction of data from reliability testing or application use monitoring.

Mask Design:

(Photomask Design)

Design techniques involved in the implementation of photolithographic patterns for microelectronic circuits. (See "Masking (PHOTOLITHOGRAPHY)").

Mask Design; Computer Aids:

(Computer-Aided Photomask Design)

Computer-aided approach to mask design. (See "Mask Design").

Masking:

The protection of areas of a wafer not to be etched or diffused by deposition of an impervious protective film.

Materials Control:

(Materials Screening)

The adoption and maintenance of adequate measures to insure control of material quality.

MATERIAL CONTROL (RAW) SPECS:

(Raw Material Screening Specs)

Specifications/standards for implementing adequate procurement and screening measures to insure control of raw material quality (See "Materials Control").

MATERIAL PREPARATION:

The processing required to prepare materials for use in fabricating solid state devices.

Mathematical Modeling:

(Logical Modeling, Design Formulation)

The development of a mathematical expression, or equation which describes the behavior of an electronic device or a physical process.

Maximum Fan-Out:

Rating, per equivalent gate circuit, of the maximum number of output ports of device network. A measure of a circuit's capability to drive a specified number of the same circuit from its output.

Less than 5	(See "Maximum Fan-Out")
5 thru 10	(See "Maximum Fan-Out")
Excess of 10	(See "Maximum Fan-Out")

Maximum Frequency of Operation:

Maximum number of periods per unit time at which device operates. An electrical rating.

Less than 10 Hz	(See Maximum Frequency of Operation)
10 Hz to less than 10 KHz	(See Maximum Frequency of Operation)
10 KHz to less than 10 MHz	(See Maximum Frequency of Operation)
10 MHz to less than 300 MHz	(See Maximum Frequency of Operation)
300 MHz to 300 GHz	(See Maximum Frequency of Operation)
Greater than 300 GHz	(See Maximum Frequency of Operation)

Maximum Operating Temperature:

Environmental capability to satisfactorily operate at given maximum thermal severity levels.

≥202.5°C	(See "Max. Operating Temp.")
172.5°C to <202.5°C	(See "Max. Operating Temp.")
152.5°C to <172.5°C	(See "Max. Operating Temp.")
102.5°C to <152.5°C	(See "Max. Operating Temp.")
<102.5°C	(See "Max. Operating Temp.")

Maximum Output Power:

Maximum rate at which electrical energy is transferred from the device output.

Less than 10 MW	(See "Max. Output Power")
10-100 MW	(See "Max. Output Power")
101-1 Watt	(See "Max. Output Power")
Greater than 1 Watt	(See "Max. Output Power")

Maximum Power Dissipation:

Maximum rate at which electrical energy is transformed into heat within the device. A device rating (per equivalent circuit input) (gate).

Less than 10 MW	(See Maximum Power Dissipation)
10 thru 30 MW	(See Maximum Power Dissipation)
Greater than 30 MW	(See Maximum Power Dissipation)

Maximum Storage Temperature:

Capability of satisfactory storage at given maximum thermal severity levels.

≥302.5°C	(See "Max. Storage Temp.")
252.5°C to <302.5°C	(See "Max. Storage Temp.")
202.5°C to <252.5°C	(See "Max. Storage Temp.")
152.5°C to <202.5°C	(See "Max. Storage Temp.")
102.5°C to <152.5°C	(See "Max. Storage Temp.")
<102.5°C	(See "Max. Storage Temp.")

Mechanical Environments, Accelerated Life Test Domain:

Test stress domain consists of an environment as included by the descriptor: "Mechanical Stress Testing". (See definition of term, as organizationally grouped under "TEST TECHNIQUES AND PROCEDURES").

Mechanical Environments, Step-Stress Test Domain:

Test stress domain consists of an environment as included by the descriptor: "Mechanical Stress Testing". (See definition of term, as organizationally grouped under "TEST TECHNIQUES AND PROCEDURES").

Mechanical Propagation:

The transport of mechanical energy through matter.

Mechanical Shock:

(Simulated Drop)

An environmental condition of suddenly applied forces or abrupt changes in motion. (See "Failure Stress Domain, Mechanical Shock").

Mechanical Stress Testing:

Environmental testing in which the applied stress domain subjects the device to bodily motion or changes in motion. "Mechanical Stress Testing" includes: the various types of vibration testing, constant acceleration and mechanical shock. (See "Failure Stress Domain, Vibration").

Medium Scale Integration (MSI):

(Less than 50)

The inclusion of an array of elemental circuits and components on a single substrate or semiconductor chip. Sometimes referred to as Complex Functions.

MEL DEVICE ELEMENT DESCRIPTOR:

A term which describes the individual electrical elements of which the microelectronic device is composed.

Metal:

An opaque substance which is a good conductor of electricity.

Metal Screen:

Deposition of a thick film in the form of a slurry by forcing the slurry through openings in a stainless steel wire mesh.

Metallization Discontinuity:

(Scratched Metallization, Gouged Metal Film)

A mechanical imperfection due to scratches, flaws, abrasions, or incomplete deposition, except pinholes, in the metal film. Metallization Discontinuity defines an irregularity in the conductive path, such as to result in an open circuit or localized current constriction.

Metallurgical Diffusion:

Diffusion of molecules of a metal used as an interconnection into the material (e.g., silicon) from which other components of the circuit are made, causing a change in the characteristics of the latter.

Metallurgical Phenomena:

Events occurring in metallic materials which change the nature of those materials.

Microcable:

"LEAD ATTACHMENT MODE" designed for interconnection with miniaturized cable connectors.

MICROELECTRONIC CATEGORY:

The unique classification of a microelectronic device in terms of its basic fabrication technology and physical/electrical form. Microelectronic Category descriptors identify currently available devices of interest.

MICROELECTRONIC DESIGN & DEVELOPMENT:

Informational content within the context of design and development of microelectronic devices or device elements.

Microfiche (Document Format):

RAC Library document is in microfiche format.

Microfilm (Document Format):

RAC Library copy of document is on microfilm.

Military:

Devices are of Qualification Class such that maintenance and replacement can be readily accomplished and down time is not critical. Parts in this class are produced to ordinary, non-Hi-Rel military specifications. Quality Assurance testing is conducted on sample basis. No special Screen/Burn-In testing is generally required. (See "QUALIFICATION CLASS").

Military and Space (Source):

Document authorship resides in a Department of Defense agency or NASA.

DOD (Military and Space Source):

Department of Defense authorship.

Air Force (Military and Space Source):

DOD agency author is an Air Force office.

Army (Military and Space Source):

DOD agency author is an Army office.

Navy (Military and Space Source):

DOD agency author is a Naval office.

NASA (Military and Space Source):

National Aeronautics and Space Administration authorship.

Military and Space (Sponsoring Organization):

A Department of Defense (DOD) agency of NASA is the client organization for authorship of document's information.

DOD (Military and Space Sponsoring Organization):

Department of Defense supported authorship.

Air Force (Military and Space Sponsoring Organization):

An Air Force agency supported authorship.

Army (Military and Space Sponsoring Organization):

An Army agency supported authorship.

Navy (Military and Space Sponsoring Organization):

Naval agency supported authorship.

Military and Space (Sponsoring Organization) (Cont'):

NASA (Military and Space Sponsoring Organization):

National Aeronautics and Space Administration supported authorship.

Military Upgraded:

Devices are qualified for use where maintenance and replacement can be performed, but is very difficult and expensive, and where reliability is imperative. Screen/Burn-In, as well as extensive QA tests are conducted on 100% of the product. Inspection procedures must meet requirements of a specification comparable to the Minuteman II requirements, or to the TX slash sheets of MIL-S-19500. (See "QUALIFICATION CLASS").

MIL-M-23700, Specification Reference:

Military Specification: MIL-M-23700 (NAVY), Microelectronic Functional Devices, General Specification for (Associated with eight specification slash sheets as of 25 June 1963).

MIL-S-19500, Specification Reference:

Military Specification MIL-S-19500 (DOD), Semiconductor Devices, General Specifications For

MIL-STD-202, Specification Reference:

Military Standard MIL-STD-202 (DOD), Test Methods for Electronic and Electrical Component Parts.

MIL-STD-750, Specification Reference:

Military Standard MIL-STD-750 (DOD), Test Methods for Semiconductor Devices.

Minimum Operating Temperature:

Environmental capability to satisfactorily operate at given minimum thermal severity levels.

$\geq$-42.5°C	(See "Min. Operating Temp.")
-62.5°C to $<$-42.5°C	(See "Min. Operating Temp.")
-82.5°C to $<$-62.5°C	(See "Min. Operating Temp.")
$<$-82.5°C	(See "Min. Operating Temp.")

Minimum Storage Temperature:

Capability of satisfactory storage at given minimum thermal severity levels.

≥-42.5°C	(See "Min. Storage Temp.")
-62.5°C to <-42.5°C	(See "Min. Storage Temp.")
-82.5°C to <-62.5°C	(See "Min. Storage Temp.")
-102.5°C to <-82.5°C	(See "Min. Storage Temp.")
<-102.5°C	(See "Min. Storage Temp.")

Misapplication:

(Improper Use, Incorrect Testing)

Mishandling or improper utilization of the microelectronic device. The descriptor: "Misapplication" includes overstressing the device, such as might occur during testing or application; erroneous positioning of the leads for external connection; and device mishandling.

Missile Environment:

Application environment associated with a weapons satellite designed for arming with warhead and being launched into a fraction of a complete earth orbit.

Modification; Circuit/Device Implementation:

(Circuit/Device Re-Work)

Implementation of improved circuits/devices through alteration or extension of previous designs. (See "CORRECTIVE MEASURES").

Module: Package Configuration:

A subassembly in a packaging scheme displaying regularity and separable repetition. May or may not be separable from other modules after initial assembly.

Modules:

"LEAD ATTACHMENT MODE" designed for interconnection with other microelectronic packages of modular configuration. (See "Module: PACKAGE CONFIGURATION").

Moisture Resistance:

(Humidity Cycling)

An atmospheric stress of cyclic changes of ambient humidity or moisture. (See "Failure Stress Domain, Moisture or Humidity").

Molded:

(See "Molded: ENCAPSULATION/PACKAGE SEALING").

Molding:

The encapsulation of a device by surrounding it with a plastic material which has been formed in a mold.

Molecular Electronic Function:

A linear or digital function which is performed by a block of semiconductor material which has been processed in such a way that no discernable circuitry is evident but which nevertheless has the properties of amplification, detection, light generation, etc.

Molybdenum:

A metallic element of Atomic Number 42.

Monolithic, Diffused (Fully IC, Diffused; Semiconductor IC, Diffused; All-Diffused Monolithic IC):

A monolithic integrated circuit in which all junctions are formed by diffusion techniques. (See "Monolithic Microelectronic Category").

Monolithic, Epitaxial (Fully IC, Epitaxial; Semiconductor IC, Epitaxial; Epitaxial Monolithic IC):

A monolithic integrated circuit in which at least one junction is formed through epitaxial growth of a crystalline layer. (See "Monolithic Microelectronic Category").

Monolithic IGFET (MOS Integrated Circuit, Metal-Oxide-Semiconductor IC, MOSFET IC, MOS IC, MTOS IC, MNS IC, SOS IC, MISFET IC):

An integrated circuit in which active elements consist of insulated-gate field effect transistor (IGFET) circuitry, and embodying composite IC technology for both passive and active circuit elements. (See "IGFET": MEL DEVICE ELEMENT DESCRIPTOR, and "Composite IC Microelectronic Category").

Monolithic Microelectronic Category (Fully IC, Pure IC, Semiconductor IC, MIC, Integral Functional Block)):

An integrated circuit in which all of the circuit components have been formed through diffusion or epitaxy in the top of a single crystal semiconductor block generally referred to as a die.

Monolithic, NOC (Not-Otherwise Classified Monolithic IC):

Monolithic integrated circuits which cannot be classified within any descriptors of the current glossary. (See "Monolithic Microelectronic Category"; "Monolithic, Diffused"; "Monolithic, Epitaxial"; and "Monolithic IGFET").

Monostable Multivibrator:

A two stage regenerative circuit capable of existing in two states, only one of which is stable. A triggering signal is required to cause the circuit to change states and after a finite time period, it returns to the original state.

MOS PROCESSES:

Specific fabrication techniques used in the production of microelectronic devices using MOS field effect transistors.

MOSTL (Digital Logic Type (Metal-Oxide-Semiconductor Transistor Logic)):

A digital logic type which is implemented through the use of metal-oxide-semiconductor (MOS) transistors in a switching circuit. (See "Monolithic IGFET" and "Digital Logic Type").

Multichip Microcircuit (Multichip Hybrid IC):

A microelectronic device whose circuit elements are fabricated upon two or more substrates and interconnected to form the device substrate assembly, to result in a set of two or more integrated circuit chips (or semiconductor IC wafers) where the IC's are within the same MICROELECTRONIC CATEGORY. (See "Hybrid Microcircuit" and "MICROELECTRONIC CATEGORY").

Multi-Layer Board:

(Multi-Layer Printed Circuits)

"LEAD ATTACHMENT MODE" permitting use of an assembly of "Printed Circuit Board(s)" consisting of several layers, with provisions for interconnections between layers.

Multiple Emitter Transistors:

(See also TTL)

A bipolar transistor, found only in integrated circuits, having multiple emitter regions and a single base and collector region. The emitter-base diodes act as the input diodes of a DTL gate.

Multivibrator:

A two stage regenerative circuit with a maximum of two stable states depending upon circuit characteristics and triggering conditions. A multivibrator may be constructed by cross connecting two logic gates. The three basic types are: astable multivibrator, monostable multivibrator, and the bistable multivibrator or flip flop. (See "Astable Multivibrator, CIRCUIT FUNCTIONS").

- N -

NAND Gate:

A logic gate with more than one input which gives an output of a logical "one" if any of the inputs are logical "zero", and an output of a logical "zero" only if all inputs are logical "one".

NASA, Specification Reference:

Classification of any NASA specification or standard.

Navigation:

A class of equipment which performs instrumentation and display, or control functions to direct the course of a vehicle's travel. This descriptor includes the term: "Radar", when such is integrally incorporated into the "Navigation" class.

N-Channel IGFET:

An insulated gate field effect transistor in which the conducting channel is contained in a bar of p-type semiconductor, into which heavily doped n-type contact regions are diffused and a lightly doped n-type layer is diffused between these contacts. This latter n-type region serves as the channel.

Negative Resistance/Gunn Effect:

When a device, through which current is being passed, exhibits a decrease in conductivity with an increase in applied voltage, it is said to have negative resistance. Negative conductance occurring in gallium arsenide at high electric field is called Gunn Effect.

Nichrome:

An alloy consisting of 80% Nickel and 20% chromium.

Nickel:

A metallic element of Atomic Number 28.

Noise Figure:

The factor by which the signal-to-noise ratio of an amplifier exceeds that of an ideal amplifier.

Noise Margin:

The largest noise pulse a digital circuit can tolerate when in a given state without switching to the opposite state.

Non-Destructive Evaluation:

(Non-Destructive Testing)

Utilization of any of the FAILURE ANALYSIS TECHNIQUES which inherently do not permanently modify the properties of the device or device element.

(Non-Functional Elements):

Elements of microelectronic devices and circuits which do not enter into the functional role of same. Generally they provide physical support or protection.

Non-Military Government Agency (Source, other than NASA):

Governmental agency authorship such as the Dept. of Commerce.

Non-Military Government Agency (Sponsoring Organization, other than NASA):

Government agency (such as the Department of Commerce) supported authorship.

NOR Gate:

A logic gate with more than one input which gives an output of a logical "zero" if any of the inputs are a logical "one", and an output of a logical "one" only if all of the inputs are a logical "zero".

Not Certified (Data Validation):

No DATA VALIDATION due to lack of signature to indicate responsibility for test results by an official of the document SOURCE organization. This DATA VALIDATION ranks lowest among the set of eight descriptors.

Certified by Responsible Report-Source Official (Data Validation):

Signature given to indicate responsibility for test results by an official of the SOURCE organization.

NPN Transistor:

A bipolar transistor in which the emitter and collector regions are formed from n-type semiconductor and the base region from p-type semiconductor.

NUMBER OF MAJOR PROCESS STEPS:

(PROCESS COMPLEXITY)

Quantity of principal steps in the fabrication process of devices. This quantity gives a supplementary index of the device complexity. Numbers reflect particular emphasis to critical diffusion and isolation steps. Such critical steps are associated with the contact cuts or pre-ohmic etches. The following table presents the "NUMBER OF MAJOR PROCESS STEPS" for typical device types. Specific values indicated by Fabrication Process data from vendors shall take precedence.

No. of Process Steps	Typical Devices
3	Enhancement Mode MOS Enhancement Mode MOS with MOS Cap
4	Triple Diff Depletion Mode MOS Resistive Isolation
5	Epitax Diff Triple Diff with MOS capacitor Res Iso with MOS capacitor Diel Isolation Enhancement Mode MOS with Thin Film Resistor
6	Epitax Diff with Buried Layer Epitax Diff with MOS CAP Triple Diffused with Thin Film Res Triple Diffused with Thin Film CAP Diel Iso with MOS CAP Diel Iso with Buried Layer Res Iso with Thin Film Cap Res Iso with Thin Film Res
7	Epitax Diff with Thin Film Res Epitax Diff with Thin Film Cap Diel Isol with Thin Film Cap Diel Isol with Thin Film Res

NUMBER OF MAJOR PROCESS STEPS (Cont'):

No. of Process Steps	Typical Devices
8	Epitax Diff with MOS Cap & Buried Layer Diel Iso with MOS Cap & Buried Layer
9	(Value as indicated by fabrication process data from vendors)
10	(Value as indicated by fabrication process data from vendors)
11	(Value as indicated by fabrication process data from vendors)
12	(Value as indicated by fabrication process data from vendors)
Other	(Value as indicated by fabrication process data from vendors)

- O -

Open Circuit:

(Open)

A circuit path through which the flow of current is discontinuous, or in which continuity is interrupted. Presence of an unusually small load current, or of an unusually large potential drop (when potential supply is a current source).

Operating Tests:

(Operation Life Tests)

Tests which subject the devices to electrical stress domains (power, voltage, current) to provide a reliability assessment of device performance. "Operating Tests" may be conducted in several categories of environment, including: laboratory life inspection and application use conditions.

Operation Amplifier:

A linear electronic circuit having very high voltage gain and provision for applying appropriate feed back to enable the circuit to perform analogic mathematical operations on electrical signals.

OPERATIONAL DYNAMIC LIFE TEST:

(A-C OPERATION LIFE TEST, FUNCTIONAL LIFE TEST)

"Operating Test(s)" in which an a-c or switching functional domain of electrical stress is applied to the circuit, and maintained as a steady-state frequency or switching repetition rate condition throughout the test. Performance indices which can be monitored during the operating life are active parameters of the test specimen. Such (dynamic) parameters, having dependences upon interacting circuit responses, include rise time, fall time, and propagation delay. Two modes of in-test monitoring of circuit parameters are particularly applicable to digital type devices. These are dynamic monitoring and functional monitoring. Dynamic monitoring may result in raw variables data; while functional monitoring logically compares the test device's response and yields go/no-go test results. (See "Operating Tests (TEST TECHNIQUES AND PROCEDURES)").

OPERATIONAL DYNAMIC TEST LOAD POWER:

Dynamic electrical stress condition of relative load-power severity level at which the "OPERATIONAL DYNAMIC LIFE TEST" is conducted.

Operational Dynamic Test Load Power (<95% Rating)

Relative severity level is less than 95 percent of rated load power.

Operational Dynamic Test Load Power (95% to <105% Rating)

Relative severity level is in the range from 95% to less than 105 percent of rated load power.

Operational Dynamic Test Load Power (105% to <155% Rating)

Relative severity level is in the range from 105 percent to less than 155 percent of rated load power.

Operational Dynamic Test Load Power (≥155% Rating)

Relative severity level is in the range greater than or equal to 155 percent of rated load power.

OPERATIONAL DYNAMIC TEST SUPPLY VOLTAGE:

Dynamic electrical stress condition of relative supply voltage severity level at which the "OPERATIONAL DYNAMIC LIFE TEST" is conducted.

Operational Dynamic Test Supply Voltage (<95% Rating)

Relative severity level is less than 95 percent of rated supply voltage.

Operational Dynamic Test Supply Voltage (95% to <105% Rating)

Relative severity level is in the range from 95 percent to less than 105 percent of rated supply voltage.

Operational Dynamic Test Supply Voltage (105% to <155% Rating)

Relative severity level is in the range from 105 percent to less than 155 percent of rated supply voltage.

Operational Dynamic Test Supply Voltage (≥155% Rating)

Relative severity level is in the range greater than or equal to 155 percent of rated supply voltage.

OPERATIONAL DYNAMIC TEST TEMPERATURE:

(AMBIENT TEMPERATURE CONDITION, A-C OPERATION LIFE)

The environmental condition of ambient thermal severity level at which the "OPERATIONAL DYNAMIC LIFE TEST" is conducted.

Operational Dynamic Test Temperature <-82.5°C:

Temperature severity level less than -82.5 degrees Centigrade.

Operational Dynamic Test Temperature -82.5°C to <-42.5°C:

Temperature severity level is in the range from -82.5 degrees to less than -42.5 degrees Centigrade.

Operational Dynamic Test Temperature -42.5°C to <21°C:

Thermal severity level is in the range from -42.5 degrees to less than 21 degrees Centigrade.

Operational Dynamic Test Temperature 21°C to <31°C:

Thermal severity level is in the range from 21 degrees to less than 31 degrees Centigrade.

Operational Dynamic Test Temperature 31°C to <102.5°C:

Thermal severity level is in the range from 31 degrees to less than 102.5 degrees Centigrade.

Operational Dynamic Test Temperature 102.5°C to <152.5°C:

Thermal severity level is in the range from 102.5 degrees to less than 152.5 degrees Centigrade.

Operational Dynamic Test Temperature 152.5°C to <202.5°C:

Thermal severity level is in the range from 152.5 degrees to less than 202.5 degrees Centigrade.

Operational Dynamic Test Temperature 202.5°C to <302.5°C:

Thermal severity level is in the range from 202.5 degrees to less than 302.5 degrees Centigrade.

Operational Dynamic Test Temperature ≥302.5°C:

Thermal severity level is in the range greater than or equal to 302.5 degrees Centigrade.

OPERATIONAL STATIC LIFE TEST:

(D-C OPERATION LIFE TEST)

"Operating Tests" in which a d-c electrical stress domain is applied to the circuit and maintained as a steady-state condition throughout the test. Such test may be considered as approaching the simulation of circuit operation with no input signal applied. Performance indices which can be detected during the operating life are parameters which are independent of other possible circuit responses (static response sampling). Malfunction examples are open circuit, short circuit, and leakages. (See "Operating Tests (TEST TECHNIQUES AND PROCEDURES)").

OPERATIONAL STATIC TEST LOAD POWER:

Static electrical stress condition of relative load-power severity level at which the "OPERATING STATIC LIFE TEST" is conducted.

Operational Static Test Load Power (<95% Rating)

Relative severity level is less than 95 percent of rated load power.

Operational Static Test Load Power (95% to <105% Rating)

Relative severity level is in the range from 95 percent to less than 105 percent of rated load power.

Operational Static Test Load Power (105% to <155% Rating)

Relative severity level is in the range from 105 percent to less than 155 percent of rated load power.

Operational Static Test Load Power (≥155% Rating)

Relative severity level is in the range greater than or equal to 155 percent of rated load power.

OPERATIONAL STATIC TEST SUPPLY VOLTAGE:

Static electrical stress condition of relative supply-voltage severity level at which the "OPERATIONAL STATIC LIFE TEST" is conducted.

Operational Static Test Supply Voltage (<95% Rating)

Relative severity level is less than 95 percent of rated supply voltage.

Operational Static Test Supply Voltage (95% to <105% Rating)

Relative severity level is in the range from 95 percent to less than 105 percent of rated supply voltage.

Operational Static Test Supply Voltage (105% to <155% Rating)

Relative severity level is in the range from 105 percent to less than 155 percent of rated supply voltage.

Operational Static Test Supply Voltage (≥155% Rating)

Relative severity level is in the range greater than or equal to 155 percent of rated supply voltage.

OPERATIONAL STATIC TEST TEMPERATURE:

(AMBIENT TEMPERATURE CONDITION, D-C OPERATION LIFE)

The environmental condition of ambient thermal severity level at which the "OPERATIONAL STATIC LIFE TEST" is conducted.

Operational Static Test Temperature <-82.5°C:

Temperature severity level less than -82.5 degrees Centigrade.

Operational Static Test Temperature -82.5°C to <-42.5°C:

Temperature severity level is in the range from -82.5 degrees to less than -42.5 degrees Centigrade.

Operational Static Test Temperature -42.5°C to <21°C:

Thermal severity level is in the range from -42.5 degrees to less than 21 degrees Centigrade.

Operational Static Test Temperature 21°C to <31°C:

Thermal severity level is in the range from 21 degrees to less than 31 degrees Centigrade.

Operational Static Test Temperature 31°C to <102.5°C:

Thermal severity level is in the range from 31 degrees to less than 102.5 degress Centigrade.

Operational Static Test Temperature 102.5°C to <152.5°C:

Thermal severity level is in the range from 102.5 degrees to less than 152.5 degrees Centigrade.

Operational Static Test Temperature 152.5°C to <202.5°C:

Thermal severity level is in the range from 152.5 degrees to less than 202.5 degrees Centigrade.

Operational Static Test Temperature 202.5°C to <302.5°C:

Thermal severity level is in the range from 202.5 degrees to less than 302.5 degrees Centigrade.

Operational Static Test Temperature ≥302.5°C:

Thermal severity level is in the range greater than or equal to 302.5 degrees Centigrade.

OPERATIONAL TYPE (NETWORK TYPE:

An expanded generic level of designations within the scope of descriptors included under "FUNCTIONAL CATEGORY", in terms of the basic network configuration of "Digital Logic Type" and "Linear Device Type"(s). (See definitions of these terms.)

OR Gate:

A logic gate with more than one input which gives an output of a logical "one" if any of the inputs are a logical "one" and an output of a logical "zero" only if all inputs are a logical "zero".

OTHER, NOC:

A termatrex category containing descriptors for relevant informational content not classifiable within any Major Termatrex Category of the current glossary.

Output Impedance:

The impedance presented by the device to the load. A device characteristic.

Less than 10 K Ohms (See "Output Impedance")
10 K thru 100 K Ohms (See "Output Impedance")
Greater than 100 K Ohms (See "output Impedance")

Overstressed Device:

(Excess Severity Level Exposure)

Application of a level of severity within a given stress domain which exceeds the device's specification or design limits.

Oxidation:

The conversion of a substance into an oxide of that substance, e.g., aluminum to aluminum oxide.

OXIDATION:

The conversion of the semiconductor material at the surface of the wafer to an oxide to act as a barrier to impurify diffusion and as protection to the completed device.

Oxidation Defect:

(Improper Oxide Protection, Inadequate Surface Passivation, Corrosion)

A surface defect due to an inadequate protective layer of oxide, except for "Pin Holes in Oxide"; or, due to presence of oxide products of corrosion.

- P -

PACKAGE CONFIGURATION:

General classification of the device package in terms of its form, sealing property, and material. (See "PACKAGE TYPE", also).

Package Failure:

(Packaging Defect)

Failure of any connection, isolation, and enclosure provisions of the microelectronic device. This failure mode includes "broken leads", "defective seal", and other mechanical damage.

Package Material (Primary):

The materials employed in fabricating encapsulating containers for microelectronic devices and circuits.

PACKAGE SEAL:

The sealing method of all apertures in a microelectronic package which prevents leakage of inert atmosphere out of and contaminating gases into the package. (See "ENCAPSULATION/PACKAGE SEALING").

Package Terminal Material:

Metallic material from which electrical terminals of a microelectronic circuit or device package are fabricated.

PACKAGE TYPE:

Specific classification of the device package in terms of the JEDEC designated "TO" type number, and according to number of leads for the "Dual In-Line, Plastic (DIP)" configuration, where these identifiers are applicable. Specific "PACKAGE TYPE" terms are listed as follows: (See "PACKAGE CONFIGURATION").

(Can, Hermetically Sealed):

TO-5 TO-72 TO-75 TO-78 TO-96

TO-70 TO-73 TO-76 TO-79 TO-99

TO-71 TO-74 TO-77 TO-80 TO-100

(Flat Pack):

TO-84	TO-87	TO-90
TO-85	TO-88	TO-91
TO-86	TO-89	TO-95

(DIP Lead Type):

Dual In-Line, 10-Lead
Dual In-Line, 14-Lead
Dual In-Line, NOC (Lead)

Packaging:

Considerations of the design of device and assembly packages, primarily with regard to facility of implementation or to ease of application.

PACKAGING & DELIVERY SPECS:

(PRODUCT HANDLING & SHIPMENT SPECS)

Specifications and standards covering the preparation of microelectronic devices for delivery, inventory storage conditions, and their handling during transmittal of order.

PART LEVEL DATA:

Quantitative information and supporting details resulting from testing and inspection activities with microelectronic devices (at the part level).

P-Channel IGFET:

An insulated gate field effect transistor in which the conducting channel is contained in a bar of n-type semiconductor into which heavily doped p-type contact areas are diffused and a lightly doped n-type layer is diffused between these contacts. This latter p-type region serves as the channel.

Performance Curves:

(Characteristics Plots, Rating/De-Rating Curves, Parameter Distribution vs. Inspection Lot)

Data in graphical form, such as may be summarized from "Performance" testing. (See "Performance: TEST TYPE"). Includes plots of: Parameter Density Distributions (Histograms).

Performance Measurement:

(Device Parameter Measurement)

Measurement of device parameter values under conditions associated with test operation, reliability inspection or application use.

Performance (Test Type):

(Operational Capability Inspection, Device Functional Characterization)

Testing oriented toward revealing operational capabilities and limitations of the device. Inspection procedures for suitably classifying the device's characteristics/rating properties.

Phosphorus:

An element of Group V of the Periodic Table which acts as a donor impurity in Si and Ge.

Photochromic Paints:

(Thermally Responsive Photochromic Materials, Thermographic Mapping with Phosphor Paints, Thermographic Mapping with Cholesteric Liquids, "Spectratherm" Material)

Inspection through utilization of the thermally sensitive iridescence or luminescence of certain materials.

Photoconductivity:

The generation of carriers in a material by the absorption of light energy.

PHOTOLITHOGRAPHY:

The photographic steps required to transfer the mask pattern from the drafting table to the wafer.

Photoresist:

An organic chemical which, when exposed to light energy, becomes polymerized and insoluble. It is impervious to etching chemicals and is used to define areas of the material which are intended to be etched.

Photoresponse Mapping:

(Photoscanning)

Evaluation of device or device element through correlation of light probe positions with generated photocurrents.

PHYSICAL DEFECTS:

(FAILURE MECHANISMS, QUALITY DEFECTS, PHYSICS OF FAILURE MECHANISMS, FAILURE DIAGNOSIS)

The device defects which substantiate failure modes at the primary in-depth level of failure analyses. Defects which result from the contributions of CAUSES OF FAILURE, FAILURE PHENOMENA, and FAILURE ENVIRONMENT/STRESS DOMAIN.

Physical Parameters:

Those measurable properties of materials and media on which design and analysis of electronic devices are based.

Physical Phenomena:

An event or characteristic occurring in nature which can be exploited in the development or operation of an electronic device.

Pilot Production:

Device status is past the stage termed "Developmental". Engineering effort is principally concerned with determining full-scale production feasibility and in refining the process techniques for the device. (See "ITEM STATUS").

Pinch Off:

In a junction field effect transistor, the bias on the gate causes the depletion region in the semiconductor to enlarge, reducing the conductivity of the semiconductor channel. When the depletion regions meet in the center of the channel, the channel is said to be pinched off and no further increase in current will occur as source-drain voltage increases.

Pin Holes in Metallization:

(Metallization Pinholes/Flaws)

A mechanical imperfection due to pinholes in a metallization layer of the device.

Pin Holes in Oxide:

(Oxide Shorts through Pinholes/Flaws, Oxide Pinholes/Flaws)

A surface defect due to pinholes in an insulative oxide or dioxide film of the device.

Planar Junction:

A pn semiconductor junction in which the contacts to both regions separated by the junction are made on the same device surface or plane.

Plastic Encapsulated (Non-DIP Plastic Cap):

A plastic encapsulation package which is not a Dual In-Line Plastic (DIP) encapsulated (Cap) type. (See "Dual In-Line, Plastic").

Plastic, Silicon Resin:

A non-metallic, organic compound using a silicon resin base capable of being molded into various shapes and hardened.

Platinum:

A noble metal element of Atomic Number 78.

PNP Lateral:

In integrated circuits, a PNP bipolar transistor formed by diffusing two p-type areas located laterally in a larger n-type region and having relatively low gain. Usually connected in series with an NPN transistor to provide increased gain.

PNPN Devices:

Transistor-like semiconductor devices having four regions of alternate polarity, P or positive and N or negative, separated by potential barriers.

PNPN Latch-Up:

The latching "on" of an integrated circuit transistor as a result of a parasitic transistor connected to it, forming a regenerative pnpn device.

PNP Transistor:

A bipolar transistor in which the emitter and collector regions are formed from p-type semiconductor and the base region from n-type semiconductor.

Polymerization:

The linking of monomer molecules of organic materials into polymer chains of molecules.

Poor Design:

(Inadequate Device Type)

Features of the device or processing poorly designed with regard to requirements. Weaknesses of the device design and fabrication process design which may serve as causes of failure.

Poor Metallization Adhesion:

(Lifted Metallization Film, Improper Metal Film Adherence)

A metallurgical or surface defect due to inadequate adherence of the deposited metal film. Other terms included in this descriptor are: lifted bond pad and poor aluminum contact at oxide windows.

Post-Production Screens:

(Screening/Burn-In Tests, Product Screen/Conditioning)

Combination of tests designed to identify specimens with quality defects (those likely to exhibit early failures); or, tests designed to stabilize the products' characteristics. (See "Failure Environment, Post-Production Screen/Burn-In").

Power:

(Power Supplies)

A class of equipment which furnishes electric energy to circuits.

Power, Accelerated Life Test Domain:

(Electric Power Input)

Accelerated life test where stress domain of interest is electrical input energy.

Power Amplifier:

A linear electronic circuit designed to provide power gain at high power levels (output power greater than 1 watt).

Power Dissipation:

(See "Maximum Power Dissipation: ELECTRICAL PROPERTIES").

Power, Intermittent Stress Domain:

(Electric Power)

Rate of transforming electrical energy, or the rate of transferring electrical energy input.

Power, Step-Stress Test Domain:

(Electric Power Input)

Step stress test where the stepped domain is electrical input energy.

Power Transistor:

A bipolar transistor of large junction area placed in a heat-sinkable package designed to handle high power levels (i.e., $P > 1$ watt).

PREDICTION AND MODELING:

(RELIABILITY THEORY, ASSESSMENT AND ANALYSIS, MATHEMATICS OF RELIABILITY)

Assessment of reliability by deduction and induction, with utilization of various analytical techniques, including extrapolation, mathematical modeling, empirical estimation from failure analysis studies, and computer-aided probabilistic simulation.

Pressure Connector:

"LEAD ATTACHMENT MODE" of a spring type insertion/detachment socket for making contact. The term "Microcable" is excluded by this descriptor.

Printed Circuit Board:

"LEAD ATTACHMENT MODE" requiring use of mounted circuit elements which serve as the fixed wiring connections, as 'printed' on the mounting board.

Probing:

Performing electrical measurements on devices while still in wafer form, using special probes, to select and reject unusable devices.

Procedure Approved by Source Sponsor (Data Validation):

Test results obtained through procedures approved by the SPONSORING ORGANIZATION, as indicated via "Certified by Responsible Report-Source Official" and either:

a) Countersignature of such statement by agent of SPONSORING ORGANIZATION;

b) Reference made to governing specifications of the SPONSORING ORGANIZATION;

c) Item (b) and use of approved reporting forms.

Proceedings, Symposia, or Conference (Report Type):

A publication or collection of papers which comprise the report of a technical meeting, symposium, or conference.

Process Control:

(Fabrication Process Monitoring)

Exercise of adequate procedures during the fabrication processes to minimize quality defects and to maximize the product yield. Detail in-process test procedures are excluded from the scope of this descriptor.

PROCESS CONTROL SPECS:

(Fabrication Process Monitoring Specs)

Specifications/standards delineating procedures and control criteria required to minimize quality defects and to maximize yield during fabrication processes. Detailed in-process test procedures are included in the scope of this descriptor. (See "Process Control" and "In-Process Inspection Procedures").

PROCESS CONTROL TECHNIQUES:

Instrumentation and measurement procedures used to monitor essential parameters during the fabrication of devices such that control over the quality of the device is maintained.

Process Design:

(Fabrication Specifications, Processing Procedures)

Delineation of the fabrication operations, including the process monitoring steps. Design of the processing system or facility.

PROCESS EFFECTIVENESS:

A term describing the merit of a process in terms of the cost, reliability, size and weight of the product.

Process Equipment Design:

(Fabrication Equipment Specification)

Design of an item of equipment used in the fabrication processes.

Process Equipment Improvement:

(Specification Upgrading of Fabrication Equipment)

Development of an improved item of equipment used in the fabrication processes.

Process Errors:

(Process Control Loss)

Deviation from required precision of equipment during device fabrication, such as to cause quality defects.

Process Improvement:

(Processing Refinement, Fabrication Specifications Upgrading)

Development of improved fabrication operations or the processing system, exclusive of the process monitoring steps (See "Process Control" for the latter connotation).

Procurement Specification:

(User Stipulation)

Documentation from the product buyer to specify his requirements for microelectronic devices.

Production:

Device status is at full-scale fabrication capability, with maturity in its basic performance capabilities. (See "ITEM STATUS").

Production Test and Inspection:

(Product Line Audit, Product Quality Monitoring)

(See "Failure Environment, Product Inspection").

Product Line Audit:

(IN-HOUSE TEST Program)

A vendor originated final inspection program, generally patterned along the lines of military lot acceptance requirements, conducted in anticipation and in partial fulfillment of user requirements for high-reliability products. In-house reliability (quality) test programs, such as SURE and PACE fall into this category.

Propagation Delay:

The maximum time required to transfer a pulse through the circuit of device.

Less than 10 Nanoseconds	(See "Propagation Delay")
10 thru 30 Nanoseconds	(See "Propagation Delay")
Greater than 30 Nanoseconds	(See "Propagation Delay")

Proprietary Information (Report Security Classification):

Restriction on dissemination of privileged information, as imposed by the document's source in accordance with their deemed interests.

Purification and Refinement:

The removal of impurities from materials to be used in device fabrication.

"Purple Plaque" Formation:

Formation of a brittle alloy of Aluminum, Gold and Silicon where all three are present in an interconnection on a microelectronic device.

QUALIFICATION CLASS (RELIABILITY CLASS):

The class of service for which device is intended or qualified, as provided through the reliability assurance measures taken during and after device fabrication.

Qualification, Procurement:

(Qualification Inspection, Product Qualification)

Specified testing conducted to ascertain a vendor's capability to produce a product in accordance with user requirements. Military users may accordingly place such product on a Qualified Products List (QPL). Initial qualification and periodic surveillance is maintained by government inspections.

Quality Assurance (Device Test Oriented):

A planned and systematic pattern of all actions necessary to provide adequate confidence that the device will satisfactorily perform according to service requirements of actual operation. Such data is generated during quality and reliability evaluations as a part of the vendor's normal quality assurance program. Included are activities such as "Screening", "Lot Acceptance", and "Qualification" testing. (See "Quality Assurance Measures (CORRECTIVE MEASURES)").

Quality Assurance Measures:

Inspection procedures employed upon the completed product to insure adequate confidence of the user in the device's ultimate reliability. (See "Quality Assurance Test Type").

QUALITY ASSURANCE SPECS:

(QUALITY CONFORMANCE SPECS/STANDARDS, QA SPECS)

Specifications/standards delineating practices and inspections to insure adequate confidence of the user in the completed device's qualifications.

Quality Control Manuals:

(Quality Procedures Manual)

Mandatory standards governing the procedures associated with the fabrication processes for optimizing continuing product yields and for processing control information on device quality.

<u>R & D & Test Laboratories</u> (Sources include University Labs.):

Document source such as ARINC, Battelle, or Stanford.

<u>R & D & Test Laboratories</u> (Sponsoring Organizations include University Labs.):

Client organization, such as ARINC, Battelle, or Stanford, which supported document's authorship.

<u>Radar</u>:

(Radio Detection and Ranging)

A class of equipment which operates through transmitting a beam of radio-frequency energy, and measuring or analyzing the reflected portion of this energy (the echo).

<u>RADC Spec. #2867, Specification Reference</u>:

RADC Specification 2867 (AFSC, RADC), Quality and Reliability Assurance Procedures for Monolithic Microcircuits.

<u>Radiation Emission/Electroluminescence</u>:

The emission of energy such that it travels in rays through space. Electroluminescence is the emission of light energy as the result of absorption of electrical energy by matter.

<u>Radiation Environments</u>:

(Radiation Exposure; Radiation, Electromagnetic)

Environmental stress domains in which devices are exposed to particulate radiation, and to irradiation by ambient energy of the electromagnetic spectrum. (See "Failure Stress Domain, Radiation Exposure, Particle" and "Failure Stress Domain, Radiation, Electromagnetic").

<u>Raw Variables Data</u>:

Data in the form of measured parameter values and associated conditions, for a complete test or inspection sample.

RCTL (Digital Logic Type) (Resistor-Capacitor-Transistor Logic):

A digital logic circuit configuration identical to RTL except that a capacitor is connected in parallel with each gate input resistor in order to decrease switching time. (See "RTL" and Digital Logic Type).

R/D Report (Report Type):

A research and development report. A periodic or singly issued technical treatise of current research and development activity or the status or pre-production concepts. A report which documents original research activity (in contradistinction to "Technical Report").

Re-Design:

(Design Re-Specification)

Redesign of microelectronic modifiers to result in a mature device. Redesign may involve the device, the fabrication processes, or the process equipment.

Reliability and Environmental Test:

(Test Equipment, Environmental Chambers, Testers)

Testing of devices subjected to operating life conditions or to controlled test environments. Provisions for application of appropriate test conditions in terms of laboratory or field test equipment and controlled environmental chambers. (See "Reliability and Environmental Test Methods (QA SPECS)").

Reliability and Environmental Test Methods:

(Test Methods for Reliable Devices)

Specification and standardization of test methods for reliability evaluation of devices in various environments.

Reliability Attributes Summary:

Reduced test or inspection data in terms of results which are time dependent (stoichastic variable summary). (See "Attributes Data Analysis"). Data in the form of attributes of reliability, such as failure rate and hazard rate. Terms such as the following are included by this descriptor: Failure Summary for Selected Parts, Failure Rate versus Stress, and Failure Rate Distribution. Also, "raw" data through measurements of the GO/NO-GO type is covered by this descriptor.

RELIABILITY DATA:

(SYSTEM/EQUIPMENT LEVEL DATA)

Quantitative information and supporting details resulting from testing and reliability inspection activities of assembled devices at the equipment level.

Reliability Data NOC:

(Not-Otherwise Classified Equipment Level Data)

Reliability Equipment-level data which cannot be classified within any descriptor of the current glossary.

Reliability Demonstration:

(See "Reliability Demonstration: TEST TYPE", and "AGREE TEST: TEST TECHNIQUES & PROCEDURES").

Reliability Demonstration:

Testing performed to assess potential reliability of the product through applying a combination of conditions (such as, life, vibration, temperature cycling, and intermittent power stressing), which are intended to closely simulate the actual conditions of operational service. (See "Reliability Demonstration (APPLICATION STATUS)").

Reliability Rating:

(Min/Max. Failure Rate)

Rated reliability capability of device in terms of specified levels of failure rate. The specification generally requires proof of compliance.

Less than 0.001% per 1000 hours	(See "Reliability Rating")
0.001% to less than 0.01% per 1000 hours	(See "Reliability Rating")
0.01% to less than 0.1% per 1000 hours	(See "Reliability Rating")
Greater than 0.1% per 1000 hours	(See "Reliability Rating")

RELIABILITY TECHNOLOGY:

Information on all elements of reliability methods, procedures, controls, statistical tools and evaluation facilities.

REPORT DATE (DOCUMENT DESCRIPTOR):

The indicated year in which RAC held document was published. Indexing example: "Report Date" - 1966.

REPORT SECURITY CLASSIFICATION (DOCUMENT DESCRIPTOR):

Status of permissible access to informational content of RAC held document, by reasons of national or industrial security.

REPORT SOURCE (DOCUMENT DESCRIPTOR):

The organizational authorship (or editorship) of information contained in RAC held document.

REPORT TYPE (DOCUMENT DESCRIPTOR):

A classification of the RAC held document in terms of the purpose of formal documentation of its informational content.

Residual Gas Analysis:

Mass spectrometric analysis of the composition of gas present in a vacuum system during thin film deposition.

Resistance Welding:

The welding of two metals in which heating of the metals is accomplished through dissipation of electrical power in the immediate vicinity of the weld.

Resistive (Intrinsic Isolation):

Isolation accomplished through utilization of intrinsic resistance between device element regions within the semiconductor substrate. This isolation method finds particular application at high frequencies. (See "Resistivity, DEVICE PARAMETERS" and "ISOLATION METHOD").

Resistivity:

The electrical resistance of a specific volume of a material.

Resonance:

The state of an oscillating system when driven by a force whose oscillating frequency is the same as the natural frequency of the system.

Resonant Gate FET:

A field effect transistor in which the gate electrode is located on the end of a mechanically resonant cantilever beam and suspended over the conducting channel in the semiconductor. The electric field which modulates the conductivity of the channel is varied by the vertical motion of the gate as the beam vibrates. This motion is maximum at the mechanical resonant frequency of the beam, thereby providing frequency selection, or filtering.

Reverse Breakdown:

The dramatic increase in current through a reversed biased diode occurring at some threshold voltage.

RF Amplifier:

A linear electronic circuit having high frequency response characteristics and medium power gain designed to amplify signals found in the high frequency stages of a communications system.

RF-IF Amp:

As a descriptor index of "CIRCUIT COMPLEXITY", this is a linear network characterized by a capability of very high frequency operation, but need not have wideband ability. RF (radio-frequency) amplifiers, and RF amplifiers coupled with frequency selective networks to serve as IF (intermediate-frequency) amplifiers, are covered by this descriptor. Another application is use as an oscillator. (See "Single Ended (Linear Device Type)").

RF Interference:

(Electromagnetic Radiation, RF; Electromagnetic Interference, RF; Radio-Frequency Noise)

An electromagnetic environment of (exposure) ambient spurious energy in the radio-frequency range. (See "Failure Stress Domain, Radiation Electromagnetic").

RTL (Digital Logic Type) (Resistor Transistor Logic):

A digital logic circuit configuration identical to DCTL except that resistors are placed in series with the base of the transistor associated with each input of a gate. The generic RTL type includes ancronyms such as MRTL, MWRTL, LPRTμL, and RTμL. (See "Digital Logic Type" and "DCTL").

- S -

Salt Atmosphere/Spray:

(Corrosion, Marine Fog)

An Atmospheric stress of a fine mist of salt solution or exposure to a sea-coast atmosphere. (See "Failure Stress Domain, Salt Atmosphere/Spray").

Sapphire:

A single crystal of aluminum oxide.

Satellite Launch:

"Spacecraft Environment" in which the system equipment is being thrusted into an orbital condition, or auxiliary subsystem to accomplish orbit.

Satellite Orbit:

(Satellite Flight)

"Spacecraft Environment" in which the system equipment is in flight (orbital) operational service.

SCALE OF INTEGRATION:

The degree to which the many circuit functions in a electronic system are integrated into a single package.

Scratches:

(Nicks, Abrasions of Device Elements, Gouges)

Abrasions or scratches occurring upon device element surface, such as to result in metallization or insulative film discontinuities, or, in the reduction of effective cross-sectional area of device element. This descriptor also includes the nicking of wire intraconnections.

Screening:

(Processing Control)

Production inspection of the product to identify and remove specimens with quality defects. (See "Screening Procedures").

Screening Procedures:

(Processing Control Procedures)

Procedures associated with production test and inspection of devices to identify and remove specimens with quality defects. (See "Post-Production Screens (CORRECTIVE MEASURES)").

Scribing:

Scratching the wafer on the lines dividing individual devices to enable separating them from each other.

Seal Leak:

(Leaky Encapsulation, Hermeticity Loss)

A mechanical imperfection of the packaging due to voids, cracks or other deficiencies of the package seal, resulting in loss of sealing quality.

Seam Weld:

(See "Seal Weld: ENCAPSULATION/PACKAGE SEALING").

Seam Welding:

The joining of header to cap by welding the seam in a metal device package.

Secondary Breakdown:

A destructive avalanche type breakdown, apparently thermally excited, occurring at high forward current density in junction transistors.

Secret (Classified, Report Security Classification):

Unauthorized disclosure of informational content is forbidden, since such could result in serious damage to the national security.

Servo Amplifier:

A linear electronic circuit of high gain and provision for appropriate feed back and capable of sufficient output power to drive a servomechanism motor.

Shear Modulus:

The degree of shearing stress required to produce a unit shear strain in a material.

Shipboard Environment:

Application environment associated with an equipment system designed for normal service in or upon water.

Shipboard Submarine:

A "Shipboard Environment" in which the equipment system is designed for submersion and travel under water.

Shipboard Surface:

A "Shipboard Environment" in which the equipment system is designed for floating and travel upon water.

Shockley 4-Layer Diode:

A PNPN semiconductor device in which contact is made only to the end regions of the device and which switches from a high forward resistance to a very low forward resistance as the applied voltage reaches a threshold value.

Short Circuit:

(Short)

A path of relatively low resistance between two points of different potential in a circuit. Presence of an unusually high load current through a device terminal, or of an unusually small potential drop across two device terminals.

Signal Processing:

A class of equipment which performs peripheral functions of conversions of electrical inputs. This class includes: Buffers, Converters, and Amplifiers.

Silicon:

(Si)

An elemental semiconductor of Atomic Number 14.

Silicon Bilateral Switch (SBS, DIAC):

A PNPN semiconductor device in which contact is made to only the end regions of the device and which exhibits a high and low conductivity state in both forward and reverse directions.

Silicon Carbide:

A dielectric compound of silicon from Group IV of the Periodic Table and carbon, also from Group IV.

Silicon Controlled Rectifier (SCR):

A PNPN semiconductor device in which contact is made to three of the four regions and which is thrown into conduction only when the gate potential is raised to a threshold level. Conduction is stopped only by removing the anode supply.

Silicon Controlled Switch (SCS):

A PNPN semiconductor device in which contact is made to all four regions which may be considered to be an ordinary transistor with a high degree of gain control.

Silicon Nitride:

A dielectric compound of silicon from Group IV of the Periodic Table and Nitrogen from Group V.

Silicon Oxide:

A dielectric compound of silicon from Group IV of the Periodic Table and Oxygen from Group VI.

Silk Screen:

Deposition of a thick film in the form of a slurry by forcing the slurry through openings in a fine mesh silk cloth.

Silver:

A metallic element with Atomic Number 47.

Single Ended (Linear Device Type (Asymmetrical Analog Network, Non-Differential Linear Device Type)):

A linear operational type in which the circuit components are intraconnected such that the network input and output are electrically asymmetric with respect to a neutral or ground point; not differential in operation (See "Differential (Linear Device Type)").

Slide (Document Format):

RAC Library document consists of a set of slides. (Requiring slide projector equipment for access).

Small Scale Integration (SSI):

The inclusion of at most 5 elemental circuit units on a single substrate or semiconductor chip.

Small Signal Transistor:

A bipolar transistor of small geometry designed especially to handle low level signals (i.e., $P < 1$ watt).

Solder:

A eutectic alloy of low melting point having good wetting properties with the metals to be joined.

Soldered:

"LEAD ATTACHMENT MODE" requiring use of a eutectic alloy of low melting point and having good wetting properties with the metals to be joined (solder).

Soldering Heat:

An environmental condition induced by application of heat to device terminals to simulate the use of solder in the lead attachment process.

Source:

In a field effect transistor the electrode through which carriers are injected into the conducting channel.

Spacecraft Environment:

Application environment associated with a satellite designed for launch into complete earth orbits or into extra-terrestrial orbits.

Special Active Devices, NOC:

Solid state devices which perform active functions other than those attributed to the common transistor types.

Special Function:

A not-otherwise-classified electronic function which cannot be considered to fall into any of the named specific function categories.

Special Military, Specification Reference:

Classification of a military specification or standard other than those organizationally grouped under "SPECIFICATION REFERENCE" in the current glossary.

Special, NOC (Not-Otherwise Classified Circuit Complexity):

A digital logic type or linear device type circuit with a function which cannot be categorized within any "CIRCUIT COMPLEXITY" descriptors of the current glossary.

"Special" networks in the digital functional category include: the A/D Converter, the D/A Converter, and Gate Expanders.

Linear functional categories of networks which are "Special" include the following. Of these, the voltage regulator has the largest variety of applications.

- Voltage Regulator
- Analog Switch
- Discriminator
- Phase Splitter
- Read Preamplifier
- Demodulator Chopper
- Converter
- D/A Switch
- Mixers

Special Reliability Study:

Testing conducted in connection with a special investigation of product quality or reliability, such as in "Process Improvement" and "Re-Design" studies.

SPECIFICATION REFERENCE:

(STANDARD/SPEC REFERENCE, SUPPORTING DOCUMENTATION)

Designation or classification of a relevant specification, standard, or documentation reference which is associated with "PART LEVEL DATA". (See "QUALITY ASSURANCE SPECIFICATIONS").

Specifications (Report Type):

Documents issued to serve as currently governing specifications and standards, or, to publicize tentative or recommended specifications and standards.

SPECIFICATIONS:

(STANDARDS, DRAWINGS)

Information serving as applicable specifications and standards, or, as tentative or recommended standards and specifications. Specifications are detailed descriptions of device characteristics and of the criteria applicable to determine conformity of devices with these descriptions. Standards establish engineering/technical limitations and applications for devices, materials, processes, designs, and practices.

Specific Information (Vendor Report Type):

An in-house report of the vendor for general distribution through his marketing or sales department. A report which contains detail performance data and application information on his product.

Spectrographic Analysis:

(Spectrum Analysis, Spectroscopic Evaluation, Gas Chromatography)

Evaluation involving the identification of chemical constituents through analysis of their light spectra.

SPONSORING ORGANIZATION (DOCUMENT DESCRIPTOR):

The client organization which supported the authorship of information contained in the RAC held document.

Sputtering:

Bombarding of the surface of a material with high energy ions so as to dislodge atoms of that material which travel to and deposit on another object.

Stacked Arrays:

"LEAD ATTACHMENT MODE" designed for interconnection with a matrix configuration of terminal fixtures.

STATISTICAL TOOLS:

(PROBABILITY INFERENCES)

Techniques for application of probabilistic mathematics for analyses of microelectronic reliability.

STEP STRESS MAXIMUM TEST TEMPERATURE:

(Ambient Temperature Condition, Step Stress)

The environmental condition of ambient thermal severity level, which is the maximum test severity applied in the "STEP STRESS TEST".

Step Stress Max. Test Temperature <21°C:

Thermal severity level is less than 21 degrees Centigrade.

Step Stress Max. Test Temperature 21°C to <102.5°C:

Thermal severity level is in the range from 21 degrees to less than 102.5 degrees Centigrade.

Step Stress Max. Test Temperature 102.5°C to <202.5°C:

Thermal severity level is in the range from 102.5 degrees to less than 202.5 degrees Centigrade.

Step Stress Max. Test Temperature 202.5°C to <302.5°C:

Thermal severity level is in the range from 202.5 degrees to less than 302.5 degrees Centigrade.

Step Stress Maximum Test Temperature >302.5°C:

Thermal severity level is in the range greater than or equal to 302.5 degrees Centigrade.

STEP STRESS TEST:

(FAILURE ACCELERATION STEP-STRESS TEST)

An "Operating Test(s)", environmental test, or a test combination of these stress domains, which is conducted in accordance with "Step Stress Testing" procedures. (See "Step Stress Testing (TEST TECHNIQUES & PROCEDURES)").

STEP STRESS TEST DOMAIN:

The specific nature of the externally applied test stress (es) of the "STEP STRESS TEST".

Step Stress Testing:

(Failure Acceleration, Step-Stress)

Testing similar to "Accelerated Testing", except that discrete levels of stress severity are increased stepwise until failure of the majority of specimens in the sample. Generally, severity levels are applied sequentially for periods of equal duration to a given sample. However, a variant technique concurrently subjects each of several sample groups to one of the chosen severity level steps. The latter procedure is known as parallel step stressing. (See "Accelerated Testing").

Stitch TC Bonding:

A variation of the wedge bonding technique in which a capillary tube, vertically oriented to the substrate, feeds the wire to be bonded. A 90° bend is formed on the end of the wire so that the edge of the capillary tube can supply the compressive force for bonding. Instead of severing the wire after bonding to a tab on the semiconductor device, the capillary is moved to a new tab where another 90° bend is formed in the still continuous wire and another bond is made. The sequence continues as long as desired, resembling a stitching process.

Storage Element (Memory):

A digital network, which may consist of an array of registers, used for computer memory or storage and transfer of logic information.

STORAGE LIFE TEST:

(HIGH TEMPERATURE LIFE TEST)

"Thermal Stress Testing" in which a steady-state stress domain of temperature is the ambient environment. (See "Thermal Stress Testing (TEST TECHNIQUES AND PROCEDURES)").

STORAGE LIFE TEST TEMPERATURE:

The environmental test stress in terms of the ambient thermal severity level of the "STORAGE LIFE TEST".

Storage Life Test Temperature <21°C:

Thermal severity level is less than 21 degrees Centigrade.

Storage Life Test Temperature 21°C to <102.5°C:

Thermal severity level is in the range from 21 degrees to less than 102.5 degrees Centigrade.

Storage Life Test Temperature 102.5°C to <152.5°C:

Thermal severity level is in the range from 102.5 degrees to less than 152.5 degrees Centigrade.

Storage Life Test Temperature 152.5°C to <202.5°C:

Thermal severity level is in the range from 152.5 degrees to less than 202.5 degrees Centigrade.

Storage Life Test Temperature 202.5°C to <302.5°C:

Thermal severity level is in the range from 202.5 degrees to less than 302.5 degrees Centigrade.

Storage Life Test Temperature >302.5°C:

Thermal severity level is in the range greater than or equal to 302.5 degrees Centigrade.

Storage Time:

In a transistor, charges injected by the emitter into the base are "stored" for a finite time when the transistor's emitter-base junction is reverse biased until the carriers can be swept out by the electric field.

Sub-Optical Electromagnetic Energization (Non-IR):

(Microwave Transmission Testing)

Evaluation of device or device element through observation of its transmission properties for electromagnetic waves in the frequency range below infrared and above the normal frequency of device operation.

Substrate Materials:

Materials used as support for circuit elements and their interconnections.

Silicon	(See earlier definitions per structured term list)
Germanium	(See earlier definitions per structured term list)

Superconducting Storage Element:

A digital memory element based on the storage of magnetic flux by a closed superconducting loop circuit.

Superconductivity:

In certain metals, alloys, and intermetallic compounds, the appearance of perfect electrical conductivity and perfect diamagnetism at temperatures near absolute zero.

SURFACE PASSIVATION:

Protection of the wafer surface from contaminants which may be found in its environment.

Surface Protection:

Materials used to isolate the surface of microelectronic devices and circuits from contaminants in its environments.

Survey and Review (Report Type):

A report which summarizes the results of a survey type study or a fact-gathering activity.

System Application:

Design approach primarily from the aspect of system requirements. (See "SYSTEMS EFFECTIVENESS: OTHER, NCC").

SYSTEMS EFFECTIVENESS:

An engineering approach which seeks to determine optimum means of implementing a system function, with degrees of freedom in the selection of actual subsystems and devices to be applied. A key objective of this approach is to minimize the total cost of system acquisition and operation.

- T -

Tantalum:

A metallic element of Atomic Number 73.

Tantalum Oxide:

A dielectric compound of tantalum from Group V of the Periodic Table and Oxygen from Group VI.

Technical Report (Report Type):

A periodic or singly issued report which documents study or technical status of a specific and currently applicable activity. A report oriented toward applied technology.

Temperature Cycling:

(Seal Strain)

A thermal stress environment of periodic variation of temperature, such as under normal conditions of service. (See "Failure Stress Domain, Thermal Shock").

Temperature, Intermittent Stress Domain:

(Thermal Stress)

The ambient thermal energy to which test specimen is exposed.

Terminals:

The ends of the package leads inside the case of a solid state device to which connection is made from the device elements.

Terminal Strength:

(Lead Pull)

Response capability of the package terminals to a mechanical force of tension.

Test Data (Report Type):

Quantitative documentation of testing activity is major purpose of report, as ascertained by at least 75 percent of the informational content of RAC held document.

Test Equipment/Procedures Approved by Non-Resident Source-Sponsor Representative (Data Validation):

Test results obtained with DATA VALIDATION corresponding to "Facility Approved by Source-Sponsor Representative" and "Procedure Approved by Source Sponsor". However, the agent of the SPONSORING ORGANIZATION was a non-resident inspector at the test facility.

Testing:

(LSI Device Element Selection, Discretionary Wiring, Wafer Probing)

Electrical probing of wafer elements and provisions for selection of "good" device elements for intraconnection in large scale integrated (LSI) circuits. (See "Failure Environment, Product Inspection").

Test Pattern:

(Design Probes, Processing Probes)

The design and utilization of control test patterns of the fabrication processes to usefully modify design of the microelectronic device or device element. (See "Modification; Circuit/Device Implementation" and "Use of Test Patterns (PROCESS CONTROL TECHNIQUES)").

Test Reports:

(Special Test Reports)

Documented results of inspection at the part level or at the equipment level, generally in connection with laboratory investigations. However, Field Test Reports are also included by this descriptor.

TEST RESULTS:

(TEST DATA)

Quantitative information or conclusions obtained from testing and inspection procedures.

TEST TECHNIQUES AND PROCEDURES:

(METHODOLOGY OF RELIABILITY MONITORING, QUALITY CONFORMANCE INSPECTION METHODS)

Techniques and procedure for electrical, environmental and physical evaluation of devices (or device elements), with relevance to reliability demonstration and assessment. Pertinent measurement techniques and failure criteria are included.

Test Techniques and Procedures, NOC:

(Not-Otherwise Classified Test Techniques and Procedures)

Reliability test techniques and procedures which cannot be defined by any descriptors of the current glossary. (See "TEST TECHNIQUES AND PROCEDURES").

TEST TYPE:

(INSPECTION CATEGORY, TEST ORIENTATION)

Nature of the test in terms of its purpose or the quality/reliability objectives towards which inspection is directed.

Thermal Conduction:

The transport of heat energy through a medium.

Thermal Conductivity:

A measure of the ability of a material to conduct heat energy.

Thermal Diffusivity:

A ratio of thermal conductivity to heat capacity used to determine the response of a material to transient heat flow.

Thermal Environments, Accelerated Life Test Domain:

(Temperature, Low Temperature, Low Ambients)

Stress domain consists of an environment as included by the descriptor: "Thermal Stress Testing" but with temperature cycled between two extremes or constant application of a temperature below room ambient. (See "Thermal Stress Testing (TEST TECHNIQUES AND PROCEDURES)" and "High Temperature").

Thermal Environments, Step-Stress Test Domain:

(Temperature, Low Temperature, Low Ambients)

Stress domain consists of an environment as included by the descriptor: "Thermal Stress Testing" but with the stress cyclically transferred between two temperature extremes. A stress step increase may either extend the temperature extremes or the number of cycles.

Thermal Shock:

(Seal Strain)

Sudden or abrupt exposure to extreme changes in temperature. (See "Failure Stress Domain, Thermal Shock").

Thermal Stress Testing:

(Elevated Temperature Testing, Temperature Stressing)

Environmental testing in which extreme severity levels of temperature or temperature changes are imposed on the device. "Thermal Stress Testing" includes: high temperature life (storage life testing), low temperature storage, temperature cycling, and thermal shock. (See "Failure Stress Domain, Thermal Shock").

Thermo-Compression Bonding:

(TC Bonding)

Bonding of wires to a base metal by heating the structure to the softening point (not the melting point) of the wire material and applying a compressive force to cause the wire material and the base metal to plastically flow together.

Thermoelectric Effect:

The production of electrical energy by the application of thermal energy to the junction between two dissimilar metals, or semiconductors; the converse of this (also known as the Peltier effect).

Thick Film:

A layer of a certain material generally considered to be greater than one micron thick.

Thick Film, Pure IC (Passive Substrate IC, Thick Film):

A film integrated circuit whose circuit elements are formed of films which are applied through processes other than vacuum deposition. (See "Film IC", and "Thick Film: DEPOSITION").

Thin Film:

A layer of a certain material generally considered to be less than one micron thick.

Thin Film, Pure IC (TFIC; Passive Substrate IC, Thin Film):

A film integrated circuit whose circuit elements are formed of films of such thicknesses as to yield electrical properties which are strongly surface-state dependent (thin films $\leq$ 10,000 angstroms, thick). There is no technical consensus on the limiting thickness dimension for thin films. A working definition of a thin films is a film which is applied through a vacuum-deposition process. (See "Film IC", and "Thin Film: DEPOSITION").

Tin:

A metallic element of Atomic Number 50.

Titanium Dioxide:

A dielectric compound of Titanium from Group IV of the Periodic Table and Oxygen from Group VI.

Tolerance; Function/Circuit Design & Optimization:

Allowable variations in the performances of device elements and in the microelectronic device. Considerations of the relationships among such variations.

Trade-Offs:

(Engineering Trade-Offs)

Engineering approaches which emphasize the design/development compromises and compensating features available for microelectronic functions and circuits.

Transconductance:

The amount of current flowing in the output circuit of an active device as a result of a certain input voltage.

Transistor(s):

A three-terminal solid state electronic device which is capable of providing power gain to an electronic circuit.

TRIAC:

A three-layer semiconductor device which can be switched into conduction in either the forward or reverse directions. Equivalent to two reverse-parallel connected SCR's.

TTL (Digital Logic Type (Transistor-Transistor Logic, T^2L, TCL)):

A digital logic circuit configuration which is very similar to DTL and wherein the gates are characterized by the use of a multiple-emitter transistor in place of the DTL input diodes. Generally, this logic type includes types such as TRTL, HLTTL, HLT^2L, SUHL I SUHL II and MTTL. (See "Digital Logic Type" and "DTL").

- U -

Ultrasonic Bonding:

A welding of two materials to be bonded (usually a wire and metal tab on a device) using ultrasonic energy.

Ultrasonic Inspection:

(Supersonic Examination, Acoustic Noise Evaluation)

Device or device element inspection with use of sound waves of frequencies above the audio range.

Unclassified (Report Security Classification):

No restrictions imposed on access to informational content of RAC held document.

Unijunction Transistor:

A three-terminal semiconductor device in which an n-type bar of semiconductor has ohmic contacts placed at each end and a metallic rectifying contact placed between them along the bar. Current injected by the emitter creates a negative resistance characteristic in the device.

Unspecified Environment:

Application environment associated with an unknown category of system application.

Unspecified Equipment Class:

An unknown or unspecified class of equipment.

Use of Test Patterns:

Special patterns, containing single devices or components, etc., which are placed on a wafer at strategic spots of the array of devices being fabricated, which enable the measurement of specific device or material properties over which control must be maintained during processing.

User Procurement, Specification Reference:

Classification of any procurement specification or standard issued by a non governmental agency.

User Proprietary Screening and Burn-In Specs:

(User Product Conditioning Specs)

User's proprietary specifications of the combinations of tests designed to identify specimens with quality defects, and specifications of tests for stabilizing the devices' characteristics.

Vacuum Deposition:

The evaporation from a source and condensation on a substrate, in vacuum, of molecules of a certain material to form a thin film.

VALUE ENGINEERING:

An engineering approach which seeks to minimize production cost of an item, while maintaining a specified standard of quality.

Vapor Deposition:

Decomposition of a vapor containing the desired material and condensation of that material into a thin film.

Variables Analysis Summaries:

Data reduced or processed through variables analysis procedures. (See "Variables Data Analysis: STATISTICAL TOOLS"). Test results such as the following are included within the scope of this descriptor:

Parameter Correlation

Parameter Drift vs. Stress

Parameter Stability vs. Stress

Parameter Distribution Drift

Selected Sample Drift History

VENDOR APPLICATION NOTES:

A report containing detail information regarding considerations to place the product into service. Generally, presents relevant operational data as well as applications information.

Vendor QA Plans and Specs:

(Performance Specs, Technical Data Sheets)

Quality assurance (QA) commitments and specifications of device qualifications by the product vendor. Vendor specifications on detailed device characteristics are included in the scope of this descriptor.

Vendor (Report Type):

A "General Catalog" and/or "Specific Information" type of publication for advertisement of a vendor's product.

Vendor Screening and Burn-In Specs:

(Vendor Product Conditioning Specs)

Vendor generated specifications of the combinations of tests designed to identify specimens with quality defects (those devices likely to exhibit early failures), and specifications of tests for stabilizing the devices' characteristics.

Vendor, Specification Reference:

Classification of a vendor issued specification or standard.

Vibration:

A mechanical stress environment of cyclic variation in directed motion, with periodic or random frequency spectrum. (See "Failure Stress Domain, Vibration").

Vibration, Fatigue:

(Shake Test)

A "vibration" environmental condition of constant periodic frequency, of such characteristics (usually at the natural mechanical frequency of key device elements) to determine early wear-out response of device. (See "Vibration").

Vibration, Random:

(Mechanical Noise Vibration)

A "vibration" environmental condition of non-periodic frequency and changes in frequency. Exposure to a mechanical frequency noise environment. (See "Vibration").

Vibration, Variable Frequency:

A "vibration" environmental stress of continuous or discrete sweeping through various mechanical frequencies. (See "Vibration").

Video Amp (Wideband Amplifier, Broad Band Amplifier):

This index of "CIRCUIT COMPLEXITY" includes single-ended amplifiers with a frequency response extending from d-c to several hundred megahertz.

Visual Inspection:

(Manual Examination)

Evaluation of device or device element through eyesight and without instrument aid.

Voltage, Accelerated Life Test Domain:

(Electric Potential Difference)

Accelerated life test where the stress domain of interest is electric potential applied to circuit of test specimen.

Voltage, Intermittent Stress Domain:

(Electric Potential Difference)

The electric potential applied to circuit of test specimen.

Voltage Regulator:

A linear electronic circuit designed especially for sensing and regulating the output voltage of a power supply.

Voltage, Step-Stress Test Domain:

(Electric Potential Difference)

Step stress test where the stepped domain is the electric potential applied to circuit of test specimen.

- W -

Wafer Cutting:

Slicing semiconductor crystals into thin preferentially oriented discs.

Wafer Etching:

Selective removal of material from the wafer surface to expose imperfections in the crystal.

Wafer Lapping:

Abrasion smoothing of the wafer surface using a rotary abrasion mill and a liquid-suspended lapping compound.

Wafer Polishing:

Production of a mirror smooth surface by chemically or mechanically removing material from the surface.

WAFER PREPARATION:

The processing of single crystal semiconductor materials into wafers suitable for device fabrication.

Washing:

Cleaning of the completed microelectronic device wafer to remove all contaminating materials.

Washing:

Cleaning the surface in deionized water to remove residue chemicals and other contaminants.

Wedge TC Bonding:

Thermo-compression bonding in which the compressive bonding force is applied by a wedge-shaped tool.

Weibull Analysis:

Statistical analysis using the Weibull distribution as the probability-density function. The standard Weibull distribution is described with three parameters. This distribution is quite flexible and may describe data of devices exhibiting increasing, constant, decreasing or any combination of failure rate with time.

Welded:

"LEAD ATTACHMENT MODE" requiring use of a technique such as cold welding for making connection. (See "Cold Welding").

Wire Material:

The metallic material used to form the wires which connect circuits and devices to each other and to their package.

Work Function:

The work required to remove a charge from the surface of a material into vacuum.

Work Hardening:

The creation of imperfections in a metal by physically stressing it such that the metal becomes hard and brittle, the imperfections acting as impurities in the crystal lattice.

Workmanship Defects:

(Human Error)

Quality defect causes due to deviation from required skills during the manual steps of device fabrication.

Workmanship Defects, NOC:

(Non-Classified Human Error)

Workmanship defect causes which cannot be defined by any descriptors of the current glossary.

X-Ray Evaluation:

(X-Ray Inspection, Fluoroscopic Examination)

Evaluation with use of x-ray imaging of the device or device element.

- Y -

Yield:

A measure of the percentage of usable microelectronic device of all those processed on a single wafer.

Youngs Modulus:

The degree of tensile stress required to produce a unit linear strain in a material.

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13. ABSTRACT

The Reliability Analysis Center is being established as a Department of Defense Data Center for the collection, analysis, and dissemination of technical information on microelectronic device reliability. Its objective is to establish a basis for correlating reliability factors with device materials, design, fabrication, quality assurance and application factors. This report describes the development, implementation, and present status of a data collection and file entry effort supplemented by a Termetrex data retrieval system. Detailed operating procedures, periodic outputs, and user services from the Center are described in detail.

Future plans call for expansion of RAC into hybrid microelectronics and discrete semiconductors used in military weapons and communications systems.

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