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RADC-TR-66-792
Final Report

RELIABILITY TESTING AND PREDICTION TECHNIQUES FOR HIGH POWER SILICON TRANSISTORS

D. R. Fewer
J. R. Tomlinson

Texas Instruments, Inc.

TECHNICAL REPORT NO. RADC-TR-66-792
June 1967

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FOREWORD

This final report was prepared by D. R. Fewer and J. R. Tomlinson of Texas Instruments, Incorporated, P. O. Box 5012, Dallas, Texas, under Contract AF30(602)-3727, project number 5519, task number 551902. Secondary report number is 03-66-115, reporting period covered was from 19 April 1965 to 19 October 1966. RADC project engineer is Regis C. Hilow (EMERR).

This technical report has been reviewed by the Foreign Disclosure Policy Office (EMLI). It is not releasable to the Clearinghouse for Federal Scientific and Technical Information because it contains information embargoed from release to Sino-Soviet Bloc Countries by AFR400-10, "Strategic Trade Control Program."

This report has been reviewed and is approved.

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ABSTRACT

Work performed under this contract is divided into two main parts: (1) a Test and Data Analysis Program designed to produce a method for reliability screening; and (2) a Physics of Failure Program on fundamental mechanisms causing device degradation. The test program was divided into three parts, Preliminary, Main and Verification Test Programs. Results of each test program are discussed. Accelerated test results and comparison of fixed stress and step stress results are presented. A nondestructive screening procedure was developed and is contained in this report. Three computer programs; SERF, LINDA 1 and LINDA 2 were developed to assist in the development of the nondestructive screening procedure.

The Physics of Failure Program consisted of studies of surfaces and oxides, noise, thermal effects and second breakdown. Extensive analyses of failures were also carried out. Surface studies included the development and analysis of techniques for the production of metal-oxide-silicon (MOS) systems that are electrically and thermally stable. This work is summarized in another volume of the final report (RADC-TR66-776). Thermal studies include results of actual temperature measurements of operating transistors using an infrared (IR) microradiometer. Results of electrical and thermal techniques are compared as a tool for measuring thermal resistance. Models to calculate the current and temperature distributions in operating power transistors give results which are in agreement with experimental data. The second breakdown studies include a discussion of a model for thermal breakdown.

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EVALUATION

The basic objectives of this program were to develop and verify nondestructive reliability screening and accelerated testing techniques for a general class of silicon planar power transistors.

This was accomplished through a detailed test program and physics of failure study of the 2N2880 and 2N3998 Transistors. The following significant accomplishments resulted from this effort:

a. A study of passivating oxides resulted in two orders of magnitude improvement in oxide stability as measured by MOS transistors under voltage and temperature stress. The results of this work are reported in a separate report entitled "Surface Studies," RADC-TR-66-776.

b. A nondestructive reliability screening procedure for small stud silicon planar epitaxial transistors has been developed. Included in this procedure are criteria for accepting and rejecting a part on thermal impedance. The cost of each screen is also treated in detail.

c. Acceleration factors for predicting the reliability of the class of devices, mentioned in b. above, are presented for various stresses.

d. A comprehensive thermal study of the two test vehicles was conducted. Results of this study have extended the knowledge of thermal behavior of transistors and are presented in sufficient detail for practical use by the industry in the reliable design of power devices.

e. Noise studies indicated that this parameter is not a good preindicator of failure.

f. A computer program, SERF, was developed to aid in development of a screen test. This program can utilized to determine sensitive preindications of failure for any component. That is, it is not restricted in use to the test vehicle in this effort.

g. Areas that need further investigation are defined along with their potential payoffs.

In summary, the most important reliability parameter of power devices that showed up in this study is that of thermal impedance which is called for in the screening procedure. In order to obtain good screening effectiveness, the test conditions for measurement of this parameter were determined to be higher than normally used collector-to-emitter voltage at rated power. Presently, this parameter is costly to measure on a 100% basis except by the method (ZOT) presented for the first time by Texas Instruments in this report.

The screening procedure that resulted from this study was directly incorporated into the TX specification for the 2N3996-3998 series of power devices and has aided in the preparation of several other Air Force Hi-Rel specifications.

REGIS C. HILOW
Reliability Engineering Section
Reliability Branch

SECTION I

INTRODUCTION

1. SUMMARY OF REPORTS

This report is one of the two volumes of the final report on this United States Air Force Contract No. AF30(602)-3727, prepared for Air Force Systems Command, Research and Technology Division, Rome Air Development Center, Griffiss Air Force Base, Rome, New York. This volume covers the work performed during the calendar period 19 April 1965 through 19 October 1966, under the test portion of the contract, as well as three of the four physics of failure activities, namely: second breakdown studies, noise studies and thermal physics. Surface studies, the other physics of failure activity, are the subject for the other volume of the final report under this contract. [1]* It also covers the calendar period 19 April 1965 through 19 October 1966 and was prepared at the same time as this volume.

There were two interim reports on this contract. The first (interim) Technical Documentary Report, RADC TR-65-464, was completed in November 1965. It covered the reporting period from 19 April 1965 to 19 October 1965. The second Technical Documentary Report, RADC-TR-66-346 was completed in May 1966. It covered the reporting period from 19 October 1965 to April 1966.

2. PROGRAM RESULTS

Work performed under this contract is divided into two main parts: (1) a test and data analysis program designed to produce a method for screening or predicting failures in silicon power devices, and (2) a physics of failure program on fundamental mechanisms causing device degradation. Section II includes a brief review of the program to date with appropriate references to prior interim reports for detailed information. [2, 3] Also in Section II is a brief description of the general contents in each of the other sections.

a. Test and Data Analysis Program

The test programs conducted during this contract are presented in detail along with the methods used in determining the stresses to be applied. In addition to

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* See References.

the matrix test and step stress tests required, additional pretreatment and 100 percent mechanical screen tests were included. Parallel to this effort evaluation experiments or "specials" were conducted using devices which had received special treatment and/or special processing. This approach permitted integration of some aspects of the physics of failure activity with the test program.

The pretreatment stresses in the Main Test Program were used to see if device behavior during low stress was indicative of future failure under high stress. More specifically, did device behavior under one type of pretreatment stress such as reverse bias preindicate later device failure under a different kind of high stress such as temperature storage? Or was the prediction of failures on a particular high stress only possible from behavior during the same kind of pretreatment stress? It has been found that predicting later failures during temperature storage and power operating stress was most successful when the prediction was done on the basis of parameter changes during power operating pretreatment. No pretreatment seemed to enhance prediction of device failure under reverse bias stress.

The computer program SERF developed for this test program is of value in isolating the preindicators of failure. It is based on the assumption that devices which are less reliable have at least one parameter whose value is higher or lower than the rest of the devices. The term parameter here may refer to delta (Δ) and percent (%) changes of a parameter. The program examines each parameter of each device and selects that parameter and that parameter level which optimizes the screening efficiency, e or e*,

$$e = \frac{\% \text{ failures removed}}{\% \text{ population removed}}$$

or

$$e^* = 0.5 + 0.5\,(F_f - F_g)$$

where

F_f = Fraction of total failures removed

F_g = Fraction of total good devices removed

Parameter level is that value of a particular parameter which is used for screening, i.e., all devices which have that particular parameter value below or above this level are eliminated.

The cost of screening may be used as input for the SERF program in the following manner. The number of screening passes or, expressed another way, the number of screening parameters will be a function of the cost of measuring those parameters. If this is very expensive, for example, the minimum number of screening passes would be allowed. Secondly, if it is more expensive to mistakenly allow a bad device to remain in the sample than to mistakenly remove a good device, the percentage of good devices which are allowed to be removed by the screening procedure can be increased. Values actually found for e ranged from 1.07 to 94. In chance screening e = 1. Values from 0.48 to 1.00 were found for e*.

The best preindicator of failure and therefore the screening parameter is not simply one parameter. Rather several parameters evolve as preindicators of failure depending on the test, number of parameters, order sequence of parameters and screening efficiency. However five parameters (also includes delta and percent change of these parameters) I_{EBO} (5 V), I_{EBO} (8 V), h_{FE} (5 mA), h_{FE} (1 A) and $V_{BE(sat)}$ were found to be the parameter most frequently included in the SERF screening procedures for the Main Test Program.

The primary failing parameters on all tests in the Main Test Program were h_{FE} (5 mA), I_{CEO} (30 V) and I_{CEO} (70 V). Analysis of devices which failed due to degradation of these parameters revealed the presence of temperature voltage induced inversion (TVI), surface contamination and presence of an unknown volatile encapsulated within the device.

In addition to the development of the SERF Program, two other computer programs LINDA 1 and LINDA 2 based on linear discriminant analysis[4] were adapted for use in this contract. The method results in the construction of a linear combination of parameter values, a linear discriminant function, which may contain as many parameters as desired, and also a critical value for the linear discriminant function which allows the devices to be separated into two categories, satisfactory or unsatisfactory. The parameter values of devices from a population similar to the population used to construct the linear discriminant function are measured and the parameter values substituted in the linear discriminant function. Those devices which exceed the critical value are placed in the appropriate class, i.e., satisfactory or unsatisfactory. The ratio of the cost of misclassification, i.e., the cost of classifying a satisfactory device as unsatisfactory or vice versa, is actually used as input data for LINDA 1, the basic linear discriminant analysis computer program, in determining the classification criterion. The computer program SERF and the technique for screening are presented in sufficient detail for other investigators to repeat the work on other device families. The other two computer programs, LINDA 1 and LINDA 2, are described in this report although relatively little use was made of them.

A nondestructive screening procedure for silicon planar epitaxial power transistors using the computer program SERF was developed under this contract. It consists of two phases. The screen selection phase (phase 1) is used to determine the parameters and parameter levels to be used in screening. The screen application phase or phase 2 consists of routinely screening the devices using the information obtained in phase 1.

A sample from a lot is sequentially processed through the steps outlined in the first column of Table 1 (phase 1).

The 15 electrical parameters of the device (Table F-1) would be measured at the times indicated in Table 1. The initial readings would not be used for screening, but if anomalies in the data were later detected, a knowledge of the device behavior prior to the constant acceleration screen, the hermetic seal tests and the thermal resistance measurements would be important. The electrical parameters are re-read prior to and after burn-in. The devices are then subjected to the high stress life tests. The devices which fail under the high stress testing are noted and this information used as input to the computer along with the electrical measurements before and after power burn-in. The computer program SERF will isolate the preindicator of failure and the appropriate level of screening. Finally, routine screening of devices may be done, following the procedure in Column 2 of Table 1 (phase 2). Although it appears that the screening results obtained for one device family cannot yet be generalized for all silicon power devices, the technique used to obtain the results can be applied to almost any semiconductor device. However, success in this type of screening will depend on whether or not the early parameter behavior of the good devices differs from that of the bad devices, i.e., those which fail early.

The estimated costs for performing phase 1 and phase 2 of the proposed screening procedure in Table 1 are in the range of $14 to $28.10 per device and $5.40 to $11.80 per device respectively.

The Arrhenius equation has been used in interpreting the test data. Actually, a generalized Arrhenius equation is used, but one in which the function of nonthermal stress is a constant, as for example, the voltage was in the power operating tests of the Main Test Program. It was thought that the refinements possible using the Eyring equation were not commensurate with the effort in using the more complicated equation. At least one investigator[4] has doubted the value of using the Eyring equation in normal testing situations.

In the Main Test Program an activation energy of 1.0 eV was calculated from the temperature storage test results for temperatures in the range 200 - 250°C. The failure rate was estimated to be about 10^{-4} %/1000 hours. A tentative activation energy of 2.2 eV has been found for temperatures in the range 250°C to 300°C. Temperature storage test results of the Verification Test Program were comparable with those of the Main Test Program.

Table 1. Proposed Screening Procedure for Small Stud Silicon Planar Epitaxial Transistors

Phase 1 Screen Selection	Phase 2 Screen Application	Details
1. Read electrical parameters	Read electrical parameters	Table F-1, Appendix F
2. Constant acceleration	Constant acceleration	10,000 G - X_1 and Y_1 planes - Stress time ≤ 1 min/plane
3. Hermeticity		
a. Hermetic seal (fine-leak) test	Hermetic seal (fine-leak) test	Using appropriate bomb times to arrive at a leak rate of 5×10^{-8} cc/sec on Helium or 5×10^{-9} cc/sec on Krypton leak test equipment.
b. Gross-leak test (liquid immersion)	Gross-leak test (liquid immersion)	Noncorrosive ethylene glycol - 150°C 15 sec. minimum -- Devices that bubble are to be removed from lot.
4. Thermal resistance	Thermal resistance	ΔV_{CBF} Method (ZOT), V_{CE} = 20 V and 30 W or by the V_{CBF} Method (Appendix B), Devices with $\theta_{J-C} \geq 3°C/W$ to be removed from lot.
5. Read electrical parameters	Read electrical parameters	Table F-1, Appendix F
6. Power burn-in	Power burn-in	96 Hr, V_{CE} = 20 V, P_C = 30 W, T_C = 100°C
7. Read electrical parameters	Read electrical parameters	Table F-1, Appendix F
8. Life Test	----------	
a. Temperature storage		T_C = 350°C, 1000 hr.
b. Power operating		T_C = 100°C, V_{CE} = 20 V, P_C = 50 W, 1000 hr.
c. Reverse bias		T_C = 200°C, V_{CB} = 100 V, V_{EB} = 7 V, 1000 hr.
9. Computer analysis	----------	Use computer program SERF to obtain preindicator of failures.
----------	Screen	Use screening procedure developed in the computer analysis of phase 1.

There appears to be a number of failure mechanisms operative on the temperature storage tests. There is, for example, a distinct change in the failure rate around 250 - 275°C, indicating different mechanisms.

For the power operating tests of the Main Test Program an activation energy of 1.5 eV was found. The failure rate for the 15 W power operating test, having a case temperature of 50°C, was about 2×10^{-3} %/1000 hours.

Thermal resistance is defined by the following equation:

$$\theta_{J-C} = \frac{T_J - T_C}{P} \tag{1}$$

where

T_J = junction temperature

T_C = case temperature

P = power dissipated

The difficulty in making this measurement has been in determining the junction temperature (T_J). Several techniques for obtaining T_J are used in the semiconductor industry, but it is not known which gives the best approximation and therefore the most meaningful value of thermal resistance. To shed some light on this problem, θ_{J-C} was measured by three different steady state methods, (V_{BE}, V_{CBF} and h_{FE}), by a pulse technique ΔV_{CBF} (ZOT) method and by an infrared (IR) microradiometer method on the same devices. It was found that the θ_{J-C} values obtained by the (ZOT) method at $V_{CE} = 20$ V more nearly approximated the θ_{J-C} values of the device as determined by the IR method. It was further observed that the θ_{J-C} of a device could vary widely; i.e., from 2°C/W, to 8° C/W, depending on both the method and conditions used in making the measurement.

A study was made in the Verification Test Program to determine how effectively θ_{J-C} measurements indicated the effective device temperature. Thermal resistance (θ_{J-C}) values obtained by the 20 V and 15 V ZOT method were used in Equation (1) to compute T_J (20 V) and T_J (15 V) respectively for all devices on the power operating tests. The devices were then ordered according to increasing T_J (20 V) and classified into two groups, those with high T_J (20 V) and those with low T_J (20 V) values. The cumulative percent failure curves were then plotted for both

these groups, using the median T_J (20 V) value of each group as the stress temperature. All this was also done for T_J (15 V). The resulting cumulative percent failure curves for the four groups correlated well with median T_J values and also with the 300°C storage life test of the Verification Test Program.

b. Physics of Failure Program

Work performed in surface studies describes techniques for obtaining clean, stable metal-oxide-silicon (MOS) samples. Sufficient description has been made to allow other investigators to repeat the work. Also the work provides manufacturers of semiconductor devices with some basic analysis of the contamination variables attendant on their processing. Hence, some techniques for clean oxide formation have been extended to the industry at large. Additionally, the results of surface studies, presented elsewhere, [1] suggest significant variables which must be controlled in the manufacture of devices to obtain maximum built-in reliability.

The results of noise studies showed that noise-figure measurements prior to stress are not a good predictor of failure. These results together with a preliminary study of transistor noise waveform characteristics are presented in the first interim report. [2]

The IR microradiometer was the primary instrument employed in the thermal studies work. This instrument made it possible to study the operating temperature of the silicon power transistors with very little disturbance of their performance. A result of this work is the determination of the temperature distribution for a transistor which shows that the peak operating temperature is much higher than was previously thought. The maximum operating temperature for silicon devices was believed to be a little above 200°C but it is now known that silicon devices do operate above 300°C, although the maximum operating temperature still has not been established because of other limitations of the device construction. Many devices have been operated with their surface temperature above 300°C and they have performed very well. With the use of the IR microradiometer, some of the limitations of the various methods for measuring junction temperature (T_J) are now established. Thus much better correlation of thermal impedance (θ_{J-C}) with device failure is possible. A more realistic use can now be made of the present methods for measuring thermal impedance, and new methods can be sought to improve its usefulness. The values used for the thermal resistance of a device are extremely dependent on the method and conditions used in making the measurement. Mathematical models were generated to study the internal operation of a transistor and are helpful in understanding its thermal behavior. The concentration of the current along the edge of the emitter fingers can now be computed and is used to calculate the heat dissipated across the emitter. By combining this capability with a solution of the heat transfer problem for transistors, a temperature profile across the surface of a transistor can be computed. Within the assumptions

used, the present results agree very well with experimentation and help support the interpretation of experimental data. With the aid of these models, the results on the particular transistor which has been under study can be extended to other transistors. Results of thermal studies can be summarized as:

1) Infrared microradiometer techniques were developed to obtain quantitative surface temperature profiles.

2) Temperature profiles were used to obtain isothermal contour maps of the power transistor during operation.

3) Hot-spot formation was demonstrated using isothermal maps.

4) Areas of self destruction in a transistor were correlated to location of hot spot generation.

5) Current distribution within operating transistors was calculated.

6) Heat generation within transistors was determined from its current distribution.

7) A simplified heat transfer model was developed for a transistor using realistic heat generation.

8) Good quantitative agreement was obtained between computed and observed temperature profiles of a transistor.

9) Electrical methods for measuring thermal impedance were evaluated.

10) Thermal impedance measurements were interpreted.

11) Results of thermal studies were used to understand the operation of transistors and to interpret results from reliability test programs.

This thermal study has extended the knowledge of the thermal behavior of transistors and has been presented in sufficient detail to help manufacturers design and screen devices for improved reliability. However, much work remains to be done in order to completely understand this behavior. Once this understanding is complete enough, transistors can be designed to minimize the influence of temperature or to use this

dependence for a beneficial purpose. More emphasis must be placed on the understanding and use of the thermal properties of semiconductor devices in order to achieve a maximum utilization of device capabilities.

The model developed in the second (thermal) breakdown studies has led to a fuller understanding of the factors influencing hot spot formation in devices. The processes limiting hot spot formation are discussed and it is shown that the distributed collector resistance is important in controlling the point at which hot spots enter breakdown. This information is presented in sufficient detail to allow other investigators to repeat the work. In addition device designers in the semiconductor industry are provided with information to improve the resistance of the device to hot spot formation and thereby improve reliability.

3. PAPERS PUBLISHED

Ten papers have been presented on the work which was primarily funded by RADC under Contract AF30(602)-3727. These papers are listed chronologically.

1. Peterman, David A., "Thermophysics of High-Power Silicon Transistors," 1965 Physics of Failure in Electronics Symposium (November, 1965). Published in Volume 4 of Physics of Failure in Electronics, Defense Documentation Center, Cameron Station, Alexandria, Virginia.

2. Carlson, H.G., Fuller, C.R., and Meyer, D.E., "Effects of Phosphorus on Sodium Distributions in Oxides," Las Vegas, Nevada (1965).

3. Carlson, H.G., Fuller, C.R., and Osborne, J.F., "Effects of Phosphorus Diffusion on Sodium Concentration Profiles in Thermally Grown Silicon-dioxide Films," Buffalo, New York (October, 1965).

4. Carlson, H.G., Brown, G.A., Fuller, C.R., and Osborne, J.F., "Effects of Phosphorus Diffusion in Thermal Oxides on the Elevated Temperature Stability of MOS Structures," 1965 Physics of Failure in Electronics Symposium (November, 1965). Published in Volume 4 of Physics of Failure in Electronics, Defense Documentation Center, Cameron Station, Alexandria, Virginia.

5. Meyer, D. E., " Retention of HF on Surfaces Common to Silicon Devices - II," Cleveland, Ohio (May, 1966).

6. Plumlee, H. R. and Peterman, D. A., "Accuracy of Junction Temperature Measurement in Silicon Power Transistor," 1966 International Electron Devices Meeting (October, 1966).

7. Carlson, H. G., Fuller, C. R., Osborne, J. F., and Brown, G. A., "Stability of Etched Oxides," The Electrochemical Society Meeting, Philadelphia, Pa. (October, 1966).

8. Carlson, H. G., Harrap, V., and Osborne, J. F., "Sodium Free Oxides," Electrochemical Society Meeting, Philadelphia, Pa. (October, 1966).

9. Peterman, D. A., and Plumlee, H. R., "Infrared Microradiometer Studies of Operating Power Transistors," 1966 International Electron Devices Meeting (October, 1966).

10. Carlson, H. G., Meyer, D. E., Fuller, C. R., Harrap, V., Osborne, J. R., and Brown, G. A., "Clean MOS Systems," Fifth Annual Physics of Failure in Electronics Symposium (November, 1966). To be published in Volume 5 of Physics of Failure in Electronics, Defense Documentation Center, Cameron Station, Alexandria, Va.

SECTION II

PROGRAM REVIEW

1. INTRODUCTION

The work performed under this contract is divided into two main parts: (a) a test and data analysis program designed to produce a method for reliability screening and (b) a physics of failure program to describe the fundamental mechanisms causing device degradation. The test program was divided into three parts: Preliminary, Main Test, and Verification Test Programs. Physics of failure activities involved surface studies, noise studies, thermal studies and second breakdown studies. The results of all the work performed on this contract will be discussed in this report, with the exception of surface studies, which will be reported on separately.[1]

The test vehicle was a double ended stud 30 watt silicon planar epitaxial NPN transistor. At the start of the program the electrical parameters to be used throughout the duration of the contract were determined. Failure criteria for degradation type failures were established on the basis of device physics. Further details pertaining to the test vehicle, electrical parameters, and failure criteria are contained in Section III.

2. TEST AND DATA ANALYSIS PROGRAM

a. Preliminary Test Program

The Preliminary Test Program is discussed in detail in the first interim report.[2] The results of the preliminary tests showed that seven of the nine tests suitably stressed the device to produce meaningful failures. These were temperature storage step stress, temperature storage life, reverse bias step stress, reverse bias life, power operating step stress, power operating life and constant acceleration step stress tests. The other two tests, thermal shock and impact shock, did not produce any failures. Three parameters I_{EBO} (5 V), I_{CEO} (70 V) and h_{FE} (5 mA) were found to be the prime failure indicators accounting for approximately 90 percent of the degradation failures. The low current h_{FE} (5 mA) degraded downward on all storage, operating and impressed voltage tests. The most sensitive leakage parameter in indicating device degradation on storage and power operating stress tests was I_{EBO} (5 V), while on impressed voltage test it was I_{CEO} (70 V). The high current h_{FE} (1 A) parameter did not degrade on any stress. Mechanical tests showed the device to be structurally sound.

Typical failures were dissected and analyzed to determine the cause of failure. Some of the primary problems identified were:

- Delamination of the Pb-Ag solder (storage tests)
- Emitter to base shorts due to diffusion imperfection (impressed voltage tests)
- Collector to emitter shorts in the proximity of the predicted hot spot determined from IR thermal contour map (operating tests).

b. Main Test Program

The Main Test Program is discussed in Section IV. It consisted of numerous pretreatment tests, a 100 percent mechanical screen and several step stress and fixed stress tests. Data generated from these tests were the primary data used for developing acceleration factors and nondestructive screening techniques.

c. Verification Test Program

The Verification Test Program is discussed in Section V. It consisted of a pretreatment test 100 percent mechanical screen and some life tests. The test vehicle used differed slightly from that of the Main Test Program. Data from these tests were used to determine how well the results of the Main Test Program could be generalized.

d. Accelerated Test Results

Section VI is devoted exclusively to the discussion of accelerated test results. Curves for determining acceleration factors based on fixed, high stress testing and step stress testing are shown. A discussion of the theory of step and fixed stress testing is given in Appendix E.

e. Nondestructive Screening

Section VII is devoted entirely to the discussion of nondestructive reliability screening techniques. In this section, data and results from all three test programs are discussed and compared. A theoretical discussion of the computer programs SERF, LINDA 1 and LINDA 2 are given in Appendix G.

f. Thermal Resistance Studies

During the contract, a study was made to determine the best method of measuring thermal resistance, θ_{J-C}. Early in the contract θ_{J-C} measurements were

made using steady state measuring techniques. These included nine different conditions using three methods (V_{BE}, V_{CBF} and h_{FE}). These results were then compared with test results and thermal impedance values determined by the IR method. Briefly the findings were:

- High thermal impedance appeared to be related to early life operating failures as anticipated
- No correlation was found between high thermal impedance and early life failure on storage and reverse bias voltage type tests
- V_{BE} and V_{CBF} methods gave values of θ_{J-C} which were in close agreement
- V_{BE} and V_{CBF} methods gave lower values of θ_{J-C} but had the same dependence upon operating conditions as values from the IR method
- h_{FE} method gave much higher values of θ_{J-C} than either V_{BE} or V_{CBF}, but lower values and a different dependence on operating conditions from the IR method.

In an attempt to obtain better correlation between θ_{J-C} obtained by IR thermal profiles and those recorded by electrical measurement techniques, the ZOT (ΔV_{CBF}) method was investigated. It was found that values obtained by both methods tracked very well, and were related by a constant factor of approximately 2. The results of the most recent work are given in Section IV.

3. PHYSICS OF FAILURE ACTIVITIES

a. Surface Studies

Surface studies received the major effort performed under the physics of failure portion of the contract. Some of the studies included measurement of contamination of the thermal oxides (e.g., Na), characterization of MOS capacitors with various oxides, postulation of models for the oxide structure and various instability modes, and analysis of techniques for production of MOS systems that are electrically and thermally stable. The surface study work is covered separately.[1]

b. Noise Studies

Noise studies conducted under this contract are summarized in the first interim report.[1] Some of those highlights are discussed in this section.

Noise figure measurements were made on fifty of the transistors tested on the Preliminary Test Program. These measurements were taken at only one set of

bias conditions. The noise figure measurements prior to test were found to be a poor indicator of the difference between reliable and unreliable devices. However, noise measurements under different bias conditions might have shown better correlation with test results. Additional studies performed included a preliminary study of transistor noise waveform characteristics which considered RMS noise magnitude as well as waveform characteristics. In this study the noise peaks above a specified threshold were applied to an integrator for a specified time period. Under the existing measurement conditions no significant differences were detected among a sample of ten devices. It was concluded from the noise studies that a detailed empirical study of the relationship between transistor reliability and noise waveforms would be quite involved. However, field plate diodes offer the possibility of separating surface and bulk noise, and studies of the differences in waveform between the two types of noise might yield useful results with a less extensive program.

c. Thermal Studies

The thermal studies were conducted early in the contract in order to allow the use of the results in the three test programs and the second breakdown studies. They were designed to investigate the thermal behavior of a high frequency planar expitaxial power transistor, both experimentally and theoretically. An infrared (IR) microradiometer was used to measure the local surface temperature of operating devices. Variations were obtained for a wide range of steady state operating conditions.

Various electrical methods of measuring the junction temperature (T_J) of a device were evaluated by comparison with microradiometer (IR) measurements. This evaluation has resulted in an explanation of the differences in measurements obtained from the various methods, and has indicated the relationship of these measurements to the actual peak junction temperature.

The electrical operating conditions, which result in the greater temperature variation, have been determined. Measurements under these electrical conditions should result in better predictions of reliability of the transistors.

The emitter current density, which tends to concentrate along the emitter-base edge, was calculated by using a theoretical model. With this result for the current distribution and a solution for the heat transfer in a silicon chip, temperature profiles were calculated across the surface of the chip. With the ability to make these temperature calculations, it is now possible to evaluate the thermal characteristics of proposed designs.

Most of the thermal study work performed under this contract is discussed in the second interim report.[3] A summary of this work is contained in Section VIII.

d. Second Breakdown Studies

The physics of failure work on second (thermal) breakdown included both practical and theoretical studies. The practical work of temperature measurements on operating devices by IR scanning methods is covered by previous reports, [2], [3] and shows the importance of voids and design parameters in causing the hot spot formation leading to breakdown. Theoretical work on a model of this phase of the breakdown, showing the importance of bulk resistance in affecting the conditions for hot spot formation, is discussed in Section IX.

SECTION III

STUDY VEHICLE AND MEASUREMENTS

1. STUDY VEHICLE

The device chosen for study under this contract is a silicon planar NPN epitaxial power transistor in a double ended stud package with a rating of 30 W (T_C = 100°C). During the contract an improved version of the study vehicle become available and it is also used in the test program. Therefore, to eliminate confusion, the designations device A and device B are used throughout. Device A is the 2N2880 or 2N3998, both with a 0.100 inch square die, and device B is the 2N3998 with a 0.110 inch square die. The devices used for the various test programs are shown below.

Preliminary Test Program	device A (2N2880)
Main Test Program	device A (2N3998)
Verification Test Program	device B (2N3998)

Figure 1 shows isometric views of both devices. A brief description of each device follows:

Device A — This device is mounted to the gold plated copper stud with lead-silver eutectic solder. The emitter consists of ten interdigitated fingers with a peripheral length of 0.52 inch. Ten mil diameter aluminum wires are sonobonded to the aluminum metallization of the base and emitter. The other ends of the wires are resistance welded to ceramic insulated gold plated copper cored nickel posts mounted on the stud. The kovar case is resistance welded to the stud in a dry nitrogen atmosphere and contact made to the terminal post by crimping the tubes in the can. A flattening, cross welding and piercing operation completes the device.

Device B — This is an improved version of device A. The new geometry consists of a comb type emitter with 0.75 inch of peripheral length. The die is attached to a molybdenum capped copper stud with gold-germanium eutectic hard solder. The other methods of construction are the same as those of device A.

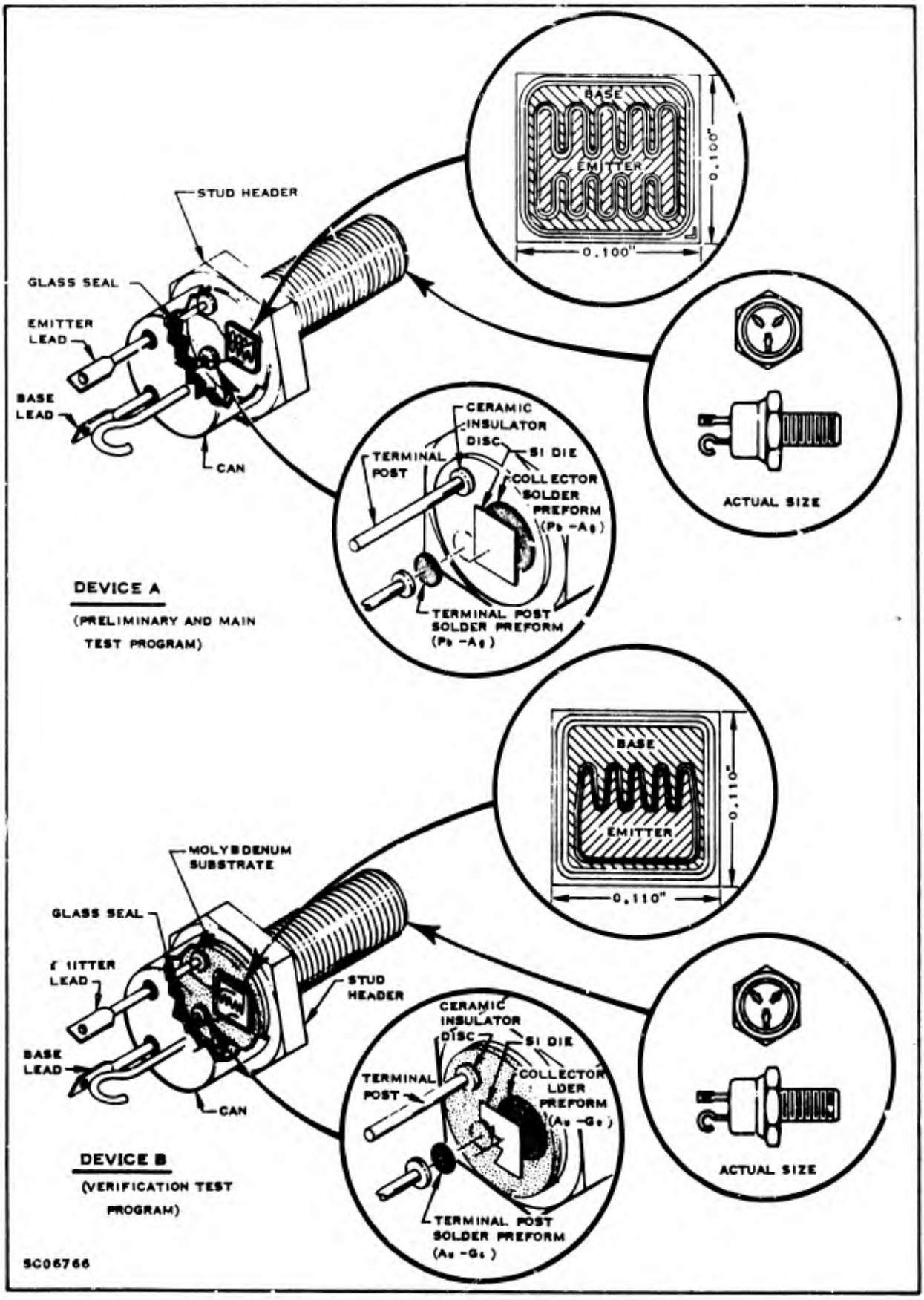


Figure 1. Isometric of Devices Used in Preliminary, Main and Verification Test Programs

2. MEASUREMENTS

a. Parameters

Ten dc parameters were used throughout the entire program. These consisted of six leakage parameters, two current gain parameters (h_{FE}), a base to emitter voltage ($V_{BE(sat)}$) and saturation voltage ($V_{CE(sat)}$). These parameters were read initially and at each readout interval on the automatic TACT (Transistor and Component Tester) machine. Parameters and conditions for making the measurements are listed in Table 2. In addition to these ten parameters, five other dc parameters were measured initially and on the surviving units of the Main Test Program. These parameters, which consisted of three more leakage parameters and two voltage breakdown parameters, and conditions of measurement are contained in Table 3.

Thermal impedance (θ_{J-C}) measurements were made on approximately 30% of the devices stressed on the power operating step stress and fixed matrix tests in the Main Test Program, by the steady state V_{CBF} and by the ΔV_{CBF} pulse technique. (Both techniques are described in Appendix B).

b. Failure Criteria

Many of the commonly used techniques for data analysis require that failure limits be defined for each of the measured parameters. Failures are usually classified as either degradation or catastrophic. In either case the specific definition of failure is a function of both the component part and the intent of the test program. The failure criteria used for degradation and catastrophic failures in Table 2 and Table 3 are discussed below.

Degradation

One way to define these degradation failure limits is in terms of system performance, i.e., a device fails when its parameters are such that it could no longer perform its assigned function in a typical system. However, in the present program failure limits are based on device physics. The procedures used to define these limits are:

a) Wherever possible the physical factors affecting a given parameter are identified.

b) The distribution of initial data was examined to verify that the values fall within the expected range.

c) An estimate was made of the change in the parameter value required to indicate when a significant physical change had occurred. Failure limits were based on this estimate.

Table 2. Parameter Degradation Failure Criteria for Both Device A and Device B

Electrical Parameters	End Point Limits	
	Minimum Value	Maximum Value
I_{CEO} V_{CE} = 30 V	—	Δ Change > 0.01 μA and % Change > +300%
I_{CEO} V_{CE} = 70 V	—	same
I_{CBO} V_{CB} = 30 V	—	same
I_{CBO} V_{CB} = 70 V	—	same
I_{EBO} V_{EB} = 5 V	—	same
I_{EBO} V_{EB} = 8 V	—	same
h_{FE} V_{CE} = 5 V, I_C = 5 mA	-30%	+30%
h_{FE} V_{CE} = 5 V, I_C = 1 A	-30%	+30%
$V_{BE(sat)}$ I_C = 1 A, I_B = 200 mA	0.6 V	0.95 V
$V_{CE(sat)}$ I_C = 1 A, I_B = 200 mA	—	0.3 V

Note: All measurements were performed at room temperature both initially and at each readout step. Opens and Shorts, only, are considered catastrophic failures.

d) In some cases test equipment resolution would not allow measurement of the small parameter changes determined from consideration of the device physics. In these cases the lowest measurable change allowed by the test equipment was used as a failure criterion.

Table 3. Special Parameters*

Electrical Parameter	Conditions
I_{CBO}	V_{CB} = 3 V
I_{CBO}	V_{CB} = 15 V
I_{CBO}	V_{CB} = 150 V
BV_{CBO}	I_C = 100 μA
BV_{EBO}	I_E = 100 μA

*Read only twice — initially and on the surviving units of the Main Test Program. These measurements were also made at room temperature.

It is reasonable to assume that a device which failed according to limits established in this manner would eventually prove unreliable in a system. Nevertheless, when failure prediction techniques are established using these limits, they are not necessarily optimized. Other failure criteria are probably necessary to optimize prediction.

A brief discussion of the device physics and the appropriate degradation allowed in each case for the leakage currents, h_{FE}, V_{CE}, and V_{BE}, is presented below.

a) Leakage Currents, I_{CEO}, I_{CBO}, I_{EBO} — The leakage currents are dependent on depletion layer carrier generation and surface effects. Surface effects are not readily calculated, and a somewhat arbitrary failure limit must be used. For the present, a device on which any leakage current increases by a factor of three will

be considered a failure, provided this increase is also 0.01 μA minimum. Therefore, for very low leakage values the delta change is the limiting criterion, and for higher values the percent change is the limiting value.

b) Current Gain, h_{FE} — The low current (5 mA) h_{FE} is primarily dependent on recombination at the surface emitter-base junction, whereas the high current (1 A) h_{FE} is dependent on high level injection effects such as conductivity modulation in the base. A change of ±30 percent has been established as the failure limit.

c) Base-emitter Voltage, V_{BE} — The V_{BE} is mainly dependent on the junction voltage and contact resistance. In saturation, conductivity modulation reduces the internal base resistance to a very small value. A device having V_{BE} less than 0.6 volt is considered to have a defective emitter-base junction, and V_{BE} above 0.95 volt is indicative of a poor contact. These values have been defined as the failure limits.

d) Collector-emitter Voltage, V_{CE} — The saturated V_{CE} depends on bulk resistances and on forward and inverse h_{FE}. The initial data indicate that 0.3 volt is a reasonable maximum limit. A device which exceeds this value during stress testing is considered to be a failure.

Degradation type failures remained on stress until test was complete.

Catastrophic

For this program, any device which exhibited an open and/or short after completion of a stress interval was defined to be a catastrophic failure, and was not subjected to further stressing.

c. Equipment Correlation

To minimize errors in measuring the electrical parameters due to station setup, equipment malfunction, equipment drift, contact problems, regulation problems, etc., a correlation sample (n = 5) was read prior to and after the regular test samples.

These values were compared with previous data history on the same devices for consistency of readings before the regular units were tested. Both the correlation cards and the test data cards were identified by the same code for later reference in the event of anomalies in the data. Prior to conducting the test program several readings on the correlation samples were accumulated over a period of several weeks. Standard deviations were calculated to give equipment capability by parameter. Degradation limits were set outside these natural tolerances for defining a failure in the program.

SECTION IV

MAIN TEST PROGRAM

1. DESCRIPTION

This section contains a discussion of the Main Test Program which is, as the name implies, the nucleus of the test programs studied under this contract. The objectives and conclusions are discussed first. These are then followed by a discussion of test description, thermal resistance studies, evaluation experiments, data analysis and results, and failure analysis. The analysis of the fixed and step stress test results of the Main Test Program found in this section is somewhat qualitative. The more detailed quantitative analysis is in Section VI.

2. OBJECTIVES

The objectives of the main test plan are:

- Determine screening effectiveness of each pretreatment stress
- Examine relationship of fixed and step stress
- Establish acceleration curves
- Determine screening effectiveness of 100 percent 10,000 G constant acceleration pretreatment test
- Establish parameter response for the pretreatment groups and compare with each other and with the control
- Evaluate thermal impedance measurement techniques.

3. CONCLUSIONS

It was found that the device response to power pretreatment could be used to predict future failures on both storage and power operating tests but was not so effective in predicting failures on reverse bias voltage tests. The data show that no pretreatment appears to enhance the prediction of failures on the reverse bias voltage tests. These results were obtained from the SERF program and are discussed in more detail in Section VII.

The relationship of fixed stress to step stress has been studied, but different results were obtained by fixed stress testing and step stress testing. This difference has not been satisfactorily explained. It appears that a number of mechanisms are operative and that it would be necessary to study individual parameter behavior in much greater detail in order to isolate the different mechanisms. Possibly then the fixed stress and step stress results can be reconciled. Details are discussed in Section VI.

The activation energies and failure rates for some of the fixed and step stress tests have been calculated. An activation energy of 1.0 eV, for example, has been calculated from the storage step stress results up to 250°C. In each of these tests there appears to be a number of mechanisms operative which have not been fully characterized yet. This is discussed in Section VI.

As anticipated, the 10,000 G constant acceleration test was effective in removing most of the mechanical "rogues" or "sports."

A Kolmogorov-Smirnov two-sample test was run on all parameter measurements at all readout steps on all tests in the Main Test Program, in order to determine if pretreatment modified device response to high stress testing. Some significant differences were noted, particularly on h_{FE} (5 mA) and I_{CEO} (70 V). This analysis is discussed in Section VII.

The thermal resistance studies indicated that θ_{J-C} measured by the ZOT (Appendix B) method at V_{CE} = 20 V more nearly approximated the temperature of the device as indicated by IR measurements than did θ_{J-C} measurements by steady state techniques or the ZOT method at lower V_{CE}. However, high θ_{J-C} values measured by this technique did not preclud survival under high stress testing, but most devices with high θ_{J-C} values did fail under high stress testing. Yet, most devices with low θ_{J-C} values did not fail under high stress testing.

The primary failing parameters were h_{FE} (5 mA), I_{CEO} (30 V) and I_{CEO} (70 V). Most degradation failures were due to temperature voltage induced inversion (TVI), surface contamination and presence of an unknown volatile encapsulated within the device. There were relatively few catastrophic failures and most of them occurred at the higher stress level. Analysis of failures is discussed in Section IV-8.

4. TEST DESCRIPTION

The Main Test Program consisted of four separate tests: (a) pretreatment tests, (b) 100 percent mechanical screen tests, (c) step stress tests, and (d) fixed matrix life tests. This test plan is shown in Figure 2. A discussion of each of these tests is presented by tests.

The silicon planar power transistor used in the Main Test Program along with related parameters and failure criteria are discussed in Section III. The device is depicted in Figure 1.

a. Pretreatment Tests

The original lot of 1140 devices was divided randomly (using random numbers table) into four equal groups of 285 each, three of which received one of the pretreatments listed in Table 4 and the other was the control.

The purposes of the pretreatments were:

1) To determine if the device response to a particular pretreatment could be used to predict future failures on other types of tests, as well as on the same type test. To illustrate refer to Figure 3. Could the response of units subjected to pretreatment (a) be used to predict early failures when those units are subjected to the same type of tests such as A or to different types of tests such as B or C.

2) To determine if different types of pretreatments such as (a) or (b), etc., depicted in Figure 3 would cause the devices to behave differently under test conditions such as A or B, etc. This might be done by comparing the parameter distributions for (a) and (b), etc., at each readout interval of test A or B, etc.

The pretreatments used for (a), (b) and (c) (groups 1, 2 and 3) were relatively minor stresses being at maximum rated conditions for groups 1 and 3 and slightly above maximum rating on reverse bias i.e., $T_A = 125°C$, rather than $T_A = 25°C$. The higher ambient was selected because many customer specifications call out $T_A = 125°C$ for burn-in. The 96-hour pretreatment interval was based on preliminary tests results.[2/] The 12 V, V_{CE}, conditions for the 30 W power operating pretreatment were selected to be 80 percent of the voltage used in the power operating matrix test.

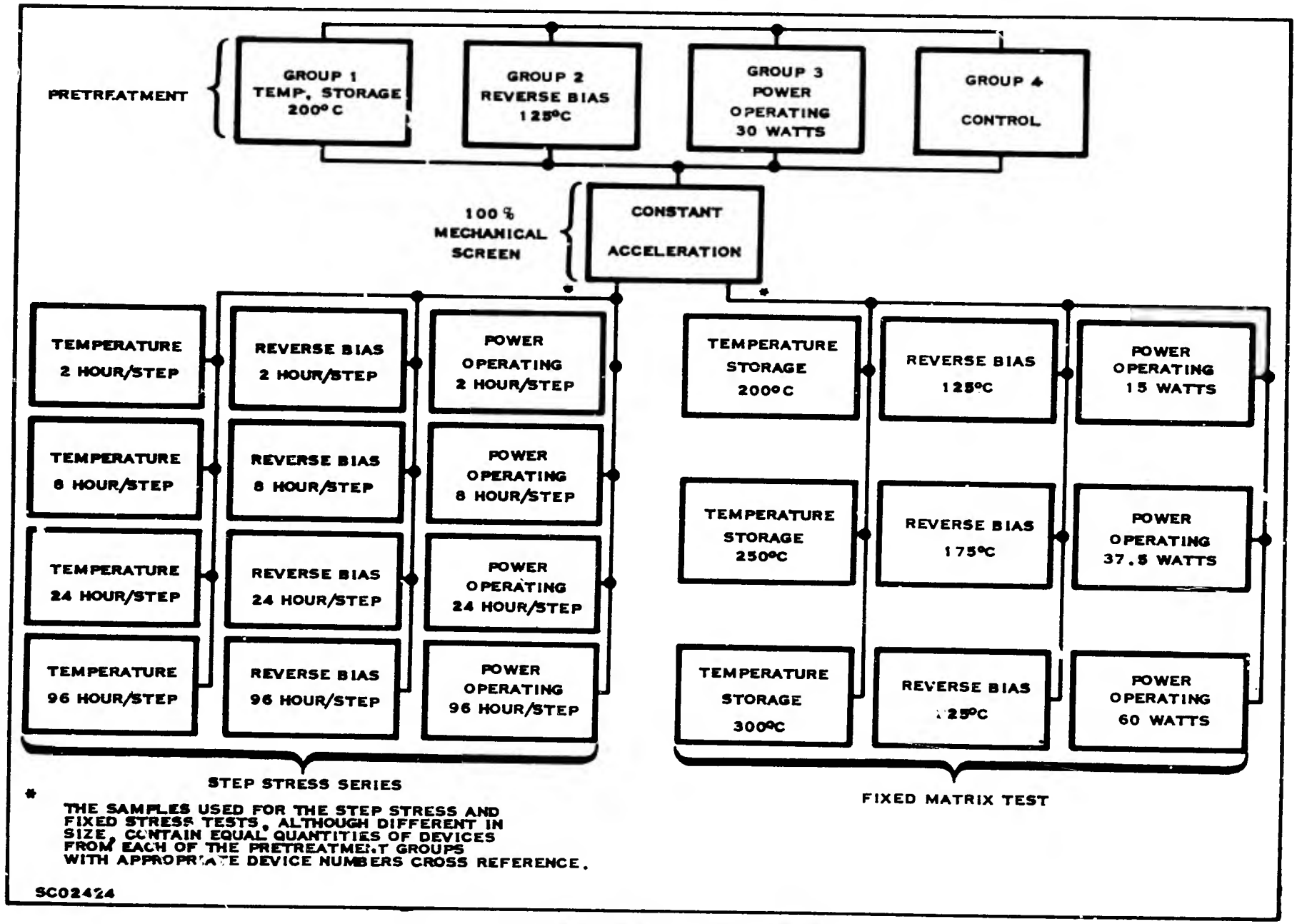


Figure 2. Description of Main Test Program

Table 4. Pretreatment Tests
(Main Test Program)

Group	Stress	Conditions	Hours
1	Temperature Storage	$T_A = 200°C\ ^{+0°C}_{-5°C}$	96
2	Reverse Bias	$T_A = 125 \pm 5°C$ $V_{CB} = 100\ V$ $V_{EB} = 7\ V$	96
3	Power Operating	$T_C = 100°C$ $V_{CE} = 12\ V$ $P = 30\ W$	96
4	Control	-	-

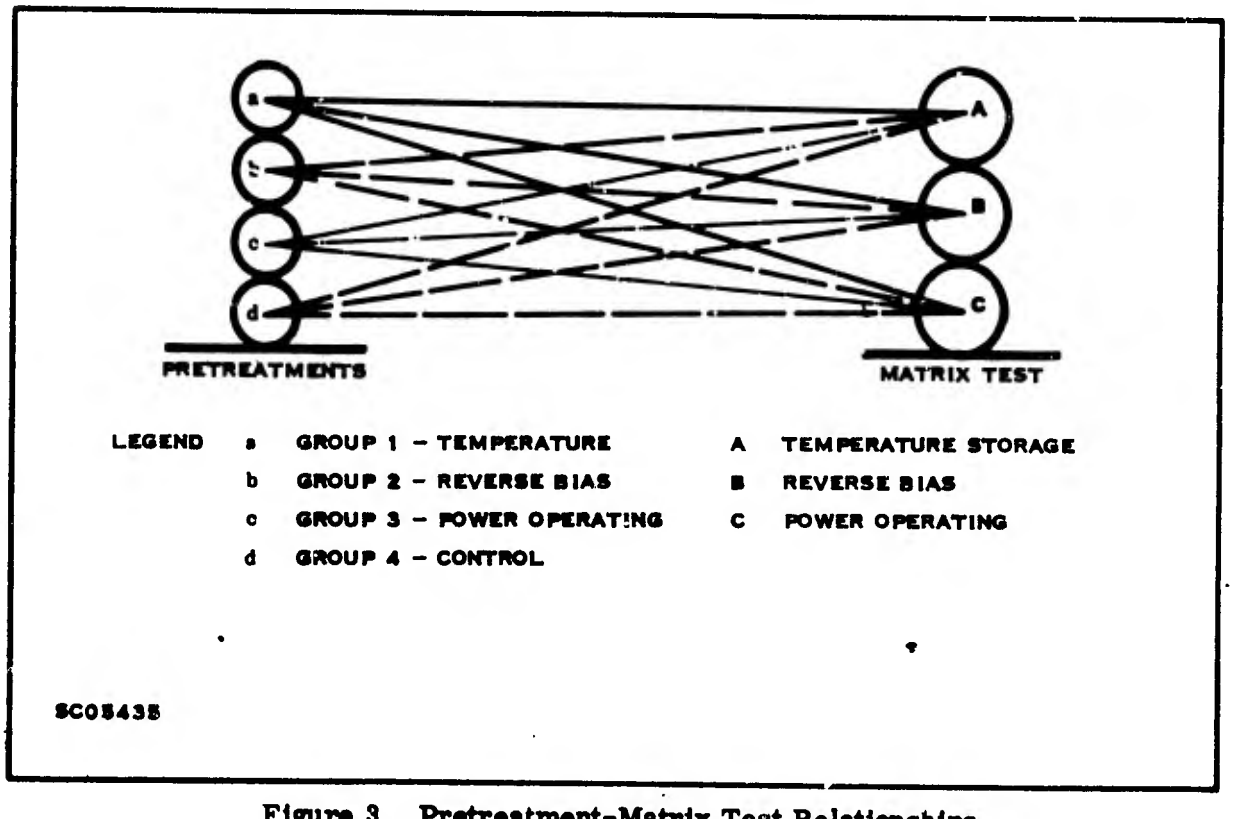


Figure 3. Pretreatment-Matrix Test Relationships
(Main Test Program)

b. 100 percent Mechanical Screen Test

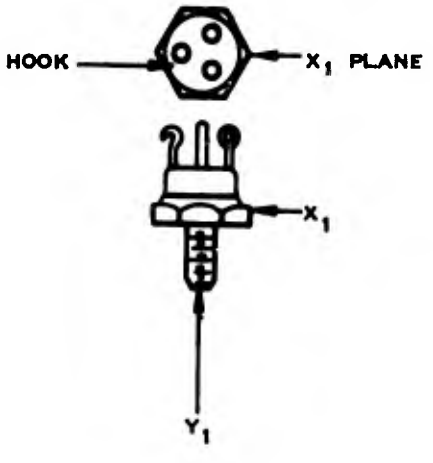
To add more validity to the step stress and matrix tests it was deemed advisable to ensure that mechanically weak units were removed from the population by employing some mechanical screen on 100 percent of the devices. Constant acceleration was chosen as the method for mechanical screen because it was the only one of three mechanical type tests used in the Preliminary Test Program that produced failures (Figure 4).

In Figure 4 it is seen that all the failures in the constant acceleration step stress test occurred at 20,000 G with no additional failures at the next higher step, which indicates that the devices that failed appeared to be weaker units which were not typical of the remaining sample. This suggested that a lower level constant acceleration stress could be used to remove abnormal units from the population. Therefore, the lower level of 10,000 G was selected for the constant acceleration stress condition. All units were subjected sequentially to this stress in both X_1 and Y_1 planes (Table 5) after the pretreatment test and post test parameter measurements.

The lot was then divided into different size samples, containing equal quantities of devices from each of the pretreatment groups, for the step stress tests and for the fixed matrix test.

Table 5. Constant Acceleration Stress (Main Test Program)

PLANE	STRESS
X_1	10,000 G
Y_1	10,000 G



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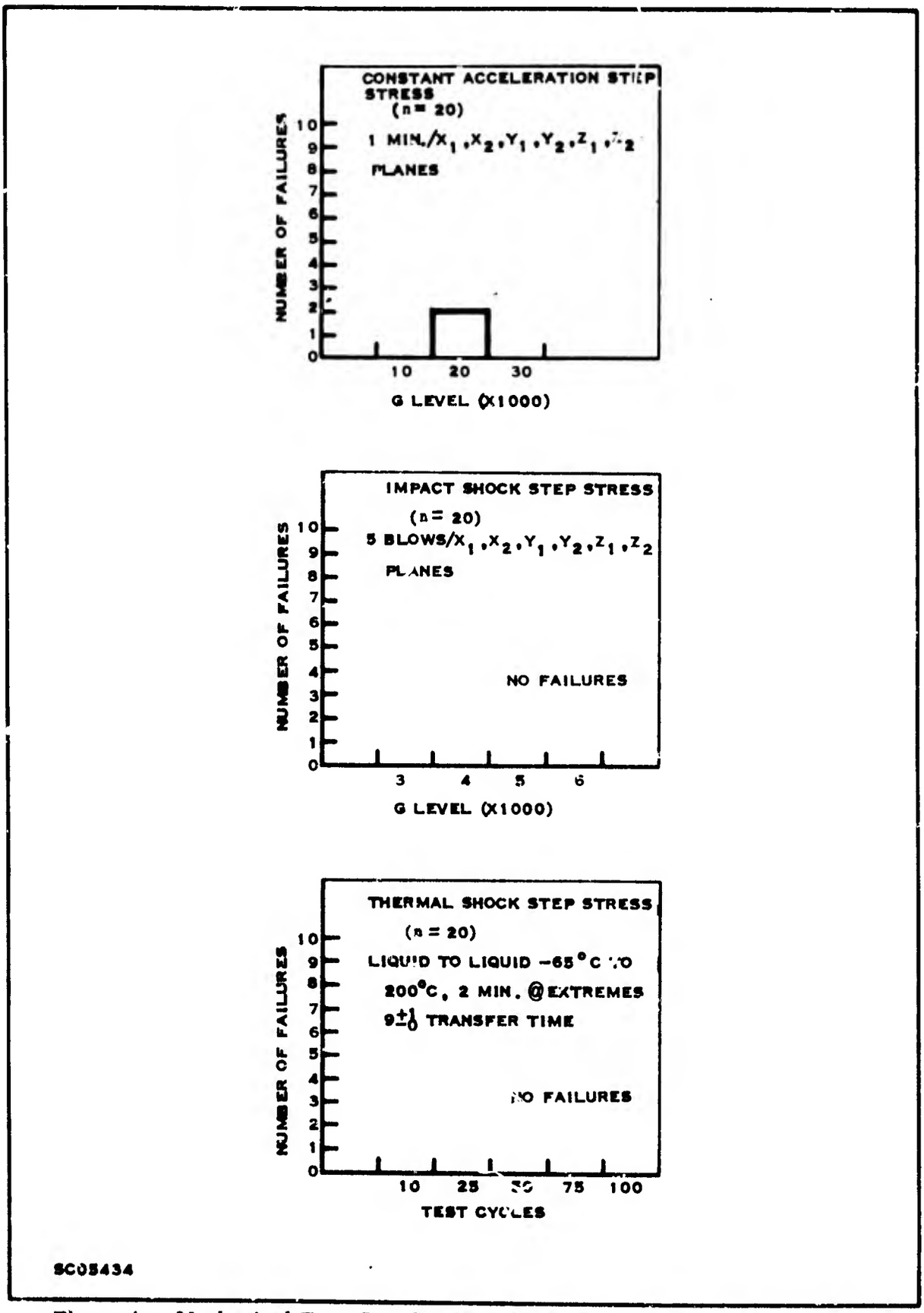

Figure 4. Mechanical Type Step Stress Results (Preliminary Test Program)

c. Step Stress Tests

The step stress tests included power operating, reverse bias and temperature tests, each with four different step intervals of 2, 8, 24 and 96 hours. The conditions for each test are in Table 6.

Table 6. Step Stress Test Conditions (Main Test Program)

Test	Steps	Range	Increments	Step Interval	Sample Size per Step Interval
1) Temperature	7	150°C to 300°C	25°C	2 hrs	20
				8 hrs	20
				24 hrs	20
				96 hrs	20
2) Operating T_C = 50°C V_{CE} = 15 V	9	I_C = 1.0 A to 5 A	0.5 A	2 hrs	20
				8 hrs	20
				24 hrs	20
				96 hrs	20
3) Reverse Bias V_{CB} = 100 V V_{EB} = 7.0 V	7	T_C = 150 to 250°C	25°C	2 hrs	20
	7			8 hrs	20
	7			24 hrs	20
	5			96 hrs	20

Temperature

The conditions chosen for the temperature step stress test were the same as those previously used in the preliminary storage step stress tests, the results of which are depicted in Figure 5. Even though no failures occurred in the Preliminary Test Program the lower three steps, 150°C, 175°C, and 200°C, were retained for all four tread lengths. This was done to determine if the new lot from which the devices were selected differed significantly in response to stress from the lot used in the Preliminary Test Program.

Reverse Bias

The reverse bias step stress test conditions differed slightly from those of the preliminary tests whose results are depicted in Figure 6. It was anticipated that the increased stress would be a more sensitive test of inversion type failures. The specific differences were: (a) the temperature of the first step was increased from T_C = 100°C to T_C = 150°C, (b) the temperature of the last step was increased

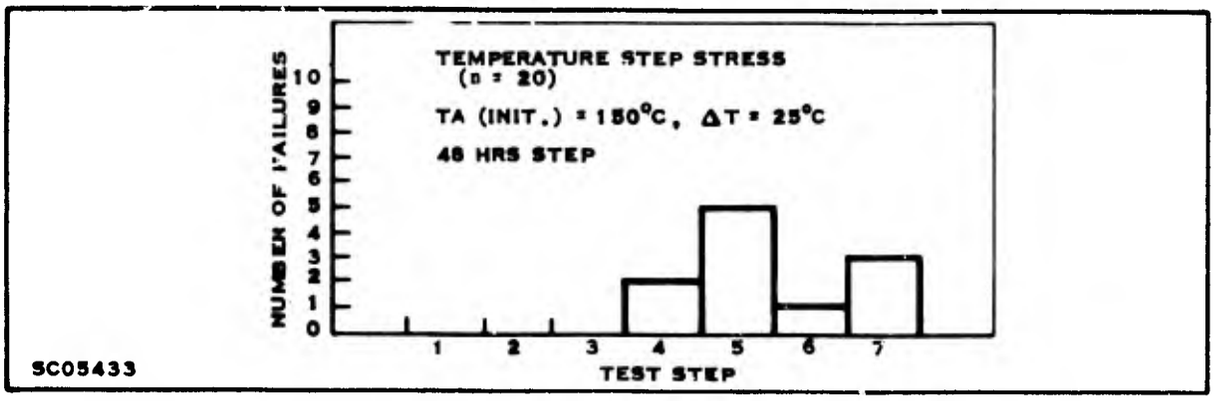

Figure 5. Temperature Step Stress Results (Preliminary Test Program)

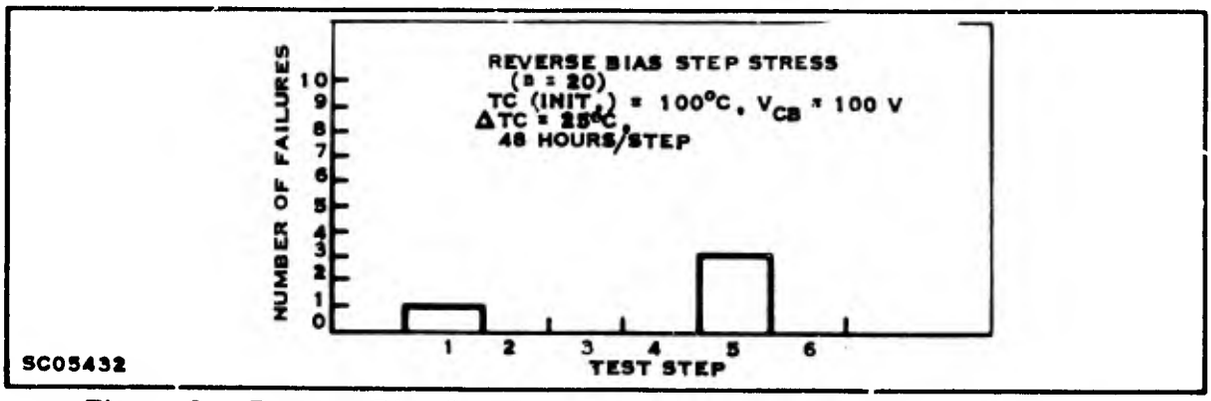

Figure 6. Reverse Bias Step Stress Results (Preliminary Test Program)

from T_C = 225°C to T_C = 250°C, (c) the stress circuit was changed from that in Figure 7 to that of Figure 8 so that both junctions were reverse biased, and (d) the reverse bias was retained on the units until they cooled to room temperature.

Power Operating

The conditions chosen for the power operating step stress tests were based on the 30 W rating of the device and results of the preliminary operating step stress test. The preliminary test data are summarized in Figure 9. Of the eleven failures noted, ten were catastrophic failures. The fact that all failures in the test occurred at the 30 W step, and no additional failures were noted at 40 W, 50 W and 60 W, indicates that 30 W at V_{CE} = 20 V is above the capability of device A. The collector-emitter voltage was 15 V at 40 W and 50 W, and 12 V at 60 W. The fact that most of the failures were due to shorted collector to emitter junctions is also indicative of an overstress condition. Additional data analysis details are included in the First Interim Report.[2]

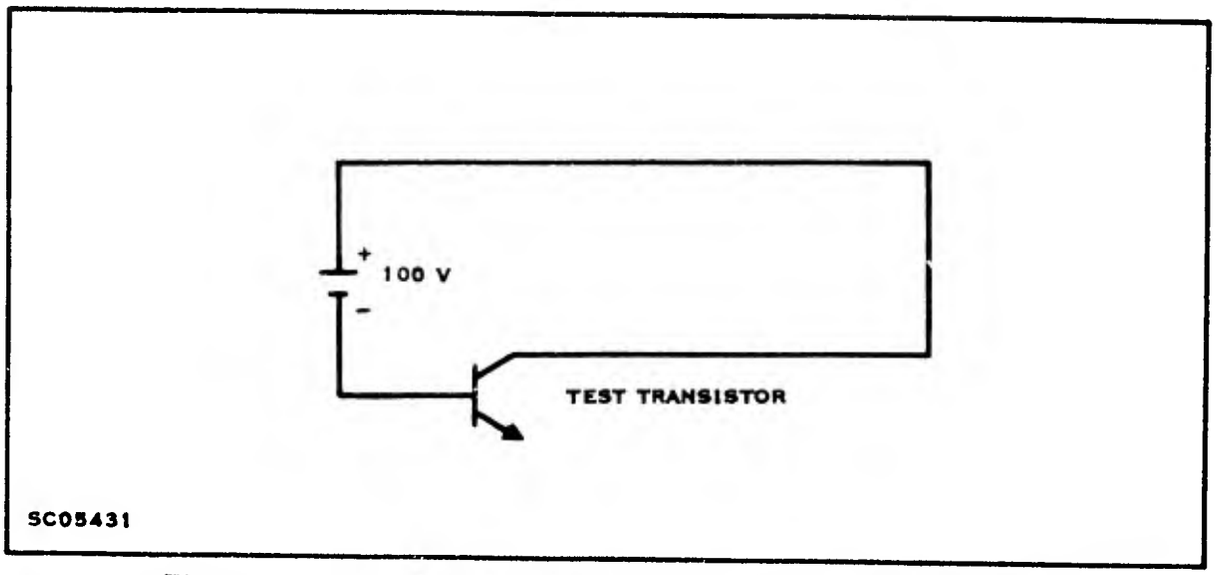

Figure 7. Reverse Bias Test Circuit (Preliminary Test Program)

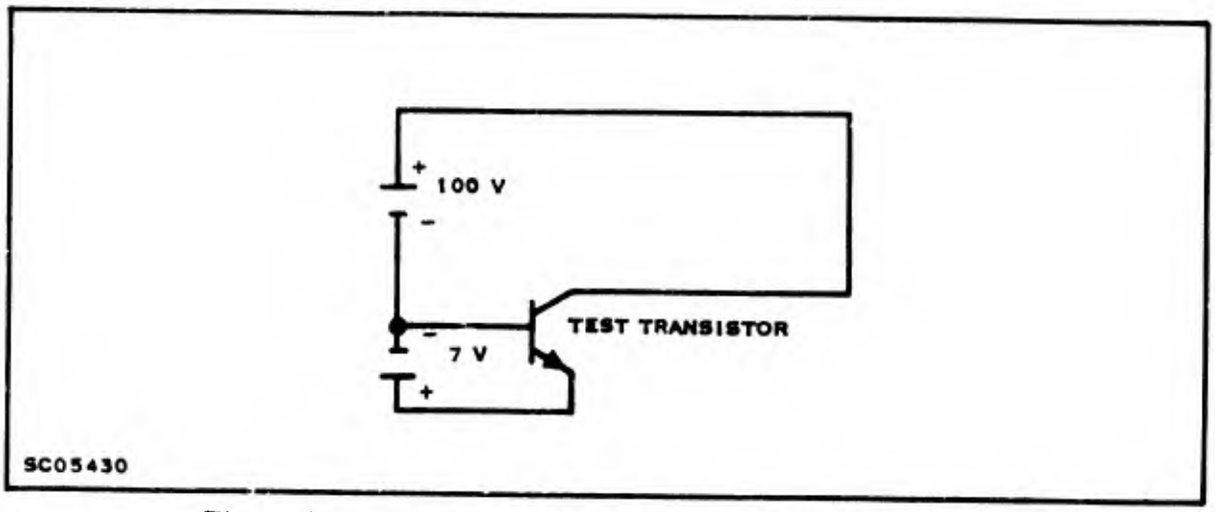

Figure 8. Reverse Bias Test Circuit (Main Test Program)

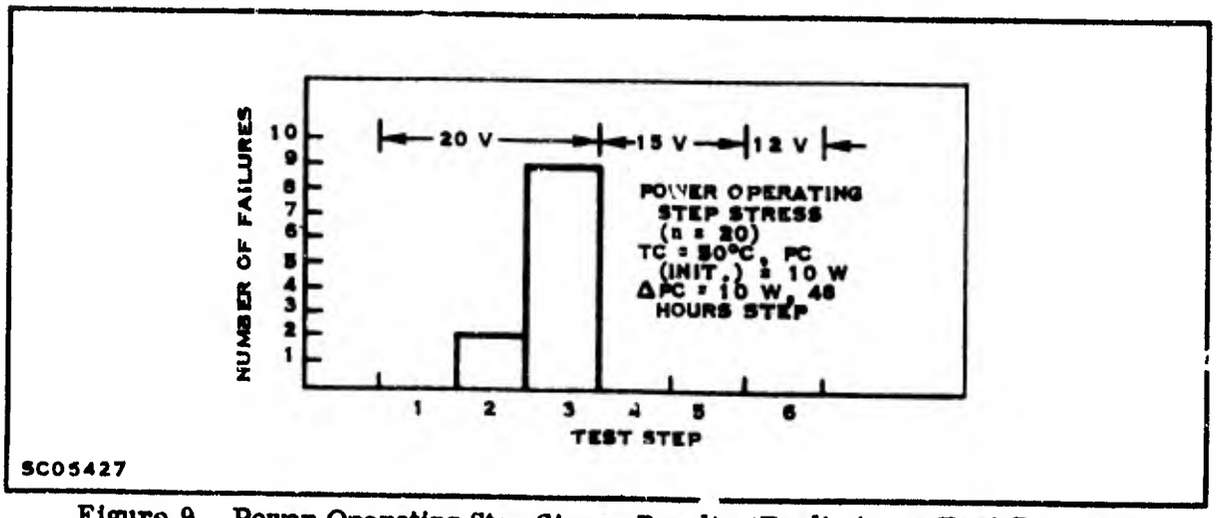

Figure 9. Power Operating Step Stress Results (Preliminary Test Program)

In addition to the data of Figure 9 the IR profiles discussed in Section VIII entitled Thermal Studies showed that the junction temperature (T_J) increased for a given power as collector-emitter voltage was increased. Figure 27 shows that for $V_{CE} \geq 20$ V the operating temperature (T_{Jmax}) increases very rapidly with small increases in collector current (I_C) and may result in thermal failures for $I_C > 1.5$ A at lower V_{CE}. The device can be operated at much higher I_C before comparable thermal failure results; this is illustrated by extrapolating the constant $V_{CE} \leq 15$ V curves in Figure 27 linearly to $I_C = 5$ A. Therefore a collector-emitter voltage (V_{CE}) of 15 V was chosen which represented the highest voltage that could be used for device A when operated at $T_C = 50°C$ without causing a large percentage of early failures. As in the Preliminary Test Program the device was mounted to a water-cooled heat sink and the temperature of the case (T_C) was maintained at 50°C during the test.

d. Fixed Matrix Tests

The fixed matrix (life) tests (Table 7) were similar to those used in the step stress series, namely power operating, reverse bias and temperature storage. Readout intervals of 2, 8, 24 and 96 hours were specified for each of the life tests for direct comparison of step stress and fixed matrix test results (Section VI).

Table 7. Fixed Stress Matrix Test Conditions (Main Test Program)

Life Tests	Description (Cell 1)	Description (Cell 2)	Description (Cell 3)
Temperature Storage	$T_A = 200°C$ 1000 hrs (n = 100)	$T_A = 250°C$ 1000 hrs (n = 100)	$T_A = 300°C$ 1000 hrs (n = 100)
Power Operating $T_C = 50°C$	P = 15 W $V_{CE} = 15$ V 1000 hrs (n = 100)	P = 37.5 W $V_{CE} = 15$ V 1000 hrs (n = 100)	P = 60 W $V_{CE} = 15$ V 1000 hrs (n = 100)
Reverse Bias	$T_C = 125°C$ $V_{CB} = 100$ V $V_E = 7.0$ V 1000 hrs (n = 100)	$T_C = 175°C$ $V_{CB} = 100$ V $V_{EB} = 7.0$ V 1000 hrs (n = 100)	$T_C = 225°C$ $V_{CB} = 100$ V $V_{EB} = 7.0$ V 1000 hrs (n = 100)
Readout Intervals	0 2 8 24 96	264 432 600	768 1000

Due to the high incidence of failures obtained in the first step on the storage life test in the Preliminary Test Program, the results of which are depicted in Figure 10, a lower storage temperature of 250°C was selected as the condition for one level of fixed stress. The 200°C temperature storage condition was chosen as another level of fixed stress as it represented the maximum rating of the device. The 300°C temperature storage condition was chosen for the upper level of fixed stress as it was the highest thermal stress that could be imposed on the device without obtaining threshold failures, i.e., exceed the melting point of the die to header mounting solder (309°C), and still provide meaningful data for acceleration factors.

Reverse Bias

The test circuit used for this fixed stress test was the same as for the step stress test depicted in Figure 8. The test consisted of three levels of fixed stress at temperatures of T_C = 125°C, T_C = 175°C, and T_C = 225°C. The Preliminary Test Program reverse bias life test results shown in Figure 11, together with other burn-in data, were used in determining these temperatures. Although the test sockets have a maximum temperature rating of 250°C they start deteriorating at this temperature

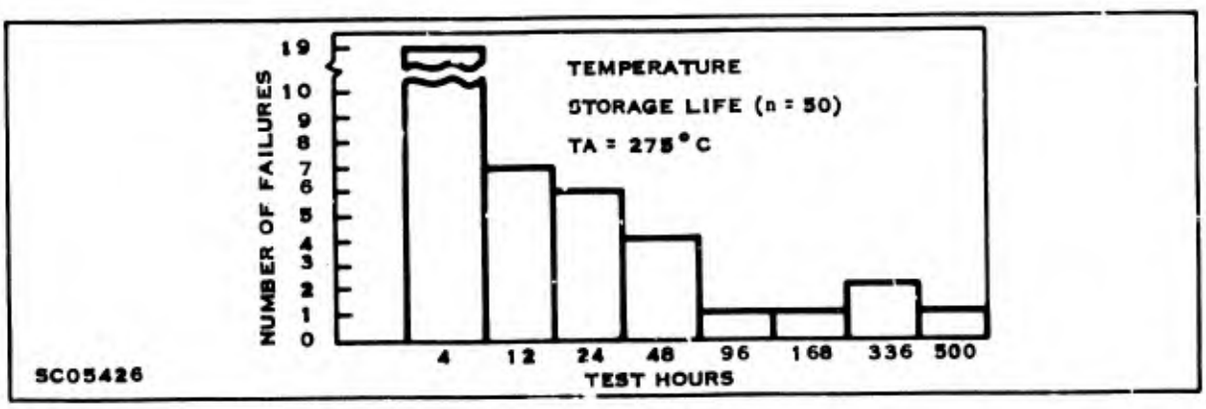

Figure 10. Temperature Storage Life Results (Preliminary Test Program)

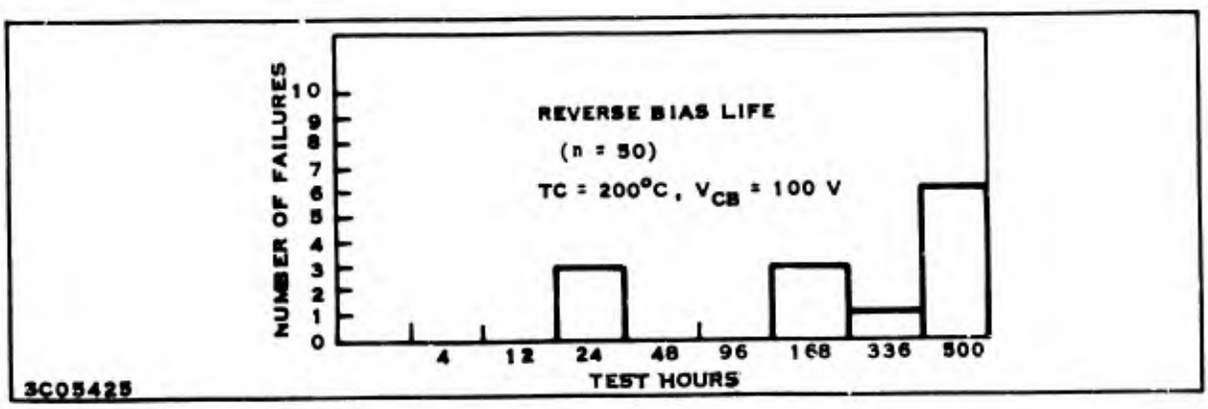

Figure 11. Reverse Bias Life Results (Preliminary Test Program)

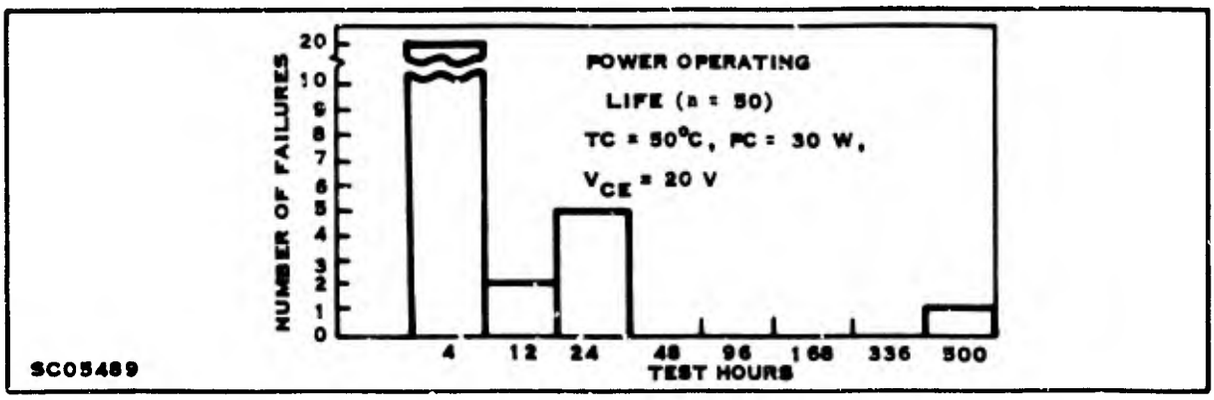

Figure 12. Power Operating Life Results (Preliminary Test Program)

under prolonged exposure but they can operate for a long time at T_C = 225°C. This fact dictated the maximum temperature that could be used on this test.

Power Operating

These fixed stress tests consisted of three at different power levels, 15 W, 37.5 W and 60 W at T_C = 50°C and V_{CE} = 15 V. The 15 V, V_{CE}, was chosen because the Preliminary Test Program results for the power operating life test depicted in Figure 12 were similar to those obtained on the Preliminary Test Program operating step stress test (Figure 9) in that they indicated that V_{CE} = 20 V (30 W) was too high a V_{CE} to use for any extended type tests.

The three power levels were chosen in such a way as to have one power level (15 W) below the maximum rating of 30 W, one slightly above (37.5 W) and one twice rated power (60 W). Using the maximum rated value of thermal resistance (θ_{J-C}) of 3°C/W, the junction temperature (T_J) to be expected was 95°C, 140°C and 230°C respectively for the three power levels.

5. THERMAL RESISTANCE STUDIES

A discussion of the various methods used for measuring thermal resistance (θ_{J-C}) in this program is contained in Appendix B. As a result of the work performed under the contract in thermal studies and the result of the Preliminary Test Program, the ZOT (ΔV_{CBF}) method was selected as the primary method to be used in making θ_{J-C} measurements. This method, therefore, was primarily used in both the Main Test Program (Section IV) and the Verification Test Program (Section V).

a. Correlation of θ_{J-C} Values with Test Results

The Wald-Wolfowitz[4/] runs test was used a number of times in correlating θ_{J-C} values with test results. This test is applicable whenever it is desired to test the hypothesis that two independent samples have been drawn from the same population. If a sufficiently large sample is used, any type of difference may be detected. This difference, for example, may be a difference of medians, of skewness, or of standard deviations. The test consists basically of ordering all of the values of the variable of interest, in this case θ_{J-C}, from low to high or high to low without considering from which population the value came. Then a count is made of the number of runs, i.e., of the number of times values of each variable occur in sequence before a value from the other population is noted. Thus, for example, suppose that the ordering of θ_{J-C} values from low to high is 2.6, 2.7, 2.8, 2.9, 3.2, 3.3, 3.5, 3.6, 3.8°C/W, where the bar denotes a value from the population, F, of devices which later failed and the other values are from the population, G, of devices which did not fail. Then the ordering would be FGGFFGGGG. There would be one run of one value from F, one run of two values from G, one run of two values from F, and one run of four values from G. Clearly if the two distributions are the same, then the values will be well mixed and there will be many runs. Statistical criteria have been derived which specify how many runs would be expected in a particular situation.

Histograms representing the distribution of θ_{J-C} values for a sample of the units which survived the power operating tests of the Main Test Program, as well as those which failed, are given in Figures 13 through 15. These θ_{J-C} measurements were made prior to placing the units on life test. Measurements were made by the 10 V, 15 V, 20 V and 25 V ZOT methods as well as by the h_{FE} and V_{CBF} methods. The θ_{J-C} values for the four step-stress power operating tests are summarized in one histogram; those of the three fixed stress power operating tests in another. Using the Wald-Wolfowitz runs test for a significance level $\alpha = 0.05$, it is found that no difference could be detected in the distributions of the θ_{J-C} values of the units which later failed and those which survived the operating tests.

b. Junction Temperature (T_J)

The θ_{J-C} values of all of the units surviving the power operating life tests were measured in order to determine the effective (junction) temperature to which each device was exposed. The 15 V and 20 V ZOT methods were used for these measurements. Junction temperatures were calculated using these θ_{J-C} values and $T_C = 50°C$. The junction temperatures (T_J) for the units on the Main Test Program which had θ_{J-C} measured by the 15 V ZOT method are given in one histogram; those which had θ_{J-C} measured by the 20 V ZOT in another (Figure 16). Three observations are immediately apparent. First, the 20 V ZOT method "spreads" the T_J values over a wider range than the 15 V ZOT method. Second, the devices with highest T_J values did not necessarily fail. Third, as expected, almost all devices with low T_J values

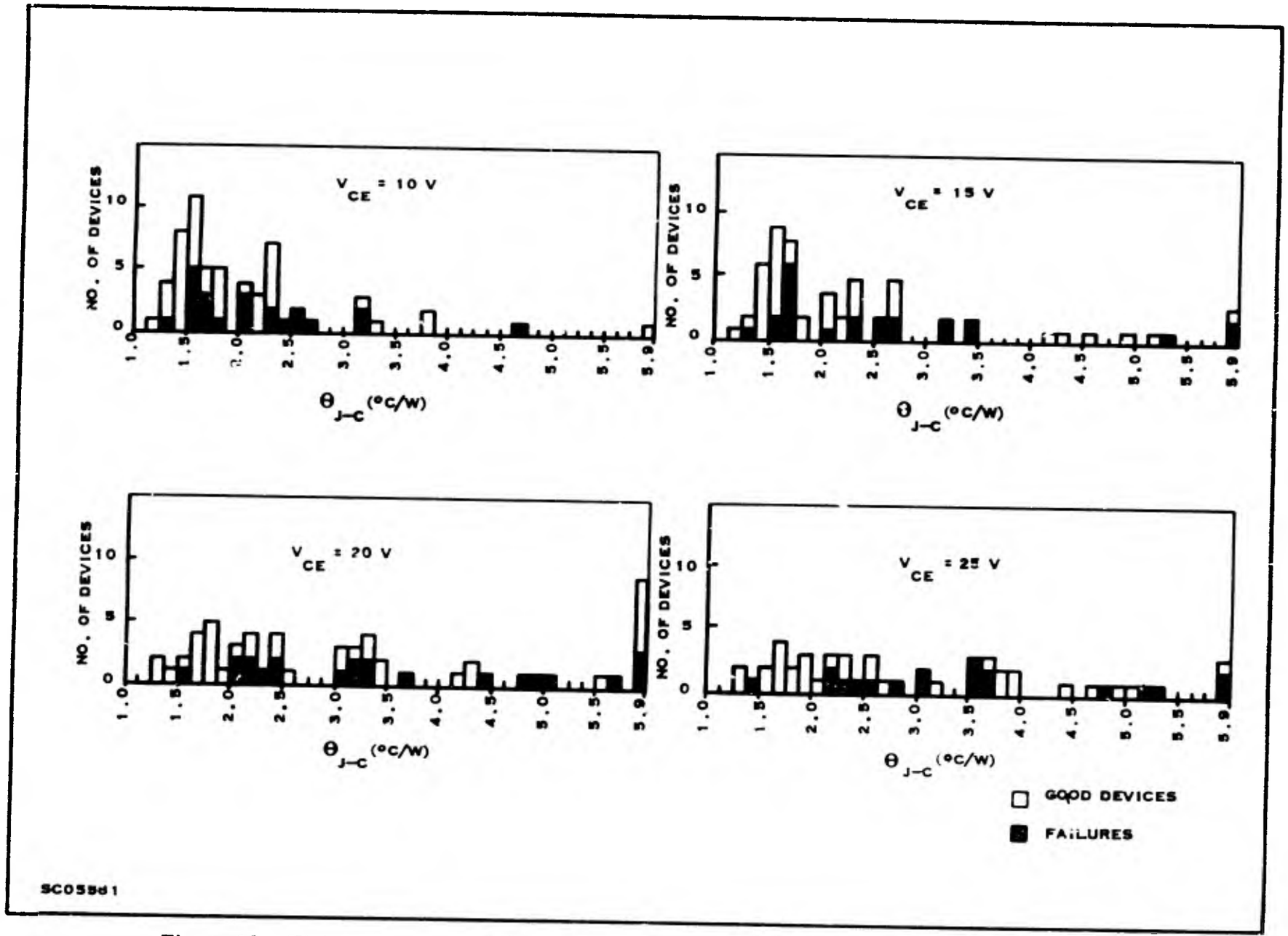

Figure 13. Histograms Showing θ_{J-C} ZOT Method Power Operating Life (Main Test Program)

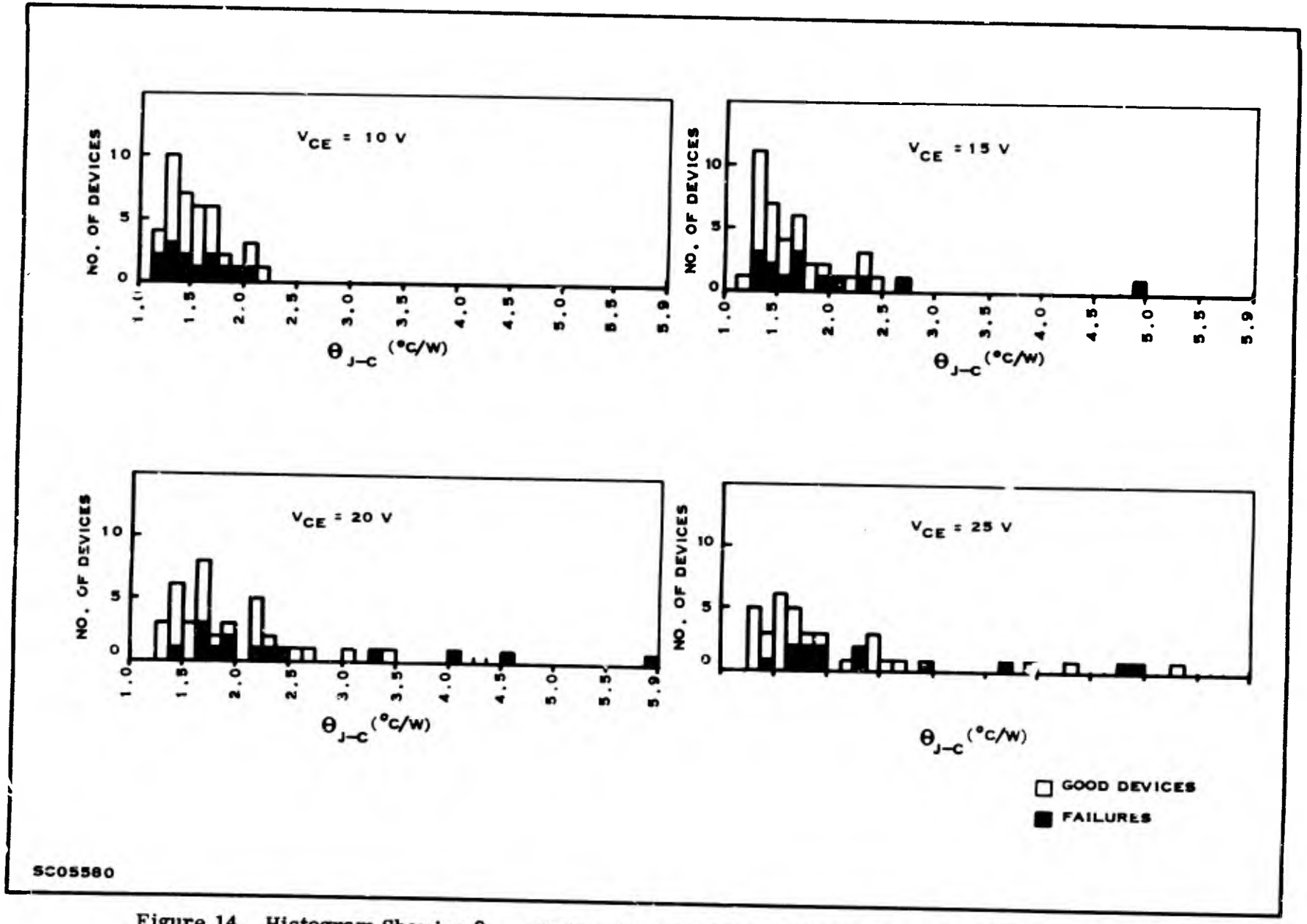

Figure 14. Histogram Showing θ_{J-C} Values for ZOT Method Power Operating Step Stress Test (Main Test Program)

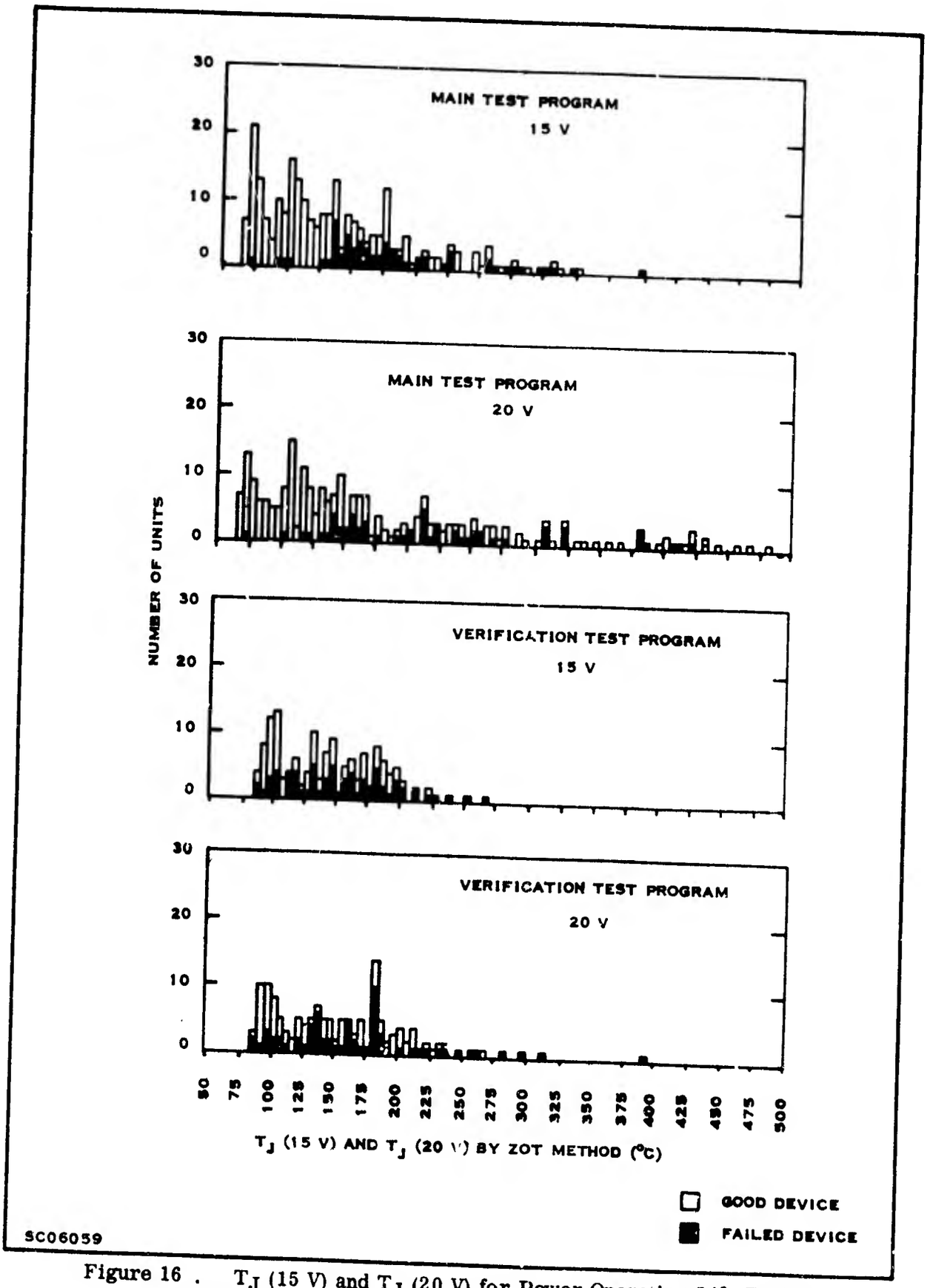

Figure 16 . T_J (15 V) and T_J (20 V) for Power Operating Life Tests of Main Test Program and Verification Test Program

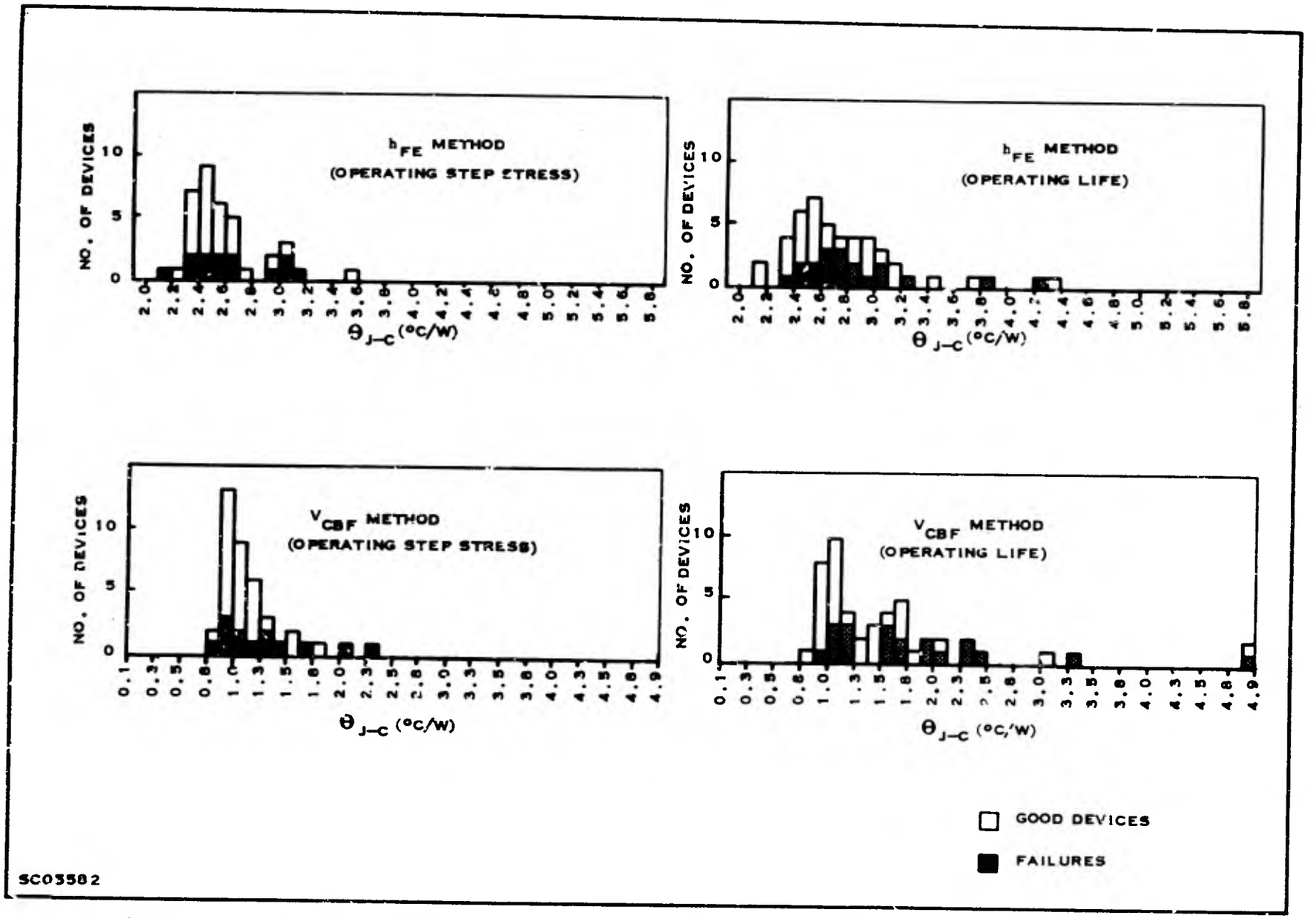

Figure 15. Histograms Showing θ_{J-C} Values for h_{FE} and V_{CBF} Method (Operating Step Stress) and h_{FE} and V_{CBF} Method (Operating Life), Main Test Program

survived the test. A Wald-Wolfowitz runs test reveals that the distribution of T_J values of the bad devices on the Main Test Program is significantly different even at the $\alpha = 0.01$ level from the T_J values of the good devices. Practically none of the devices with low T_J values failed. This was not true, however, for the power operating tests in the Verification Test Program; Figure 16 (the Verification Test Program is discussed in Section V). Here the Wald-Wolfowitz test revealed no difference for $\alpha = 0.05$ in the distributions of the T_J values of good and bad devices. Some devices failed even for very low values of T_J. Failures from both the Main Test Program and Verification Test Program were analyzed. It was not determined if devices with low values of T_J, which failed, have failure modes different from the rest of the failures.

6. EVALUATION EXPERIMENTS

In addition to the tests described for the Main Test Program in Figure 2, several evaluation experiments were conducted using devices which had received special treatment and/or special processing. All such evaluation experiments are called "specials." Five "specials" evaluated during the contract were:

- Second breakdown pretreatment
- Paint on the surface
- Isolated collector
- Second breakdown characterization
- Second breakdown screen

Highlights of each follow in the text. Additional details for the first three "specials," listed above, may be found in Appendices VI, VII, and VIII, respectively, of the Second Interim Report[3]. Details for the other two "specials," listed above, are contained in Appendix C of this report.

a. Second Breakdown Pretreatment

The objective was to determine the effects on reliability and device parameters of units repeatedly operated in second breakdown prior to stress. Several 2N3998 devices (device A, Figure 1) were given a specified second breakdown stress. Two levels of stress were used (hereafter called "light" and "heavy"). The stresses were applied to the groups 10 or 100 times. The stress pulses were 1.8 A for approximately 0.5 ms and 3.5 ms respectively for the light and heavy stress. After this

second breakdown pretreatment devices were stressed for 120 hours on the following power operating test:

$T_C = 100°C$

$V_{CE} = 40$ V

$I_C = 0.375$ A

Results[3] from this experiment indicate that units can be operated several times for short periods in second breakdown and the survivors do not appear to suffer any harmful effects on parameters or reliability. The 100-cycle stress produced a higher percentage of failures than the 10-cycle stress but survivors of the 100-cycle stress were more resistant to failure on power operating than survivors of the 10-cycle stress. There were no obvious differences in results between devices that had received "light" or "heavy" cycles of second breakdown stress.

b. Paint on the Surface

This experiment evaluated the effects on device behavior of black paint after it was sprayed on the surface. A group of 2N2880 devices (device A, Figure 1) was removed from the dry box prior to canning and spray coated with the black paint used for emissivity control[3] when making IR profiles. Units were then air baked for two hours at 200°C, placed in the dry box, canned and sent to final test for electrical measurement. These were then stressed for 72 hours on the following power operating test:

$T_C = 100°C$

$V_{CE} = 40$ V

$I_C = 0.375$ A

These test conditions approximated those used initially by the thermal physics group in their thermal (IR) studies under this contract. The results[3] indicate that the two paints evaluated (Krylon flat black spray enamel No. 1602 and 3M velvet coating 101-C10 black) were not detrimental to IR profiling of the device at high V_{CE} (40 V) and 15 W (1/2 rated power). The paints increased leakage initially but the leakage did not degrade further as a result of stress.

c. Isolated Collector

The objective of this experiment was to examine the behavior of the isolated collector version of device A (2N3996) on power operating and environmental type step stress tests. The test plan consisted of two power operating step stress tests at $T_C = 100°C$, $V_{CE} = 20$ V and $V_{CE} = 40$ V and two environmental step stress tests, thermal shock (liquid to liquid) and constant acceleration (6 planes). In addition to the 10 dc parameters, thermal resistance was measured on those devices stressed on the operating tests.

The test results[3] indicate that the isolated collector version (2N3996) of the 2N3998 appears to be more sensitive to V_{CE} on power operating type tests. Also the thermal resistance values for the 2N3996 were approximately 1° C/W higher than the control (2N3998). On the environment tests the 2N3996 experienced less parameter shifts after thermal shock than the control with no failures experienced by either group after 30,000 G constant acceleration test.

d. Second Breakdown Characterization Experiment

The objective of this experiment was to study the influence of repeated breakdowns of various durations on device degradation and to establish conditions for a second breakdown stress for the next experiment.

Results of this experiment showed that device degradation resulting from being driven repeatedly into second breakdown is not a simple function either of total time in second breakdown or of total number of second breakdown stresses. These results are compatible with the model proposed in Section IX. The conditions recommended for the second breakdown screen experiment (below) were to induce breakdown with 60 V at 1.5 A and maintain the stress in breakdown at 1.8 A for 3 ms. Details of the experiment are found in Appendix C.

e. Second Breakdown Screen Experiment

This experiment was designed to evaluate the use of second breakdown preconditioning as a possible screen. The units were divided into five groups. Four groups were driven into second breakdown for 10, 25, 60 and 100 times respectively under the conditions established by the above characterization experiment. The other group was the control. After the second breakdown preconditioning, all five groups were stressed for 120 hours on the following power operating test:

$$T_C = 100°C$$
$$V_{CE} = 40 \text{ V}$$
$$I_C = 0.35 \text{ A}$$

Thermal resistance values and delay time (time it takes unit to go into second breakdown after application of second breakdown stress) were measured on each device.

The results show (a) some correlation between failures after breakdown, (b) some correlation between θ_{J-C} and failures and (c) poor correlation between θ_{J-C} and delay time. The data indicate that additional work would be necessary to determine if this technique would be suitable for use as a screening procedure. Details of this experiment are found also in Appendix C.

7. DATA ANALYSIS AND TEST RESULTS

A brief discussion of failure bar graphs and of failing parameters is presented for each of the tests in the Main Test Program. Where applicable the results of the Preliminary Test Program are included for reference. As mentioned previously the quantitative analysis of the data using the Computer Program SERF is presented in Section VI and VII.

a. Pretreatment Tests

A summary of the results of the pretreatment stresses is given in Table 8. All failing parameters are listed for each group. The largest number of failures occurred in the power operating test; the smallest number occurred in the 200°C temperature storage test. The E-B junction leakage parameters, I_{EBO} (5 V) and I_{EBO} (8 V) are the major failing parameters in all groups. The next most frequently occurring failure parameter is I_{CEO} (30 V). Defining a catastrophic failure as either a delta change of 100 μA on at least one leakage parameter or else an open or short, it is noted that the power operating test also caused the greatest number of catastrophic failures. The number of failures which were catastrophic is indicated in parentheses in the "Total Failures" column of Table 8. It was found that the power operating pretreatment was the only pretreatment which could be used to predict future failures on other types of tests. The other test for which the prediction holds is temperature storage. It is also shown in Section VII that devices with different pretreatments behave differently under the same test conditions.

b. 100 percent Mechanical Screen Test

Results of the constant acceleration test for all four pretreatment groups are shown in Table 9. The greatest number of failures on this test were from group 1, the one which had temperature storage pretreatment prior to constant acceleration. These four units were either V_{BE} or V_{CE} degradation failures. In the case of group 3, the power operating pretreatment test, no failures occurred on the constant acceleration test. Since power operating test was the more severe pretreatment stress it may have removed the units which would have failed on the constant acceleration test. The number of failures on the constant acceleration test is too small to confirm this statistically but the results suggest such a conclusion.

Table 8. Summary of Failures Resulting from Pretreatment Tests (Main Test Program)

Pretreatment	Total Failures	List of Failing Parameters									
		I_{CEO} 30 V	I_{CEO} 70 V	I_{CBO} 30 V	I_{CBO} 70 V	I_{EBO} 5 V	I_{EBO} 8 V	h_{FE} 5 mA	h_{FE} 1 A	V_{BE} (Sat)	V_{CE} (Sat)
Group 1 **Temperature Storage** **200° C 96 Hours**	10* (3)	1	1	1	0	1	4	2	0	1	0
Group 2 **Reverse Bias** $T_A = 125°C$ $V_{CB} = 100$ V, $V_{EB} = 7$ V 96 Hours	14* (3)	6	4	3	3	6	6	2	1	4	0
Group 3 **Power Operating** $T_C = 100°$ C $V_{CE} = 12$ V, $P_C = 30$ W 96 Hours	17* (7)	8	8	7	7	12	12	4	1	0	0
Group 4 **Control**	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

* Includes both degradation and catastrophic failures.

Table 9. Summary of Failures Resulting from 100 percent Mechanical Screen (Main Test Program)

Pretreatment Stress	Pretreatment Group Number	Total Failures	I_{CEO} 30 V	I_{CEO} 70 V	I_{CBO} 30 V	I_{CBO} 70 V	I_{CBO} 5 V	I_{EBO} 8 V	h_{FE} 5 mA	h_{FE} 1 A	V_{BE} (Sat)	V_{CE} (Sat)
Constant Acceleration	1	4	0	0	0	0	0	0	0	0	3	1
10,000 G	2	2	1	1	1	1	1	1	0	0	0	1
X_1 and Y_1 Planes	3	0	0	0	0	0	0	0	0	0	0	0
1 Min/Plane	4	2	0	1	0	1	0	1	0	0	0	0

c. Temperature Storage Fixed Stress and Temperature Step Stress Tests

In the 200°C life test (Figure 17) there is a constant, small number of failures occurring at each readout step from 96 to 768 hours with no failures at the last readout step. Here only a few of the weaker devices are being eliminated. In the 250°C life test one notes a gradual decrease in the number of failures with a maximum occurring at an intermediate step, between 24 to 96 hours. The primary failure parameter on all of these tests is h_{FE} (5 mA). The second most important failure parameter is i_{CEO} (70 V).

When the summary of failing parameters by test step in Table D-2 on the 250°C and 300°C tests is examined, there is nothing interesting about the 250°C test except that in the final steps (readout intervals) there is an increase in the number of low current h_{FE} failures. However, there is a definite pattern on the 300°C test. On the first four steps of this test the primary failure parameter (indicator) is h_{FE} (5 mA), and there is a considerable number of leakage parameter failures. On the last four steps of the test there is only one h_{FE} (5 mA) failure, the leakage parameters are the primary failure indicators on the remainder of the test.

Examining the median values of the primary failure indicators on the 300°C test it is noted that h_{FE} (5 mA) initially decreases slightly, strongly increases, then dips and finally increases again. This is illustrated in Figure 18, the variation of median h_{FE} (5 mA) values with time for the 300°C test. Here the dip occurs at about 264 hours. Examination of the median values of the other parameters on the 300°C test reveals that at 264 hours there is a sharp jump in the leakage parameter values. For example, I_{CEO} (30 V) increases from 0.0043 μA to 0.0150 μA, I_{CEO} (70 V) from 0.0159 μA to 0.0674 μA, and I_{EBO} (5 V) from 0.0364 μA to 0.0539 μA. Variation of the median value of I_{CEO} (30 V) with time is plotted in Figure 19. Degradation of leakage parameters and low level h_{FE} are indicative of surface problems. Samples of these failures were analyzed after completion of tests. Failure analysis results are in Section IV-8a.

As pointed out in the first interim report,[2/] results of the 275°C temperature storage test of the Preliminary Test Program showed a gradual decrease in the number of failures per step from the initial high to 48 hours (Figure 10), after which there is a constant number of failures for the remainder of the test. Again the primary failure indicators are h_{FE} (5 mA) and I_{CEO}.

In the Main Test Program there is nothing worthy of note in the temperature step stress bar graphs (Figure 20). The primary failure indicator on these tests is the 70 V I_{CEO} reading as indicated in Table D-1.

To review the temperature step stress results on the Preliminary Test Program (Figure 5) show approximately a normal distribution of failures from the 225°C step to the 300°C step. The median occurs about 250°C. The primary failure indicator is low current h_{FE}.

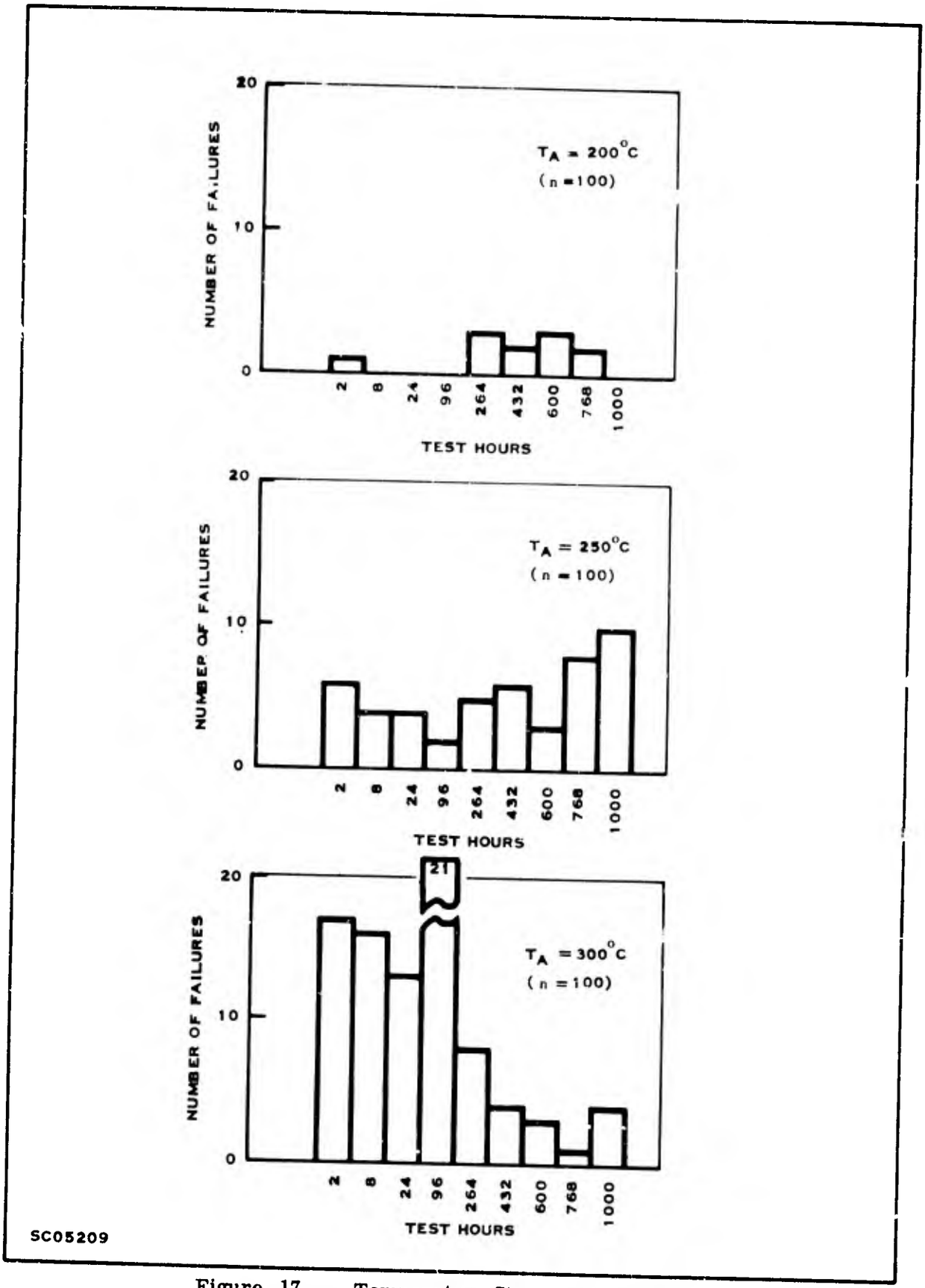

Figure 17. Temperature Storage Life Results
(Fixed Matrix Test - Main Test Program)

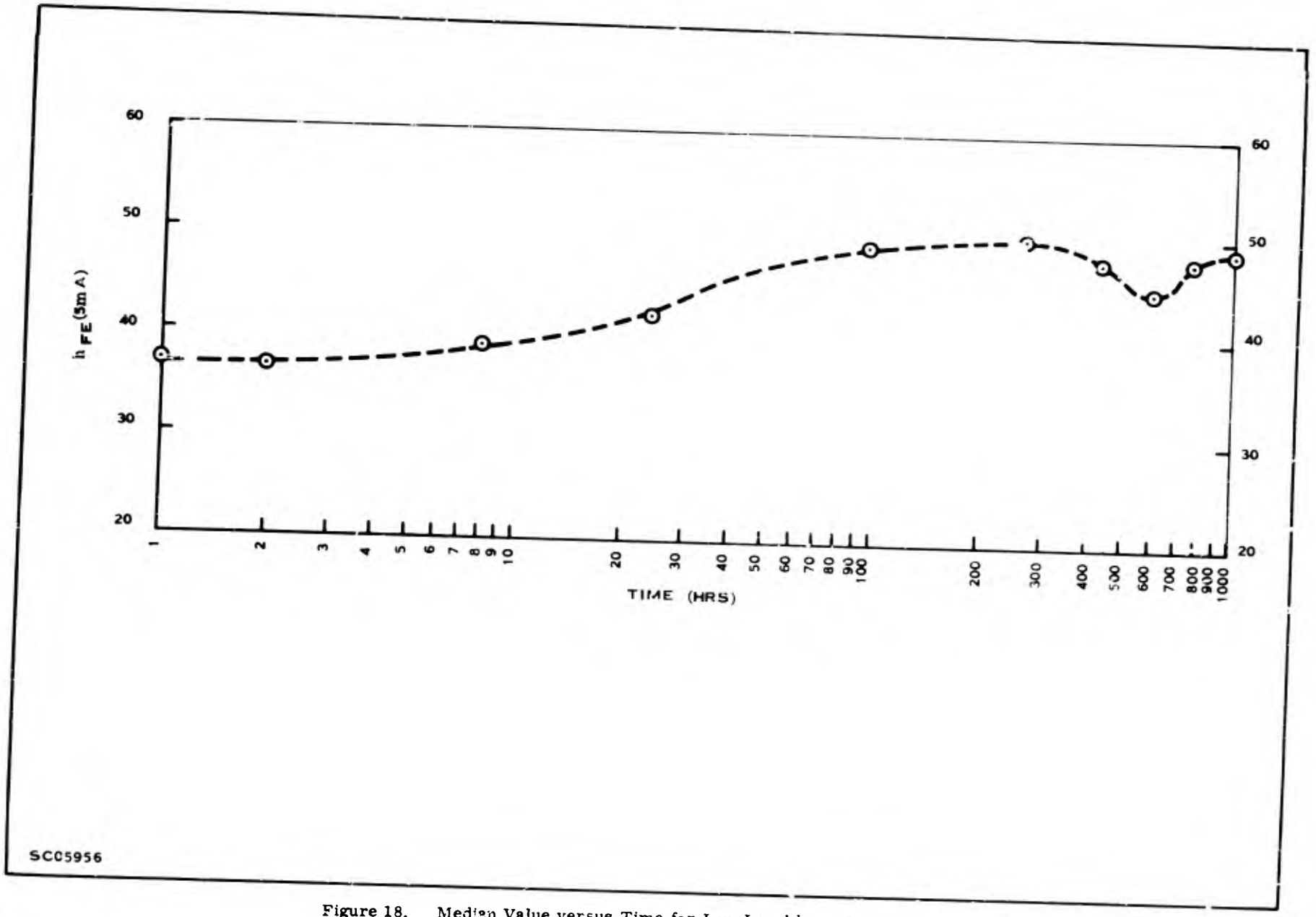

Figure 18. Median Value versus Time for Low Level h_{FE} (5 mA)
300° C Temperature Storage Fixed Stress Test (Main Test Program)

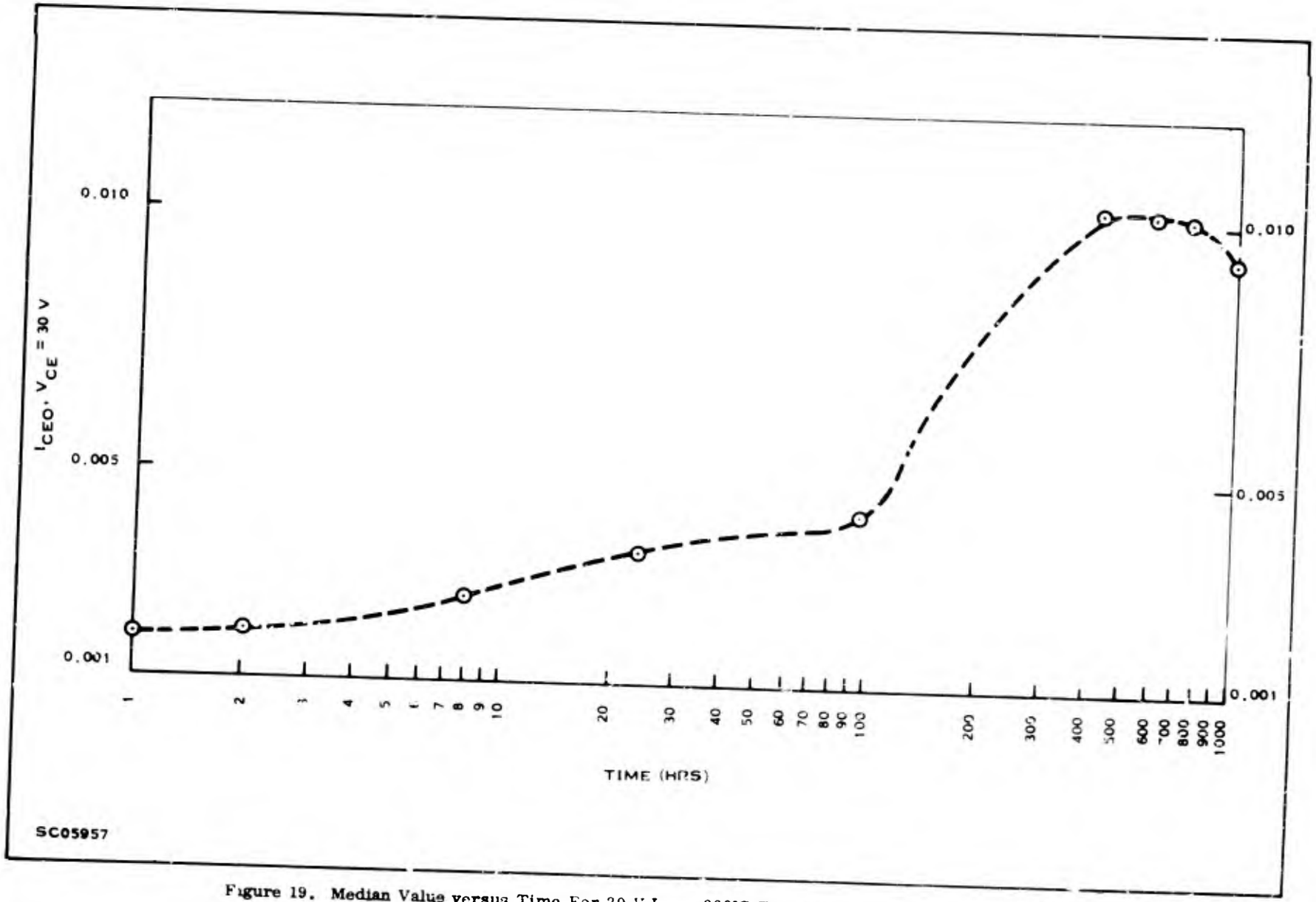

Figure 19. Median Value versus Time For 30 V I_{CEO} 300°C Temperature Storage Fixed Stress Test (Main Test Program)

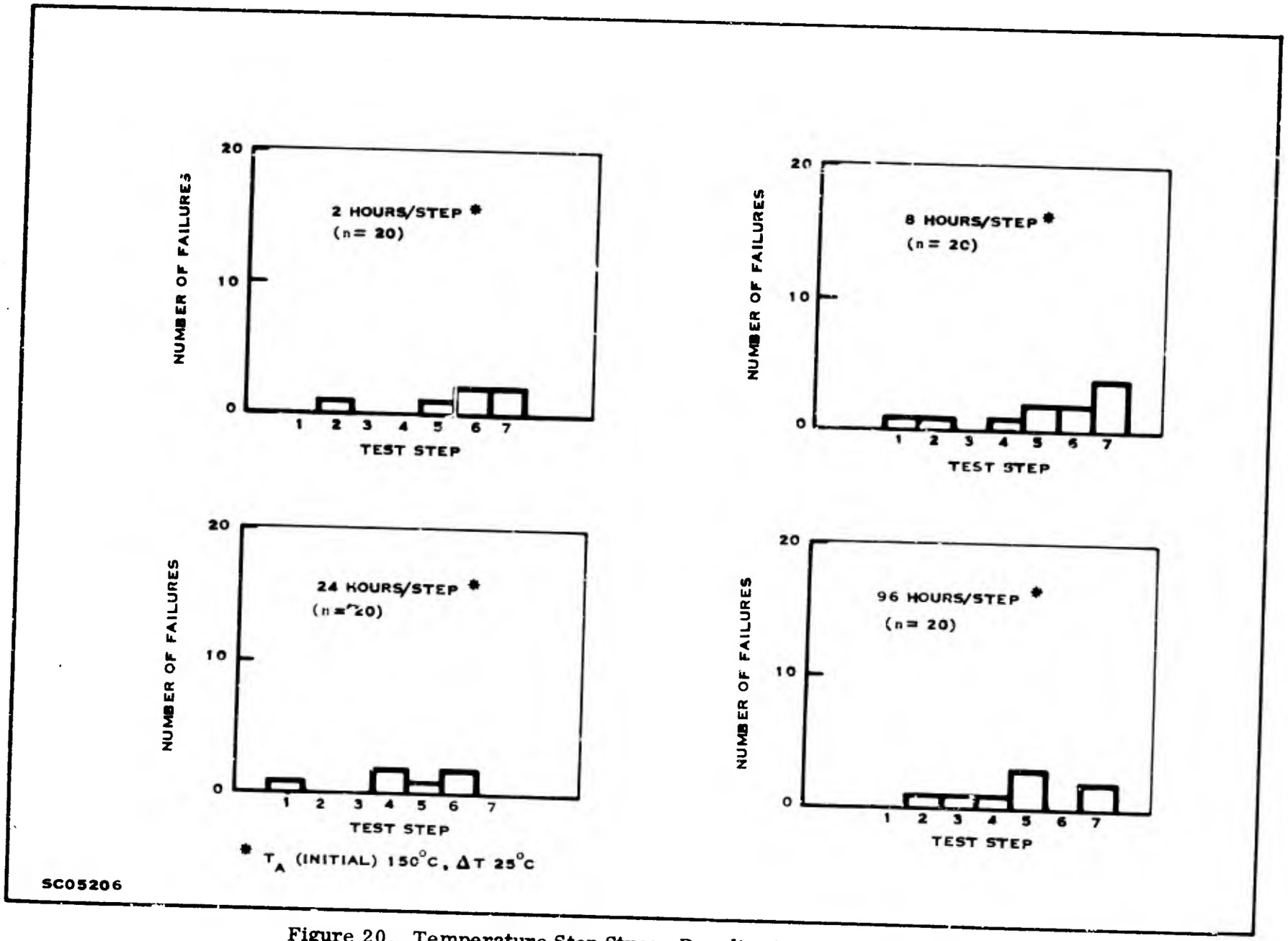

Figure 20. Temperature Step Stress Results (Main Test Program)

d. Reverse Bias Fixed Stress and Reverse Bias Step Stress Tests

In Figure 21 it is observed that the maximum number of failures occurs during one of the final intervals in all three reverse bias fixed stress tests. This maximum occurs between 600 and 768 hours for the 125°C test and between 432 and 600 hours on the 175°C test. On both tests there are relatively few failures until after 264 hours. On the three steps between 96 and 600 hours on the 225°C test there is a maximum number of failures occurring during each step. Complicating an understanding of the results of these reverse bias tests is the appearance of shorts as well as degradation failures. A summary of these is given in Table 10. Additional grouping of failures by test interval and pretreatment group for the three levels of reverse bias is in Tables 18, 19, and 20. Since there were no shorts on the 500 hour reverse bias life test in the Preliminary Test Program, the appearance of shorts on the reverse bias tests of the Main Test Program was not anticipated. It is believed that shorting occurred due to thermal runaway (see Section IV-8b for more detail).

Important failure indicators (Table D-4) on the 125°C tests are all of the leakage parameters and h_{FE} (5 mA). The more important failure indicators on the 175°C test are the 30 V and 70 V, I_{CEO}, readings. The other parameters are equally important as failure indicators with the exception of h_{FE} (1 A). There are the same number of failures on the 125°C and 175°C tests (52 and 53 respectively). Almost all of the devices failed on the 225°C test (89/100). Primary failure indicators on both the Main Test Program and the Preliminary Test Program are h_{FE} (5 mA) and I_{CEO}, both 30 V and 70 V. Almost of equal importance are the two I_{CBO} parameters (30 V and 70 V) as failure indicators. On the 2, 8, and 24 hour reverse bias step stress tests of the Main Test Program (Figure 22), the greatest number of failures occurred on the last test step. However, on the 96 hour step stress test the greatest number of failures occurred during the second step as seen in Table D-3. The more important failure indicators on these stress tests are h_{FE} (5 mA), and the leakage parameters, primarily I_{CEO} both 30 V and 70 V.

Table 10. Summary of Failures for Reverse Bias Fixed Stress Tests (Main Test Program)

Tests	Total Failures	Failures Due to Shorts	Time of Appearance of First Shorts
Reverse Bias 125° C	52	23	600 hours
Reverse Bias 175° C	53	36	432 hours
Reverse Bias 225° C	89	41	264 hours

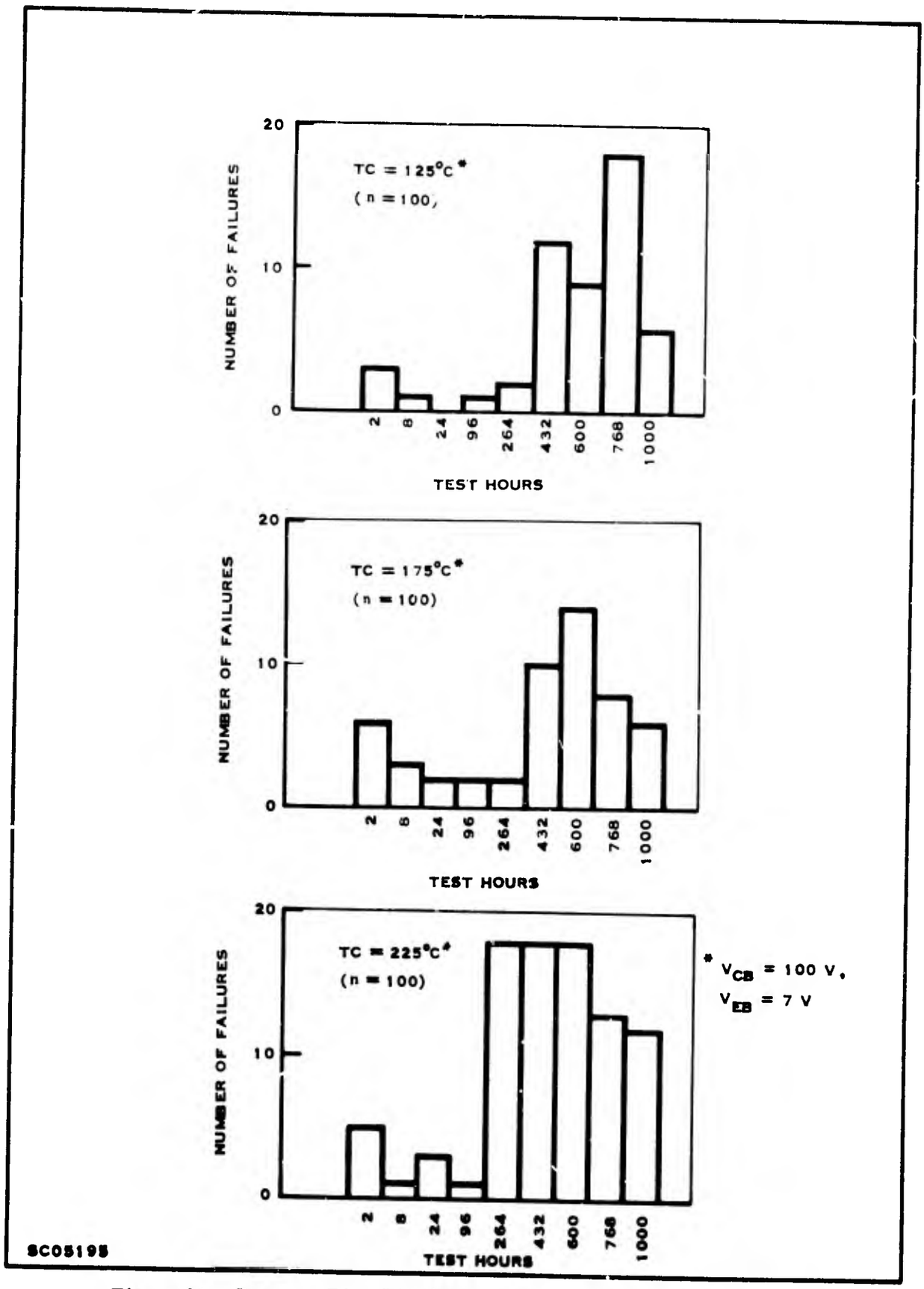

Figure 21. Reverse Bias Fixed Stress Results (Main Test Program)

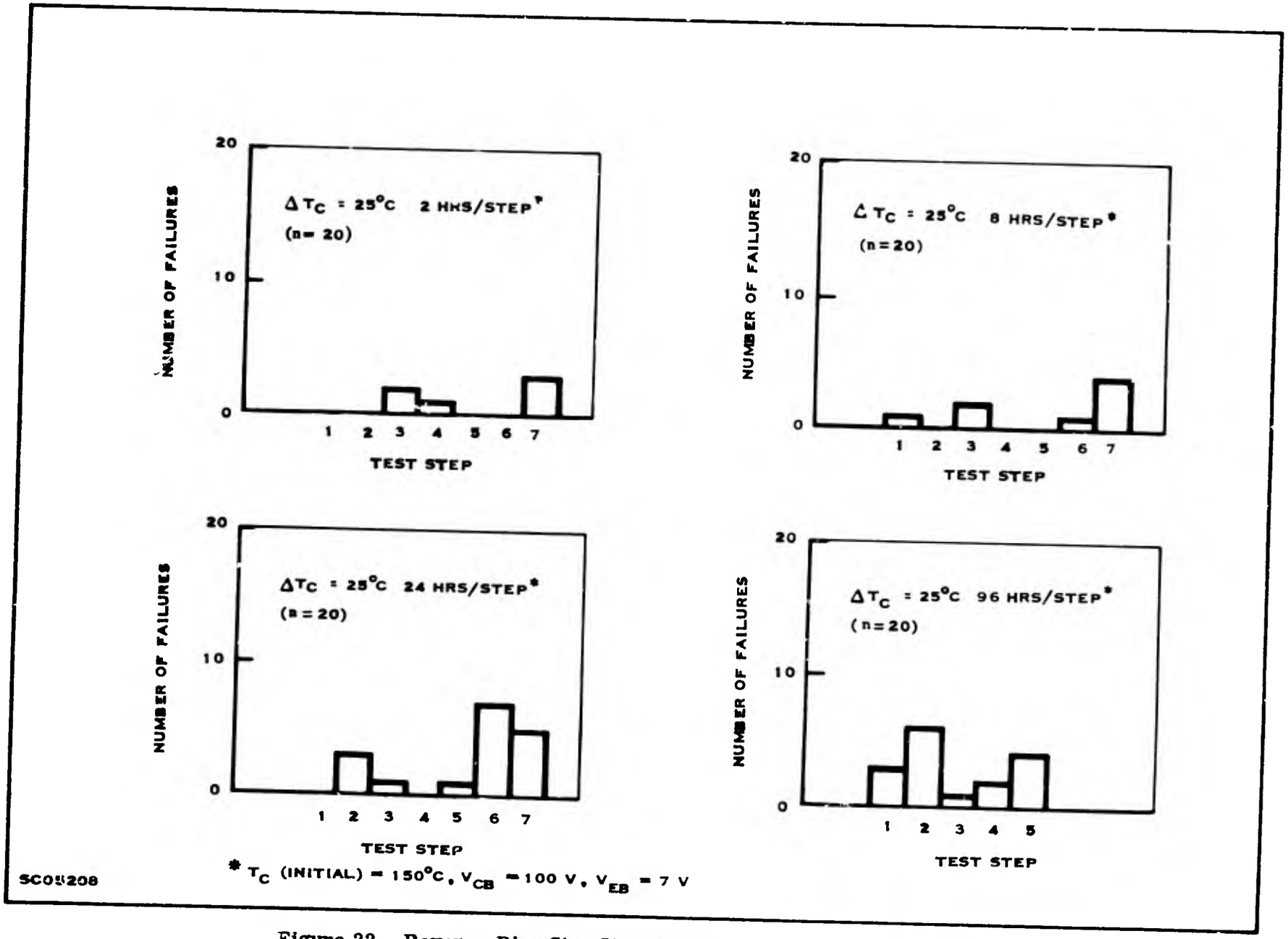

Figure 22. Reverse Bias Step Stress Results (Main Test Program)

On the reverse bias step stress test of the Preliminary Test Program, there was an isolated failure on the first step (Figure 6). The only other failures occurred at the fifth step.

The predominant failure mechanism of the degradation failures appears to be different from that of the devices which shorted as evidenced by the failure analysis results in Section IV-8b.

e. Power Operating Fixed Stress and Power Operating Step Stress Tests

In the power operating fixed stress tests few failures on the 15 W test (Figure 23) are noted. On the 37.5 W test the greatest number of failures for any readout step occurs prior to 2 hours and then there is a decrease in the number of failures for the remainder of the test except for 768 to 1000 hours, when a second maximum occurs. This pattern of the greatest number of failures occurring at the first readout step is quite apparent in the 60 W test. Here 43 percent of the units failed prior to 2 hours.

Results of the power operating test in the Preliminary Test Program are shown in Figure 12. It is seen that most of the failures on this 30 W power operating test occurred during the first 9 hours. There were some failures on the next two steps but after 24 hours there was only one failure on the remainder of the test.

Primary failure indicators (Table D-6) on the 37.5 W test of the Main Test Program are I_{EBO} (5 V), I_{EBO} (8 V) and h_{FE} (5 mA). All of the leakage parameters as well as low current h_{FE} are important failure indicators on the 60 W test but the most important failure indicators are I_{CEO} (70 V) and I_{CBO} (70 V). In comparison, the important failure indicators on the 30 W test in the Preliminary Test Program are low current h_{FE} and all of the leakage parameters. Worthy of note is that on all of the power operating life tests in both the Main Test Program and the Preliminary Test Program there are practically no failures on high-current h_{FE}, V_{BE}, or V_{CE}.

In the power operating step stress tests of the Main Test Program (Figure 23) practically no failures occurred prior to the fifth readout step. The maximum number of failures occurred at the sixth or seventh step and there were relatively few failures after that. Primary failure indicators (Table D-5) on this series were I_{EBO} and low-current h_{FE}. There were practically no failures on high-current h_{FE}, V_{BE} or V_{CE}.

In the power operating step stress test of the Preliminary Test Program practically all of the failures occurred in the third step, the 30 W step (Figure 9). There were no failures at the 40 W, 50 W, or 60 W steps. Primary failing parameters were all of the leakage parameters and low-current h_{FE}.

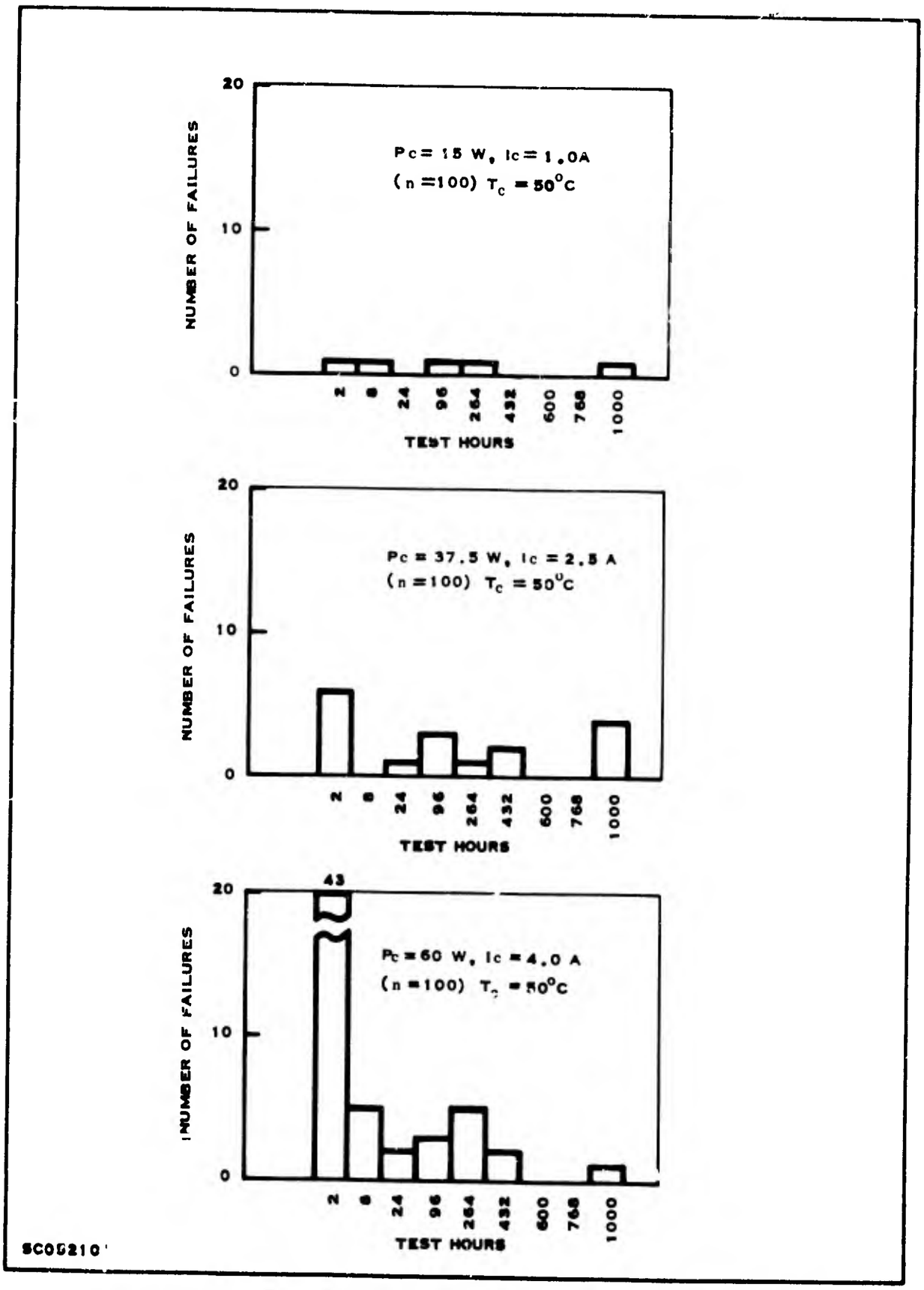

Figure 23. Power Operating Fixed Test Results (Main Test Program)

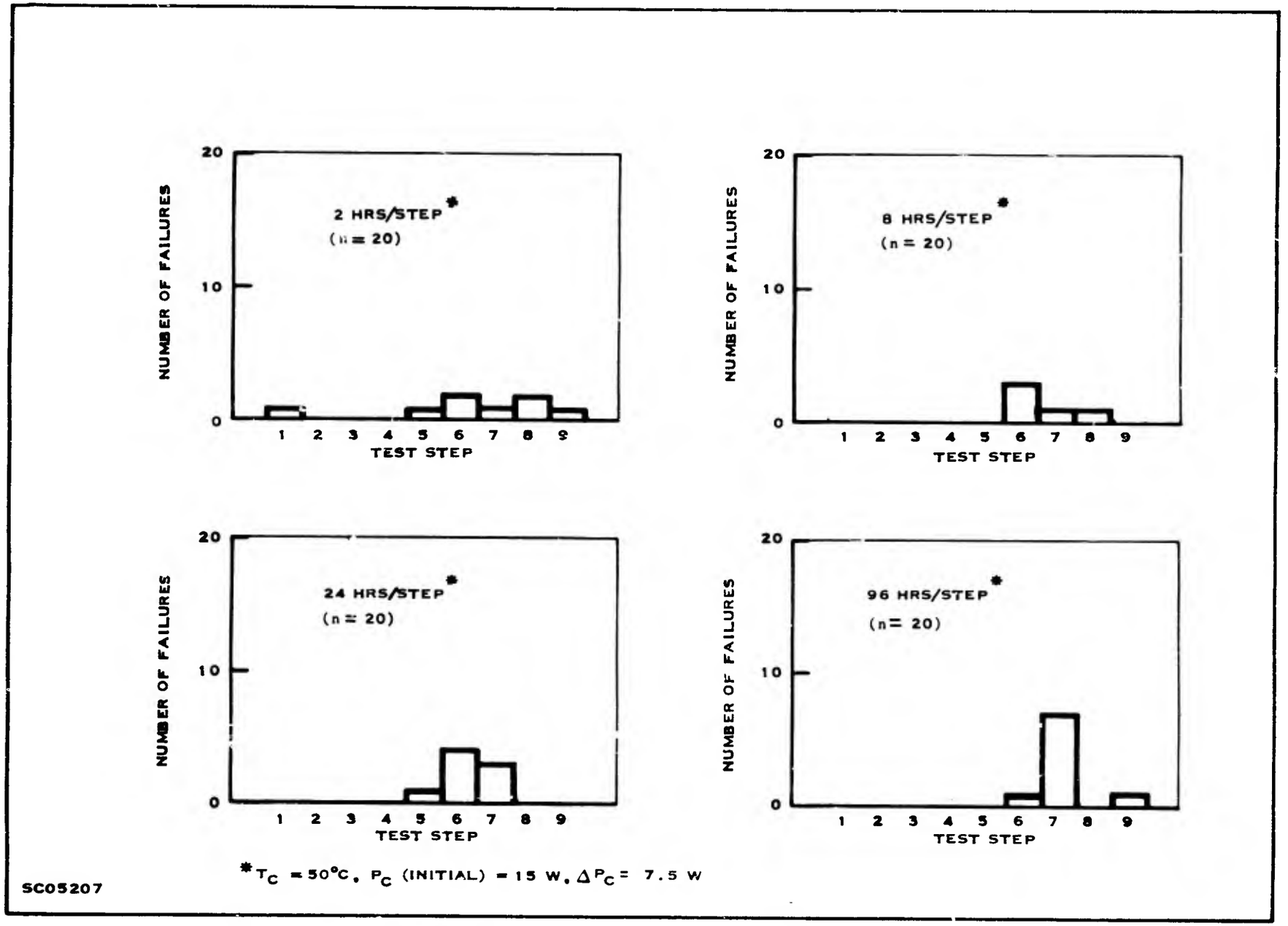

Figure 24. Operating Step Stress Results (Main Test Program)

The difference in behavior of the devices on these power operating tests in both the Main Test Program and Preliminary Test Program is believed to be primarily due to the fact that different values of V_{CE} were used on each test. To recap, V_{CE} = 15 V was used in the Main Test Program and V_{CE} = 20 V was used in the Preliminary Test Program.

f. Summary

Primary failure indicators on all tests in the Main Test Program were h_{FE} (5 mA), I_{CEO} (30 V) and I_{CEO} (70 V). Analysis of degradation failures revealed the presence of temperature voltage induced inversion (TVI), surface contamination and presence of an unknown volatile encapsulated within the device.

On the power operating life tests there were practically no failures on h_{FE} (1 A), V_{BE}, or V_{CE}. This fact supports the conditions selected for the high stress tests.

On the reverse bias tests there are many catastrophic failures (shorts), the initialones occurring from 264 hours (225°C test) to 600 hours (125°C test). It is believed that shorting occurred due to thermal runaway. Further discussion of this failure mode is in Section IV-8b.

All h_{FE} (5 mA) failures in the Preliminary Test Program exceeded the -30 percent change criteria. This was not true on subsequent tests in the Main Test Program, Table 11. Although most of the h_{FE} (5 mA) failures on the power operating and reverse bias tests were -30 percent change failures there were a few which were +30 percent change failures. On the temperature storage tests, however, the mechanism causing increase in h_{FE} (5 mA) values is predominant.

Cause of the -30 percent h_{FE} (5 mA) failures was attributed to entrapment of an extraneous unknown contaminant within the package. For the +30 percent h_{FE} (5 mA) failures, cause is believed to be attributed to a slight channeling present on the emitter-base diode prior to stress which was later removed during stress.

8. FAILURE ANALYSIS RESULTS

Catastrophic failures were removed from stress as they occurred and were candidates for failure analysis. Degradation failures remained on stress until the test was complete. Then certain types of degradation failures became candidates for failure analysis. Both catastrophic and degradation failures were analyzed. These findings are reported by test type. Failure criteria are contained in Table 2.

Table 11. Summary of h_{FE} (5 mA) Failures Which Exceeded ±30 Percent Change (Main Test Program)

Fixed Stress Test	h_{FE} (5 mA) Failures That Exceeded -30% Change Criteria	h_{FE} (5 mA) Failures That Exceeded + 30% Change Criteria
Temperature Storage		
200° C	5	0
250° C	3	17
300° C	15	25
Power Operating		
15 W	1	0
37.5 W	4	3
60 W	18	1
Reverse Bias		
125° C	8	2
175° C	5	1
225° C	10	6

a. Temperature Storage Tests

The primary failure modes for catastrophic failures were:

- Delamination of the die
- Weld flange separation
- Post-to-wire weld separation
- Cracked dies

The preponderance of failures occurred on the 300°C temperature storage fixed stress test. All four failure modes listed above occurred in samples that had been stressed at 250°C or above. However, only the latter failure mode was observed on the 200°C temperature storage fixed stress test.

Examination of units that failed due to delamination of the die revealed separation at the interface of the collector nickel plate and the solder. Visual examinations were made to determine whether or not the separation occurred within the nickel plate or at the nickel-solder interface. However, these were unsuccessful.

Analysis of weld flange failures indicated that the modes were primarily due to formation of gold-lead eutectic beneath the die. Subsequently the gold on top of the header was absorbed by the eutectic to the extent that this compound migrated over the header primarily in those devices which were stored on their side. In many cases the gold at the can flange-weld interface was absorbed by the migrating eutectic causing the units to be gross hermetic seal leakers. In some cases the cans came off the headers. For this failure mode to occur, at least three conditions must be met: can attachment must be by fusion to the gold plate rather than welding to the weld ring (both types are good hermetic seals); the gold plate on top of the header must be thicker than the maximum indicated in the header plating specification; and the temperature must exceed the 215°C gold-lead eutectic for an extended period of time.

In the case of failures due to a cracked die, two observations were made: (a) All units were from group 3 power operating pretreatment, and (b) threads were either damaged or the top surface of the hex shoulder was deformed. It is suspected that the treatment which causes such damage to the stud imparted a permanent mechanical stress on the die, and subsequently the die cracked during thermal stress.

Several failures analyzed were found to have open emitter wires at the post. In all cases the wire had been poorly welded to the post as evidenced by the small weld nugget remaining after the emitter wire had separated from the post.

Representative samples of failures as indicated by degradation parameters such as I_{CEO}, I_{CBO}, I_{EBO}, h_{FE} (5 mA), $V_{BE(sat)}$, $V_{CE(sat)}$ were analyzed. The failure modes for some of these could not be determined. The failure modes of the others were:

- Contamination on die or in oxide
- Defective hermetic seal
- Unknown volatile encapsulated within device
- Slight channeling of the diodes prior to stress

Some of the devices from the fixed stress tests which exceeded the current leakage failure criteria were brought back into specification after decanning and cleaning of the dies. This indicated that the cause of failure was due to contamination on the die, in the oxide or both. Several of these failures were found to be hermetic seal failures (radiflo analysis). However, it was not possible to ascertain the degree of influence the poor hermeticity had on degrading the electrical parameters.

The failures due to h_{FE} (5 mA) exceeding the ±30 percent criteria were found to be due to two different mechanisms. In the case where low level h_{FE} exceeded the +30 pe ent criteria the parameter continued to be out of specification even after decanning and surface cleaning of the dies. This type of failure is believed to be attributed to slight channeling present on the emitter-base diode prior to stress. During the temperature storage test, h_{FE} (5 mA) increased due to dissipation of these channe In or turn the +30 percent failures to "in-specification" values, the conditions causing channels would have to be re-established. However, in the case where low level h_{FE} exceeded the -30 percent criteria, it was found that h_{FE} (5 mA) was within specification after 12 hour exposure of the decanned devices to room ambient. This type of failure is attributed to entrapment of an extraneous unknown contaminant. This was apparently a volatile contaminant as h_{FE} degraded negatively during storage life. This contaminant quickly dissipated during the 12 hours after decanning of the devices.

b. Reverse Bias Tests

Catastrophic failures were analyzed and confirmed to have all junctions shorted. Many of the devices exhibited excessive voiding beneath the dies. This failure mode is called eutectic shorting. As pointed out in the previous section, failure times of the devices were different. This is due to: inherent differences of reverse breakdown voltage and leakage, voiding, both in number and size, and also due to differences in thermal resistance (θ_{J-C}) of the devices.

It is believed that shorting occurred due to carriers thermally generated within the silicon die. The explanation follows: increasing numbers of carrier electrons are freed when the temperature of a silicon die is raised. With devices subjected to high reverse bias conditions at elevated temperatures, a significant portion of the total leakage current is due to these thermally generated carriers. This current leakage in turn generates additional carriers due to the increased dissipation of the device. The effect is cumulative, and when the critical temperature of the silicon die is reached the current concentrates. The temperature in that area quickly increases to the point when the lowest eutectic is reached, flow-through occurs.

The effect of temperature on carrier generation is illustrated in Figure 25. These data were obtained from three devices. Each device was stabilized at several temperatures. The decreasing BV_{CBO} and BV_{EBO} values at a constant 100 μA were obtained by pulse reading on a curve tracer. It can be seen that breakdown voltages rapidly approach zero at temperatures of 225°C or above.

Some of the devices which had exceeded the degradation leakage parameter limits were analyzed. As anticipated, a number of these failures were determined to be temperature voltage induced inversions (TVI) of the base regions. Analysis consisted of measuring the forward E-B and C-B bias currents at low voltages (20 mV, 50 mV, 100 mV, 150 mV, etc. to 450 mV) which was followed by plotting these data

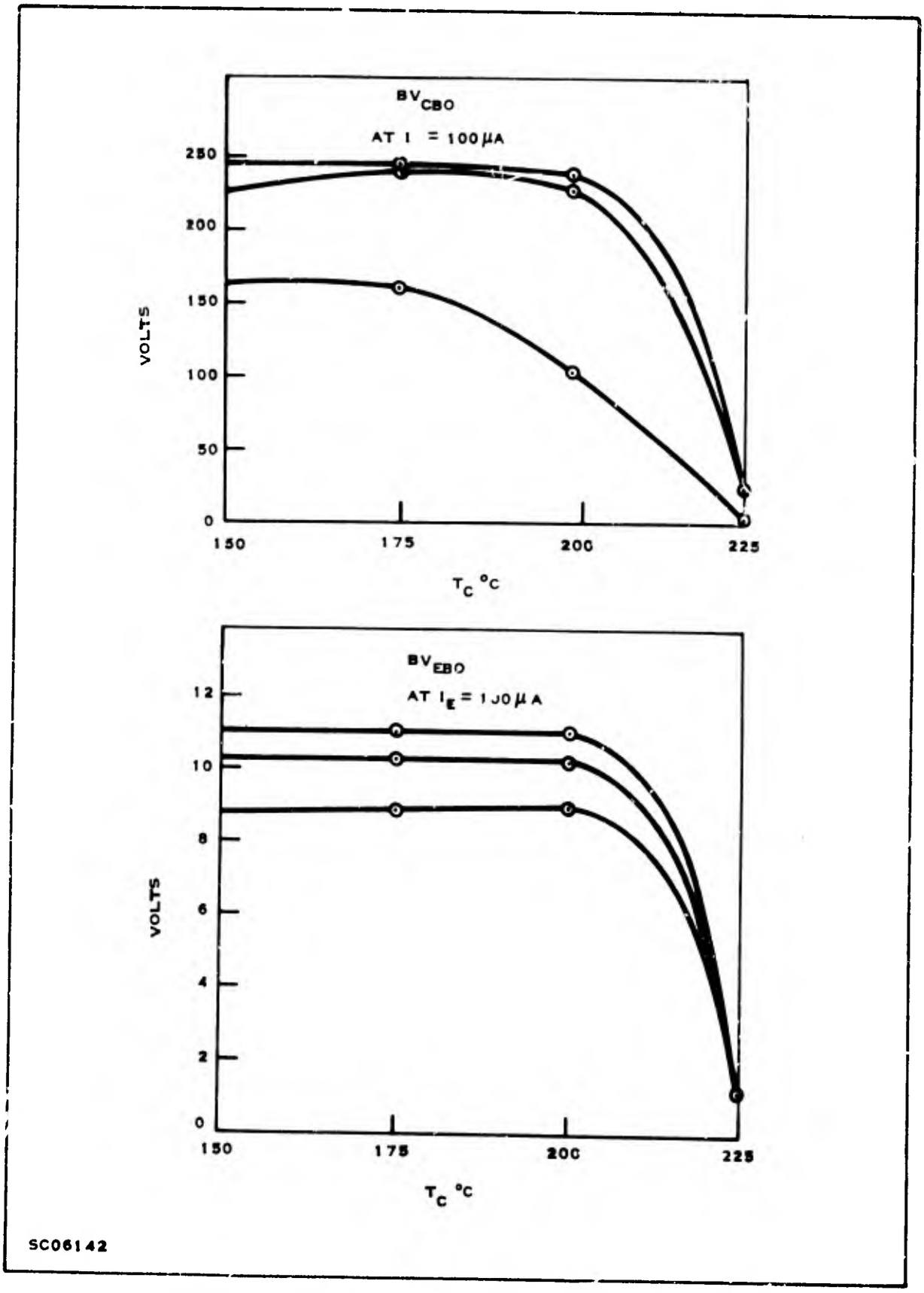

Figure 25. Change of Breakdown Voltage at Constant Current versus Case Temperature (T_C)

on semi-log paper. Curvatures of the initial E-B and C-B plots are indicative of channeling, characteristic of TVI. The post bake forward bias curves were much more linear, which indicated some dissipation of the inversions. In addition, low and high level h_{FE} readings were made before and after bake. Low level h_{FE} increased after bake. This further substantiated that channeling was being dissipated.

The remaining degradation failures were believed to have been due to surface contamination and/or bulk defects, as they did not respond to the above procedure in the same fashion.

c. Power Operating Tests

There were only three catastrophic failures on the power operating tests. These were primarily caused by voids which increased the temperature in a localized area thus resulting in burn-out. This failure mode is thermal runaway. More of these catastrophic failures may have occurred had it not been for the individual electronic control for each device (Appendix A). Analysis of the data indicated that the degradation failures were of the general type discussed under the other tests.

d. Summary

(1). Temperature Storage Tests

Most catastrophic failures occurred on the 300° C stress. These failures were: delamination of the solder, weld flange separation, post-to-wire weld separation, and cracked dies Failures that were due to degradation of parameters were: contamination on die or in oxide, defective hermetic seal, unknown volatile encapsulated within device, and slight channeling of the diodes prior to stress.

(2). Reverse Bias Tests

Many catastrophic failures were due to voiding beneath wafers causing shorting. Other catastrophic failures were found to be due to thermally generated carriers within the dies causing shorting. Failures that were due to degradation of parameters were temperature voltage induced inversions (TVI) and surface contamination and/or bulk defects.

(3). Power Operating Tests

The few catastrophic failures that occurred were due to thermal runaway caused by voiding beneath dies. Degradation failures were of the same general types already discussed.

SECTION V

VERIFICATION TEST PROGRAM

1. DESCRIPTION

The Verification Test Program (VTP) which is discussed in this section was conducted after completion of the Main Test Program (MTP) (discussed in Section IV). The objectives and conclusions are discussed first. These are then followed by a discussion of test description, data analysis and results, and failure analysis.

2. OBJECTIVES

The objectives of the VTP were to determine if the results obtained in the MTP using device A (Figure 1) could be generalized and applied to related types of silicon planar power transistors. Specifically the approach was aimed at the following:

- Verify the best nondestructive screening procedures derived from all previous tests.
- Determine acceleration factors and compare them with results obtained in the MTP.
- Determine activation energy (E_A) and compare the results with those obtained in the MTP.

3. CONCLUSIONS

The computer program SERF was used successfully to isolate the preindicators of failure. However, the preindicators of failure found in the VTP are not the same as those found in the MTP (discussed in Section VII.) In some cases different parameters are isolated as preindicators of failure, and even for those parameters which are the same there is a different level of screening. This suggests that the knowledge of the preindicators of failure of one device is not necessarily the same for another device with the same generic number if both devices are fabricated by different processes. Predicted failures are compared against a pre-established failure criteria using SERF and these failure criteria may not be the same for devices with the same generic number when made by different processes. However, if the failure mechanisms are understood and the stresses for accelerating them are determined, then the knowledge of the preindicator of failure can be applied to all devices with the same generic number.

The 10,000 G constant acceleration screening test was effective in removing mechanically weak units. Failure analysis found that the failures (opens) were due to weak post-to-wire welds. Prior to failure, on this mechanical test there was no indication of any anomalies in the electrical parameters measured.

Power operating pretreatment appears to stabilize the device. This was also observed in the MTP. The same percentage of devices exceeded the degradation limit for I_{EBO} (5 V) and I_{EBO} (8 V) on both the MTP and VTP.

Acceleration factors and activation energy are discussed in Section VI. In most cases the results are comparable with those obtained on the MTP.

The primary failure parameters on the temperature storage life test were h_{FE} (5 mA) and I_{CEO}. On the power operating life tests they were I_{EBO} (5 V), I_{EBO} (8 V) and h_{FE} (5 mA). In both the VTP and MTP all low current gain failures exceeded the -30% change criteria except on the temperature storage life tests of the VTP which was just the opposite. Section V-6 gives an explanation for the change in low current gain but does not explain the opposite effects obtained in the two test programs.

Most of the failure modes in the VTP and MTP are the same. Some different failure modes observed on the VTP are faulty collector nickel plate and delamination of gold plate from molybdenum substrate.

Attempts to relate power operating life test results to temperature storage life test results were reasonably successful. This was accomplished by determining the individual junction temperature of the devices on the power operating life tests and grouping according to junction temperature. From this data cumulative percent failure curves are obtained similar to those of the storage tests.

4. TEST DESCRIPTION

The VTP was similar to the MTP (discussed in Section IV) but of lesser scope. It consisted of three separate tests:

a) Pretreatment

b) 100 percent Mechanical Screen

c) Life Matrix.

A block diagram of the VTP is shown in Figure 26. A discussion of each test is presented below.

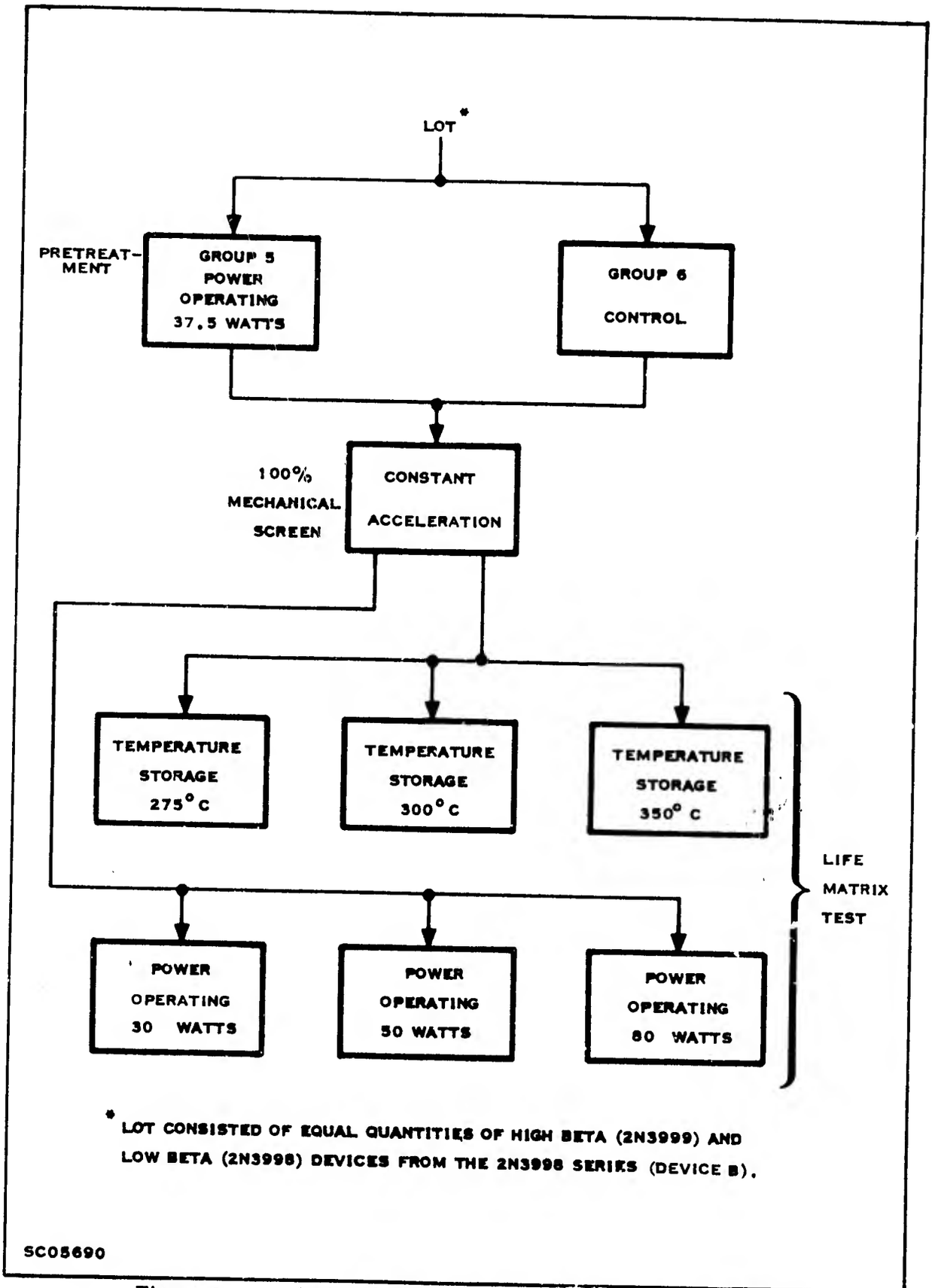

Figure 26. Block Diagram of the Verification Test Program

The silicon planar power transistor used in the VTP was device B which is depicted in Figure 1. It differed slightly from device A used in the Main Test Program. A description of device B, along with a discussion of related parameters and failure criteria are contained in Section III.

a. Pretreatment Test

The pretreatment test used was a 96 hour power operating type test. It was chosen because the MTP data, which is summarized in Table 8 indicated that the power operating pretreatment test was more effective in screening out the weaker units than either of the other two pretreatment tests. As will be pointed out in Section V-4c, the V_{CE} for the power operating life test was increased from 15 V (used in the MTP) to 20 V. The collector-to-emitter voltage of the pretreatment test was 15 V rather than 12 V which was used in the MTP. The V_{CE} was changed in order to maintain the pretreatment voltage stress approximately 80% of that used in the life tests. The test conditions for the pretreatment test are in Table 12.

Table 12. Pretreatment Test Conditions (Power Operating — Group 5) (Verification Test Program)

Parameter	Condition
V_{CE}	15 V
I_C	2.5 A
P_C	37.5 W
T_C	100°C

b. 100 percent Mechanical Screen Test

As in the MTP, 10,000 G constant acceleration was used to remove mechanical "rogue" failures thus assuring the mechanical integrity of the lot. All units (Groups 5 and 6) were subjected sequentially to this stress in both the X_1 and Y_1 planes (Table 5) after the pretreatment test and post test parameter measurements.

c. Life Matrix Test

After the 100 percent mechanical screen test the 300 units were divided into 6 samples of 50 units each containing equal quantities of high h_{FE} (2N3999) and

low h_{FE} (2N3998) devices from the 2N3998 series (device B, Figure 1). These were then placed on life test as described in Table 13. At least one cell in each of the life tests had the same test conditions as a cell in a similar test in the MTP. These were cell No. 2 of the temperature storage life test and cells No. 2 and 3 of the power operating life test (Same T_J's as the 37.5 W and 60 W test of the MTP respectively).

Table 13. Life Matrix Test Conditions
(Verification Test Program)

Test Type	Cell 1	Cell 2	Cell 3
Temperature Storage	T_A = 275°C 1000 hrs (n = 50)	T_A = 300°C 1000 hrs (n = 50)	T_A = 350°C 1000 hrs (n = 50)
Power Operating T_C = 50°C	P_C = 30 W V_{CE} = 20 V 1000 hrs (n = 50)	P_C = 50 W V_{CE} = 20 V 1000 hrs (n = 50)	P_C = 80 W V_{CE} = 20 V 1000 hrs (n = 50)
Readout Intervals (Cumulative Time on Stress)	0 2 8 24 96 432 1000 hrs		

Temperature Storage

The upper storage temperature of 350°C (Table 13) was chosen as it was the maximum temperature that could be imparted on the device without creating threshold failures. A higher temperature was not possible because the melting point of the Au-Ge solder used to mount the chip to the header is 356° C. The 300° C temperature storage condition was selected, as mentioned previously, to permit direct comparison of the performance of device B and device A under conditions of similar stress. The 275° C temperature storage condition was selected to be midway between two levels (250° C and 300° C) of the temperature storage stress employed in the MTP. It was also the same temperature used in the temperature storage life test used in the Preliminary Test Program (PTP) (Section II) for stressing device A.

Power Operating

As indicated in the thermal studies which are discussed in Section VIII the maximum temperature of the junction is very dependent on V_{CE} as depicted by isothermal maps of Figure 65 and Figure 66. From similar type data at different values of V_{CE} the characteristic curve of T_{J-max} versus I_C in Figure 27 was generated for device A used in the Main Test Program. A similar characteristic curve (Figure 28) was generated for device B used in the VTP. In an attempt to stress device B at an equivalent stress as device A so that the results could be readily compared, it was necessary to have a common parameter. The parameter selected was T_{J-max}. In determining T_{J-max} for device A the conditions for the 15 W power operating test in the MTP (V_{CE} = 15 V and I_C = 1.0 A) were used in conjunction with Figure 27, thus the indicated T_{J-max} was about 146° C at T_C = 100° C.

It is seen from Figure 28 that the approximate conditions under which device B should be stressed for equivalent thermal stress as device A are V_{CE} = 21 V and I_C = 1.0 A. However, as a good approximation V_{CE} of 20 V was used for all the power operating life tests in the VTP. These test conditions are listed in Table 13. The 30 W test was selected so that one of the power operating life tests was within the maximum rating of the device. In this case device B, when operating at 30 W (V_{CE} = 20 V) has a lower T_{J-max} than device A when it operated at 37.5 W (V_{CE} = 15 V) in the MTP. Both the 50 W and 80 W tests were selected so that direct comparison could be made with the results of the 37.5 W and 60 W test respectively of the MTP.

5. DATA ANALYSIS AND TEST RESULTS

The techniques developed, using the Computer Program SERF, to analyze the data generated in the MTP were applied to the data resulting from this program. These results are discussed together with those of the MTP in Section VI (Accelerated Test Results) and in Section VII (Nondestructive Screening). A brief discussion of bar graphs and failing parameters is presented here by test.

a. Pretreatment

Six percent of the devices exposed to the power operating pretreatment failed during pretreatment. This is summarized in Table 14. The same percentage of devices were eliminated during power operating pretreatment in the MTP. In both cases the primary failing parameters were I_{EBO} (5 V) and I_{EBO} (8 V).

b. 100 percent Mechanical Screen (Constant Acceleration)

The constant acceleration stress prior to the life matrix test caused 3.2 percent of the control sample and 3.5 percent of the pretreatment sample to exceed

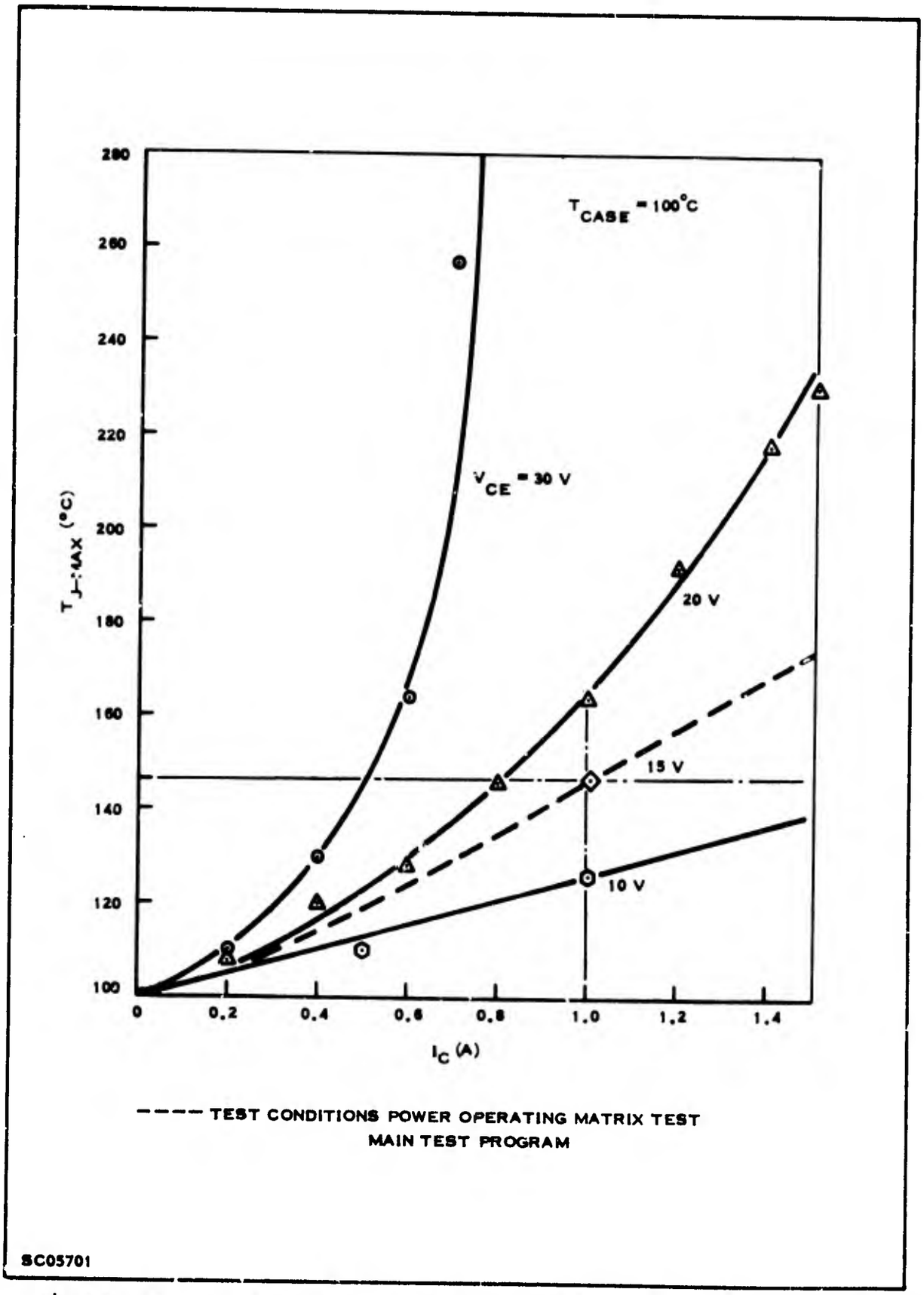

Figure 27. Maximum Temperature of Device A (Using an IR Radiometer) as a Function of Collector Current (I_C) for Several Constant Values of Collector-to-Emitter Voltages (VCE)

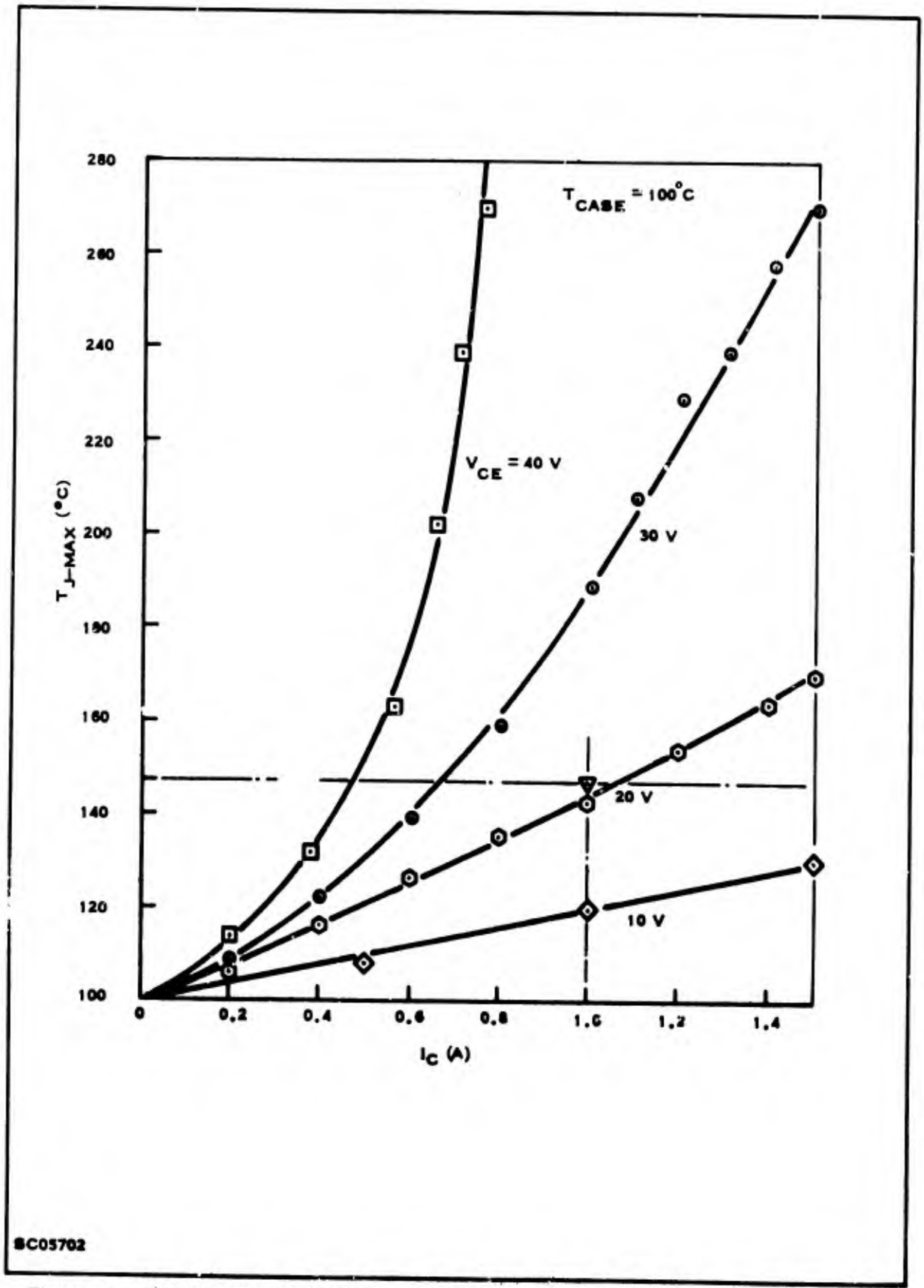

Figure 28. Maximum Temperature of Device B (Using an IR Radiometer) as a Function of Collector Current (I_C) for Several Constant Values of Collector-to-Emitter Voltages (V_{CE})

Table 14. Summary of Failures in Pretreatment Tests
(Verification Test Program)

Pretreatments Stress		Total Failures	List of Failing Parameters									
			I_{CEO} (30 V)	I_{CEO} (70 V)	I_{CBO} (30 V)	I_{CBO} (70 V)	I_{EBO} (5 V)	I_{EBO} (8 V)	h_{FE} (5 mA)	h_{FE} (1.0 A)	V_{BE} (sat)	V_{CE} (sat)
Control (Group 5) No Pretreatment n = 150		0	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Power Operating T_C=100°C, V_{CE}=15 V, I_C=2.5 A (Group 6) n=150		9			1		8	5	1	1	1	1
Constant Acceleration 10,000 G X_1 & Y_1 planes 1 min per plane	Group 5 n=150	4	1	1	1	1			1	2	2	3
	Group 6 n = 150	5			1	1			3	4	3	4

the parameter degradation limits. (For purposes of comparison it is noted that in the Main Test Program the same stress caused only 1.5 percent of the control sample and none of the power operating pretreatment sample to exceed the parameter degradation limits.) Primary failure indicators for the devices which failed the control acceleration stress were h_{FE} (5 mA), h_{FE} (1 A), $V_{BE(sat)}$, and $V_{CE(sat)}$ in all cases. The values for these parameters were exceedingly high and subsequent stress caused the devices to exhibit an open in all cases. (On any other test program the units would have been removed prior to the next stress.) As shown in Section V-6 these failures were due to weak post-wire welds; thus this test accomplishes its objective.

c. Temperature Storage Life

Bar graphs depicting failures at each readout step for the temperature storage life test are contained in Figure 29. Note that the maximum number of failures on the 275° C test occurs between 8 and 24 hours. In the 300° C test there is a decrease in the number of failures per readout step from an initial high to approximately a constant number of failures per step for the remainder of the test. By far the largest number of failures occur on the initial step of the 350° C test, then there is a sharp decrease in the number of failures with another maximum, however, occurring between 96 and 432 hours. The cause for this sharp increase in failures was found to be due to faulty collector nickel plate (Section V-6).

In the 275° C test an interesting fact is that the number of h_{FE} (5 mA) failures (Appendix D, Table D-7) increases to a maximum at the third step and then decreases afterwards. There is roughly a constant number of h_{FE} (5 mA) failures on the 300° C tests after an initial high number of h_{FE} (5 mA) failures. Analysis of failures and of the data history of each failed device did not reveal the cause of such behavior.

The primary failure indicators (Table D-12) are h_{FE} (5 mA) and I_{CEO}. However, in the case of the 350° C test, we note also that the I_{CBO} parameters are important failure indicators. There were many more devices which exceeded the h_{FE} (5 mA) + 30% change criteria. These are summarized in Table 15. The opposite was observed in the MTP as pointed out previously in Section IV-7. The mechanism causing the h_{FE} (5 mA) failures is discussed in Section V-6.

d. Power Operating Life

There is a gradual increase in the number of failures per step on the 30 W test (Figure 30, a maximum occurring between 96 and 432 hours. There is roughly a constant number of failures occurring during the first 432 hours of the 50 W test. The greatest number of failures occurs between 432 and 1000 hours; it does not occur at the first readout step as it does on the 15 W and 37.5 W power operating test in the

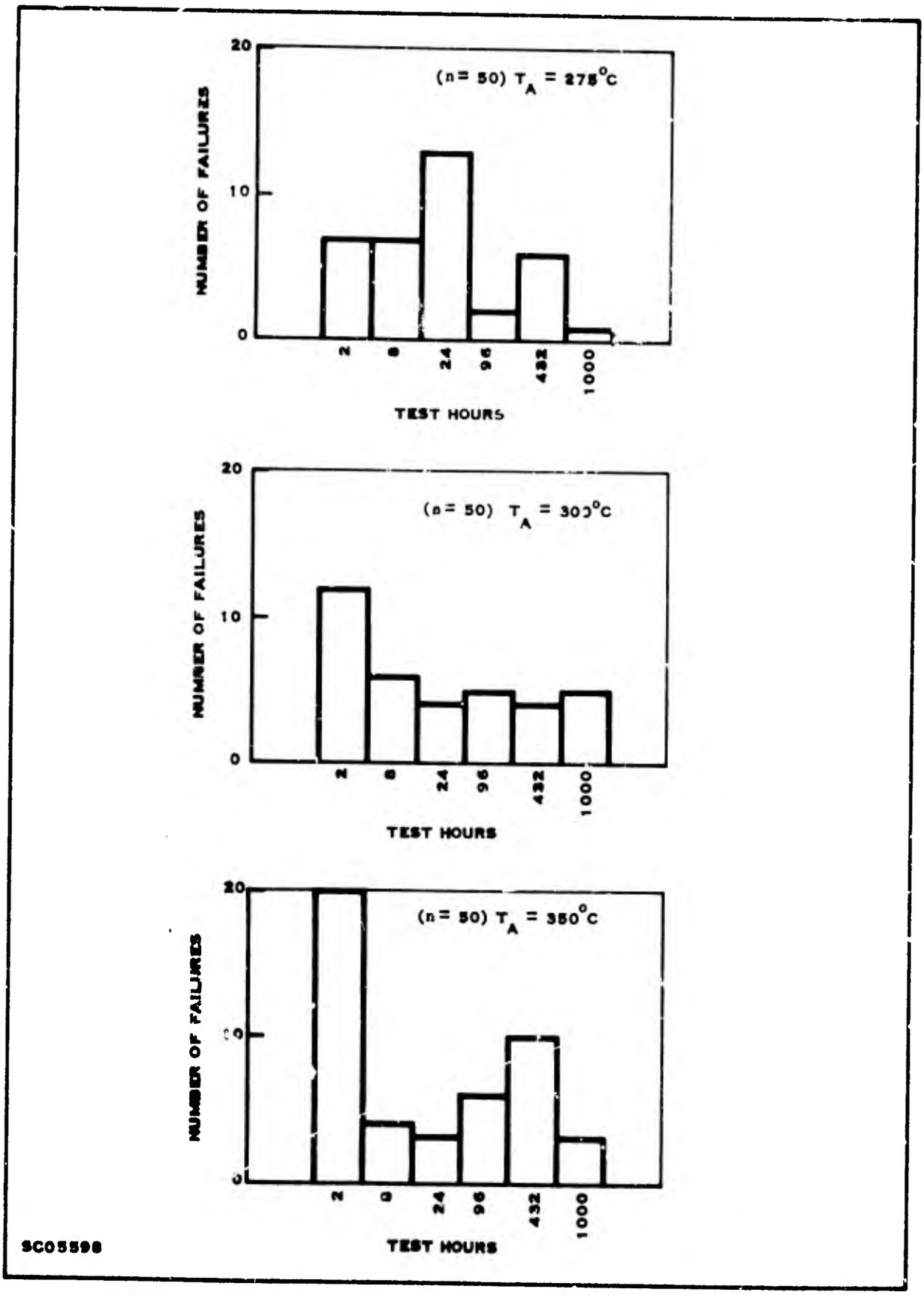

Figure 29. Temperature Storage Life Results (Verification Test Program)

Table 15. Summary of h_{FE} (5 mA) Failures Which Exceeded the ±30% Failure Criteria (Verification Test Program)

Life Test	h_{FE} (5 mA) Failures That Exceeded -30% Criteria	h_{FE} (5 mA) Failures That Exceeded +30% Criteria
Temperature Storage		
275°C	21	4
300°C	19	7
350°C	24	7
Power Operating		
30 W	2	3
50 W	7	1
80 W	8	1

MTP (Figure 8). The greatest number of failures occur prior to 2 hours, but there is not such a sharp decrease afterwards. Furthermore, there is a secondary maximum almost as large as the initial maximum.

It is very interesting that by far the primary failing parameters (Table D-12) on the three operating tests are I_{EBO} (5 V), I_{EBO} (8 V) and h_{FE} (5 mA). A total of 91 devices on all three tests failed by exceeding at least one of these three parameter limits; only 9 devices exceeded all the other parameter limits. As in the temperature storage life test, there were more -30% h_{FE} (5 mA) failures than +30% h_{FE} (5 mA) failures, see Table 15. This was also noted in the MTP as pointed out in Section IV-7. The mechanism causing degradation failures is discussed in Section V-6.

e. Summary

There were the same number of failures in this pretreatment as were observed in the MTP pretreatment. About the same percentage of pretreated devices failed the 100 percent mechanical screening. These failures were found to be weak post-wire welds which opened during constant acceleration.

Equal populations of high and low beta units (Figure 26) were used on each test in the VTP. It was observed that high beta units tended to dominate the failures on most tests failing on the -30% h_{FE} (5 mA) change criterion.

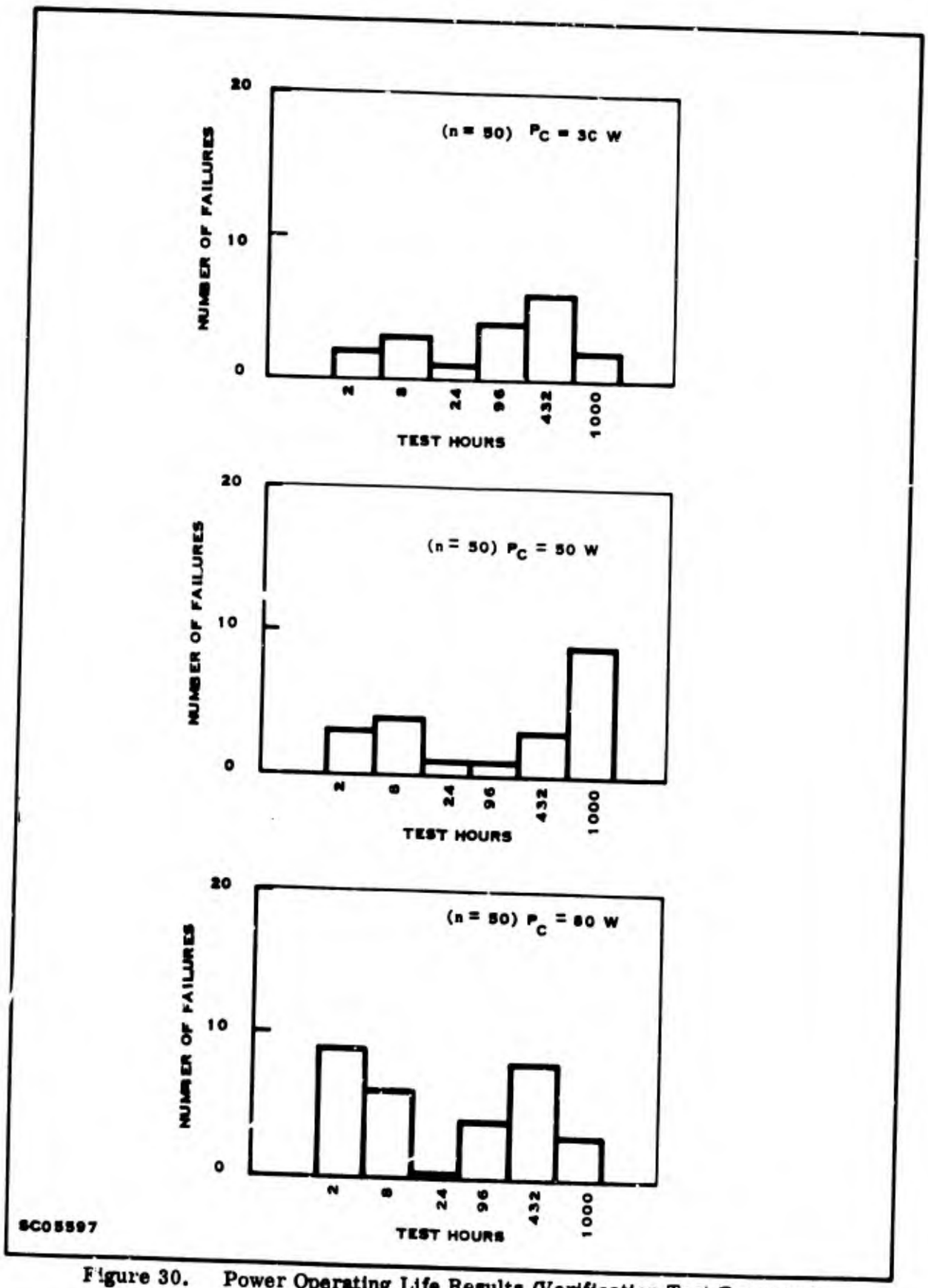

Figure 30. Power Operating Life Results (Verification Test Program)

The primary failure indicators on the temperature storage life test were h_{FE} (5 mA) and I_{CEO}. There were many more devices which failed the h_{FE} (5 mA) -30% change criteria than failed the +30% change criteria. This is opposite to the situation in the MTP. Failure analysis (Section V-6) provides an explanation for the change in low level h_{FE} but not for the opposite effects obtained in the two test programs. The fact that device A was used in the MTP and device B was used in the VTP could account for the difference in this behavior but the reason is not apparent.

Most of the failures observed on the power operating life test were due to I_{EBO} (5 V), I_{EBO} (8 V), or h_{FE} (5 mA). Only 10 percent of the total failures did not exceed the failure limits on one of these parameters. There were more failures due to -30% change in h_{FE} than to +30% change in h_{FE}. This same h_{FE} failure pattern was noted in the MTP.

6. FAILURE ANALYSIS RESULTS

Catastrophic failures were removed from stress as they occurred and were candidates for failure analysis. Degradation failures remained on stress until the test was complete. Representative samples were selected and analyzed by the Failure Analysis Laboratory. These findings are reported by test type. Failure criteria are contained in Table 2.

a. 100 percent Mechanical Screen (Constant Acceleration)

Analysis of constant acceleration test failures showed them to have either open emitter or open base wires at the post weld. Prior to failure, the electrical parameters measured did not indicate any anomalies. This would suggest that initially the wire-to-post weld was electrically good but mechanically weak. Additional support to this argument was the fact that the wire was properly formed which indicated that the welding pressure was applied, although very little evidence of welding was apparent on the post. Also, analysis of failures on the other verification tests allows the postulate: the tube shearing force mechanism (described in Section V-7b) responsible for post-to-wire weld opens on life tests also contributed to the opening of welds which were screened out by this test.

b. Temperature Storage Tests

The primary failure modes for catastrophic failures were:

- Faulty collector nickel plate.
- Delamination of gold plate from molybdenum substrate.

Most catastrophic failures were due to faulty collector nickel plate. All of these failures occurred between 96 and 432 hours storage at 350° C. Migration of gold through the silicon die was believed to be the mechanism of failure. Apparently the gold found entry to the silicon surface via small defects (pinholes, blisters, etc.) in the collector nickel plating and subsequently migrated through the silicon to the emitter-base region where the junctions were shorted. Results of this migration are shown in the photograph of a microsection through the shorted area (Figure 31B). A top view of the failure is shown in Figure 31A. The build-up of metallization (gold-aluminum) on the top of the die which resulted from the gold migration through the die is visible in both photographs. The failure mechanism was not believed to be due to alloying as formation of gold-silicon eutectic occurs at 370° C. Verification of oven temperature showed that it remained within the 350° C ±3° C specification. Similarly, the failure mechanism was not due to molten gold-germanium (eutectic is 356° C). This would have caused failures to occur in a much shorter period of time.

The other catastrophic failures were due to delamination of the gold plate from the molybdenum substrate. These failures occurred between 96 and 432 hours storage at either 300° C or 350° C. There was no parameter degradation on the devices at the 96 hour readout interval but they were shorted at the 432 hour readout interval. After decanning, the die and posts (Figure 1) were loose from the headers. The gold plating peeled from the molybdenum substrate where wafer and post separations occurred. It is postulated that the high temperature stress caused separation of the gold plate-to-molybdenum substrate interface. This may have been due to unclean plating surfaces. Subsequently, during the parameter measurements, particularly h_{FE} (1 A), the die was shorted due to excessive temperature.

Representative samples of I_{CEO}, I_{CBO}, I_{EBO}, h_{FE} (5 mA) and V_{BE} degradation failures were analyzed. The failure modes determined were:

- Contamination on die or in oxide.
- Defective hermetic seal.
- Slight channeling of the E-B diodes prior to stress which then dissipated under stress.
- Unknown extraneous contaminant encapsulated within device.
- Post-to-wire weld degradation.

Some of the devices which exceeded the current leakage failure criteria were brought back into specification by decanning and cleaning of the dies. This indicated that the cause of failure was due to contamination on the die, in the oxide, or both.

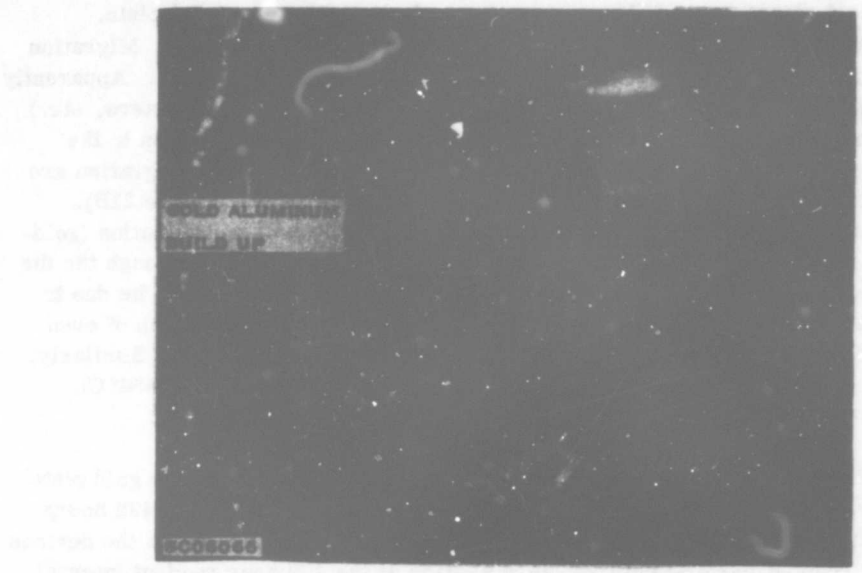

Figure 31B. Microsection of 350°C Storage Failure through Section B-B Showing Migration of Gold through Die

One degradation failure was found to be a gross leak hermetic seal failure. Microscopic analysis revealed that the glass used to seal the tubes into the can had cracked through to the device interior. Cracking of the glass probably occurred during the 350° C temperature storage tests.

The failures on the three storage tests (275° C, 300° C and 350° C) which were due to h_{FE} (5 mA) exceeding the ±30 percent criteria were found to be due to two different mechanisms: 1) In the case where low-level h_{FE} exceeded the +30 percent criteria, the parameter continued to be out of specification even after decanning and vacuum baking. This type of failure is believed to be attributed to the presence of slight channeling of the emitter-base diode prior to stress. During these temperature storage tests, h_{FE} (5 mA) increased due to dissipation of these channels. In order to return the +30 percent failures to "in-specification" values, the conditions causing the channels would have to be re-established. 2) In the case where low level h_{FE} exceeded the -30 percent criteria, it was found that h_{FE} (5 mA) in some devices was within specification after decanning and exposure to room ambient for twelve hours. Other devices did not respond to the twelve-hour ambient exposure but required a vacuum bake for twenty-four hours before h_{FE} (5 mA) returned to "in-specification" values. Such failures are attributed to entrapment of extraneous unknown contaminants. These unknown contaminants were characterized as volatile (dissipation occurred at room temperature and pressure) and volatilizable (dissipation occurred as a result of vacuum bake) contaminants.

Several V_{BE} and V_{CE} failures were found to have degraded post-to-wire welds. Initially these welds were good, but subsequently they deteriorated due to the presence of an abnormal vertical shear force on the post-to-wire weld while the devices were subjected to the temperature storage tests. The abnormal shear stress resulted from the aluminum lead wire being welded too high on the terminal posts which allowed the bottom of the can tube (Section III) to exert the downward shearing force on the aluminum wire at the weld. The weld became more resistive (degraded) and ultimately the lead wire separated at the post weld due to cold flow of the aluminum at the weld nugget as a result of the shear force at the elevated temperature.

c. Power Operating Tests

The single catastrophic failure of the 150 units stressed was due to an emitter wire open at the post weld. This failure occurred after 96 hours on the 30 W test. The weld was resistive initially as evidenced by a high $V_{CE(sat)}$ reading. The 4 A of emitter current during the 80 W test probably continued the degradation of the weld until it opened.

Representative samples of I_{CEO}, I_{CBO}, I_{EBO}, h_{FE} (5 mA), $V_{CE(sat)}$ and $V_{BE(sat)}$ degradation failures were analyzed. Failure modes determined were:

- Post-to-wire weld separation.
- Temperature-voltage induced inversion of the base region.
- Slight channeling of E-B diodes prior to stress.
- Surface effects

Degradation failures attributed to the post-to-wire weld separation were of the same general type as previously discussed in the other life tests.

The failure mode of some of the devices which exceeded degradation current leakage parameter limits was believed to be temperature-voltage induced inversions of the base region (TVI). Substantiation of the suspected TVI failure mode was achieved by baking the devices at 200° C for 24 hours which accelerated the decrease in current leakage to "in-specification" values.

Failures due to h_{FE} (5 mA) exceeding the ±30 percent low level h_{FE} degradation parameter limit, were due to two different mechanisms. The failure mode believed to be responsible for the +30 percent degradation failures is slight channeling of the E-B diodes prior to stress and is discussed in Section V-6b. The failure mode believed to be responsible for the -30 percent degradation failures is due to surface effects which is also discussed in Section V-6b.

Evaluations of the slopes of the junction V-I characteristics showed the presence of Sah, Noyce, Shockley current.[5] The specific cause of these surface effects was not determined but was removed under stress, thereby resulting in an increase in h_{FE}.

d. Summary

100 percent Mechanical Screen (Constant Acceleration)

The 10,000 G constant acceleration mechanical screening test was effective in removing mechanically weak units. Failure analysis confirmed that the failures of post-to-wire separation were due to weak post-to-wire welds.

Temperature Storage Tests

Most catastrophic failures were due to pinholes and blisters in the collector nickel plate (occurring between 96 and 432 hours at 350° C) which allowed the gold from the die mounting preform to penetrate through the die, shorting all junctions. The other catastrophic failures were due to delamination of gold plate

from the molybdenum substrate beneath the die (at 96 to 432 hours, at 300°C and at 350° C temperatures) which caused the die to separate from the header, thus opening the collector circuit.

The degradation failure modes were: 1) contamination on die or in oxide, 2) defective hermetic seal which proved to be a cracked glass, 3) slight channeling of the E-B diodes prior to stress, low-level h_{FE} (5 mA) increased during stress and remained stable, 4) unknown extraneous contaminant encapsulated within device, low-level h_{FE} (5 mA) decreased during stress and returned to normal after decanning, and 5) post-to-wire weld degradation, prolonged exertion of shear force from tubes on wires initially welded too high on posts.

Power Operating Tests

The only catastrophic failure was due to an open emitter wire at the post-to-wire weld. This failure mode is due to the same mechanism that caused the post-to-wire weld degradation failure discussed previously. The degradation failure modes were temperature voltage induced inversions (TVI) of the base region and other surface effects. Other degradation failures were of the same general types already discussed, post-to-wire weld separation and slight channeling of the E-B diodes prior to stress.

SECTION VI

ACCELERATED TEST RESULTS

1. INTRODUCTION

A brief review of the theory relating fixed and step stress testing is given in Appendix E. Also included is a review of the use of the Arrhenius equation in the interpretation of life test data. This is followed by a discussion of the method used in trying to relate fixed and step stress. Appendix E should be read prior to reading this section for definition of terms and analysis technique. In this section the discussion evolves around results of the Main Test Program (MTP) where most of the testing was done. (MTP previously discussed in Section IV.) A discussion of the results of the Verification Test Program (VTP) is also presented (VTP previously discussed in Section V). Data from the Preliminary Test Program (PTP) have been included in the discussion of results of those tests from MTP where comparable stress conditions were used (PTP is summarized in Section II). The test results of the temperature storage tests, the power operating tests and the reverse bias tests are discussed in that order. Preceding each discussion is a listing of the tests for reference purposes.

2. TEMPERATURE STORAGE TEST RESULTS

a. Temperature Storage Tests

A listing of the temperature storage tests follows:

Temperature Storage Step Stress Tests	48 hours/step	Preliminary Test Program (PTP)
	2 hours/step	Main Test Program (MTP)
	8 hours/step	Main Test Program (MTP)
	24 hours/step	Main Test Program (MTP)
	96 hours/step	Main Test Program (MTP)
Temperature Storage Life Tests	275° C 500 hours	Preliminary Test Program (PTP)
	200° C 1000 hours	Main Test Program (MTP)
	250° C 1000 hours	Main Test Program (MTP)
	300° C 1000 hours	Main Test Program (MTP)
	275° C 1000 hours	Verification Test Program (VTP)
	300° C 1000 hours	Verification Test Program (VTP)
	350° C 1000 hours	Verification Test Program (VTP)

b. Main and Preliminary Test Programs

The cumulative percent failure curves for the temperature storage step stress tests are given in Figures 32 and 33. The actual points and least squares fit curves will be found in Figure E-5 of Appendix E. The following regression equations are obtained for the least squares fit of the data.

$$\lambda_p = 9.92 - 3.13 \frac{1000}{T} \qquad \text{(2 hours/step)}$$

$$\lambda_p = 11.0 - 3.55 \frac{1000}{T} \qquad \text{(24 hours/step)}$$

$$\lambda_p = 10.4 - 3.14 \frac{1000}{T} \qquad \text{(96 hours/step)}$$

$$\lambda_p = 13.9 - 5.00 \frac{1000}{T} \qquad \text{(48 hours/step)}$$

Values of the standard deviations of the distribution of the failures with respect to stress are:

2 hours/step	$\sigma_s = 0.32 \times 10^{-3}$
24 hours/step	$\sigma_s = 0.28 \times 10^{-3}$
96 hours/step	$\sigma_s = 0.32 \times 10^{-3}$
Average	$\sigma_s = 0.31 \times 10^{-3}$

It is noted that the 2, 24, and 96 hours/step data have approximately the same standard deviation, satisfying one of the necessary conditions for being able to relate fixed and step stress results. The standard deviation, σ_s, for the PTP temperature storage step stress test (48 hours/step) was 0.20×10^{-3}.

Acceleration curves for the step stress data for the 2, 24, and 96 hours/step are shown in Figure 34. The regression equations for these curves are shown below. The 8 hour/step data as previously discussed in Section IV depart from the failure pattern and are not used.

$$\frac{1000}{T} = 1.96 + 0.086 \log_{10} t \qquad \text{(10\% failure)}$$

$$\frac{1000}{T} = 1.82 + 0.086 \log_{10} t \qquad \text{(20\% failure)}$$

$$\frac{1000}{T} = 1.72 + 0.080 \log_{10} t \qquad \text{(30\% failure)}$$

$$\frac{1000}{T} = 1.55 + 0.087 \log_{10} t \qquad \text{(50\% failure)}$$

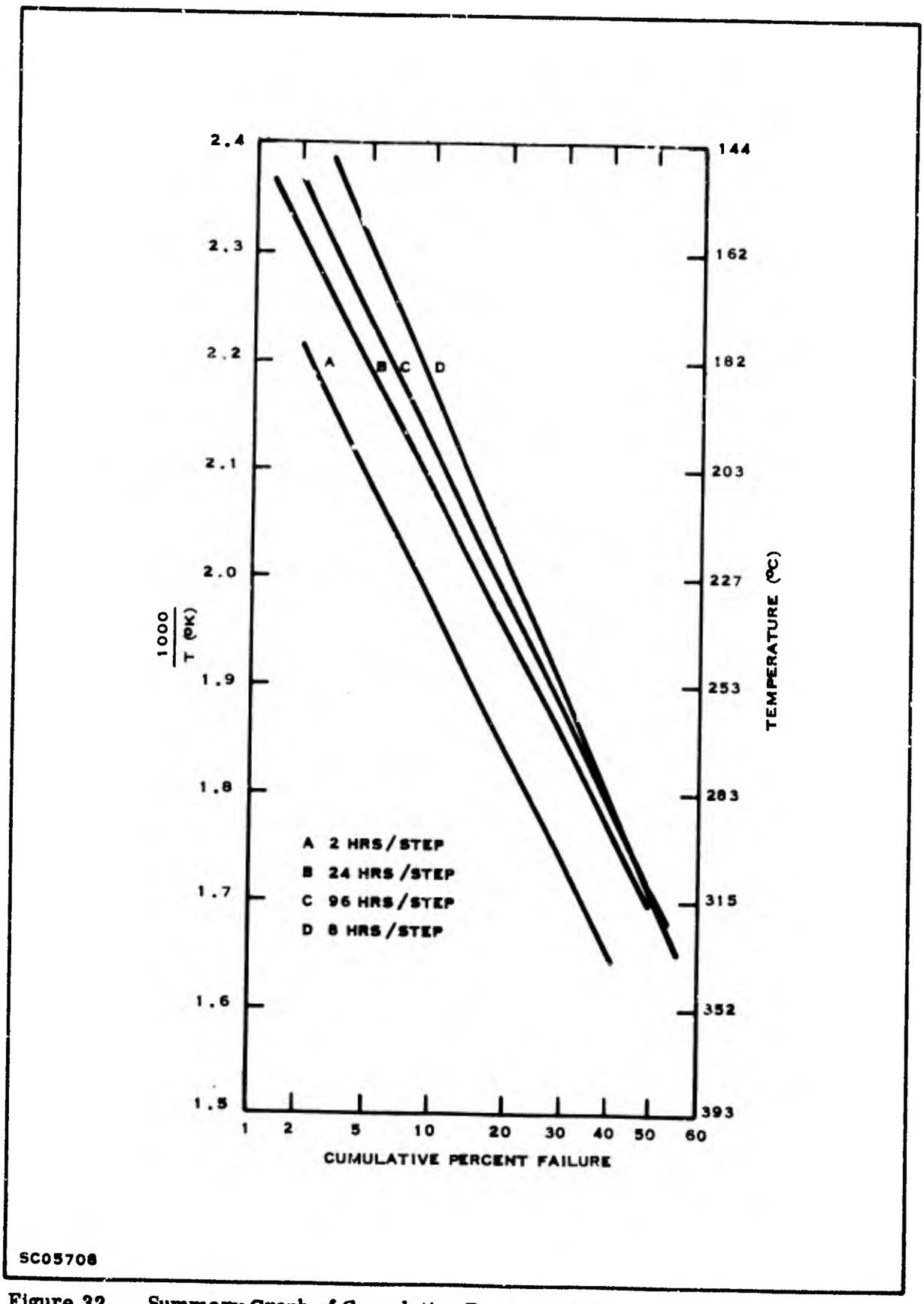

Figure 32. Summary Graph of Cumulative Percent Failure Curves for Temperature Step Stress Test (Main Test Program)

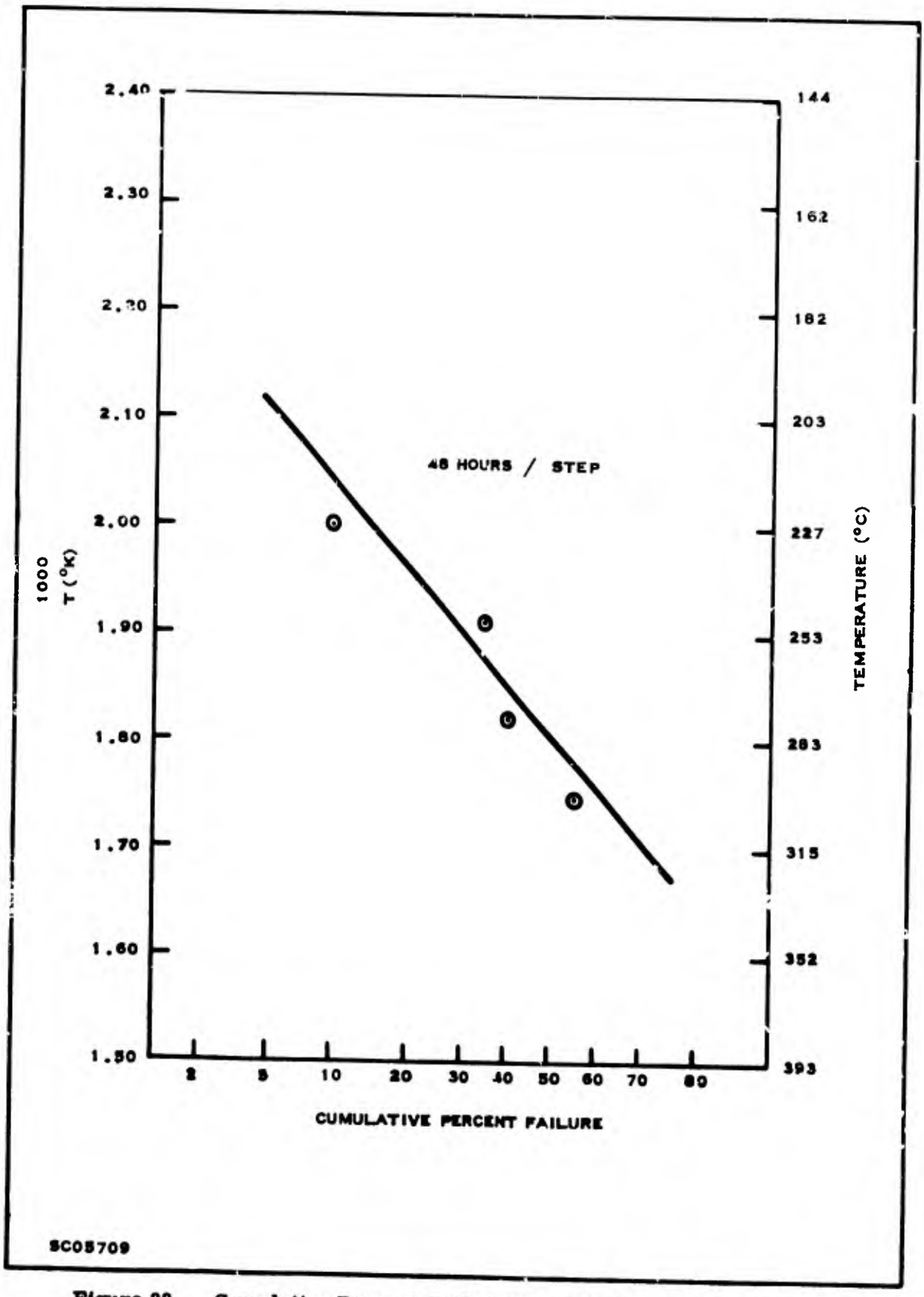

Figure 33. Cumulative Percent Failure Curve for Storage Step Stress Test (Preliminary Test Program)

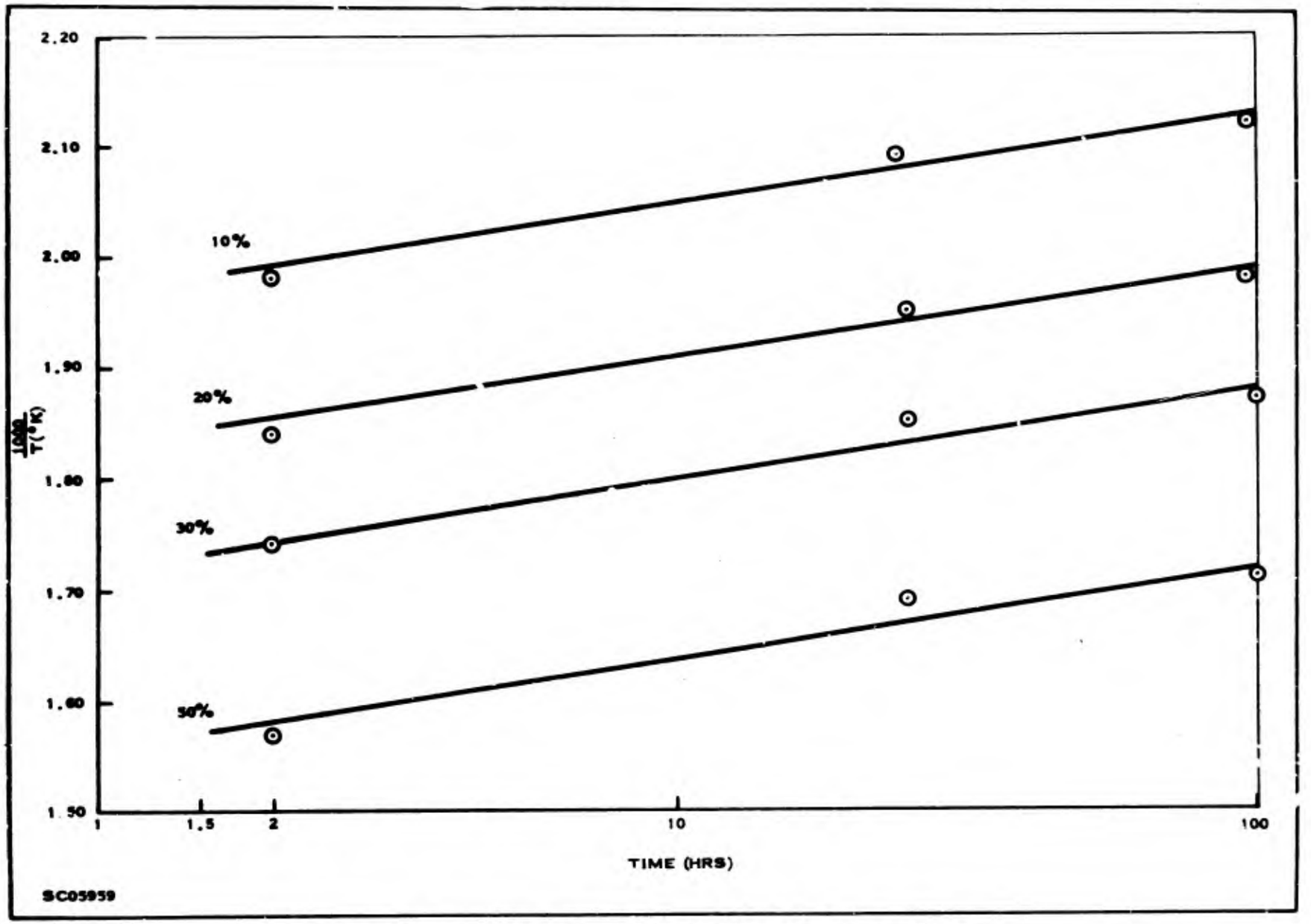

Figure 34. Acceleration Curves (10%–50% Failures) Temperature Step Stress (Main Test Program)

The fact that these curves are parallel indicates that a true acceleration is being considered. These curves are written as a function of 1000/T for convenience; the actual acceleration curve, for 10% failure, for example, is $1/T = 1.96 \times 10^{-3} + 0.086 \times 10^{-3} \log_{10} t$. The average slope for these curves is 8.5×10^{-5} giving an activation energy, E_A, of 2.4 eV.

The data generated by the temperature storage life tests present a somewhat more complicated picture than that of the step stress tests. In the MTP results shown in Figure 35, the 200° C line is uncomplicated, but there are definitely two segments of the curve for the 250° C test. A break is also shown in the 300° C curve, although a reasonably straight line could be drawn through all of the points. The presence of this break is also noted in the results of the 275° C life test of the PTP shown in Figure 36.

The equations for these curves are:

$\lambda_p = 0.79 + 1.02 \log_{10} t$ (200°C)

$\lambda_p = 3.34 + 0.382 \log_{10} t$ (250°C, Segment 1)

$\lambda_p = 0.80 + 1.37 \log_{10} t$ (250°C, Segment 2)

$\lambda_p = 3.79 + 0.825 \log_{10} t$ (300°C, Segment 1)

$\lambda_p = 4.17 + 0.630 \log_{10} t$ (300°C, Segment 2)

$\lambda_p = 4.19 + 0.831 \log_{10} t$ (275°C, Segment 1)

$\lambda_p = 4.99 + 0.337 \log_{10} t$ (275°C, Segment 2)

Analysis of the pretreatment data given in Section IV showed that groups 1, 2, and 3 as well as the control group had essentially the same cumulative percent failure plots. For each group the cumulative percent failure plots showed breaks in the 250° C and 300° C curves. These plots of pretreatment data are not included in this report.

A comparison of these life test results to the step stress results was made. First the 200° C curve, segment 2 of the 250° C curve, segment 1 of the 300°C curve, and segment 1 of the PTP were checked to see if they were parallel; if there was a constant standard deviation from stress level to stress level. The following values of σ_t are obtained for:

200° C	$\sigma_t = 0.98$
250° C, Segment 2	$\sigma_t = 0.73$
275° C, Segment 1	$\sigma_t = 1.21$
300° C, Segment 1	$\sigma_t = 1.22$
Average	$\sigma_t = 1.04$

The activation energy obtained from the relation Avg σ_s/Avg σ_t = m (slope of acceleration curve) is 0.67 eV.

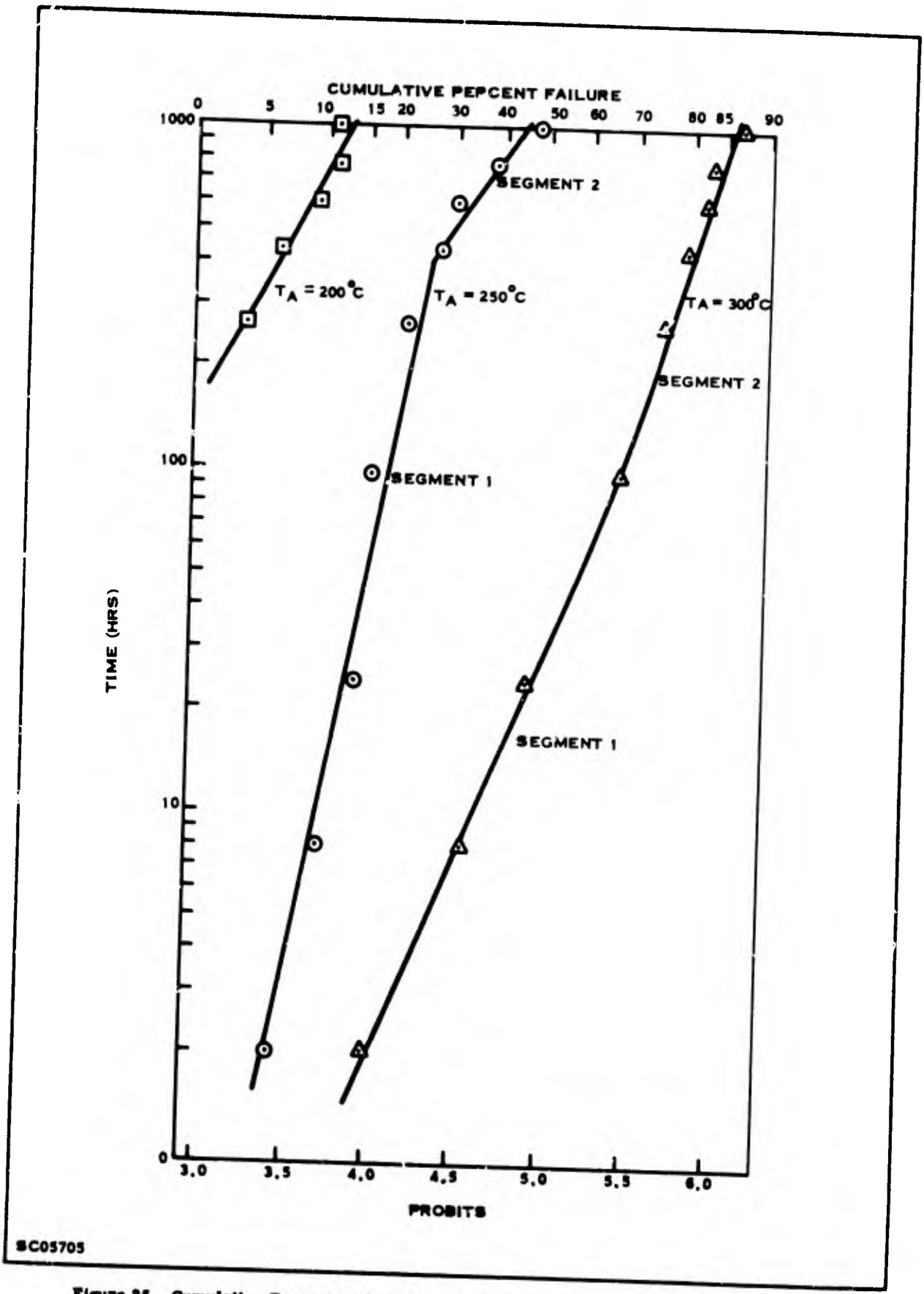

Figure 35. Cumulative Percent Failure Curves for Temperature Storage Life Tests (Main Test Program)

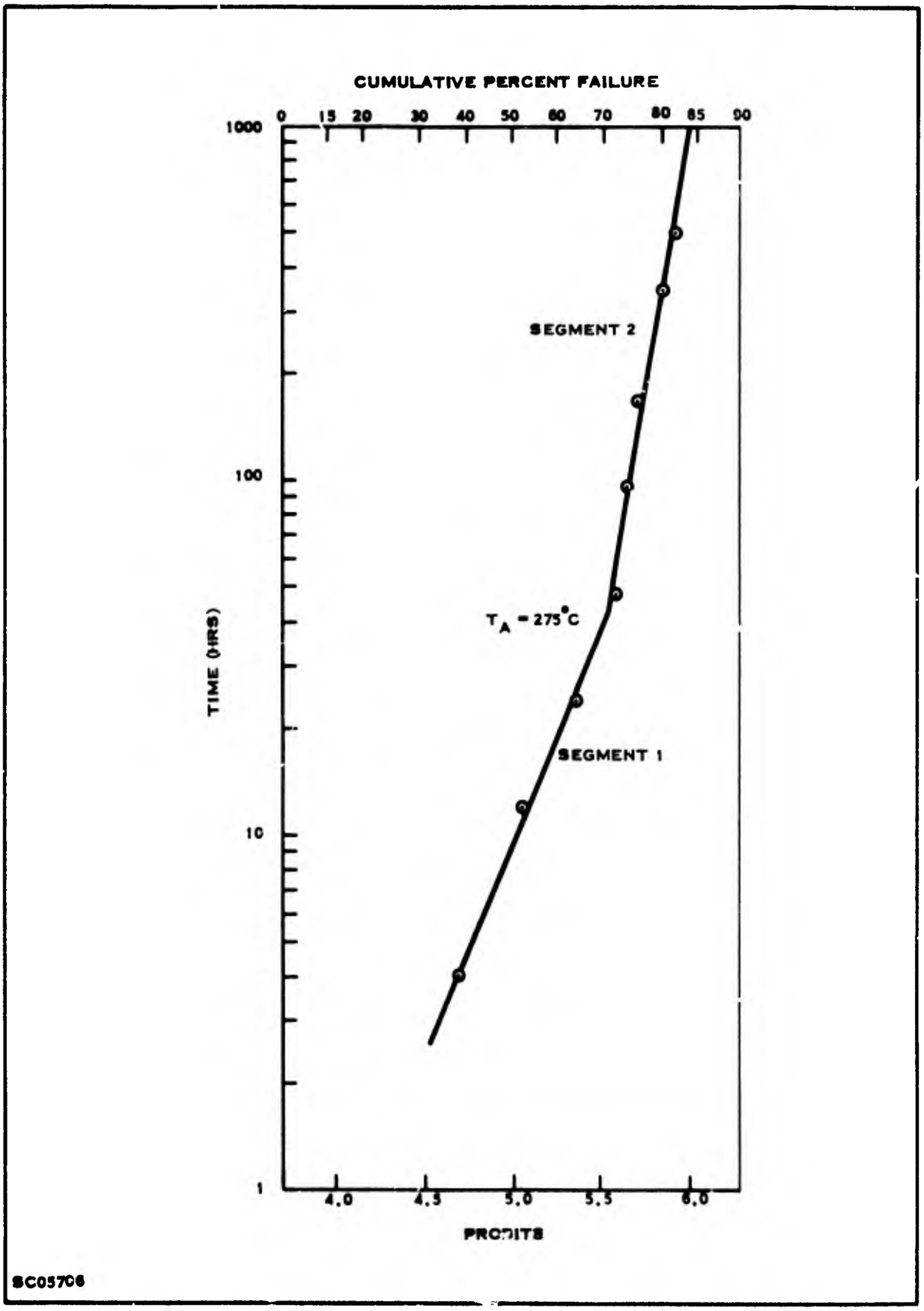

Figure 36. Cumulative Percent Failure Curve for Temperature Storage Life Tests (Preliminary Test Program)

The regression equations for the storage life test on the MTP are:

$$1000/T = 1.83 + 0.093 \log_{10} t \quad \text{(10\% failure)}$$
$$1000/T = 1.67 + 0.122 \log_{10} t \quad \text{(20\% failure)}$$
$$1000/T = 1.35 + 0.210 \log_{10} t \quad \text{(30\% failure)}$$
$$1000/T = 1.52 + 0.136 \log_{10} t \quad \text{(50\% failure)}$$

These acceleration curves are given in Figures 37, 38, 39, and 40 along with the previously determined step stress curves (Figure 34) and points obtained from the PTP for comparison.

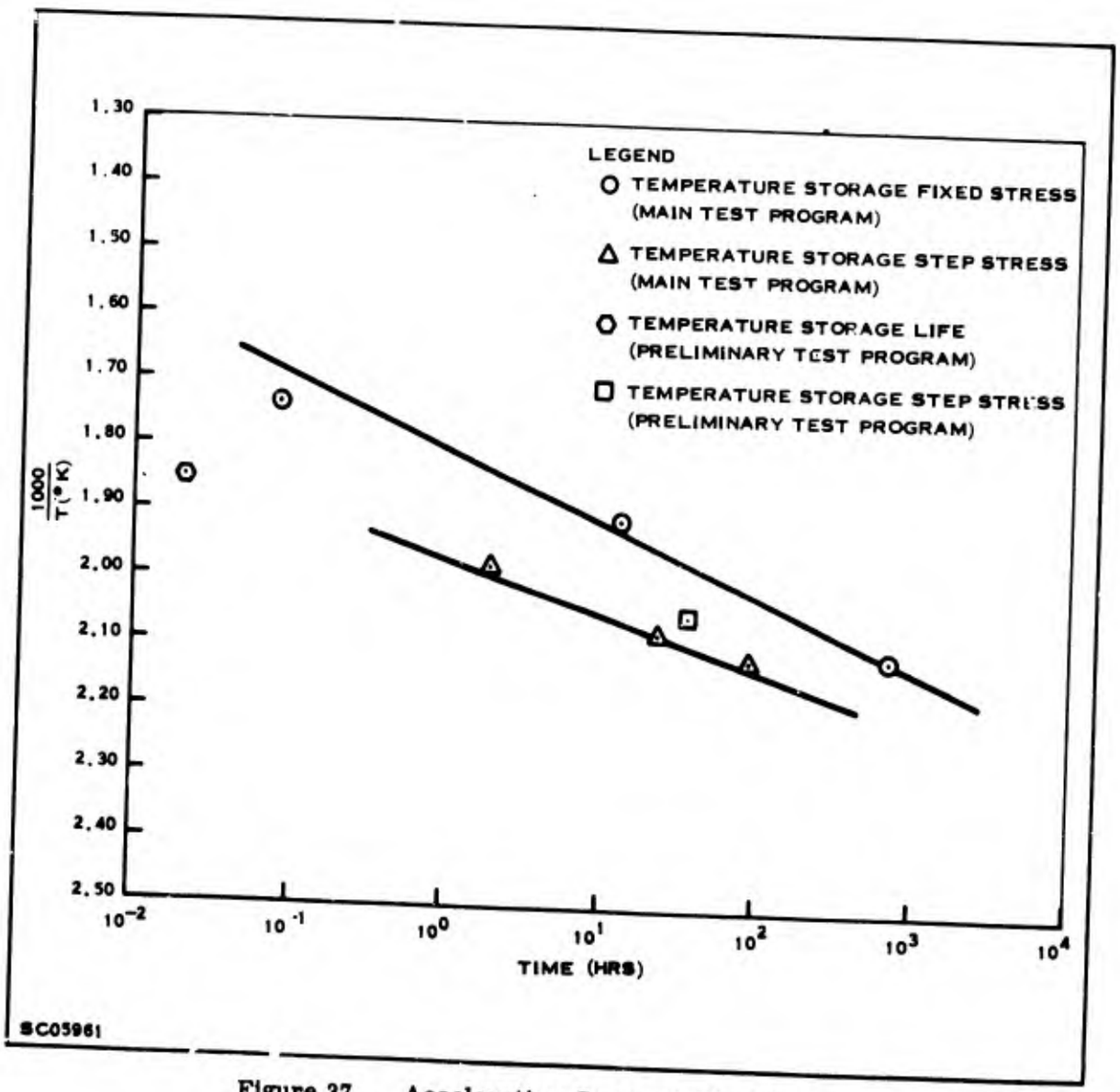

Figure 37. Acceleration Curves (10% Failure)

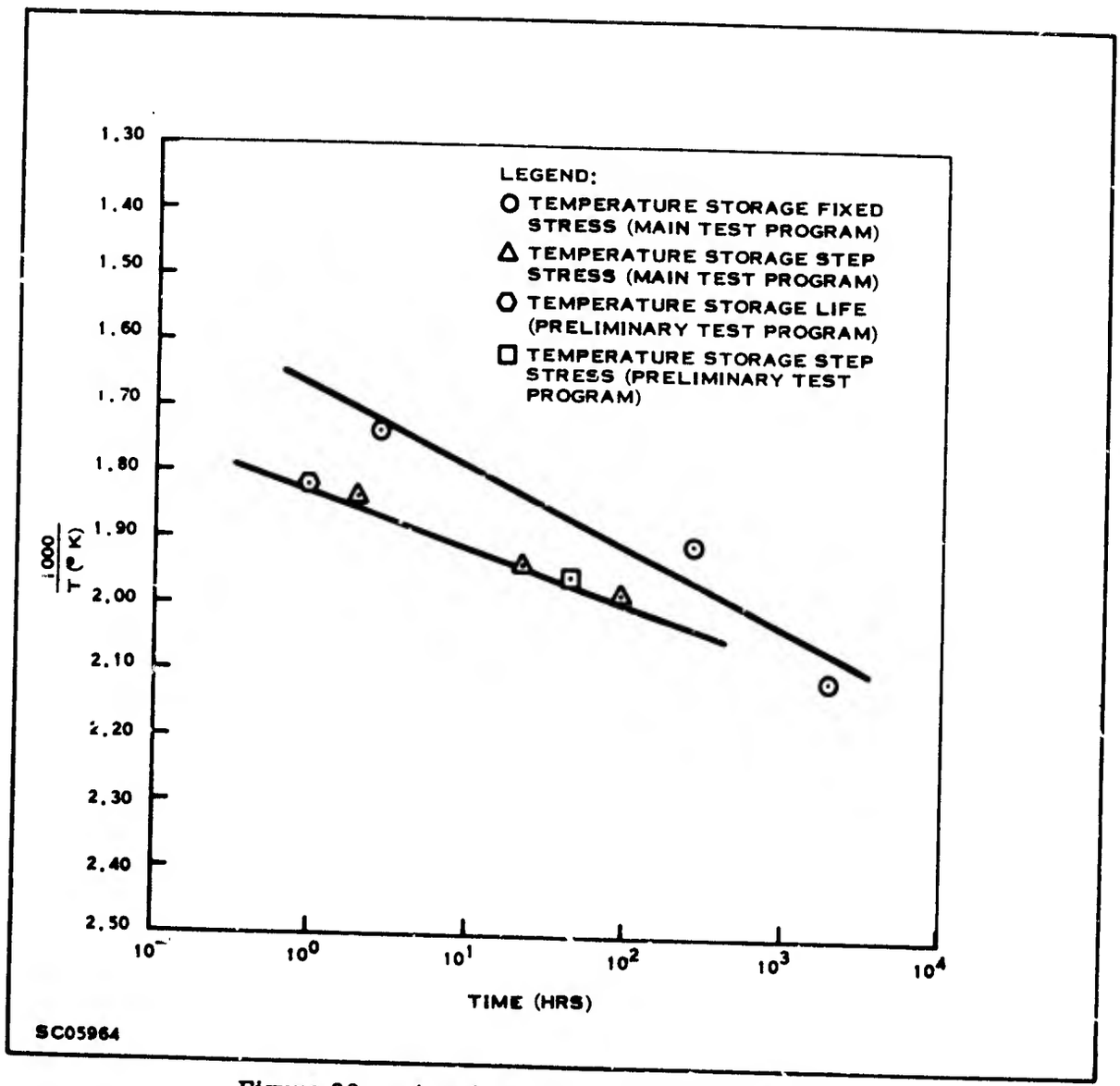

Figure 38. Acceleration Curves (20% Failure)

Activation energies corresponding to these acceleration curves are 2.2 eV, 1.6 eV, 1.0 eV, and 1.5 eV, respectively. These are to be compared with the previously determined values of 2.4 eV and 0.67 eV.

Thus the three methods for determining activation energy have yielded very different results. Furthermore, extrapolation of the fixed and step stress results to room temperature (25°C) provides meaningless failure rates. For example, extrapolation of the 10% cumulative failure acceleration curves gives failure rates of 10^{-12}%/1000 hours. If the 300°C and 250°C points are connected by one line and the 250°C and 200°C points by another line, such as in Figure 41, then extrapolation of the 250°C to 200°C line to room temperature gives a failure rate of 4×10^{-5}%/1000 hours, a more realistic number. The slopes of the new acceleration curves have been obtained and

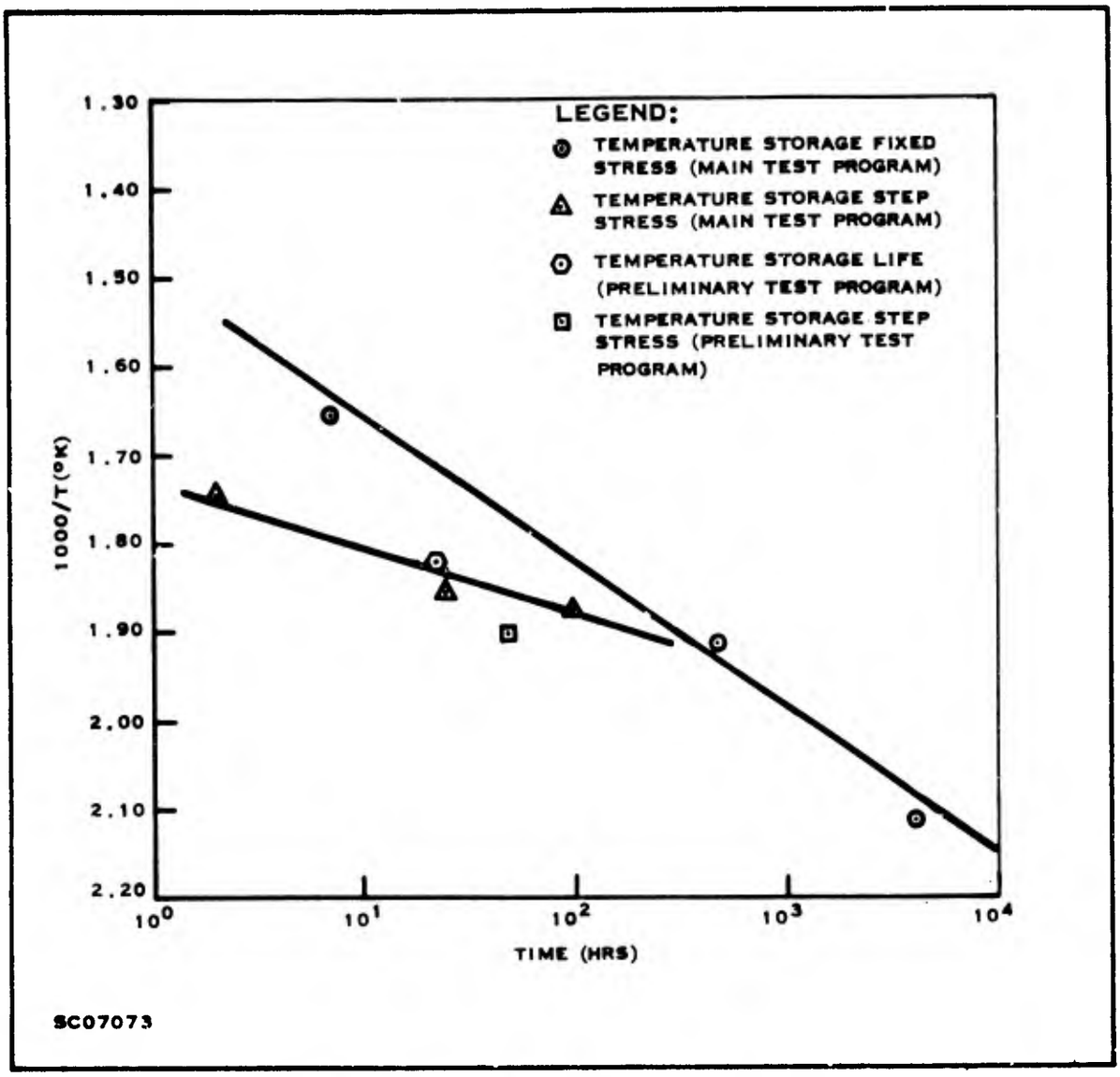

Figure 39. Acceleration Curves (30% Failure)

are given in Table 16. There will be one line for the 300°C to 250°C data and one line for the 250°C to 200°C data.

Re-examining the step stress curves in Figure E-5 reveals that these possibly should not be straight lines. The 24 hours/step step stress curve, for example, may be redrawn as in Figure 42. All of these breaks in the step stress curves appear to be at about 1.9×10^{-3} °K^{-1} to 2.0×10^{-3}°K^{-1} or 250°C to 275°C. Since the fixed stress results are quite anomalous at 250°C it would be expected that the step stress results would also exhibit some anomaly at about the same temperature. The σ_s values for the new step stress cumulative percent failure curves have been calculated and are given in Table 17. There will be one line and one σ_s value for the data below 250°C and one for the data above 250°C. The 8-hour data have not been included since, as mentioned before, they are quite different from other test data.

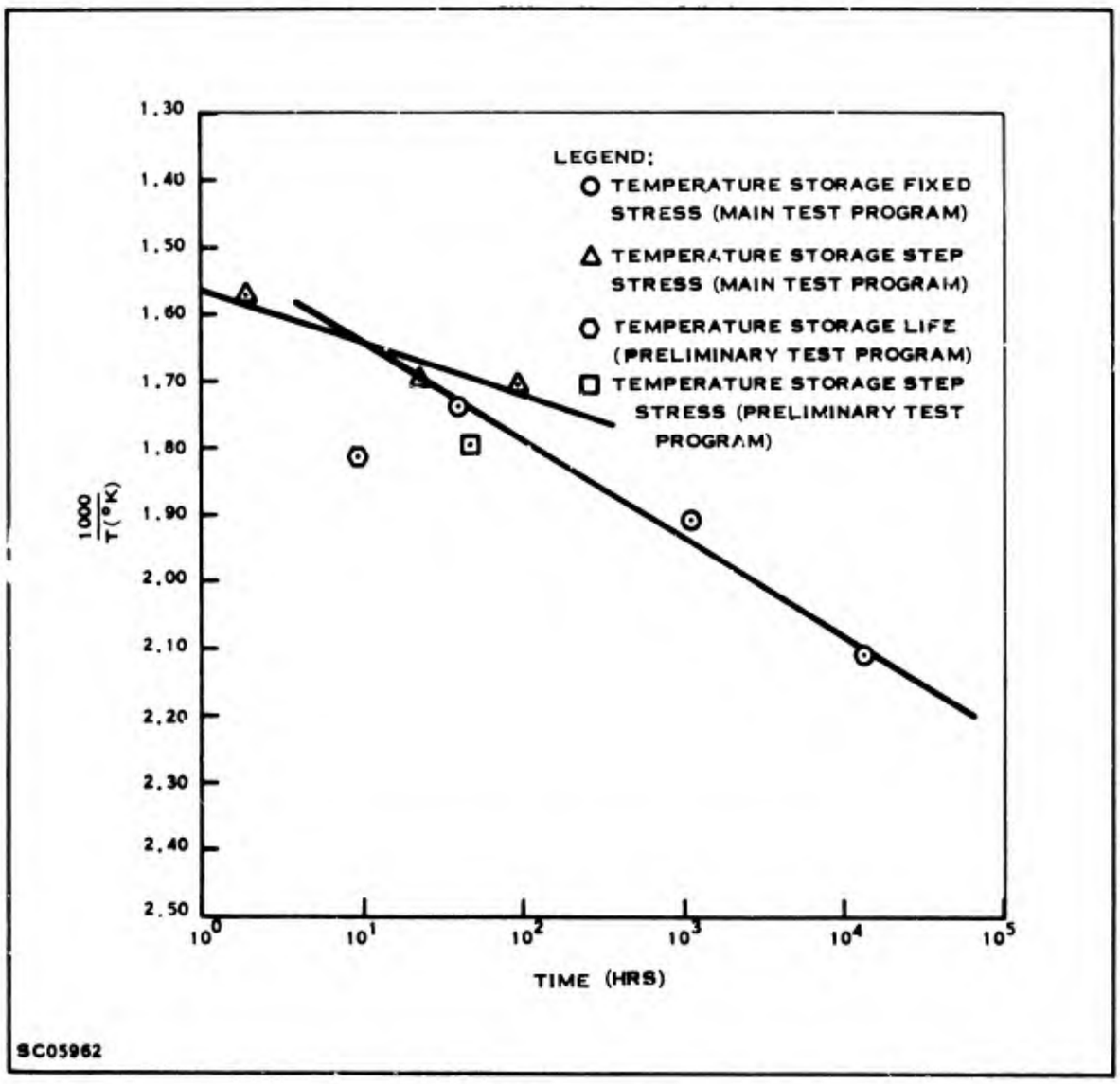

Figure 40. Acceleration Curves (50% Failure)

Table 16. Slopes of Acceleration Curves for Temperature Storage Life Tests (Main Test Program)

Acceleration Curve	Slope of Acceleration Curve	
	300° C ≤ T < 250° C	250° C > T ≥ 200° C
10% Cumulative Failure	0.8×10^{-4}	1.1×10^{-4}
20% Cumulative Failure	0.9×10^{-4}	2.4×10^{-4}
30% Cumulative Failure	1.4×10^{-4}	2.2×10^{-4}
50% Cumulative Failure	1.2×10^{-4}	1.8×10^{-4}
Average	1.1×10^{-4}	1.9×10^{-4}

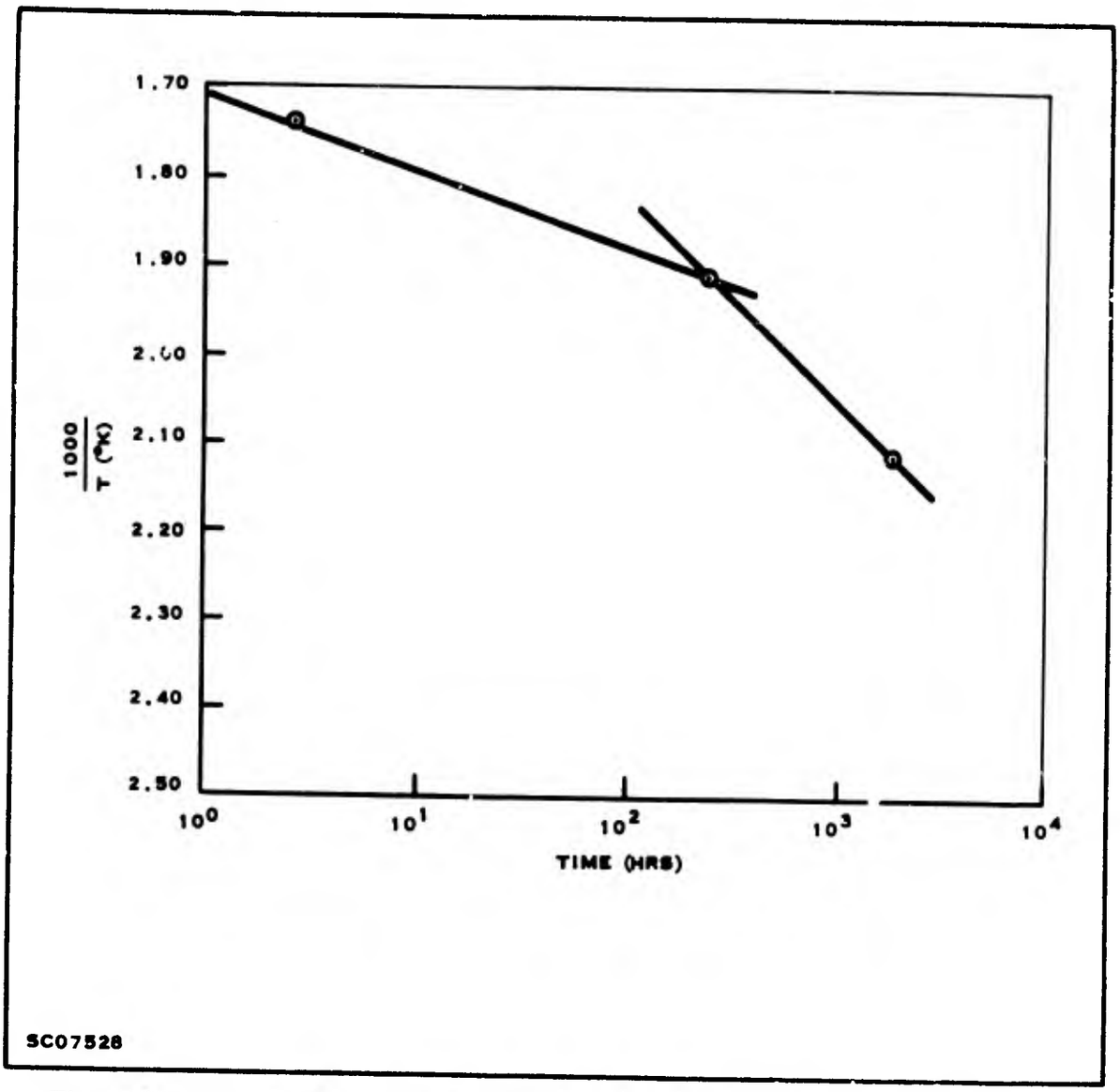

Figure 41. Acceleration Curve (20% Failure) Temperature Storage Life Test (Main Test Program)

Table 17. σ_s Values for Temperature Storage Step Stress Results (Main Test Program

Step Stress Test	σ_s for T ≤ 250° C	σ_s for T ≥ 250° C
2 hours/step	2.1×10^{-4}	3.0×10^{-4}
24 hours/step	2.0×10^{-4}	4.2×10^{-4}
48 hours/step	1.1×10^{-4}	2.9×10^{-4}
96 hours/step	2.8×10^{-4}	4.7×10^{-4}
Average	2.0×10^{-4}	3.7×10^{-4}

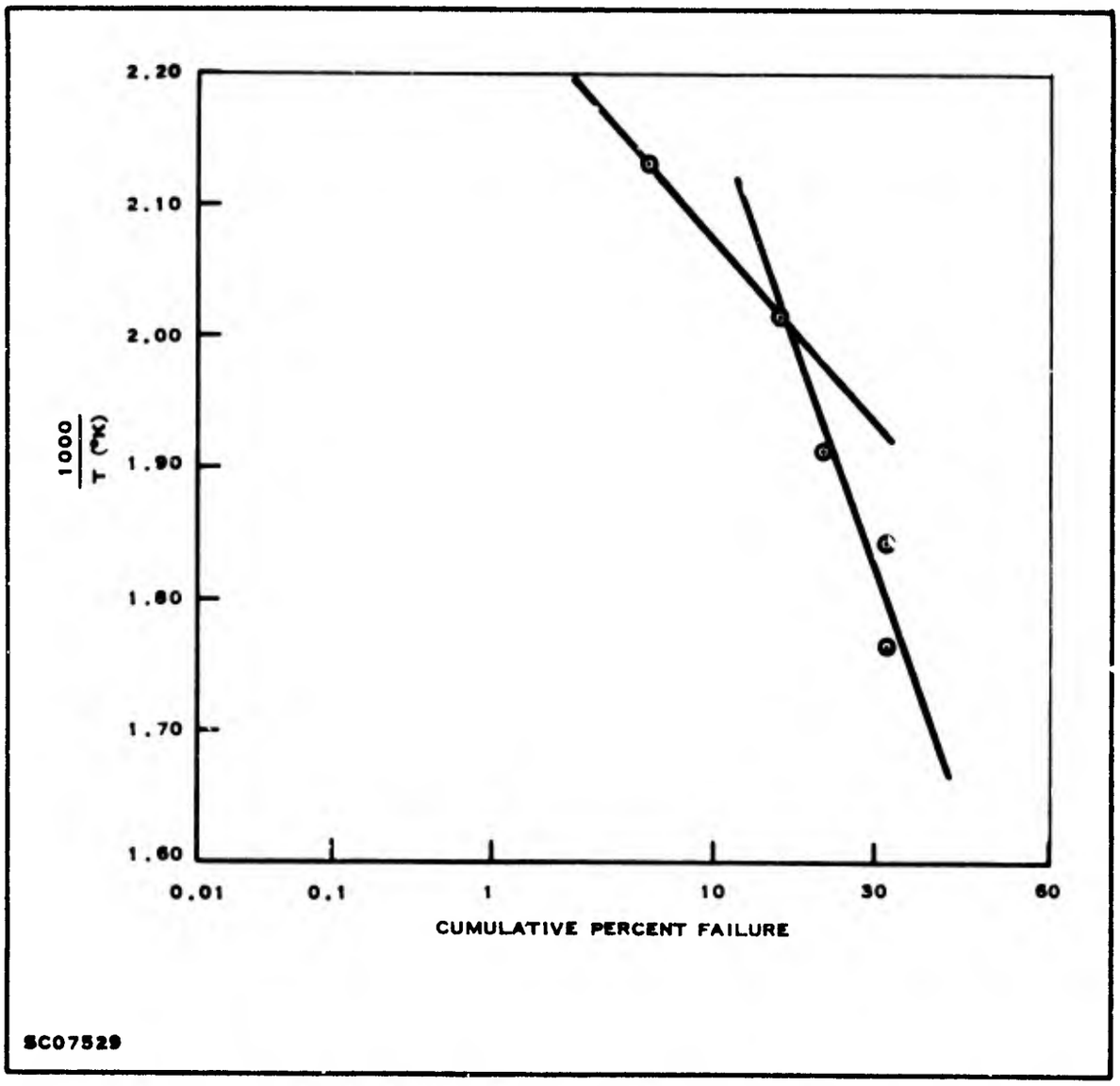

Figure 42. Cumulative Percent Failure Curve for 24 Hours/Step Temperature Storage Step Stress Test (Main Test Program)

Using the value of 2.0×10^{-4} for the σ_s associated with the step stress curve below 250° C-275° C and the value of 1.04 calculated for σ_t previously would yield a slope of 1.9×10^{-4} and an activation energy of 1.1 eV. This slope is the same as the average slope of the acceleration curve for the fixed stress results between 200° C and 250° C (Table 16).

In an attempt to determine the failure mechanisms operative, it was decided to study individual parameter behavior. I_{CEO} (70 V) was studied for the 250° C and 300° C life test of the MTP. Only devices exceeding the failure limits (Section III) on this parameter were considered failures. These plots are given in Figure 43. The

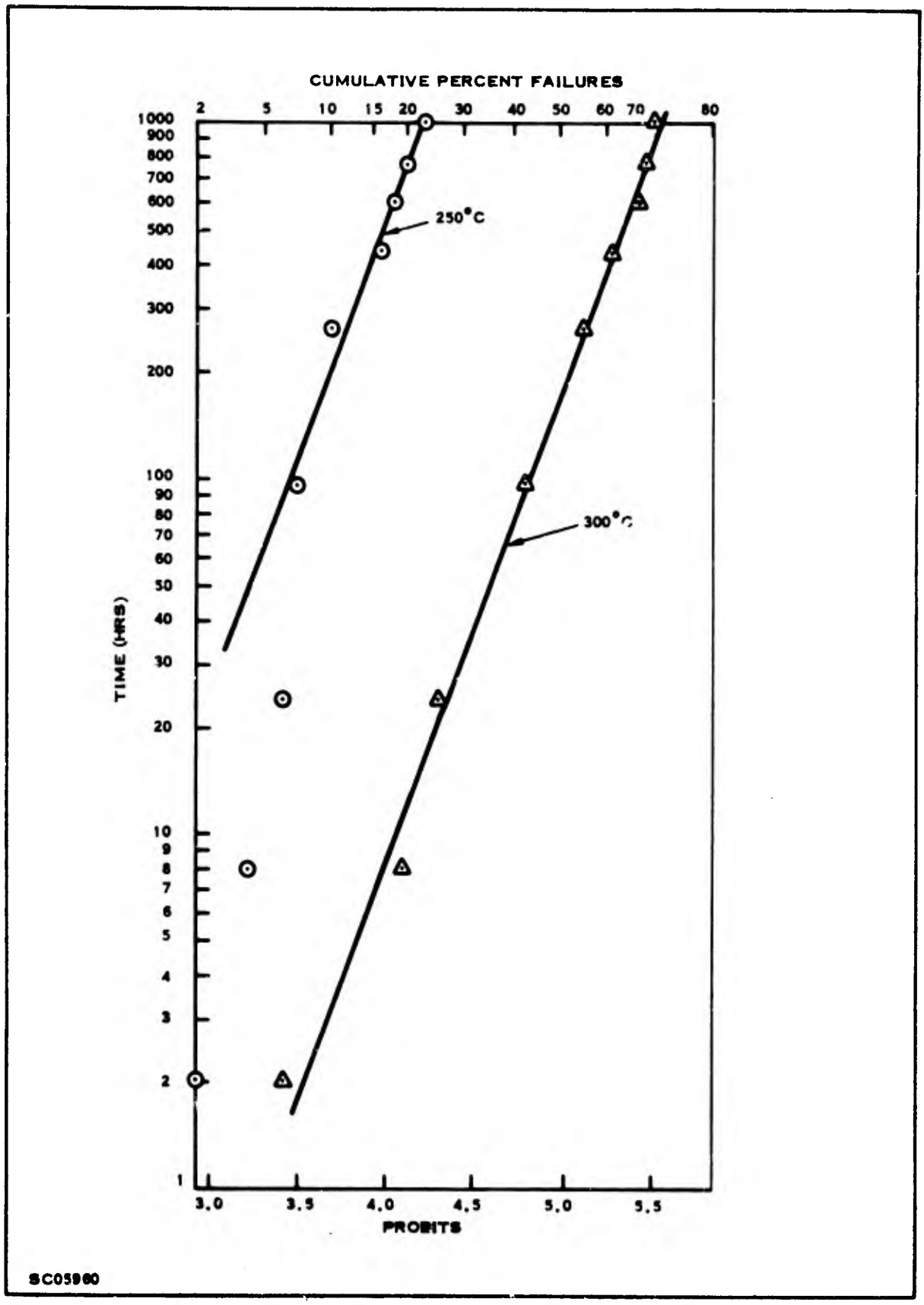

Figure 43. Cumulative Percent Failure I_{CEO} (70 V) Temperature Storage Life Test (Main Test Program)

equations for these curves are:

$$\lambda_p = 2.00 + 0.747 \log_{10} t \quad (250°\,C)$$
$$\lambda_p = 3.32 + 0.749 \log_{10} t \quad (300°\,C)$$

The σ_t calculated for these curves is 1.3,comparable to the values calculated from the storage life results of the MTP using the usual failure criteria. The slope of the acceleration curve obtained from the I_{CEO} (70 V) data for 250° and 300° C is 0.9×10^{-4}, yielding an activation energy of 2.2 eV. This may be compared with the slope of 1.1×10^{-4} and activation energy of 1.8 eV found for the activation energy of the MTP results for data between 250° C and 300° C, using the usual failure criteria. Using the value of σ_s calculated from the MTP step stress data above 250° C, Table 17, and the value of 1.04 for σ_t gives a slope, m, of $3.7 \times 10^{-4}/1.04 = 3.7 \times 10^{-4}$, and an activation energy of 0.54 eV. This value is completely different from the activation energies of 2.2 eV and 1.8 eV calculated above.

c. Verification Test Program

Interpretation of the cumulative percent failure curves for the temperature storage tests of the VTP (Figure 44) is even more challenging. The equations for the temperature storage life tests of the VTP are:

$$\lambda_p = 3.55 + 1.08 \log_{10} t \quad (275°\,C, \text{ Segment 1})$$
$$\lambda_p = 4.63 + 0.322 \log_{10} t \quad (275°\,C, \text{ Segment 2})$$
$$\lambda_p = 4.20 + 0.447 \log_{10} t \quad (300°\,C)$$
$$\lambda_p = 4.61 + 0.387 \log_{10} t \quad (350°\,C, \text{ Segment 1})$$
$$\lambda_p = 3.48 + 0.976 \log_{10} t \quad (350°\,C, \text{ Segment 2})$$

The 300° C and 350° C (Segment 1) values are compared with the MTP acceleration curves in Figures 45, 46, 47, and 48. It is seen that the results of the 300° C and 350° C storage temperature tests of the VTP agree well with the MTP results.

3. POWER OPERATING TEST RESULTS

a. Power Operating Tests

A listing of the power operating tests follows.

Power Operating	2 hours/step	Main Test Program (MTP)
Step Stress	8 hours/step	Main Test Program (MTP)
	24 hours/step	Main Test Program (MTP)
	96 hours/step	Main Test Program (MTP)

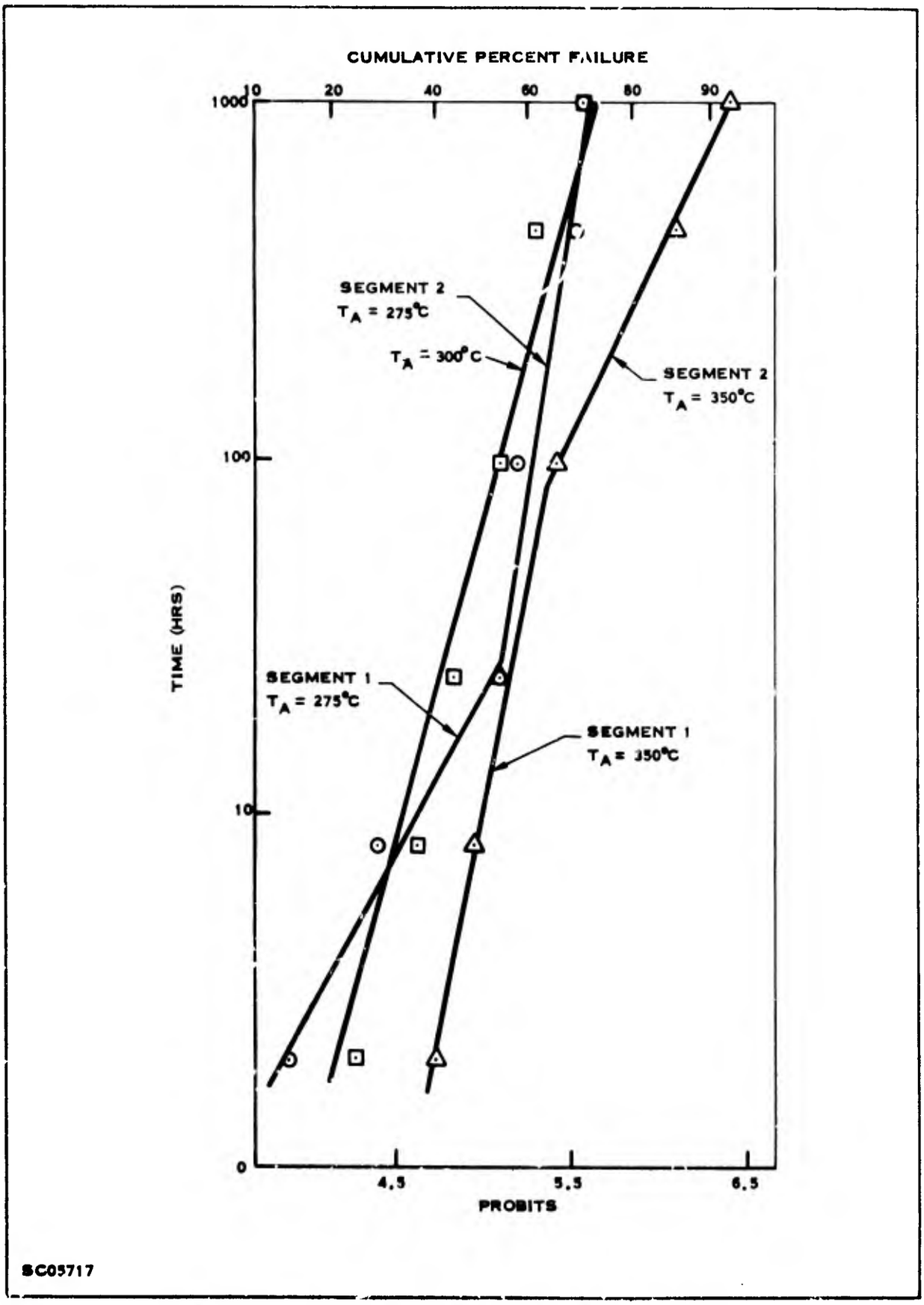

Figure 44. Cumulative Percent Failure Curve for Temperature Storage Life Test (Verification Test Program)

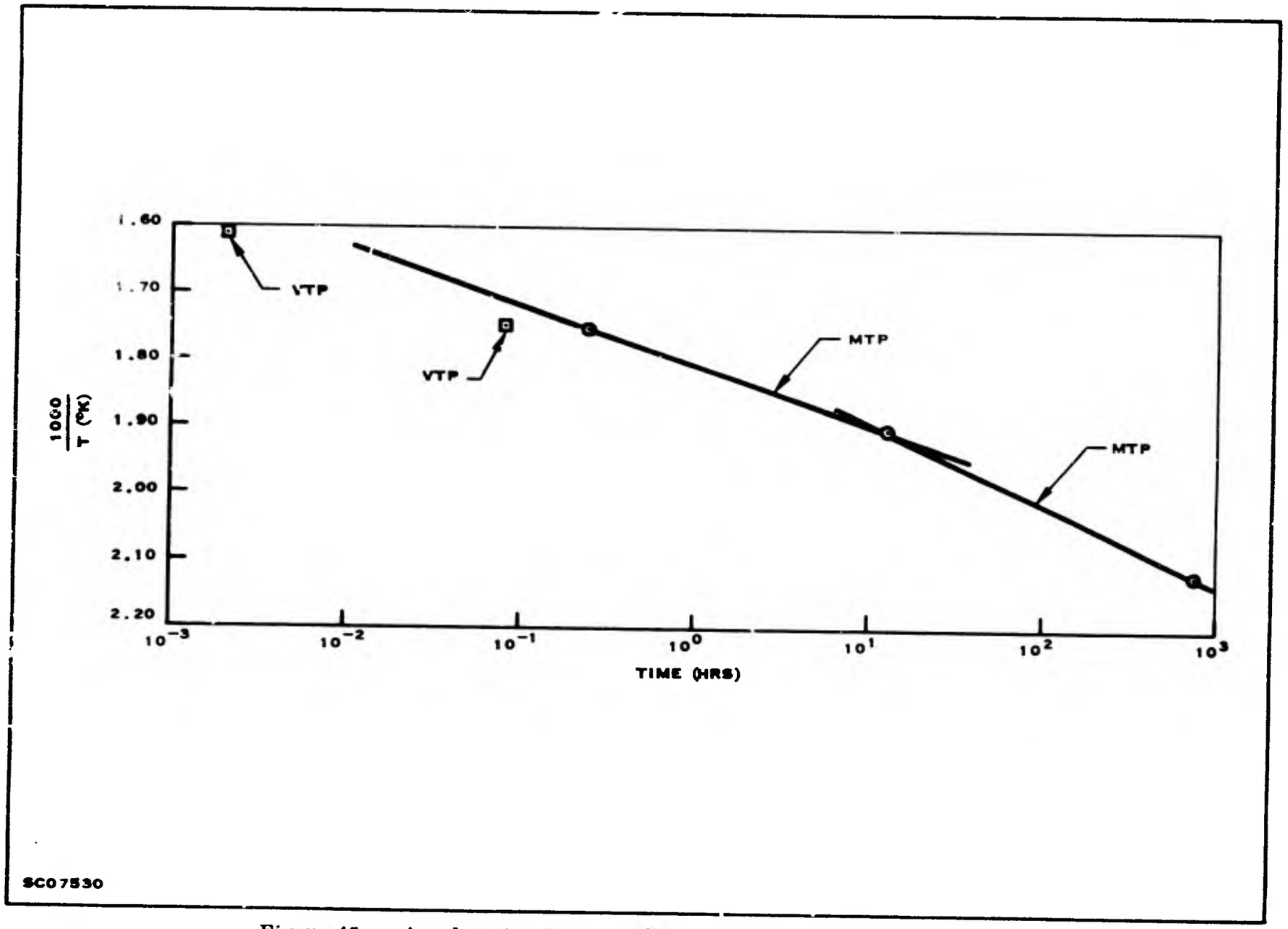

Figure 45. Acceleration Curve (10% Failures) Temperature Storage Test (Main and Verification Test Programs)

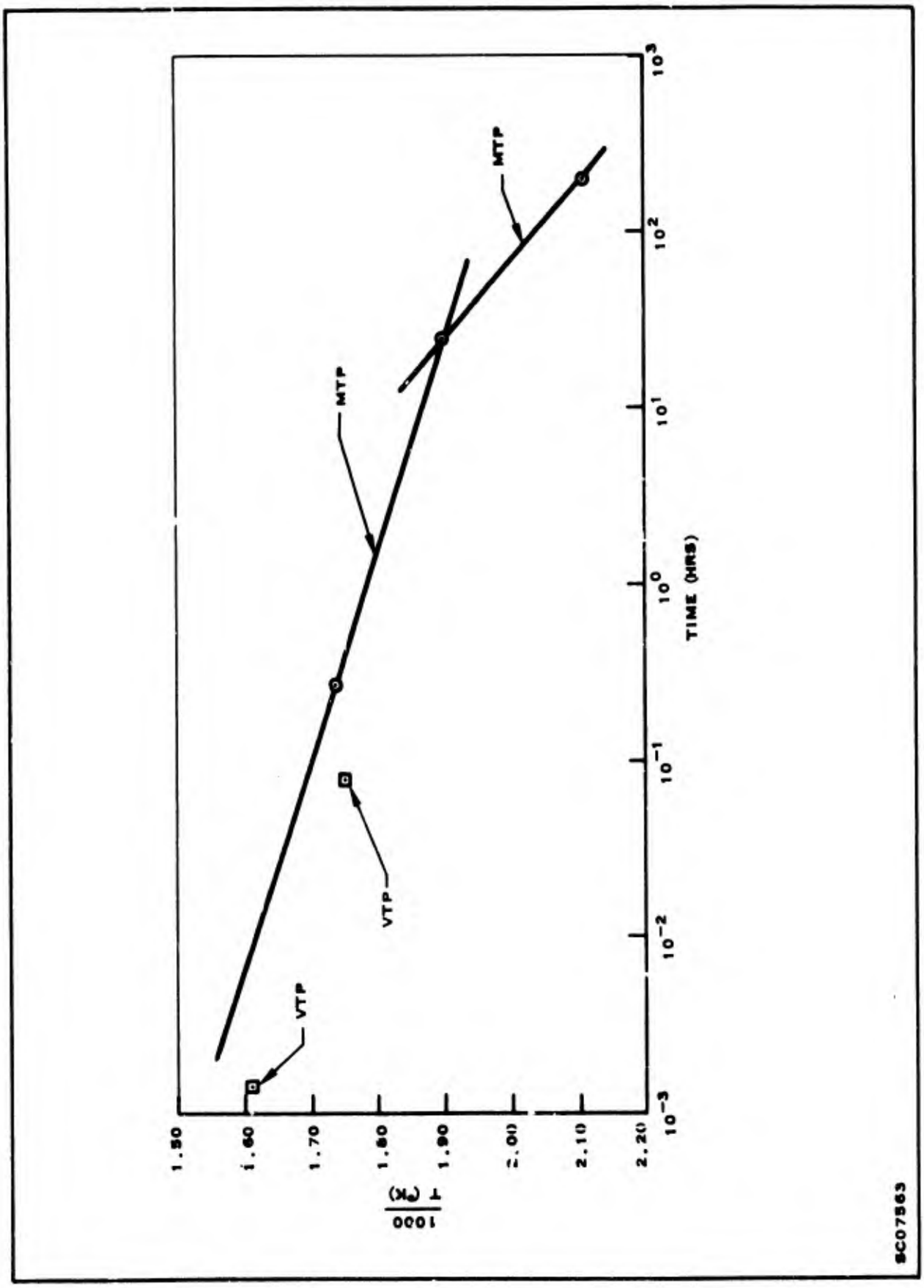

Figure 46. Acceleration Curve (20% Failures) of Temperature Storage Tests (Main and Verification Test Programs)

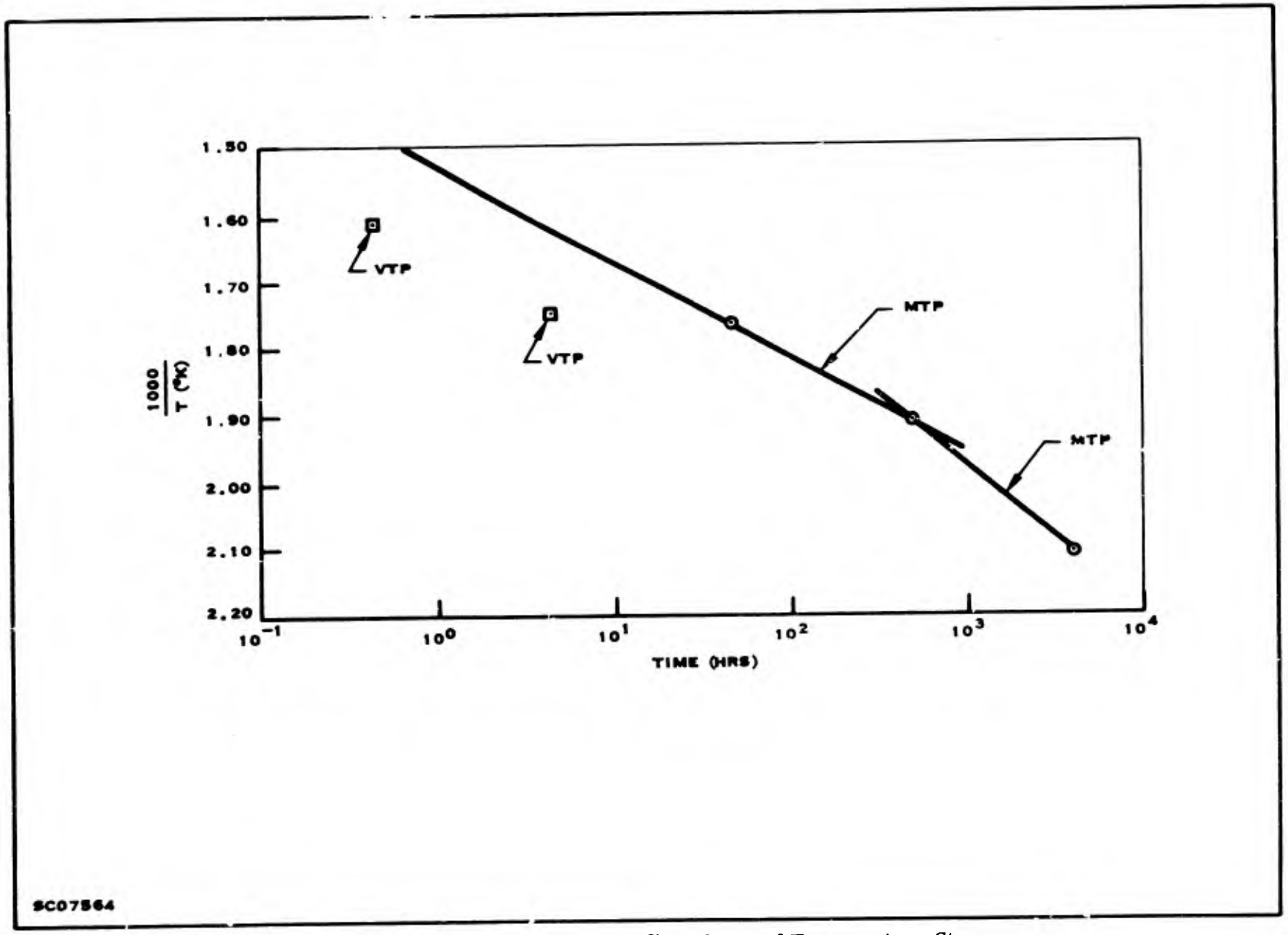

Figure 47. Acceleration Curve (30% Failure) of Temperature Storage Tests (Main and Verification Test Programs)

Power Operating Life Tests	30 W, V_{CE} = 20 V, 500 hours	Preliminary Test Program (PTP)
	15 W, V_{CE} = 15 V, 1000 hours	Main Test Program (MTP)
	37.5 W, V_{CE} = 15 V, 1000 hours	Main Test Program (MTP)
	60 W, V_{CE} = 15 V, 1000 hours	Main Test Program (MTP)
	30 W, V_{CE} = 20 V, 1000 hours	Verification Test Program (VTP)
	50 W, V_{CE} = 20 V, 1000 hours	Verification Test Program (VTP)
	80 W, V_{CE} = 20 V, 1000 hours	Verification Test Program (VTP)

b. Main Test Program

Cumulative percent failure curves for power operating tests of the MTP are given in Figure 49. A similar curve for the 30 W power operating life tests of the PTP is given in Figure 50. The following regression equations are obtained for the least squares fit of the data.

$$\lambda_p = 2.71 + 0.205 \log_{10} t \quad \text{(15 W)}$$

$$\lambda_p = 3.22 + 0.248 \log_{10} t \quad \text{(37.5 W)}$$

$$\lambda_p = 4.77 + 0.169 \log_{10} t \quad \text{(60 W)}$$

$$\lambda_p = 4.74 + 0.165 \log_{10} t \quad \text{(30 W)}$$

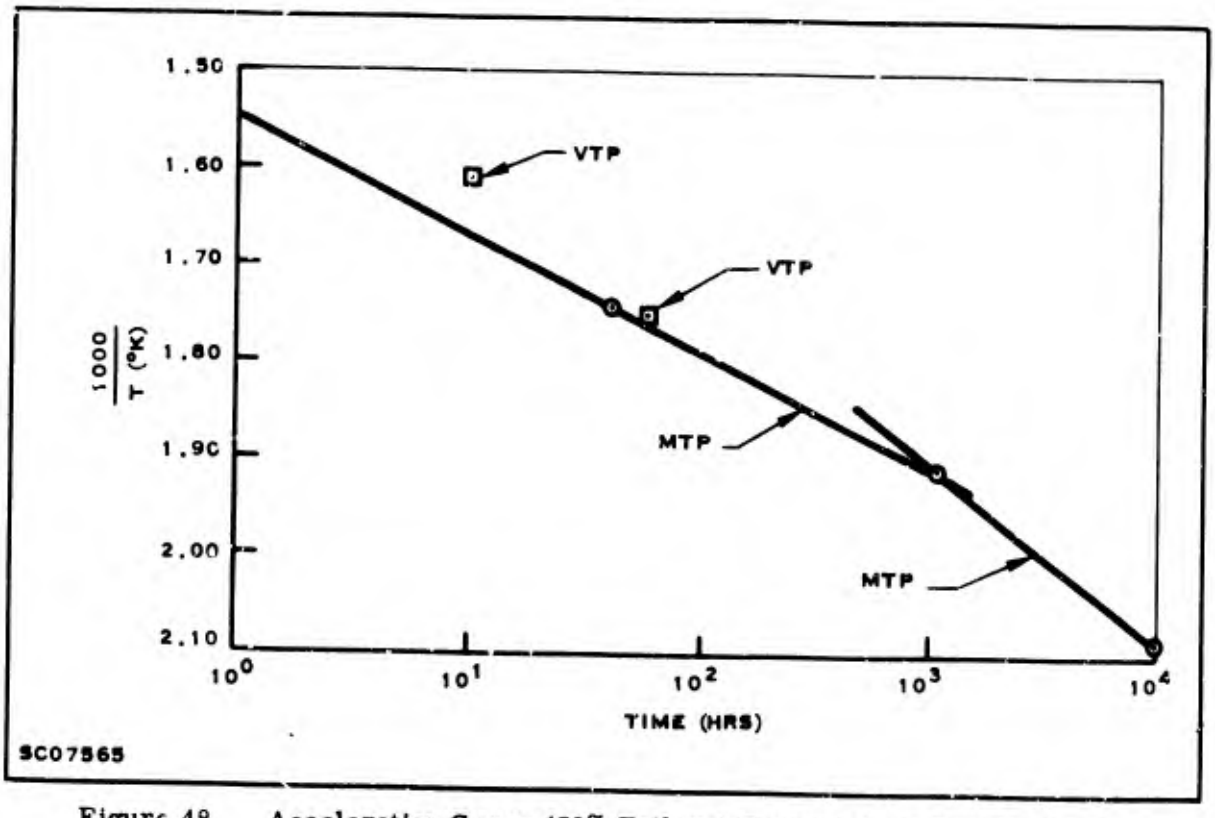

Figure 48. Acceleration Curve (50% Failure) Temperature Storage Tests (Main and Verification Test Programs)

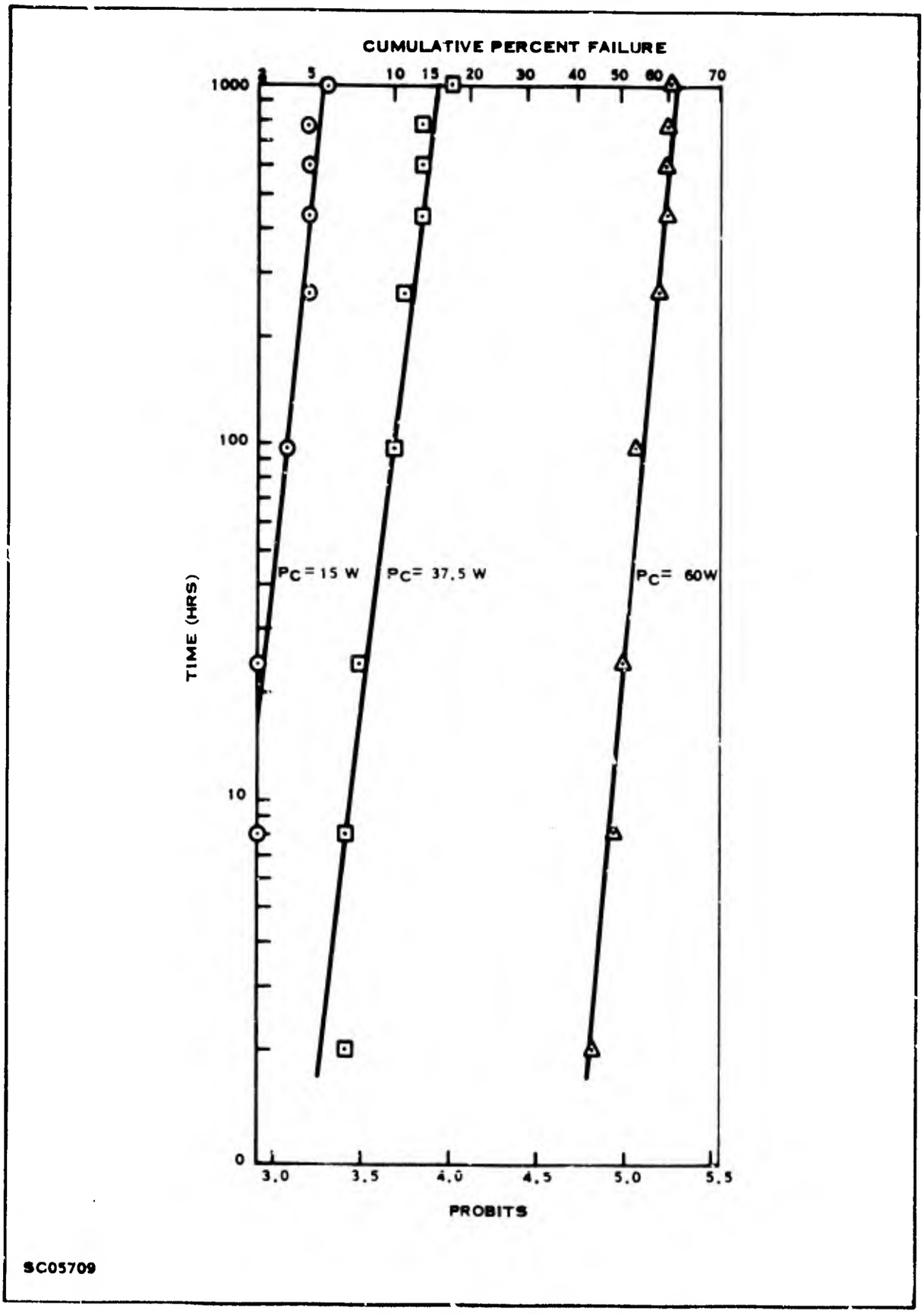

Figure 49. Cumulative Percent Failure Curves for Power Operating Life Test (Main Test Program)

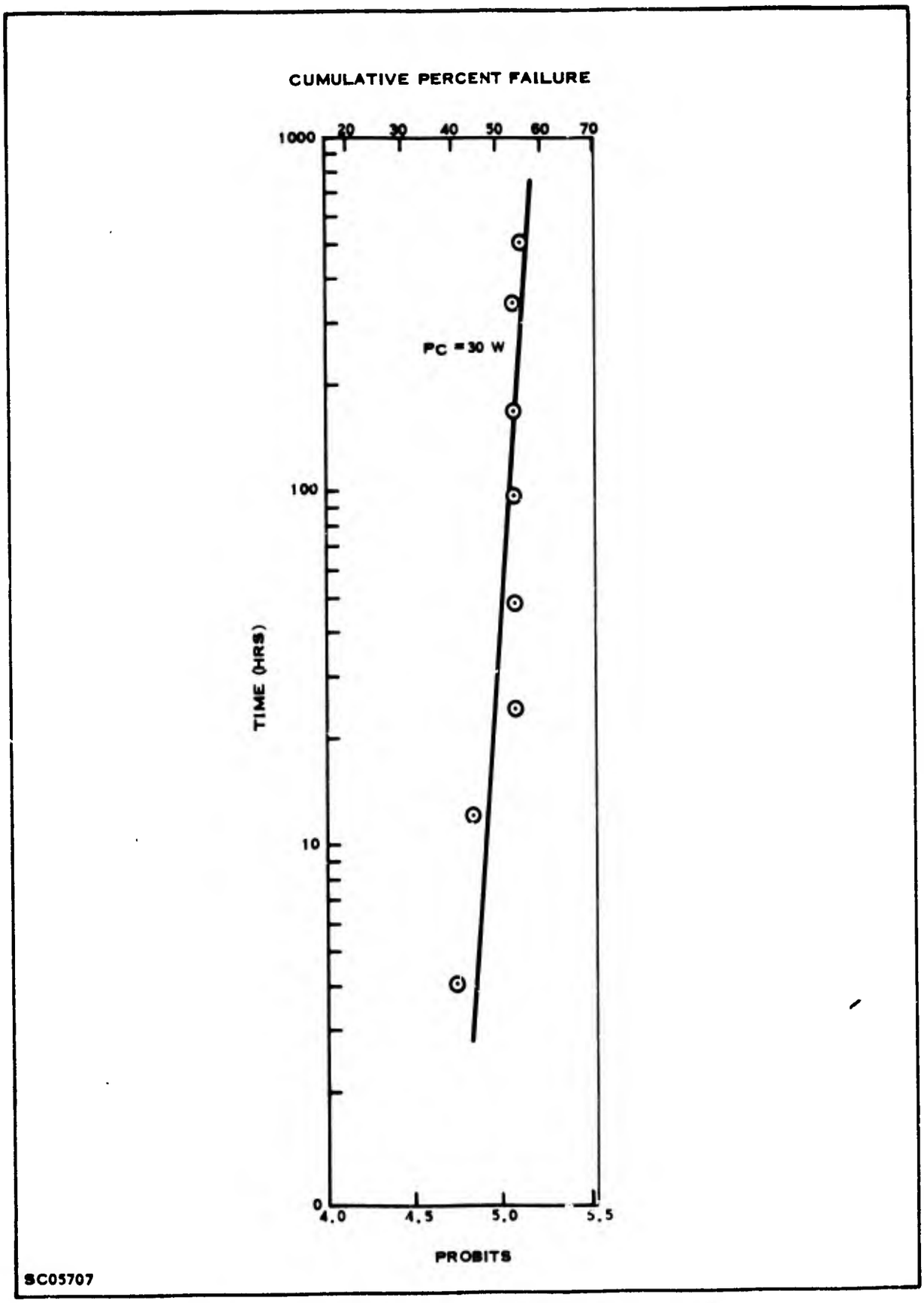

Figure 50. Cumulative Percent Failures for Power Operating Life Test (Preliminary Test Program)

The acceleration curve for 20 percent failures is plotted for the 15 W and 37.5 W tests in Figure 51. Included for comparison is the acceleration curve from Figure 45 for 20 percent failures on the temperature storage fixed stress tests of the MTP.

The slope of the power operating test acceleration curve is 1.3×10^{-4} and the activation energy is 1.5 eV. The junction temperatures used in plotting the power operating acceleration curve were calculated using an average θ_{J-C} value. This θ_{J-C} value of 3.2°C/W was an average of over 200 measurements using the 20 V ZOT method. Since the ambient temperature was 50°C, the junction temperature of the 15 W test was 98°C and of the 37.5 W test was 170°C.

The 60 W test was not used in calculating the acceleration curve because it was a much more severe overstress than the two lower stresses. For example, the estimated time to produce 10 percent failures would be about 10^{-6} hours, 10^{2} hours, and 10^{5} hours for the 60 W, 37.5 W, and 15 W tests, respectively. An interesting fact is that the cumulative percent failure curve for the 30 W test of the PTP is almost identical to the 60 W test of the MTP.

This similarity can be explained by referring to Figure 52 and Section V. The 30 W test was a 1.5 A, 20 V stress, giving a $T_{MAX}-T_{CASE}$ value of 150°C. The 60 W test was a 4.0 A, 15 V stress, giving a $T_{MAX}-T_{CASE}$ value of 160°C. Thus the devices on the two tests were exposed to comparable temperatures.

c. Verification Test Program

The cumulative percent failure curves for power operating life test for the VTP are given in Figure 53. Like the power operating tests of the MTP, they appear to be fairly linear. The regression equations are:

$$\lambda_p = 3.38 + 0.468 \log_{10} t \qquad \text{(30 W)}$$

$$\lambda_p = 3.41 + 0.417 \log_{10} t \qquad \text{(50 W)}$$

$$\lambda_p = 3.96 + 0.453 \log_{10} t \qquad \text{(80 W)}$$

The acceleration curves for 20 percent and 50 percent failures are plotted in Figure 54.

The θ_{J-C} values for all of the units on the VTP power operating tests were measured by the 15 V and 20 V ZOT method. The actual values of thermal resistance were used to compute the junction temperatures rather than an average value as was done in the MTP.

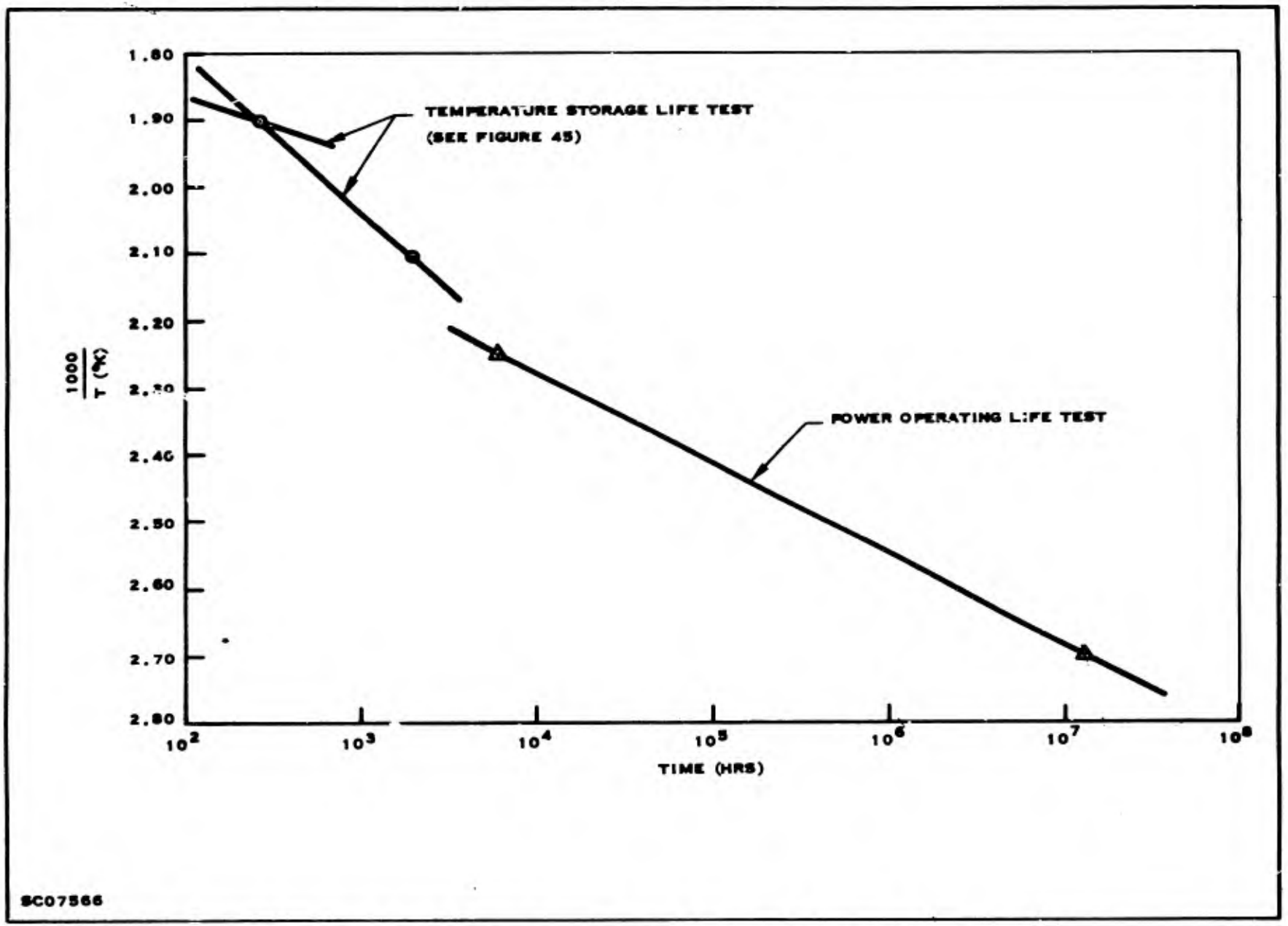

Figure 51. Cumulative Percent Failure Curves for Devices Rearranged According to T_J (15 V) (Verification Test Program)

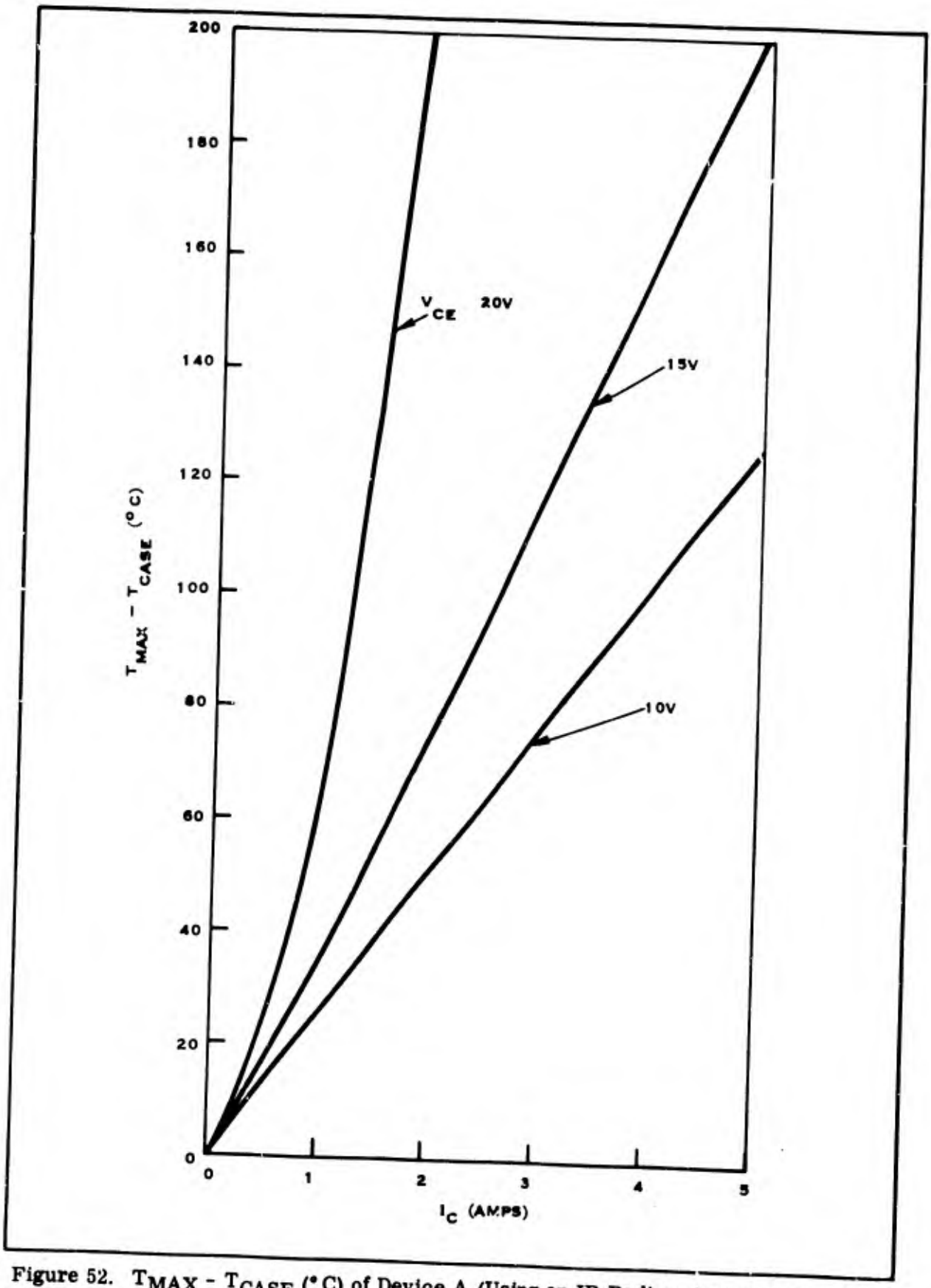

Figure 52. $T_{MAX} - T_{CASE}$ (°C) of Device A (Using an IR Radiometer) as a Function of Collector Current (I_C) for Several Constant Values of Collector to Emitter Voltages (V_{CE})

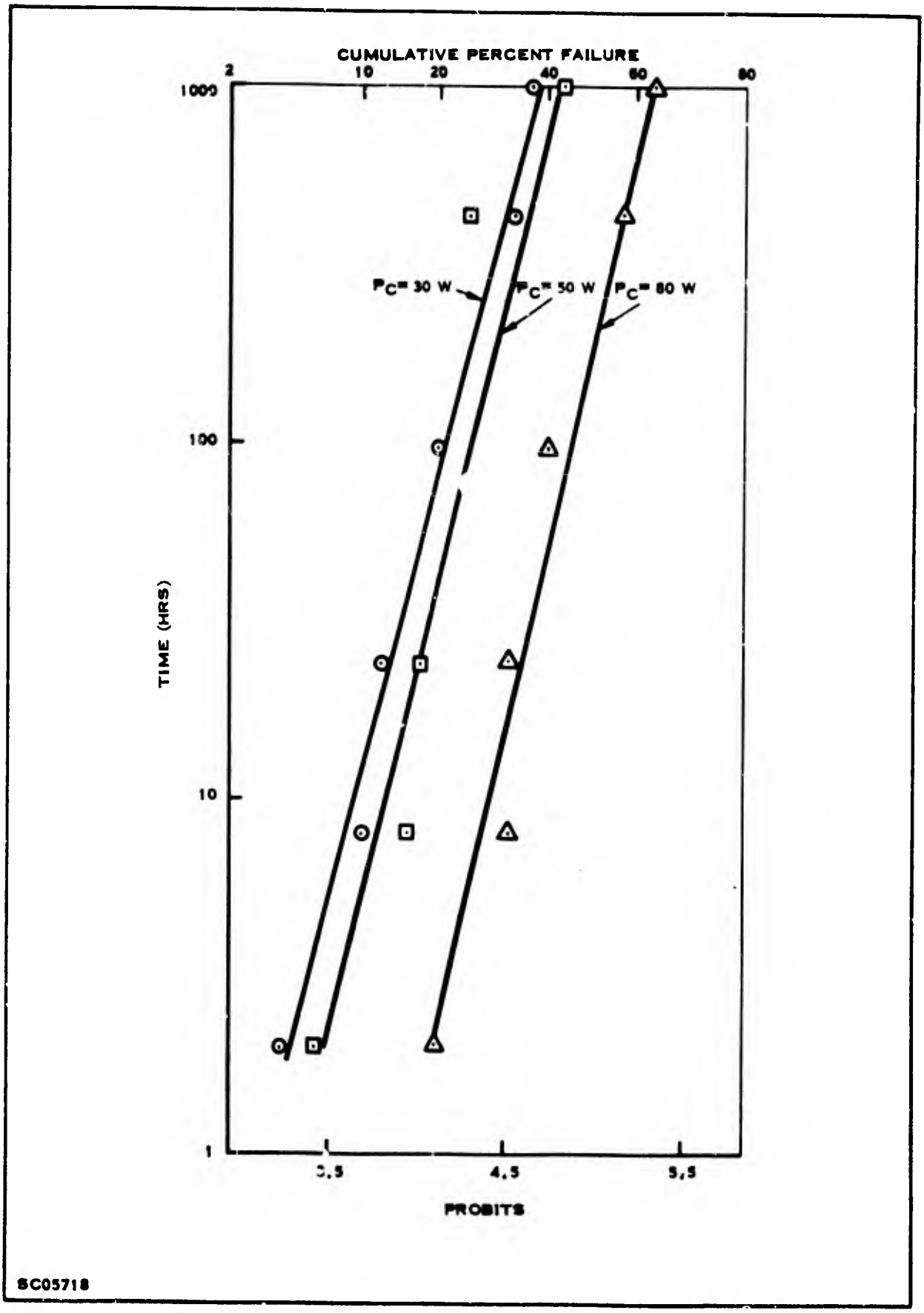

Figure 53. Cumulative Percent Failures for Power Operating Test (Verification Test Program)

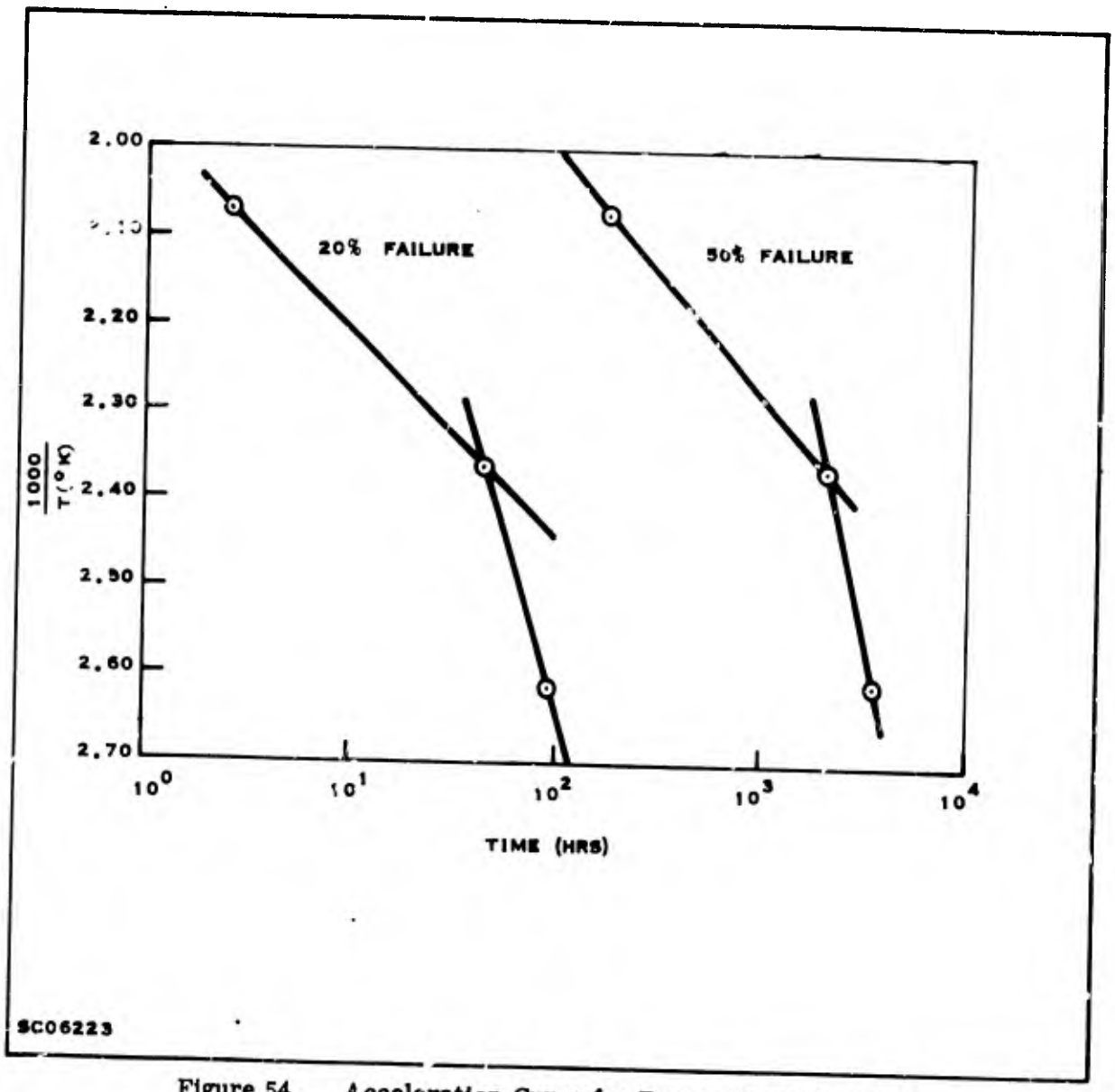

Figure 54. Acceleration Curve for Power Operating Test (Verification Test Program)

The units with θ_{J-C} measured by the 15 V ZOT method were divided into two groups, those with junction temperatures less than 150° C (Group 1) and those with junction temperatures above 150° C (Group 2). The median temperatures for these groups were 127°C and 193°C, respectively. The units with θ_{J-C} measured by the 20 V ZOT method were divided into two groups also, those with junction temperatures less than 150° C (Group 3) and those with junction temperatures above 150° C (Group 4). The median temperatures of these groups were 108° C and 181° C, respectively. The cumulative percent failure of the units in each group, irrespective of which power operating test they were on, has been plotted in Figures 55 and 56. It is assumed that the median junction temperature of each group was the stress temperature of each device in the group.

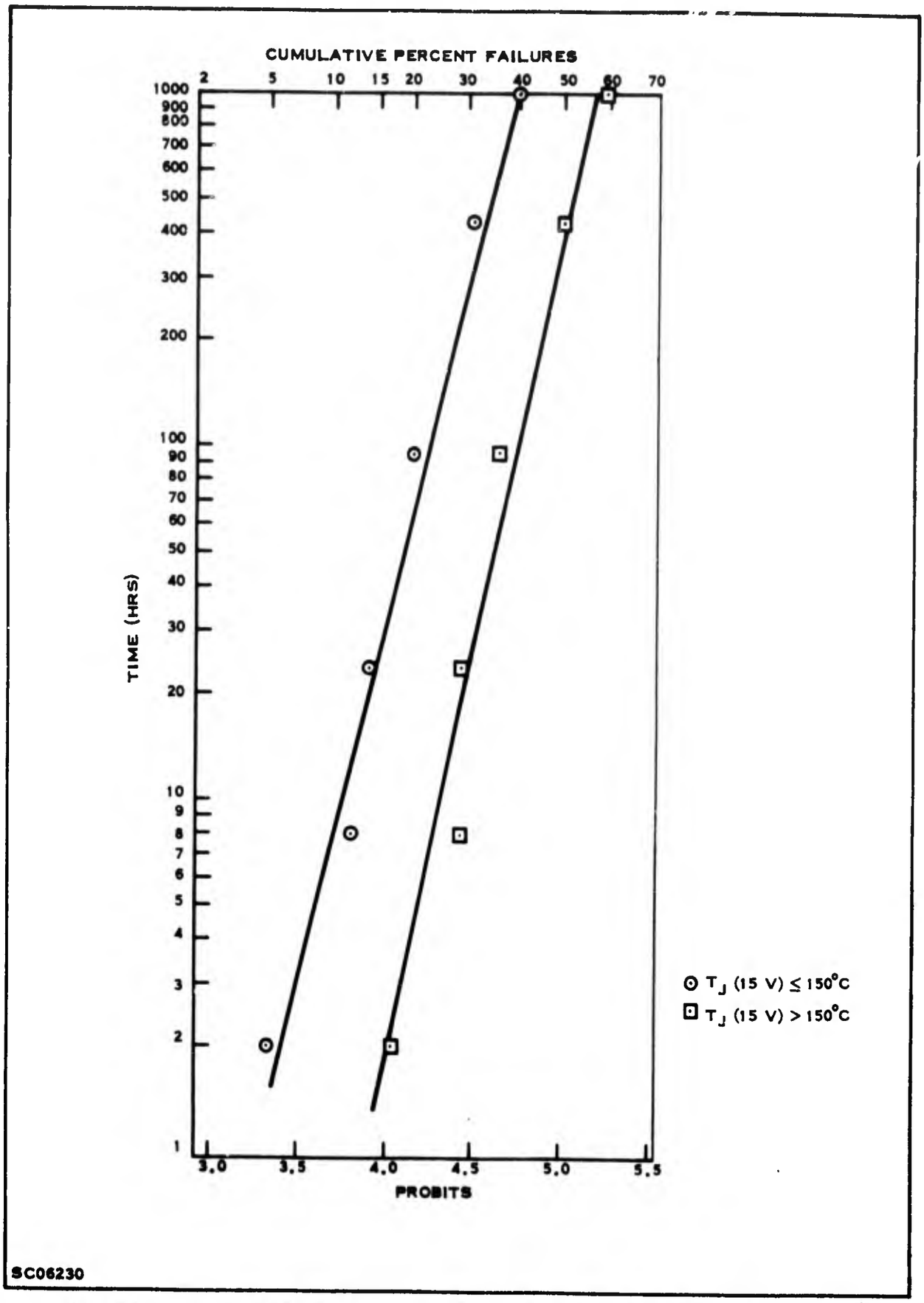

Figure 55. Cumulative Percent Failure Curves for Devices Rearranged According to T_J (15 V) (Verification Test Program)

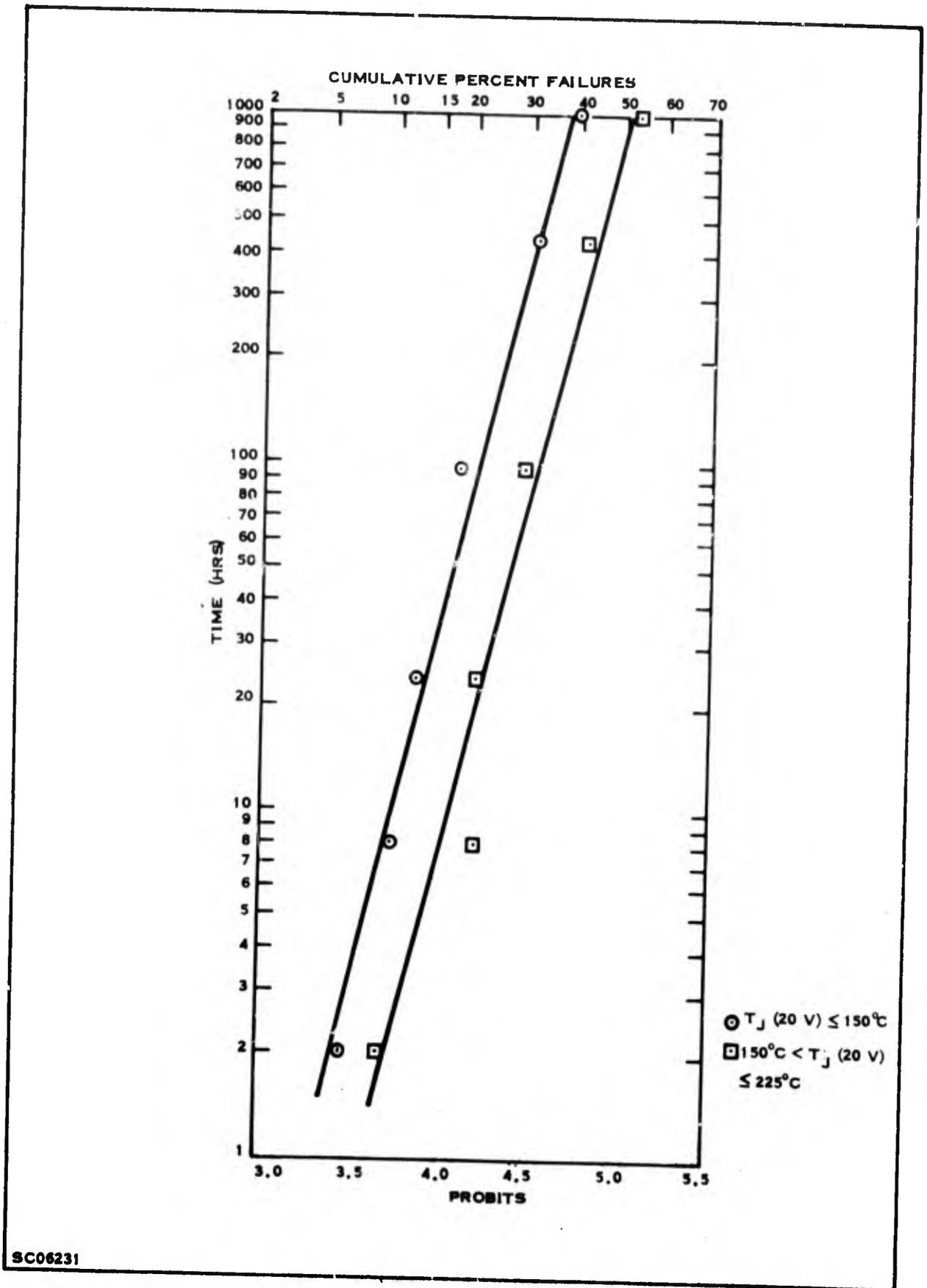

Figure 56. Cumulative Percent Failure Curves for Devices Rearranged According to T_J (20 V) (Verification Test Program)

The equations for these curves are given below.

$\lambda_p = 3.30 + 0.479 \log_{10} t$	T_J (15 V) $\leq 150°C$	Group 1
$\lambda_p = 3.91 + 0.419 \log_{10} t$	T_J (15 V) $> 150°C$	Group 2
$\lambda_p = 3.27 + 0.462 \log_{10} t$	T_J (20 V) $\leq 150°C$	Group 3
$\lambda_p = 3.53 + 0.495 \log_{10} t$	$150°C < T_J$ (20 V) $\leq 225°C$	Group 4

All four cumulative percent failure curves are plotted in Figure 57. Included for comparison is the 300° C VTP temperature storage curve.

The acceleration curves for these four groups are given in Figure 58. These curves are quite similar to those of Figure 54. A direct comparison is made in Figure 59.

The following approximate values were obtained for the activation energies:

20 percent Failure, 20 V Groups	$E_A = 0.29$ eV
20 percent Failure, 15 V Groups	$E_A = 0.69$ eV
50 percent Failure, 20 V Groups	$E_A = 0.22$ eV
50 percent Failure, 15 V Groups	$E_A = 0.51$ eV
20 percent Failure, Lower Curve, Figure 54	$E_A = 0.24$ eV
20 percent Failure, Upper Curve, Figure 54	$E_A = 0.85$ eV
50 percent Failure, Lower Curve, Figure 54	$E_A = 0.19$ eV
50 percent Failure, Upper Curve, Figure 54	$E_A = 0.72$ eV

4. REVERSE BIAS TEST RESULTS

a. Reverse Bias Tests

The reverse bias tests conducted during this contract are below:

Reverse Bias Step Stress	2 hours/step	Main Test Program (MTP)
	8 hours/step	Main Test Program (MTP)
	24 hours/step	Main Test Program (MTP)
	96 hours/step	Main Test Program (MTP)

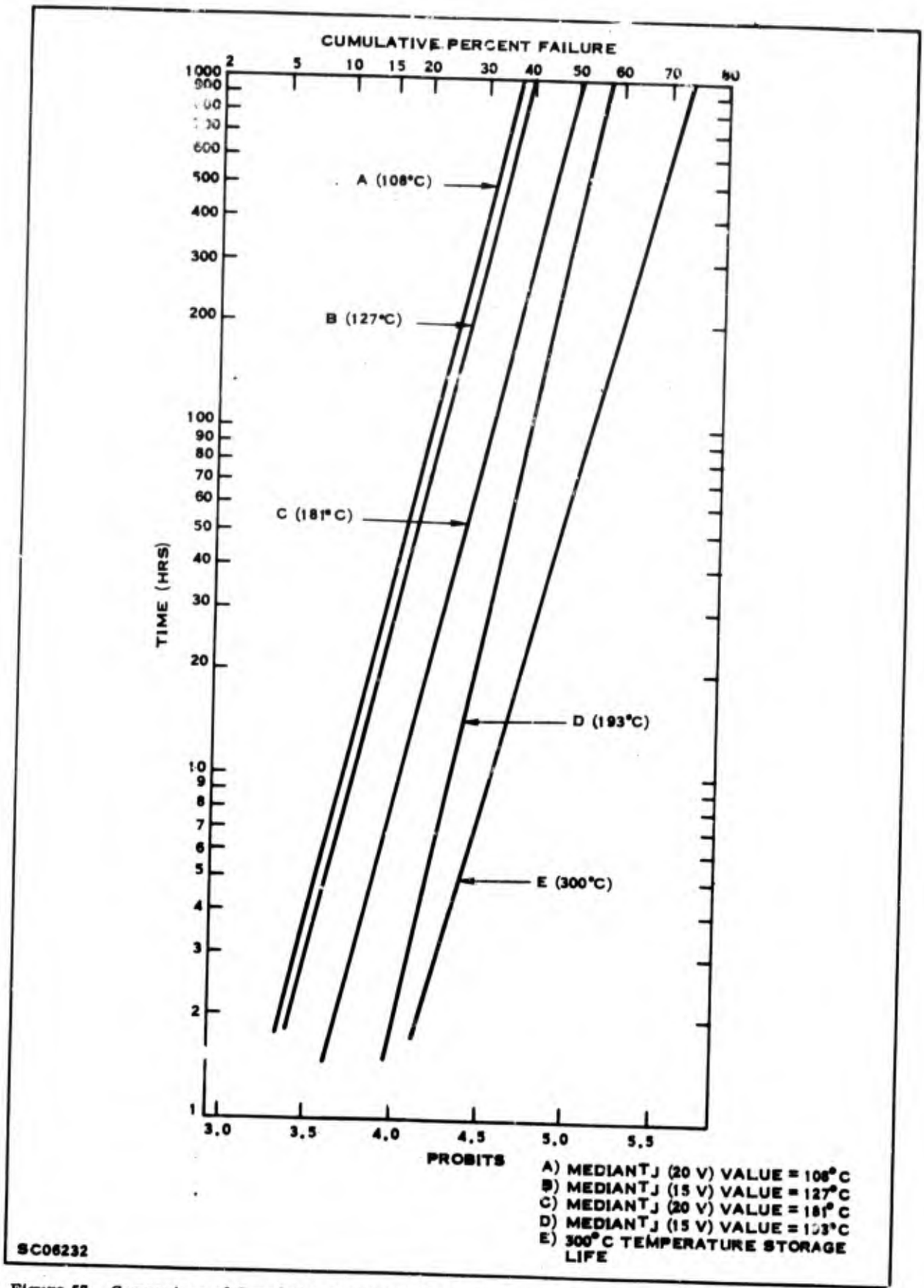

Figure 57. Comparison of Cumulative Percent Failure Curves for Devices Rearranged According to T_J With 300° C Storage Life Curve (Verification Test Program)

Reverse Bias Life Tests	125°C 1000 hours	Main Test Program (MTP)
	175°C 1000 hours	Main Test Program (MTP)
	225°C 1000 hours	Main Test Program (MTP)

b. Main Test Program

Data Analyses on these tests are discussed in Section IV-6. There was no clear pattern in the life test results and the step stress data were of little help in interpreting the life test data. In an attempt to interpret the life test results, the individual pretreatment group (Section IV) data were examined. It was found that the group which had reverse bias pretreatment and the group which had no pretreatment

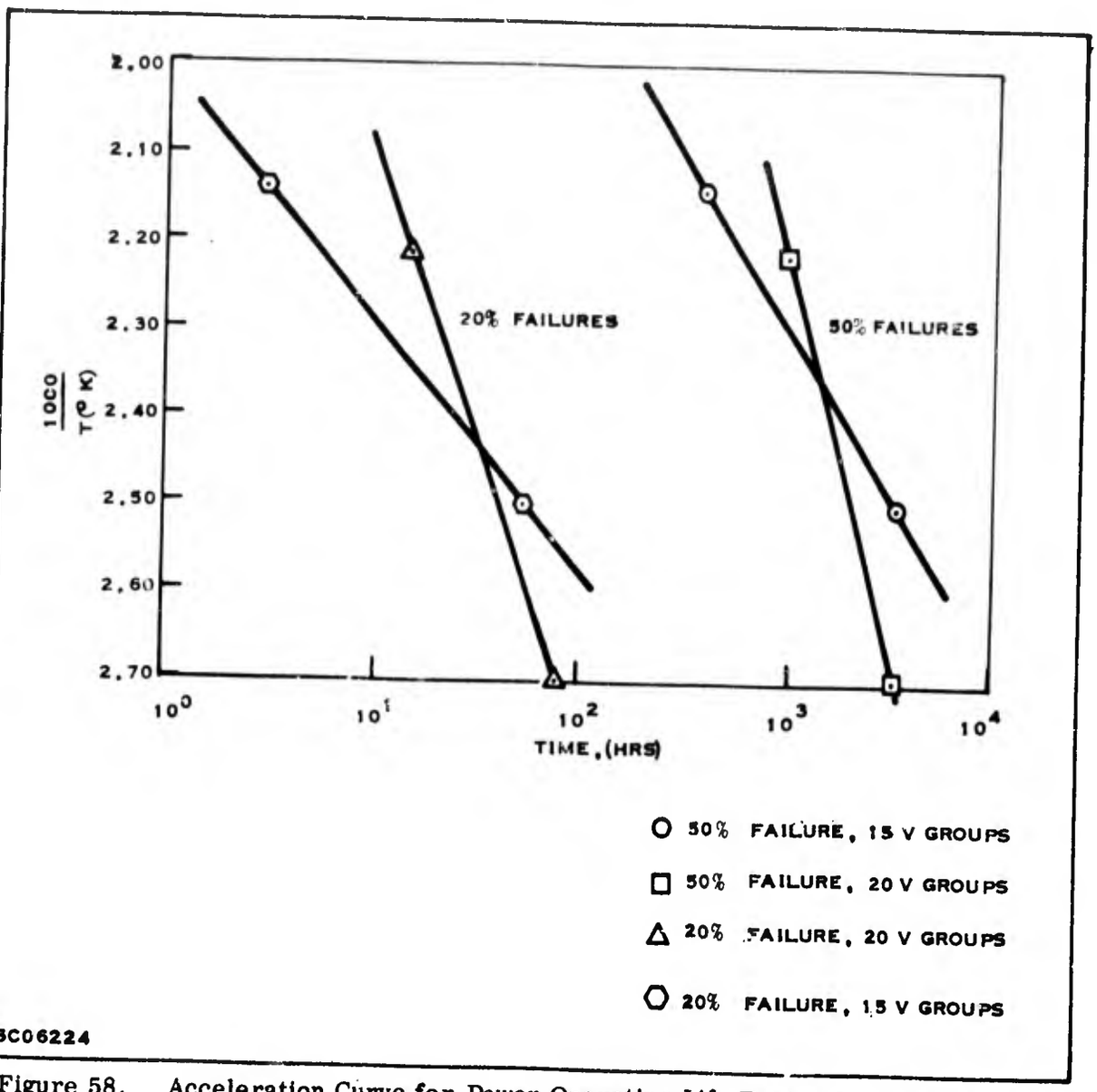

Figure 58. Acceleration Curve for Power Operating Life Tests, Devices Regrouped According to T_J (Verification Test Program)

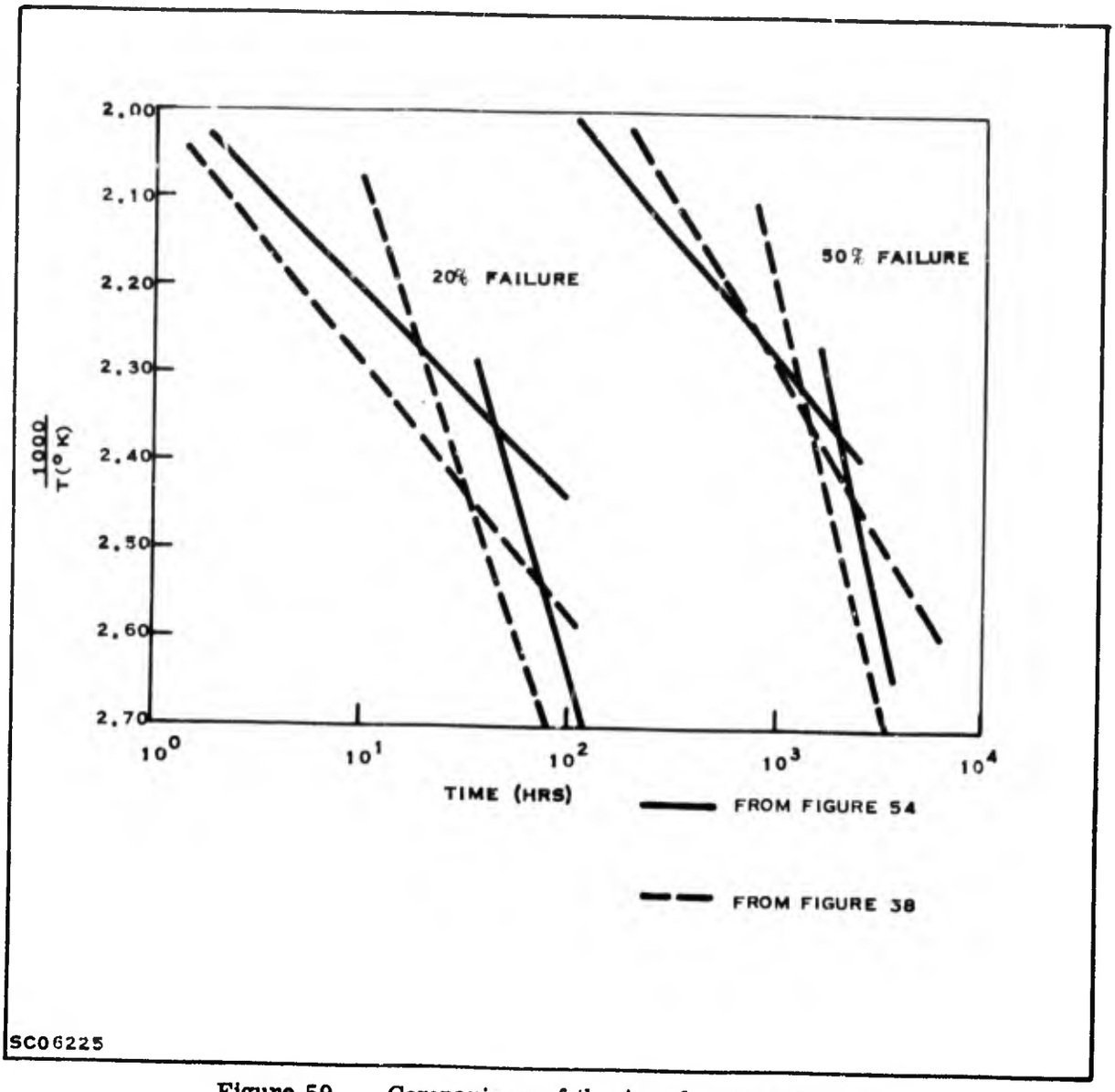

Figure 59. Comparison of the Acceleration Curves (Verification Test Program)

responded in the same way to the reverse bias stress on the life tests. Completely different cumulative percent failure curves were obtained for the groups which were pretreated by power operating or temperature stress. Interpretation of the results of the data regrouped into two groups according to pretreatment is further complicated by the appearance of a large number of catastrophic failures (shorts) as discussed in Section IV. The failures were of three types. First, there were a large number of degradation failures. Second, a number of shorts eventually appeared which had previously been degradation failures. Third, some of these shorts were not previously degradation failures. Cumulative percent failure curves have been plotted for many of the combinations mentioned above. For example, plots of cumulative percent failure for shorts which had not previously been degradation failures were constructed, for shorts which had previously been degradation failures for shorts of any kind, for

degradation failures ignoring shorts, for total failures, and all of these were considered separately for the two different pretreatment groups. These plots gave little insight on how to interpret the data.

To illustrate, some of these plots are included herein. The cumulative percent failure curves for the reverse bias tests in the MTP are given in Figure 60. Cumulative percent failure curves for the reverse bias tests with pretreatment groups 1 and 3, and 2 and 4 combined are given in Figures 61, 62, and 63. Total failures, both degradation and catastrophic, are plotted in these figures.

Considerably more work is needed to interpret the test results. Tables 18, 19, and 20 summarize the number of failures for the three levels of the reverse bias fixed stress tests of the MTP.

5. DISCUSSION OF RESULTS

a. Temperature Storage Results

The lack of agreement between the results of the fixed and step stress temperature storage tests of the MTP led to additional analysis of the data. The possibility of a discontinuity in the cumulative percent failure curves of the step stress results and in the acceleration curves of the fixed stress tests was considered. This led to good agreement of the activation energies calculated from the fixed stress and step stress results for temperatures below 250°C. In the case of the fixed stress tests, the activation energy was calculated from the slope of the acceleration curve. The other calculation of the activation energy was based on the relation σ_s / σ_t = slope acceleration curve. In both cases an activation energy of 1.0 eV was found. The failure rate at 80°C was estimated to be about 10^{-4}%/1000 hours.

The activation energy calculated from the 250°C to 300°C position of the fixed stress acceleration curve was 1.8 eV. One of the primary failing parameters for the temperature storage fixed stress tests of the MTP was I_{CEO} (70 V). Considering a device as a failure only on the basis of exceeding the I_{CEO} (70 V) failure limits led to the calculation of an activation energy of 2.2 eV for the I_{CEO} (70 V) failure mechanism. This calculation was based on data valid from 250°C to 300°C.

The data points calculated from the 300°C and 350°C temperature storage tests of VTP on a device of the same family as the device used in the MTP were compatible with the acceleration curve of the fixed stress MTP.

The temperature storage test results cannot be considered definitive, since a value of $\sigma_s = 3.7 \times 10^{-4}$ was calculated for step stress data above 250°C and using the relation σ_s / σ_t = slope of acceleration curve would lead to an activation energy of 0.67 eV, entirely different from the 1.8 eV calculated for the MTP fixed stress results.

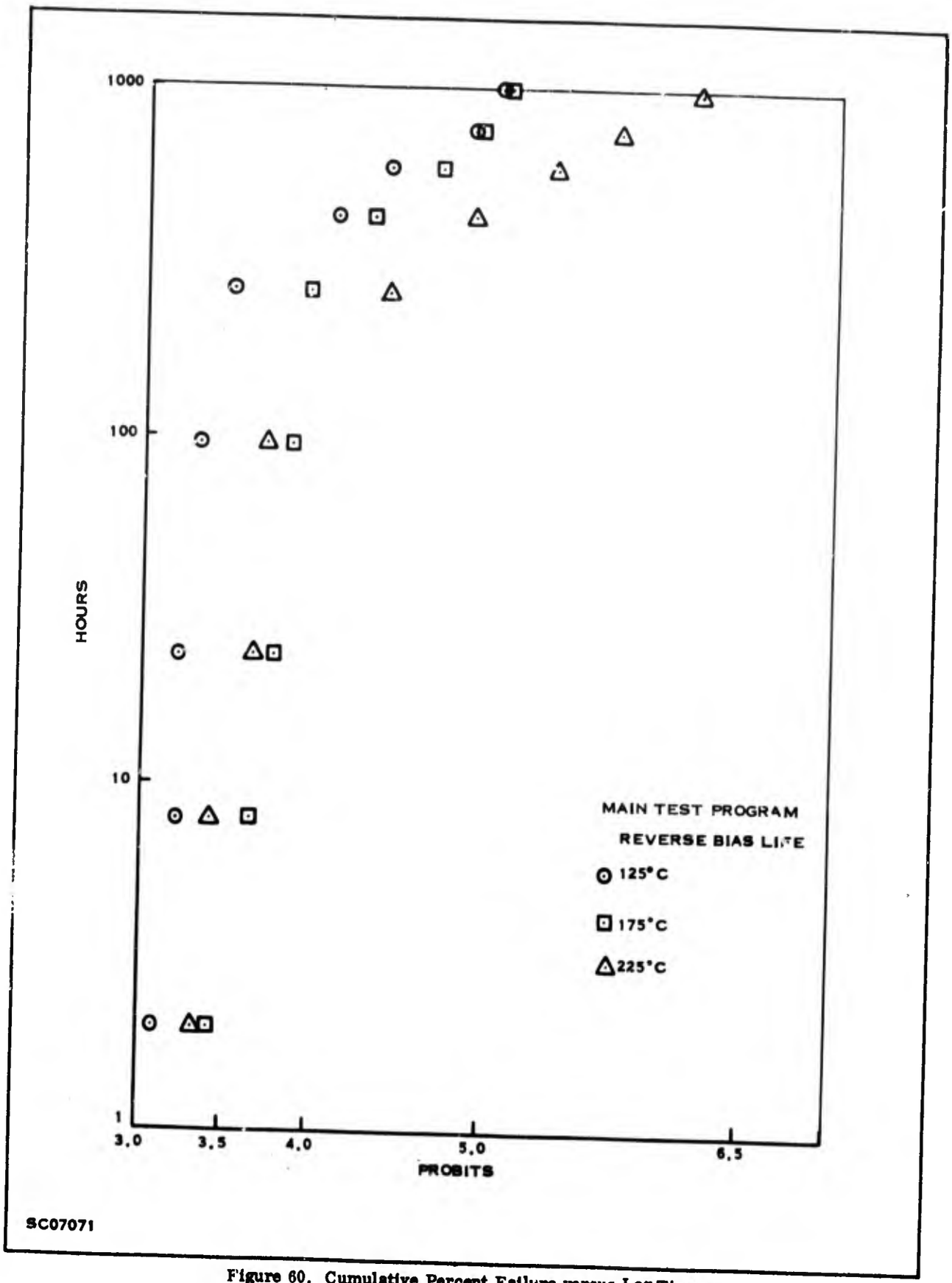

Figure 60. Cumulative Percent Failure versus Log Time for Reverse Bias Life Test (Main Test Program)

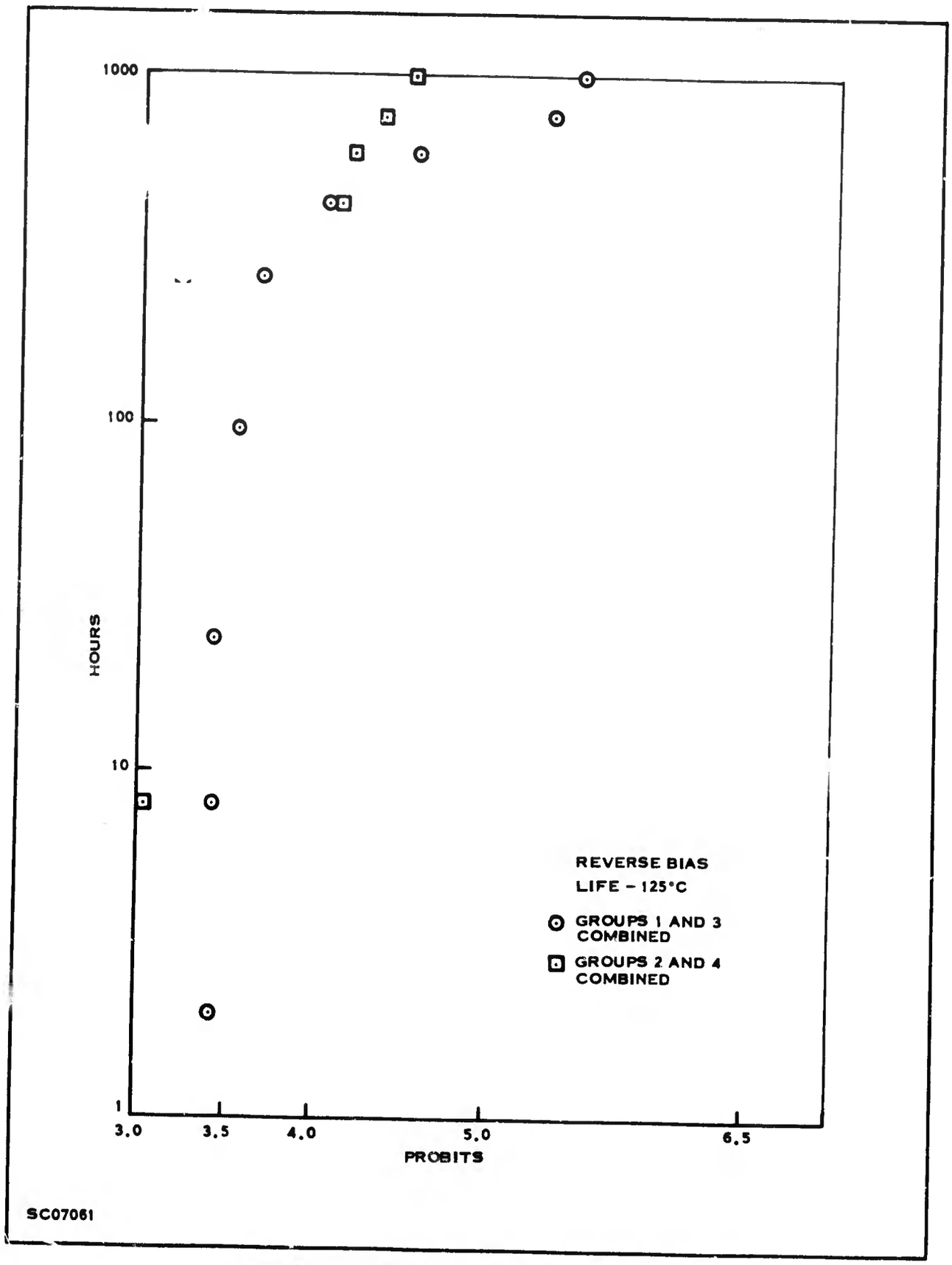

Figure 61. Cumulative Percent Failure versus Log Time For Reverse Bias Life Test (Main Test Program)

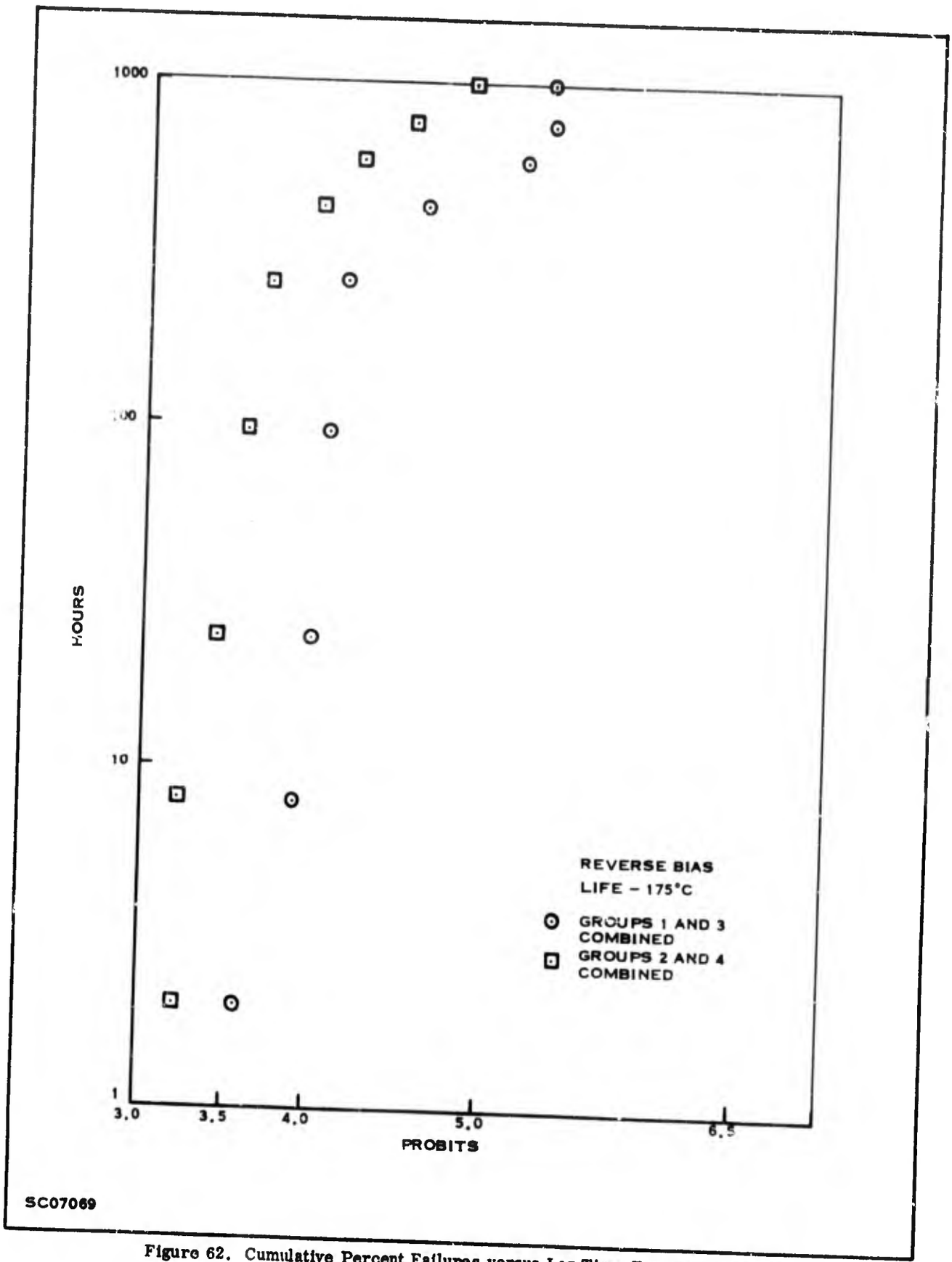

Figure 62. Cumulative Percent Failures versus Log Time For 175°C Reverse Bias Life Test (Main Test Program)

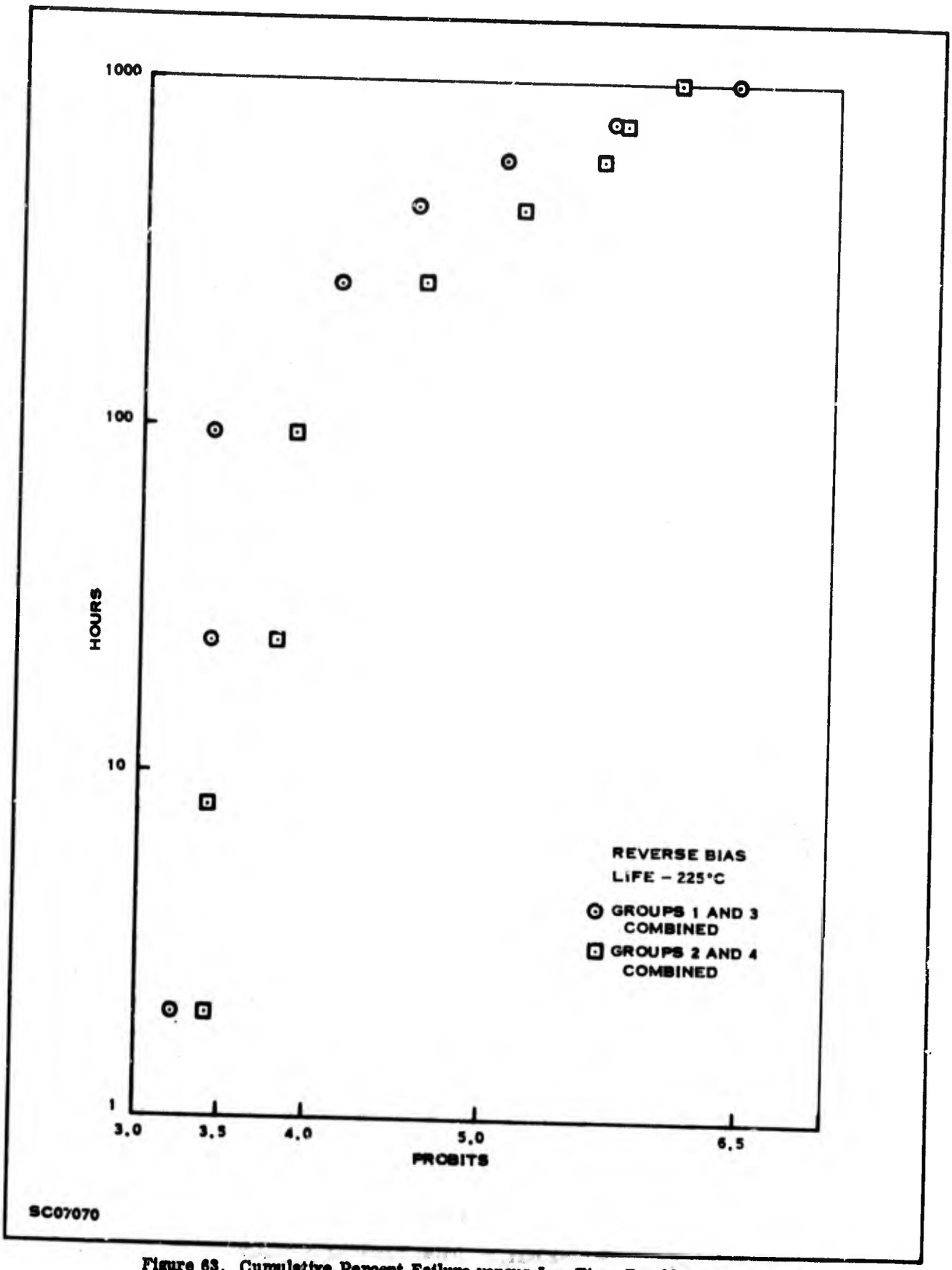

Figure 63. Cumulative Percent Failure versus Log Time For 225°C Reverse Bias Life Test (Main Test Program)

Table 18. Main Test Program Failure Summary Reverse Bias Life 125°C

Pretreatment Group*	Step 1 (2 hr)	Step 2 (8 hr)	Step 3 (24 hr)	Step 4 (96 hr)	Step 5 (264 hr)	Step 6 (432 hr)	Step 7 (600 hr)	Step 8 (768 hr)	Step 9 (1000 hr)	Total Failures
1	2	0	0	0	0	2	5	5	1	15
2	0	1	0	0	0	4	0	2	1	8
3	1	0	0	1	1	2	3	10	2	20
4	0	0	0	0	1	4	1	1	2	9

Failure Definition: Both degradation and catastrophic failures by criteria given in Section III.

Pretreatment Group*	Step 1	Step 2	Step 3	Step 4	Step 5	Step 6	Step 7	Step 8	Step 9	Total Failures
1	0	0	0	0	0	2	3	4	0	7
2	0	1	0	0	0	4	0	2	0	2
3	0	0	0	0	0	2	2	9	0	11
4	0	0	0	0	0	4	1	1	1	3

Failure Definition: Shorts not previously degradation failures

Pretreatment Group*	Step 1	Step 2	Step 3	Step 4	Step 5	Step 6	Step 7	Step 8	Step 9	Total Failures
1	0	0	0	0	0	0	0	2	0	2
2	0	0	0	0	0	0	0	1	0	1
3	0	0	0	0	0	0	0	1	4	5
4	0	0	0	0	0	0	0	0	0	0

Failure Definition: Shorts that were previously degradation failures

* 1 - Temperature Storage; 2 - Reverse Bias; 3 - Power Operating; 4 - Control

Table 19. Main Test Program Failure Summary Reverse Bias Life 175°C

Pretreatment Group*	Step 1 (2 hr)	Step 2 (8 hr)	Step 3 (24 hr)	Step 4 (96 hr)	Step 5 (264 hr)	Step 6 (432 hr)	Step 7 (600 hr)	Step 8 (768 hr)	Step 9 (1000 hr)	Total Failure
1	0	3	0	0	1	6	5	2	0	17
2	1	0	0	0	1	1	1	3	4	11
3	4	0	1	1	0	1	6	1	0	14
4	1	0	1	1	0	2	2	2	2	11

Failure Definition: Both degradation and catastrophic failures as per criteria given in Section III

Pretreatment Group*	Step 1	Step 2	Step 3	Step 4	Step 5	Step 6	Step 7	Step 8	Step 9	Total Failures
1	0	0	0	0	0	2	5	2	0	9
2	0	0	0	0	0	0	1	1	4	6
3	0	0	0	0	0	0	6	1	0	7
4	0	0	0	0	0	0	0	2	2	4

Failure Definition: Shorts not previously degradation failures

Pretreatment Group*	Step 1	Step 2	Step 3	Step 4	Step 5	Step 6	Step 7	Step 8	Step 9	Total Failures
1	0	0	0	0	0	0	4	1	0	5
2	0	0	0	0	0	0	0	0	2	2
3	0	0	0	0	0	0	0	0	0	0
4	0	0	0	0	0	0	0	1	0	1

Failure Definition: Shorts that were previously degradation failures

* 1 - Temperature Storage; 2 - Reverse Bias; 3 - Power Operating; 4 - Control

Table 20. Main Test Program Failure Summary Reverse Bias Life 225°C

Pretreatment Group*	Step 1 (2 hr)	Step 2 (8 hr)	Step 3 (24 hr)	Step 4 (96 hr)	Step 5 (264 hr)	Step 6 (432 hr)	Step 7 (600 hr)	Step 8 (768 hr)	Step 9 (1000 hr)	Total Failure
1	0	1	0	0	6	3	3	8	2	23
2	0	0	0	0	7	4	7	0	3	22
3	0	0	0	0	1	4	7	3	6	23
4	0	0	3	1	4	7	1	2	1	21

Failure Definition: Both degradation and catastrophic failures as per criteria given in Section III

Pretreatment Group*	Step 1	Step 2	Step 3	Step 4	Step 5	Step 6	Step 7	Step 8	Step 9	Total Failures
1	0	0	0	0	1	2	3	6	2	14
2	0	0	0	0	1	1	5	0	2	9
3	0	0	0	0	0	1	5	2	4	12
4	0	0	0	0	0	3	0	2	1	6

Failure Definition: Shorts not previously degradation failures

Pretreatment Group*	Step 1	Step 2	Step 3	Step 4	Step 5	Step 6	Step 7	Step 8	Step 9	Total Failures
1	0	0	0	0	0	1	3	1	3	8
2	0	0	0	0	0	0	5	5	1	11
3	0	0	0	0	0	0	0	3	2	5
4	0	0	0	0	1	0	2	3	3	9

Failure Definition: Shorts that were previously degradation failures
* 1 - Temperature Storage; 2 - Reverse Bias; 3 - Power Operating; 4 - Control

The step stress data would have been adequate for determining acceleration factors if there had only been one failure mechanism operative over the temperature range considered. As it was, the two (or more) acceleration curves were poorly defined. The fixed stress temperature storage data, for the PTP, the MTP and for the VTP indicated that a number of mechanisms were operative. Pronounced discontinuities in the cumulative percent failure curves around 250°C to 275°C were evident. These mechanisms are associated with degradation failures and are more difficult to characterize than catastrophic failures where failure analysis on the failed device often clearly indicates the failure mechanism.

There were other attempts to clarify the temperature storage test results. The possibility that the appropriate failure distribution was Weibull rather than log-normal was considered but this did not assist in the interpretation of the data. A correction factor for cumulative stress damage on the step stress tests was also considered, but this did not appreciably increase the agreement of the fixed and step stress data.

b. Power Operating Results

An activation energy of 1.5 eV was calculated from the acceleration curve of the 15 W and 37.5 W power operating tests of the MTP. The junction temperatures were calculated using an average θ_{J-C} value. The device operating at 15 W with an ambient temperature of 50°C had a failure rate of 2×10^{-3}%/1000 hours; at 37.5 W and same ambient temperature the failure rate was about 3%/1000 hours.

The θ_{J-C} value for each device on the power operating test of the VTP was measured using both the 15 V and 20 V ZOT methods. Calculating the junction temperature of each device and grouping the devices for purposes of analysis according to calculated junction temperature, independent of which of the three power operating tests the device was actually on, gave the same acceleration curves as using an average θ_{J-C} value for all devices on the tests. There appear to be two reaction mechanisms operative, one below 140°C and one about 140°C. Activation energies for these mechanisms are about 0.20 eV and 0.70 eV, respectively.

c. Reverse Bias Results

Little information of value was extracted from the reverse bias tests of the MTP. Consideration of the cumulative percent failure curves of each pretreated group for the temperature storage test revealed little difference. However, there was considerable difference in the response of the pretreated groups to reverse bias stress. The groups given temperature storage and power pretreatment responded similarly to

the reverse bias stress. Devices pretreated using reverse bias pretreatment or else no pretreatment responded in the same way. This latter similarity would be expected since the reverse bias pretreatment can be considered as an early application of the reverse bias stress to a group with no pretreatment.

However, even considering the test results of the devices given temperature storage or power pretreatment separately from the test results of the devices given reverse bias pretreatment or no pretreatment did not provide enough information to allow an estimate of an activation energy. The fact that there was more than one kind of failure complicated the analysis.

The early failures were degradation failures but the later failures were shorts. Some of the devices which were degradation failures remained so throughout the test; some later became shorts. Some devices became shorts without having previously been degradation failures. There appears to be more than one mechanism operative.

SECTION VII

SCREENING RESULTS

1. INTRODUCTION

This section contains the pretreatment screening results from the Main Test Program using the computer program SERF, a discussion of the high stress screening results, a discussion of some linear discriminant analysis results and a discussion of the development of a screening procedure.

2. INTRODUCTION TO SERF RESULTS

The description and flow chart of the computer program SERF will be found in Appendix G. This program is designed to isolate preindicators of failure, i.e. to determine the most suitable parameter for predicting which device in the population will fail prematurely under stress, and to assist in developing screening procedures. Before the results of using this computer program are discussed, the criterion used for deciding the best preindicating parameter and the level of screening on that parameter should be determined. Suppose, for example, 5 devices are removed by screening at a certain level, i.e., discarding all devices with parameter readings above this level. In screening a little lower, 6 bad devices may be removed but suppose 1 good device is removed also. In screening even lower, more bad devices may be removed but also more good ones. The question is then, at what level should screening stop, i.e. what should be the screening criterion?

During initial studies, the screening criterion, e, used was

$$e = \frac{(\% \text{ Failures Removed})}{(\% \text{ Population Removed})}$$

This criterion, however, easily leads to trivial results. Consider as an example a collection of 100 devices, 15 of which failed during the high stress test. If screening on parameter 1 removed one device which was a failure, the e value would be

$$e_1 = \frac{\left(\frac{1}{15}\right)}{\left(\frac{1}{100}\right)} = 6.67 \quad (e_1 \text{ refers to parameter 1, etc.})$$

If screening on parameter 2 would have removed 12 devices, 11 of which were failures, the e value would have been

$$e_2 = \frac{\left(\frac{11}{15}\right)}{\left(\frac{12}{100}\right)} = 6.11,$$

and parameter 1 would have been selected as the screening parameter although parameter 2 is much more interesting as a preindicator of failure. To circumvent this difficulty a modified screening criterion was used. A definition of e* was made. The modified screening criterion, e* is defined as

$$e^* = 0.5 + 0.5\,(F_f \quad F_g)$$

where F_f = Fraction of total failures removed

F_g = Fraction of total good devices removed

This e* value can vary from 0 to 1, the first case occurring when all of the good and none of the bad in the population are removed; the second, when all of the bad and none of the good in the population are removed. Returning to the example mentioned above, screening on parameter 1 would give

$$e_1^* = 0.5 + 0.5\left[\left(\frac{1}{15}\right)-\left(\frac{0}{85}\right)\right] = 0.53 \quad (e_1^* \text{ refers to parameter 1, etc.})$$

and parameter 2 would give

$$e_2^* = 0.5 + 0.5\left[\left(\frac{11}{15}\right)-\left(\frac{1}{85}\right)\right] = 0.86$$

Clearly parameter 2 would have been selected as the screening parameter. However, there are limitations in the use of e * as a definition of screening efficiency. Consider, for example, 100 devices, 15 of which are failures and suppose that screening on parameter 1 removes 15 devices, 9 of which are failures, and screening on parameter 2 removes 7 devices, all of which are failures. Then

$$e_1^* = 0.5 + 0.5\left[\left(\frac{9}{15}\right) - \left(\frac{6}{85}\right)\right] = 0.77$$

$$e_2^* = 0.5 + 0.5\left[\left(\frac{7}{15}\right) - \left(\frac{0}{85}\right)\right] = 0.73$$

Table 21. Summary of Pretreatment Screening Results
(Main Test Program)

Fixed Matrix Tests	Percent of High-Stress Failures Removed (Initial Data Used)				Percent of High-Stress Failures Removed (Post-Pretreatment Test Data Used)			
	Group 1 Temperature Storage	Group 2 Reverse Bias	Group 3 Power Operating	Group 4 Control	Group 1 Temperature Storage	Group 2 Reverse Bias	Group 3 Power Operating	Group 4 Control
Temperature Storage Life								
200°C	50	†	20	25	50	50	80	
250°C	50	33	50	30	56	33	50	
300°C	36	38	67	22	43	44	61	N
Average *	44	39	54	25	50	41	60	O
Reverse Bias Life								T
125°C	47	25	55	33	60	38	55	A
175°C	47	45	43	45	59	45	50	P
225°C	50	33	28	9	60	25	43	P
Average *	48	35	46	29	60	35	51	L
Power Operating Life								I
15.0 W	50	†	100	100	50	†	100	C
37.5 W	33	22	100	40	33	33	100	A
60.0 W	63	30	27	35	50	38	80	B
Average *	57	27	35	39	48	36	82	L
								E
Average All Tests	48	35	47	30	54	33	60	
Average All Tests and All Groups	--	--	--	33	--	--	49	

*The average is calculated by summing the number of failures removed and dividing it by the sum of the number of later failures.

†Results not available

Clearly parameter 2 is the more valid preindicator of failure, but parameter 1 would have been selected for screening. Thus we can see that e is too restrictive to use as our definition of screening efficiency, since using it favors the removal of practically none of the good devices and, on the other hand, e* is too weak a definition for us to use since using it favors the removal of many bad devices with too little weight being given the good devices removed. It was finally decided to use e* as our definition of screening efficiency but to impose the additional constraints that if n devices were removed by screening, no more than m of these could be good units; these values are given below:

Number of Devices Removed by Screening (n)	Number of Good Units Allowed in n (m)
1 to 3	0
4 to 6	1
7 to 15	2
16 to 20	3
over 20	4

3. PRETREATMENT SCREENING

The pretreatment stresses in the Main Test Program were used to see if device behavior during low stress was indicative of future failure under high stress. More specifically, did device behavior under one type of pretreatment stress such as reverse bias preindicate later device failure under a different kind of high stress such as temperature storage or was the prediction of failures on a particular high stress only possible from behavior during the same kind of pretreatment stress? The successful prediction of failures from low stress pretreatment data would enable a screening procedure to be developed to eliminate failures from a particular kind of high stress. Further, if device behavior during a particular pretreatment was indicative of future failure under a different kind of stress, this information could be of assistance in understanding the high-stress failure mechanism.

The pretreatments are described in detail in Section IV-4a. To review briefly, there were four pretreatment groups; group 1 was temperature storage, group 2 was reverse bias, group 3 was power operating, and group 4 was the control.

Some results of this pretreatment screening using the computer program SERF are summarized in Table 21. There were two screening passes for devices from each group which were used for the data obtained at the readout step before (initial data) and after pretreatment (post pretreatment test data). There are only initial data for the control since no pretreatment was received. The percentage of later failures which could have

been removed by screening on initial or post readings are given in the table. In this case the rule used was that no good devices could be removed in this screening. Many other schemes could have been used, such as the e and e* values mentioned in subsection 2 of this chapter, but it was thought appropriate to use this criterion in comparing the merits of the different pretreatments.

To assist in understanding Table 21 consider, for example, the 200° C storage life information. Fifty percent of the devices which were given storage pretreatment (group 1) and which later failed during the 200°C storage life test could have been removed by screening on the data available before pretreatment. Similarly, 20% of the devices which were given power operating pretreatment (group 3) and later failed on the 200°C storage life test and 25% of the control sample (group 4) which was not given any pretreatment and which later failed on the 200°C storage life test could have been removed by screening on the initial data.

Screening can be done also on the parameter values read after pretreatment and also on the delta and percent changes of these parameters which occurred as a result of the pretreatment. It would be suspected that screening on parameter changes due to stress would give better results than only screening on the initial values. The values in the last three columns of the 200°C storage life test illustrate this increase in predictability. Using initial data only 20% of the devices which were given power operating pretreatment (group 3) and which later failed on the 200°C storage life test could have been screened out, but 80% of the later failures could have been removed by using the post pretreatment test data.

Considering all of the results in Table 21, it can be seen that screening after reverse bias pretreatment (group 2) does not give much improvement over screening on initial data. There is some improvement in screening after storage pretreatment (group 1) and after power operating pretreatment (group 3). The greatest improvement in screening was after power operating pretreatment (group 3) on the 200° C storage life test.

Referring again to Table 21, it can be seen that using initial data to screen devices which were subjected to storage pretreatment (group 1) and then placed on 200°C storage life test was more effective in eliminating high stress failures than in using initial data of devices which were given no pretreatment (group 4). The screening on initial data of devices which were first given power operating pretreatment (group 3) was less effective than using no pretreatment (group 4) and more effective than using reverse bias pretreatment (group 2). This information is summarized in Table 22, and is based on the percentages given in Table 21.

Table 22. Order of Prediction of Failures on Life Test (Main Test Program)

Life Tests Temperature Storage	Order of Prediction on Pretreatment Data						
	Initial				Post-Pretreatment		
	Best	2nd Best	3rd Best	4th Best	Best	2nd Best	3rd Best
200°C	Group 1 (Temp. Stg.)	Group 4 (Control)	Group 3 (Pwr. Opr.)	- - -	Group 3	Group 1, 2	- - -
250°C	1,3	Group 2 (Rev. Bias)	4	- - -	1	3	2
300°C	3	2	1	4	3	2	1
Reverse Bias							
125°C	3	1	4	2	1	3	2
175°C	1	2,4	3	- - -			
225°C	1	2	3	4	1	3	2
Power Operating							
15 W	3,4	1	- - -	- - -	3	1	- - -
37.5 W	3	4	1	2	3	1,2	- - -
60 W	1	4	2	3	3	1	2
Temp. Stg. (Avg.)	3	1	2	4	3	1	2
Reverse Bias (Avg.)	1	2	3	4	1	3	2
Pwr. Operating (Avg.)	1	4	2	3	3	1	2

These tables, of course, over-simplify the comparison. Data obtained during testing show that some of the pretreatments, storage or power prior to the reverse bias test, for example, appear to be detrimental to the device used, since they produce more failures while operating pretreatment stabilizes the device on power operating tests.

The four pretreatment groups were studied to see if they would respond similarly to the accelerated testing conditions.[2/] Each pretreated group of 25 among the 100 unit sample subjected to a particular test condition was studied separately. The plots of cumulative percent failure versus log time appeared to be similar for the four groups except on reverse bias tests. They were not exactly the same since there can be some variation from sample to sample.

It was then decided to use the Kolmogorov-Smirnov two-sample test to see if any difference could be detected between the response of the three pretreated groups and the control. The Kolmogorov-Smirnov two-sample test is a test of whether two independent samples have been drawn from populations with the same distributions. It is an excellent test to apply since it is non-parametric and is sensitive to any kind of difference in the two distributions. At a particular read-out step, each parameter range was divided into a collection of 40 cells; there were four such collections, one for each of the pretreated groups. The number of devices having parameter values in each cell was noted and then the cumulative percent of the devices which had parameter values in a particular cell or in a previous cell was calculated for each cell. The maximum percent difference irrespective of sign between the cumulative distributions of the pretreated group and the control sample was calculated and examined for significance at the 0.05 level. This was done for all fixed stress tests at all readout intervals.

The results of the Kolmogorov-Smirnov two sample test are presented below. There was no significant difference in any of the parameter distributions in the 200° C or 300°C storage life tests nor on the 125°C or 175° C reverse bias life tests at the initial reading prior to being placed on high stress. This would indicate that the different pretreatments had not affected the device parameters differently. There was a difference in the h_{FE} (1A) distributions between group 1 (storage pretreatment) and group 4 (control) at the beginning of the 225°C reverse bias life test; this difference was observed throughout the test. After the first 2 hours of this test, there was also a significant difference in the parameter distributions of h_{FE} (5 mA) between groups 1 and 4. There was a significant difference in $V_{CE(sat)}$ between groups 1 and 4 during the 37.5 W power operating life test. After the first two hours, a significant difference developed between group 2 (reverse bias pretreatment) and group 4 on this test. A significant difference was observed also between group 3 (power operating pretreatment) and group 4 on the 250°C storage life test on I_{CEO} (70 V) and between groups 2 and 4 on the 15 W power operating life test on I_{CEO} (70 V).

Examination of Table 23 shows that reverse bias pretreated units failed more than the control on the operating life tests, while operating pretreatment had a stabilizing effect. Storage and operating pretreatment resulted in more units failing on reverse bias life tests than the control or reverse bias pretreatment.

By eliminating the devices which were predicted failures from pretreatment data, the percentage of failures in the sample after screening on the pretreatment data may be calculated. Table 24 gives these percentages. This table indicates that screening on operating pretreatment would be advantageous on storage and power operating life tests. No pretreatment appears advantageous for the reverse bias life test.

Table 23. Total Number of Failures on Fixed Matrix Tests by Pretreatment Group (Main Test Program)

Fixed Matrix Tests	Pretreatment Groups			
	Group 1 Temperature Storage	Group 2 Reverse Bias	Group 3 Power Operating	Group 4 Control
Temperature Storage Life	38	38	24	36
Reverse Bias Life	58	41	57	41
Power Operating Life	21	34	15	23

Table 24. Percent Failures on Fixed Matrix Tests After Removal of Predicted Failures from Pretreatment Data (Main Test Program)

Fixed Matrix Tests	Percent Failures in Screened Sample (Initial Data Used)				Percent Failure in Screened Sample (Post-pretreatment Test Data Used)		
	Pretreatment Groups				Pretreatment Groups*		
	Group 1 Temperature Storage	Group 2 Reverse Bias	Group 3 Power Operating	Group 4 Control	Group 1 Temperature Storage	Group 2 Reverse Bias	Group 3 Power Operating
Temperature Storage Life	36	38	28	41	34	37	25
Reverse Bias Life	64	44	63	46	57	44	57
Power Operating Life	9	38	14	15	17	35	5

*Group 4 — Not Applicable Control

A study of the parameters which were preindicators of failure during pretreatment for each of the pretreated groups on each of the high stress tests was made. To simplify analysis and comparisons of results the screening efficiency criterion, as mentioned previously in this subsection, was that no good units be eliminated. The analysis is incomplete and will not be given here in detail. However, there did not appear to be any preindicators of failure which were common to all of the pretreatment groups. For example, I_{CBO} (30 V) was a preindicator for group 1 (storage pretreatment) on the 125°C reverse bias life test, but the preindicators of failure for group 2 (reverse bias pretreatment) were delta and percent changes in $V_{BE(sat)}$, and for group 3 (operating pretreatment) were h_{FE} (5 mA), $V_{BE(sat)}$, and delta changes in I_{CBO} (30 V) and I_{CBO} (70 V). It would be interesting to compare the failure preindicators during pretreatment with the failure parameters during high stress for each of the pretreated groups. This information, however, would not be available without much more data analysis.

4. HIGH STRESS TESTING

Table F-4, screening results for the 250°C temperature storage life test (Main Test Program), will be used to assist in understanding the screening tables in Appendix F. Column 1 of Table F-4 is the screening step given as i-j, where i refers to the readout step during the high stress test (1 for initial) and j refers to the screening pass number (j = 1, 2, ..., 5). The computer program SERF examines all of the electrical parameters measured at a particular readout step as well as the delta and percent changes in that parameter. That parameter or change in parameter and parameter limits which maximizes the screening efficiency is selected as the screening parameter and screening level for the first screening pass for any readout step, i (screening pass i - 1). Devices with screening parameter values above or below the screening parameter levels (limits) are eliminated (screened) from the sample. The best screening parameter for the remaining devices is then selected for screening pass i - 2. This continues for a total of 5 screening passes. In other words, 5 parameters are selected for inclusion in the final screening procedure. The number of screening passes used to examine the data at each readout step is a value which the user supplies as input to the SERF computer program. In practice it has been found that 5 passes suffice.

At all of the readout steps during the fixed matrix tests of the Main Test Program except the initial and final readings, ten electrical parameters were measured. These are the first ten parameters listed in Table F-1. At the initial and final readout steps, an additional 5 parameters also listed in Table F-1 were measured. Column 2 of Table F-4 gives the screening parameter selected for each screening pass. For the screening on initial data (screening passes 1-1 to 1-5) for each test, the number in column 2 refers to the appropriate parameter described in Table F-1. Referring to Table F-4, it is seen that parameter 15 was selected as the first screening parameter. Referring to Table F-1, it is seen that this is BV_{EBO} (I_E = 100 μA).

However, on all screening passes after 1-5, a different numbering system is used for screening parameters. In the new system, parameters 1 to 10 refer to the first 10 parameters in Table F-1, parameters 11 to 20 are the delta changes of parameters 1 to 10, and parameters 21 to 30 are the percent changes of parameters 1 to 10 (Figure F-2). Thus, for example, referring to Table F-4, the screening parameter on screening pass 2-1 is parameter 11, delta change in parameter 1, I_{CEO} (V_{CE} = 30 V).

The 95 entry in column 3 of Table F-4 at screening step 1-1 means that at the beginning of the test there were 95 devices. In column 4 of Table F-4 it is seen that forty-eight of these devices failed after the initial step. Screening on parameter 15, BV_{EBO} (I_E = 100 μA), 5 devices were rejected (column 5 of Table F-4) and column 8 of Table F-4 indicates that there were no (0) good devices among those rejected. Thus there were 43 failures (column 6 of Table F-4) which were not rejected when screening on parameter 15. The 47 devices in the original sample of 95 which did not fail on stress are in column 7 of Table F-4.

The e and e* values are given for this first screening step. After rejecting the first 5 devices on screening step 1-1, there are 90 devices remaining to be screened. Screening at step 1-2 on parameter 7, h_{FE} (5 mA), removes 7 additional devices, 6 of which later failed.

After screening on the initial data (screening passes 1-1 to 1-5) the data for the next readout step are examined, screening passes 2-1 to 2-5. It should be noted again that the number of devices in column 3 is always the number of devices remaining on test whose parameter values did not exceed the failure criterion (Table 2 and Table 3) after the readout step on which data the current screening step is being done. Thus referring to Table F-4 screening pass 2-1, it is seen that there were 89 devices whose parameters had not exceeded the failure criteria. Screening at step 2, then, would remove the 6 devices (95-89) which were first detected as failures at the second readout step but there would be no prediction involved.

Thus screening at step 2-1 on parameter 10 ($V_{CE(sat)}$) would remove 9 additional devices, 2 of which were actually good. This results in 15 devices being eliminated, the 9 predicted failures and the 6 devices which were actual failures due to exceeding the failure criteria at that readout step.

Examination of the screening results in Appendix F reveals that on the temperature storage life tests I_{EBO} (V_{EB} = 8 V) (parameter 6, 16, 26) and h_{FE} (5 mA) (parameter 7) are the parameters most frequently included in the screening procedures (Tables F-3, 4, and 5). Here reference to a parameter also includes delta and percent changes in that parameter. On the power operating life tests (Tables F-6, 7 and 8) h_{FE} (1A) (parameter 8) occurs frequently. On the reverse bias life test (Tables F-9, 10 and 11) I_{EBO} (V_{EB} = 5 V) (parameter 5) and $V_{BE(sat)}$ (parameter 9) occur most frequently. It should be noted in selecting the screening parameter that when

more than one parameter gives the same screening efficiency, the computer program SERF simply selects the first of these parameters on the list. Thus I_{CEO} (30 V) (parameter 1) occurs frequently in the screening procedures and can simply indicate that all parameters give poor screening and that parameter 1 was actually used in screening since it occurred first on the list.

Analyzing the parameters which were selected on the first screening pass, those which give the highest screening efficiency, it is noted that I_{EBO} (5 V), I_{EBO} (8 V), and h_{FE} (5 mA) (parameters 5, 6 and 7, respectively) occur most frequently on the temperature storage tests as seen in Tables F-3, 4 and 5. Referring to Table D-2 it can be seen that the primary failing parameters on the temperature storage test are h_{FE} (5 mA), but that relatively few devices failed due to I_{EBO} limits being exceeded. The most frequently occurring screening parameters on the power operating tests (Tables F-6, 7 and 8) are I_{EBO} (8 V) and h_{FE} (1 A) (parameter 6 and 8). On these tests h_{FE} (1 A) is practically never a failing parameter and I_{EBO} (8 V) occurs fairly frequently as seen in Table D-6. On the reverse bias test I_{CEO} (30 V), I_{CEO} (70 V), I_{CBO} (70 V), I_{EBO} (5 V), and $V_{BE(sat)}$ (parameters 1, 2, 4, 5 and 9, respectively) appear most frequently as the screening parameters. They also are frequently failing parameters as seen in Table D-4.

Predicting later failure from the initial readings immediately prior to high stress will assist in the development of a screening procedure. The data in Appendix F indicate that the parameters selected for screening will be functions of the particular stress to which the device will be exposed. Pretreatment data indicate that it is a function of pretreatment also. To some extent all of this would be expected, since there are evidently a number of failure mechanisms operative and the equilibrium may easily be shifted by stress change.

There are a number of reasons why screening during high stress tests could be of importance. Predicting later failure initially and during high stressing can supply information of value to a physics of failure study. For example, the I_{EBO} (8 V) parameter with values $\leq 0.240\ \mu A$ predicted 56 failures on the 300°C storage life test (Table F-5) although this was a failing parameter for only 19 devices (Table D-2). Also it was found that 30 of the 31 units with the highest initial $V_{CE(sat)}$ values ($V_{CE(sat)} = 0.104$ to 0.132 V) later failed on this test, as shown in Figure 64. Also screening during high stress testing could lead to the discovery of an excellent way to eliminate later failures after only a short time under high stress. This was not observed during this test program, but it is a possibility for justifying the consideration of early screening during a high stress test. For example, it could be found that screening after hours under a very high overstress resulted in excellent prediction of later failure but that this overstress for even two hours damaged the device. Consideration could then be given to screening at (say) 15 minutes from the start of the test which would minimize any damage to the device that might result from the stress. Relatively soon after the beginning of the high stress test the parameter change preindicating failure may already be evident.

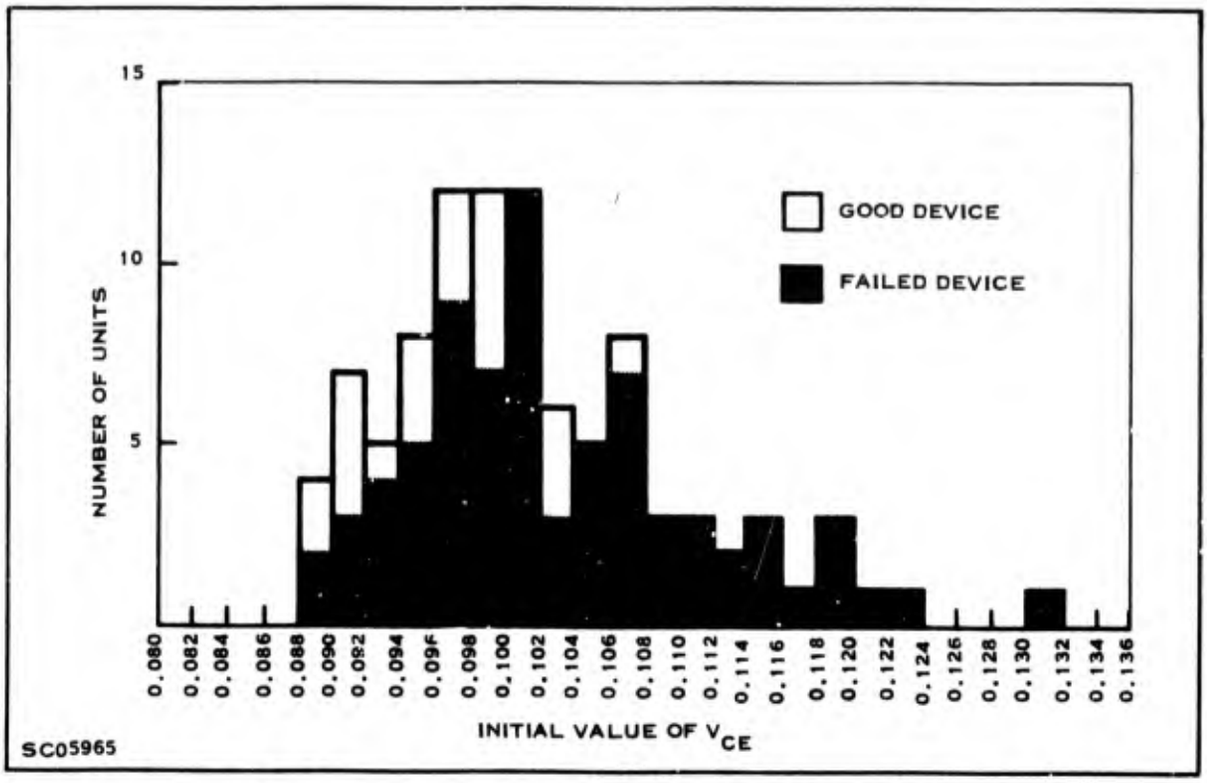

Figure 64 . Distribution of Initial V_{CE} Values, 300°C Temperature Storage Test (Main Test Program)

Application of these techniques for predicting failures from initial data and from high-stress data could prove useful in designing burn-in tests. That is, the burn-in test could be selected on the basis of its ability to eliminate (screen) the largest percentage of potential failures from a given lot. In fact it may be advantageous to change the burn-in test periodically for a given device series since the more prevalent failure mode may change due to process change.

5. CRITIQUE OF SCREENING RESULTS

There is some evidence that screening during power operating pretreatment will result in a smaller percentage of devices failing on the storage and power operating life tests. No pretreatment seems to enhance prediction prior to reverse bias life testing. The proper screening procedure will be a function of the pretreatment stress and the type of stress (life test) to which the devices will be exposed.

It should be emphasized that these results are based on a small sample and only a few manufacturing lots were represented in the tests. It also should be noted that prediction in this test program is done "after the fact," i.e., after a device is considered a failure the data is re-examined to see if there was a preindication of failure. Much further testing would be necessary to make these results definitive.

6. LINEAR DISCRIMINANT ANALYSIS

a. Introduction and Summary

The computer program SERF is of value in isolating those parameters which are preindicators of failure. It can be of value in constructing a screening procedure and in providing information of value to a physics of failure study. However, a major disadvantage of this program is that it cannot screen simultaneously on more than one parameter. Suppose, for example, that units with a high value of one parameter or a low value of some other parameter are not particularly liable to fail. It is quite possible that later failure would be associated with both a high value of one parameter and the low value of another parameter. A linear discriminant analysis computer program (LINDA 1), however, allows us to screen on many parameters at once.

There are three major disadvantages of linear discriminant analysis, however. First, deciding on the proper parameters to incorporate in the linear discriminant function is not a simple problem. An arbitrary collection of parameters could be selected, but discrimination would not necessarily be good. W. G. Cochran[7] has derived a relatively simple method for deciding which parameters should be included in the linear discriminant function. Second, the assumption is usually made that the covariance matrices of the two populations, in the case of transistors, into good and bad, are equal. This is not necessarily true, but merely a convenient assumption. Recently, T. W. Anderson and R. R. Bahadur[6] have solved the classification problem when there are unequal covariance matrices. A computer program, LINDA 2, has been written to handle the unequal covariance matrix case. A description of the program will be found in Appendix G. Third, the assumption is made that the distributions are multivariate normal. In the case of transistor parameter distributions this does not necessarily appear to be the case. Preliminary attempts have been made to investigate the possibility that there may be satisfactory discrimination even when the distributions are non-normal.

If the distributions of the parameters of the satisfactory and unsatisfactory devices are normal then the computer programs given in Appendix G can be used to develop a classification procedure using linear discriminant analysis. A few studies investigating the applicability of linear discriminant analysis when the distributions are not normal were made during this contract and are reported in this section.

Two non-normal distributions, a bivariate (two parameter) uniform distribution and a bivariate "contaminated" normal distribution, were generated by computer simulation. The probabilities of misclassification were calculated for these distributions and compared with the probabilities of misclassification for the normal distributions. It was found that the probabilities of misclassification in the contaminated case were comparable to those in the normal case. The uniform distribution study was not of practical interest.

These results are based on a few initial studies. Much further simulation of various non-normal distributions and evaluation of the probabilities of misclassification would be required before the extent of the applicability of linear discriminant analysis to non-normal data could be understood. This could allow much more use of the powerful linear discriminant analysis in analyzing transistor parameter data. A more technical discussion of this simulation study is given in subsections 6b and 6c of this section. Subsection 6d lists further possibilities of investigation and the important points are given below in more qualitative form:

1) Investigate other non-normal distributions.

2) Vary the correlation between parameters.

3) Investigate non-parametric classification procedures. The classification procedure of linear discriminant analysis is based on the underlying distributions being normal. The studies mentioned in this report investigate the effect of non-normality on the classification procedures. Non-parametric procedures, however, are those which are independent of the underlying distributions even in theory.

4) Investigate which parameters should be included in the linear discriminant function. Many electrical parameters may be measured and it would be impractical to include all of them in the linear discriminant function. Knowing something about the statistical relations between the parameters in theory assists in the selection of those parameters to be included in the linear discriminant function.

b. Investigation of Non-normality Assumptions

1. Explanation

A well-defined classification procedure is given in Appendix G. But suppose the underlying populations π_1 and π_2 are not normally distributed. A complete study of this situation is virtually impossible, but some insights can be gained by studying special cases by means of simulation methods. The distribution of U, the linear discriminant function, was investigated under the following assumptions:

π_1, π_2 have bivariate uniform distributions.

π_1, π_2 have contaminated bivariate normal distributions.

Probabilities of misclassification were approximately computed under these assumptions and compared to probabilities of misclassification under normal assumptions. For purposes of investigation, underlying population means and covariances were assumed to be known. The thirteen cases studied are shown in Table 25. In each case the correlation ρ was taken to be 0.1.

2. Construction of Empirical Distributions

This section outlines the technique used for constructing the empirical distribution functions from which approximate probabilities of misclassification were computed (Table 25).

Uniform Case. Suppose we want an item from a bivariate uniform distribution with mean $(a,b)'$. The covariance matrix is

$$\begin{pmatrix} 1/12 & 0 \\ 0 & 1/12 \end{pmatrix}$$

We generate two independent items from the univariate uniform distribution on 0,1, say x_1 and x_2. Then $(x_1 + a - 1/2,\ x_2 + b - 1/2)'$ constitutes an item from a bivariate uniform distribution with mean $(a, b)'$.

Contaminated Case. Generate a random item from the uniform distribution on $[0,1]$, say q. If $q > 0.1$, generate an item from the underlying population π. If $q \leq 0.1$, generate an item from a population with the same mean and correlation as π, but with variances nine times larger.

To obtain an item from[8/]

$$N\left[\begin{pmatrix} 0 \\ 0 \end{pmatrix}, \begin{pmatrix} 1 & 0.1 \\ 0.1 & 1 \end{pmatrix}\right]$$

let x_1 and z_2 be independent items from n(0.1). Let $x_2 = 0.1x_1 + 0.99z_2$. Then $(x_1, x_2)'$ is an item from

$$N\left[\begin{pmatrix} 0 \\ 0 \end{pmatrix}, \begin{pmatrix} 1 & 0.1 \\ 0.1 & 0.9901 \end{pmatrix}\right] \approx N\left[\begin{pmatrix} 0 \\ 0 \end{pmatrix}, \begin{pmatrix} 1 & 0.1 \\ 0.1 & 1 \end{pmatrix}\right]$$

which follows from the fact that every linear combination of x_1 and x_2 is normally distributed and Theorem 2.6.2 in[9/]. Here the correlation $\rho = 0.1/\sqrt{0.9901} = 0.1005 \approx 0.1$.

To obtain an item from a bivariate population with mean $(a, b)'$, variances σ_1^2 and σ_2^2, and correlation 0.1, transform $(x_1\ x_2)'_1$ as follows. Let $w_1 = \sigma_1 x_1 + a$ and $w_2 = \sigma_2 x_2 + b$. Then $E\left[(w_1, w_2)'\right] = (a, b)'$, $\sigma w_1^2 = \sigma_1^2$, $\sigma w_2^2 = \sigma_2^2$, and the correlation is 0.1, by problem 31, p. 43.[9]

Table 25. Thirteen Cases Studied Empirically

Case	$\underset{\sim}{\mu}^{(1)}$	$\underset{\sim}{\mu}^{(2)}$	$\underset{\sim}{\Sigma}$
1	$\begin{pmatrix}0\\0\end{pmatrix}$	$\begin{pmatrix}2\\2\end{pmatrix}$	$\begin{pmatrix}1 & 0.5\\0.5 & 25\end{pmatrix}$
2	$\begin{pmatrix}0\\0\end{pmatrix}$	$\begin{pmatrix}2\\2\end{pmatrix}$	$\begin{pmatrix}25 & 2.5\\2.5 & 25\end{pmatrix}$
3	$\begin{pmatrix}0\\0\end{pmatrix}$	$\begin{pmatrix}2\\10\end{pmatrix}$	$\begin{pmatrix}25 & 2.5\\2.5 & 25\end{pmatrix}$
4	$\begin{pmatrix}0\\0\end{pmatrix}$	$\begin{pmatrix}10\\10\end{pmatrix}$	$\begin{pmatrix}25 & 2.5\\2.5 & 25\end{pmatrix}$
5	$\begin{pmatrix}0\\0\end{pmatrix}$	$\begin{pmatrix}2\\2\end{pmatrix}$	$\begin{pmatrix}1 & 1\\1 & 100\end{pmatrix}$
6	$\begin{pmatrix}0\\0\end{pmatrix}$	$\begin{pmatrix}2\\2\end{pmatrix}$	$\begin{pmatrix}100 & 10\\10 & 100\end{pmatrix}$
7	$\begin{pmatrix}0\\0\end{pmatrix}$	$\begin{pmatrix}2\\10\end{pmatrix}$	$\begin{pmatrix}100 & 10\\10 & 100\end{pmatrix}$
8	$\begin{pmatrix}0\\0\end{pmatrix}$	$\begin{pmatrix}10\\10\end{pmatrix}$	$\begin{pmatrix}100 & 10\\10 & 100\end{pmatrix}$
9	$\begin{pmatrix}0\\0\end{pmatrix}$	$\begin{pmatrix}1\\5\end{pmatrix}$	$\begin{pmatrix}25 & 2.5\\2.5 & 1\end{pmatrix}$
10	$\begin{pmatrix}0\\0\end{pmatrix}$	$\begin{pmatrix}1\\5\end{pmatrix}$	$\begin{pmatrix}1 & 0.5\\0.5 & 25\end{pmatrix}$
11	$\begin{pmatrix}0\\0\end{pmatrix}$	$\begin{pmatrix}5\\5\end{pmatrix}$	$\begin{pmatrix}25 & 2.5\\2.5 & 25\end{pmatrix}$
12	$\begin{pmatrix}0\\0\end{pmatrix}$	$\begin{pmatrix}1\\5\end{pmatrix}$	$\begin{pmatrix}25 & 2.5\\2.5 & 25\end{pmatrix}$
13	$\begin{pmatrix}0\\0\end{pmatrix}$	$\begin{pmatrix}1\\1\end{pmatrix}$	$\begin{pmatrix}25 & 2.5\\2.5 & 25\end{pmatrix}$

After 500 items are generated from a given distribution, arrange them in ascending order, $u_1 < u_2 < \ldots < u_{500}$, and compute the empirical distribution function of U, $F_{500}(u_i) = i/500$. From the empirical distribution function compute approximate probabilities of misclassification.

The algebraic form of U in the bivariate case is obtained below.

Let

$$\underset{\sim}{X} = \begin{pmatrix} x_1 \\ x_2 \end{pmatrix}, \quad \underset{\sim}{\Sigma} = \begin{pmatrix} \sigma_{11} & \sigma_{12} \\ \sigma_{12} & \sigma_{22} \end{pmatrix}, \quad \underset{\sim}{\mu}^{(1)} = \begin{pmatrix} \mu_{11} \\ \mu_{12} \end{pmatrix}, \quad \text{and}$$

$$\mu^{(2)} = \begin{pmatrix} \mu_{21} \\ \mu_{22} \end{pmatrix}. \quad \text{Then } \underset{\sim}{\Sigma}^{-1} = \frac{1}{\sigma_{11}\sigma_{22} - \sigma_{12}^2} \begin{pmatrix} \sigma_{22} & -\sigma_{12} \\ -\sigma_{12} & \sigma_{11} \end{pmatrix}, \quad \text{and}$$

$$U = \frac{1}{\sigma_{11}\sigma_{22} - \sigma_{12}^2} \left\{ (x_1 \sigma_{22} - x_2 \sigma_{12}) d_1 + (x_2 \sigma_{11} - x_1 \sigma_{12}) d_2 - \right.$$

$$\left. \frac{1}{2}(S_1 \sigma_{22} - S_1 \sigma_{12}) d_1 - \frac{1}{2}(S_2 \sigma_{11} - S_1 \sigma_{12}) d_2 \right\},$$

where

$$d_1 = \mu_{11} - \mu_{21}$$

$$d_2 = \mu_{12} - \mu_{22}$$

$$S_1 = \mu_{11} + \mu_{21}$$

$$S_2 = \mu_{12} + \mu_{22}$$

3. Results

One result of this study is a computer program designed to perform linear discriminant analysis which includes routines for finding the Bayes and minimax solutions for c (defined on page G-14 of Appendix G). Here c is a measure of the relative costs of misclassification, i.e., the relative costs of classifying a good device as bad or vice versa. It is shown on page G-14 of Appendix G that if q_1, the probability that a device is from the population of good devices and q_2, the probability that a device is from the population of bad devices, are known,

then,

$$c = \log \left[q_2 \; c\,(1/2) / q_1 \; c\,(2/1) \right],$$

where c (1/2) is the cost of misclassifying a bad device as good and c (2/1) is the cost of misclassifying a good device as bad. The meaning of c when q_1 and q_2 are not known is also discussed on page G-15 of Appendix G.

Table F-12 in Appendix F displays the results of the simulation process. Column (0) gives the case number, column (1) the means and common covariance matrix of π_1 and π_2, column (2) the theoretical value of the variance of U on the assumption of underlying normal populations, column (3) the theoretical mean of U, and columns (4) and (5) give the empirical mean and variance of U on the assumptions of uniformity and contamination, respectively. One check simulation was done using underlying normal populations. The result is displayed in Table F-13.

Now turn to the comparison of probabilities of misclassification in normal and non-normal situations. Four values of c were studied, i.e., c = 0, c = 1, c = 2, c = 4. Tables F-14, F-15, F-16, and F-17 summarize the results. Column (0) gives the case number, and columns (1), (2), (3) give probabilities of misclassification on the assumptions of underlying normality, uniformity, and contamination, respectively. P(2/1) is the probability of classifying an item into π_2 when it is really from π_1, and P(1/2) is the probability of classifying an item into π_1 when it is really from π_2.

c. Critique of Linear Discriminant Analysis Studies

For fixed mean differences and correlation, probabilities of misclassification generally tend to increase as variances in the underlying populations increase (e.g., compare cases 1 and 5, 2 and 6, 3 and 7, and 4 and 8 in Tables F-14, F-15, F-16 and F-17). Of course, the larger variances mean that the populations are "mixed up," and classification of items is more difficult than in cases where the populations are quite distinct.

Probabilities of misclassification based on the contaminated populations tend to be reasonably close to those based on normal populations. More experimentation must be done, but the preliminary evidence is that classification based on the linear discriminant function may be satisfactory at least when the underlying populations are more "heavy-tailed" than normal populations.

The uniform case produces odd results because of the small underlying variances. This case seems to be not of much practical interest, however.

Apart from consideration of probabilities of misclassification one can justify use of the linear discriminant function on intuitive grounds. As noted on p. 136[9], $\underset{\sim}{X}' \underset{\sim}{\Sigma}^{-1}[\underset{\sim}{\mu}^{(1)} - \underset{\sim}{\mu}^{(2)}]$ is the linear function that maximizes the quantity

$$\frac{\left[E_1 (\underset{\sim}{X}'\underset{\sim}{d}) - E_2 (\underset{\sim}{X}'\underset{\sim}{d})\right]^2}{\text{Var } (\underset{\sim}{X}'\underset{\sim}{d})}$$

with respect to d. Thus the linear discriminant function, which is a function of $\underset{\sim}{X}' \underset{\sim}{\Sigma}^{-1}[\underset{\sim}{\mu}^{(1)} - \underset{\sim}{\mu}^{(2)}]$ should provide maximum power of discrimination. Note that this result is independent of the form of the distributions of the underlying populations π_1 and π_2. Similar remarks hold for the case where population parameters must be estimated, for, as noted on p. 153[9], $\underset{\sim}{d} = \underset{\sim}{S}^{-1} [\underset{\sim}{\bar{X}}(1) - \underset{\sim}{\bar{X}}(2)]$ is the linear function which maximizes the quantity

$$\frac{\left[\underset{\sim}{d}' \underset{\sim}{\bar{x}}^{(1)} - \underset{\sim}{d}' \underset{\sim}{\bar{x}}^{(2)}\right]^2}{\sum_{i=1}^{N_1} \left(\underset{\sim}{d}' \underset{\sim}{x}_i^{(1)} - \underset{\sim}{d}' \underset{\sim}{\bar{x}}^{(1)}\right)^2 \sum_{i=1}^{N_2} \left(\underset{\sim}{d}' \underset{\sim}{x}_i^{(2)} - \underset{\sim}{d}' \underset{\sim}{\bar{x}}^{(2)}\right)^2}$$

with respect to $\underset{\sim}{d}$.

Thus, if one is willing to accept linear discrimination as a working procedure, he may turn his attention to other problems, e.g., the inequality of the covariance matrices of π_1 and π_2 (point 5 below).

d. **Further Possibilities of Investigation**

The first four (4) possibilities of investigation are given in more qualitative form at the end of Section VII-6a.

1. Check the behavior of U against non-normality assumptions other than those of uniformity and contamination, e.g., bivariate gamma or even bivariate Poisson.

2. Vary the correlation ρ.

3. Explore the possibilities of non-parametric classification procedures. (Compare references 16 and 17.)

4. Investigate the problem of selecting the best discriminatory variates. Giri [10] discusses the maximum likelihood test for testing whether the last p-q variates of a p-dimensional vector of normal variates contribute significantly to discrimination. The test assumes that the (distinct) underlying means and the (common) covariance matrix are unknown. Cochran [7] discusses some principles underlying the selection of discriminatory variates and suggests a simple test to determine whether one or more variates will contribute to discrimination. (See also references 11 and 12.)

5. Examine the assumption that π_1 and π_2 share a common covariance matrix. Anderson [9], pp. 247-250, 256-259, contains a test of this assumption. Anderson [6] gives optimal "linear" classification procedures when the underlying covariance matrices are not equal. Linear procedures are those which require the sample space to be divided into two regions of classification by means of a hyperplane. Cooper [13] discusses some non-linear procedures which are optimal for not only underlying multivariate normal populations, but also underlying multivariate Pearson Type II and Type VII populations. Geisser [14] discusses classification quite generally from a Bayesian point of view. A feature of the Bayesian approach is that posterior probabilities that x comes from π_1 and π_2 are obtainable.

Welch and Wimpress [15] outline a computer program of the minimax procedure derived in reference 6. Welch and Wimpress, p. 429, point out that this procedure produces the vector $\underset{\sim}{b}^*$ which maximizes

$$\frac{|\underset{\sim}{b}' \underset{\sim}{\mu}^{(2)} - \underset{\sim}{b}' \underset{\sim}{\mu}^{(1)}|}{(\underset{\sim}{b}' \underset{\sim}{\Sigma}_1 \underset{\sim}{b})^{1/2} + (\underset{\sim}{b}' \underset{\sim}{\Sigma}_2 \underset{\sim}{b})^{1/2}} .$$

This result is independent of assumptions made about the distributions of π_1 and π_2 and hence offers intuitive justification for the procedure presented. In view of the evidence collected so far, it appears that the procedures discussed by Anderson [6] have much to recommend them.

7. DEVELOPMENT OF SCREENING PROCEDURE

a. Introduction

A nondestructive screening procedure was developed under this contract using the modified SERF computer program for small stud silicon planar epitaxial NPN power transistors having an all aluminum metallization contact system and other materials of construction, compatible with the temperatures employed in the screen. This procedure is outlined in Table 1.

Prior to initiating the screen, a random sample is selected from a given lot of devices to be screened. The procedure consists of two phases for each lot.

Phase 1 (screen selection) is designed principally to select the best screening procedure for the lot. The random sample is subjected sequentially to a constant acceleration screen, hermetic seal check, thermal resistance screen, and power burn-in; followed by three separate 1000 hour high stress life tests (Table 1). Electrical parameter measurements are made several times and attribute data recorded on IBM cards for input to the computer program. From these data the best parameters to use for screening are determined by the SERF program.

Phase 2 (screen application) is designed for 100% processing the remainder of the lot. This procedure is also in Table 1. The lot is sequentially processed through the same stresses used in phase 1, up to and including power burn-in.

The lot is then routinely screened by the computer using the results obtained in phase 1. Screen selection, screen application and cost of each of these two phases of the screening procedure are discussed in more detail below.

b. Screen Selection (Phase 1)

A discussion of each step of the screening procedure is presented in order of occurrence for phase 1 (Table 1). A quantity of devices is chosen for the lot and a random sample of 400 is recommended for processing through phase 1. This size sample allows for yield loss at the various steps in phase 1, still leaving 100 units for each of the three life tests. A 100 unit sample is considered a minimum size sample for each of the life tests on which the prediction technique is based. The 400 unit sample will be serialized in some convenient way for traceability. Unit identity is maintained.

Step 1 - Read Electrical Parameters

The screening results obtained from SERF (discussed in Section VII-4) indicate that all fifteen parameters used in the test program on this contract (Tables 2 and 3) are useful in predicting failures on high stress tests. Attribute data are taken and recorded on IBM cards for later use. Correlation samples (Section III-2c) are also used before and after reading the electrical parameters of the sample. The 400 unit sample is then subjected to step 2.

Step 2 - Constant Acceleration

This test is included in the screen to remove mechanically weaker units which are not typical of the entire sample. Data obtained in the Preliminary Test Program showed that constant acceleration is more effective than thermal shock or impact shock for removing mechanically weaker units (Section II-2a). The data used in selecting the stress of 10,000 G for the X_1 and Y_1 planes are discussed in Section IV-b. In the Verification Test Program the constant acceleration test successfully removed units with weak post-to-wire welds (Section V-7a). The conditions for performing step 2 for the screen were based on actual results in this program. It is recognized that stressing a device from a particular manufacturer in both planes may not be necessary. In general, one plane should be sufficient if the nature of the mechanical rogues is known. The Y_1 plane is recognized by the industry and the military as the most likely orientation for the stress. If one plane must be chosen the Y_1 plane appears to be the best choice.

Step 3 - Hermetic Seal

Hermetic seal testing is included to assure package integrity. In the present program the hermetic seal was not checked except on failed devices and in several cases defective hermetic seals were found to be a cause of failure. Inclusion of the hermetic seal check should catch any escapes. The devices will be given a fine-leak test on helium or krypton leak test equipment and devices which exceed a leak rate of 5×10^{-8} cc/sec using helium or 5×10^{-9} cc/sec using krypton will be rejected. The selection of the leak rates is based upon data depicted in Figure 64a which demonstrate that a difference of approximately one order of magnitude exists between the results of helium techniques and krypton techniques in the 10^{-8} cc/sec region for the small stud package (TO-111). Following the fine-leak test the entire sample will be gross-leak tested by immersion in noncorrosive ethylene glycol at 150°C for a minimum of 15 seconds. The remainder of the sample is then subjected to step 4.

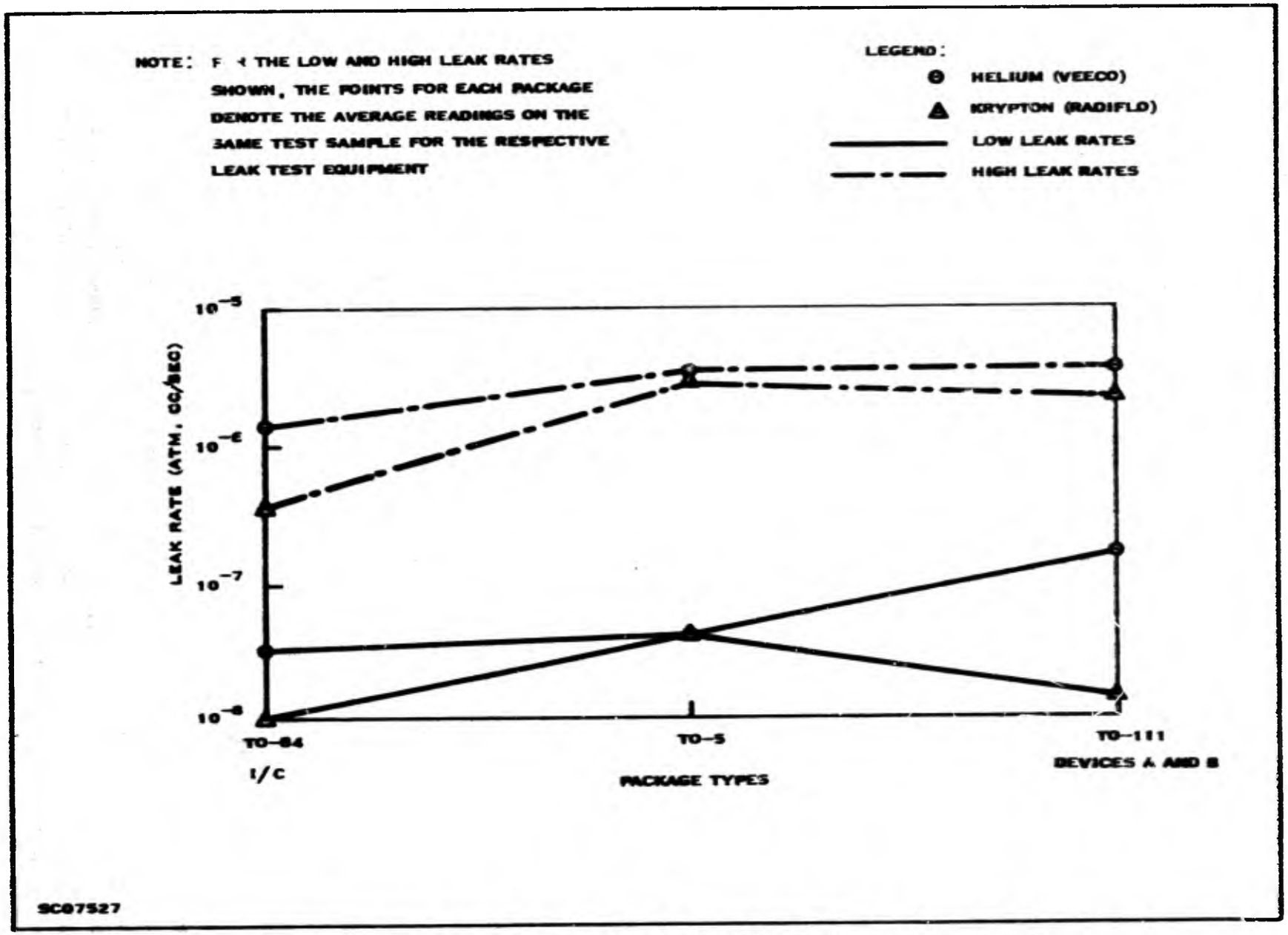

Figure 64a. Variation in Leak Rate Results Using Helium and Krypton Fine- . Leak Test Equipment

Step 4 - Thermal Resistance

The thermal resistance measurement is included because of the extreme dependency of T_J on V_{CE} as shown by the thermal studies in Figures 27 and 28. It was further shown that a pulse technique for measuring thermal resistance more nearly approximated the actual surface temperature as determined by an IR scan than did steady state techniques (Section VIII). The method selected was the ΔV_{CBF} (ZOT) method (Appendix B) because it was rapid, and gave good agreement with the IR scan results (Section VIII). The conditions of V_{CE} = 20 V and 30 W were chosen because the data (Section IV-5) indicated that the high V_{CE} at the power rating of the device was more effective than lower V_{CE} in removing poor devices. The data sheet value of 3°C/W was selected as reject criterion and devices which exceed the value are removed from the lot. The devices are then subjected to step 5.

Step 5 - Read Electrical Parameters

Same as for step 1 except devices are moved to step 6 after readings are made.

Step 6 - Power Burn-In

The power burn-in selection is based on the results of the pretreatment tests in the Main Test Program which are discussed in Section VII. The conditions for power burn-in are selected so that the device will be stressed at its power rating of 30 W at T_C = 100°C and V_{CE} = 20 V. This value of V_{CE} is chosen based on the power operating life tests results in the Verification Test Program (Section V) which were conducted at V_{CE} = 20 V. A burn-in facility comparable to that discussed in Appendix A is recommended. Next the devices are subjected to step 7.

Step 7 - Read Electrical Parameter

Same procedure as for step 1 except devices are moved to step 8 after readings are taken.

Step 8 - Life Tests

The remainder of the 400 unit sample (only catastrophic failures having been removed) is then divided into three smaller samples of 100 units each (the remainder of the lot are spares). It is important that unit identity be maintained. Each of the 100 unit lots is then placed on separate 1000 hour life tests (temperature storage, reverse bias, power operating). Three life tests are chosen because the test results obtained on this program showed that different failure modes often occur on the different tests. Additional data will be necessary for a particular manufacturer before any of the three life tests can be omitted from phase 1.

Step 8a

This test is included to accelerate failures such as those due to chemical reactions,to collector bond degradation and hermeticity. The conditions for stress are T_C = 350°C for 1000 hours. Units are to be placed in the ovens in three positions — horizontal, vertical and inverted — to take into account any effect gravity has on the mounting medium beneath the die. This is a safeguard measure and was incorporated in all three test programs in this contract. This method of storage was beneficial on the Main Test Program as poor can welds were revealed (this is discussed in Section IV-8). The stress condition is that used in the Verification Program. This was selected as it accelerates the failures without apparently introducing failures not related to use conditions. At this high temperature, the effects of pin holes in the collector nickel plate are accelerated which resulted in a break in the 350°C cumulative percent failure curve given in Figure 44. The same fifteen electrical parameters will be read at 2, 24, 250, 500 and 1000 hours in the manner described in the procedure of step 1.

Step 8b

This test is designed to accelerate failures due to collector bond flaws, crystal imperfections and abnormal thermal behavior due to problems of second breakdown and/or voids. Units will be stressed at T_C = 100°C and V_{CE} = 20 V at P_C = 50 W for 1000 hours. The same fifteen electrical parameters will be read at 2, 24, 250, 500 and 1000 hours in the manner described in the procedure of step 1. The test conditions chosen are those used in the Verification Test Program. The junction temperature (T_J) of the device will be ≥ 200°C for units with $\theta_{J-C} \geq 2$°C/W; however, results from the Verification Test Program indicate that this high stress test is effective in revealing device weaknesses.

Step 8c - Reverse Bias

This test is designed to show the incidence of temperature voltage induced inversion (TVI) and other modes dependent on electric fields. Units are stressed at $T_C = T_A$ = 200°C at V_{CB} = 100 V and V_{EB} = 7 V for 1000 hours. The same fifteen electrical parameters will be read at 2, 24, 250, 500 and 1000 hours in the manner described in the procedure of step 1. The bias conditions selected are the same as those used in the Main Test Program. The stress temperature of T_A = 200°C is chosen based on failure analysis results (Section IV-8c) and second (thermal) breakdown studies which showed that breakdown voltage of each junction decreases rapidly at temperatures above 200°C. Units are cooled to room temperature with bias applied and bias is not removed until immediately prior to parameter measurements. In the Main Test Program, the devices were cooled to room temperature with bias applied but some of the difficulty in interpreting the test results (Section VI-4) may be alleviated by retaining the bias on the units until immediately prior to parameter measurements.

Step 9 - Computer Analysis

The computer is used to compute delta (Δ) and percent (%) change of the parameter between steps 1 and 5. This is retained and will be used to compare different lots receiving the same processing. The SERF program is employed first to screen out potential failures using data from devices after the 100% burn-in (step 7) in conjunction with the data at step 5. However, this analysis is not performed until after the three life tests are completed. The SERF program is also used to screen out potential failures using data from the first four intervals of the life tests in conjunction with the initial data (step 7) prior to life tests. From such an analysis, a screening procedure is obtained for use in phase 2 (screen application). This completes phase 1. Then phase 2 is performed.

c. Application of Screen (Phase 2)

In this phase of the screening procedure the remainder of the lot is processed through steps 1 - 7 in the same manner as was done in phase 1. After completion of step 7 (burn-in) the lot is screened using the screening criteria obtained from SERF in phase 1.

d. General Considerations

Technique of dividing the lot and processing the sample prior to processing the lot is not mandatory. Rather the entire lot can be processed through step 7 and the random sample pulled for the life tests (still 100 units minimum per test).

Several options are available after completion of phase 1 depending on the computer (SERF) screening results of phase 1. For example, the SERF results may indicate that the units cannot be screened properly using post burn-in data. Rather, the SERF results may indicate that additional stress for a few hours on one or more tests similar to the life tests is necessary. As experience is gained with the SERF method by the various manufacturers, they will find techniques which will allow them to optimize their results for a given device type. One thing that the manufacturer might do to optimize the screening result is to change the e * criterion (Section VII) to allow more good units to be removed which may permit removal of a larger percentage of the bad units. Once the new e * criterion is determined it can be incorporated easily in the SERF program.

The techniques employed in the screening procedure should be applicable to most semiconductors but an exploratory investigation will probably be necessary on each device type before determining the adaptability of the technique.

e. Cost of Screening

The estimated costs of performing phase 1 and phase 2 of the proposed screening procedure in Table 1 are $14.00 to $28.70 and $5.40 to $11.80 per device respectively. The lower value of cost in either range is based on recording attributes data on 8 parameters and on two levels of screening using SERF, but omitting IBM card processing, failure verification, changes in SERF programming, and changes in failure criteria. The higher value of cost is based on recording attributes data on 15 parameters, five levels of screening using SERF and the other elements composing the cost factors W, X, Y, Z listed below.

These estimated costs for performing the proposed screening procedure on 100 devices may be expressed as,

$$C_1 = W + A_1 X + B_1 Y + C_1 Z \qquad \text{(Phase 1)}$$

and

$$C_2 = \frac{W}{2} + A_2 X + B_2 Y \qquad \text{(Phase 2)}$$

where

W, X, Y, Z = Costs which are defined in Table 26

A_1, A_2 = The number of steps where X costs apply in the respective phase of the screening procedure

B_1, B_2 = The number of steps where Y costs apply in the respective phase of the screening procedure

C_1 = Number of life tests

Each cost factor is composed of several elements, most of which are listed below.

Cost Factor X

- Record attributes data on 8 to 15 parameters
- Equipment set up
- Use of correlation sample
- Maintain $\overline{X}$ - R chart on correlation sample

Table 26. Factors Used in Estimating Costs of Performing The Proposed Screening Procedure

Screening Steps in Cost Grouping	Cost Factor ($)	Costs Per 100 Starting Devices	
		Lower ($)	Upper ($)
Steps 1, 5, 7	X	100	190
Steps 2, 3, 4, 6	Y	10	90
Steps 8a, 8b, 8c	Z	220	480
Step 9	W	400	500
Total Cost Per Device — Phase 1		14.00	28.70
Total Cost Per Device — Phase 2		5.40	11.80

- Maintain unit identity
- IBM card processing and data listing
- Labor costs for performing the tests

Cost Factor Y

- Go-No-Go testing on fine leak equipment
- Setup of equipment to perform required test
- Labor costs for performing the tests
- Labor costs for loading and unloading units on the various tests
- Maintain unit identity

Cost Factor Z

- Fixed costs for a particular life test - differs for each life test
- Y costs for 4 other loadings and unloadings (after initial)
- X costs for 5 intervals of readings with attributes data on 10 to 15 parameters
- Maintain unit identity

Cost Factor W

- Computer analysis of data using SERF including delta (Δ) and percent (%) change for 8 to 15 parameters
- Two to five levels of screening using SERF including delta (Δ) and percent (%) change for 8 to 15 parameters
- Data plotting
- Failure verification
- Changes in SERF programming
- Professional labor for data analysis and interpretation
- Up dating failure criteria

Although the equations for estimating the costs for the proposed screening procedure are of a general nature, they are not all inclusive. It is believed that any costs derived from them will be applicable in a relative fashion to any additions or subtraction of similar steps to the screening procedure. A list of some of the items not included in the estimated costs is given.

Not Included In Estimated Cost Factors

- Cost of sockets
- Design cost of test facility
- Cost of life test facility
- Failure analysis
- Yield
- Report

In determining these costs it was assumed that many lots of 1000 units or more would be subjected to the screening procedure. This allows amortizing some small fixed costs in cost factor Z. Thus cost factor Z as quoted above should not be used, as they would be too low, for calculating the cost of processing only one or two lots.

SECTION VIII

THERMAL STUDIES

1. INTRODUCTION

The thermal studies were conducted early in the contract in order to allow the use of the results in the reliability test program and the second breakdown studies. This section is primarily a summary of the thermal studies already reported in the two interim reports.[2,3]. Many of the details are left out of this section but can be found in the previous reports.

The physical dimensions of the two transistor designs used in this study are given in Section III. For convenience, the transistor with a double set of emitter fingers is referred to as device A and is shown in Figure 1. The transistor with a single set of emitter fingers is referred to as device B and is also shown in Figure 1. Under this contract the thermal studies conducted were designed to investigate the thermal behavior of a high frequency planar epitaxial power transistor both experimentally and theoretically. Thermal behavior which relates to transistor reliability has been of prime concern. An infrared (IR) microradiometer was used to measure the local surface temperature of operating devices. Variations were obtained for a wide range of steady state operating conditions.

Various electrical methods of measuring the junction temperature of a device were evaluated by comparison with microradiometer measurements. This evaluation has resulted in an explanation for the differences in measurements from the various methods and has indicated the relationship of these measurements to the actual peak junction temperature. Since the measurement of junction temperature is used to determine thermal impedance, θ_{J-C}, this evaluation has been important in understanding how thermal impedance values can be used more effectively. It is primarily necessary to select with care the test operating conditions of transistors in order to determine useful values of θ_{J-C}.

It has been possible to make a better selection of the electrical operating conditions for preliminary measurements on transistors used in the reliability test program. This study has shown that these conditions for testing have a great influence on the effectiveness of the measurements. The electrical operating conditions which result in the greater temperature variation have been determined. Measurements under these electrical conditions should result in better predictions of reliability of the transistors.

By using a theoretical model, it has been possible to determine the current density concentration in the base region under the emitter. The emitter current tends to concentrate along the emitter-base edge as the total current is increased. With this result for the current distribution and a solution for the heat transfer in a silicon chip, temperature profiles were calculated across the surface of the chip. The values of temperature were found to be in close agreement with experimental measurements. These calculations have helped to interpret the details of the experimental data and have extended the understanding of heat generated in transistors. With the ability to make these temperature calculations, it is now possible to evaluate the thermal characteristics of proposed designs.

A discussion of the results of the thermal studies is given in Subsection 2. Subsection 3 gives the conclusions that have resulted from this work and a discussion of additional work that is necessary.

2. DISCUSSION OF RESULTS

a. Temperature Studies of Operating Transistors

With the use of an infrared microradiometer,[18] the surface temperature across a steady state operating transistor has been measured. Isothermal contour maps have been constructed from consecutive temperature profiles as discussed by Peterman.[19] From such isothermal maps, the development of hot spots has been observed for various operating conditions. Figures 65 and 66 illustrate the change in temperature distribution of device A for different operating conditions while holding the power constant. Figure 65 was obtained for $I_C = 5$ A and $V_{CE} = 10$ V. This map indicates a relatively uniform heat dissipation across the active area of the device. The longer emitter fingers produced a little more heating than the shorter ones with a maximum temperature just over 180°C. Figure 66 was obtained for the same device with $I_C = 2$ A and $V_{CE} = 25$ V which maintained operation at the same total power. The maximum temperature increased to over 320°C along the long emitter finger side while the short emitter finger side was dissipating very little heat. Although hot spot formation has previously been predicted and qualitatively observed, the contour maps shown in Figures 65 and 66 are quantitative. Such isothermal contour maps indicate that a mechanism, other than power level, also influences current concentration resulting in local heating and hot spots. Preliminary work to investigate this mechanism is discussed in the second breakdown studies of Section IX.

The operating conditions of a transistor do influence the distribution of power dissipation resulting in temperature variations. Collector-emitter voltages, V_{CE}, of 25 V or higher can result in large temperature gradients and peak temperatures which can exceed 300°C as illustrated in Figure 66 . Such devices are under a greater thermal stress than those operating at a lower V_{CE} and therefore are more prone to thermal runaway and self-destruction. This indicates the importance of the

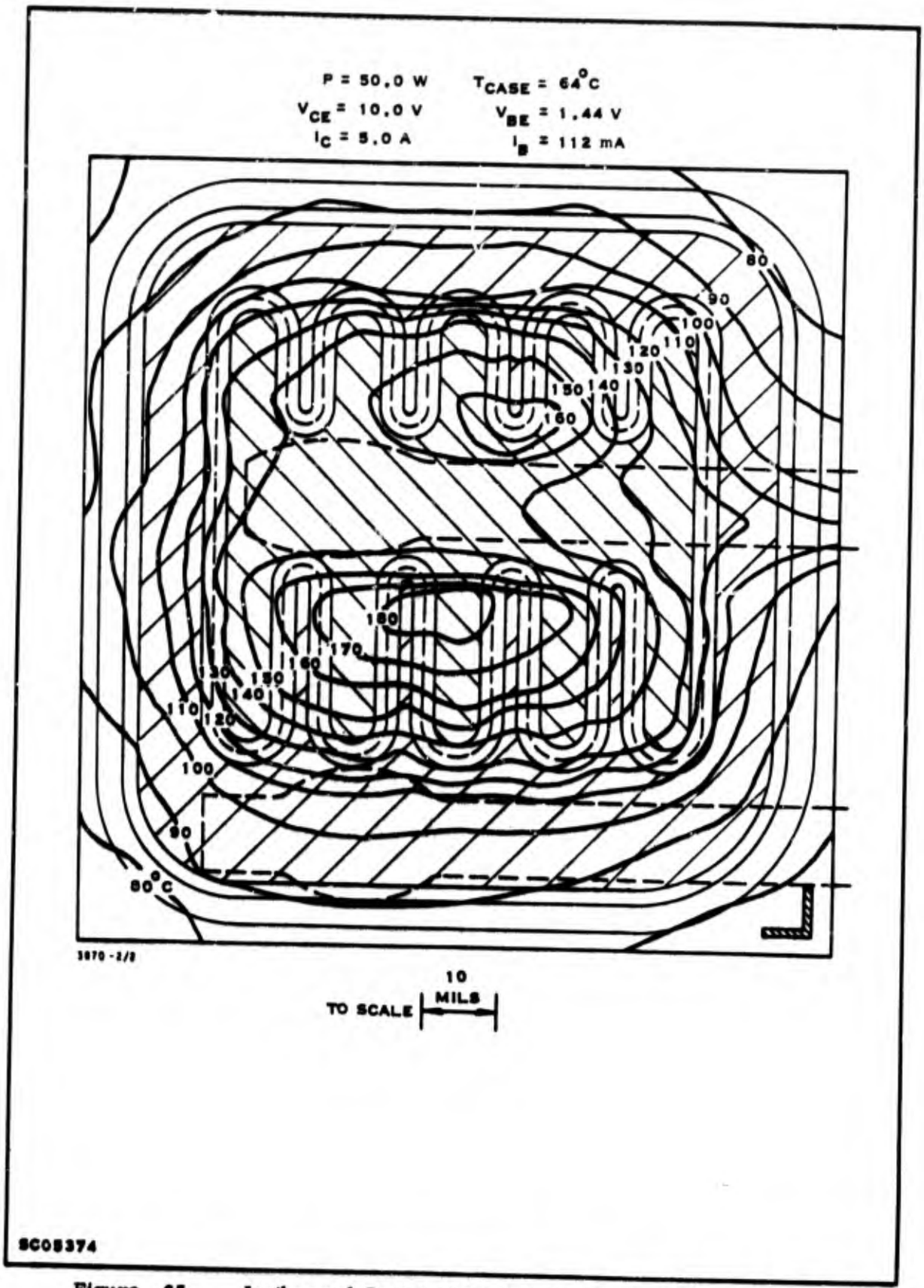

Figure 65. Isothermal Contour Map of a Device A, Transistor No. 1

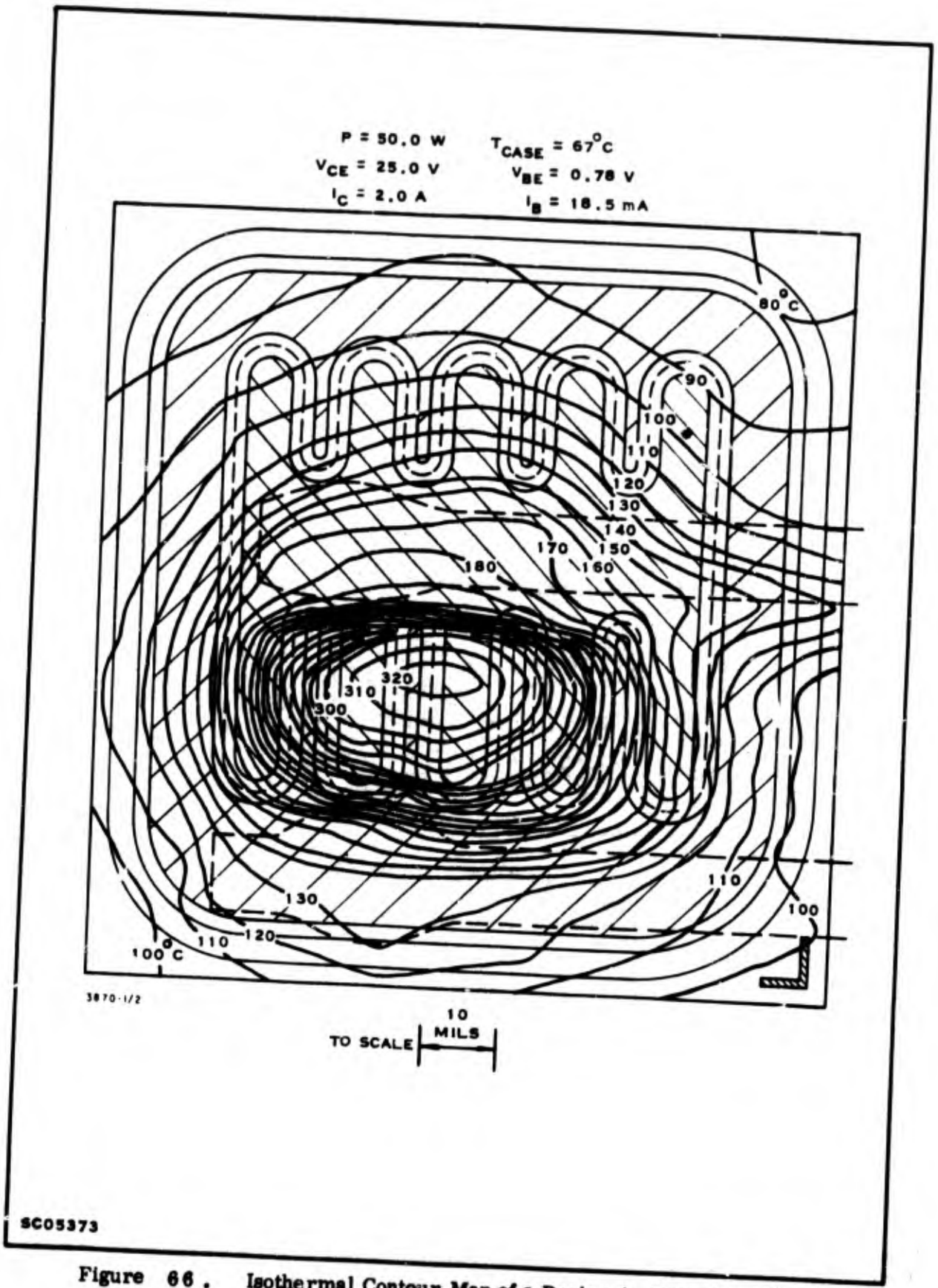

Figure 66. Isothermal Contour Map of a Device A, Transistor No. 1

proper selection of the electrical operating conditions when the thermal impedance of a device is measured. The poor correlation between thermal impedance measurements and reliability of devices under operating conditions can partially be explained by the improper selection of testing conditions. This conclusion was employed in the selection of test conditions used in the latter phase of reliability test program discussed in the Verification Test Program in Section V. Also the electrical methods used to measure thermal impedance of transistors are discussed in detail in Section VIII-2b.

The location of hot spots which may not be located at the center of a transistor chip has been correlated with the location of voids which exist between the silicon chip and the header. Such voids greatly intensify hot spot formations. Figure 67 shows an isothermal contour map of a transistor at the given operating conditions of 20 watts and V_{CE} = 20 V with three hot spots. When this device was over stressed, it went into thermal runaway and resulted in self-destruction. A photograph of the surface of the same transistor after the catastrophic failure is shown in Figure 68. It is obvious that self-destruction took place at the most intense hot spot. An x-ray photograph of the same device is shown in Figure 69 where the lighter areas indicate the voids between the chip and the header. Although many voids are indicated, the largest void was located under the hottest spot and helped to determine the location of failure. A great amount of effort is continually being expended toward improving the process of mounting chips to headers.

Figure 70 shows an isothermal contour map of a transistor of device B. It is seen that only one set of emitter fingers is present. As the power and temperature concentrates, there is not a second set of emitter fingers to become inactive which reduces even further the efficiency of the device. This design appears to have better thermal characteristics over a wider range of operating conditions than the double set of emitter finger structures. This thermal study was very instrumental in the implementation of the new design, device B, earlier than originally planned.

b. Evaluation of Electrical Methods of Measuring Thermal Impedance

The reliability of an operating transistor is influenced by the temperature that it generates.[20] Therefore, it is necessary to use some convenient method to measure the thermal behavior of transistors. The most convenient methods involve the measurement of a temperature dependent electrical parameter which has been calibrated in some manner with temperature. The methods used for the contract work are described in Appendix B. However, it is well known that by using different electrical parameters different values of junction temperature are indicated.[21] Since the junction temperature is not uniform for an operating transistor as shown in Section VIII-2a, it is necessary to correlate the indicated junction temperature with the actual temperature distribution. Therefore, it is not surprising that a discrepancy exists between the various methods.

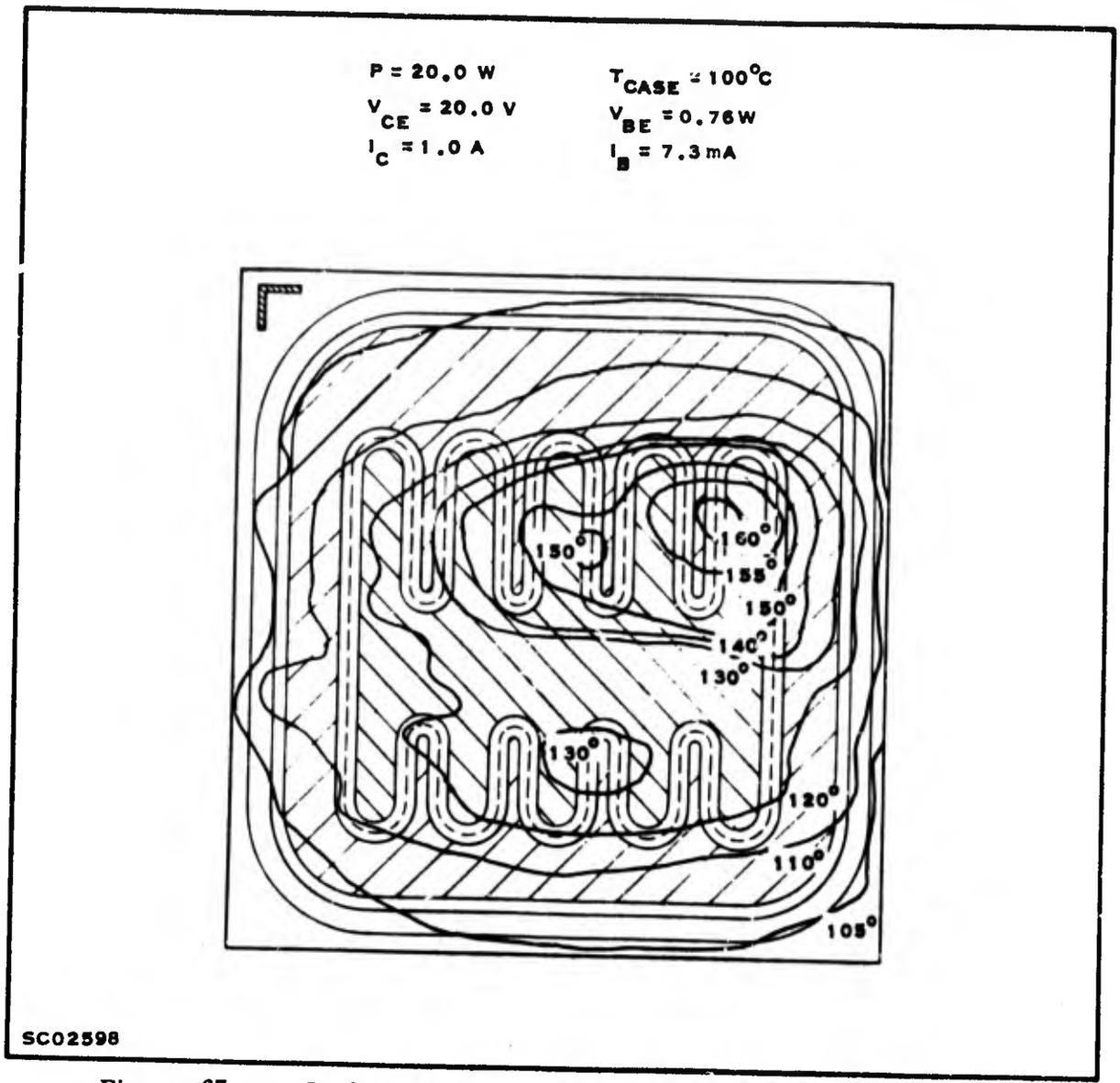

Figure 67. Isothermal Contour Map of a Device A, Transistor No. 2

The maximum junction temperature (T_{J-MAX}) is the critical temperature of a device since it determines the thermal operating limit. The infrared microradiometer can measure directly this parameter (T_{J-MAX}). Since the infrared microradiometer is only a laboratory instrument, it was used to obtain reference data. Junction temperatures (T_J) measured by the V_{CBF} and ZOT (ΔV_{CBF}) methods have been compared with this reference (IR) data. The h_{FE} method [7] gave values which were not consistent with actual measured values and the V_{BE} method [6] gave results similar to the V_{CBF} method. Therefore, the h_{FE} and V_{BE} methods are not included in this evaluation.

The ZOT method [8] has been added to this evaluation because of its convenience of measurement. Although the electronic equipment necessary for this method is quite complex, the actual measurement is very quickly made. This method measures the change in V_{CBF} (ΔV_{CBF}) at two conditions — one before and the other immediately after the application of a power pulse.

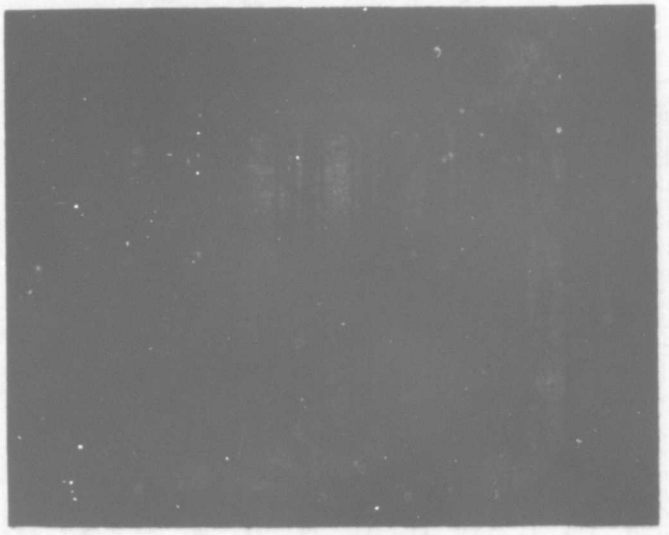

Figure 68. Surface of Transistor No. 2 After Self-destruction Caused Thermal Runaway

Figure 69. X-ray Photograph of Transistor No. 2, Lighter Areas are Voids Between the Silicon Chip and Header

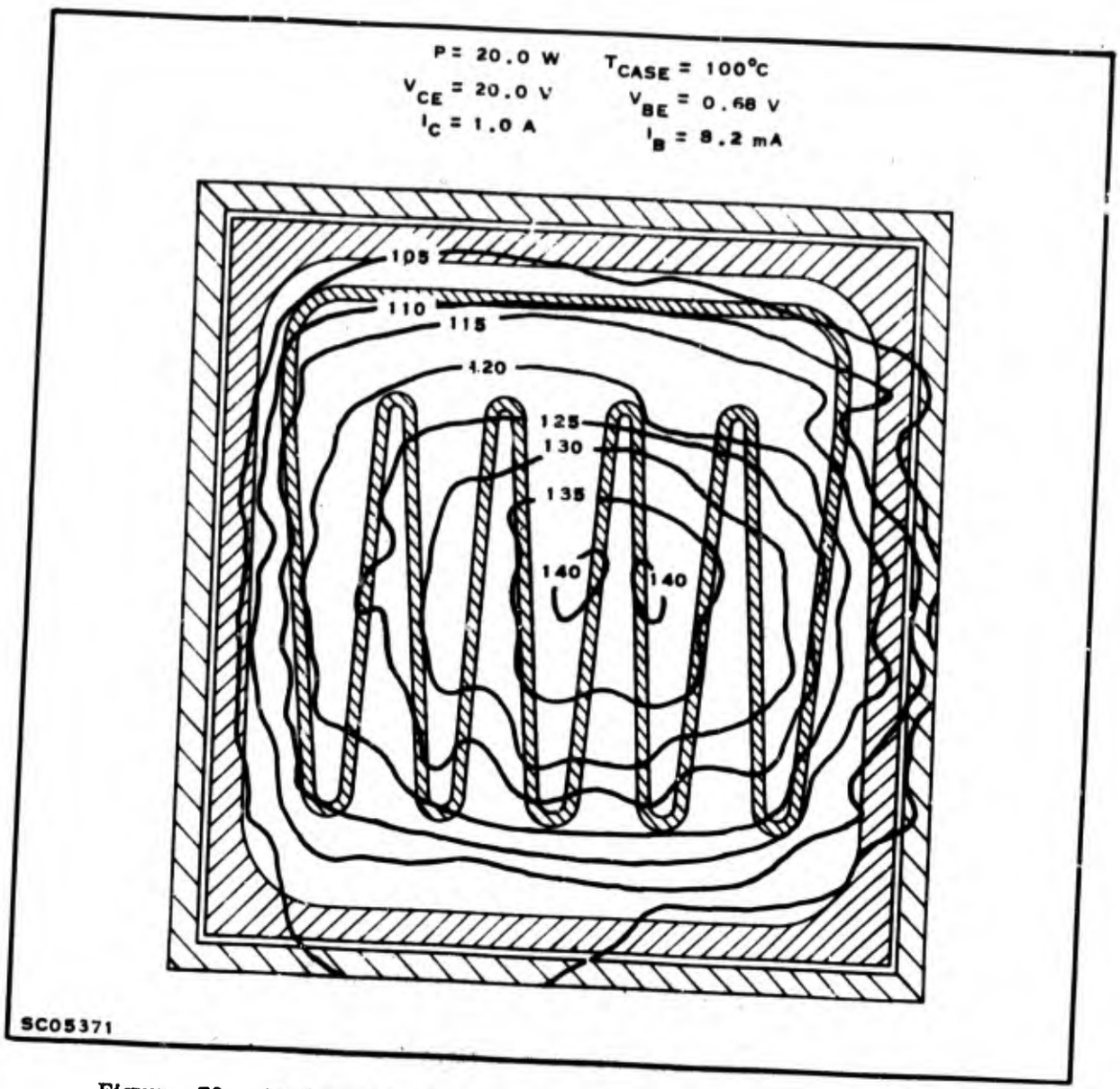

Figure 70 . Isothermal Contour Map of Device B, Transitor No. 3

The resulting change in junction temperature should be large relative to the change in case temperature to simplify this measurement.

Since the temperature distribution of a transistor junction changes with the operating conditions of the transistor, it is necessary to compare the results from the various methods over a range of operating values. Figure 71 shows that the V_{CBF} method indicates the lowest junction temperature although the ZOT method indicates temperature only slightly higher. It should be noted that the data for the V_{CBF} method at V_{CE}= 30 V was obtained for $I_C \leq 0.6$ A and is superimposed on the data for the ΔV_{CBF} method in Figure 71. However, both of these methods indicate temperature rises which are approximately half the temperature rise between the case and the peak temperature.

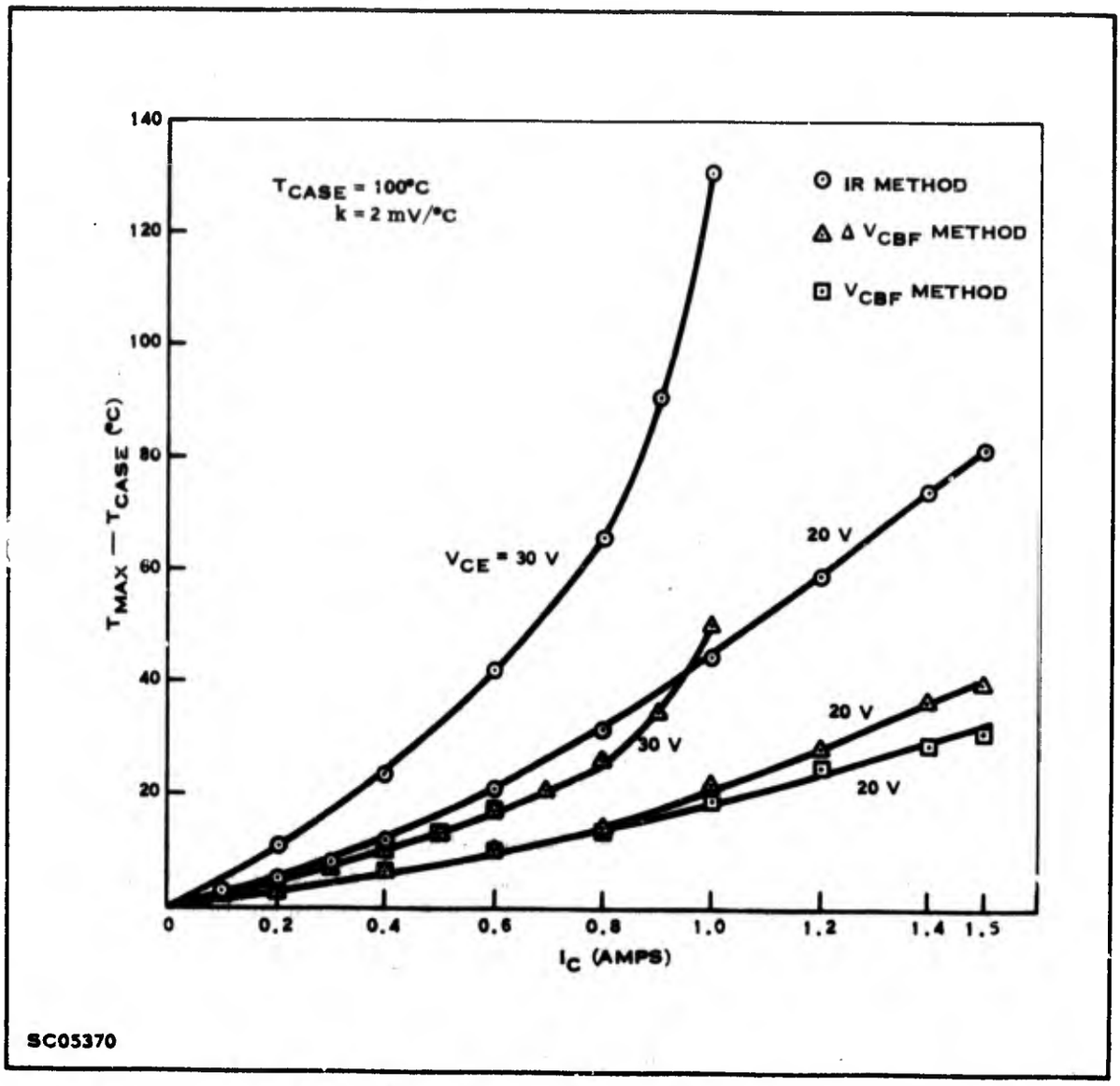

Figure 71. Comparison of Three Methods for Determining T_{MAX}- T_{CASE} vs I_C, Device B, Transistor No. 4

The indicated thermal impedance, θ_{J-C}, for this transistor is shown in Figure 72 . The θ_{J-C} calculated from the ZOT and V_{CBF} methods is approximately half that calculated from the microradiometer measurements. This difference is a direct result of the difference in the indicated temperatures. Also the value of θ_{J-C} varies with operating conditions. This shows the necessity to select with care the test conditions for obtaining θ_{J-C} for a given application, as was indicated in Section VIII-2a.

The change, k, in the V_{CBF} with temperature for this type of device has been determined to be approximately 2 mV/°C. This value was determined when the temperature of the junction was elevated to various uniform temperatures and when no internal power was being dissipated. It is interesting to note that if this value of k is

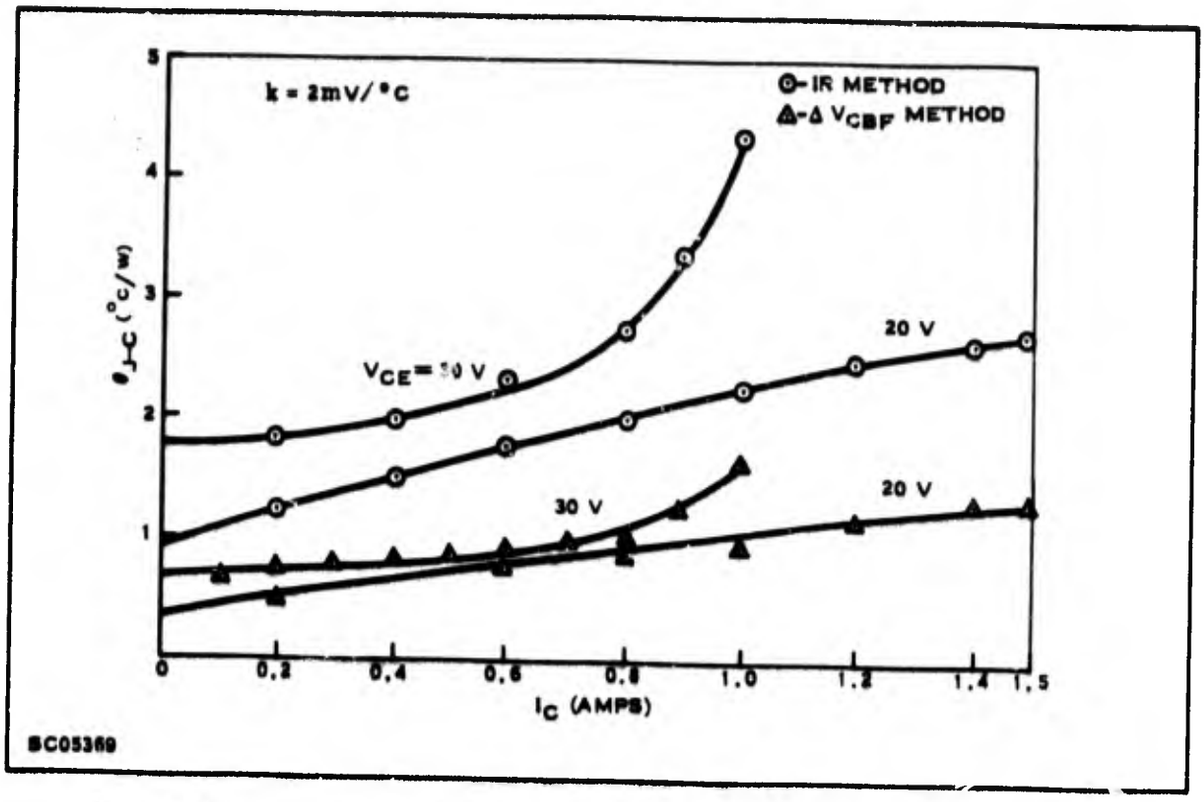

Figure 72. Comparison of Two Methods for Determining θ_{J-C} vs I_C, Device B, Transistor No. 4

taken as only 1 mV/°C then the agreement between the measurements from the V_{CBF} and ZOT methods and the measurements from the microradiometer is very good as shown in Figure 73. This agreement indicates that θ_{J-C} as normally measured is approximately half that value as measured by the reference (IR) method.

Values for the change in V_{CBF} with temperature are very difficult to obtain for operating transistors. These values are determined for uniformly heated junctions but are applied to test data that is obtained when very nonuniform temperatures exist. The nonuniform temperature does imply nonuniform current concentration in the transistor. This concentration will increase the voltage developed (V_{CBF}) for a given total current and will indicate some average temperature.

Since the ZOT method uses a single pulse of power, it is possible to take measurements at much higher operating levels with less danger of damage to transistors. This is why the data by the V_{CBF} method does not cover the same operating range as for the ZOT method. Also since the ZOT method allows measurements to be taken in a short time interval, it lends itself to be used on automatic test equipment. This latter point can have a major impact on reliability by greatly reducing the cost of θ_{J-C} measurements.

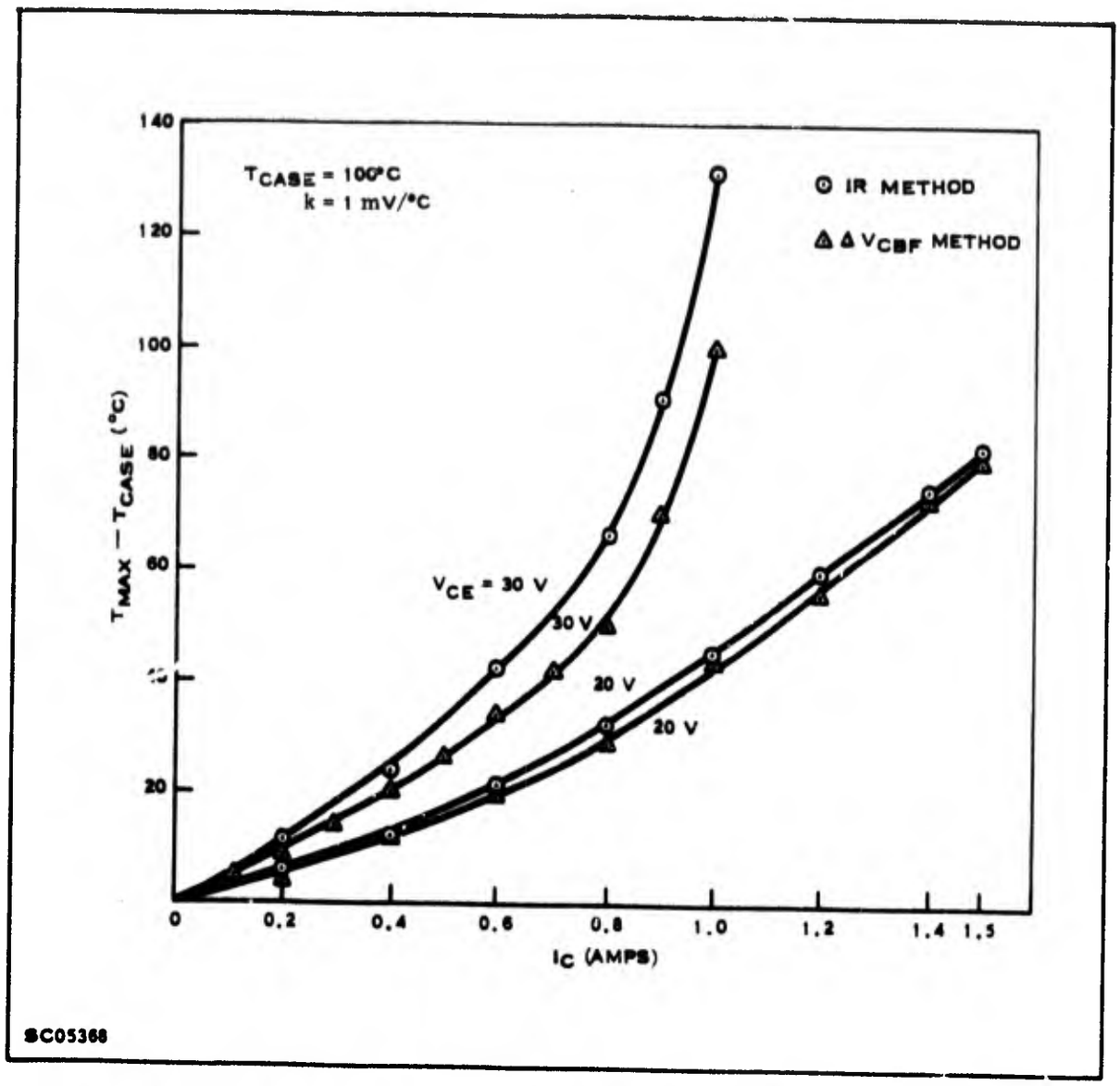

Figure 73. Comparison of Two Methods for Determining $T_{MAX} - T_{CASE}$ vs I_C, Device B, Transistor No. 4

c. Current Distribution Study of Transistors

The understanding of heat generation and transfer in semiconductor devices is one of the most important factors in understanding the thermal behavior of transistors under operating conditions. In order to determine the power dissipation in a transistor, it is necessary to have a thorough knowledge of the current density distribution. Fletcher [22], [23] and Hauser [24] have determined such a current density of simple geometry for the weak injection case where the minority carrier density is very small compared to the net doping density in the base region. Emeis, et al., [25] investigated the strong injection case where the carrier density is very large compared to the net doping density. However, neither of these assumptions is valid at normal current density levels which exist in commercial power transistors.

A solution for the current density for the arbitrary injection level has been determined which is applicable to certain power transistor geometries. The details of obtaining this solution have been reported earlier. From this solution it has been possible to calculate the collector current density along the region under the emitter.

It was determined that as the total current was increased, more current is concentrated along the emitter edge. This concentration of current along the edge of the symmetrical emitter greatly influenced the operation of the device, particularly in determining the limit of its safe operation. For device A, it was found that for emitter currents of over 1 A, the current density will vary by more than a factor of 10 across the emitter. This variation is illustrated in Figure 74 . Current densities at the emitter edge are normalized to unity for several values of total current. As the total current increases from 0.1 to 1.75 A, the variation of the current density across the emitter changes from 0.65 to 0.06 of the edge value.

d. Heat Transfer in Transistors

To study the heat transfer in a transistor, a two-dimensional heat transfer problem was solved for a rectangular chip which was applicable to planar power transistors. The heat generation was assumed to be primarily at the collector-base junction with the current density determined by the results of the current density study. It was also assumed that this junction was located at the surface of the device.[26]

From this solution, temperature profiles were calculated and compared to actual device data. Figures 75 and 76 illustrate such a comparison for a geometry consisting of 5 emitter fingers of 9 mil width and 5 mil spacings on 100 x 100 x 8 mil silicon chip, device A. Figure 75 gives a calculated temperature profile for a current distribution which gives a total dissipation of 50 W at 5 A. The temperature profile given in Figure 76 is from experimental measurements taken on a device of the same geometry. This comparison shows that the heat transfer model is quite good since the magnitude is about the same although the details do not give perfect agreement. The primary shortcoming of the model results from not including the effect that the different layers of material contribute. The extreme peaks and valleys of the calculated temperature result from not including the layer of material above the junction region. The rounding of the peaks toward the side is enhanced by the copper header material which also is not included in the model.

However, the agreement with experimental data is good and indicates that the basic understanding of temperature variation has been established. It is now necessary to refine this understanding in order to study the more severe effects that temperature variation creates.

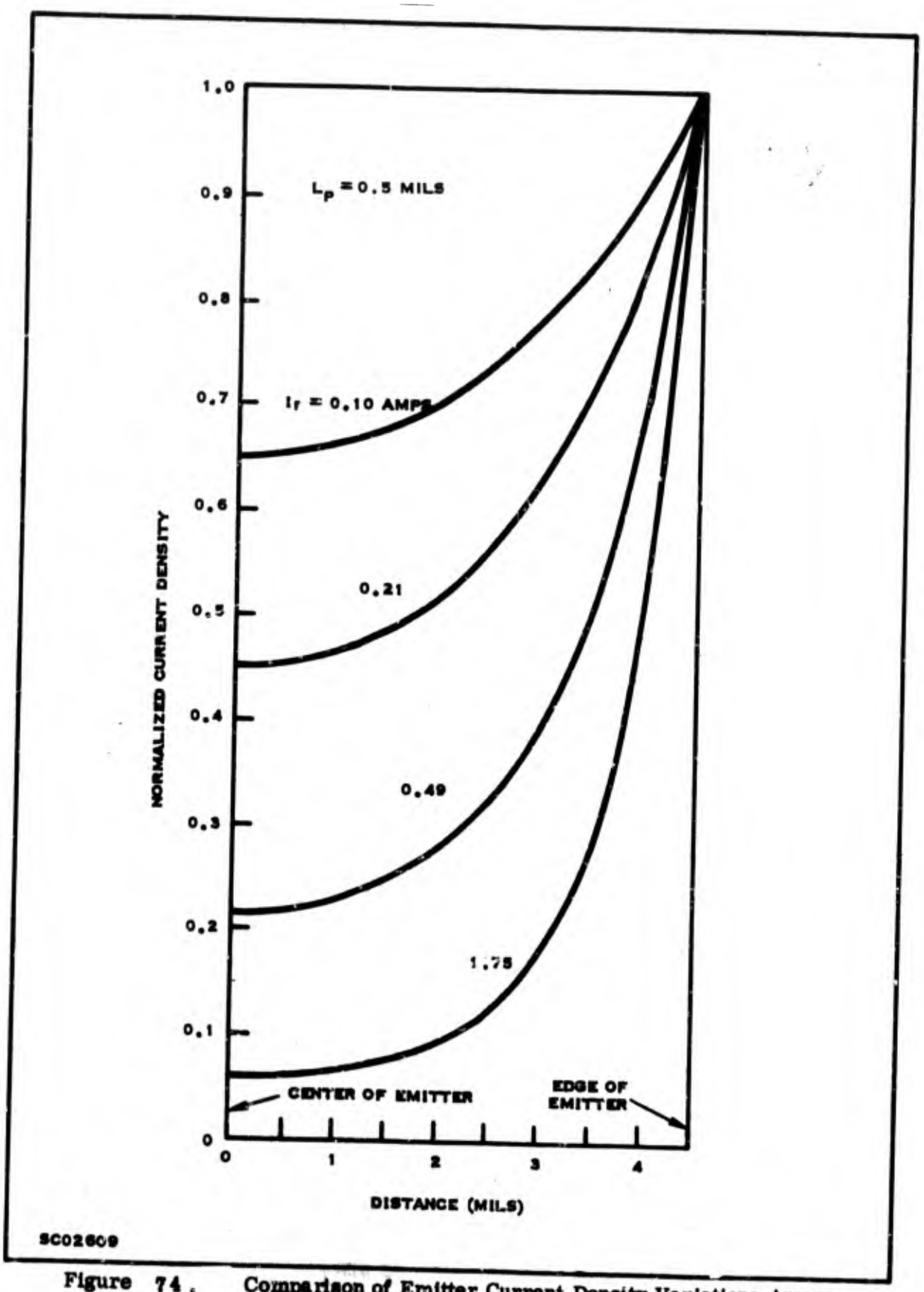

Figure 74. Comparison of Emitter Current Density Variations Across an Emitter Finger, Device A Transistor

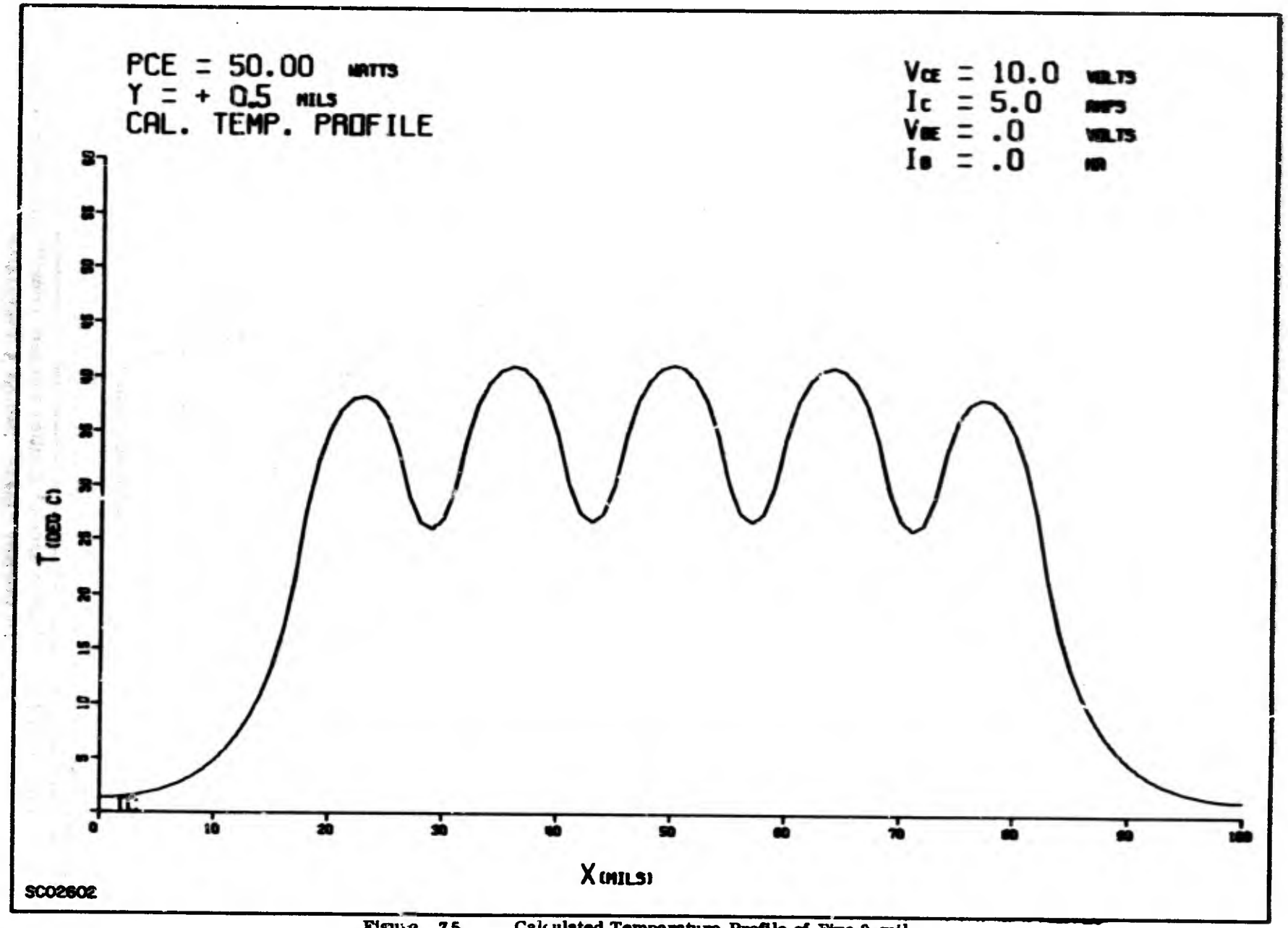

Figure 75. Calculated Temperature Profile of Five 9-mil Emitter Fingers With Uniform Heat Generation, Device A

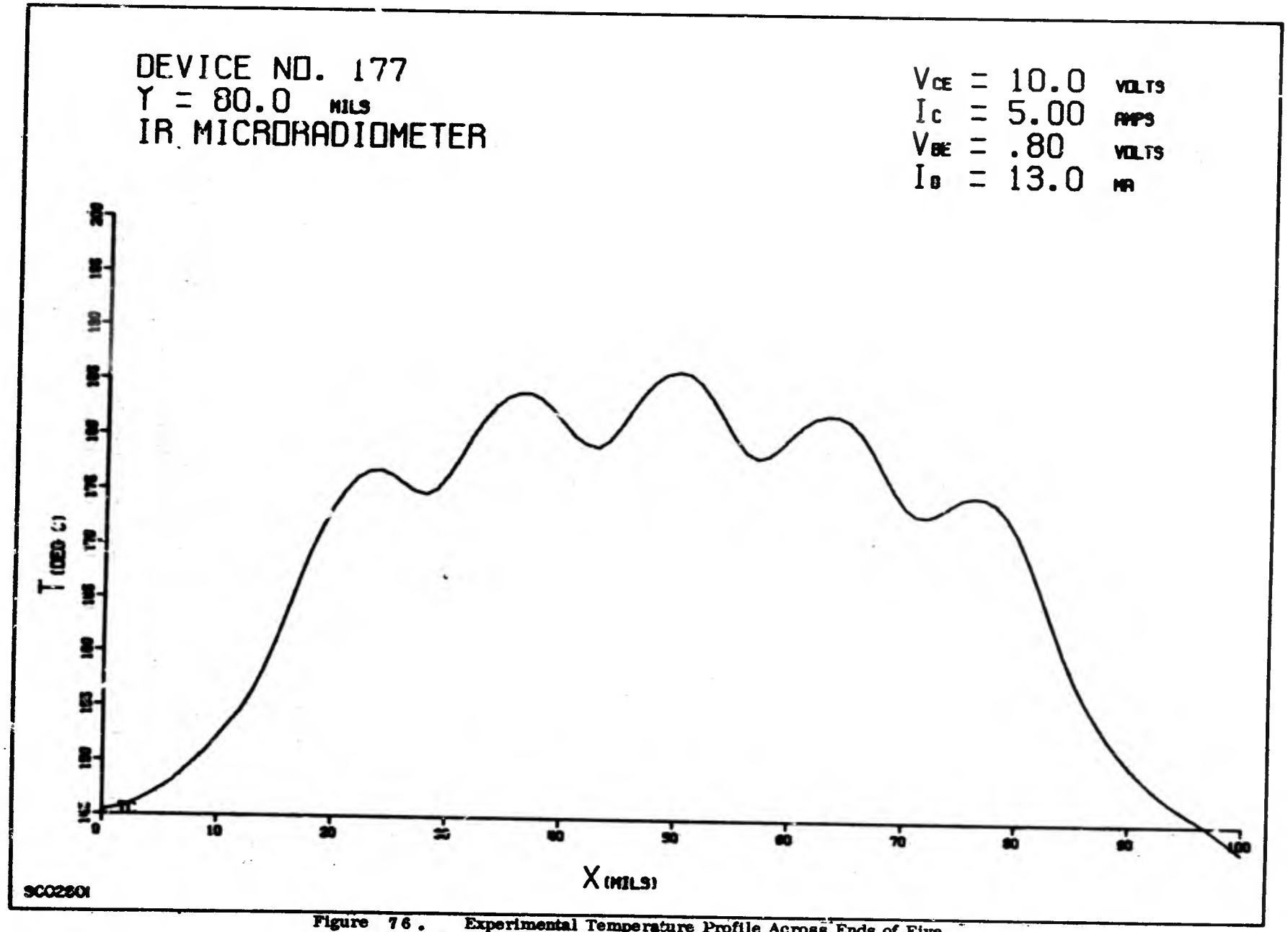

Figure 76. Experimental Temperature Profile Across Ends of Five 9-mil Emitter Fingers With Uniform Heat Generation, Device A

3. CONCLUSIONS

The general thermal properties of high-frequency power devices are much better known and understood. With the use of the infrared microradiometer, it has been possible to study the operating temperature of transistors with very little disturbance of its performance. A result of this work is the determination of the temperature distribution for a transistor which shows that the peak operating temperature is much higher than was previously thought. The maximum operating temperature for silicon devices was believed to be a little above 200°C but it is now known that silicon devices do operate above 300° C, although the maximum operating temperature still has not been established because of other limitations of the device construction. Many devices have been operated with their surface temperature above 300°C and they have performed very well.

The most misleading aspect about the operating temperature of a transistor has been the inability to evaluate various methods for measuring junction temperature. With the use of the infrared microradiometer, some of the limits of the thermal impedance determined by these measurements are now established, and much better correlation of thermal impedance and device failure are possible. A more realistic use can now be made of the present methods for measuring thermal impedance, and new methods can be sought to improve its usefulness. The present knowledge of the various methods has been applied to the latter portion of the reliability test programs. These results are discussed in Section V.

The mathematical models generated to study the internal operation of a transistor are also helpful in understanding its thermal behavior. A study of the current flow through a device is necessary to determine the heat generated in it. Concentration of the current along the edge of the emitter-base junction can now be computed and is used to calculate the heat dissipated across the emitter. By combining this capability with a solution of the heat transfer problem for transistors, a temperature profile across the surface of a transistor can be computed. Within the assumption used, the present results agree very well with experimentation and helps support the interpretation of experimental data. With the aid of these models, the adaptability of extending the present general understanding of one particular transistor which has been under study can be more fully examined and utilized.

Results of this study can be summarized as:

a) Infrared microradiometer techniques were developed to obtain quantitative surface temperature profiles.

b) Temperature profiles were used to obtain isothermal contour maps of the power transistor during operation.

c) Hot spot formation was demonstrated using isothermal maps.

d) Areas of self-destruction in a transistor were correlated to location of hot-spot generation.

e) Current distribution within operating transistors was calculated.

f) Heat generation within transistors was determined from its current distribution.

g) A simplified heat transfer model was solved for a transistor using realistic heat generation.

h) Good quantitative agreement was obtained between computed and observed temperature profiles of a transistor.

i) Electrical methods for measuring thermal impedance were evaluated.

j) Thermal impedance measurements were interpreted.

k) Results of thermal studies were used to understand the operation of transistors and to interpret results from reliability test programs.

This thermal study has extended the knowledge of the thermal behavior of transistors in order to help design and screen devices which are more reliable. However, much work remains to be done in order to completely understand this behavior. Once this understanding is complete enough, transistors can be designed to minimize the influence of temperature or to use this dependence for a beneficial purpose. More emphasis must be placed on the understanding and use of the thermal properties of semiconductor devices in order to achieve a maximum utilization of the devices capabilities.

Some areas of study that should be continued are as follows:

a) Effect of temperature variation on current densities in semiconductor devices.

b) Heat transfer solution of multi-layer material chips on an enlarged heat sink.

c) Effect of resistance in the emitter leads on hot spot formation.

d) Study novel design of chips to reduce thermal effects.

e) Investigate better ways to mount chips on heat sinks.

f) Determine values of temperature present at thermal runaway.

g) Determine actual safe operating conditions for transistor.

h) Develop new electrical methods of measuring junction temperature.

SECTION IX

SECOND OR THERMAL BREAKDOWN STUDIES

1. INTRODUCTION

a. General

The work reported is a study of second (thermal) breakdown and its relation to device reliability. The breakdown phenomenon causes a high proportion of device failures and limits the operating region of the device. It was first observed in transistors[27] but has recently been found to occur in diodes[28] and even n^+nn^+ structures.[29,30] The breakdown is not inherently damaging, but the high temperatures associated with it commonly cause device degradation or catastrophic failure.

Two classes of breakdown can be distinguished in transistors (although there are intermediate cases). The first occurs with reverse base bias and normally occurs very rapidly compared to the other one, which is seen under forward base bias. In support of recent efforts to improve the terminology of this subject, this report uses thermal breakdown to refer to the latter, and second breakdown is restricted to the former. This report covers thermal breakdown in planar epitaxial silicon transistors and, in particular, the study vehicle which is described in Section III.

b. Previous Approaches

The phenomena of second and thermal breakdown have been the subject of considerable study.[31,32] Recent interest has focused on two major areas, the thermal-electrical interactions causing concentration of current into a hot spot prior to breakdown[33,34] and the existence of a molten region or a solid-state plasma within the device after breakdown[35,36,37,38] The thermal-electrical interactions are twofold: the heat flow pattern and, therefore, temperature distribution depend on the disposition of the power dissipation; current injection density across the emitter-base junction depends exponentially on the temperature distribution in the plane of the junction. Thus, any active area of the device with a higher thermal resistance to the heat sink, or carrying more current because of some defect, or just hotter as a result of device geometry, will become hotter than the remainder of the active area, and will then carry a higher current density and become still hotter. This sequence may, as with Achilles and the Tortoise,[39] converge to a specific distribution (Achilles faster than

Tortoise) or diverge (vice versa) to form extreme concentrations of current. Scarlett, Shockley [33, 34] and others [41] discuss the stability of the situation, and the work reported here is a modification and extension of their work.

c. Approach

The formation of a hot spot by thermal-electrical interactions is a necessary prelude to the breakdown of this hot spot, without which thermal breakdown would not occur except at extreme power levels. The present study was therefore concentrated on these interactions.

A representative model of the heat and current flow with the resulting temperature, voltage, and current relations was established. The behavior of this model was then studied, as a function of changing device parameters. No consideration was given to device defects, as other studies have shown [40, 42] that geometrical factors outweigh all but the most severe semiconductor defects, and voids between the device and the header, although important, are difficult to model and do not contribute to understanding the phenomenon. Their effects are primarily accelerations of the basic process described by the model.

d. Summary of Remainder of this Section

Section IX-2 contains a detailed description of the device model and its relation to real devices, and the method used to study the behavior of this model. Section IX-3 gives the results, in the form of the model behavior itself, and the agreement with experimental results. Section IX-4 is a discussion of the mechanisms contributing to thermal breakdown. Section IX-5 contains the conclusions and some suggestions for future work.

2. THE DEVICE MODEL

a. Relation of Model to Real Devices

A silicon planar epitaxial power transistor has a rectangular silicon chip mounted on a thermally conducting header. The model uses a cuboid (a rectangular parallelapiped) of uniform thermal conductivity. By appropriate choice of cuboid thickness, we may simulate the chip alone on a perfectly conducting header, or the chip and header together. In the case of multiple layer structures, an approximation can be obtained by reduction to a one layer structure, with suitable choice of size and material properties. A perspective sketch of the model is given in Figure 77. The active area of a device is defined primarily by the pattern chosen for the emitter diffusion, and a rectangle is normally a good approximation, with base contact intrusions to keep the base voltage as uniform as possible over the area. A few typical patterns illustrating this are shown in Figure 78. The model assumes a rectangle, split up into 16 lumped elements (Figure 77). The diffusions in planar devices are generally

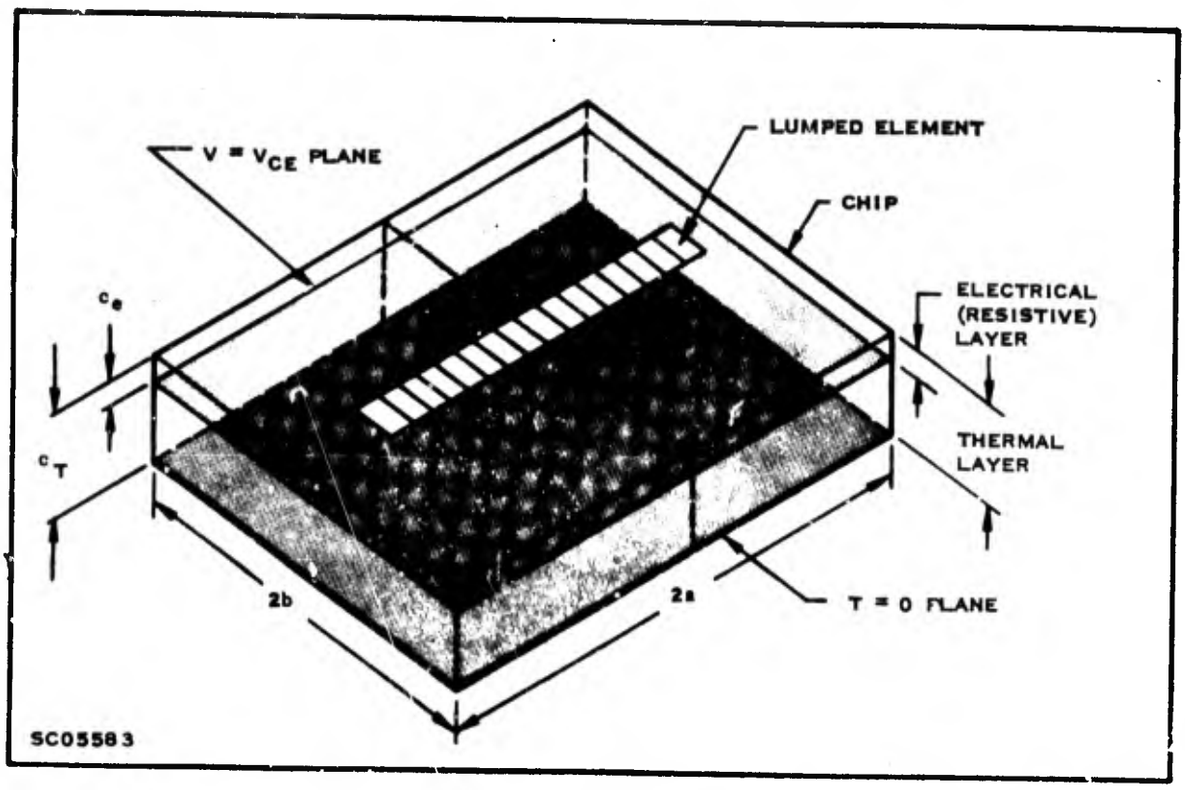

Figure 77. Sketch of Model

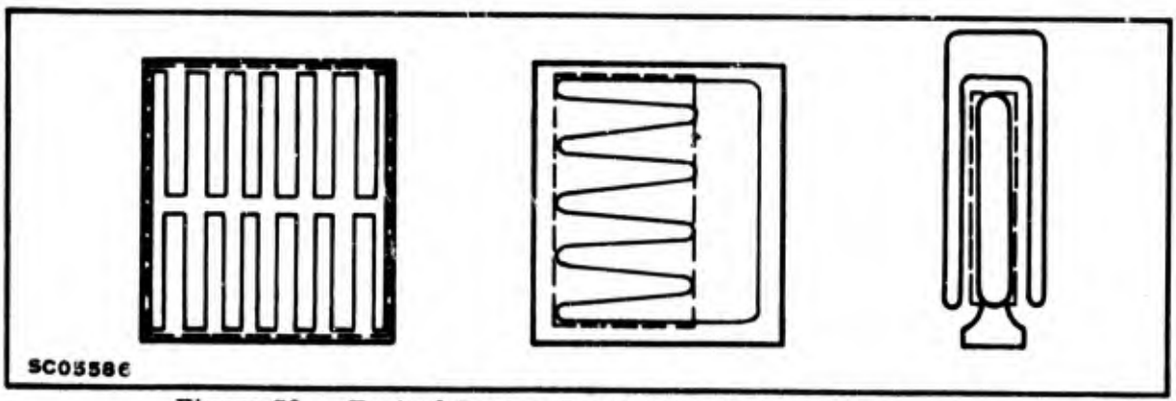

Figure 78. Typical Device Geometries Showing Rectangular Approximation to Emitter

shallow compared to other device dimensions, and it is convenient to assume that both junction planes lie at the top surface. The thickness of the epitaxial layer (for a non-epitaxial device, the bulk resistive region in the collector) is significant, and the model assumes a resistive layer whose thickness may be very different from the effective thermal thickness.

b. Description of Physical Model

In the description, device symbols are used for the related model parameters where practicable. A list of the symbols used and their meanings is given in Table 27. The assumptions made are in general described in terms of the device-related equivalent. The bottom and sides of the model are held at a constant temperature and the thermal conductivity is assumed to be constant. The top surface is thermally insulated, but a uniform power density is injected in each element. The power density varies from element to element according to the electrical conditions described below. The steady-state heat conduction equation (a Laplace equation for the temperature)

$$\nabla^2 T = 0 \tag{1}$$

is solved for an element in the center of the model with unit power density, and the resulting temperature rises at all elements determined by Fourier analysis. It is assumed that all elements are sufficiently remote from the edge of the chip that this temperature rise is only a function of the distance between the elements, so the "mutual thermal resistance" between elements i and j is given by the functional relation

$$\frac{\partial T_j}{\partial P_i} = \theta_{ij} = \theta(|i-j|)$$

If the power density in the ith element is given by P_i, the jth element temperature rise ΔT_j is given by

$$\Delta T_j = \sum_i P_i \, \theta(|i-j|) \tag{2}$$

The $\theta(|i-j|)$ need only be calculated once for each element size, chip size, and thermal resistance. Similarly, the bottom and sides of the resistive layer are held at the applied voltage V_{CE} and the mutual electrical resistances $R_{ij} = R(|i-j|)$ are calculated from the Laplace equation analogous to Equation (1),

$$\nabla^2 V = 0 \tag{3}$$

for uniform current density in the ith element and constant resistivity. The voltage drop at each element due to the element current I_i flowing in the resistive layer (note that the element current is proportional to the current density for constant element area) is given by

$$V_j^d = \sum_i R_{ij} I_i = \sum_i R(|i-j|) I_i \tag{4}$$

Table 27. List of Symbols

Symbols	Definitions
e	Electronic charge
E_g	Semiconductor energy gap (1.1 eV for silicon)
I_o	Current factor (saturation current or recomb./gen. current)
I_i	Element current in the ith element
I_e	Total emitter current
I_c	Collector current
k	Boltzmann's constant
K, K', K''	Constants replacing slowly varying functions of temperature
n_i, n_p, p_n	Carrier densities; intrinsic, electrons in p material, and holes in n material, respectively
P_i	Total effective power dissipation at the surface of the ith element
P_i^j	Power dissipation at the junction in the ith element
P_i^r	Power dissipation in the resistive layer due to I_i
R_{ij}	Voltage drop at element j due to unit I_i (mutual electrical resistance)
$R(n)$	Mutual electrical resistance between two elements n elements apart
T	Temperature at any point in thermal layer
T_i	Absolute temperature of the ith element top surface
ΔT_i	Temperature rise of the ith element top surface
V	Voltage at any point in resistive layer
V_{BEi}	(Average) base-emitter voltage in ith element
V_{CE}	Voltage applied between the emitter and the bottom of the resistive layer
V_i	Voltage between top of resistive layer and emitter at ith element
V_i^d	Voltage drop in resistive layer to ith element
α, β	Constants related to relative diffusion and recombination currents
θ_{ij}	Temperature rise at element j due to unit P_i (mutual thermal resistance)
$\theta(n)$	Mutual thermal resistance between two elements spaced n elements apart

and the remaining voltage across the junctions is

$$V_j = V_{CE} - V_j^d = V_{CE} - \sum_i R(|i-j|)\, I_i \tag{5}$$

The element currents I_i are given by expressions of the type

$$I_i = I_o \exp\left[\frac{eV_{BEi}}{\alpha k T_i}\right] - I_o \tag{6}$$

where α is between 1 and 2, and I_o is related to element area and n_i, n_p, and p_n, depending on the injection level, recombination-generation rate, etc., but is of the form

$$I_o \simeq K'' \exp\left[\frac{-E_g}{2kT_i}\right]$$

where K'' varies slowly with the absolute temperature T_i. Thus, since $I_o \ll I_i$

$$I_i \simeq K'' \exp\left[\frac{\beta eV_{BEi} - E_g}{2kT_i}\right] \tag{7}$$

where $\beta = 2/\alpha$. Now within the current and temperature ranges of interest, β, e, and E_g are constant. If we neglect the lateral voltage drop in the base due to lateral base resistance, we can assume that the V_{BE} for each element is the same at any given instant, so that we may replace $1/2(\beta eV_{BEi} - E_g)$ by D and write the ratio between element currents

$$\frac{I_i}{I_j} \simeq \exp\left[\frac{D}{kT_i} - \frac{D}{kT_j}\right] = \exp\left[\frac{D}{kT_iT_j}\,(T_j - T_i)\right] \tag{8}$$

Since the proportionate change in the product $T_i\,T_j$ is much less than the difference in element temperatures, and also D will be negative and increase in magnitude with temperature, we may define a constant K as an average value of the quantity $D/k\,T_i\,T_j$ and put

$$\frac{I_i}{I_j} \simeq \exp\left\{K(T_j - T_i)\right\} = \exp\left\{K(\Delta T_j - \Delta T_i)\right\} \tag{9}$$

An additional effect to be considered is that of element saturation when the collector-base junction becomes forward biased. This is equivalent to the collector-emitter voltage falling to near zero, and can be allowed for in the model by multiplying each current I_i by a factor

$$\left(1 - \exp\left|\frac{-eV_i}{kT}\right|\right)$$

The offset voltage at the junction

$$V_i \neq 0 \text{ at } I_i = 0$$

is ignored because this is small compared to normal operating voltages. This gives

$$\frac{I_i}{I_j} \simeq \exp\left\{K(\Delta T_j - \Delta T_i)\right\} \frac{1 - \exp\left|\frac{eV_i}{kT}\right|}{1 - \exp\left|\frac{eV_j}{kT}\right|} \tag{10}$$

$$\simeq \exp\left\{K(\Delta T_j - \Delta T_i)\right\} \frac{1 - \exp(K'V_i)}{1 - \exp(K'V_j)}$$

where K' is constant.

It is convenient at this point to introduce a further constraint on the model specifying the circuit conditions in which the device operates. For study, it is useful (and relevant) to fix the total device current,

$$\sum_i I_i = I_e \simeq I_c \tag{11}$$

The element currents are completely specified by Equations (10) and (11).

Dissipation in the ith element at the junction plane is

$$P_i^J = V_i I_i \tag{12}$$

and the dissipation in the resistive layer due to the ith element current is

$$P_i^r = V_i^d I_i \tag{13}$$

The latter dissipation is distributed throughout the resistive layer, and its effect on the temperature profile is too complex to assess exactly. However, the thickness of the resistive layer is generally small compared to the lateral extent of the active area of a power device and we may neglect the dissipation in the jth element due to the current in the ith element (except when i = j) and the dissipation outside the active area. The dissipation is approximately uniform below the originating element, and may be considered as occurring on the center plane of the resistive layer (Figure 79). This is equivalent to an effective dissipation at the surface given by

$$P_i^r \frac{2c_t - c_e}{2c_t} \tag{14}$$

where c_t and c_e are the thicknesses of the thermal and electrical layers respectively (Figure 77). Thus, the total effective power dissipation density P_i is the sum of Equations (12) and (13),

$$P_i \simeq \left[V_i I_i + (V_{CE} - V_i) I_i \frac{2c_t - c_e}{2c_t} \right] / A \tag{15}$$

where A is the element area.

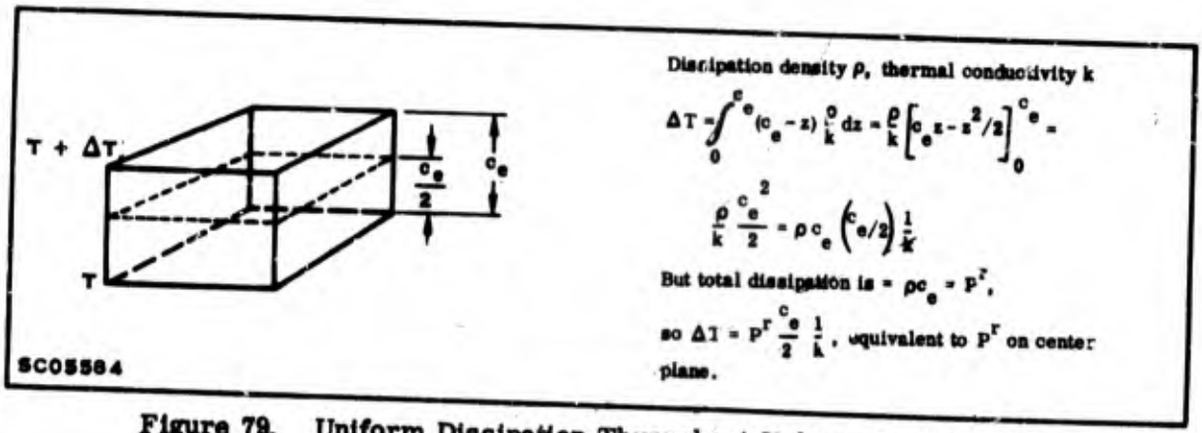

Figure 79. Uniform Dissipation Throughout Volume Equivalent to Total Dissipation in Center Plane

The model does not consider the effects of leakage currents on the current flow. For a silicon device at moderate temperatures these currents are negligible; but this assumption, together with others such as the constancy of electrical resistivity, limits the validity of the model at temperatures of more than about 300°C.

c. Method of Solution by Iteration

Equations (2), (5), (10), (11), and (15) form a set of nonlinear simultaneous equations, with 65 unknowns. Direct solution is impracticable, but examination of the equations will show that an initial choice of a set of currents I_i will allow successive substitution in Equations (5) to give V_i, then (15) to give P_i, and (2) to give ΔT_i. We may then substitute these in Equations (10) and use (11) to give a new set of I_i values. The process may then be repeated. This iterative operation will correspond qualitatively to the processes occurring in the device itself under a step function applied pulse. The electrical time constants will be small compared to thermal time constants, so the current, voltage, and power distributions will correspond exactly to the temperature distribution. In this case, the temperature and current density are initially uniform. The power dissipation will lead to a new temperature distribution. This changing temperature will alter the current distribution, and hence the voltage and power distributions, and so on. The rate of change of the temperature will be proportional to the difference between the instantaneous temperature and that temperature corresponding to the instantaneous power dissipation. The rate will also depend on the effective thermal capacity of an element, which will not change greatly. The temperature given from the power dissipation by Equation (2) is in effect extrapolated at the rate of change over one thermal time constant as illustrated in Figure 80. Thus, the number of iterations performed will give a qualitative indication of the time elapsed in a real device.

d. Possible Iteration Limits

There are several possible paths for an iteration process. The most desirable is for the iteration to converge to a state where further iteration regenerates essentially the same state. This corresponds to a relation between successive iterations similar to that shown in Figure 81a where the two converge. It is also possible for the iteration process to diverge, corresponding to Figure 81b. This would correspond to a real device behavior, for temperatures within the range in which the model is valid. A further possibility is for successive iterations to oscillate about some value as shown in Figure 81c. This was observed to occur for situations in which a number of elements saturated. These oscillations appear to be caused by the large extrapolation step size in the iteration process. The oscillations were reduced and in many cases eliminated by interpolation between successive iterations, and probably do not correspond to device behavior.

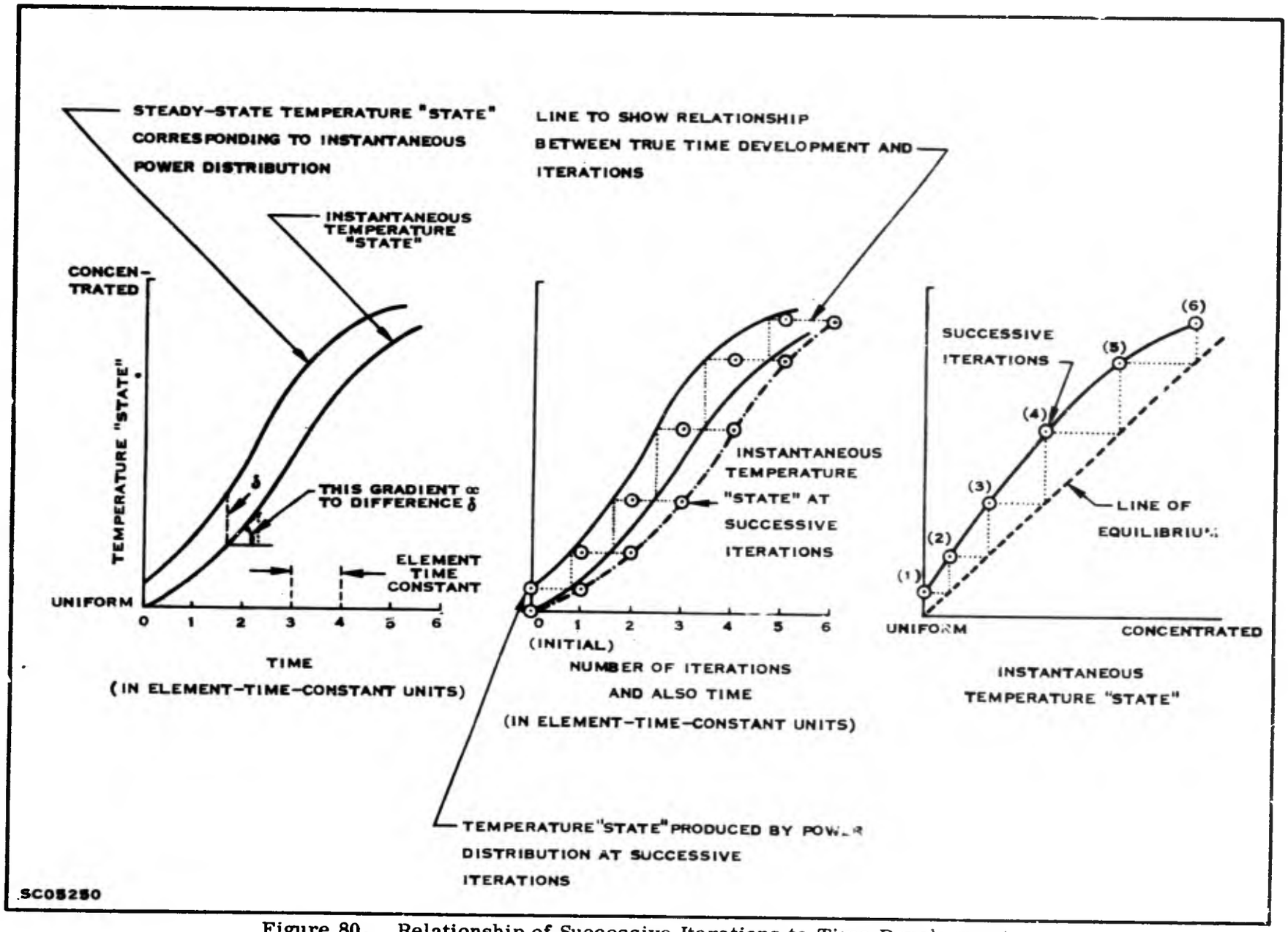

Figure 80. Relationship of Successive Iterations to Time Development

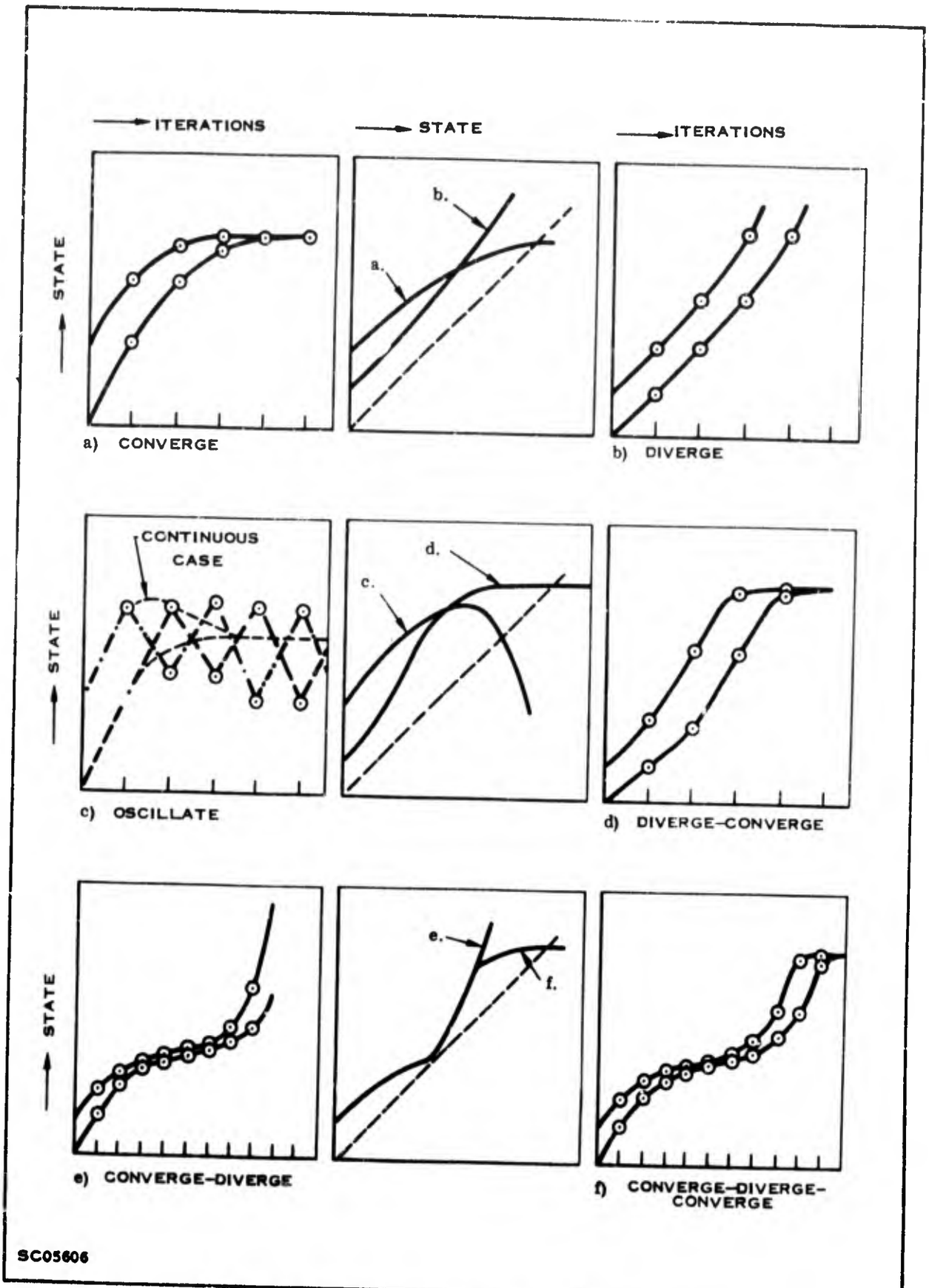

Figure 81. Possible Paths for Iteration and Continuous Behavior
Iteration and Relative Time Scale for (e) and (f) Half that of (a) Through (d)

More complex paths can also occur. A solution may diverge initially, then converge (Figure 81d) or nearly converge initially, then diverge (Figure 81e), or nearly converge, then diverge, then converge (Figure 81f). All these situations have been observed, although the diverging paths might have converged if allowed to continue beyond the range of applicability of the model. The path shown in Figure 81f is the most general path observed, and all others can be considered special cases in which one part is suppressed, or the path is truncated. This is discussed in Section IX-3.

If the major part of the current is carried by a few elements, the nearly continuous nature of the model breaks down. Provision was made to recognize this situation, and to reduce the element size, reapportion the currents, and recalculate the mutual electrical and thermal resistances if this situation should arise in the course of an interation.

The reasons for terminating an iteration are as follows:

1) Iteration has reached a stable state.

2) Peak temperature has exceeded some value beyond the range of validity of the model.

3) Number of iterations has exceeded a preset value, and the iteration is probably oscillating.

4) Element size has been reduced to a level where it is not useful to reduce it further.

5) Device is completely saturated and cannot carry the current specified at the specified voltage.

A set of computer programs was written to perform the iteration, subject to the various constraints above; to print out in graphical form the progress of the iteration and the states at certain intermediate conditions; and to print out the final state, together with other information about the reasons for termination, etc. The programs are discussed in Appendix H.

3. RESULTS

a. The Model Behavior

The iteration process was performed for several geometries at constant values of V_{CE} and the other parameters for a succession of values of I_c. The computer program will do this automatically. At low powers the iteration behaves much as indicated in Figure 81a, converging rapidly to a stable distribution. A typical plot of the successive iterations is given in Figure 82 and the final stable distribution in Figure 83. A plot of the peak temperature of the stable distribution against current

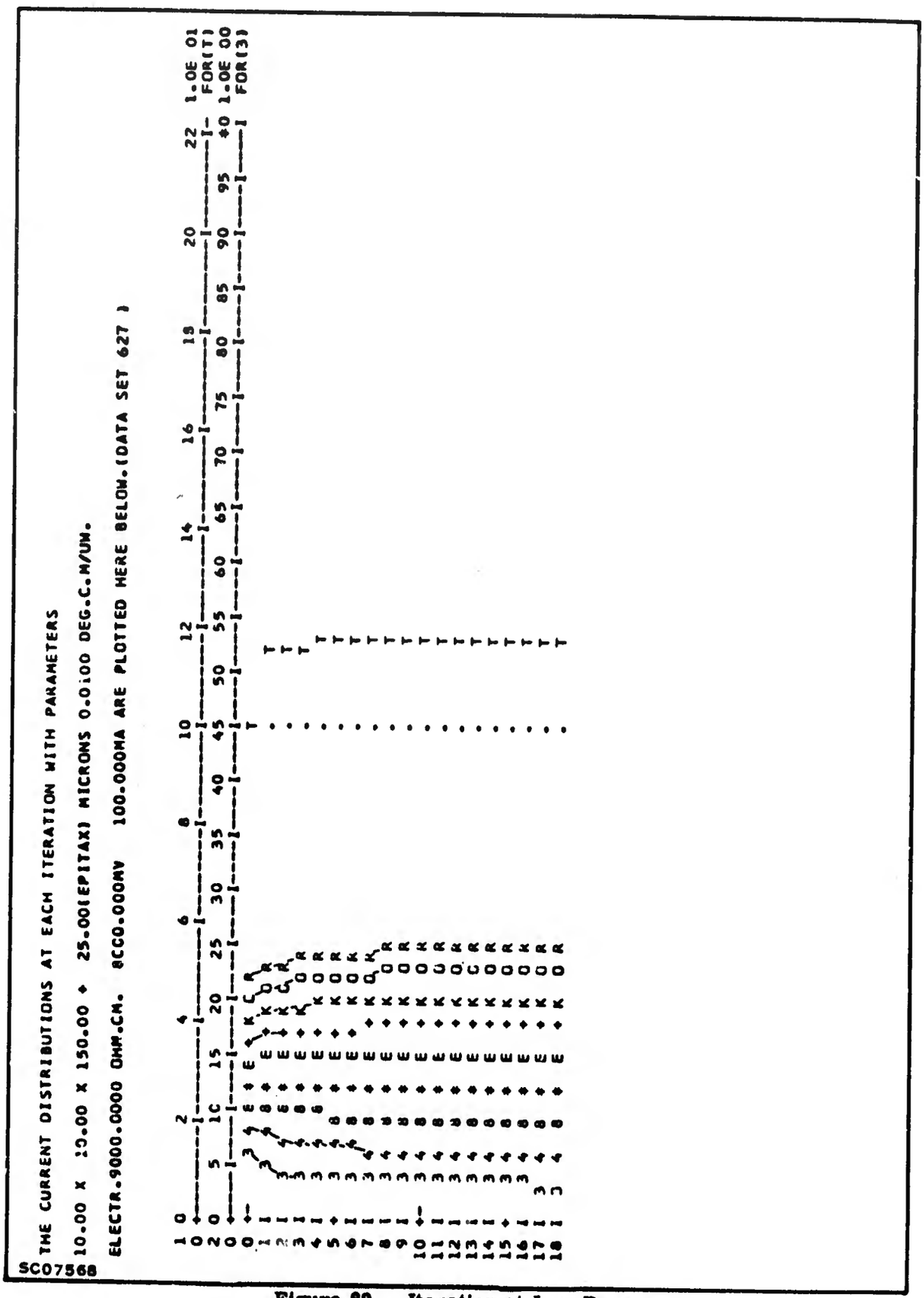

Figure 82. Iteration at Low Power

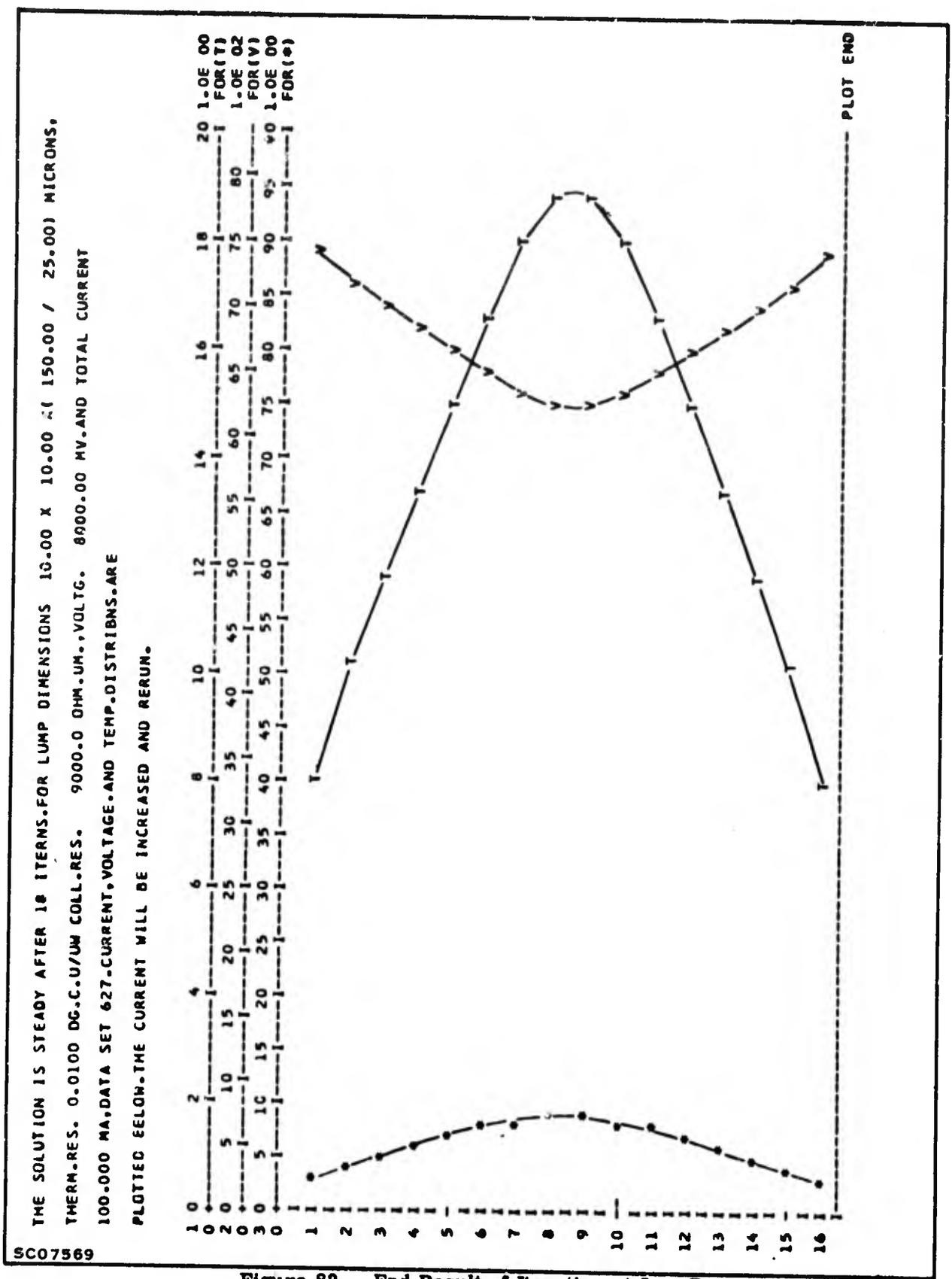

Figure 83. End Result of Iteration at Low Power

(and therefore power) at low voltages is nearly a straight line, and the stable distributions are close to uniform. At higher currents, the non-uniformity increases, and the peak temperature rises more rapidly than the current. The number of iterations needed to reach such a solution is much greater, and the current distribution and temperature profile show pronounced peaks. A typical plot of successive iterations for this type of condition is shown in Figure 84. The behavior is of the type shown in Figure 81d. The final stable distribution is shown in Figure 85. Note that those elements carrying the current are near saturation conditions. A plot of the peak surface temperature rise as a function of total device current for a fixed applied voltage (8 V curve) is shown in Figure 86. As discussed in Section IX-2b, the temperature at a point on the surface of the model corresponds to the temperature rise between the junctions and the case for the device. At higher voltages, the upward turn in the peak temperature of the final distributions begins considerably sooner, and is more pronounced, as shown by the 10 V curve in Figure 86.

At high voltages, the transition from final distributions of the type shown in Figure 83 to one as shown in Figure 85 is not progressive, as it is in the above cases, but is abrupt. A set of plots for an iteration below this abrupt transition is shown in Figures 87 and 88, where it can be seen that they are similar to Figures 82, 83, and 81a. A similar set above this transition, showing strong concentration of the current necessitating element size reduction, and the final stable distribution with a small high-current density region which is fully saturated, is shown in Figures 89 and 90. This development is of the type indicated in Figure 81f. The plot of peak temperature against current for a high voltage case in Figure 86 shows the jump clearly. At still higher voltages, the condition corresponding to Figure 90 is above the validity range of the model, and only the region up to the abrupt transition can be followed.

b. Two Types of Stable Distributions

We may distinguish between two types of stable distributions, those which are relatively uniform (Figures 83, and 88) with small voltage drop in the resistive layer, and those with relatively peaked current flow (Figures 89, and 90) in a region at or near saturation conditions. At low voltages, stable distributions occur which are a combination of both types, but the distinction is useful in discussing the results in terms of basic mechanisms in Section IX-4. By obtaining a set of curves such as those shown in Figure 86 for several voltages, we can define the boundary of the abrupt transition region. This boundary is shown, together with the curves of Figure 86 in Figure 91. Also, on this figure are shown approximate extensions of the upper and lower limits of the abrupt jump into the region where no jump occurs. These lines delineate approximately the boundaries of these two types of stable distributions and the overlap region of intermediate distributions. Constant power lines are also shown on Figure 91. If no current concentration occurred, the temperature rise would be very nearly proportional to power, and a constant power line would be parallel to the current axis. Shown to the right of Figure 91 are the temperature rises that would

Figure 84. Iteration to Concentrated Distribution

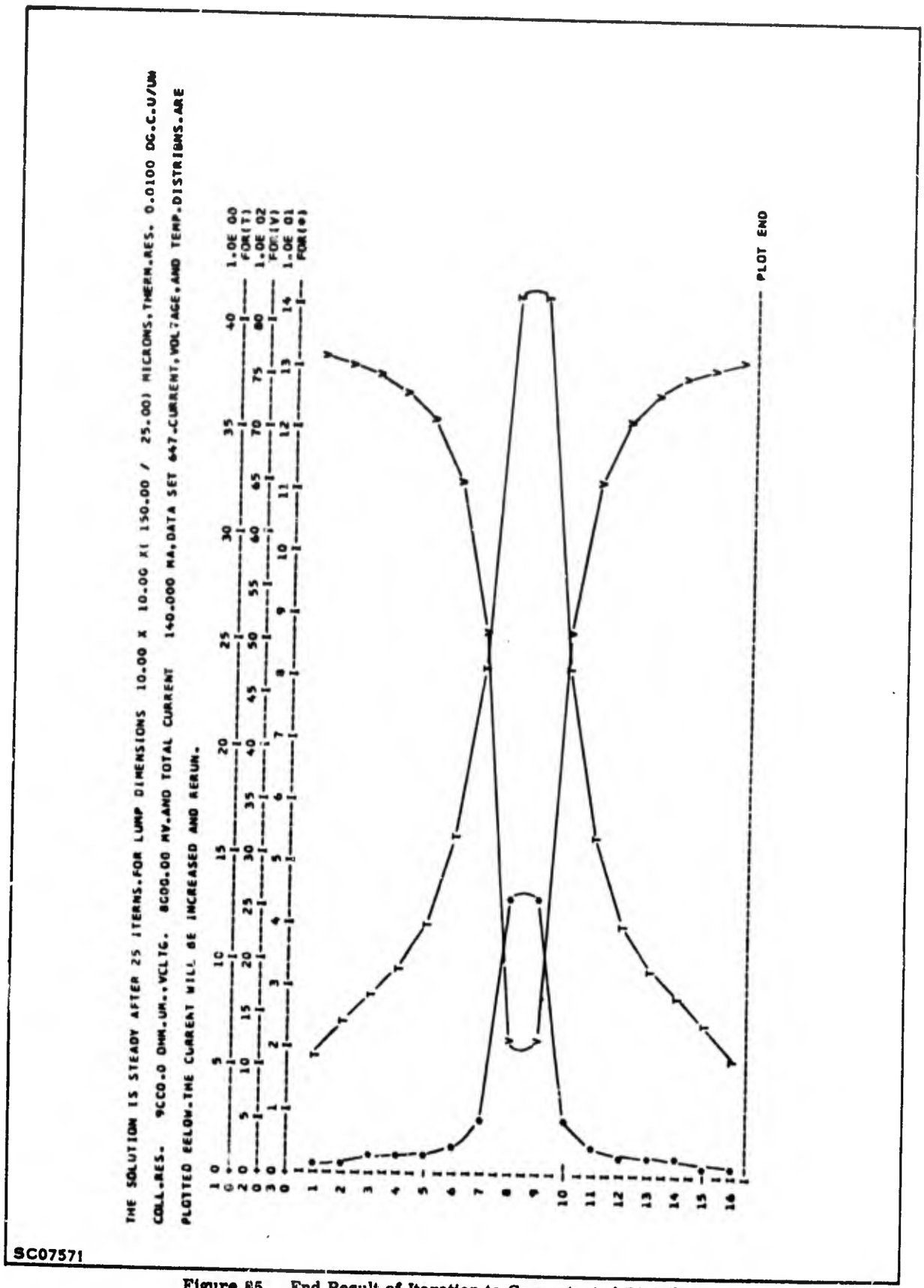

Figure 85. End Result of Iteration to Concentrated Distribution

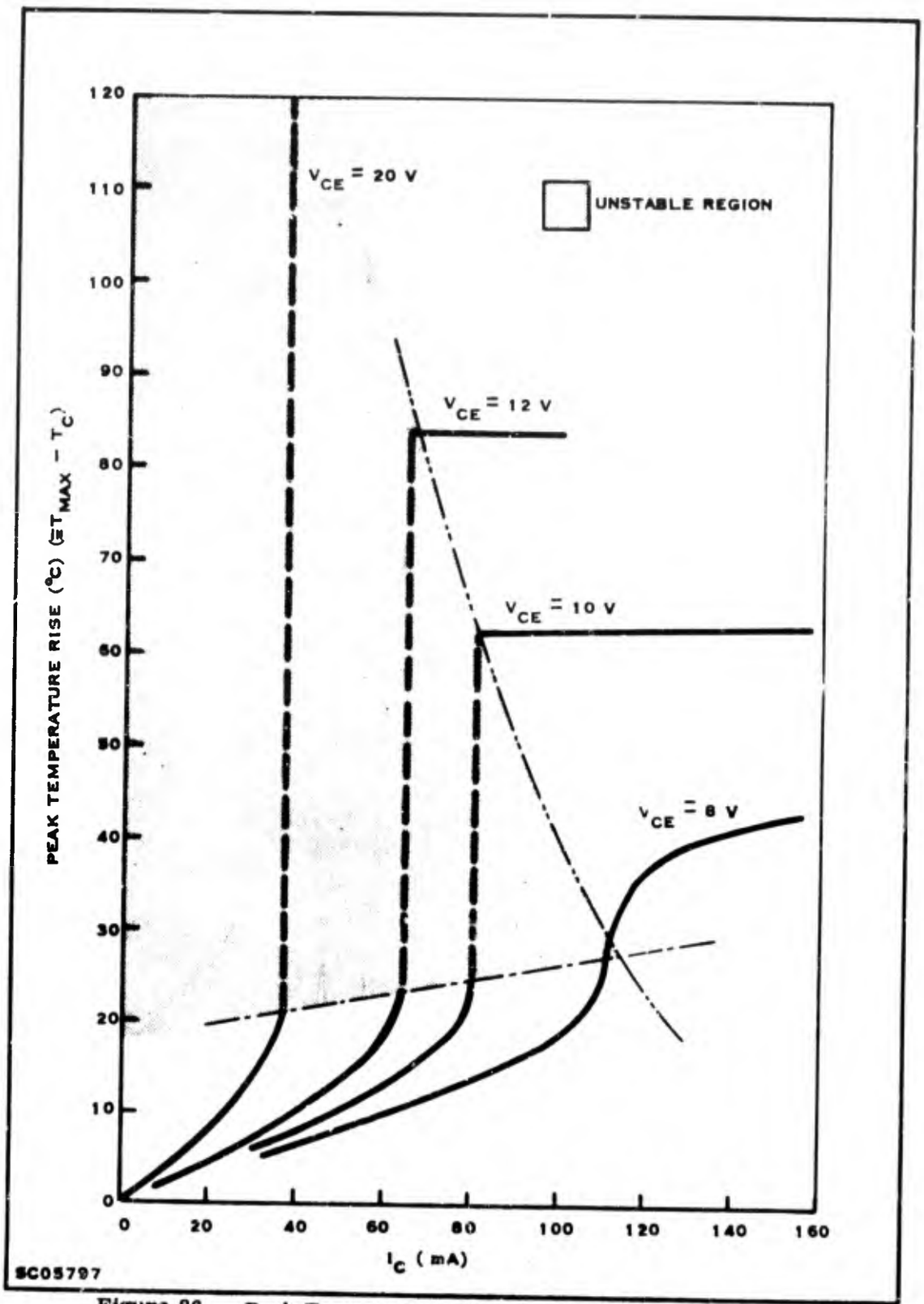

Figure 86. Peak Temperature Rise for Small Area Model

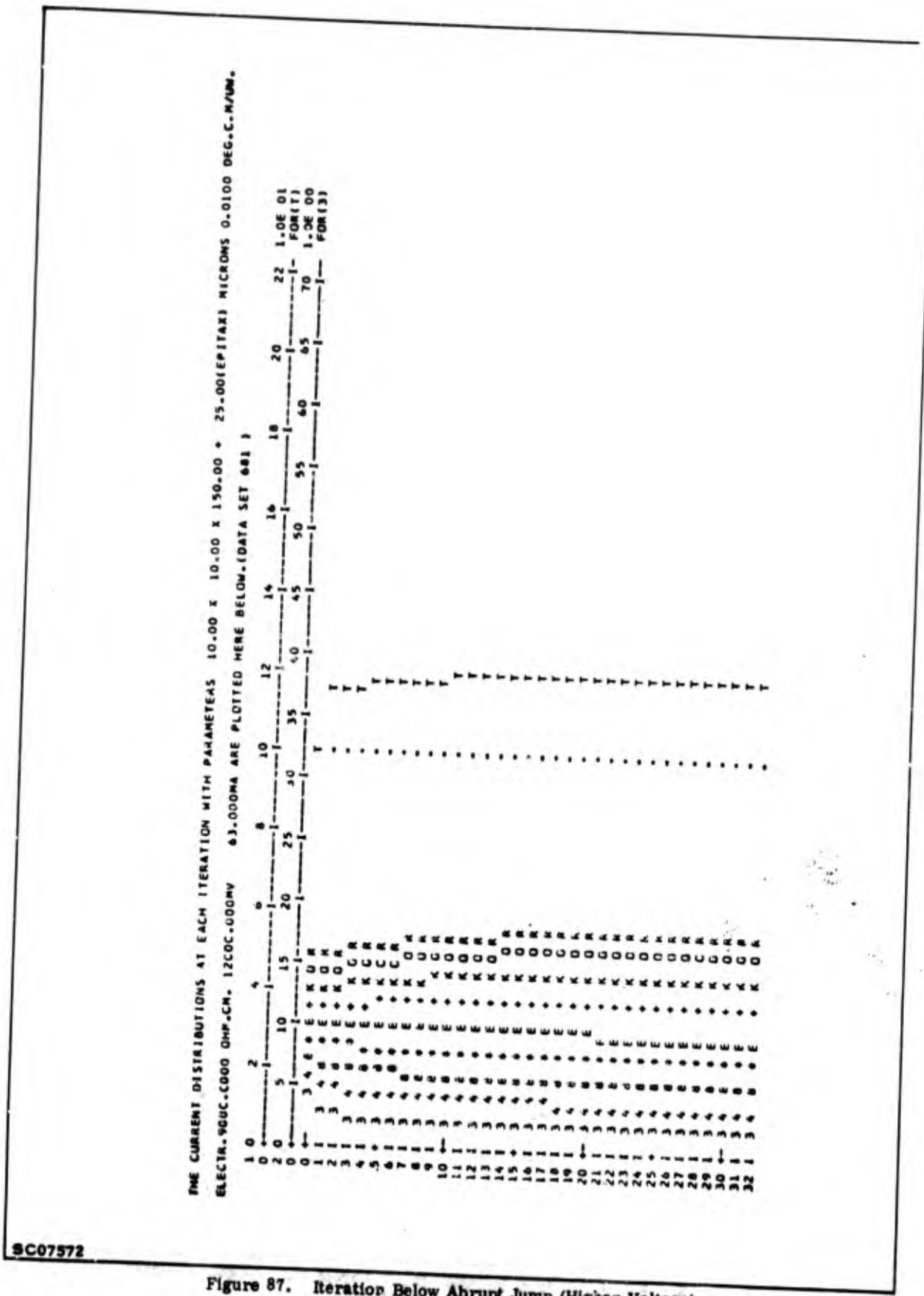

Figure 87. Iteration Below Abrupt Jump (Higher Voltage)

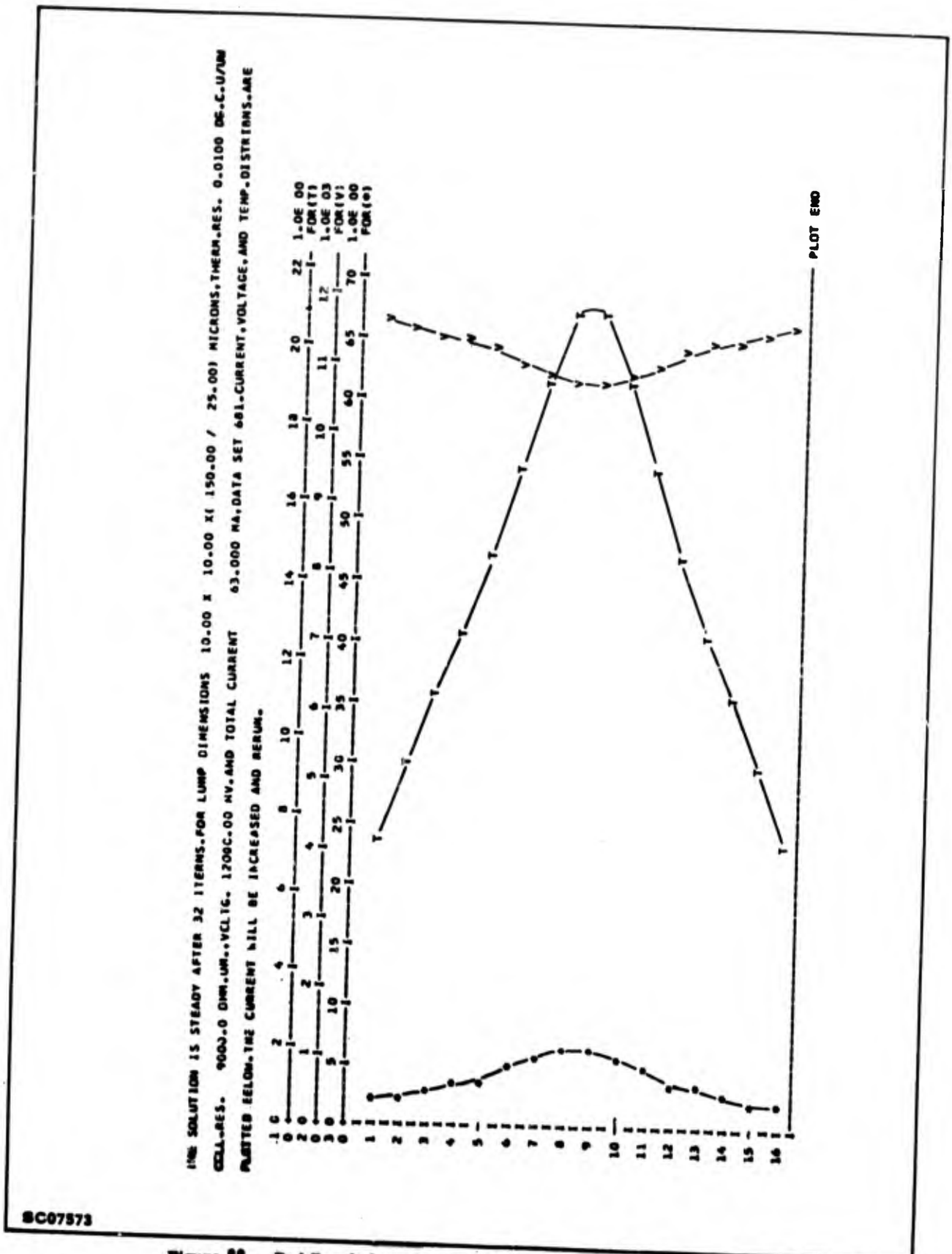

Figure 86. End Result from Reration Below Abrupt Jump (Higher Voltage)

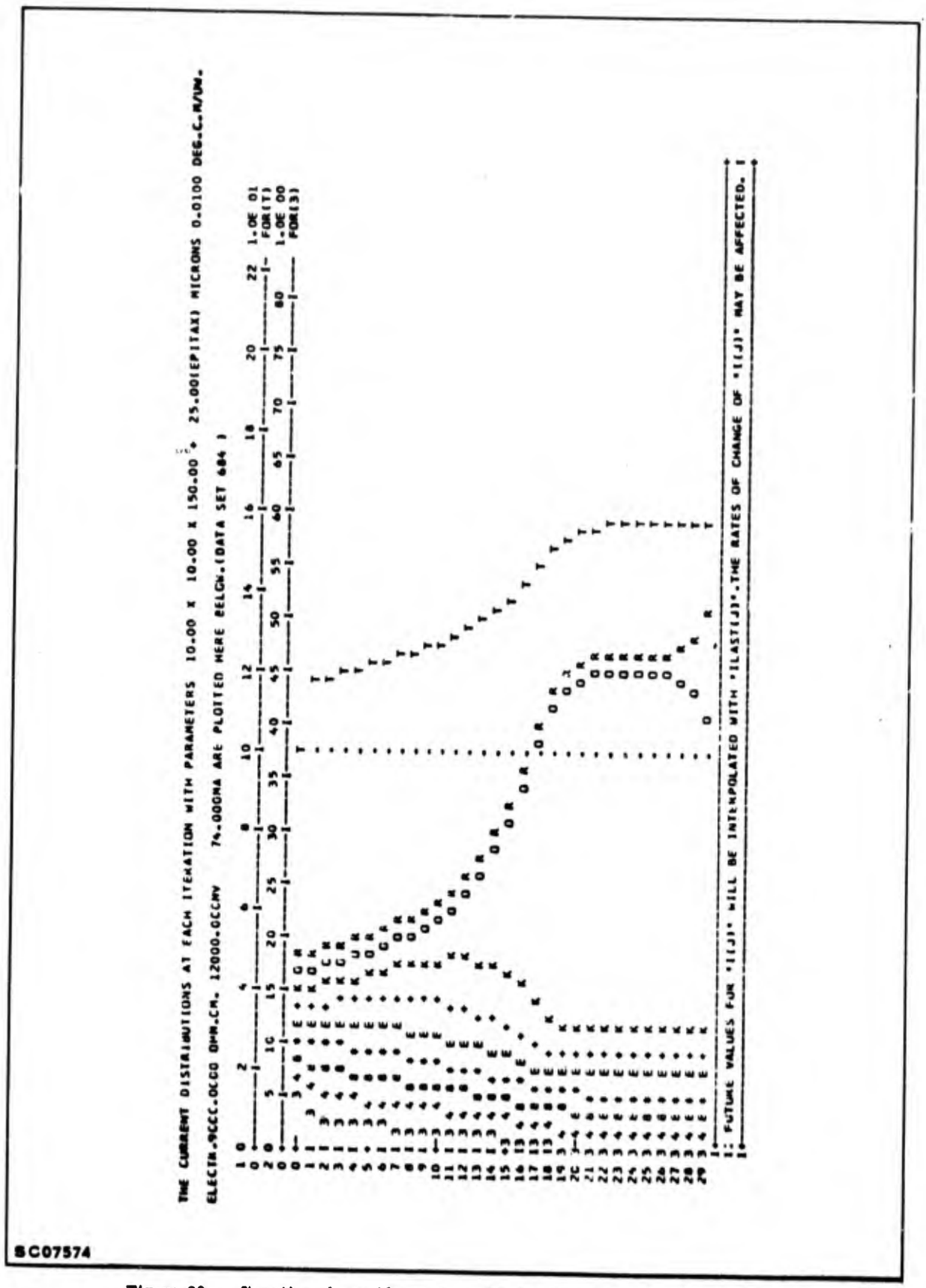

Figure 89. Iteration above Abrupt Jump (Higher Voltage), Sheet 1 of 5

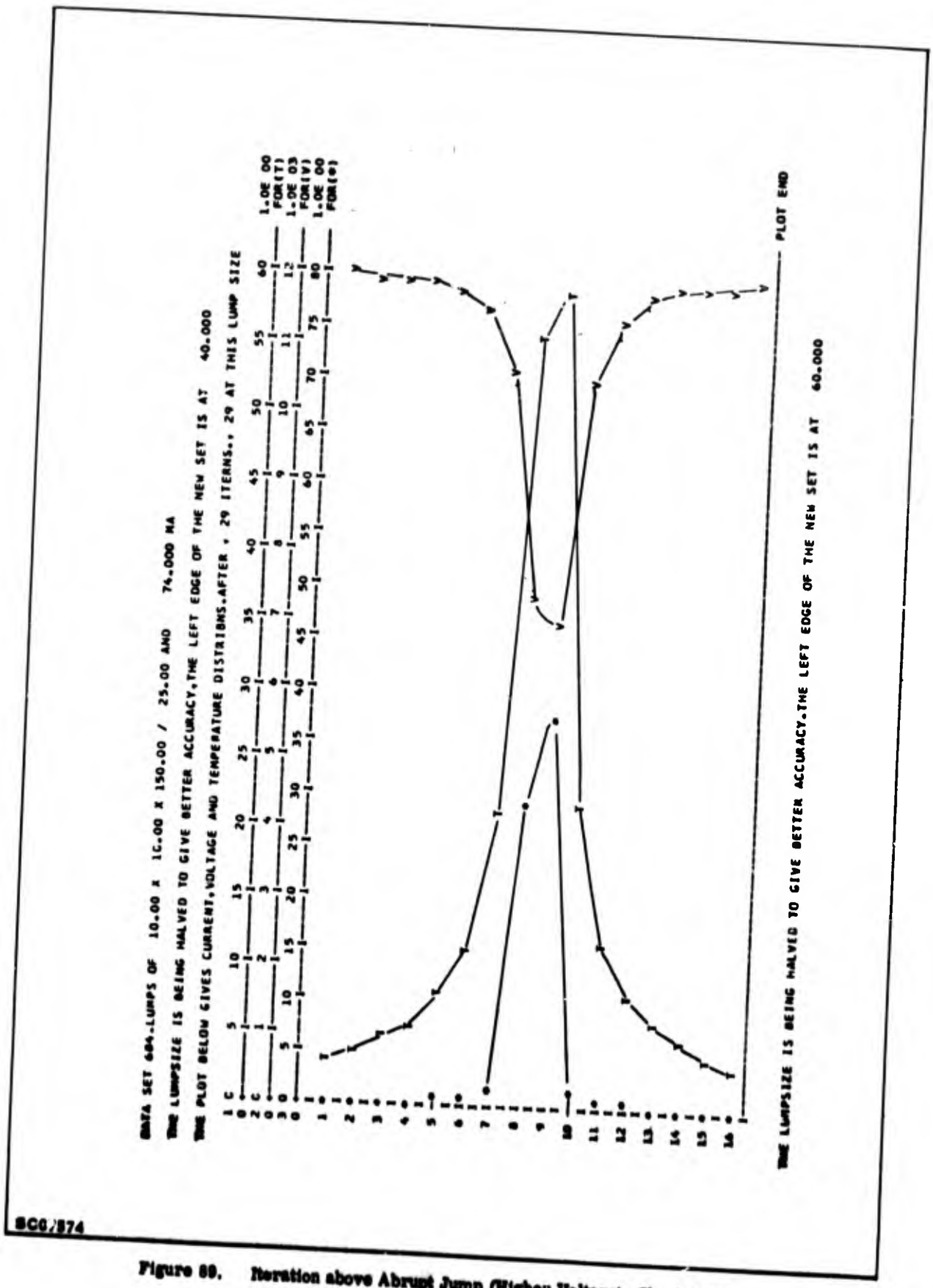

Figure 89. Iteration above Abrupt Jump (Higher Voltage), Sheet 2 of 5

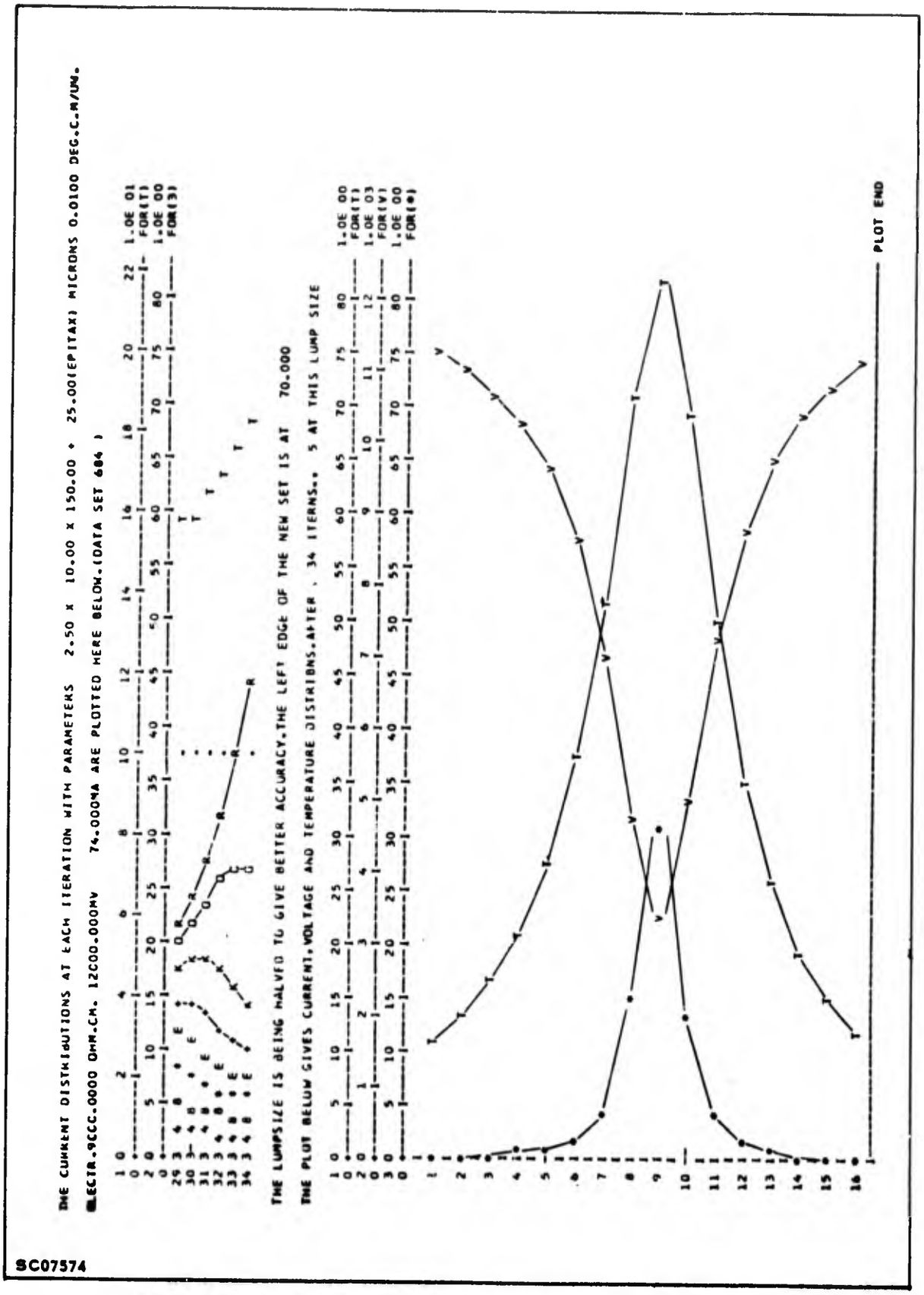

Figure 89. Iteration above Abrupt Jump (Higher Voltage), Sheet 3 of 5

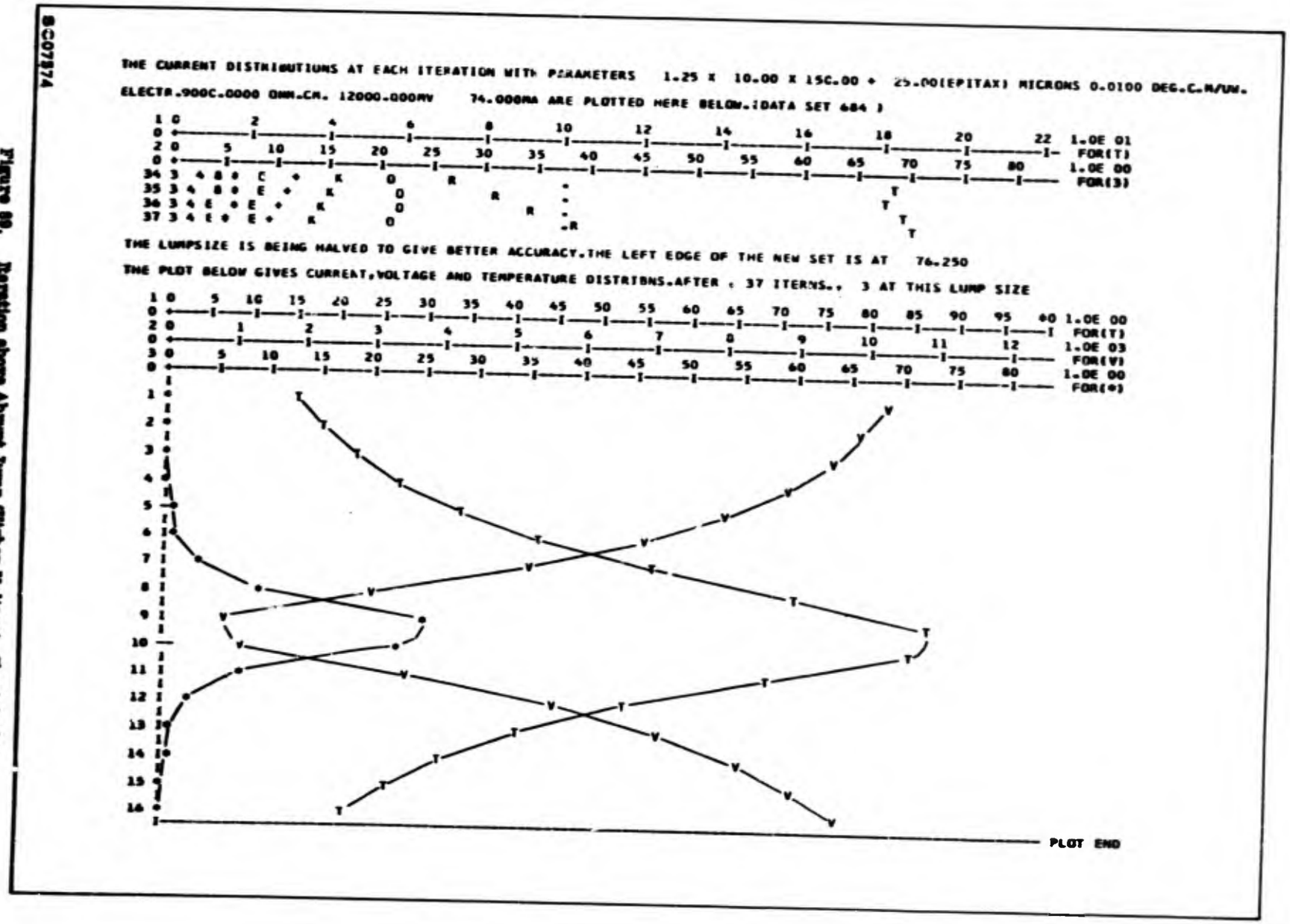

Figure 89. Reaction above Abrupt Jump (Higher Voltage), Sheet 4 of 5

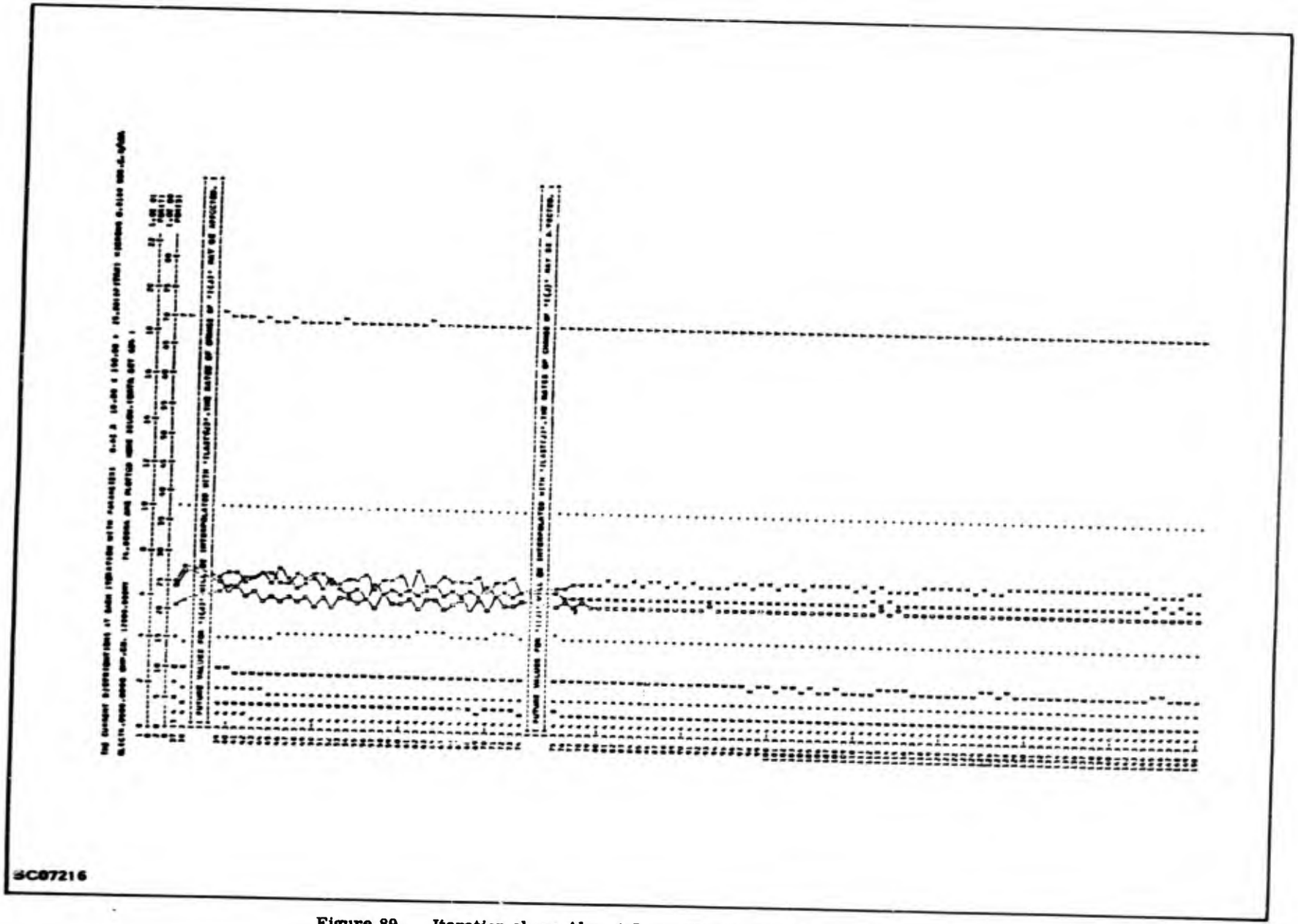

Figure 89. Iteration above Abrupt Jump (Higher Voltage), Sheet 5 of 5

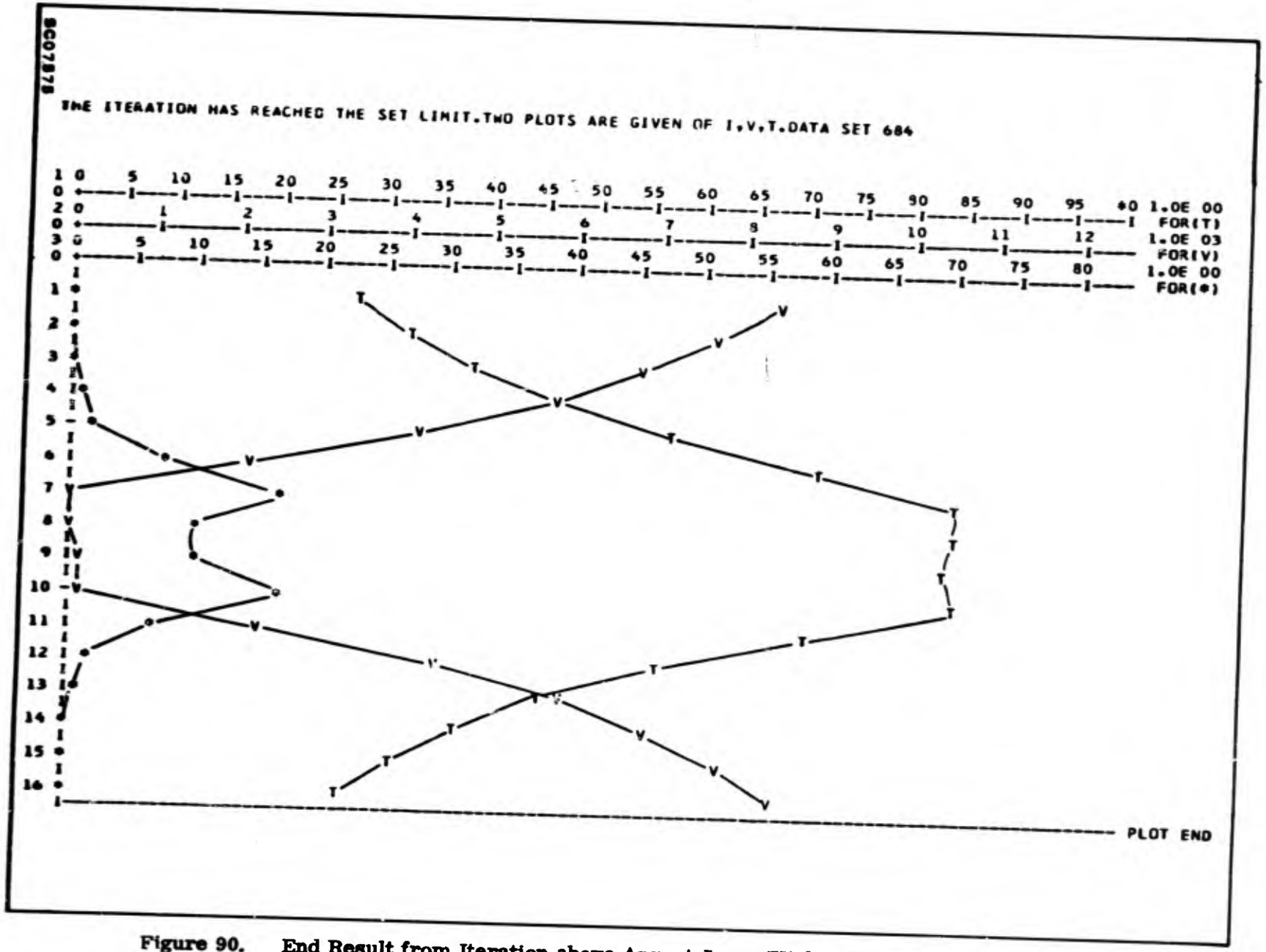

Figure 90. End Result from Iteration above Aprupt Jump (Higher Voltage), Sheet 1 of 2

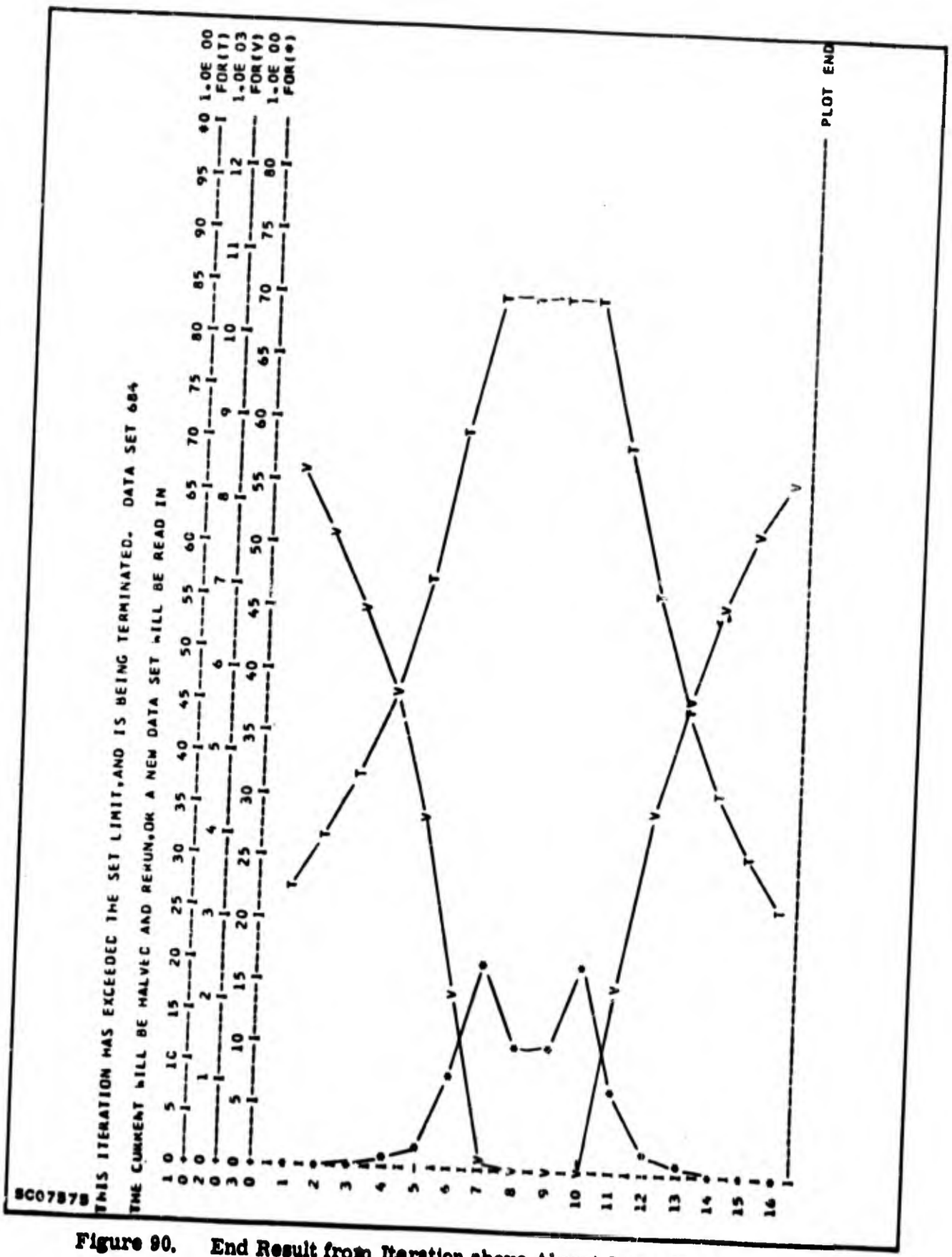

Figure 90. End Result from Iteration above Abrupt Jump (Higher Voltage)
Sheet 2 of 2

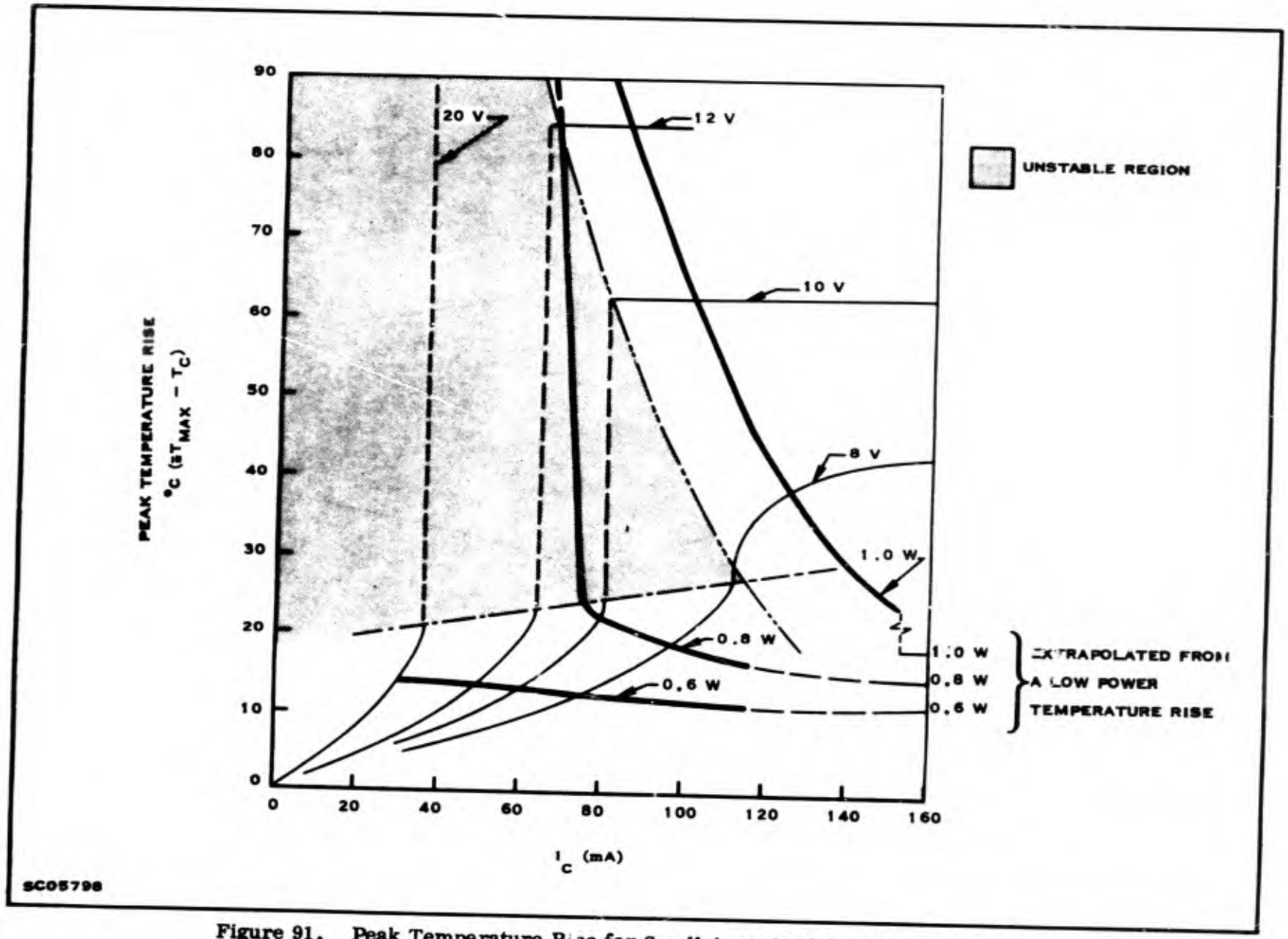

Figure 91. Peak Temperature Rise for Small Area Model with Boundaries of Types of Stable Regions and Constant Power Lines

occur under these conditions extrapolated from temperature rises at low power where the current concentration is negligible. It is interesting to note that the constant power curves approach these extrapolated values at high currents.

c. Relationship to Hot Spots

Stable distributions with a small high current density saturated region operate at a high temperature, which rises rapidly with current increases. The model shows that at high voltages this type of hot spot will form at much lower powers than are needed at low voltages (Figure 91). The hot spot produced in the model would seem to correspond well to the hot spots appearing in actual devices, as discussed in Section VIII of this report, and elsewhere [33, 34, 41]. The size of this hot spot is limited in the model only by the minimum area that will carry the current without the collector-emitter voltage in that area becoming negative. In actual devices, the base resistivity will also tend to limit hot spot size, but at the higher temperatures this limitation will disappear as the collector base leakage currents and the current gain increase, and the base current flow into the hot spot decreases.

d. Agreement with Experimental Results

The qualitative agreement between the lower-voltages plot in Figure 86 and the microradiometer readings in Figure 71 (Section VIII of this report) is quite good. Experimental observations using an infrared microradiometer [43] show the discontinuity in peak temperature versus current at high voltages as in Figure 86. The existence of stable hot spots at temperatures of over 300°C is demonstrated by Figure 66 in Section VIII.

The assumption made in the model that the case temperature does not significantly affect the temperature rise has been found to be justified also. Characteristics of this type taken at case temperatures of from 50°C to 150°C are virtually identical [43]. To assess the quantitative agreement, the model parameters were set up to simulate a 2N3998 device (device A - Figure 1). The limitations of geometry in the present model are such that the simulation can only be approximate, particularly in relation to the heat flow parameters. A cross-section of the device is shown in Figure 92a. The major part of the material affecting the heat flow is the copper stud while the lateral heat conduction in the active area is significantly influenced by the silicon chip and the solders with various thermal conductivities. As the model assumes only one (thermal) layer, it is not immediately obvious whether it would be better to shrink the copper and solder regions in thickness to the "appropriate" silicon thicknesses,

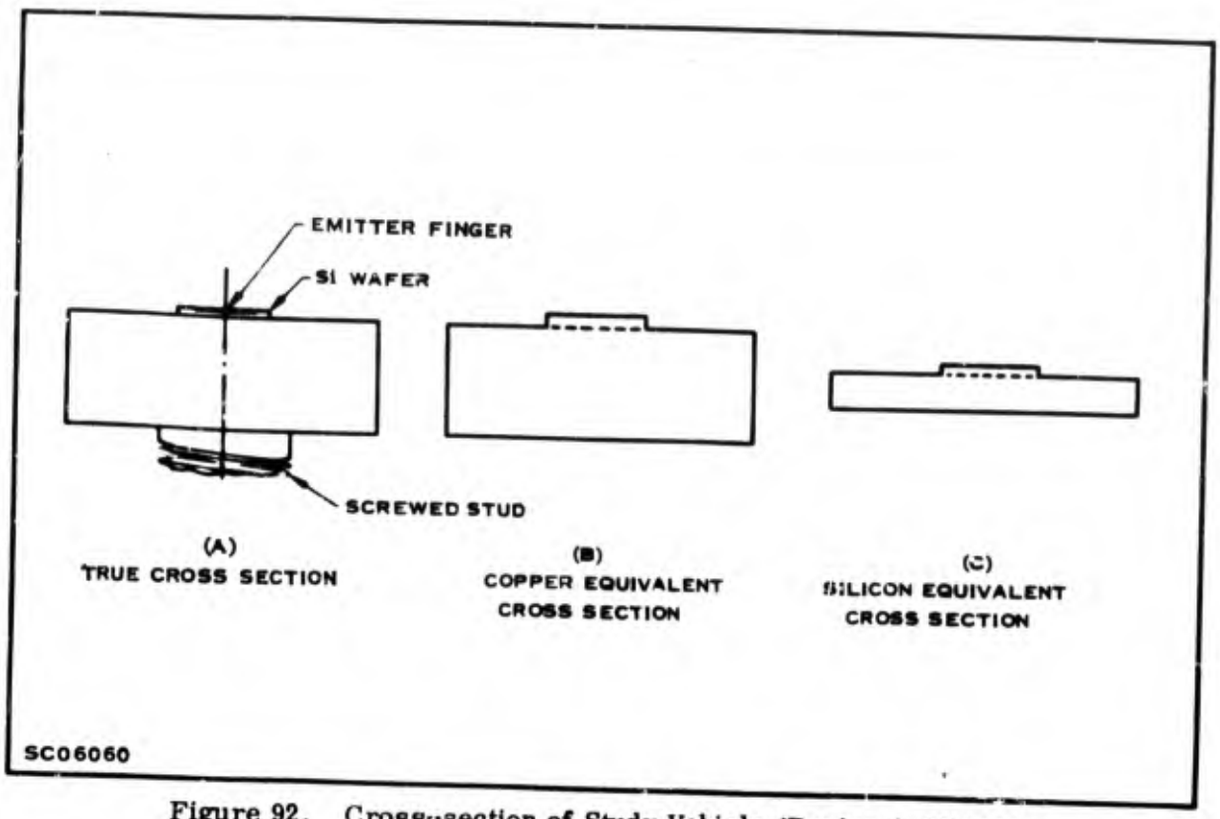

Figure 92. Cross-section of Study Vehicle (Device A-2N3998)

or to expand the silicon to the "equivalent" copper thickness, and treat the material as homogeneous. These two possibilities are illustrated in cross-section in Figures 92b and 92c. A further difficulty arises over the size of cuboid to model. The silicon chip (Figure 1) itself is about 100 mils square, but the stud on which it is mounted is hexagonal and 430 mils across. A rectangle approximating the hexagon, with silicon "equivalent" thickness, and thermal resistance, was found to give reasonable results in comparison with experiment. A peak temperature versus current plot for various voltages for these conditions is given in Figure 93, and gives satisfactory correlation with the infrared microradiometer readings given in Figure 27 and similar data measured at higher voltages.[43] The experimentally determined region of discontinuity[43] is similar to the theoretically predicted region and the curves are of similar shape.

If we assume that the development of a hot spot into thermal breakdown occurs at a temperature that does not depend strongly on the voltage and current conditions, then the area in the voltage current plane in which breakdown occurs should correspond to that area where the temperature exceeds some value. Figure 94 shows a plot taken from Figure 93 of voltage and current conditions not exceeding constant temperatures, and also constant power lines. Measurements on devices have indicated that the incidence of thermal breakdown does indeed fall in such an area.

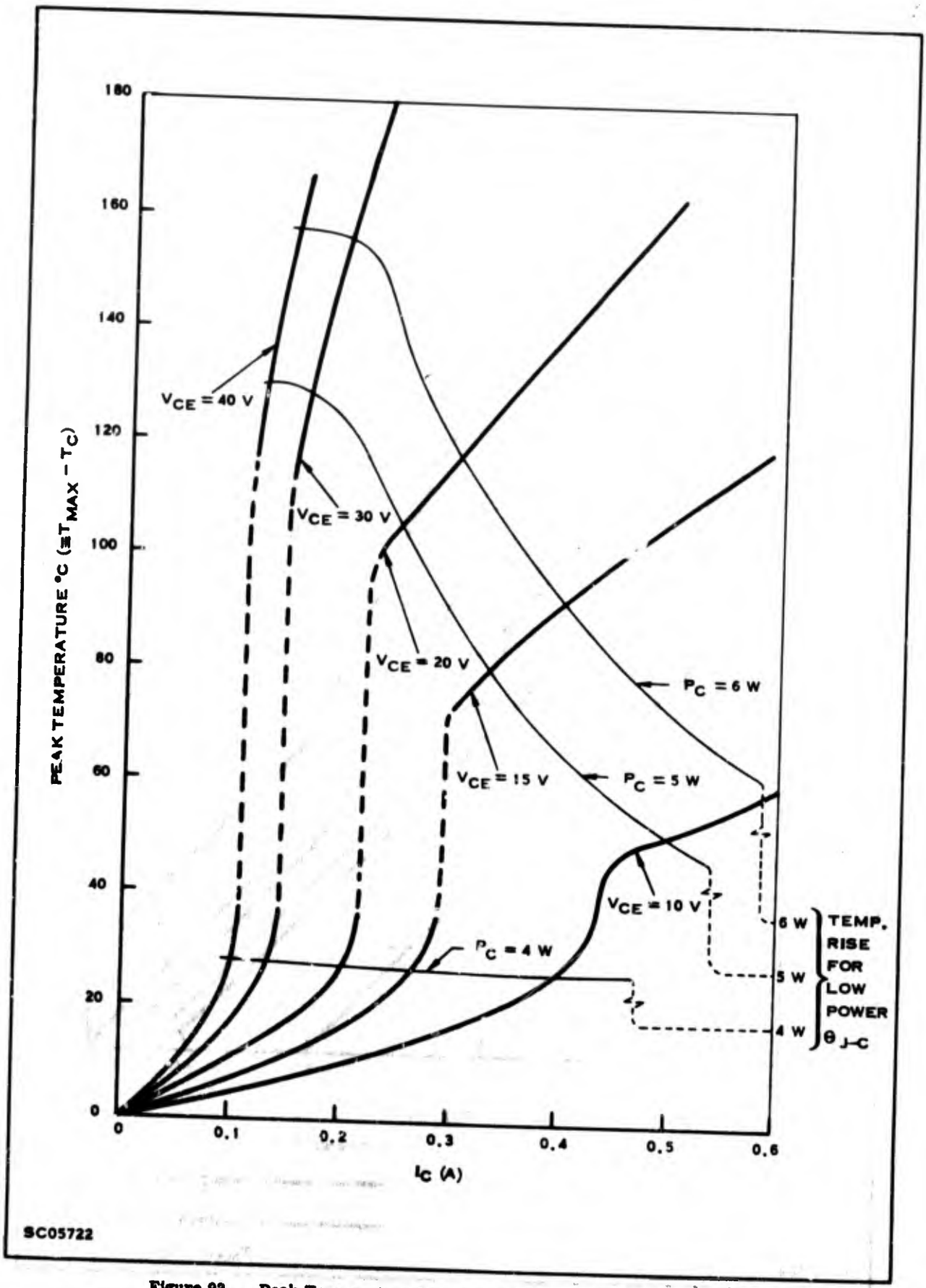

Figure 93. Peak Temperature Rise for Device A (2N3998) Type Model

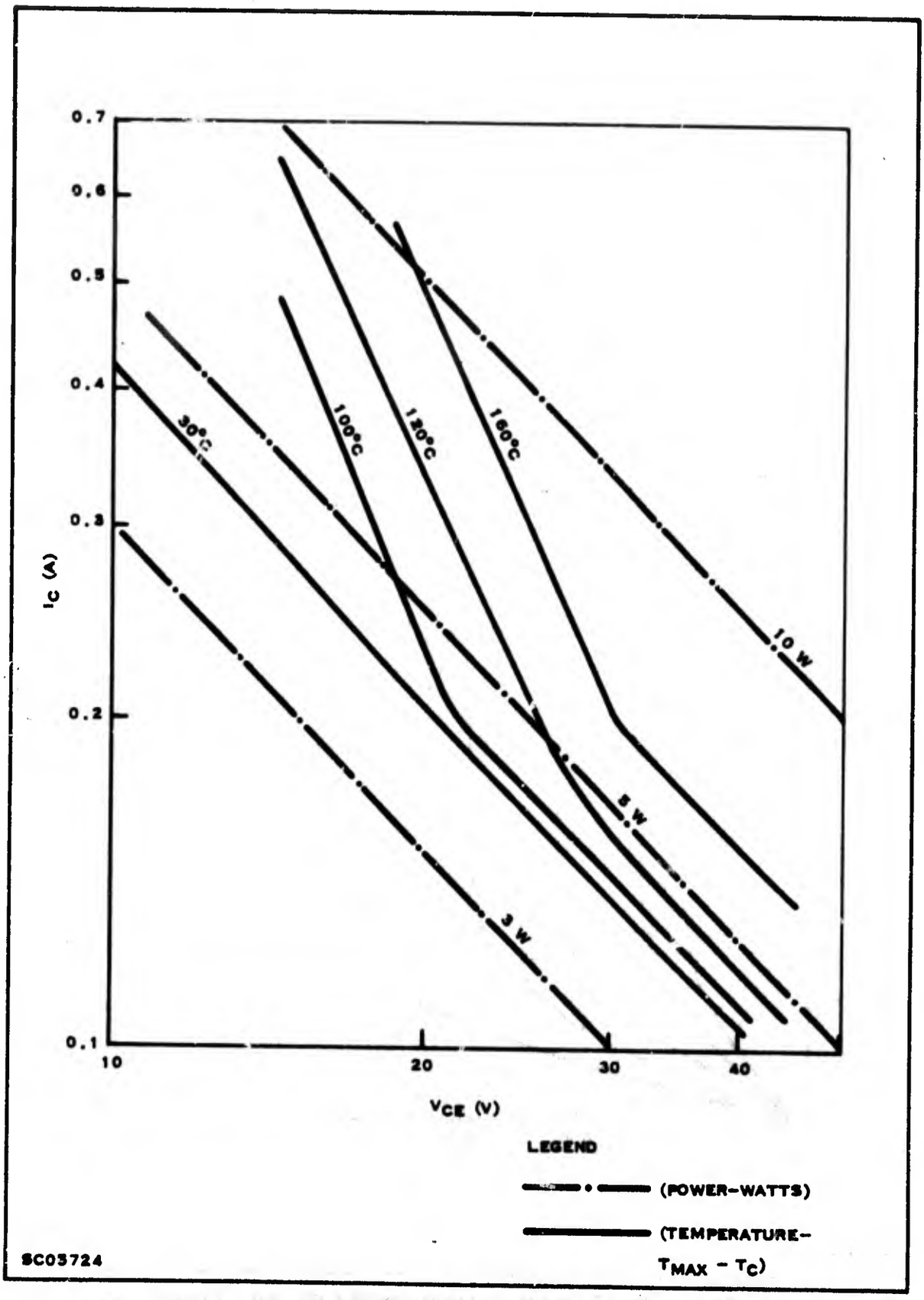

Figure 94. Plot of Current and Voltage Conditions to Give Constant Temperatures for Device A(2N3998) Type Model

4. DISCUSSION

a. Proposed Basic Mechanisms

The mechanisms proposed for thermal breakdown occur in two phases. Phase 1 is essentially that covered by the present study and described by the device model. Phase 2 is somewhat speculative, but is compatible with the available evidence.

Phase 1

This phase is governed by the unstable interaction between the temperature and current distributions at the junction surfaces of the device. This interaction is stronger for greater concentration of current and for higher power levels but is opposed by two groups of stabilizing effects. The first is the lateral heat conduction at the surface of the device. It is most effective, for a given geometry, when the temperature differences are small (Equation 10). This mechanism is independent of the electrical applied conditions and heat sink temperature (except that the thermal conductivities of the materials depend on temperature). It is able to dominate the other influences at low power levels. The second group of stabilizing effects includes the base resistivity, which will tend to debias those areas of the emitter-base junction generating most base current, and the collector resistivity, which will reduce the collector-emitter voltage, the emitter current, and the collector-base junction dissipation in the high-current areas, and spread the remaining dissipation through the collector resistive layer. These are most effective at high current densities, due to the higher voltage drops. The collector resistivity also has more effect at low voltages. Thus they will stabilize the distribution most effectively for more concentrated distributions at higher currents and at lower applied voltages.

The type of relatively uniform stable distribution shown in Figures 83 and 88 is caused by the first stabilizing effect, partly assisted, at low voltage and high current, by the second group of stabilizing effects. This additional stabilization (from the second group) causes the transition from nearly uniform to highly concentrated distributions to occur at higher powers or to be suppressed altogether under low voltage high current conditions. For applied voltage and current levels greater than the limit of this type of stability, the unstable interaction will dominate until the concentration of current causes the second group of stabilizers to take control (assisted by the first group if the peak temperature is moderate). For high current low voltage conditions, the transition may be fairly smooth, and the unstable interaction never dominate the combined stabilizing effects. For many applied conditions, the concentrated type of stability will occur only when most of the hot spot is in saturation, particularly for the higher voltage conditions. Also, for sufficiently high hot-spot temperature, the collector-base leakage current and the increased current gain will reduce the base current requirements for a given device current, reducing this

stabilizing influence. The high temperature limit of Phase 1 is thus a concentrated current distribution where the hot spot is saturated and virtually no base drive is required — indeed, the base current may even be negative. The hot-spot size is limited by the collector resistivity, and we may consider the emitter as being locally short circuited to the collector for all practical purposes while the hot spot remains.

Phase 2

The epitaxial material normally used for power transistors has from 4 to 8×10^{14} donors/cc. A curve of resistivity against temperature for such material is given in Figure 95. [44] The resistivity rises by a factor of about 3 from the room temperature value, but above a temperature of the order of 200°C, the resistivity begins to fall, and at about 300°C is near the room temperature value again. At higher temperatures, the resistivity begins to drop steeply to 1/10 at 400°C, 1/20 at 500°C, and 1/100 at 700°C. Thus, if the hot spot temperature exceeds some value between 300°C and 400°C, the limiting influence of the collector resistivity will decrease and an increase in current concentration will occur. This will further reduce collector resistivity. The current handling capacity is no longer limited by the base drive and will sharply increase, and a considerable drop will occur in the voltage across the device. The high injection level from the emitter may also reduce the effective resistivity of the hot spot region. Increasing the current through the device will increase

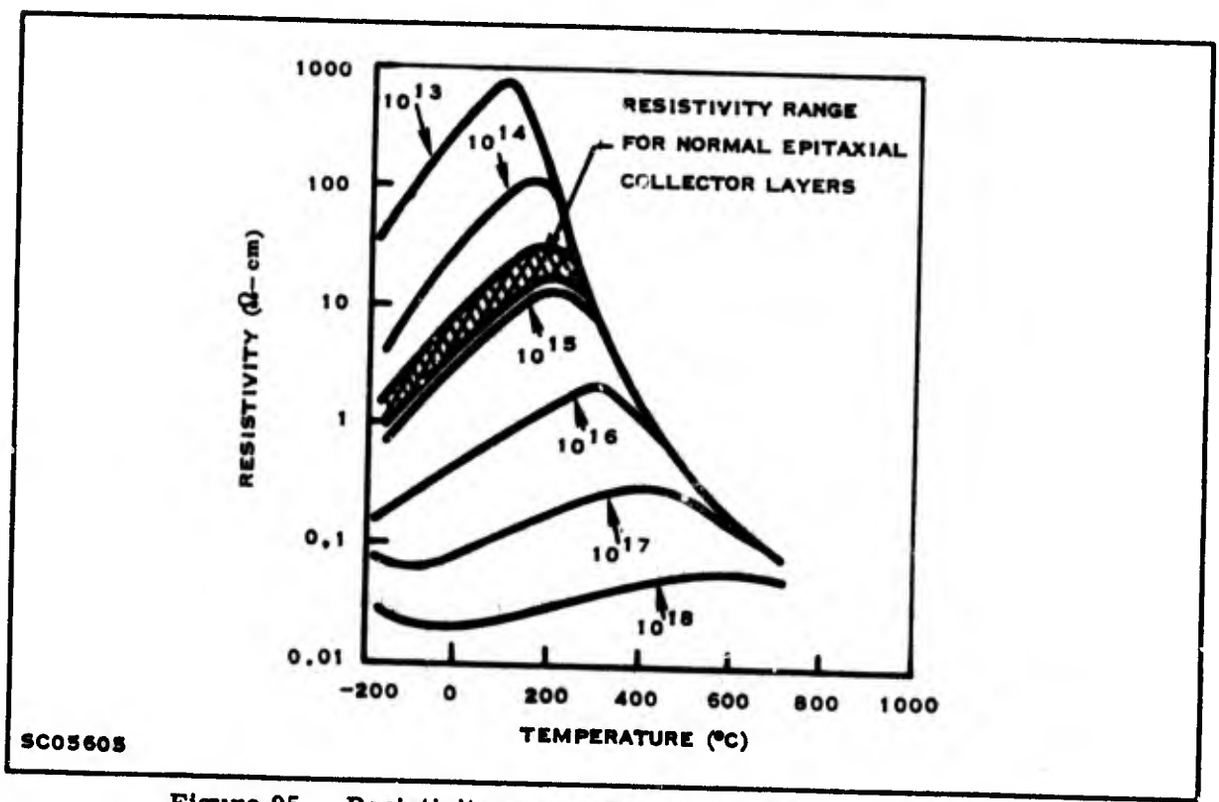

Figure 95. Resistivity versus Temperature for n-type Silicon (Theoretical Curves for Sb-doped Si)

the peak temperature, the hot spot size, and the injection level, and may reduce the resistivity enough that the voltage across the device falls, thus giving the negative resistance characteristics often observed in thermal breakdown. The high temperature and current density may also cause solid state plasma effects.[38] It is probable that under these conditions the peak temperature will rise without inherent limit. The rate of increase will depend upon the thermal capacity of the hot region, which will be small compared to that of the whole device. The normal contact material used for silicon planar transistors is aluminum. If the surface temperature above the hot spot exceeds 577°C,[45] a liquid phase will occur at the silicon-aluminum interface, and dissolve silicon to give the 12% silicon eutectic. For the thicknesses of aluminum layer and emitter diffusion commonly used, the liquid phase will not immediately reach the emitter-base junction and little or no permanent change in device characteristics would result. However, if the applied conditions continue, the thermal gradient in the liquid phase would induce dissolution of silicon at the hotter side and separation of silicon on the cool side, and a consequent migration of the liquid phase toward the hot spot, causing successively an emitter-base short circuit and an emitter-base-collector short circuit. This is illustrated in Figure 96.

The use of a contact material with a higher eutectic temperature (such as molybdenum)[46] would reduce the risk of device degradation, but would not avoid the breakdown itself.[47]

In support of this rather speculative discussion of Phase 2, it has been observed that thermal breakdown can occur without apparent device degradation, and that resistive base-emitter characteristics and related parameter changes occur before complete short circuit. The characterization data in Section IV-4 shows that for units spending controlled time periods in thermal breakdown operation on a number of occasions, short periods are less effective than long periods in causing degradation in a given total time of operation. The discussion suggests that a delay would occur before a liquid phase was formed or reformed, and the migration of the phase would depend on the temperature difference across the phase, and other factors. The longer period

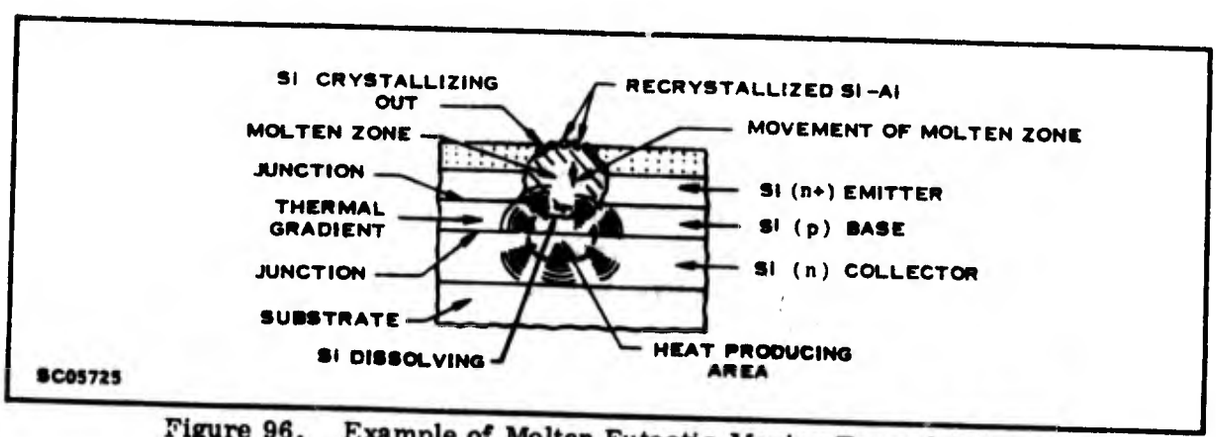

Figure 96. Example of Molten Eutectic Moving Toward Hot Spot

of breakdown would surely give faster migration, and so quicker degradation than shorter periods. The data suggests that the delay is short, and that the increased effectiveness of longer periods is marked.

The mechanism for Phase 2 also explains the similarity between breakdown in n^+nn^+ structures and transistors. These structures must presumably reach the intrinsic temperature in the n region to initiate concentration and the Phase 2 mechanisms. Breakdown in diodes probably occurs in the same way.

b. Relation to Reliability

The results presented above, together with other work in this area,[32,33,40] show that the limit on the operation region of the device set by the onset of thermal breakdown is a function of the thermal-electrical interactions collectively termed Phase 1 above. Device degradation primarily occurs during Phase 2. There are two approaches to the improvement of reliability in this area, related to the two phases.

One approach is to avoid the degradation occurring in Phase 2. As mentioned in Section IX-3b, the use of a molybdenum or similar contact material will prevent severe device damage in cases where it would occur with aluminum contacts.[47] However, it is probable that degradation will not be entirely prevented, since in many circuit environments it may be possible to achieve temperatures of over 1400°C. The resistivity of these contact materials is high and in normal use they may need to be over-coated with gold, which can introduce further problems for power devices. This approach does not avoid circuit malfunction or possible damage to other components, since the breakdown itself will still occur.

The other approach involves strengthening or assisting the stabilizing mechanisms (see Section IX-3a) in the device design, so that the unstable thermal-electrical interactions do not dominate until higher powers (and temperatures) are reached. The thermal breakdown limits on device operation could be effectively removed, avoiding circuit malfunction, degradation of the device itself, and possible damage to other components. Various approaches have been used to implement this, the main effort being directed toward discrete or distributed emitter resistors. By this technique any emitter area increasing its current flow becomes debiased relative to its neighbors, providing an additional stabilizing influence. Considerable improvements in performance can be achieved with only small losses in other device parameters, though there are technological problems associated with the technique.[40] Other possible techniques are the use of a temperature equalizing slab of a good thermal conductor applied to the top of a device, or the use of specially shaped headers, or special device design geometries to equalize temperatures over the active region.

The results of this work suggest that thermal resistance studies and operating life tests should be conducted at high voltages, with correspondingly reduced currents. The most severe operating life test under these conditions may well be at low case temperature and high power, rather than vice versa. These conclusions are in agreement with those from the thermal resistance studies in Section VIII of this report. Screening procedures giving non-destructive tests for voids, and tests for collector resistivity (such as small signal R_{CS} measurements) could remove units with potentially low thermal breakdown resistance.

5. CONCLUSIONS

a. General

A representative model for the thermal-electrical interactions in silicon planar transistors has been developed and shows good correlation with device behavior. The model demonstrates the importance of the resistivity of the collector region in controlling hot spot formation. Two modes of operation of the model have been discussed in terms of these interactions and evidence has been presented to show that they do occur in device operation. The model has assisted in developing a clear description of thermal breakdown in terms of two distinct phases. The first phase is the lateral thermal instability leading to hot spots and the second phase occurs when the hot spot reaches some critical temperature.

b. Possibilities for Further Work

A few possible areas of further study have already been suggested by this section of the report. In addition, the model could be improved by the inclusion of base resistivity, multiple thermal layers, and a more general geometry. More study is needed of the second phase of thermal breakdown (when the hot spot is intrinsic), and of the breakdown mechanisms in diodes, n^+nn^+ structures, and second breakdown. The impact of the interactions discussed in this report on device design needs to be explored, more particularly in designing devices essentially free of thermal breakdown within normal operating power ranges.

SECTION X

PROGRAM CRITIQUE

Work performed under this contract is divided into two parts: (1) a test and data analysis program designed to produce a method for screening or predicting failures in silicon power devices, and (2) a physics of failure program on fundamental degradation. Results, problems, and deficiencies of both programs are presented in this section. In addition, areas pertaining to future work are noted.

One of the major problems inherent in the design of this program was to stress test production devices and simultaneously to do physics of failure studies. To accomplish this, several small special tests (called specials) were conducted to bridge the gap. This provided a means for examining different processes or devices after mutual agreement between RADC and Texas Instruments Incorporated. This flexibility was not possible prior to the introduction of this concept which provided a valuable method of incorporating physics of failure studies into the test program. The results of this approach have been discussed in Section IV under "Evaluation Experiments".

In both the Main and Verification Test Programs it was found that the power operating pretreatment tended to stabilize the device parameters. Fewer devices given power operating pretreatment failed on the power operating tests than devices given other pretreatments. Further study of this stabilization phenomenon is recommended.

In the Verification Test Program the test sample was composed of equal quantities of high and low beta devices. There is some indication that the high beta units are more prone to failure. Further work is needed to study this effect and determine its cause.

Additional work is needed in the area of relating results on reverse bias tests at different temperatures as a function of bias voltage relative to breakdown. That is, do the same failure modes occur at the same rate if a 200 volt breakdown device is stressed at 100 volts (50 percent of breakdown) and a 150 volt device is stressed at 75 volts (50 percent of breakdown)? Similarly the same knowledge is needed for the emitter-base junction.

Another area where additional study is needed involves determination of the device's performance while under stress; that is, the parameter of the device should be

measured while the device is being stressed. These data should be compared with the data of the device when measured at room temperature. Such an approach might decrease the frequency of measurement; certainly it would decrease handling and possibly damage to the device during handling, and may in fact find additional failure modes heretofore masked.

Work needs to be done in the area of developing a power operating test at room ambient (T_A = 25°C) rather than at elevated temperature (T_C = 100°C). If this could be developed, then the capital investment for a supplier of discrete power transistors would be considerably less (by approximately a factor of 10) and still permit compliance with the military specification.

In reviewing the various tests performed during the contract, one sees that some tests did not provide many failures within the time span of the test. A specific example of this is the 2-hr/step reverse bias step stress test in the Main Test Program. In other cases too many failures were obtained by the time the test was concluded. For example, the 350°C temperature storage life test in the Verification Test Program experienced 90 percent failures. However, both situations can be altered by merely changing the failure criteria in the screening procedure. Time constraints in the program did not permit evaluation of failures by changing the failure criteria from those which are described in Section III of this report. Altering the failure criteria will provide a different screening procedure.

Programs of this type, where physics of failure is integrated with the test program, are difficult to implement but in some cases have proven useful. For example, thermal studies play a part in the test program by coupling the study of thermal resistance with infrared and other physics of failure studies. These studies provided a much better insight into the problems encountered in measuring thermal resistance.

The results also pointed out that θ_{J-C} was sensitive to V_{CE} and that θ_{J-C} at 20 volts more nearly reflected the thermal resistance of the device. These results have been incorporated into procedures for measuring θ_{J-C} in the power department. Through this improvement, lots which previously had been failing on life tests exhibit a great frequency of acceptance. This should result in more easily meeting the required goals of shipping schedules and therefore benefit customers such as the Air Force. Although further work needs to be done in the thermal resistance measurement area, it certainly has been made clear that conditions for making thermal-resistance measurement are far more important than perhaps had been recognized, and future specifications should include conditions for and the method of making this measurement.

The computer program SERF developed for this test program was used to isolate the preindicators of failure. It is based on the assumption that devices which are less reliable have at least one parameter whose behavior pattern under stress differs from

that of good devices. The program examines each parameter of each device, and selects that parameter and parameter level which optimize the screening efficiency criterion. This computer program overcame two limitations of the earlier program of Bevington and Ingle:[48] First, screening may be done simultaneously from both the high and low ends of the parameter readings. Second, clustering of many readings in a few cells has been reduced by suitable programming. Another refinement worthy of note is the option in the selection of the screening efficiency criterion.

Two other refinement options, which have not been incorporated, could be of value. One would be an option allowing the user to provide limits on the number of good devices he would allow removed. He might desire, for example, to remove only 10 percent of the good units in screening. This has been done during this contract by examining and selecting from the screening results those screening procedures which satisfy this condition. The other option of merit would be to input the measurement errors associated with the reading of each electrical parameter. Delta and percent changes considered for screening would be compared with the measurement accuracy. If the delta and percent changes were within measurement error, these changes would not be considered for screening.

Costs of screening for the proposed screening procedure developed under this contract do not include all the factors involved. For example, the SERF program as written, considering the ratio of good to bad devices removed, affects screening yields and hence costs.

SERF has been applied to pretreatment (burn-in) data prior to the devices being placed on stress, as well as to data obtained during stress. The prestress data are of value in developing screening procedures and in isolating preindicators of failure to assist in a physics of failure study. Screening during high stress also can be of assistance in defining mechanisms operative at a particular time during high stress. It could be of value also if it were found that screening early during high stress was effective in predicting later failures. A study could be made regarding how soon prediction of later failures was possible after the devices were placed on high stress. Perhaps only a very short exposure to high stress would be needed, not damaging the device. Such an approach is useful as a burn-in on high reliability devices.

It should be emphasized that any [illegible]tion done was "after the fact", that is, devices already known to be failures were examined to determine whether some parameter preindicated failure. This procedure must be verified using a number of samples from different manufacturing lots which are screened, according to the procedure, prior to stress. Results obtained in this manner may be more readily accepted by the various manufacturers.

Nondestructive screening techniques are not the only way of attaining high reliability of devices from a given population. Another way is to develop a high stress lot acceptance test which accelerates in relatively short time those failure modes which are reliability problems peculiar to the device being tested. Each lot would be accepted or rejected on the basis of the sample's performance on the high stress test. Such a technique could provide quick feedback to the device engineer, who in turn could correct any reliability problems exposed by the high stress tests.

SERI can comprehend only one parameter at a time. Therefore this program is not suitable for cases where the simultaneous behavior of two or more parameters must be determined. The programs LINDA 1 and LINDA 2 allow such cases to be considered. These linear discriminant analysis programs result in the construction of a linear combination of parameter values, a linear discriminant function, which may contain as many parameters as desired. A critical value for the linear discriminant function allows the devices to be separated into two categories, satisfactory or unsatisfactory. Parameter values of devices from a population similar to the population used to construct the linear discriminant function are measured, and the parameter values substituted in the linear discriminant function. Those devices which exceed the critical value are placed in the appropriate class, i.e., satisfactory or unsatisfactory.

However, three problems are associated with this approach: (1) First, the analysis assumes that the satisfactory and unsatisfactory devices have the same covariance matrix. Recently some work[49] has appeared which considers linear discriminant analysis without this equal covariance assumption. A computer program, LINDA 2, has been written based on this work. (2) Second problem is that the distribution is assumed to be multivariate normal, a situation which usually does not exist for semiconductor device data. Transforming the distribution into a multivariate normal distribution can be impractical. There is some indication, however, based on very limited results obtained during this contract, that the probability of misclassification is not too sensitive to the non-normality of the underlying distribution. Much more work along these lines, simulating various non-normal distributions and studying the resulting probabilities of misclassification, could contribute substantially to development of screening procedures. (3) The third problem is in selection of parameters to be included in the linear discriminant function. Recently statistical research [50] has been done which provides some simple statistical tests indicating what the contribution of each parameter would be to the discriminant function prior to constructing the function.

Two advantages of using computer programs based on linear discriminant analysis such as LINDA are worth mentioning. The first, mentioned previously, is that of dividing the devices into two categories, satisfactory and unsatisfactory;

actually a large number of categories may be constructed. For example, devices could be divided into three categories: those failing early; those with normal failure times, and those which fail later. Second, the ratio of the cost of misclassification i.e., cost of classifying a satisfactory device as unsatisfactory or vice versa can be actually used as input data for LINDA 1, the basic linear discriminant analysis computer program, in determining the classification criterion.

Surface studies performed under this contract were a major portion of the physics of failure program. These studies were concentrated on the study of stable metal oxide silicon (MOS) systems rather than on specific failure mechanisms. Future studies after stable MOS is achieved would have concerned the controlled addition of impurities to the oxide in an attempt to reproduce some of the more commonly occurring failure mechanisms observed in bipolar devices. Although a stable MOS was achieved, there was not time to pursue the addition of impurity experiments. The specific critique for surface studies is included in the other volume of this final report (RADC TR66-776). Need for such studies was pointed out again in the analysis of degradation failures; many of these failed due to surface effects usually attributed to impurities in or on the oxide. Future work might include the study of the effects on reliability of transistors fabricated with specific impurities added to the oxide, using as control a device fabricated with the stable or "clean" oxide.

Studies of 1/f noise as a possible predictor of failure showed negative results. 49/ However, this was a limited approach, and further work under other bias conditions may prove useful. Studies on the relationships between 1/f noise amplitude distributions and failures are recommended.

Thermal studies extended the knowledge of thermal behavior in transistors under dc operation. Thermal characteristics were determined from infrared microradiometric (IR) temperature measurements on the device surface. This characterization has led to an increased understanding of thermal failure mechanisms and conditions necessary for improving reliability screening tests. With this understanding of the basic dc operation of power transistors, meaningful studies of transient operation now can be conducted to determine the influence of such variables as duty cycle, repetition rate, and thermal time constant in pulse or switching operations. Although no new knowledge concerning failure mechanisms is expected to result from such studies, the work is necessary to define additional thermal limitations for such transient operation. The utility of these studies in reliability screening has been shown to be severely limited by inaccurate and unreliable thermal impedance data obtained from present electrical methods of measuring junction temperature. Most failure mechanisms are temperature dependent and since wide valuations in thermal resistance are encountered a thermal resistance value should be identified with each individual device for most test programs. An accurate economical method for measuring thermal impedance must be developed which can be implemented reliably in large volume screening applications. This situation clearly explains the difficulty of reducing failure rates utilizing thermal impedance

screening. It is hoped that the results of this work will sufficiently illustrate this critical limitation on reliability screening and thereby provide the impetus to develop a satisfactory method of measuring thermal impedance.

One area for future work, which is a continuation of some work under this contract, includes thermal studies coupled with a test program. That is, thermal studies should be conducted on several different device families with the idea in mind of determining a common parameter T_{J-MAX} over the full test range where this common parameter should be used. Once this has been established, a test program should be conducted to prove the validity of the approach. The work done in this contract indicates that such an approach is feasible and well within the present technology.

In the second breakdown study a model was developed for the device behavior which causes hot spot formation and thermal instability. This model shows good correlation to actual measurements on devices. The variety of geometries which can be treated by the present model can be increased by a relatively simple extension of the method to an arbitrary two-dimensional array of active elements which will allow other geometries to be considered.

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APPENDIX A

POWER OPERATING LIFE TEST FACILITY DESCRIPTION

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POWER OPERATING LIFE TEST FACILITY DESCRIPTION

1. INTRODUCTION

The operating life tests were conducted on a universal transistor life test facility. The universal design concept was employed to provide a flexible collector current operating range allowing all life tests to be conducted on one facility. The facility was used exclusively for testing RADC devices for the duration of the contract.

The facility consists of three basic modules: a heat sink system to provide precision temperature control, a stable dc power source and transistorized current regulator modules which maintain a constant power in the test transistor by compensating for variations occurring after bias conditions are established.

2. DISCUSSION OF BASIC MODULES

a. Heat Sink System

The heat sink is a recirculating water cooled system designed to maintain the case temperature of operating transistors within ±5° C of a pre-set temperature. It is capable of regulating a transistor power dissipation load of 10 kW with a heat sink temperature range continuously adjustable from 20° C to 100° C. As illustrated in Figure A-1, the system consists of an aluminum heat sink with extruded parallel tubes which provide an even water flow distribution over the entire mounting surface. A small copper plate, fabricated to accept the test unit, attaches to the parallel tubes to provide a flat mounting surface. A water pump, capable of 60 gallons per minute flow rate, produces the necessary pressure for closed system operation. Constant heat sink temperature is maintained by regulating the temperature of the recirculating water. An adjustable thermostat, mounted in the water flow path, activates an electronic valve which allows chilled water into the system when the water temperature reaches the programmed temperature. If the power dissipation of the operating load is not sufficient to heat the system to the programmed temperature, an immersion heater automatically activates and supplies additional heat until the pre-set temperature is attained.

An over-temperature control, mounted in the water flow, is manually set to disconnect the bias power supplies should temperature increase 5° C above the pre-

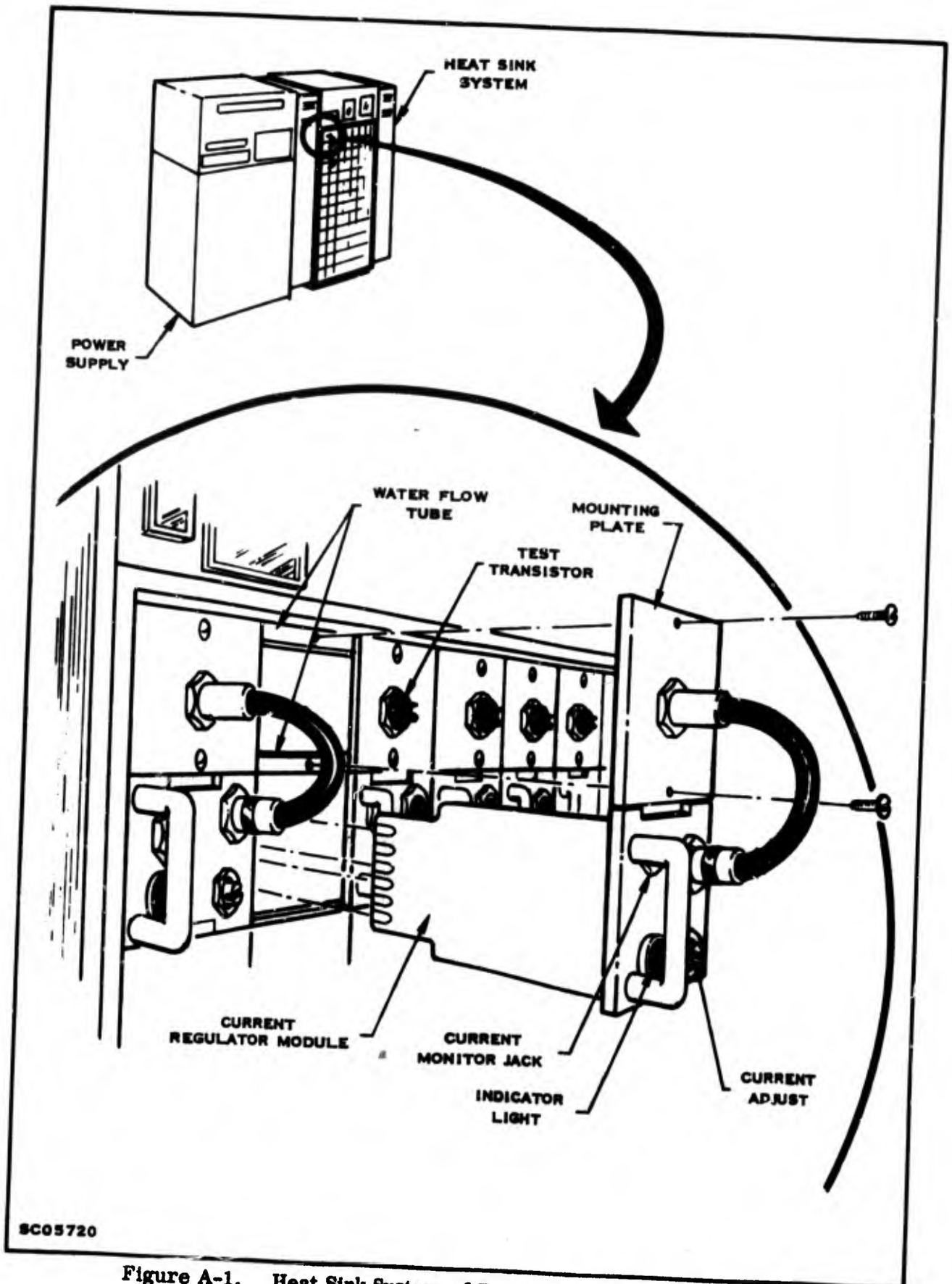

Figure A-1. Heat Sink System of Power Transistor Test Facility

set condition. The thermal resistance from the case of the operating transistor to the water is held to 0.2° C/W by mounting each transistor to the heat sink plate, using a socket wrench set at 8 inch-pounds of torque. A constant water temperature and controlled case to water thermal resistance ensure a constant case temperature (T_C) of the operating units.

b. Power Source

The power source consists of a 0 to 50 V, 500 A power supply for collector bias and a 40 V, 10 A current regulator supply. Voltage regulation, output ripple and transient response of each supply were elevated prior to testing to ensure that the operating units would receive the stress as specified by the test conditions.

c. Current Regulators

The function of the current regulator is to maintain the operating transistors at a constant power dissipation. The circuit will hold emitter current constant to within 5 percent of a set current and compensate for h_{FE} changes in the device or 20 percent changes in the power supply voltages.

As shown in Figure A-2, the regulator is a common emitter configuration. Constant current operation is accomplished by using a differential amplifier to compare the emitter current with a standard voltage reference. Should the emitter current attempt to increase, the voltage across the 0.5 Ω emitter resistor would increase, resulting in an unbalance of the differential amplifier. The error is fed by the differential amplifier to a dc amplifier which decreases the base drive current of the test unit until the differential reaches a balanced condition. A reverse action would result should the emitter current attempt to decrease. The total gain of the feedback circuit is greater than 1000.

An electronic switch is employed in the emitter circuit to protect the test circuit should a mounting error or thermal runaway occur. The switch consists of a saturated transistor with an SCR shunting the base-emitter circuit. When the emitter current reaches 5.5 A, the SCR fires, turning off the series transistor which removes all bias from the operating unit. The circuit is re-set by turning the current adjustment pot counterclockwise. A 6 A fuse is in series with the emitter for protection should the electronic switch fail to function properly. An incandescent lamp is in parallel with the switch and illuminates when the switch turns off indicating a defective test unit or circuit malfunction.

The control circuit is packaged on a printed circuit board and mounts in the heat sink near the operating unit as shown in Figure A-1. The current adjustment pot, indicator lamp, and current and voltage monitoring jack are accessible from the

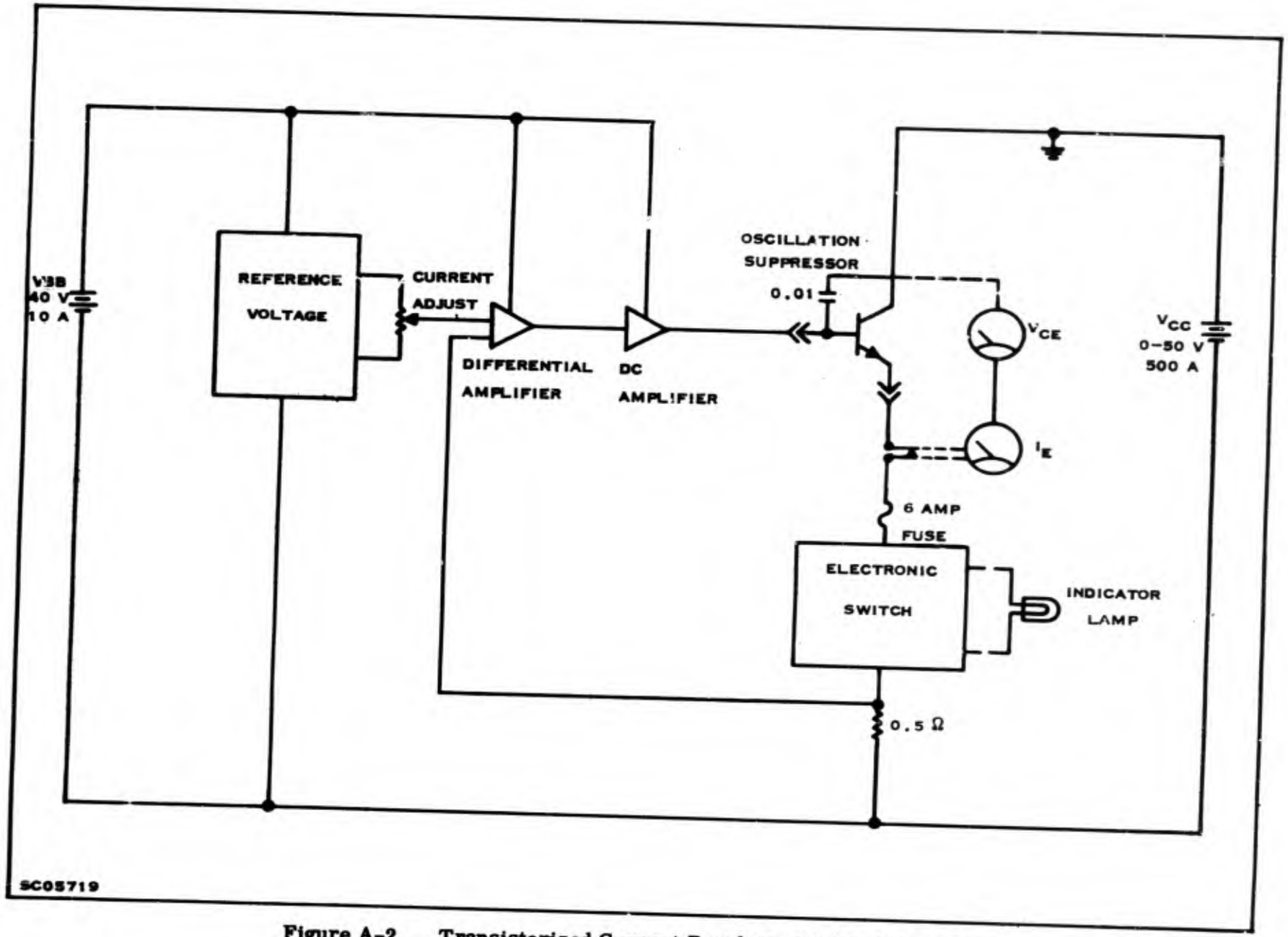

Figure A-2. Transistorized Current Regulator Module Schematic for Power Transistor Test Facility

front. The circuit is connected to the test unit with a telephone jack wired to a socket which accepts the test unit terminals.

3. TEST PROCEDURE

A step-by-step procedure is followed when placing units on the test rack. Silicone grease is applied to the heat sink surface and each unit is mounted with a socket wrench set at 8 inch-pounds of stud torque pressure. The current adjust controls on each current regulator module are turned counterclockwise. This opens the electronic switch and protects all test units should a set-up error occur. The power supply voltages are adjusted to the specified conditions and overvoltage and overtemperature trip points are set. An external test box, which plugs into the current regulator module, is used to adjust the proper emitter current and monitor the collector to emitter voltage (V_{CE}). The emitter current (I_C) is increased from zero to the specified value on each individual test transistor. This procedure is repeated each time the units are placed on the operating facility.

APPENDIX B

METHODS OF MEASURING THERMAL IMPEDANCE

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METHODS OF MEASURING THERMAL IMPEDANCE

The five methods for determining thermal impedance used in this contract work are described in this appendix. Four of the methods use some temperature dependent electrical parameter of the transistor in order to determine the junction temperature. The fifth method measures temperature directly using an infrared microradiometer.

1. PULSE SAMPLING V_{BE} AND V_{CBF} METHODS

The V_{BE} method uses the forward voltage drop of the emitter base diode as the temperature sensitive parameter and the V_{CBF} method uses the forward voltage drop of the collector base diode. These methods use a heating power pulse which is on for 99.97% of the cycle. During the remaining portion of the cycle when the power is off, a small forward bias current pulse is applied through the emitter base junction and the forward voltage drop is measured as illustrated in Figure B-1. The time of measurement must be short compared to the thermal time constant of the device being measured.

This method uses a constant junction temperature approach. The calibration for each device is determined by elevating the case or ambient temperature to some high temperature value such that T_J does not exceed the maximum temperature rating. Then the value of V_{BE} or V_{CBF} is measured with the heating power turned off. The case or ambient temperature is reduced to a lower temperature, T_C, and the power, $V_{CE}I_C$, is applied to heat the transistor by increasing the heating power pulses until the same value of V_{BE} is measured as previously measured. The thermal impedance, θ_{J-C}, is then computed as

$$\theta_{J-C} = \frac{T_J - T_C}{V_{CE}I_C}$$

2. POWER PULSED ZOT (ΔV_{CBF} METHOD)

The ZOT (ΔV_{CBF}) method uses the forward voltage drop of the collector base diode as the temperature sensitive parameter. This method is designed to measure the change in V_{CBF} due to the temperature change of the junction resulting from an applied power pulse. The power pulse is set by current magnitude, voltage magnitude,

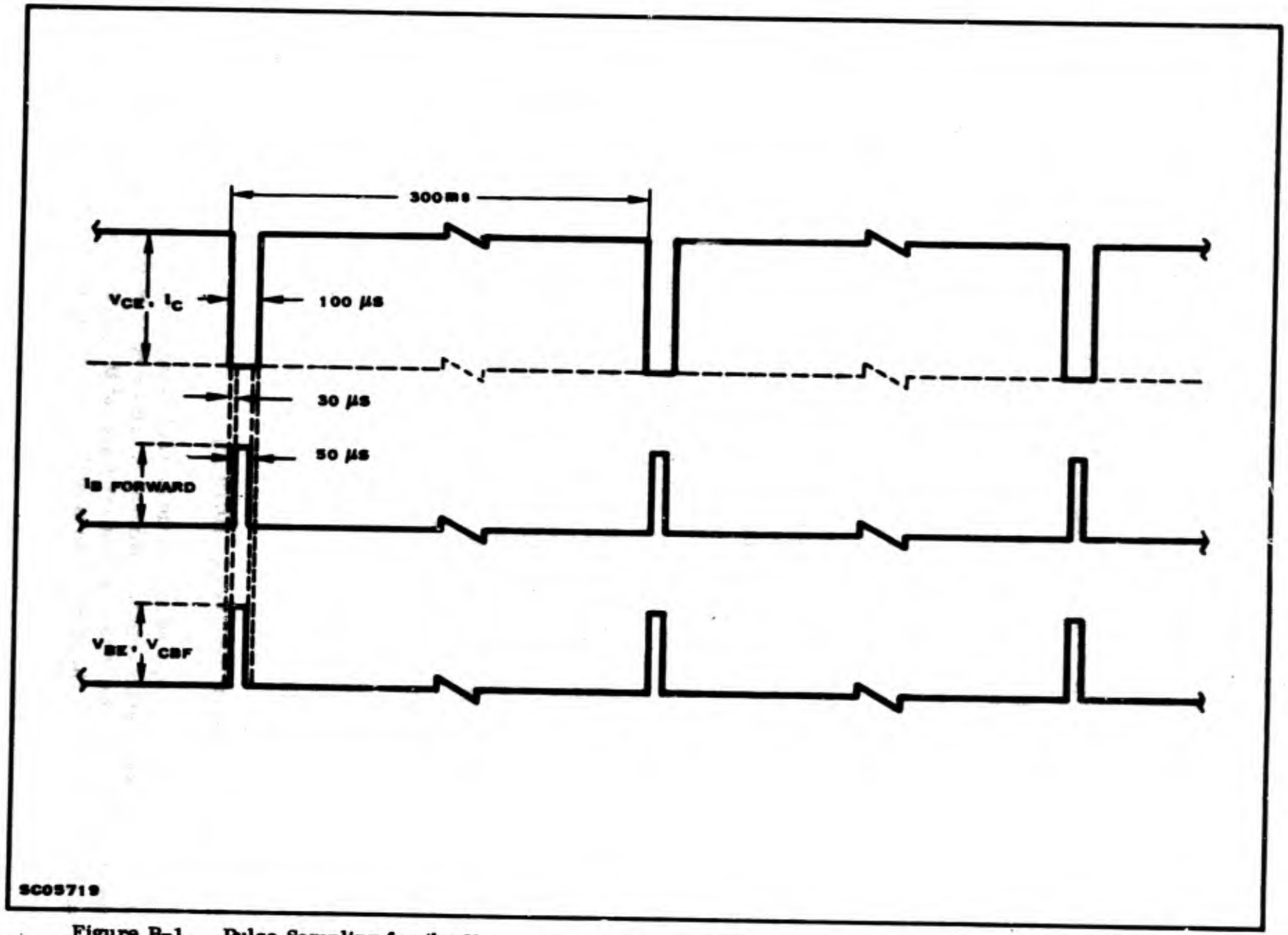

Figure B-1. Pulse Sampling for the V_{BE} and V_{CBF} Methods of Indicating Operating Junction Temperature

and pulse duration. The power pulse is applied only long enough to heat the region of the junction to steady state but not long enough to heat the outside of the case appreciably.

When a device is placed in the test socket, a test current (I_{CBF}) is automatically established through the collector-base junction until a forward bias voltage (V_{CBF}) of 500 mV is obtained as illustrated in Figure B-2. The power pulse is applied to the device when the test switch is pushed. Within 100 μsec after the termination of this power pulse, the initial test current (I_{CBF}) is re-established and V_{CBF} is displayed on an oscilloscope through a differential preamplifier. 500 mV is subtracted in this pre-amplifier to take into account the value of V_{CBF} at room temperature.

The temperature difference between the elevated junction temperature, T_J, and the initial junction temperature which is in fact the case temperature, T_C, is determined from the peak ΔV_{CBF} reading as

$$T_J - T_{Case} = \frac{\Delta V_{CBF}}{k}$$

where k is the slope of the dependence of V_{CBF} on temperature ($\Delta V_{CBF}/\Delta T$). For silicon power devices k has a value of approximately 2.0 mV/°C and is very constant up to at least 200°C. Thermal impedance is calculated as

$$\theta_{J-C} = \frac{\Delta V_{CBF}}{k V_{CE} I_C}$$

3. CONTINUOUS OPERATION h_{FE} METHOD

The h_{FE} method uses the current gain of a transistor as the temperature sensitive parameter. This method uses dc operation at two conditions with no preliminary measurement necessary. The case or ambient of the device is elevated to a temperature T_1 and a bias is applied to the transistor to give an applied power P_1. The ambient temperature plus the temperature due to bias heating should not exceed the maximum temperature rating of the device. The value of h_{FE} is noted at some current level. The case or ambient temperature is increased to a higher temperature T_2 and the power is reduced to P_2 which maintains the same value of h_{FE} at the same current level as read at the lower temperature. The thermal impedance is calculated as

$$\theta_{J-C} = \frac{T_2 - T_1}{P_1 - P_2} \Bigg|_{\substack{h_{FE} = \text{constant} \\ I_C = \text{constant}}}$$

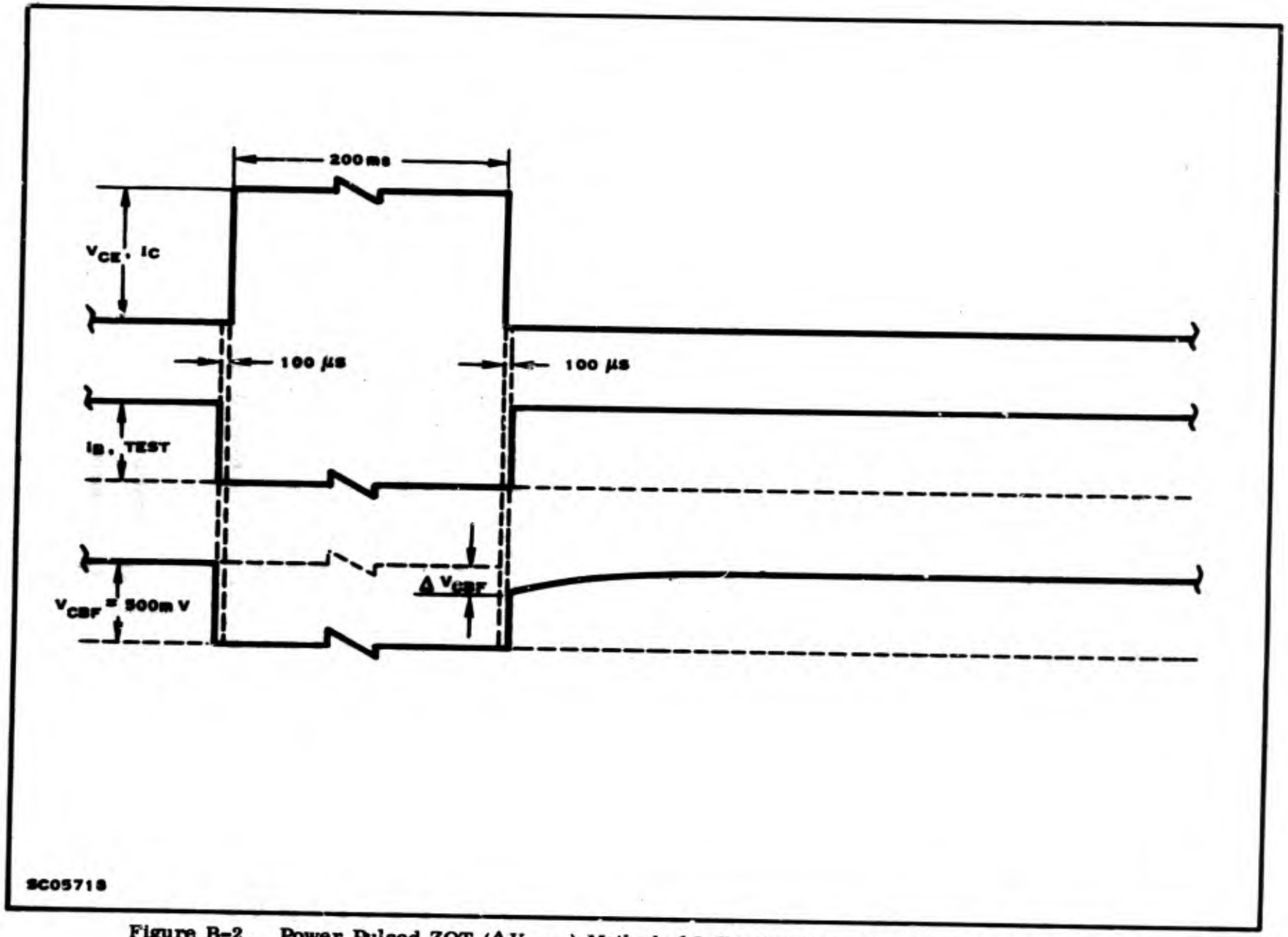

Figure B-2. Power Pulsed ZOT (ΔV_{CBF}) Method of Indicating Operating Junction Temperature

4. INFRARED MICRORADIOMETER METHOD

An infrared microradiometer is used to measure the infrared radiation in the 2 to 5.6 μ range being emitted from an area 1.5 by 1.5 mils. The emissivity of the surface is controlled by applying a thin uniform high-emissivity coating. With a calibration of the system, the temperature on the surface of an operating transistor can be measured directly. By using the measured peak surface temperature, which is only a few percent less than peak junction temperature $T_{J\text{-}MAX}$, and the case temperature T_C, a definition for thermal impedance can now be made which indicates the actual maximum thermal stress of the device. It has been suggested by Peterman[4] that a new symbol be used to indicate thermal impedance when the $T_{J\text{-}MAX}$ is used. This new symbol is defined as

$$\varphi_{J\text{-}C} = \frac{T_{J\text{-}MAX} - T_C}{P}$$

where P is the applied power. The symbol distinguishes the use of $T_{J\text{-}MAX}$ from the use of the junction temperature (T_J) determined by indirect electrical techniques. Although it is felt that such a new symbol makes a useful distinction only the traditional symbol, $\theta_{J\text{-}C}$, is used in this report to indicate thermal impedance.

APPENDIX C

EVALUATION EXPERIMENTS

APPENDIX C

EVALUATION EXPERIMENTS

1. SECOND BREAKDOWN CHARACTERIZATION EXPERIMENT

a. Introduction

An experiment was designed to ascertain whether the probability of failure of a device subjected repeatedly to thermal (second) breakdown for a limited period was a function primarily of the number of times the device was subjected to such treatment, or of the total time spent in such treatment, or some function of both. A random batch of devices was split up into five groups (of ten devices each). Each device in a group was then subjected to a series of operations in the thermal-breakdown mode, the stress duration being different for each group, until the device parameters showed significant degradation. Thus, for each group it was possible to measure the proportion of units failing as a function of the number of operations, and equally as a function of the total time in operation.

b. Stress Circuit

The equipment used for this experiment is a modified form of the equipment described in a previous report.[3] A block schematic is shown in Figure C-1. The application of a pulse to the base of T_1 turns on the emitter and collector supplies to the transistor under test (TUT). When the device enters breakdown, the collector current is limited, and the collector-base voltage falls abruptly. This fall is used to trigger a time-delay circuit which, after a controlled delay (0.5 to 15 ms) turns off the pulse applied to T_1, removing the emitter and collector supplies. This time delay is the stress duration. If no breakdown occurs, the applied pulse is terminated automatically after 20 to 25 ms. The waveforms of the collector-base and collector-emitter voltages, and the collector current can be monitored by an oscilloscope as shown.

c. Discussion and Results

The prebreakdown conditions are established at V_{CE} = 60 V, I_C = 1.5 A, and the post-breakdown current is set to 1.8 A. The stress durations used for the groups are 2, 5, 8, and 10 ms. The results of the experiment are tabulated in Table C-1, and graphically presented in Figures C-2 and C-3. The variation

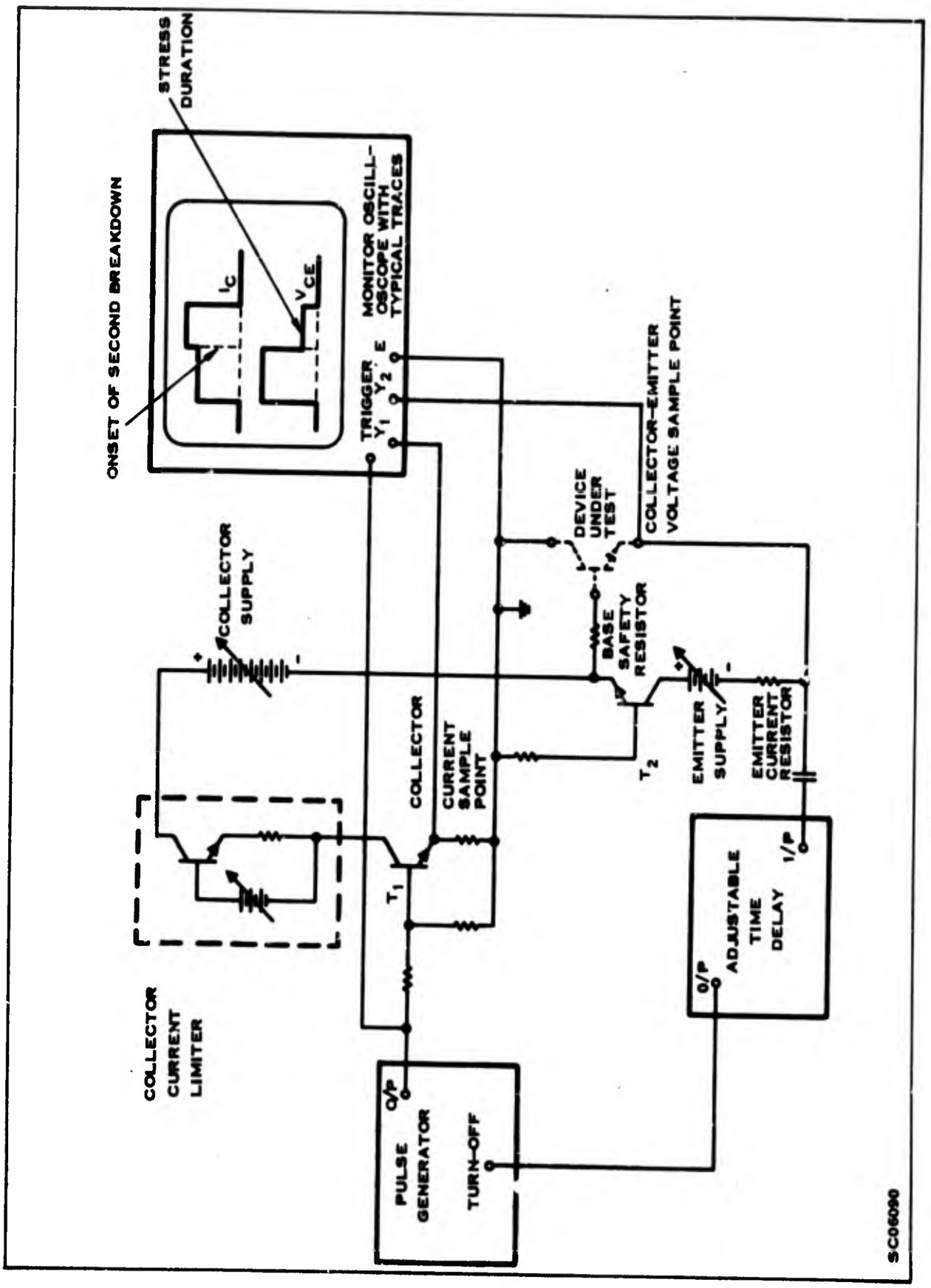

Figure C-1. Circuit Used to Stress Devices

Table C-1. Results of Characterization Experiment

Failures (%)	Test Groups							
	No. 1 (2 ms Stress Duration)		No. 2 (5 ms Stress Duration)		No. 3 (8 ms Stress Duration)		No. 4 (10 ms Stress Duration)	
	Actual Time in Second Breakdown (ms)	No. of Applied Stresses	Actual Time in Second Breakdown (ms)	No. of Applied Stresses	Actual Time in Second Breakdown (ms)	No. of Applied Stresses	Actual Time in Second Breakdown (ms)	No. of Applied Stresses
10	34	17	20	4	72	9	50	5
20	42	21	40	8	156	17	50	5
30	44	22	45	9	176	22	60	6
40	80	40	95	19	216	27	70	7
50	110	55	245	49	248	31	90	9
60	122	61	325	65	320	40	140	14
70	258	129	340	68	360	45	150	15
80	544	272	460	92	384	48	290	29
90	704	352	490	98	400	50	640	64
100	1280	640	1635	327	592	74	3050	305

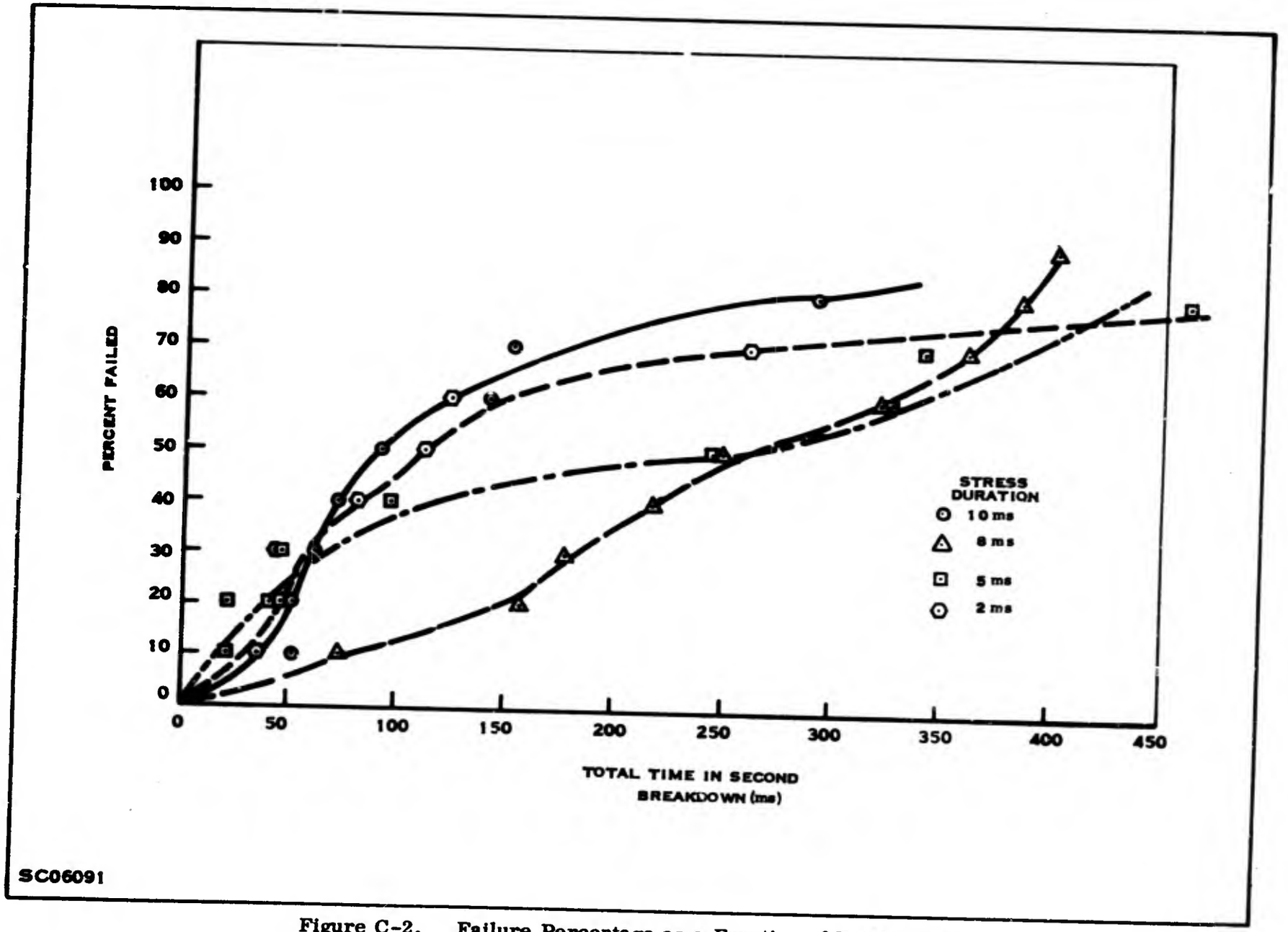

Figure C-2. Failure Percentage as a Function of Total Time

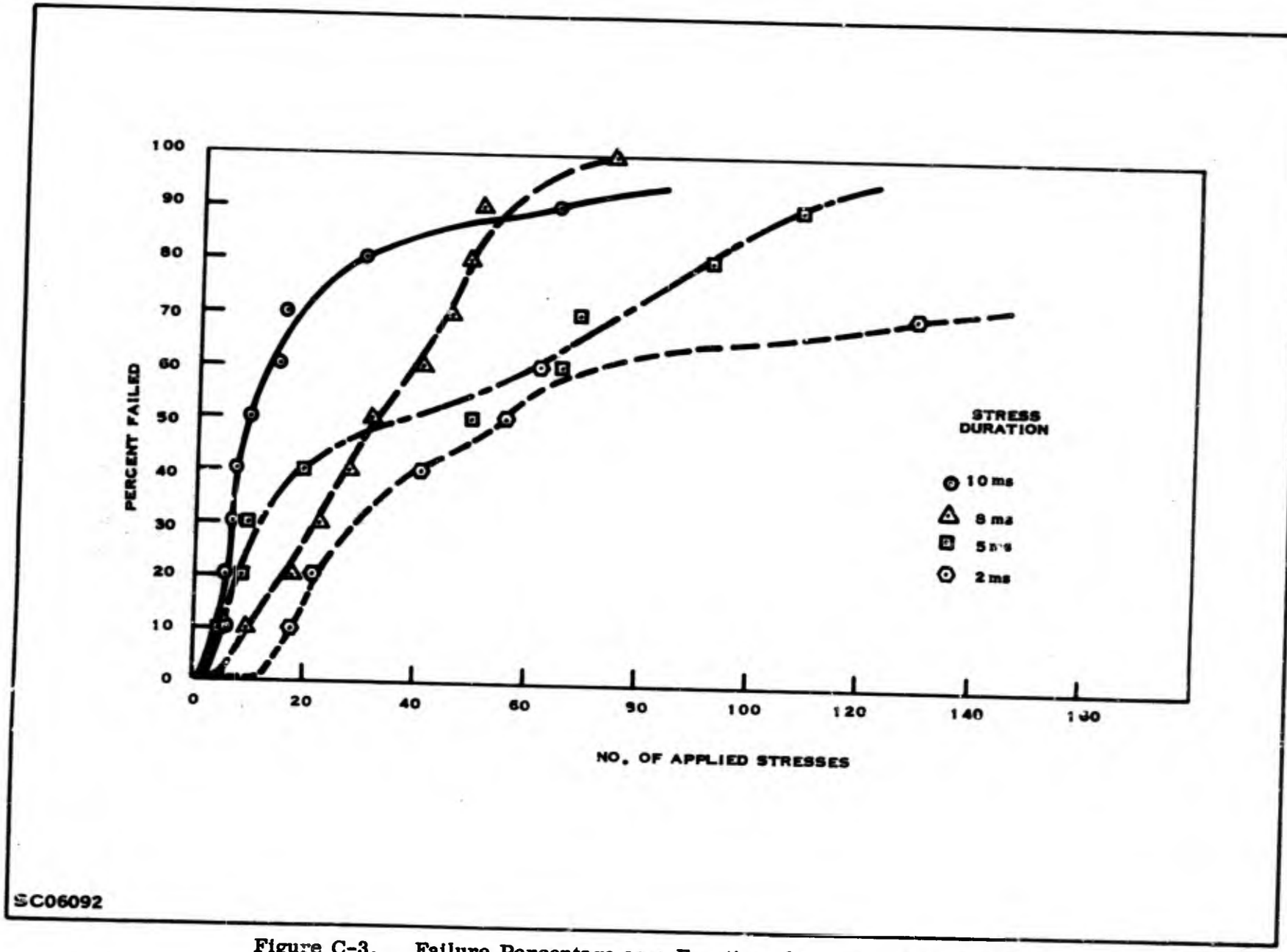

Figure C-3. Failure Percentage as a Function of Number of Stresses

between devices is considerable. There are some anomalies among the results and the pattern that emerges is somewhat subjective. But there is a suggestion at least that for a given total time under stress (i.e., number of pulses x duration of the pulse), long pulses are more effective in inducing failure than short ones.

The mechanisms proposed in Section IX suggest that changes in the device due to the breakdown are progressive and cumulative and, furthermore, that the rate of change should increase during the breakdown period. If so, we would expect that the groups subjected to greater stress durations would require less total time to degrade, as is observed. If a minimum period of operation in breakdown were required before any such damage occurred, then repeated operation for stress duration below this would cause no degradation and, just above the threshold, the total time to degradation would be very long. The results suggest that any such delay must be short and certainly less than the shortest period used in this experiment.

2. SECOND BREAKDOWN SCREEN EXPERIMENT

a. Discussion

On the basis of the above experiment, a set of preconditioning stresses can be set up to test the reliability changes in devices after such pretreatment. A preliminary experiment of this type is discussed in a previous report, [3] however the new equipment (Figure C-1) allows better control of the time spent by the device in the thermal-breakdown mode. Also, readings were taken of the thermal resistance of the device at 30 V, 1.0 A and at 40 V, 0.5 A before the preconditioning. A measurement was made of the delay time between applying the full conditions of 60 V V_{CE} and 1.5 A I_C to the device, and the breakdown to the limiting current of 1.8 A. It was hoped to correlate these readings and to relate them to the failures observed on the power operating life test. The power operating life test was 120 hours at a case temperature (T_C) of 100°C with V_{CE} = 40 V and I_C = 0.35 A.

The data taken after the preconditioning were found to be in error but this fact was not discovered until the test had been completed. The data on this experiment is presented below.

b. Test Results

The units were divided into five groups. Four groups received different amounts of controlled stresses and the other group was the control. The amount of controlled stresses for the four groups were 10, 25, 60 and, 100 stresses respectively. After application of these preconditioning stresses, all surviving units, together with the control group, were placed on the power operating life test. The results are given

in Table C-2. As expected, the proportion of total failures increases with stress. Also the proportion of those units which fail on life test after preconditioning appears to increase with stress level.

Table C-2. Summary of Failures that Occurred During Breakdown Preconditioning and After Subsequent Power Operating Life Tests

Group	Preconditioning Groups				
	Control	10 Stresses	25 Stresses	60 Stresses	100 Stresses
UNITS STARTED ON PRECONDITIONING	20	18	23	22	8
Preconditioning Failures* (A)	--	3	8	9	6
Failed to Enter Breakdown	--	0	1	0	0
Units Surviving Preconditioning	20	15	14	13	2
UNITS STARTED ON LIFE TEST	20	15	14	13	2
Catastrophic Failures	2	3	3	4	2
Degradation Failures	1	2	2	0	0
Total Failures on Life Test (B)	3	5	5	4	2
TOTAL FAILURES (A and B)	3	8	13	13	8

*The criterion for this type of failure is not the same as for the other failures. See Text.

A summary of the units failing at each stage as a function of their delay times is shown in Table C-3. The data indicate poor correlation of total failures with delay time but there appears to be some correlation between preconditioning failures and delay time. A graph of the number of stresses survived by units against their thermal resistance is shown in Figure C-4. The units which failed earliest were predominantely those with highest values of thermal resistance.

One might expect units with high thermal resistance to have a short delay time before breakdown. Figure C-5 shows that the correlation only operates for high thermal resistance units taken at V_{CE} = 40 V. This correlation disappears for high thermal resistance taken at a low voltage (V_{CE} = 30 V) as seen in Figure C-6.

Table C-3. Summary of Failures at Different Delay Times

Delay Time (ms)	8.0 to 8.4	8.5 to 8.9	9.0 to 9.4	9.5 to 9.9	10.0 to 10.4	10.5 to 10.9	11.0 to 11.4	11.5 to 11.9	12.0 to 12.4	12.5 to 12.9	13.0 to 13.4	13.5 to 13.9	14.0 to 14.5	> 15	Not Known	Total	Control
Total Units		1	2	1	9	10	10	9	8	8	3	5	1	1	3	71	20
Preconditioning Failures*		1	2	0	6	4	3	2	1	1	0	3	0	0	3	23	0
Catastrophic Failures		0	0	1	0	1	2	3	2	0	3	0	0	0	0	12	2
Degradation Failures		0	0	0	1	0	0	0	1	2	0	0	0	0	0	4	1
Survivors		0	0	0	2	5	5	4	4	5	0	2	1	1	0	29	17

*The criterion for this type of failure is not the same as for the other failures. See text.

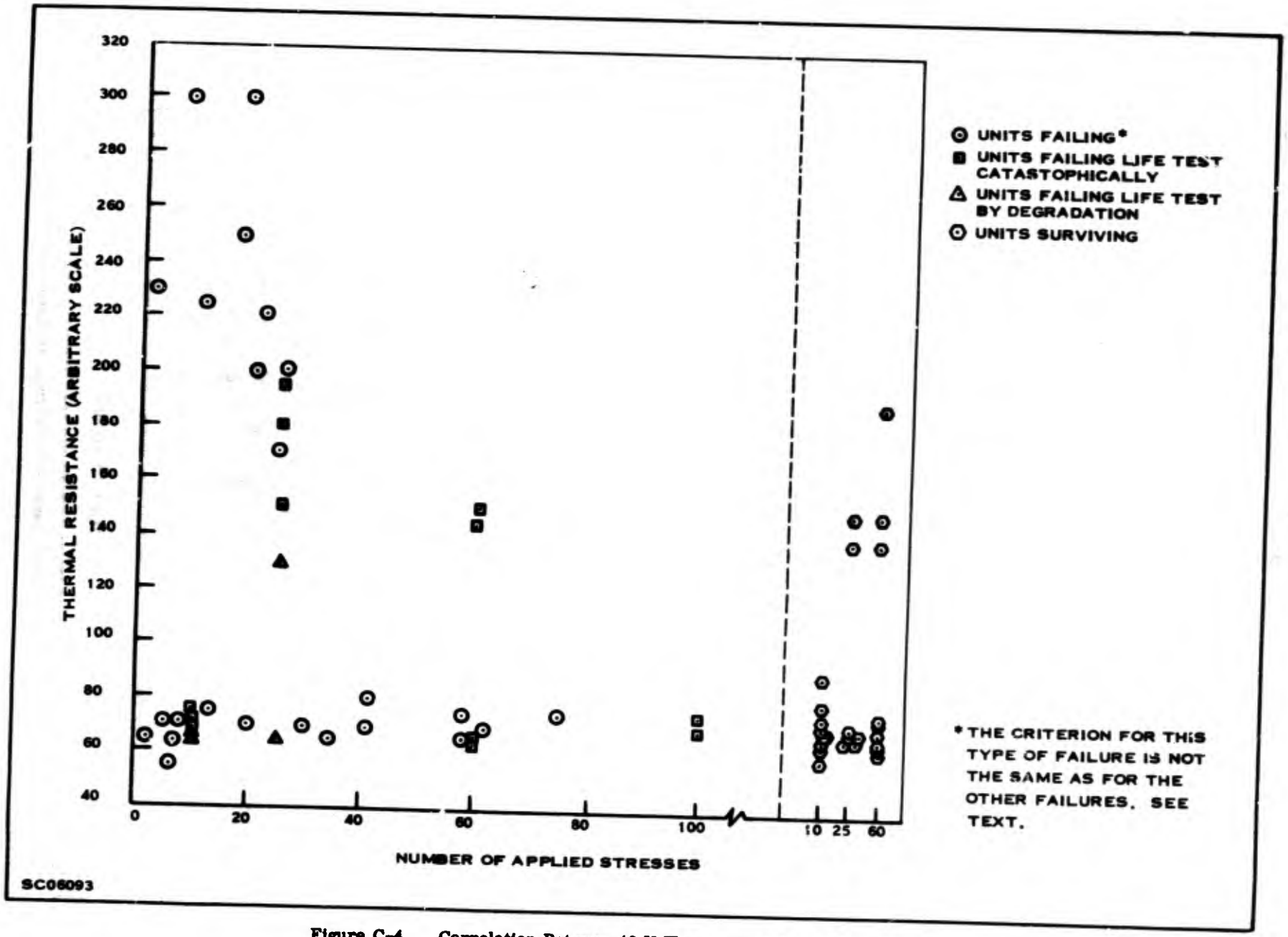

Figure C-4. Correlation Between 40 V Thermal Resistance and Failure

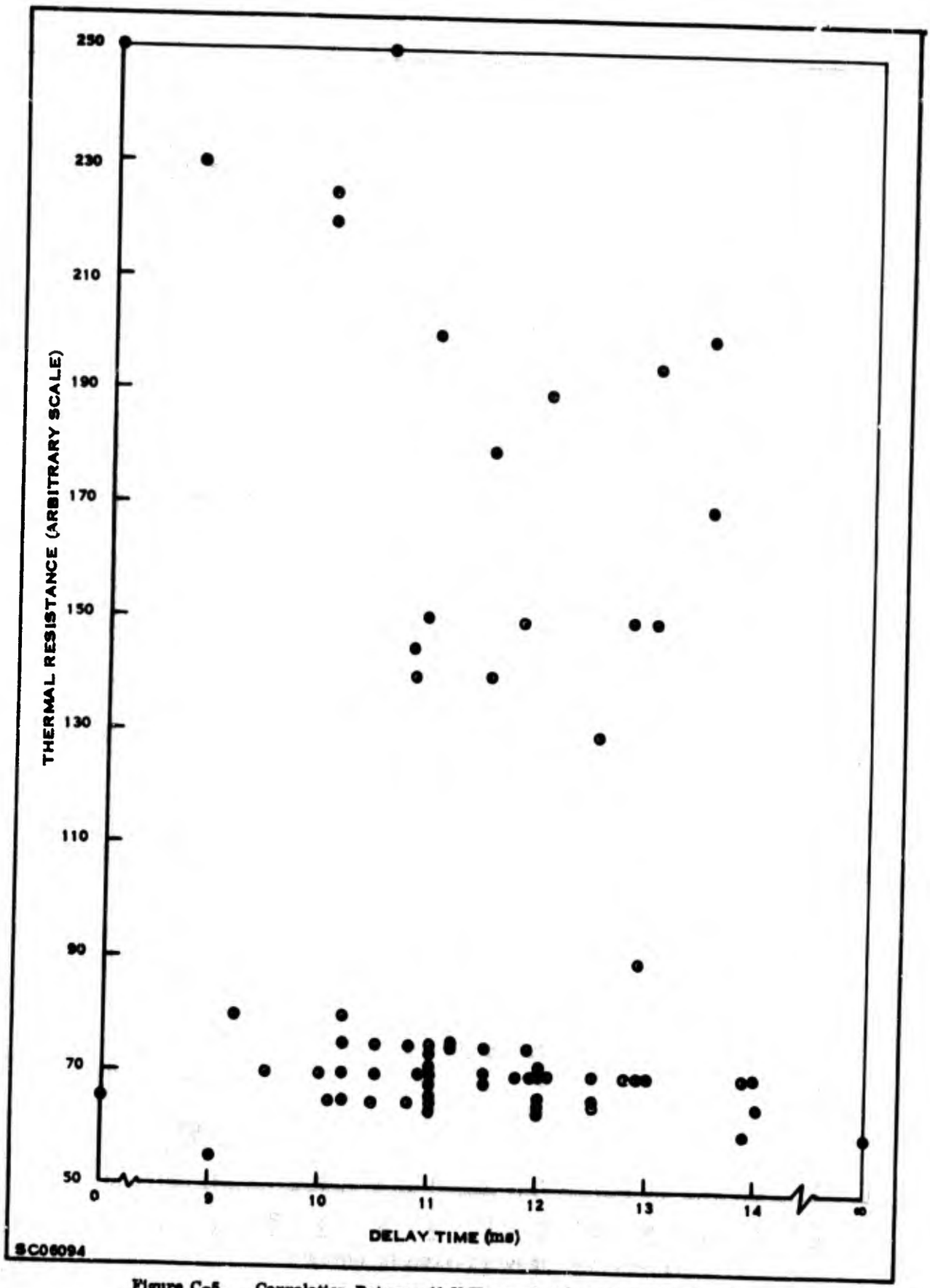

Figure C-5. Correlation Between 40 V Thermal Resistance and Delay Time

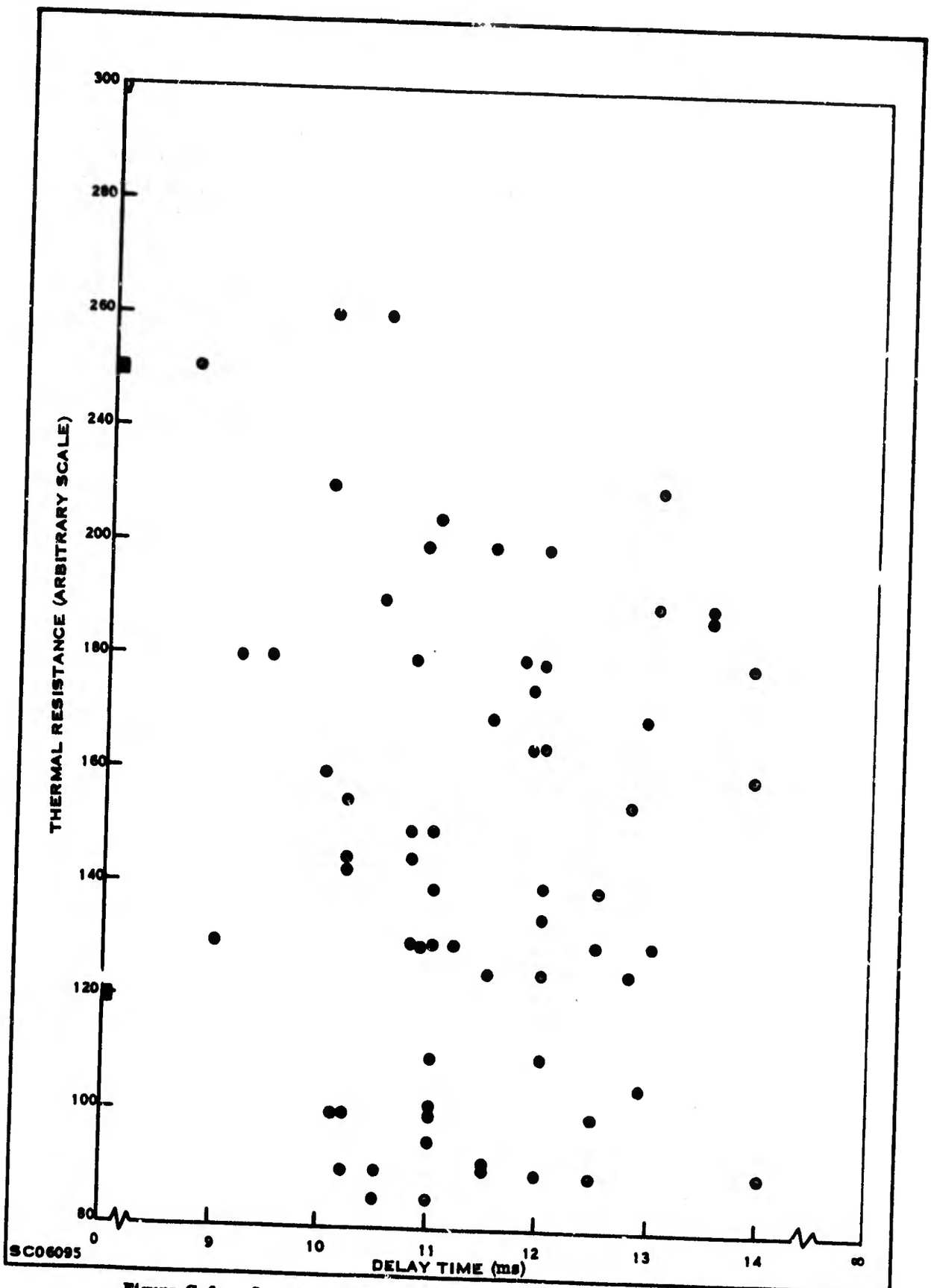

Figure C-6. Correlation Between 30 V Thermal Resistance and Delay Time

c. Conclusion

Pulsing devices into second breakdown showed that for a fixed total stress time (i.e., number of pulses x duration of the pulse), long pulses are more effective in inducing failure than short pulses. It was observed that units with high thermal resistance values obtained at a high voltage (V_{CE} = 40 V) correlated with a short delay time before breakdown. This correlation disappears for high thermal resistance values taken at a lower voltage (V_{CE} = 30 V).

APPENDIX D

SUMMARY OF FAILING PARAMETERS BY TEST STEP FOR BOTH MAIN TEST AND VERIFICATION TEST PROGRAMS

APPENDIX D

SUMMARY OF FAILING PARAMETERS BY TEST STEP FOR BOTH MAIN TEST AND VERIFICATION TEST PROGRAMS

This appendix contains tables of backup data for the failure summary tables in Section IV-7 and Section V-5. This backup data in Tables D-1 through D-8 summarizes the failing parameters by test step for each test.

Additional tables summarizing the failure parameters (indicators) for each test are presented in Tables D-9 through D-12. To recap; the first time at which a device exceeds one or more degradation parameter limits (Section III) is considered the failure step and those parameters which are outside the limits are referred to as the failure indicators. The number of devices which exceeded the parameter limit the first time is found in the left hand column of Tables D-9, D-10 and D-11 for the Main Test Program and in Table D-12 for the Verification Test Program. Also included in the tables is supplementary information regarding the number of times that particular parameter limits were exceeded independent of the failure step. Thus, for example, a group of devices could fail by a number of different parameters at the failure step but all might subsequently exceed a particular parameter limit. This is not a failure indicator since it occurred after the device was considered a failure but it can be of interest in deciding on the correct failure mechanism.

The number of times that each parameter limit was exceeded for all devices, independent of test step for each test, is found in the right hand side of each column in Tables D-9, D-10 and D-11 for the Main Test Program and in Table D-12 for the Verification Test Program. Further explanation of these tables is presented. Refer to Table D-9 and the 200°C Temperature Storage Life Test. It is seen that there were 11 devices which exceeded the failure criteria (Section III). Five exceeded the h_{FE}(5 mA) failure criteria at the first point of failure, i.e., the first step at which the current gain of that device exceeded the failure criteria. During the nine readout times of this test the limits of this parameter h_{FE}(5 mA) where exceeded a total of 18 times by some or all of the 11 failures. The remainder of the table is interpreted in the same manner.

Table D-1. Summary of Failing Parameters by Test Step — Temperature Storage Step Stress Tests — Main Test Program

Test Description Temp. Step Stress (Hrs/Step)	Test Step	Failures/ Step	I_{CEO} 30 V	I_{CEO} 70 V	I_{CBO} 30 V	I_{CBO} 70 V	I_{EBO} 5 V	I_{EBO} 8 V	h_{FE} 5.0 mA	h_{FE} 1.0 A	V_{BE} (sat)	V_{CE} (sat)	Cum. Failures
2	1	0											0
	2	1	1	1	1								1
	3	0											1
	4	0											1
	5	1					1	1					2
	6	2					1	1			1		4
	7	2					1				1		6
Totals			1	1	1		3	2			2		
8	1	1											1
	2	1		1									2
	3	0											2
	4	1	1	1		1	1						3
	5	2						1	1				5
	6	2	1	1	1	2	1	1	1				7
	7	4		2			1	1					11
Totals			2	5	1	3	3	3	2				
24	1	1		1		1							1
	2	0											1
	3	0											1
	4	2		2		1	1	1					3
	5	1	1										4
	6	2	1	1	1	1					1		6
	7	0											6
Totals			2	4	1	3	1	1			1		
96	1	0											0
	2	1	1	1									1
	3	1							1				2
	4	1		1									3
	5	3	1	2	1	1	2	1					6
	6	0											6
	7	2							2				8
Totals			2	4	1	1	2	1	3				

Table D-2. Summary of Failing Parameters by Test Step — Temperature Storage Fixed Matrix Tests — Main Test Program

Test Description Storage Life	Test Step	Failures/ Step	I_{CEO} 30 V	I_{CEO} 70 V	I_{CBO} 30 V	I_{CBO} 70 V	I_{EBO} 5 V	I_{EBO} 8 V	h_{FE} 5.0 mA	h_{FE} 1.0 A	V_{BE} (sat)	V_{CE} (sat)	Cum. Failures
(°C)	1	1	1	1		1							1
	2	0											1
	3	0											1
	4	0											1
200	5	3		1				1	1		1		4
	6	2	1						1				6
	7	3							3				9
	8	2						1			1		11
	9	0											11
Totals			2	2		1		2	5		2		
	1	6	2	2		2	1	1			1		6
	2	4	1	2	1	2	1		1				10
	3	4		1					2		2		14
	4	2		1				1	1				16
250	5	5	1	3		1		1	1				21
	6	6	2	3	2	2		1	3		1	1	27
	7	3							3				30
	8	8	2	2		2			3		3	1	38
	9	10	1	2		1	1	2	6		1	1	48
Totals			9	16	3	10	3	6	20		8	3	
	1	17	5	6	3	5	7	6	8		2	2	17
	2	16	7	9	6	7	2	4	8			1	33
	3	13	1	3	1	2	4	5	6	2			46
	4	21	6	11	2	3	1	1	12	2	1	2	67
300	5	8	7	7	7	7	4	3	4	3	2	3	75
	6	4	3	4	3	1	1		1				79
	7	3		3									82
	8	1	1	1	1	1							83
	9	4	1	1	1	1					1		87
Totals			31	45	24	27	19	19	39	7	6	8	

Table D-3. Summary of Failing Parameters by Test Step — Reverse Bias Step Stress Tests — Main Test Program

Test Description Reverse Bias Step Stress (Hrs/Step)	Test Step	Failures/ Step	I_{CEO} 30 V	I_{CEO} 70 V	I_{CBO} 30 V	I_{CBO} 70 V	I_{EBO} 5 V	I_{EBO} 8 V	h_{FE} 5.0 mA	h_{FE} 1.0 A	V_{BE} (sat)	V_{CE} (sat)	Cum. Failures
2	1	0											0
	2	0											0
	3	2											2
	4	1	1	1									3
	5	0											3
	6	0											3
	7	3	2	2	2	2	1		1				6
Totals			3	3	2	2	1		1				
8	1	1	1	1	1	1							1
	2	0											1
	3	2	1	2	1	2	1	1	1	1	1	1	3
	4	0											3
	5	0											3
	6	1	1		1								4
	7	4	1	2	1	1			2				8
Totals			4	5	4	4	1	1	3	1	1	1	
24	1	0											0
	2	3	3	3	3	3	3	3	3	3	2	3	3
	3	1	1	1	1	1							4
	4	0											4
	5	1							1				5
	6	7	1	1			1	1					12
	7	5	2	2	2	2	1		3				17
Totals			7	7	6	6	5	4	7	3	2	3	
96	1	3	2	2	1	1					1		3
	2	6	1						3				9
	3	1											10
	4	2	1	2	1	2			1				12
	5	4	2	2	2	1	2	1	2	1			16
Totals			6	6	4	4	2	1	6	1	1		

Table D-4. Summary of Failing Parameters by Test Step — Reverse Bias
Fixed Matrix Tests — Main Test Program

Test Description Reverse Bias Life	Test Step	Failures/ Step	I_{CEO} 30 V	I_{CEO} 70 V	I_{CBO} 30 V	I_{CBO} 70 V	I_{EBO} 5 V	I_{EBO} 8 V	h_{FE} 5.0 mA	h_{FE} 1.0 A	V_{BE} (sat)	V_{CE} (sat)	Cum. Failures
(°C)	1	3		1			2	2			1		3
	2	1									1		4
	3	0											4
	4	1		1									5
125	5	2	1				1	1			1		7
	6	12	9	7	9	7	4	4	1		1		19
	7	9	1						2				28
	8	18	1	1	1	1	1	1	2	1			46
	9	6	3	3	3	3	3	4	4	3	2	2	52
Totals			15	13	13	11	11	12	10	4	6	2	
	1	6	3	4	1	2	1	1				1	6
	2	3	2	2	1	1			1				9
	3	2	1	1	1						1		11
	4	2	2	2	1	1							13
175	5	2	1	2		2							15
	6	10	2	2	1	2	1	1	1		4	3	25
	7	14							2				39
	8	8	1	1	1	1	1	1	2	1	1	1	47
	9	6											53
Totals			12	14	6	9	3	3	6	1	6	5	
	1	5	2	2	2	2	2	1			1		5
	2	1	1	1									6
	3	3	2	1	1							1	9
	4	1							1				10
225	5	18	7	8	8	8	2	3	4	3	1	1	28
	6	18		1		1	1	2	5	2	1		46
	7	18	2	2	1	1	1	2	4	2	1	1	64
	8	13	1	3					1	1	1		77
	9	12							1		2		89
Totals			15	18	12	12	6	8	16	8	7	3	

Table D-5. Summary of Failing Parameters by Test Step — Power Operating Step Stress Tests — Main Test Program

Test Description Oper. Step Stress (Hrs/Step)	Test Step	Failures/ Step	I_{CEO} 30 V	I_{CEO} 70 V	I_{CBO} 30 V	I_{CBO} 70 V	I_{EBO} 5 V	I_{EBO} 8 V	h_{FE} 5.0 mA	h_{FE} 1.0 A	V_{BE} (sat)	V_{SAT} (sat)	Cum. Failures
2	1	1					1	1	1				1
	2	0											1
	3	0											1
	4	0											1
	5	1							1				2
	6	2					2	1	1	1	1	1	4
	7	1							1				5
	8	2	1	1	1	1	2	1	1				7
	9	1					1						8
Totals			1	1	1	1	6	3	5	1	1	1	
8	1	0											0
	2	0											0
	3	0											0
	4	0											0
	5	0											0
	6	3	2	1	1	1	2	2	1				3
	7	1									1		4
	8	1							1				5
	9	0											5
Totals			2	1	1	1	2	2	2		1		
24	1	0											0
	2	0											0
	3	0											0
	4	0											0
	5	1		1									1
	6	4	1	1	1	1	4	3	1				5
	7	3					1	1	3				8
	8	0											8
	9	0											8
Totals			1	2	1	1	5	4	4				
96	1	0											0
	2	0											0
	3	0											0
	4	0											0
	5	0											0
	6	1							1				1
	7	7	1	2	2	2	6	5	5				8
	8	0											8
	9	1	1	1	1	1	1	1	1				9
Totals			2	3	3	3	7	6	7				

Table D-6. Summary of Failing Parameters by Test Step — Power Operating Fixed Matrix Tests — Main Test Program

Test Description Oper. Life	Test Step	Failures/ Step	I_{CEO} 30 V	I_{CEO} 70 V	I_{CBO} 30 V	I_{CBO} 70 V	I_{EBO} 5 V	I_{EBO} 8 V	h_{FE} 5.0 mA	h_{FE} 1.0 A	V_{BE} (sat)	V_{CE} (sat)	Cum. Failures
(W)	1	1					1	1	1				1
	2	1						1					2
	3	0											2
	4	1					1						3
15	5	1		1									4
	6	0											4
	7	0											4
	8	0											4
	9	1						1					5
Totals				1			2	3	1				
	1	6	1	1	1	1	6	6	3				6
	2	0											6
	3	1									1		7
	4	3	1		1		1	1	1				10
37.5	5	1									1		11
	6	2		1			1	1	1				13
	7	0											13
	8	0											13
	9	4						2	2				17
Totals			2	2	2	1	8	10	7		2		
	1	43	23	28	17	26	9	10	10	1			43
	2	5		1	1	1	1		4				48
	3	2	1	1	1	1	1	1	1				50
	4	3			1		1		1				53
60	5	5	3	3	3	3	4	1	3	1	1	1	58
	6	2					1	2					60
	7	0											60
	8	0											60
	9	1		1		1							61
Totals			27	34	23	32	17	14	19	2	1	1	

Table D-7. Summary of Failing Parameters by Test Step — Temperature Storage Life Tests — Verification Test Program

Test Description Storage Life	Test Step	Failures/ Step	I_{CEO} 30 V	I_{CEO} 70 V	I^{*}_{CBO} 30 V	I_{CBO} 70 V	I_{EBO} 5 V	I_{EBO} 8 V	h_{FE} 5.0 mA	h_{FE} 1.0 A	V_{BE} (sat)	V_{CE} (sat)	Cum. Failures
(°C)	1	7					1	1	4	2			7
	2	7	2	2	1	2			6				14
275	3	13	2	2					11				27
	4	2							1		1		29
	5	6	1	2				2	2				35
	6	1							1				36
Totals			5	6	1	2	1	3	25	2	1		
	1	12	5	5	3	3			8				12
	2	6	1	2	1	1			4				18
300	3	4		1					4	1			22
	4	5		1			1	1	4				27
	5	4						1	2		1		31
	6	5	2	2	3	2	2	2	4	1	1		36
Totals			8	11	7	6	3	4	26	2	2		
	1		8	7	7	6	4	3	13	1			20
	2								4	2			24
	3	3	2	2					2				27
350	4	6	2	1	1	1			4		1		33
	5	10	2	2	4	3		3	7	2			43
	6	3		1		1	1	2	1	1			46
Totals			14	13	12	11	5	8	31	6	1		

Table D-8. Summary of Failing Parameters by Test Step — Power Operating Life Test — Verification Test Program

Test Description Operating Life	Test Step	Failures/ Step	I_{CEO} 30 V	I_{CEO} 70 V	I_{CBO} 30 V	I_{CBO} 70 V	I_{EBO} 5 V	I_{EBO} 8 V	h_{FE} 5.0 mA	h_{FE} 1.0 A	V_{BE} (sat)	V_{CE} (sat)	Failures Cum.
(W)	1	2							1	1			2
	2	3					2	2		1			5
30	3	1	1										6
	4	4				1	1	1	2				10
	5	6					2	5	1				16
	6	2					1	1	1				18
Totals			1			1	6	9	5	2			
	1	3					3	3					3
	2	4					2		2				7
50	3	1							1				8
	4	1					1						9
	5	3					1	2	1				12
	6	9					4	5	4		1		21
Totals							11	10	8		1		
	1	9					4	4	2	2	1		9
	2	6					5	5	2				15
80	3	0											15
	4	4					3	3	1				19
	5	8	1	1			4	3	1		1		27
	6	3					1	1	3				30
Totals			1	1			17	16	9	2	2		

Table D-9. Summary of Failure Indicators in Temperature Storage Life (Main Test Program)

Test Description	No. Fail	I_{CEO} 30 V	I_{CEO} 70 V	I_{CBO} 30 V	I_{CBO} 70 V	I_{EBO} 5 V	I_{EBO} 8 V	h_{FE} 5.0 mA	h_{FE} 1.0 A	V_{BE} (sat)	V_{CE} (sat)
Temperature Storage Life											
200° C	11	*2 †5	2 12	0 0	1 1	0 0	2 3	5 18	0 1	2 4	0 1
250° C	48	9 41	16 81	3 16	10 47	3 14	6 18	20 64	0 4	8 31	3 6
300° C	87	31 240	42 285	24 147	27 213	19 124	19 123	41 288	7 123	5 51	8 135
Temperature Step Stress											
2 Hrs/Step	6	*1 †5	1 6	1 5	0 6	3 4	2 3	0 1	0 0	2 5	0 0
8 Hrs/Step	11	2 9	5 19	1 5	3 16	3 13	3 14	2 8	0 0	0 0	0 0
24 Hrs/Step	6	2 7	4 14	1 5	3 13	1 4	1 4	0 1	0 0	1 2	0 0
96 Hrs/Step	8	2 10	4 13	1 7	1 7	2 5	1 3	3 11	0 0	0 1	0 0

* The left-hand entries are the number of devices which exceeded the parameter limit at the first point of failure.

† The right-hand entries are the number of readout times for which the devices exceeded the parameter limits.

Table D-10. Summary of Failure Indicators for Reverse Bias Life and Reverse Bias Step Stress (Main Test Program)

Test Description	No. Fail	I_{CEO} 30 V	I_{CEO} 70 V	I_{CBO} 30 V	I_{CBO} 70 V	I_{EBO} 5 V	I_{EBO} 8 V	h_{FE} 5.0 mA	h_{FE} 1.0 A	V_{BE} (sat)	V_{CE} (sat)
Reverse Bias Life											
125° C	52	*15 †40	13 40	13 32	11 31	10 28	12 36	10 19	4 7	6 18	2 9
175° C	53	12 54	14 57	6 32	9 43	3 16	3 17	6 19	1 4	6 14	5 16
225° C	89	15 42	18 46	12 35	12 36	6 34	8 34	16 37	8 16	7 23	3 18
Reverse Bias Step Stress											
2 Hrs/Step	6	* 3 † 4	3 4	2 3	2 3	1 1	0 0	1 1	0 0	0 0	0 0
8 Hrs/Step	8	4 10	5 12	4 10	4 11	1 3	1 3	3 4	1 1	1 1	1 1
24 Hrs/Step	17	7 [illegible]	7 11	6 9	6 9	5 7	4 6	7 18	3 11	2 4	3 4
96 Hrs/Step	16	6 18	6 21	4 14	4 18	2 3	1 2	6 14	1 1	1 3	0 0

*The left-hand entries are the number of devices which exceeded the parameter limit at the first point of failure.

†The right-hand entries are the number of readout times for which the devices exceeded the parameter limits.

Table D-11. Summary of Failure Indicators for Power Operating Life and Power Operating Step Stress Tests (Main Test Program)

Test Description	No. Fail	I_{CEO} 30 V	I_{CEO} 70 V	I_{CBO} 30 V	I_{CBO} 70 V	I_{EBO} 5 V	I_{EBO} 8 V	h_{FE} 5.0 mA	h_{FE} 1.0 A	V_{BE} (sat)	V_{CE} (sat)
Power Operating Life											
15 W	5	*0 †0	1 5	0 0	0 0	2 15	3 19	1 7	0 0	0 0	0 0
37.5 W	17	2 15	2 16	2 16	1 10	8 60	10 60	7 33	0 1	2 7	0 3
60 W	61	27 175	34 203	23 160	32 202	17 129	14 116	20 155	2 16	1 5	1 4
Power Operating Step Stress											
2 Hrs/Step	8	*1 †6	1 7	1 7	1 7	6 26	3 20	5 22	1 3	1 3	1 2
8 Hrs/Step	5	2 6	1 4	1 4	1 4	2 8	2 9	2 9	0 1	1 2	0 0
24 Hrs/Step	8	1 6	2 8	1 7	1 7	5 19	4 15	4 16	0 0	0 0	0 0
96 Hrs/Step	9	2 6	3 7	3 7	3 7	7 19	6 19	7 20	0 2	0 2	0 2

*The left-hand entries are the number of devices which exceeded the parameter limit at the first point of failure.

†The right-hand entries are the number of readout times for which the devices exceeded the parameter limits.

Table D-12. Summary of Failure Indicators in Temperature Storage and Power Operating Tests (Verification Test Program)

Test Description (Life Tests)	I_{CEO} 30V	I_{CEO} 70 V	I_{CBO} 30 V	I_{CBO} 70 V	I_{EBO} 5 V	I_{EBO} 8 V	h_{FE} 5.0 mA	h_{FE} 1.0 A	V_{BE} (sat)	V_{CE} (sat)
Temperature Storage										
275°C	*5 †32	6 33	1 11	2 12	1 4	3 10	25 83	4 14	1 6	--
300°C	8 46	11 56	7 24	6 32	3 11	4 20	26 82	2 10	2 8	0 1
350°C	14 78	13 76	12 61	11 62	5 31	8 35	31 111	6 41	1 11	--
Power Operating										
30 W	*1 †4	0 1	--	1 2	6 17	9 25	5 16	2 6	--	--
50 W	--	--	--	--	11 42	10 38	8 24	0 1	1 1	--
80 W	1 2	1 3	--	0 2	17 80	16 76	9 47	0 14	2 8	0 3

*The left-hand entries are the number of devices which exceeded the parameter limit at the first point of failure.

†The right-hand entries are the number of readout times for which the devices exceeded the parameter limits.

APPENDIX E

THEORY OF FIXED AND STEP STRESS TESTING

APPENDIX E

THEORY OF FIXED AND STEP STRESS TESTING

A brief discussion of the theory relating fixed to step stress will be given here. A more complete discussion is given in References 19, 20, 21, 22, and 23. If a sample of devices is exposed to a stress level S_2 and the number of devices failing at each read-out time is recorded during the stressing, a distribution of the number of failures as a function of time will be obtained. This is represented by B in Figure E-1. Subjecting another sample of devices to a different stress level such as S_1 will provide another distribution such as C. None of these distributions are necessarily normal. If the time for median failure for each stress level is plotted, the non-linear acceleration curve in Figure E-1 is obtained. Suitable transformations of stress and time can make the acceleration curve linear, such as the curve in Figure E-2. To be of value, these transformations must satisfy the following conditions:

a) The transformed distributions are normally distributed.

b) The standard deviations, σ, are constant and independent of the mean, μ.

c) The acceleration curve mentioned above should be linear with respect to the transferred scale.

The asterisks used in Figure E-2 denote transformed stress and time variables and the resulting transformed distributions. In Figure E-2, the stress variable is transformed by some function f_2. The same transformations are not used for both stress and time; the asterisks merely indicate that the variable has been transformed. An appropriate transformation for thermal stress is 1/T (°K) and for time is the logarithm of time. Knowing the standard deviation of the transformed normal distribution, the acceleration curve for other cumulative percent failures may be obtained. Thus the dotted line in Figure E-2 is the acceleration curve for a cumulative 3% failure (2 standard deviations from the mean).

An alternative method of generating the acceleration curve is by means of step stress testing, where a constant time for application of the stress is maintained and the stress levels are varied. In this type of testing, a group of devices is exposed to a certain stress level for a given time and then the surviving devices are exposed to the next higher stress level for the same length of time. This is usually continued until all or most of the devices have failed. It is assumed that the probability of failure at

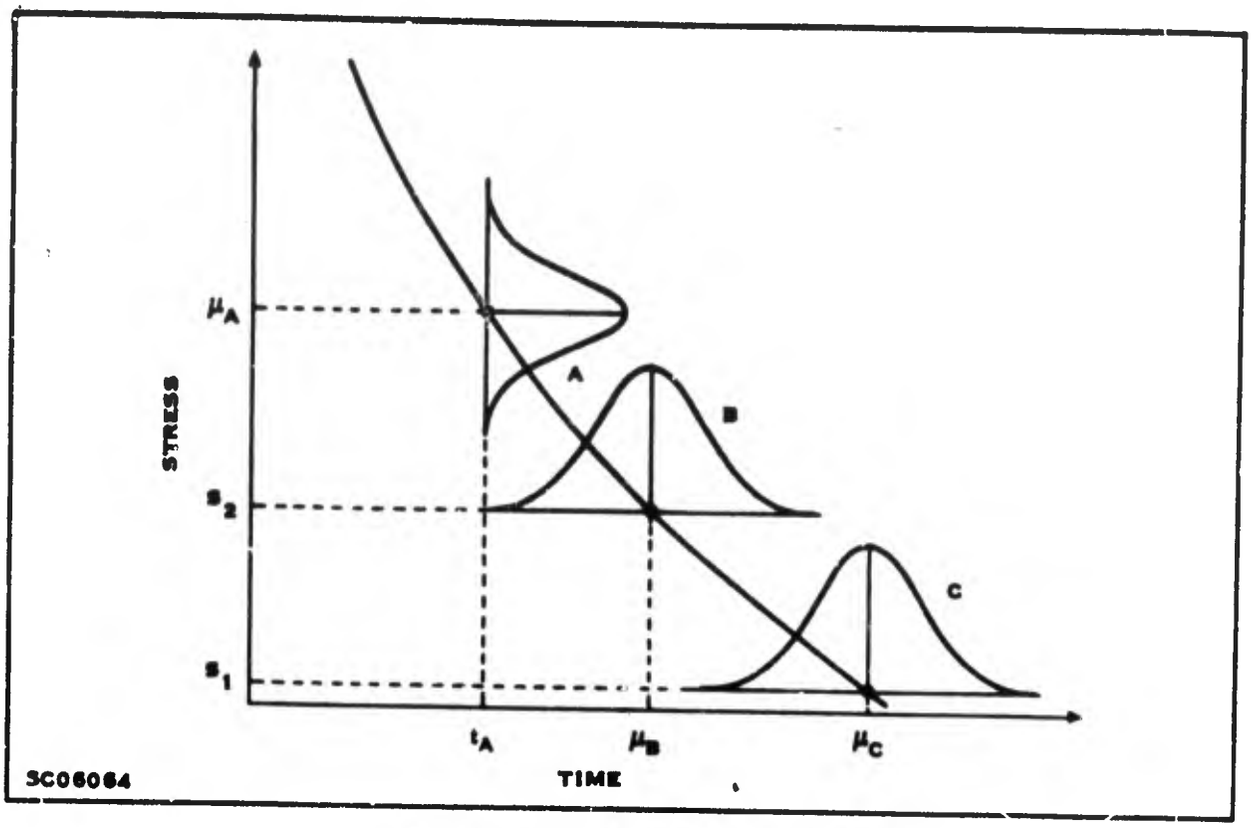

Figure E-1. Acceleration Curve

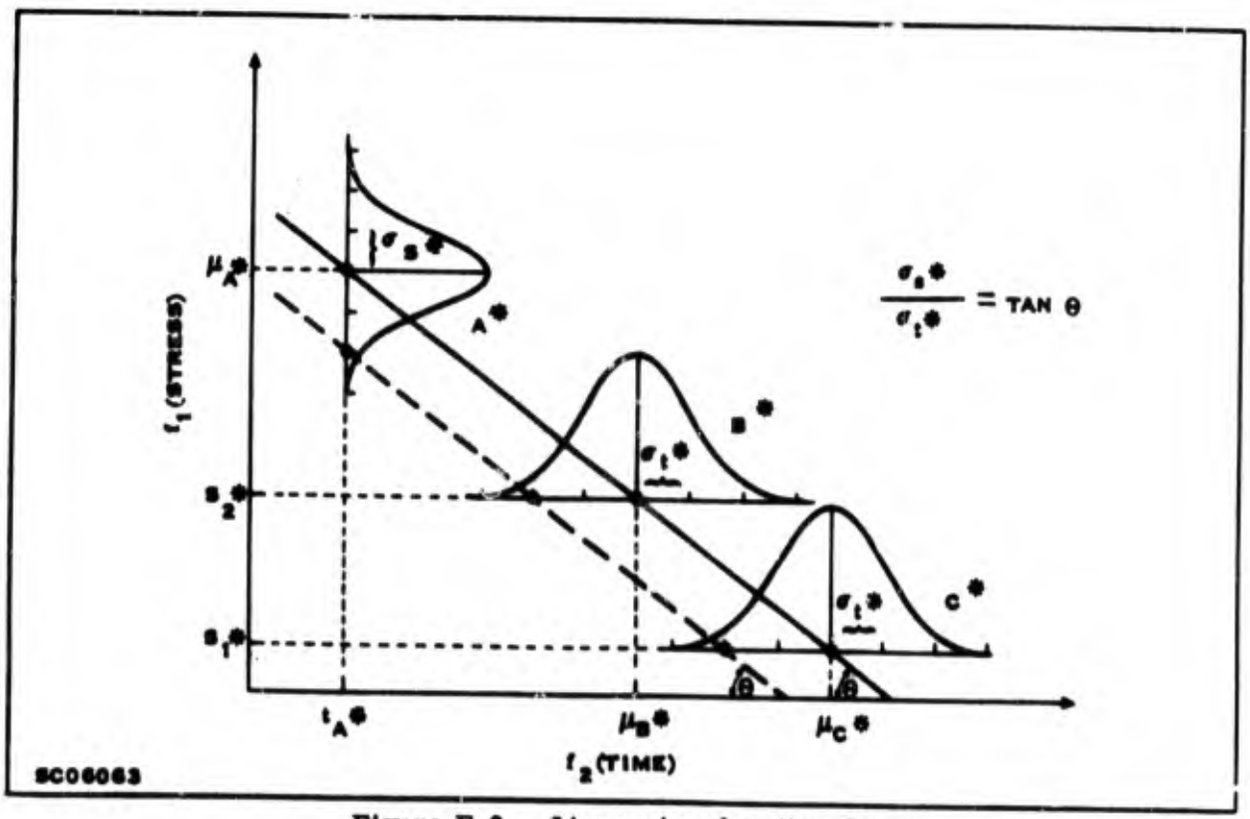

Figure E-2. Linear Acceleration Curve

a given point in the stress-time domain is independent of the path used to arrive at that point. For example, if a sample of devices is placed on a step stress test with tread-length t and the number of devices surviving after stress level S is noted, this same number of survivors should be obtained by using a constant stress test at level S for t hours. Using this assumption, the distribution of the number of failures as a function of stress obtained. An example of this is represented by A in Figure E-1. None of these distributions are necessarily normal. The median failure stresses, when plotted in the stress-time domain, should yield the same acceleration curve that is obtained by constant stress testing. Using the same transformations mentioned above, as well as assumptions a, b, and c, a linear acceleration curve such as the one in Figure E-2 may be obtained. This transformed constant time acceleration curve should be the same as the transformed constant stress acceleration curve. The transformed standard deviations of the stress and time distributions are not independent; they are related by the equation:

$$m(\text{slope of acceleration curve}) = \tan\theta = \frac{\sigma_s^*}{\sigma_t^*} \qquad \text{(E-1)}$$

The asterisks denoting transformed variables will not be used in subsequent discussions. It will be assumed, however, that in the discussions transformed stress and time is meant.

A number of other assumptions are implicit in the discussion above. First, it is assumed that the devices have been selected at random from a manufacturing process. Second, it is assumed that measurement error is very small relative to the measurement of the stress levels. Third, it is assumed that the dominant failure mechanism is being accelerated and that this dominant failure mechanism does not change over the extrapolation range. A discontinuity in either the cumulative percent failure curve or the acceleration curve may be indicative that true acceleration is not being considered. The linear approximations to the nonlinear curve may be studied in the same way that the linear curve has been studied above.

The statistical model mentioned above has not yet been tied to the actual physical degradation process. This is done by assuming that there is a predominant reaction among all the complex chemical reactions which could be taking place during degradation. This predominant reaction may be characterized by some equation which allows the degradation rate observed at high stress to be related to that at low stress.

The analysis is based on the assumption that the Arrhenius equation adequately relates reaction rate to temperature. If Q is some parameter which indicates the extent of degradation then the rate equation will be

$$\frac{dQ}{dt} = R(T) = e^{A-B/T}$$

where T is absolute temperature and A and B are constants. Integrating from some initial time t_o to any later time t, and assuming R(T) is independent of time

$$\int_{Q_0}^{Q} dQ = \int_{t_0}^{t} R(T)\, dt$$

or

$$Q - Q_0 = R(T)\ (t-t_0)$$

Substituting for R(T) and taking the log of both sides we have

$$\ell n\ (Q - Q_0) = A - B/T + \ell n\ (t - t_0)$$

or (assuming for the sake of simplicity that $t_0 = 0$),

$$\frac{1}{T} = \frac{1}{B}\ell n\, t + \frac{A - \ell n\ (Q - Q0)}{B}$$

Letting

$$\frac{A - \ell n\ (Q - Q_0)}{B} = C$$

where C is a constant the equation relating temperature and time for a fixed amount of degradation is given below. This equation is referred to as the acceleration equation.

$$\frac{1}{T} = \frac{1}{B}\ \ell nt + C$$

Using logarithms to the base 10, we would have

$$\frac{1}{T} = \frac{2.303}{B}\ \log_{10} t + C \qquad \text{(E-2)}$$

Thus if we were to plot 1/T versus $\log_{10} t$, the slope, m, would be equal to 2.303/B. Furthermore,

$$B = \frac{q E_A}{k}$$

where:

q = electron charge, 1.592×10^{-19} coulombs

E_A = activation energy (electron volts)

k = Boltzmann's constant, 1.38×10^{-23} Joules $°C^{-1}$

Having determined the slope of (2), E_A may be calculated:

$$m = \frac{2.303}{B} = \frac{2.303k}{qE_A}$$

or

$$E_A = \frac{2.303k}{qm} = \frac{1.996 \times 10^{-4}}{m} \text{ eV} \qquad \text{(E-3)}$$

All that has been done above is to assume a simple rate equation and to derive a relation between 1/T and $\log_{10} t$. Numerous investigators have found that life test data indicates that the relation between temperature and time to failure is of the form $1/T = a \log_{10} t + b$, supporting the assumptions that often the numerous complex reactions taking place may be considered as one reaction, that the Arrhenius equation adequately describes this combination of reactions, and that it may be used to relate high stress results to low stress results.

Next a procedure is described which is used to determine the acceleration curves for fixed stress. First the cumulative percent failures versus time for each level of stress is plotted to see if the lognormal distribution is indicated. A least square fit is made of each linear section of the curve if there is a discontinuity. Some cumulative percent number is selected and the time to produce this percent failure calculated from the least square line. A point is obtained for each stress level and these are plotted as 1/T (effective temperature) versus time. The resulting 1/T versus $\log_{10} t$ points are fitted by least squares. The resulting curve is the acceleration curve for a given cumulative percent failure. The slope of the acceleration curve is available from the least square line and is used in calculating activation energy and acceleration factors.

For step stress tests the cumulative percent failure versus stress level is plotted to determine if a normal distribution is indicated. If indicated, a least square fit of the points is made. Next a certain cumulative percent failure is selected and the stress necessary to produce that percent failure determined. One point is obtained from each step stress test. These are plotted as 1/T (effective temperature) versus time to obtain an acceleration curve for the step stress data.

Plotting a normal cumulative distribution function on probability paper will give a straight line. The cumulative percent failure axis, however, is not linear. For ease in curve fitting and analysis, the cumulative percent failure points are converted to the appropriate "probit" value, λp, since the probit scale on normal probability paper is linear. The regression equations obtained from the test data are then expressed in probits. A short table of probit values for some cumulative percent points is given in Table E-1. A more complete table can be found in Reference 56. Additional information about the normal distribution and probit values can be found in Reference 57.

The constant stress tests will provide plots of cumulative percent failure versus $\log_{10} t$ and the step stress tests will provide plots of cumulative percent failure versus 1/T (°K). Converting these cumulative percent failure points to probability units and fitting a least square line will yield an equation of the form

$$\lambda^{(1)}_p = a_1 + b_1 \log_{10} t \qquad \text{(E-4)}$$

or

$$\lambda^{(2)}_p = a_2 + b_2 \times 10^3 \left(\frac{1}{T}\right) \qquad \text{(E-5)}$$

The superscripts in Equations (E-4) and (E-5) are used here to avoid confusing the fixed stress and step stress data. These superscripts will not be used in Section VI since each equation is clearly described. The terms b_1 and $b_2 \times 10^3$ are reciprocals of standard deviations G_t and G_s respectively, shown in Figure E-2. It has been shown in Equation (E-1) that σ_t and σ_s are related by the equation $\sigma_s/\sigma_t = \tan\theta = m$. Knowing these σ values allows the comparison of the fixed and step stress results.

An example is now used to illustrate the use of some of the equations mentioned in this Appendix. Suppose the following regression equations are derived from the hypothetical step stress data presented graphically in Figure E-3.

$$\lambda p = 23.0 - 10.0 \frac{1000}{T} \quad \text{(8 hr/step)} \qquad \text{(E-6)}$$

Table E-1. Probit Values for Selected Cumulative Percent Points

Cumulative Percent	Probit Value
5	3.36
10	3.72
15	3.96
20	4.16
25	4.33
30	4.48
35	4.61
40	4.75
45	4.87
50	5.00
55	5.12
60	5.25
65	5.39
70	5.50
75	5.67
80	5.84
85	6.04
90	6.28
95	6.65

$$\lambda p = 23.7 - 10.0 \frac{1000}{T} \quad \text{(16 hr/step)} \tag{E-7}$$

$$\lambda p = 25.1 - 10.0 \frac{1000}{T} \quad \text{(64 hr/step)} \tag{E-8}$$

The stress necessary to produce 50% failure in the 8 hour/step stress data will be calculated. Referring to the probit listing in Table E-1, the probit value corresponding to 50% failure is 5.00, so substituting in Equation (E-6),

$$5.00 = 23.0 - 10.0 \frac{1000}{T}$$

or

$$T = 555°K \ (= 272°C)$$

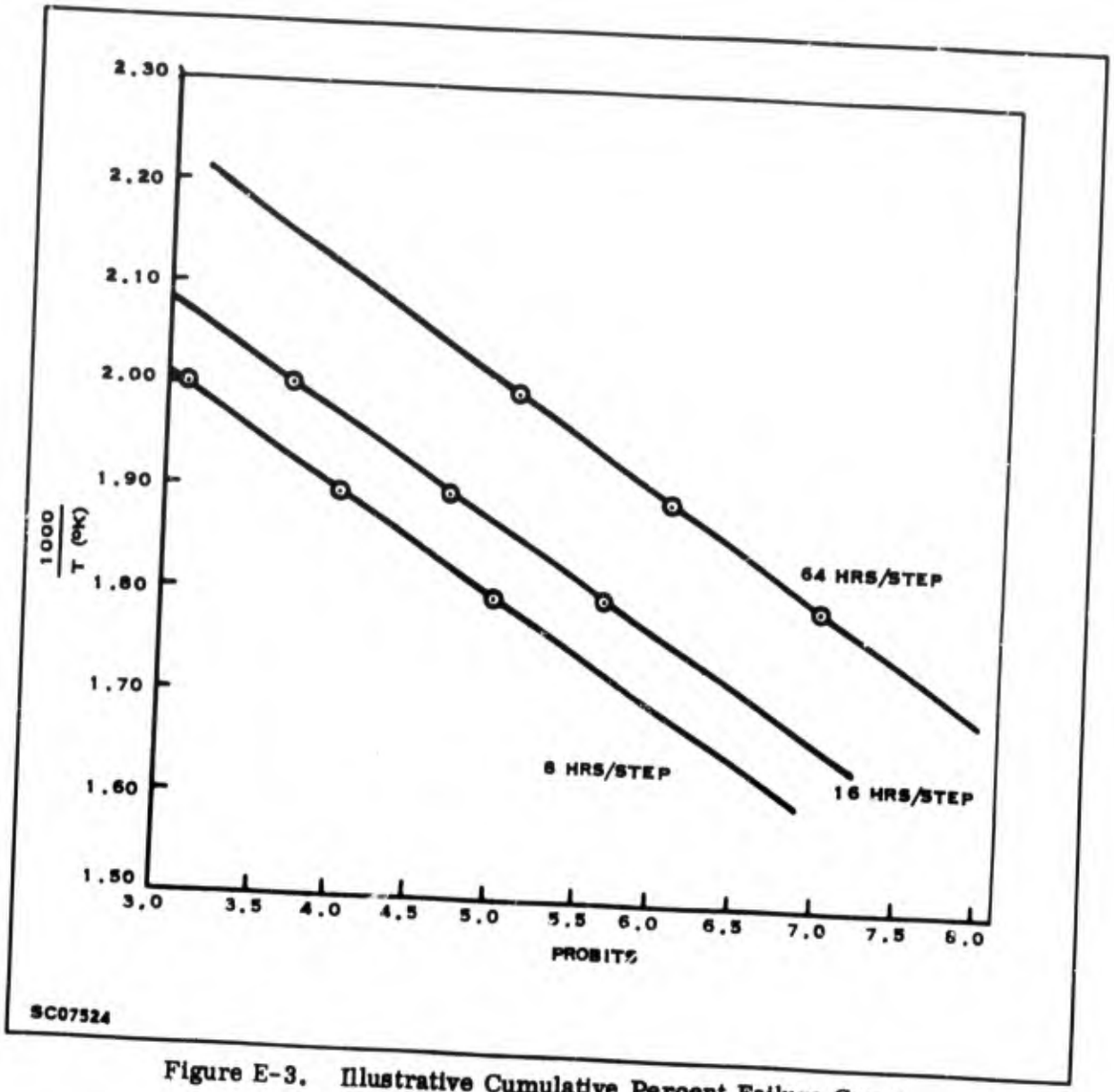

Figure E-3. Illustrative Cumulative Percent Failure Curve

Thus according to the 8 hr/step stress results, 50% failure occurs at 272°C. Conversely, if it were desired to calculate the cumulative percent failure of the 8 hr/step stress tests up to a temperature of 272°C, Equation (E-6) could be used to solve for λp in probits and thus connected to cumulative percent failure as noted in Equation (E-6), the standard deviations of these normal distributions are simply the reciprocals of the coefficients of the 1/T term. In this case the standard deviation, G_s, of these three cumulative percent failure curves would be $1/(10 \times 10^3) = 1.0 \times 10^{-4}$.

The temperature for 50% failure on each of the 3 step stress tests is plotted in Figure E-4. A least square fit to these points is the acceleration curve,

$$\frac{1000}{T} = 1.60 + 0.230 \log_{10} t$$

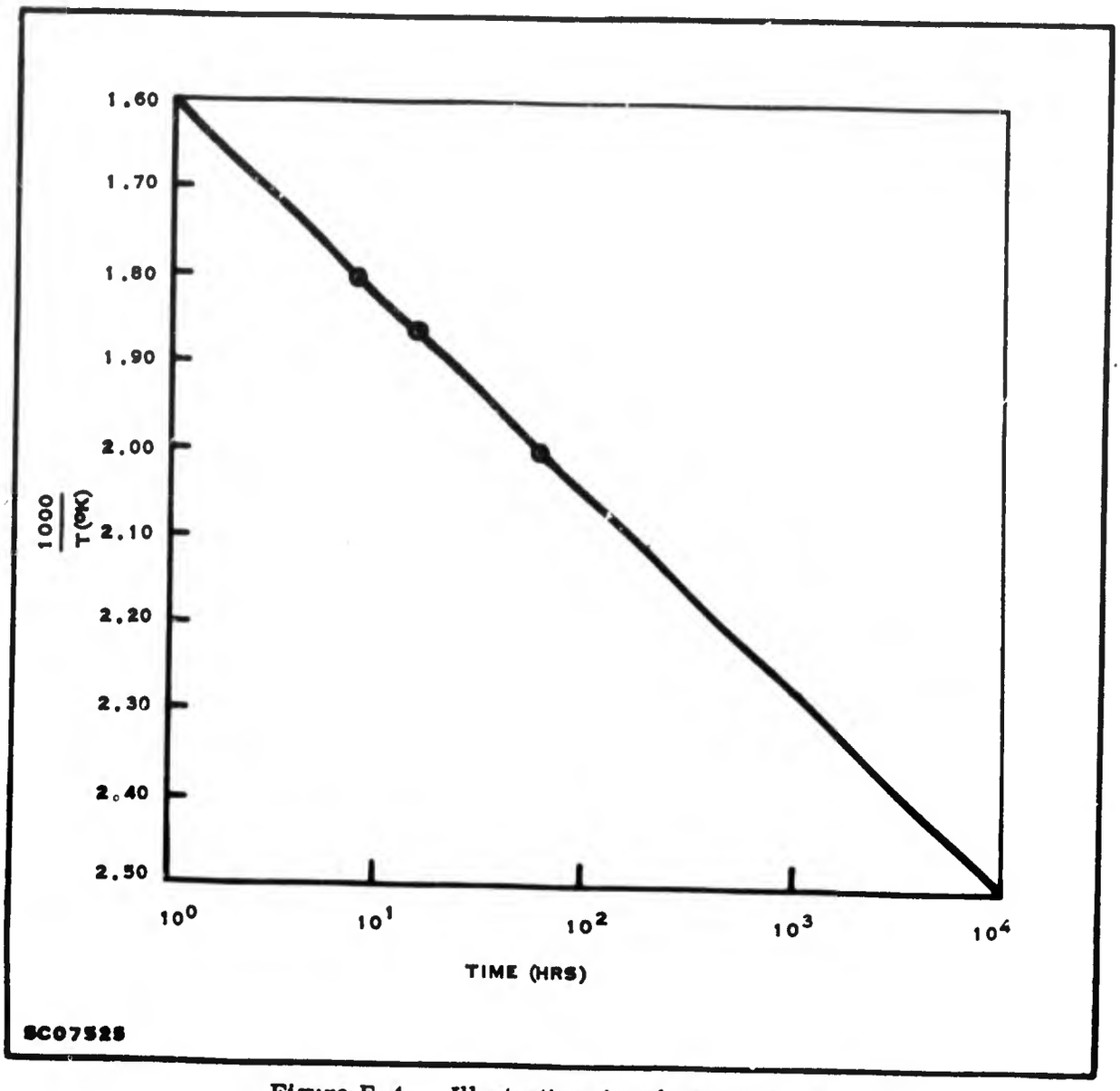

Figure E-4. Illustrative Acceleration Curve

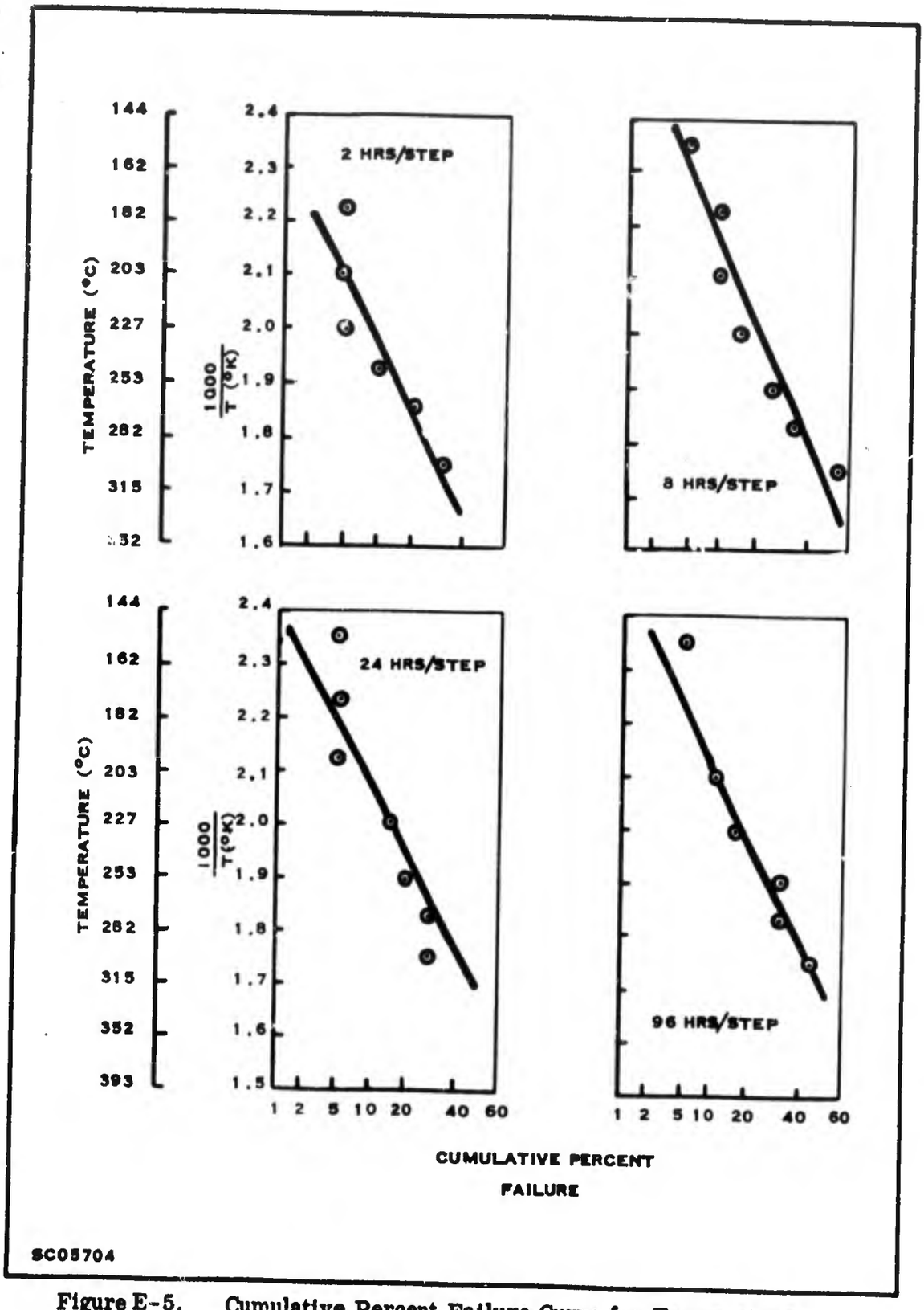

Figure E-5. Cumulative Percent Failure Curve for Temperature Step Stress Test (Main Test Program)

APPENDIX F

TABULATIONS OF

SCREENING RESULTS

APPENDIX F

TABULATIONS OF SCREENING RESULTS

INTRODUCTION

This appendix contains the number codes to identify parameters used in the computer program SERF and the results of using the computer program SERF to isolate the preindicators of later failure on the high stress tests. Also included are a few tables containing some information about the non-normal distributions and the probability of misclassifications in normal and non-normal situations. The probabilities of misclassification were calculated using the linear discriminant analysis computer program (LINDA).

The parameters used throughout the contract are listed in Table F-1 and F-2 together with number codes used in the computer program SERF to identify the parameters. Again the reader is reminded that parameters 11 through 15 (Table F-1) which were read initially and after test completion are not the same parameters as parameters 11 through 15 (Table F-2) used for the data at the various readout intervals for delta change of parameters 1 through 5 respectively.

The results of using the computer program SERF to isolate the preindicators of later failure on the high stress matrix (life) test of the Main Test Program, are contained in Tables F-3 through F-12. A detail explanation of how to read these tables is in Section VII-4.

Tables F-12 through F-17 contain information about the distributions generated and the probabilities of misclassification in the study of the applicability of linear discriminant analysis to non-normal distributions. Explanation of these tables will be found in Section VII-6b.

Table F-1. Electrical Parameters Used During the Contract

Number Code	Parameter	Conditions
Par. 1	I_{CEO}	V_{CE} = 30 V
Par. 2	I_{CEO}	V_{CE} = 70 V
Par. 3	I_{CBO}	V_{CB} = 30 V
Par. 4	I_{CBO}	V_{CB} = 70 V
Par. 5	I_{EBO}	V_{EB} = 5 V
Par. 6	I_{EBO}	V_{EB} = 8 V
Par. 7	h_{FE}	V_{CE} = 5 V, I_C = 5 mA
Par. 8	h_{FE}	V_{CE} = 5 V, I_C = 1 A
Par. 9	$V_{BE(sat)}$	I_B = 200 mA, I_C = 1 A
Par. 10	$V_{CE(sat)}$	I_B = 200 mA, I_C = 1 A
Par. 11*	I_{CBO}	V_{CB} = 3 V
Par. 12*	I_{CBO}	V_{CB} = 15 V
Par. 13*	I_{CBO}	V_{CB} = 150 V
Par. 14*	BV_{CBO}	I_C = 100 μA
Par. 15*	BV_{EBO}	I_E = 100 μA

* Special parameters read initially and at final step.

Table F-2. Description of Parameters Used at Each Readout Interval for Screening with SERF Program

Parameters (Number Code)	Description
1 through 10	Same as those in Table F-1
11 through 20	Delta change of parameters 1 through 10 respectively: i.e., parameter 11 is the delta change in parameter 1, etc.
21 through 30	Percent change of parameters 1 through 10 respectively: i.e., parameter 21 is the percent change in parameter 1, etc.

Table F-3. Screening Results for 200°C Temperature Storage Fixed Stress Test (Main Test Program)

Screening Step	Screening Parameter	Number Devices	Number Failures	Number Failures Removed	Number Failures Remaining	Number Good	Number Good Removed	e	e*
Initial Readout									
1-1	8	93	11	1	10	82	0	8.45	0.55
1-2	9	92	10	1	9	82	0		
1-3	5	91	9	1	8	82	2		
1-4	10	88	8	1	7	80	2		
1-5	11	85	7	1	6	78	2		
								3.84	0.69
2 hr Readout Interval									
2-1	11	92	10	2	8	82	1	6.13	0.60
2-2	8	89	8	1	7	81	0		
2-3	26	88	7	1	6	81	1		
2-4	10	86	6	1	5	80	2		
2-5	15	83	5	1	4	78	2		
								4.60	0.77
8 hr Readout Interval									
3-1	8	92	10	1	9	82	0	9.20	0.55
3-2	9	91	9	1	8	82	0		
3-3	4	90	8	1	7	82	1		
3-4	16	88	7	1	6	81	1		
3-5	10	86	6	1	5	80	2		
								5.11	0.73
24 hr Readout Interval									
4-1	12	92	10	2	8	82	1	6.13	0.60
4-2	9	89	8	1	7	81	0		
4-3	14	88	7	1	6	81	1		
4-4	6	86	6	1	5	80	2		
4-5	7	83	5	1	4	78	2		
								4.60	0.77
96 hr Readout Interval									
5-1	16	92	10	2	8	82	0	9.20	0.60
5-2	13	90	8	2	6	82	1		
5-3	17	87	6	2	4	81	1		
5-4	9	84	4	1	3	80	0		
5-5	12	83	3	1	2	80	1		
								6.69	0.88
264 hr Readout Interval									
6-1	17	89	7	3	4	82	0	12.71	0.72
6-2	5	86	4	1	3	82	0		
6-3	8	85	3	1	2	82	0		
6-4	13	84	2	1	1	82	1		
6-5	1	82	1	1	0	81	1		
								9.88	0.99
432 hr Readout Interval									
7-1	7	87	5	3	2	82	0	17.40	0.80
7-2	6	84	2	1	1	82	2		
7-3	5	81	1	1	0	80	2		
								9.66	0.98
600 hr Readout Interval									
8-1	6	84	2	1	1	82	0	42.00	0.75
8-2	1	83	1	0	1	82	1		
8-3	1	82	1	0	1	81	1		
8-4	1	81	1	0	1	80	1		
8-5	1	80	1	0	1	79	1		
								8.40	0.73

Table F-4. Screening Results for 250° Temperature Storage Fixed Stress Test (Main Test Program)

Screening Step	Screening Parameter	Number Devices	Number Failures	Number Failures Removed	Number Failures Remaining	Number Good	Number Good Removed	e	e*
Initial Readout									
1-1	15	95	48	5	43	47	0	1.97	0.55
1-2	7	90	43	6	37	47	1		
1-3	6	83	37	5	32	46	2		
1-4	7	76	32	4	28	44	1		
1-5	8	71	28	2	26	43	1		
								1.61	0.68
2 hr Readout Interval									
2-1	10	89	42	9	33	47	2	1.73	0.59
2-2	7	78	33	6	27	45	1		
2-3	20	71	27	3	24	44	0		
2-4	27	68	24	3	21	44	0		
2-5	8	65	21	2	19	44	0		
								1.87	0.75
8 hr Readout Interval									
3-1	7	85	38	7	31	47	1	1.95	0.58
3-2	15	77	31	6	25	46	1		
3-3	10	70	25	6	19	45	2		
3-4	17	62	19	3	16	43	0		
3-5	16	59	16	2	14	43	0		
								1.91	0.77
24 hr Readout Interval									
4-1	7	81	34	5	29	47	1	1.98	0.57
4-2	8	75	29	3	26	46	0		
4-3	9	72	26	3	23	46	0		
4-4	10	69	23	2	21	46	0		
4-5	12	67	21	2	19	46	1		
								2.10	0.70
96 hr Readout Interval									
5-1	16	79	32	7	25	47	0	2.46	0.61
5-2	6	72	25	5	20	47	2		
5-3	4	65	20	3	17	45	1		
5-4	21	61	17	2	15	44	0		
5-5	7	59	15	2	13	44	1		
								2.03	0.75
264 hr Readout Interval									
6-1	16	74	27	7	20	47	1	2.39	0.62
6-2	27	66	20	3	17	46	0		
6-3	12	63	17	2	15	46	0		
6-4	7	61	15	2	13	46	1		
6-5	7	58	13	3	10	45	1		
								2.32	0.79
432 hr Readout Interval									
7-1	17	68	21	2	19	47	0	3.23	0.55
7-2	25	66	19	2	17	47	0		
7-3	27	64	17	2	15	47	0		
7-4	12	62	15	2	13	47	1		
7-5	12	59	13	2	11	46	1		
								2.69	0.72
600 hr Readout Interval									
8-1	20	65	18	4	14	47	0	3.61	0.61
8-2	16	61	14	3	11	47	1		
8-3	27	57	11	2	9	46	0		
8-4	13	55	9	2	7	46	1		
8-5	19	52	7	2	5	45	1		
								2.93	0.83
768 hr Readout Interval									
9-1	27	57	10	2	8	47	0	5.70	0.60
9-2	15	55	8	2	6	47	1		
9-3	13	52	6	1	5	46	0		
9-4	9	51	5	1	4	46	1		
9-5	26	49	4	1	3	45	1		
								3.99	0.82

Table F-5. Screening Results for 300°C Temperature Storage Fixed Stress Test (Main Test Program)

Screening Step	Screening Parameter	Number Devices	Number Failures	Number Failures Removed	Number Failures Remaining	Number Good	Number Good Removed	e	e*
Initial Readout									
1-1	6	99	87	56	31	12	0	1.13	0.82
1-2	15	43	31	24	7	12	3		
1-3	1	16	7	5	2	9	2		
1-4	7	9	2	2	0	7	0		
								1.07	0.79
2 hr Readout Interval									
2-1	5	82	70	46	24	12	1	1.14	0.79
2-2	4	35	24	18	6	11	2		
2-3	27	15	6	3	3	9	0		
2-4	19	12	3	2	1	9	0		
2-5	26	10	1	1	0	9	0		
								1.12	0.88
8 hr Readout Interval									
3-1	5	66	54	37	17	12	1	1.19	0.81
3-2	3	28	17	12	5	11	1		
3-3	11	15	5	3	2	10	0		
3-4	16	12	2	2	0	10	1		
								1.16	0.88
24 hr Readout Interval									
4-1	3	57	41	34	7	12	1	1.35	0.88
4-2	5	22	7	7	0	11	1		
								1.10	0.92
96 hr Readout Interval									
5-1	5	32	20	15	5	12	1	1.50	0.84
5-2	10	16	5	5	0	11	1		
								1.45	0.92
264 hr Readout Interval									
6-1	3	24	12	9	3	12	1	1.80	0.84
6-2	5	14	3	3	0	11	1		
								1.71	0.92
432 hr Readout Interval									
7-1	2	20	8	5	2	12	0	2.50	0.82
7-2	12	15	3	2	1	12	0		
7-3	4	3	1	1	0	12	0		
								2.50	1.00
600 hr Readout Interval									
8-1	18	17	5	3	2	12	1	2.55	0.76
8-2	19	13	2	2	0	11	1		
								2.42	0.92
768 hr Readout Interval									
9-1	3	16	4	2	2	12	0	4.00	0.75
9-2	7	14	2	2	0	12	1		
								3.20	0.96

Table F-6. Screening Results for 15 W Power Operating Fixed Stress Test (Main Test Program)

Screening Step	Screening Parameter	Number Devices	Number Failures	Number Failures Removed	Number Failures Remaining	Number Good	Number Good Removed	e	e*
Initial Readout									
1-1	1	98	5	1	4	93	1	9.80	0.60
1-2	1	96	4	1	3	92	1		
1-3	1	94	3	0	3	91	1		
1-4	1	93	3	0	3	90	1		
1-5	1	92	3	0	3	89	1		
								5.60	0.68
8 hr Readout Interval									
3-1	1	96	3	1	2	93	2	10.66	0.66
3-2	1	93	2	0	2	91	1		
3-3	1	92	2	0	2	90	1		
3-4	2	91	2	0	2	89	1		
3-5	2	90	2	0	2	88	1		
								4.57	0.64
24 hr Readout Interval									
4-1	1	96	3	0	3	93	1	0	0.50
4-2	1	95	3	0	3	92	1		
4-3	1	94	3	0	3	91	1		
4-4	3	93	3	1	2	90	1		
4-5	1	91	2	0	2	89	1		
								5.33	0.64

Screening Step	Screening Parameter	Number Devices	Number Failures	Number Failures Removed	Number Failures Remaining	Number Good	Number Good Removed	e	e*
96 hr Readout Interval									
5-1	22	95	2	1	1	93	0	47.50	0.75
5-2	1	94	1	0	1	93	1		
5-3	2	93	1	0	1	92	1		
5-4	2	92	1	0	1	91	1		
5-5	1	91	1	0	1	90	1		
								9.50	0.73
264 hr Readout Interval									
6-1	4	94	1	1	0	93	9	9.40	1.00
								9.40	1.00
768 hr Readout Interval									
9-1	1	94	1	0	1	93	1	0	0.50
9-2	1	93	1	0	1	92	1		
9-3	1	92	1	0	1	91	1		
9-4	1	91	1	0	1	90	1		
9-5	1	90	1	1	0	89	2		
								13.42	0.97

Table F-7. Screening Results for 37.5 W Power Operating Fixed Stress Test (Main Test Program)

Screening Step	Screening Parameter	Number Devices	Number Failures	Number Failures Removed	Number Failures Remaining	Number Good	Number Good Removed	e	e*
Initial Readout									
1-1	5	97	17	2	15	80	0	5.70	0.56
1-2	7	95	15	1	14	80	0		
1-3	10	94	14	1	13	80	0		
1-4	15	93	13	1	12	80	0		
1-5	3	92	12	1	11	80	1		
								4.89	0.67
2 hr Readout Interval									
2-1	16	91	11	3	8	80	1	6.20	0.63
2-2	17	87	8	2	6	79	0		
2-3	18	85	6	2	4	79	1		
2-4	6	82	4	1	3	78	0		
2-5	10	81	3	1	2	78	0		
								6.76	0.90
8 hr Readout Interval									
3-1	16	91	11	5	6	80	1	6.89	0.75
3-2	10	85	6	2	4	79	1		
3-3	17	82	4	2	2	78	1		
3-4	5	79	2	1	1	77	0		
3-5	20	78	1	1	0	77	0		
								6.50	0.98
24 hr Readout Interval									
4-1	15	90	10	5	5	80	1	7.50	0.72
4-2	13	84	5	2	3	79	1		
4-3	5	81	3	1	2	78	0		
4-4	20	80	2	1	1	78	0		
4-5	8	79	1	1	0	78	1		
								6.92	0.98

Screening Step	Screening Parameter	Number Devices	Number Failures	Number Failures Removed	Number Failures Remaining	Number Good	Number Good Removed	e	e*
96 hr Readout Interval									
5-1	9	87	7	2	5	80	0	12.42	0.65
5-2	17	85	5	2	3	80	0		
5-3	12	83	3	2	1	80	1		
5-4	16	80	1	1	0	79	0		
								10.87	1.00
264 hr Readout Interval									
6-1	17	86	6	2	4	80	0	14.33	0.67
6-2	10	84	4	2	2	80	1		
6-3	5	81	2	1	1	79	0		
6-4	15	80	1	1	0	79	2		
								9.55	0.98
432 hr Readout Interval									
7-1	8	84	4	1	3	80	0	21.00	0.63
7-2	18	83	3	1	2	80	0		
7-3	10	82	2	1	1	80	1		
7-4	1	80	1	0	1	79	1		
7-5	1	79	1	0	1	78	1		
								10.50	0.86
600 hr Readout Interval									
8-1	17	84	4	2	2	80	0	21.00	0.75
8-2	5	82	2	1	1	80	0		
8-3	1	81	1	0	1	80	1		
8-4	1	80	1	0	1	79	1		
8-5	8	79	1	1	0	78	1		
								12.00	0.98
768 hr Readout Interval									
9-1	5	84	4	1	3	80	1	10.50	0.62
9-2	9	82	3	1	2	79	2		
9-3	1	79	2	0	2	77	1		
9-4	1	78	2	0	2	76	1		
9-5	1	77	2	0	2	75	1		
								5.25	0.71

Table F-8. Screening Results for 60 W Power Operating Fixed Stress Test (Main Test Program)

Screening Step	Screening Parameter	Number Devices	Number Failures	Number Failures Removed	Number Failures Remaining	Number Good	Number Good Removed	e	e*
Initial Readout									
1-1	6	99	61	5	56	38	1	1.35	0.53
1-2	14	93	56	3	53	37	0		
1-3	10	90	53	2	51	37	0		
1-4	2	88	51	3	48	37	1		
1-5	5	84	48	1	47	36	0		
								1.42	0.59
2 hr Readout Interval									
2-1	12	57	19	3	16	38	0	3.00	0.58
2-2	28	54	16	3	13	38	1		
2-3	1	50	13	2	11	37	1		
2-4	10	47	11	2	9	36	1		
2-5	13	44	9	1	8	35	1		
								2.20	0.74
8 hr Readout Interval									
3-1	28	51	13	2	11	38	0	3.92	0.58
3-2	3	49	11	2	9	38	1		
3-3	15	46	9	2	7	37	1		
3-4	15	43	7	2	5	36	0		
3-5	19	41	5	1	4	36	0		
								3.20	0.82
24 hr Readout Interval									
4-1	28	49	11	4	7	38	0	4.45	0.68
4-2	24	45	7	2	5	38	0		
4-3	9	43	5	1	4	38	1		
4-4	12	41	4	1	3	37	2		
4-5	1	38	3	0	3	35	1		
								2.96	0.81
96 hr Readout Interval									
5-1	28	46	8	4	4	38	1	4.60	0.74
5-2	10	41	4	1	3	37	1		
5-3	19	29	2	1	2	36	1		
5-4	1	37	2	0	2	35	1		
5-5	1	36	2	0	2	34	1		
								3.13	0.81
264 hr Readout Interval									
6-1	16	41	3	1	2	38	0	13.66	0.67
6-2	28	40	2	1	1	38	0		
6-3	1	39	1	0	1	38	1		
6-4	1	38	1	0	1	37	1		
6-5	1	37	1	0	1	36	1		
								5.46	0.80

Table F-9. Screening Results for 125°C Reverse Bias Fixed Stress Test (Main Test Program)

Screening Step	Screening Parameter	Number Devices	Number Failures	Number Failures Removed	Number Failures Remaining	Number Good	Number Good Removed	e	e*
Initial Readout									
1-1	9	99	52	10	42	47	1	1.73	0.59
1-2	7	88	42	6	36	46	1		
1-3	12	81	36	3	33	45	0		
1-4	15	78	33	3	30	45	0		
1-5	3	75	30	2	28	45	0		
								1.75	0.71
2 hr Readout Interval									
2-1	7	96	49	7	42	47	1	1.71	0.58
2-2	25	88	42	4	38	46	0		
2-3	9	84	38	6	32	46	1		
2-4	3	77	32	2	30	45	0		
2-5	5	75	30	2	28	45	1		
								1.71	0.69
8 hr Readout Interval									
3-1	9	95	48	11	37	47	1	1.81	0.60
3-2	4	83	37	6	31	46	2		
3-3	28	75	31	5	26	44	1		
3-4	1	69	26	2	24	43	0		
3-5	3	67	24	2	22	43	1		
								1.65	0.72
24 hr Readout Interval									
4-1	9	95	48	8	40	47	1	1.75	0.57
4-2	1	86	40	8	32	46	2		
4-3	27	76	32	8	24	44	4		
4-4	18	64	24	7	17	40	1		
4-5	16	56	17	3	14	39	0		
								1.60	0.77
96 hr Readout Interval									
5-1	9	94	47	10	37	47	3	1.53	0.58
5-2	25	81	37	6	31	44	1		
5-3	20	74	31	10	21	43	10		
5-4	10	54	21	2	19	33	0		
5-5	7	52	19	2	17	33	1		
								1.33	0.66
264 hr Readout Interval									
6-1	7	92	45	8	37	47	1	1.81	0.58
6-2	9	83	37	8	29	46	3		
6-3	21	72	29	4	25	43	1		
6-4	25	67	25	4	21	42	1		
6-5	26	62	21	2	19	41	0		
								1.66	0.73
432 hr Readout Interval									
7-1	25	80	33	7	26	47	1	2.12	0.60
7-2	18	72	26	4	22	46	1		
7-3	9	67	22	3	19	45	1		
7-4	1	63	19	4	15	44	4		
7-5	3	55	15	2	13	40	1		
								1.73	0.72
600 hr Readout Interval									
8-1	25	71	24	6	18	47	2	2.21	0.61
8-2	1	63	18	2	16	45	1		
8-3	7	60	16	3	13	44	4		
8-4	11	53	13	2	11	40	1		
8-5	20	50	11	3	8	39	4		
								1.69	0.71
768 hr Readout Interval									
9-1	16	53	6	2	4	47	0	8.83	0.67
9-2	3	51	4	1	3	47	0		
9-3	12	50	3	1	2	47	1		
9-4	16	48	2	1	1	46	1		
9-5	1	46	1	1	0	45	1		
								5.88	0.97

Table F-10. Screening Results for 175°C Reverse Bias Fixed Stress Test (Main Test Program)

Screening Step	Screening Parameter	Number Devices	Number Failures	Number Failures Removed	Number Failures Remaining	Number Good	Number Good Removed	e	e*
Initial Readout									
1-1	1	99	53	18	35	46	4	1.52	0.63
1-2	9	77	35	6	29	42	2		
1-3	13	65	29	5	24	40	2		
1-4	5	58	24	3	21	38	0		
1-5	4	55	21	2	19	38	1		
								1.47	0.72
2 hr Readout Interval									
2-1	21	93	47	15	32	46	3	1.64	0.63
2-2	3	75	32	7	25	43	2		
2-3	19	66	25	5	20	41	1		
2-4	25	60	20	4	16	40	1		
2-5	17	55	16	2	14	39	1		
								1.59	0.77
8 hr Readout Interval									
3-1	16	90	44	13	31	46	3	1.66	0.62
3-2	21	74	31	8	23	43	1		
3-3	19	65	23	6	17	42	2		
3-4	26	57	17	3	14	40	0		
3-5	10	54	14	2	12	40	0		
								1.72	0.80
24 hr Readout Interval									
4-1	25	88	52	9	33	46	1	1.52	0.58
4-2	22	78	33	6	27	45	2		
4-3	3	70	27	5	22	43	2		
4-4	11	63	22	3	19	41	1		
4-5	19	59	19	3	16	40	1		
								1.33	0.68
96 hr Readout Interval									
5-1	25	86	40	13	27	46	3	1.74	0.63
5-2	20	70	27	5	22	43	0		
5-3	27	65	22	6	16	43	2		
5-4	4	57	16	5	11	41	2		
5-5	13	50	11	2	9	39	0		
								1.75	0.82
264 hr Readout Interval									
6-1	16	84	38	9	29	46	2	1.80	0.60
6-2	23	73	29	5	24	44	2		
6-3	11	66	24	3	21	42	0		
6-4	19	63	21	3	18	42	1		
6-5	22	59	18	2	16	41	0		
								1.80	0.74
432 hr Readout Interval									
7-1	21	74	28	10	18	46	5	1.76	0.63
7-2	23	59	18	4	14	41	2		
7-3	3	53	14	2	12	39	0		
7-4	10	51	12	2	10	39	1		
7-5	19	48	10	1	9	38	0		
								1.85	0.76
600 hr Readout Interval									
8-1	21	60	14	6	8	46	2	3.21	0.69
8-2	1	52	8	2	6	44	0		
8-3	5	50	6	1	5	44	0		
8-4	7	49	5	1	4	44	0		
8-5	3	48	4	1	3	44	1		
								3.36	0.86
768 hr Readout Interval									
9-1	19	52	6	1	5	46	0	8.66	0.59
9-2	12	51	5	1	4	46	1		
9-3	11	49	4	1	3	45	1		
9-4	25	47	3	1	2	44	1		
9-5	1	45	2	2	0	43	1		
								5.20	0.96

Table F-11. Screening Results for 225°C Reverse Bias Fixed Stress Test (Main Test Program)

Screening Step	Screening Parameter	Number Devices	Number Failures	Number Failures Removed	Number Failures Remaining	Number Good	Number Good Removed	e	e*
Initial Readout									
1-1	12	100	89	61	28	11	2	1.08	0.76
1-2	4	37	28	22	6	9	3		
1-3	6	12	6	6	0	6	2		
								1.04	0.68
2 hr Readout Interval									
2-1	22	95	84	43	41	11	1	1.10	0.71
2-2	10	51	41	25	16	10	2		
2-3	25	22	16	10	6	8	1		
2-4	15	11	6	5	1	7	2		
2-5	1	3	1	1	0	5	0		
								1.05	0.73
8 hr Readout Interval									
3-1	12	94	83	45	38	11	1	1.10	0.73
3-2	10	48	38	22	16	10	2		
3-3	15	24	16	15	1	8	2		
3-4	3	7	1	1	0	6	0		
								1.06	0.78
24 hr Readout Interval									
4-1	22	91	80	30	50	11	0	1.13	0.69
4-2	6	61	50	29	21	11	2		
4-3	8	30	21	20	1	9	4		
4-4	1	6	1	1	0	5	0		
								1.05	0.73
96 hr Readout Interval									
5-1	4	90	79	43	36	11	2	1.08	0.68
5-2	16	45	36	23	13	9	2		
5-3	13	20	13	10	3	7	1		
5-4	1	9	3	2	1	6	0		
5-5	3	7	1	1	0	6	0		
								1.07	0.78
264 hr Readout Interval									
6-1	4	72	61	19	42	11	1	1.12	0.61
6-2	14	53	42	22	20	11	1		
6-3	3	30	20	17	3	10	4		
6-4	5	9	3	2	1	6	0		
6-5	14	7	1	1	0	6	0		
								1.07	0.73
432 hr Readout Interval									
7-1	4	54	43	26	17	11	2	1.16	0.71
7-2	11	26	17	12	5	9	2		
7-3	15	12	5	3	2	7	1		
7-4	4	8	2	2	0	6	1		
								1.10	0.73
600 hr Readout Interval									
8-1	11	36	25	15	10	11	1	1.35	0.76
8-2	3	20	10	5	5	10	0		
8-3	6	15	5	3	2	10	1		
8-4	1	11	2	2	0	9	1		
								1.28	0.87
768 hr Readout Interval									
9-1	4	23	12	9	3	11	1	1.72	0.83
9-2	11	13	3	2	1	10	0		
9-3	1	11	1	1	0	10	0		
								1.76	0.96

Table F-12. Distributions Generated in Studying Applicability of Linear Discriminate Analysis to Non-normal Distributions

Case (0)	$\underset{\sim}{\mu}^{(1)}$ $\underset{\sim}{\mu}^{(2)}$	$\underset{\sim}{\Sigma}$ (1)	α (2)	$\alpha/2$ (3)	Uniform U Mean	Uniform U Variance (4)	Contaminated U Mean	Contaminated U Variance (5)
1	$\begin{pmatrix}0\\0\end{pmatrix}$ $\begin{pmatrix}2\\2\end{pmatrix}$	$\begin{pmatrix}1 & 0.5\\0.5 & 25\end{pmatrix}$	4.444	2.2222	2.040 -2.000	0.339 0.339	2.110 -1.825	6.870 6.980
2	$\begin{pmatrix}0\\0\end{pmatrix}$ $\begin{pmatrix}2\\2\end{pmatrix}$	$\begin{pmatrix}25 & 2.5\\2.5 & 25\end{pmatrix}$	0.2909	0.1454	0.143 -0.148	0.001 0.001	0.142 -0.162	0.483 0.434
3	$\begin{pmatrix}0\\0\end{pmatrix}$ $\begin{pmatrix}2\\10\end{pmatrix}$	$\begin{pmatrix}25 & 2.5\\2.5 & 25\end{pmatrix}$	4.0404	2.0202	2.003 -2.038	0.014 0.014	1.932 -2.061	6.584 6.989
4	$\begin{pmatrix}0\\0\end{pmatrix}$ $\begin{pmatrix}10\\10\end{pmatrix}$	$\begin{pmatrix}25 & 2.5\\2.5 & 25\end{pmatrix}$	7.2727	3.6363	3.624 -3.649	0.023 0.023	3.747 -3.698	12.777 12.139
5	$\begin{pmatrix}0\\0\end{pmatrix}$ $\begin{pmatrix}2\\2\end{pmatrix}$	$\begin{pmatrix}1 & 1\\1 & 100\end{pmatrix}$	4.0000	2.0000	1.994 -2.006	0.338 0.338	2.069 -1.964	6.447 6.553
6	$\begin{pmatrix}0\\0\end{pmatrix}$ $\begin{pmatrix}2\\2\end{pmatrix}$	$\begin{pmatrix}100 & 10\\10 & 100\end{pmatrix}$	0.0727	0.0363	0.036 -0.037	0^+ 0^+	0.033 -0.041	0.113 0.126
7	$\begin{pmatrix}0\\0\end{pmatrix}$ $\begin{pmatrix}2\\10\end{pmatrix}$	$\begin{pmatrix}100 & 10\\10 & 100\end{pmatrix}$	1.0101	0.5050	0.505 -0.506	0.001 0.001	0.456 -0.580	1.720 1.451
8	$\begin{pmatrix}0\\0\end{pmatrix}$ $\begin{pmatrix}10\\10\end{pmatrix}$	$\begin{pmatrix}100 & 10\\10 & 100\end{pmatrix}$	1.8181	0.9090	0.908 -0.910	0.001 0.001	0.830 -0.944	3.073 3.731
9	$\begin{pmatrix}0\\0\end{pmatrix}$ $\begin{pmatrix}1\\3\end{pmatrix}$	$\begin{pmatrix}25 & 0.5\\0.5 & 1\end{pmatrix}$	25.0505	12.5252			12.390 -12.481	46.509 39.320
10	$\begin{pmatrix}2\\0\end{pmatrix}$ $\begin{pmatrix}1\\3\end{pmatrix}$	$\begin{pmatrix}1 & 0.5\\0.5 & 25\end{pmatrix}$	1.8181	0.9090			1.022	2.885
11	$\begin{pmatrix}0\\0\end{pmatrix}$ $\begin{pmatrix}5\\5\end{pmatrix}$	$\begin{pmatrix}25 & 2.5\\2.5 & 25\end{pmatrix}$	1.8181	0.9090	No Simulation		0.983 -0.858	3.116 2.715
12	$\begin{pmatrix}0\\0\end{pmatrix}$ $\begin{pmatrix}1\\3\end{pmatrix}$	$\begin{pmatrix}25 & 2.5\\2.5 & 25\end{pmatrix}$	1.0101	0.5050			0.526 -0.452	1.679 1.804
13	$\begin{pmatrix}0\\0\end{pmatrix}$ $\begin{pmatrix}1\\3\end{pmatrix}$	$\begin{pmatrix}25 & 2.5\\2.5 & 25\end{pmatrix}$	0.0727	0.0363			0.047 -0.019	0.114 0.112

Table F-13. Normal Distributions Generated to Compare the Applicability of Linear Discriminate Analysis to Non-Normal Distributions

Case (0)	$\underset{\sim}{\mu}^{(1)}$ $\underset{\sim}{\mu}^{(2)}$ (1)	$\underset{\sim}{\Sigma}$	α (2)	$\frac{\alpha}{2}$ (3)	Normal U Mean (4)	Variance
3	$\begin{pmatrix}0\\0\end{pmatrix}$ $\begin{pmatrix}2\\10\end{pmatrix}$	$\begin{pmatrix}25 & 2.5\\ 2.5 & 25\end{pmatrix}$	4.0404	2.0202	1.916 -2.124	3.987 3.987

Table F-14. Comparisons of Probabilities of Misclassification in Normal and Non-Normal Situations (C = 0)*

Case (0)	Normal P(2/1) (1)	P(1/2)	Uniform P(2/1) (2)	P(1/2)	Contaminated P(2/1) (3)	P(1/2)
1	0.147	0.147	0	0	0.173	0.187
2	0.394	0.394	0	0	0.386	0.401
3	0.156	0.156	0	0	0.186	0.147
4	0.089	0.089	0	0	0.107	0.108
5	0.159	0.159	0	0	0.171	0.177
6	0.446	0.446	0	0	0.478	0.438
7	0.309	0.309	0	0	0.329	0.266
8	0.250	0.250	0	0	0.276	0.230
9	0.006	0.006	0	0	0.025	0.020
10	0.249	0.249	0	0	0.241	0.278
11	0.249	0.249	0	0	0.246	0.284
12	0.308	0.308	0	0	0.308	0.306
13	0.446	0.446	0	0	0.429	0.454

*Note: C is defined in Section VII. (Common to Tables F-14 through F-17).

Table F-15. Comparisons of Probabilities of Misclassification in Normal and Non-Normal Situations (C = 2)

Case (0)	Normal P(2/1) (1)	Normal P(1/2) (1)	Uniform P(2/1) (2)	Uniform P(1/2) (2)	Contaminated P(2/1) (3)	Contaminated P(1/2) (3)
1	0.280	0.064	0	0	0.299	0.112
2	0.943	0.017	0	0	0.927	0.024
3	0.283	0.067	0	0	0.318	0.091
4	0.165	0.043	0	0	0.170	0.050
5	0.309	0.067	0	0	0.319	0.096
6	0.999	0.001	1	0	0.991	0.009
7	0.688	0.067	1	0	0.718	0.075
8	0.526	0.079	1	0	0.534	0.084

Table F-16. Comparisons of Probabilities of Misclassification in Normal and Non-Normal Situations (C = 2)*

Case (0)	Normal P(2/1) (1)	Normal P(1/2) (1)	Uniform P(2/1) (2)	Uniform F(1/2) (2)	Contaminated P(2/1) (3)	Contaminated P(1/2) (3)
1	0.458	0.036	0.483	0	0.468	0.056
2	0.999	0.000	1	0	0.993	0.002
3	0.496	0.067	0.529	0	0.513	0.044
4	0.271	0.034	.0	0	0.261	0.031
5	0.500	0.023	0.493	0	0.519	0.036
6	1.000	0	1	0	1.000	0
7	0.932	0.007	1	0	0.934	0.018
8	0.791	0.015	1	0	0.796	0.043

*Note: See Table F-14.

Table F-17. Comparisons of Probabilities of Misclassification in Normal and Non-Normal Situations (C = 3)*

Case (0)	Normal P(2/1) (1)	Normal P(1/2) (1)	Uniform P(2/1) (2)	Uniform P(1/2) (2)	Contaminated P(2/1) (3)	Contaminated P(1/2) (3)
1.	0.800	0.002	1	0	0.826	0.017
2	1.000	0	1	0	1.000	0
3	0.837	0.001	1	0	0.851	0.016
4	0.552	0.002	1	0	0.545	0.012
5	0.841	0.001	1	0	0.816	0.015
6	1.000	0	1	0	1.000	0
7	0.999	0.000	1	0	0.987	0.001
8	0.909	0.000	1	0	0.968	0.011

*Note: See Table F-14.

APPENDIX G

COMPUTER PROGRAMS — SERF AND LINDA

APPENDIX G

COMPUTER PROGRAMS — SERF AND LINDA

For ease of reference th.. ppendix is in two parts. The first part contains a general description of the computer program SERF followed by a flow chart (Figure G-1). The last part contains a discussion of the theory relevant to linear discriminant analysis LINDA.

1. SERF

One of the computer programs written to isolate preindicators of failure and to establish screening criteria is an adaptation of the reliability screening techniques developed by Bevington and Ingle.[48] The SERF program (Screening Efficiency Reliability Factors) described here embodies some of the major features of the Sigma 6 program used by the above authors. The relative screening efficiencies of up to 40 measured parameter values, as well as delta and percent change of these values, a total of 120 parameters on up to 100 components are determined from input data. We use the term parameter in the following discussion to mean any electrical quantity together with the conditions (e.g., time, thermal stress, electrical stress, etc.) under which it is measured.

We may use the electrical parameter data at any readout step to predict the failures which were detected at a later readout step. One group of control cards read in with the measurement data are "failure cards" which identify at which readout step each failure was first detected. All devices which become failures at a later readout step than the readout step at which screening is being done are included, along with the devices, in the sample to be screened.

The optimum screening criterion is derived by maximizing either the screening efficiency

$$e = \frac{\text{\% failures removed}}{\text{\% population removed}}$$

or

$$e^* = 0.5 + 0.5\,(F_f - F_g)$$

where

F_f = fraction of total failures removed

and

F_g = fraction of total good devices removed.

for a fixed number of screening levels for each parameter; the criterion is expressed as a series of truncation levels for the parameters considered in the calculation. Basically the program provides a means of evaluating the predictive efficiency obtainable by using varying parameters and varying test conditions.

We will assume that we are screening n devices ($n \leq 100$) having m parameters ($m \leq 40$). After the input data has been read in, the range of each parameter is partitioned into 20 subintervals (cells) and the two out-of-limits categories added to bring the total number of cells for each parameter to 22. Parameter values for each component are then examined, and the number NT_{ij} of components whose i^{th} parameter value lies in cell j recorded, producing an m x 22 matrix of values. Simultaneously, the number NF_{ij} of later failures "in" each cell is recorded, producing a second m x 22 matrix.

Next, the cumulative number CN_{1jk} (and the number CF_{1jk} of later failures) which would be removed by screening of parameter 1 at the jth lower level and kth upper level ($1 \leq j \leq k \leq 22$) is computed and the resulting 22 x 22 matrices are used to calculate the screening efficiency values

$$E_{1jk} = \left(\frac{CF_{1jk}}{F}\right) \Big/ \left(\frac{CN_{1jk}}{N}\right) \tag{1}$$

or

$$E^*_{1jk} = \frac{1}{2} + \frac{1}{2}\left(\frac{CF_{1jk}}{F} - \frac{CN_{1jk} - CF_{1jk}}{N - F}\right) \tag{2}$$

The maximum value of E_{1jk} (or E^*_{1jk}), $E_{1j_1k_1}$ (or $E^*_{1j_1k_1}$) is calculated and stored along with j_1 and k_1. If the maximum is not unique, the number of components removed is maximized in selecting the optimum screening state (j_1, k_1). This procedure is continued for all m parameters and the maximum value of all these screening efficiencies, $\tilde{E}_{ij_ik_i}$ is calculated and stored, along with i, j_i and k_i. Devices having parameter i values in cells 1 to j_i and k_i to 22 are the screened devices.

The components to be deleted are identified by serial number. The following information is printed:

screening criterion (parameter number and level)

sample size

number screened

number of failures screened

percent of sample removed in screening

percent failures in screened group

percent failures and good present at the end of the previous screening level which were removed by the current screening

cumulative percent of the number of prescreening failures and good which were removed at the end of the current screening

screening efficiency achieved.

The specified termination mode is then examined and the problem terminated if the criterion is satisfied. If not, the parameter data is revised by deletion of the components screened; the data is revised to reflect the number of components and later failures remaining, and a second screening pass initiated.

In summary, the SERF program may be used to select the sequence of screening levels on a set of parameter values which produce the optimum screening efficiency as indicated above. By altering the combinations of parameters and/or failure criteria, information may be extracted concerning the best indicators of specific failure modes. Both failure and parameter are used here in the broadest sense. Any condition of interest may be used to identify elements as "failures"; any condition or quality to which a meaningful numerical value can be assigned may be used as a parameter.

The results of the screening analysis may be used to identify sensitive indicators of particular conditions, or to establish practical screening levels as required. The sequence of screening passes may be terminated at any level in establishing such screens, contingent on the percentage of the failures or total population it is desired to remove.

A number of options are provided to increase the usefulness of the program. Changing the failure criteria will redefine failures and could result in entirely different screening results. By simply changing the "failure cards" the data can be screened again to explore the effects of the new failure criteria.

Screening may be terminated either by specifying the number of screening passes or else by supplying a lower boundary on the screening efficiency below which screening is terminated.

Upper and lower limits for the range of each parameter are used for the 20 cell partitioning as well as the specification of the two out of range cells. A good cell selection will use cells as small as possible to minimize clustering of many parameter values of both good and bad devices in a few cells, preventing clean separation of the outliners. One option for constructing the cells uses the maximum and minimum parameter values as the upper and lower limits. After the parameter values have been distributed among the cells, the cells are examined in sequence starting from both the lowest and highest cell until a cell is detected at each end which contains a parameter value of a good unit. The parameter values which define the lower limit of this low cell and the upper limit of this high cell are used as the new lower and upper limits of the parameter range. A new set of cells is then constructed. Thus in effect the parameter values of the bad units are moved to the out of range cells and the resolution of the cell partitioning increased.

Alternatively the user may specify his own upper and lower limits or else, assuming the parameter values are normally distributed, and the mean and standard deviation of each parameter is computed and $\mu-3\sigma$ is used as the lower limit and $\mu+3\sigma$ used as the upper limit.

Provision has been made to allow screening on any subset of the parameters read in and further to allow specification of a list of parameters to be screened on one at a time and in the order specified.

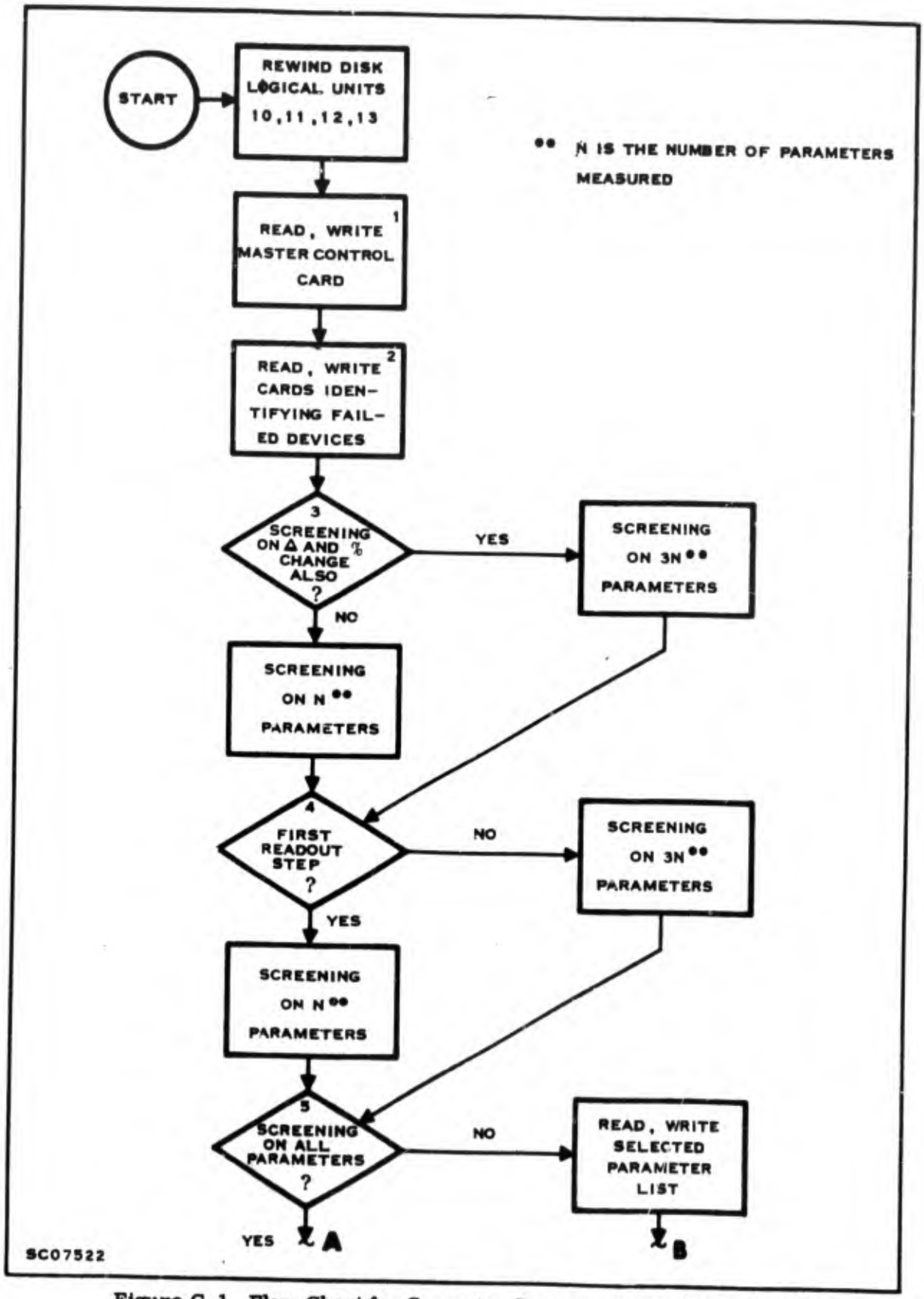

Figure G-1. Flow Chart for Computer Program SERF (Sheet 1 of 9)

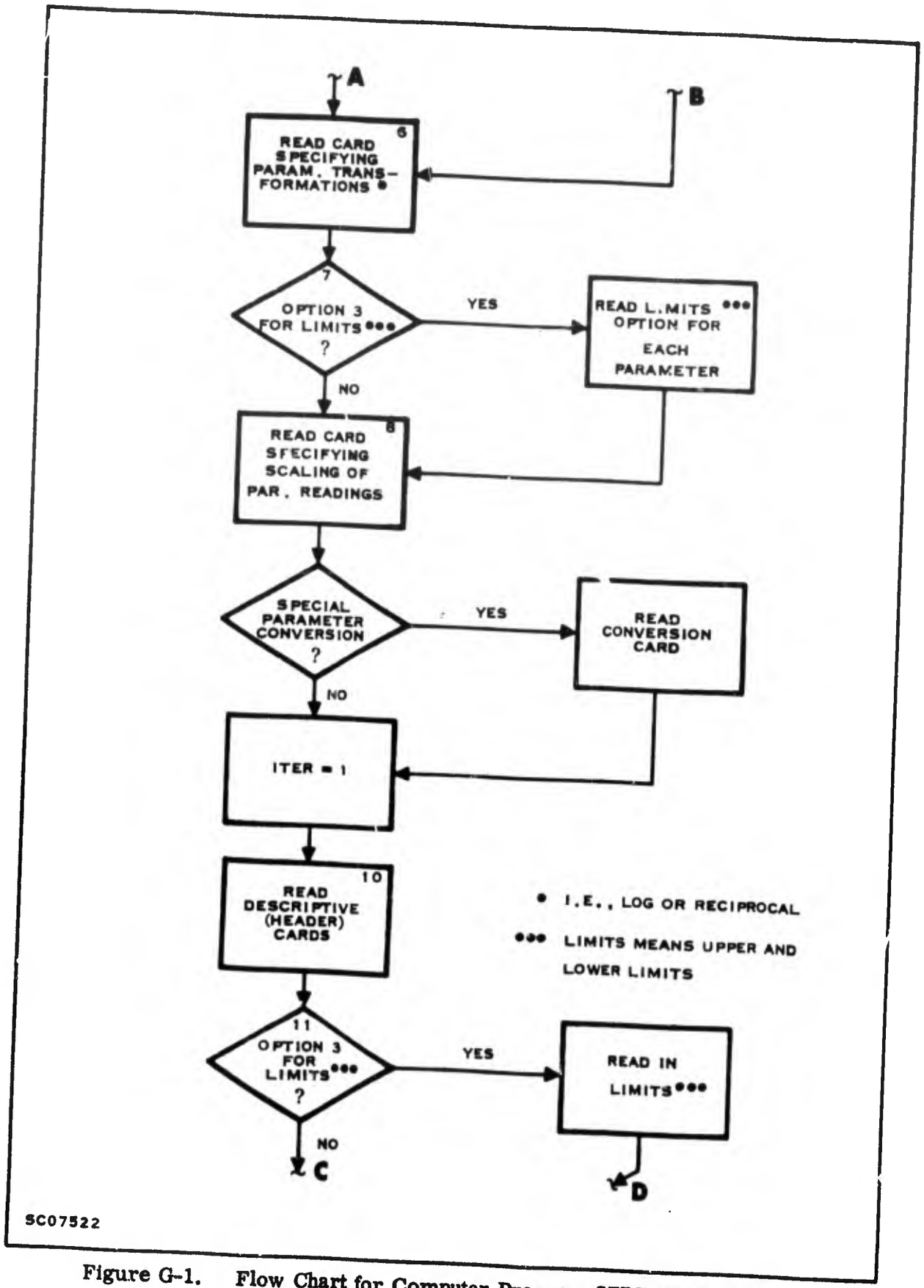

Figure G-1. Flow Chart for Computer Program SERF (Sheet 2 of 9)

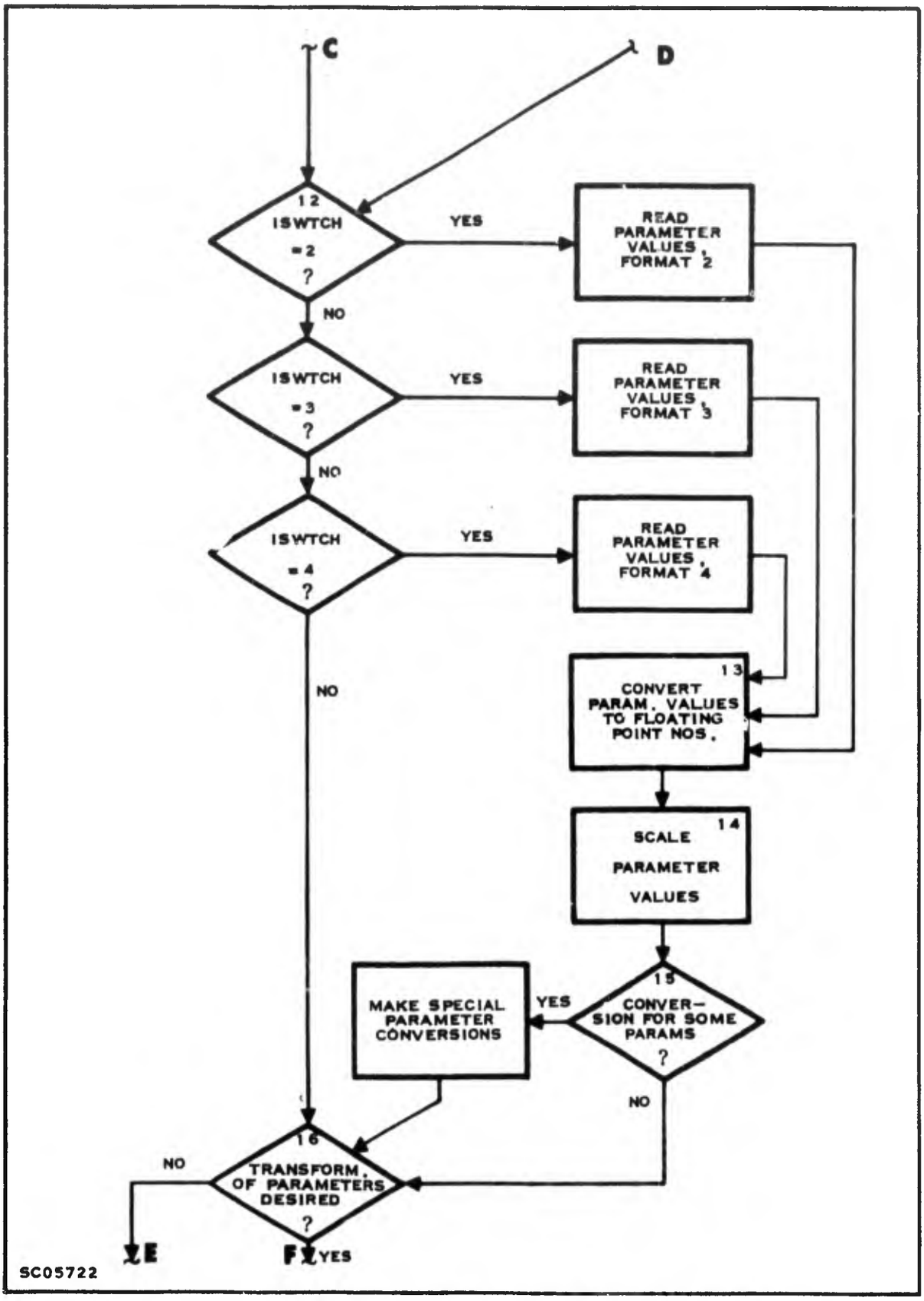

Figure G-1. Flow Chart for Computer Program SERF (Sheet 3 of 9)

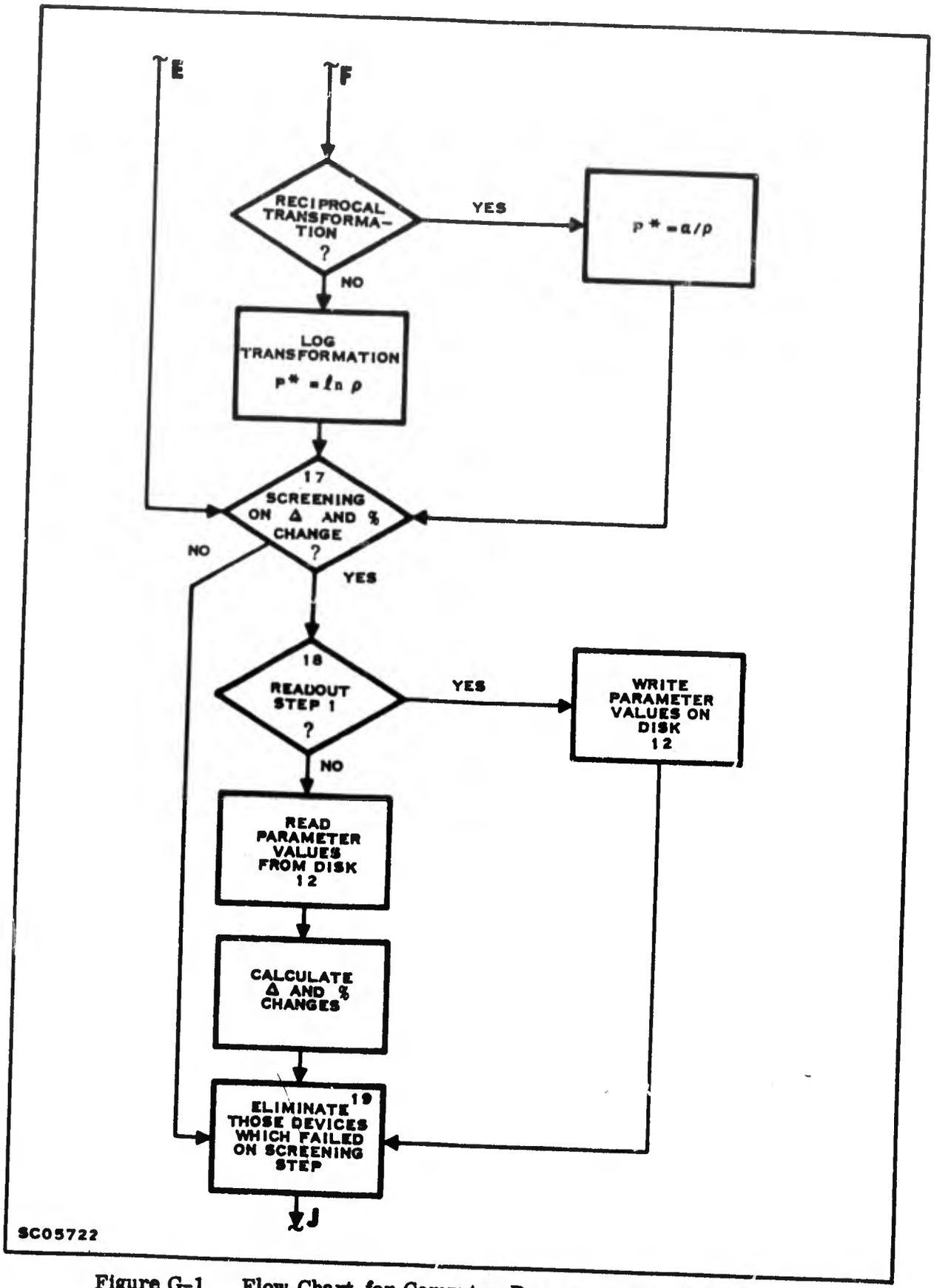

Figure G-1. Flow Chart for Computer Program SERF (Sheet 4 of 9)

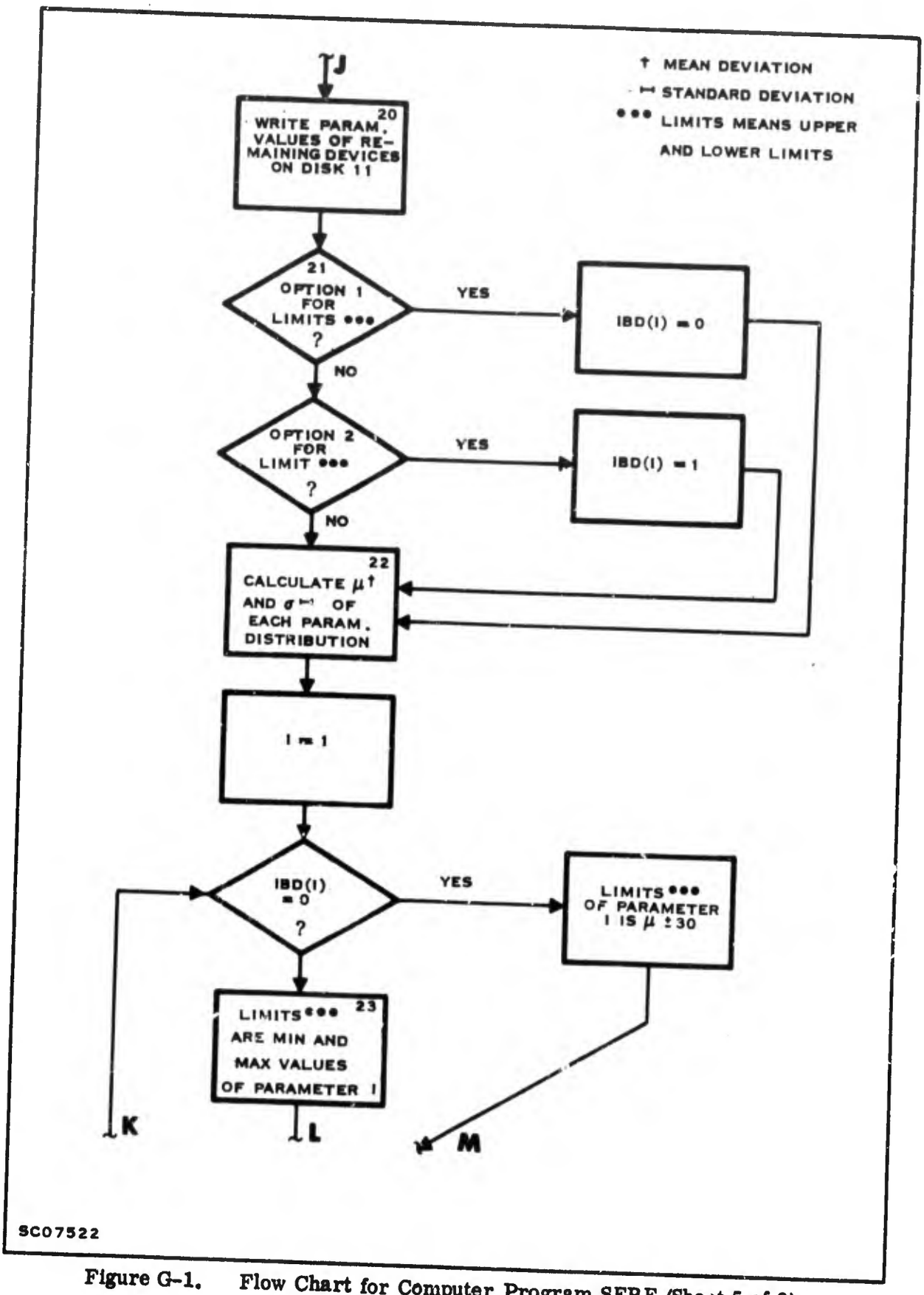

Figure G-1. Flow Chart for Computer Program SERF (Sheet 5 of 9)

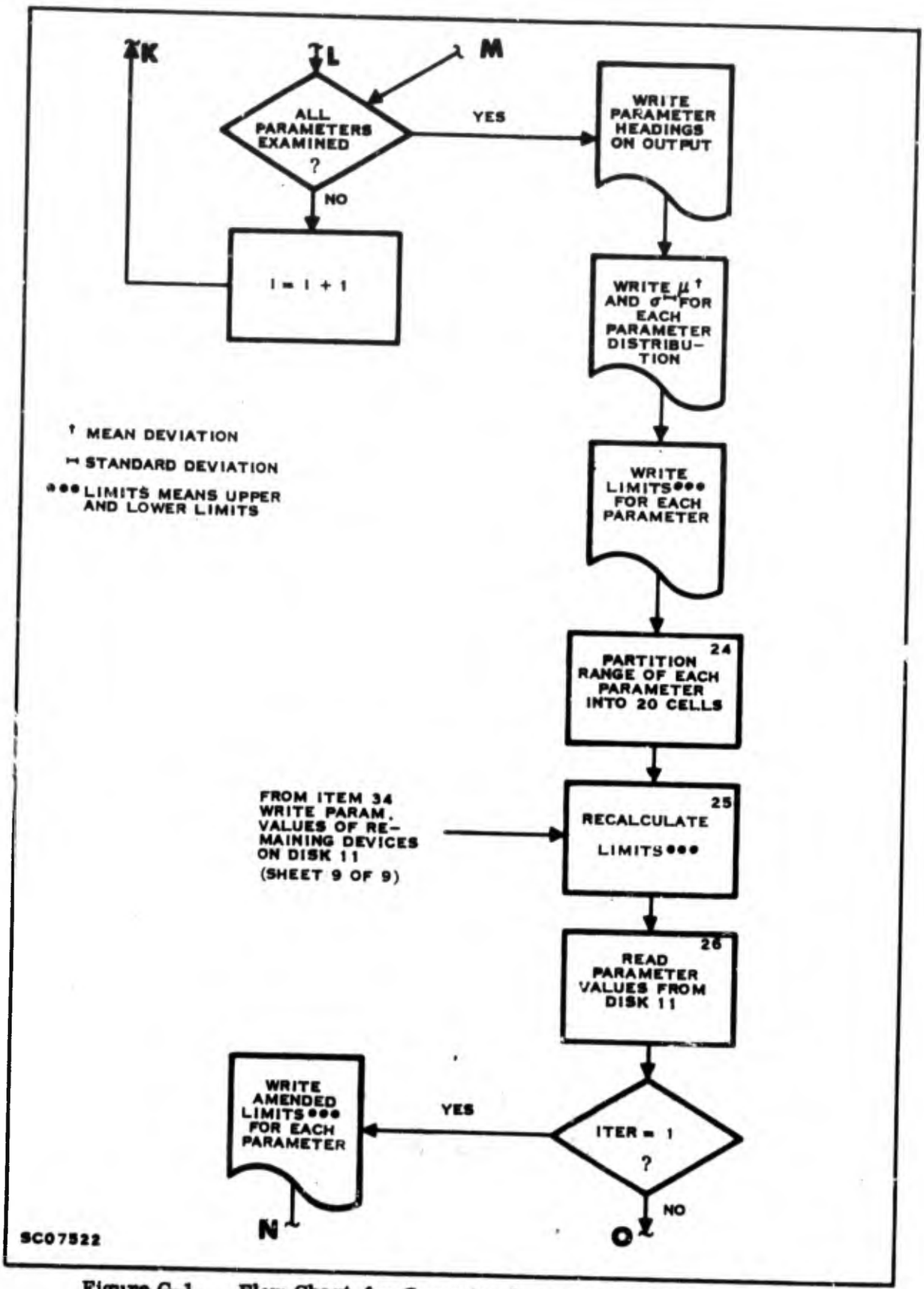

Figure G-1. Flow Chart for Computer Program SERF (Sheet 6 of 9)

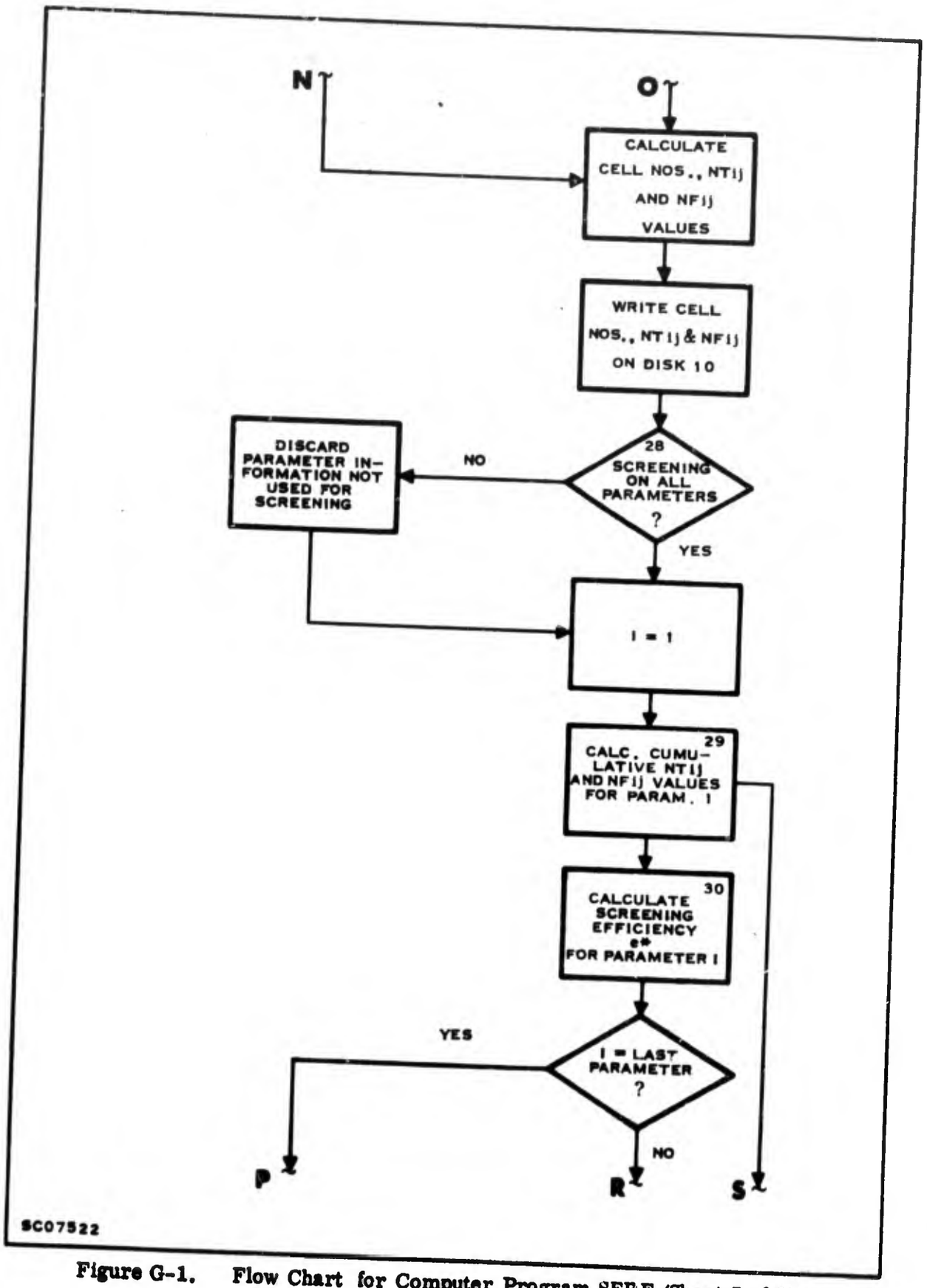

Figure G-1. Flow Chart for Computer Program SERF (Sheet 7 of 9)

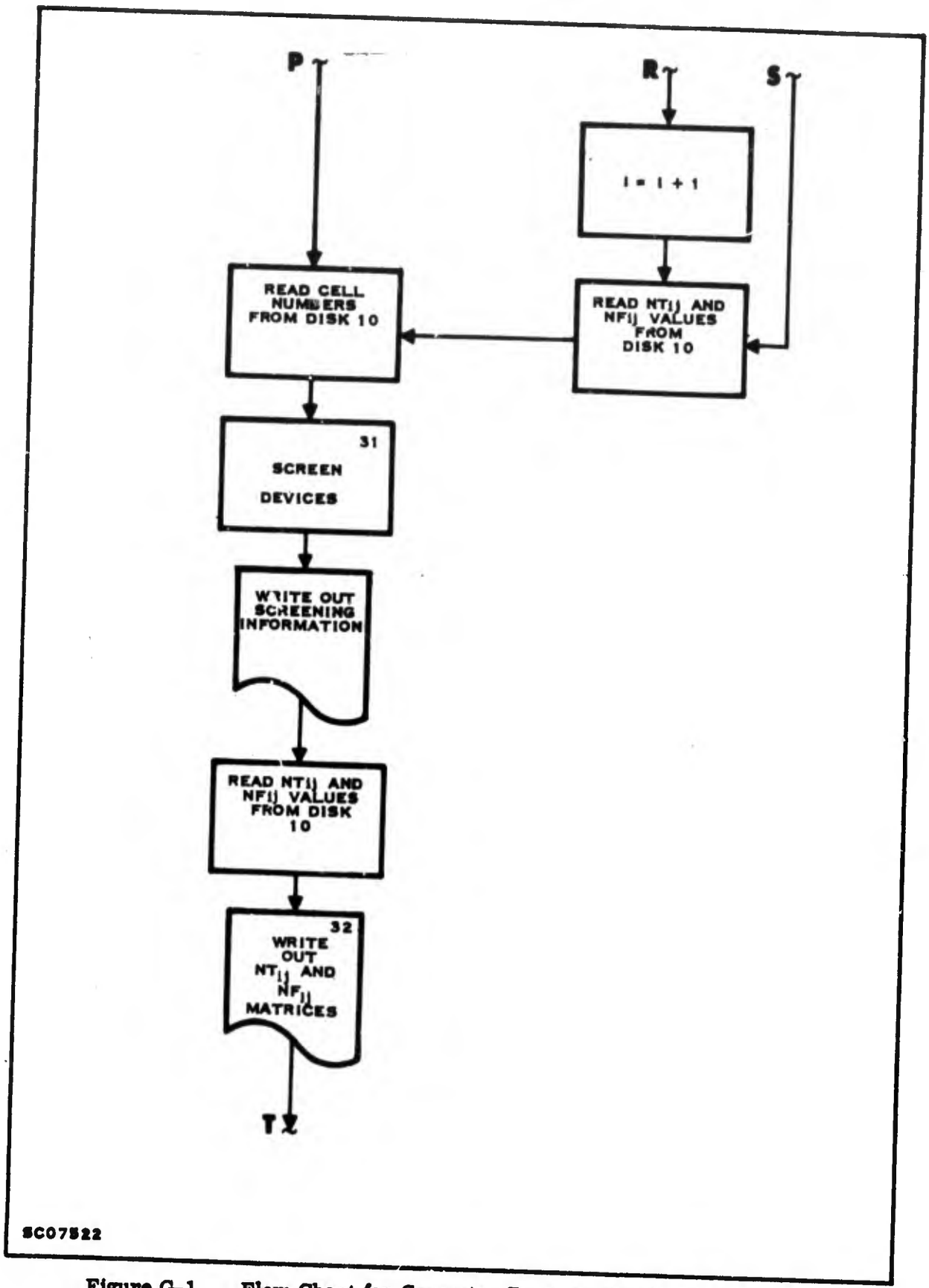

Figure G-1. Flow Chart for Computer Program SERF (Sheet 8 of 9)

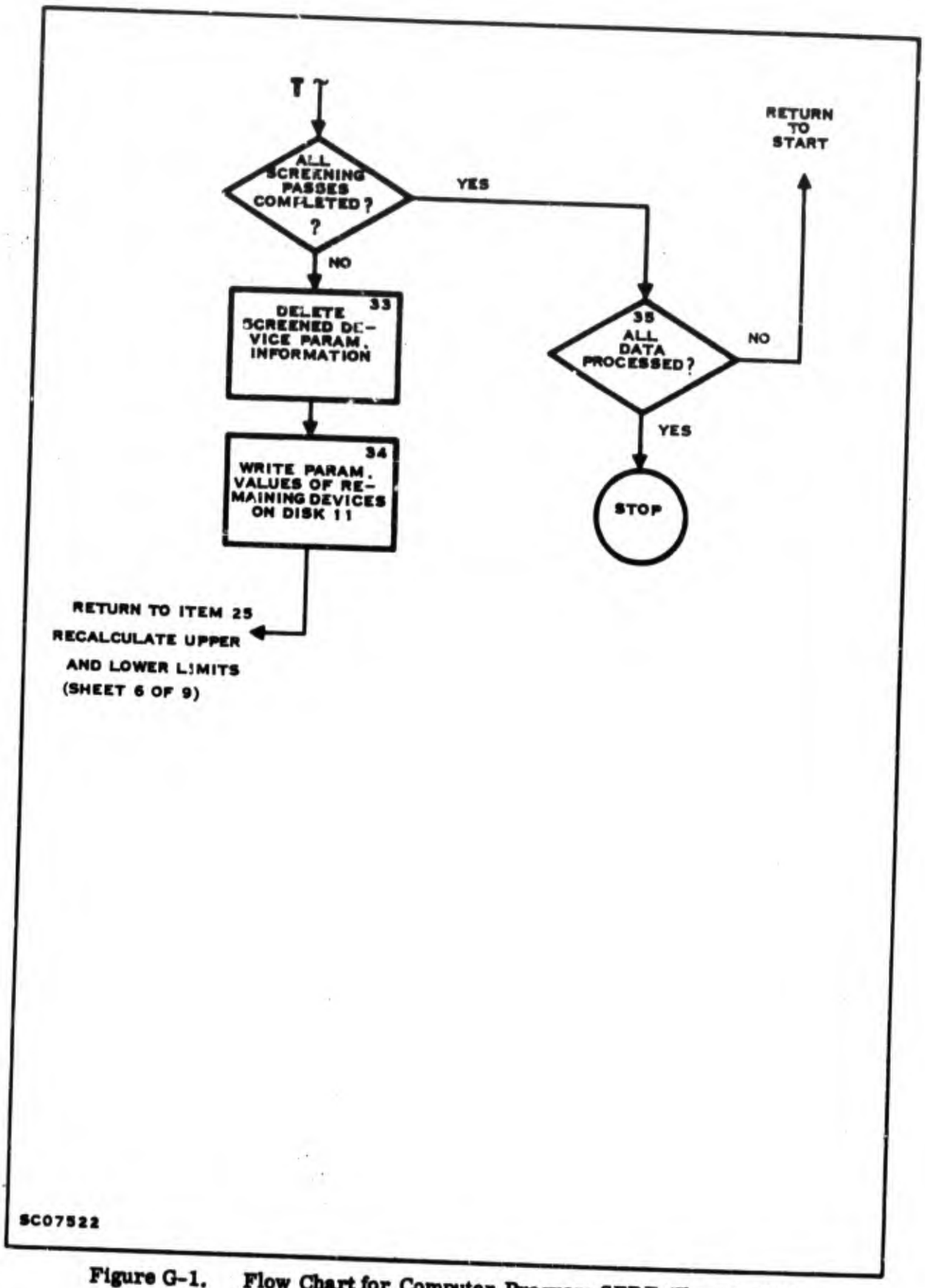

Figure G-1. Flow Chart for Computer Program SERF (Sheet 9 of 9)

2. LINEAR DISCRIMINANT ANALYSIS (LINDA)

In this discussion it is assumed that several parameter measurements be used to predict whether or not a device will perform satisfactorily over a period of time. The problem can be expressed as one of classification [9] where there are two populations, satisfactory and unsatisfactory; it is desired to classify a given device into one of these on the basis of parameter measurements. The theory behind the classification procedure has been worked out for the case where the underlying populations are multivariate normal. The classification criterion turns out to be a linear combination of the elements of the vector of measurements on the device. This is a convenient criterion to employ, and it would be useful to know how the criterion behaves when the underlying populations are non-normal. The assumption is made consistently that the satisfactory and unsatisfactory populations share a common covariance matrix, although, in practice this assumption may be questioned. Another problem of interest is the determination of which variates constitute the best classifiers.

a. Theory

What follows is a summary of the theory given in Reference 9. Let π_1 and π_2 be the two populations into one of which we wish to classify an observation $\underset{\sim}{x}$ (mxl). Assume that π_1 is multivariate normal with mean $\mu^{(1)}$ (mxl) and covariance matrix $\underset{\sim}{\sum}$ (mxm), and that π_2 is multivariate normal with mean $\mu^{(2)}$ (mxl) and covariance matrix $\underset{\sim}{\sum}$(mxm). Let $p_i(\underset{\sim}{x})$, $i = 1, 2$, be the probability density functions associated with π_i, $i = 1, 2$, respectively. Let $R = (R_1, R_2)$ denote a classification rule, i.e., if $\underset{\sim}{x}$ lies in region R_1, we classify $\underset{\sim}{x}$ into π_1, and if $\underset{\sim}{x}$ lies in R_2, we classify $\underset{\sim}{x}$ into π_2.

Let

$$P(2/1, R) = \int^{R_2} P_1(\underset{\sim}{x})\, d\underset{\sim}{x}$$

and

$$P(1/2, R) = \int^{R_1} P_2(\underset{\sim}{x})\, d\underset{\sim}{x}$$

where $dx = dx_1\, dx_2 \ldots\ldots\ldots dx_m$. Then $P(2/1, R)$ is the probability of classifying $\underset{\sim}{x}$ into π_2 when $\underset{\sim}{x}$ is really from π_1, and $P(1/2, R)$ is the probability of classifying $\underset{\sim}{x}$ into π_1 when $\underset{\sim}{x}$ is really from π_2. These are the $P(i/j, R)$ probabilities of misclassification.

Let q_1 and q_2 be the probability that a random observation comes from π_1 and π_2 respectively. Further, let $C(2/1)$ denote the cost of classifying $\underset{\sim}{x}$ into π_2 when $\underset{\sim}{x}$ is really from π_1, and let $C(1/2)$ denote the cost of classifying $\underset{\sim}{x}$ into π_1 when $\underset{\sim}{x}$ is really from π_2. Then for a given classification rule, $R = (R_1, R_2)$, the total expected cost of misclassifying the observation $\underset{\sim}{x}$ is

$$C(2/1)\, q_1\, P(1/2) + C(1/2)\, q_2\, P(1/2).$$

We seek a rule R such that the total expected cost of misclassification is minimized. We must take two cases into consideration: 1) the probabilities of a random observation coming from π_1 or π_2 are known, and 2) these probabilities are not known.

Case 1: Suppose q_1 and q_2 are known. The rule that minimizes the total expected cost of misclassification is

$$R_1 = \left\{ \underset{\sim}{x}: \frac{p_1(\underset{\sim}{x})}{p_2(\underset{\sim}{x})} \geq \frac{q_2\, C(1/2)}{q_1\, C(2/1)} \right\}$$

$$R_2 = \left\{ \underset{\sim}{x}: \frac{p_1(\underset{\sim}{x})}{p_2(\underset{\sim}{x})} < \frac{q_2\, C(1/2)}{q_1\, C(2/1)} \right\}.$$

Note that R can also be expressed as

$$R_1 = \left\{ \underset{\sim}{x}: \log \frac{p_1(\underset{\sim}{x})}{p_2(\underset{\sim}{x})} \geq \log k \right\}$$

$$R_2 = \left\{ \underset{\sim}{x}: \log \frac{p_1(\underset{\sim}{x})}{p_2(\underset{\sim}{x})} < \log k \right\},$$

where $k = q_2 C(1/2) / q_1 C(2/1)$. The classification procedure defined by R is called a Bayes procedure.

Case 2: If q_1 and q_2 are not known, one must look for the class of "admissible" classification procedures, i.e., the class of procedures which cannot be improved upon. It turns out that the class of admissible procedures is identical with the class of Bayes procedures. Hence in the search for a classification rule, one should restrict himself to the class of Bayes procedures. One such Bayes procedure is the minimax procedure. If R* is a classification rule, $r(1, R^*) = C(2/1)\, P(2/1, R^*)$ and $r(2, R^*) = C(1/2)\, P(1/2, R^*)$, then R* is minimax if $\max r(i, R^*)$ is a minimum with respect to all admissible R. The minimax procedure requires that $r(1, R^*) = r(2, R^*)$. Thus our rule is

$$R_1^* = \left\{ \underset{\sim}{x}: \log \frac{p_1(\underset{\sim}{x})}{p_2(\underset{\sim}{x})} \geq \log k \right\}$$

$$R_2^* = \left\{ \underset{\sim}{x}: \log \frac{p_1(\underset{\sim}{x})}{p_2(\underset{\sim}{x})} < \log k \right\},$$

where $\log k = c$ is determined so that $r(1, R^*) = r(2, R^*)$.

In any event we must examine the ratio $p_1(\underset{\sim}{x}) / p_2(\underset{\sim}{x})$. Now

$$p_i(\underset{\sim}{x}) = \frac{1}{(2\pi)^{m/2}\sqrt{|\underset{\sim}{\Sigma}|}} \exp\left[-1/2\,(\underset{\sim}{x} - \underset{\sim}{\mu}^{(i)})'\,\underset{\sim}{\Sigma}^{-1}(\underset{\sim}{x} - \underset{\sim}{\mu}^{(i)})\right], \quad i = 1, 2.$$

$$\text{Thus } \log \frac{p_1(\underset{\sim}{x})}{p_2(\underset{\sim}{x})} = \log \exp \; -1/2\left[(\underset{\sim}{x}-\underset{\sim}{\mu}^{(1)})'\,\underset{\sim}{\Sigma}^{-1}(\underset{\sim}{x} - \underset{\sim}{\mu}^{(1)}) - (\underset{\sim}{x} - \underset{\sim}{\mu}^{(2)})'\,\underset{\sim}{\Sigma}^{-1}(\underset{\sim}{x} - \underset{\sim}{\mu}^{(2)})\right]$$

$$= \underset{\sim}{x}'\,\underset{\sim}{\Sigma}^{-1}(\underset{\sim}{\mu}^{(1)} - \underset{\sim}{\mu}^{(2)}) - 1/2\,(\underset{\sim}{\mu}^{(1)} + \underset{\sim}{\mu}^{(2)})'\,\underset{\sim}{\Sigma}^{-1}\,(\underset{\sim}{\mu}^{(1)} - \underset{\sim}{\mu}^{(2)}) \; .$$

If $U = \underset{\sim}{X}'\,\underset{\sim}{\Sigma}^{-1}\,(\underset{\sim}{\mu}^{(1)} - \underset{\sim}{\mu}^{(2)}) - 1/2\,(\underset{\sim}{\mu}^{(1)} + \underset{\sim}{\mu}^{(2)})\,\underset{\sim}{\Sigma}^{-1}\,(\underset{\sim}{\mu}^{(1)} - \underset{\sim}{\mu}^{(2)})$, it is easy to show that U has a normal distribution with mean $1/2\,\alpha$ and variance α if $\underset{\sim}{x}$ is from π_1, and with mean $-1/2\,\alpha$ and variance α if $\underset{\sim}{x}$ is from π_2, where $\alpha = (\underset{\sim}{\mu}^{(1)} - \underset{\sim}{\mu}^{(2)})\,\underset{\sim}{\Sigma}^{-1}\,(\underset{\sim}{\mu}^{(1)} - \underset{\sim}{\mu}^{(2)})$. Thus probabilities of misclassification are easy to compute. We have

$$P(2/1) = \int_{-\infty}^{c} \frac{1}{\sqrt{2\pi\alpha}}\, e^{-1/2\frac{(u - 1/2\,\alpha)^2}{\alpha}}\, du$$

$$= \int_{-\infty}^{\frac{c-1/2\,\alpha}{\sqrt{\alpha}}} \frac{1}{\sqrt{2\pi}}\, e^{-1/2y^2}\, dy,$$

and

$$P(1/2) = \int_{c}^{\infty} \frac{1}{\sqrt{2\pi\alpha}}\, e^{-1/2\,\frac{(u + 1/2\,\alpha)^2}{\alpha}}\, du$$

$$= \int_{\frac{c + 1/2\,\alpha}{\sqrt{\alpha}}}^{\infty} \frac{1}{\sqrt{2\pi}}\, e^{-1/2\,y^2}\, dy.$$

If q_1 and q_2 are known, $c = \log k = \log q_2 C(1/2) / q_1 C(2/1)$. For the minimax solution we choose c so that

$$C(1/2) \int_{\frac{c + 1/2\,\alpha}{\sqrt{\alpha}}}^{\infty} \frac{1}{\sqrt{2\pi}} e^{-1/2y^2}\, dy = C(2/1) \int_{-\infty}^{\frac{c-1/2\alpha}{\sqrt{\alpha}}} \frac{1}{\sqrt{2\pi}} e^{-1/2\,y^2}\, dy.$$

Of course, in most cases $\underset{\sim}{\mu}^{(1)}$, $\underset{\sim}{\mu}^{(2)}$, and $\underset{\sim}{\Sigma}$ are not known. Hence they must be estimated before the above theory can be applied. Suppose we have a sample,

$$\underset{\sim}{x}_1^{(1)}, \ldots, \underset{\sim}{x}_{N_1}^{(1)},$$

from π_1 and a sample,

$$\underset{\sim}{x}_1^{(2)}, \ldots, \underset{\sim}{x}_{N_2}^{(2)},$$

from π_2. The estimates of $\underset{\sim}{\mu}^{(1)}$ and $\underset{\sim}{\mu}^{(2)}$ are $\overline{\underset{\sim}{x}}^{(1)}$

$$= \frac{1}{N_1} \sum_{i=1}^{N_1} \underset{\sim}{x}_i^{(1)} \quad \text{and} \quad \overline{\underset{\sim}{x}}^{(2)}$$

$$= \frac{1}{N_2} \sum_{i=1}^{N_2} \underset{\sim}{x}_i^{(2)}.$$

An estimate of $\underset{\sim}{\Sigma}$, say $\underset{\sim}{S}$, may be defined by

$$(N_1 + N_2 - 2)\,\underset{\sim}{S} = \sum_{i=1}^{N_1} (\underset{\sim}{x}_i^{(1)} - \overline{\underset{\sim}{x}}^{(1)})\,(\underset{\sim}{x}_i^{(1)} - \overline{\underset{\sim}{x}}^{(1)})'$$

$$+ \sum_{i=1}^{N_2} (\underset{\sim}{x}_i^{(2)} - \overline{\underset{\sim}{x}}^{(2)})\,(\underset{\sim}{x}_i^{(2)} - \overline{\underset{\sim}{x}}^{(2)})'$$

Then we use

$$V = \underset{\sim}{x}' \; \underset{\sim}{S}^{-1} \left(\bar{\underset{\sim}{x}}^{(1)} - \bar{\underset{\sim}{x}}^{(2)} \right) - 1/2 \left(\bar{\underset{\sim}{x}}^{(1)} + \bar{\underset{\sim}{x}}^{(2)} \right)' \; \underset{\sim}{S}^{-1} \left(\bar{\underset{\sim}{x}}^{(1)} - \bar{\underset{\sim}{x}}^{(2)} \right)$$

as our classification statistic. It can be shown that the limiting distribution of V is the distribution of U. (Investigations of the distribution of V can be found in References 58 and 59. We shall use the asymptotic results only.

b. Computer Programs

Two computer programs based on linear discriminant analysis have been written. One computer program, LINDA 1, is applicable when the covariance matrices of the populations of good devices and of bad devices are equal. Two different procedures are used in this computer program, depending on whether the user's problem falls under Case 1 or Case 2 as defined in the previous discussions.

The second computer program, LINDA 2, is applicable whether or not the covariance matrices are equal. This program is based on the theoretical work of Anderson and Bahadur [6] and the outline of the computer programs written by Welch and Wimpress [15]. Basically, LINDA 2 calculates the vector $\underset{\sim}{b}$ from the equation

$$\underset{\sim}{b} = \left[y \underset{\sim}{\Sigma}_1 + (1 - y) \underset{\sim}{\Sigma}_2 \right]^{-1} \left(\underset{\sim}{\mu}^{(2)} - \underset{\sim}{\mu}^{(1)} \right)$$

where

$$\underset{\sim}{\Sigma}_1, \; \underset{\sim}{\mu}^{(1)} \text{ and } \underset{\sim}{\Sigma}_2, \; \underset{\sim}{\mu}^{(2)}$$

are the covariance matrices and mean vectors for populations 1 and 2, respectively, and y ($0 \leq y \leq 1$) is the solution of the equation

$$\left\{ \left[y \underset{\sim}{\Sigma}_1 + (1 - y) \underset{\sim}{\Sigma}_2 \right]^{-1} \left(\underset{\sim}{\mu}^{(2)} - \underset{\sim}{\mu}^{(1)} \right) \right\}' \left\{ y^2 \underset{\sim}{\Sigma}_1 + (1 - y) \underset{\sim}{\Sigma}_2 \right\} \left\{ \left[y \underset{\sim}{\Sigma}_1 + (1 - y) \underset{\sim}{\Sigma}_2 \right]^{-1} \left(\underset{\sim}{\mu}^{(2)} - \underset{\sim}{\mu}^{(1)} \right) \right\} = 0$$

If

$$\underset{\sim}{X} = \begin{pmatrix} X_1 \\ X_2 \\ \vdots \\ X_n \end{pmatrix}$$

is the vector of parameter measurements, then if

$$\underset{\sim}{b}' \underset{\sim}{X} + p \geq 0, \quad \underset{\sim}{X} \text{ belongs to population 1}$$

$$\underset{\sim}{b}' \underset{\sim}{X} + p < 0, \quad \underset{\sim}{X} \text{ belongs to population 2.}$$

where b' is the transpose of the vector b. The scalar p is calculated from the equation

$$p = - \frac{\left(\underset{\sim}{b}' \underset{\sim}{\sum}_2 \underset{\sim}{b}\right)^{1/2} \underset{\sim}{b}' \underset{\sim}{\mu}^{(1)} + \left(\underset{\sim}{b}' \underset{\sim}{\sum}_1 \underset{\sim}{b}\right)^{1/2} \underset{\sim}{b}' \underset{\sim}{\mu}^{(2)}}{\left(\underset{\sim}{b}' \underset{\sim}{\sum}_1 \underset{\sim}{b}\right)^{1/2} + \left(\underset{\sim}{b}' \underset{\sim}{\sum}_2 \underset{\sim}{b}\right)^{1/2}}$$

APPENDIX H

COMPUTER PROGRAMS FOR SECOND BREAKDOWN STUDIES

APPENDIX H

COMPUTER PROGRAMS FOR SECOND BREAKDOWN STUDIES

1. INTRODUCTION

This appendix concerns the computer programs written to perform the iteration on the device model described in Section IX-2. There are five programs in all, a main program called E173C, and four subprograms called FOURIB, MPLOT, PLTLIN, and SCALES. The last three, MPLOT, PLTLIN, and SCALES, are described in a previous report[3], and will be only listed here, as no significant modifications have been in any of these programs. A discussion of the others follows.

2. E173C

This program performs the iteration described in Section IX-2c on Equations (2), (5), (10), (11) and (15) in Section IX-2b , subject to the termination criteria defined in Section IX-2d. The program also reduces the element size when necessary. After an iteration has terminated, the program will establish a new total current on the basis of previous results, the number of iterations performed to termination, and the reason for termination, reinitiate the necessary quantities, and perform a new iteration. E173C is a modified version of E173B, described previously[3], the main differences being that the chip size is not changed when the element (lump) size changes. A few changes have also been made in those program sections setting up the new total current for the next iteration and controlling the interpolation procedure. A flow diagram for the new program is shown in Figure H-1, and the Fortran listing is given in Table H-1.

3. FOURIB

This program, which is a modified version of FOURIA, described previously[3], calculates mutual thermal or electrical resistances between the lumped elements (the $\theta(|i-j|)$ of Equation (2), and $R(|i-j|)$ of Equation (4), Section IX-2b. The main change from FOURIA is the independent specification of the block and lumped element sizes. This change is not very great, but since the original program FOURIA was in error, and the description of it[3] was not correct either, a new description is given.

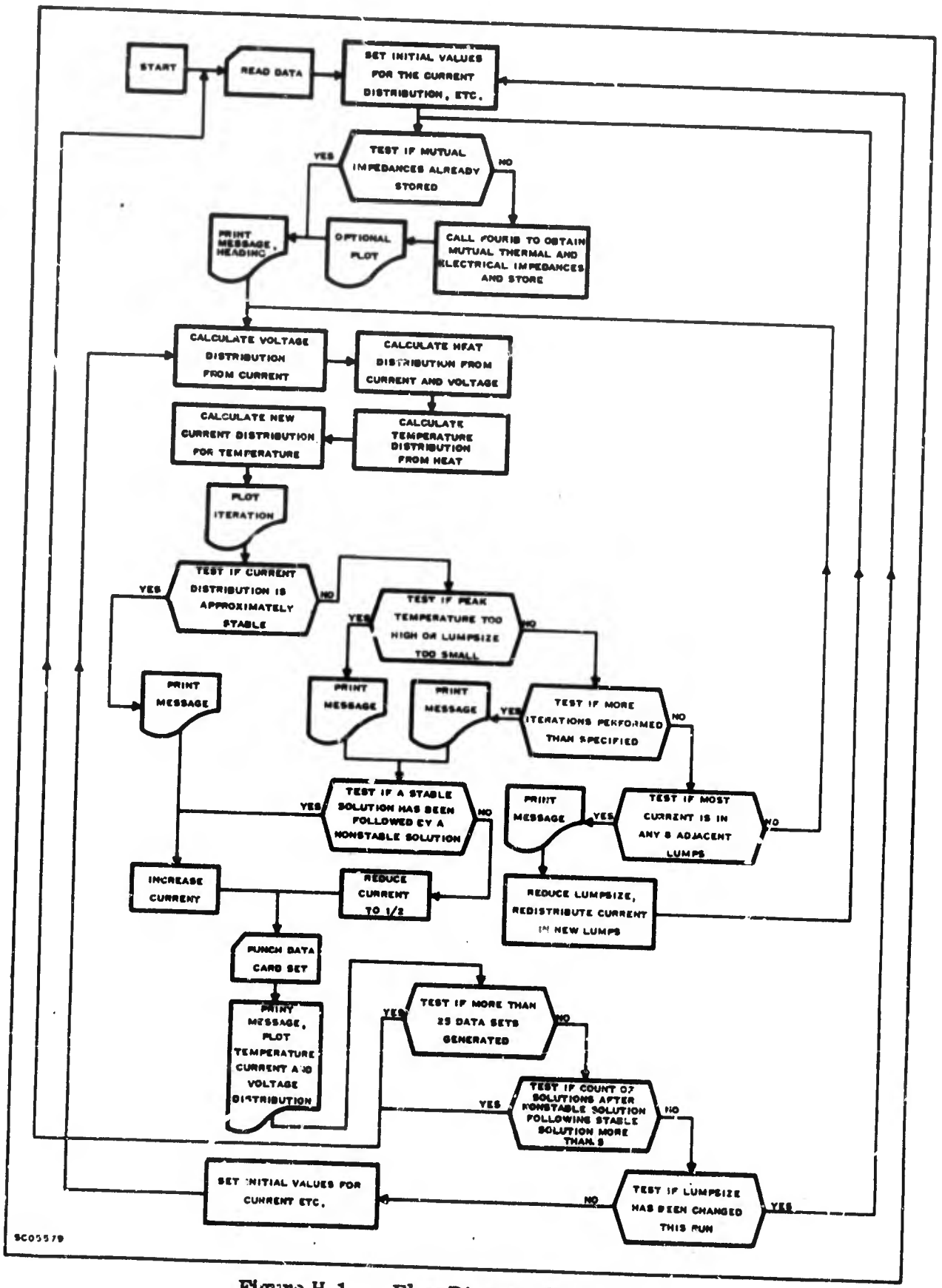

Figure H-1. Flow Diagram for E-173C

The symbols used in the program and in this text are shown with the model in Figure H-2. The chip is symmetrical, and by using a zero gradient boundary condition on the planes of symmetry, we can reduce the problem to the solution to Laplaces' equation within the block. The additional boundary conditions are as outlined in Section IX-2b. If we ignore the boundary condition on the top face, we obtain solutions of the form.

$$A \frac{\sinh\ [\ell(c-z)]}{\sinh\ (\ell c)} \quad \cos \left[\frac{(2m+1)\ \pi x}{2a}\right] \quad \cos \left[\frac{(2n+1)\ \pi y}{2b}\right]$$

where

$$\ell^2 = \left[\frac{(2m+1)\ \pi}{2a}\right]^2 + \left[\frac{(2n+1)\ \pi}{2b}\right]^2$$

and m and n are integers. The gradient of this solution on the top surface of the block is:

$$- A\ \ell \coth(\ell c) \cos \left[\frac{(2m+1)\ \pi x}{2a}\right] \cos \left[\frac{(2n+1)\ \pi y}{2b}\right]$$

A sum of such terms can be formed to give the required boundary condition on the top face, such that

$$f(x,y,z) = \sum_{m,n} a_{mn} \frac{\sinh \ell(c-z)}{\sinh\ (\ell c)} \cos \left[\frac{(2m+1)\ \pi x}{2a}\right] \cos \left[\frac{(2n+1)\ \pi y}{2b}\right]$$

and the a_{mn} are Fourier coefficients given by the boundary condition. The gradient on the top face of this sum is

$$\frac{\partial f}{\partial z} = \sum_{m,n} a_{mn}\ \ell \coth(\ell c) \cos \left[\frac{(2m+1)\ \pi x}{2a}\right] \cos \left[\frac{(2n+1)\ \pi y}{2b}\right]$$

and performing the normal Fourier analysis procedures we obtain

$$a_{mn} = \frac{4}{a\ b\ \ell \coth(\ell c)} \int_0^e \int_0^d \cos \left[\frac{(2m+1)\ \pi x}{2a}\right] \cos \left[\frac{(2n+1)\ \pi y}{2b}\right] dx\ dy$$

$$= \frac{16 \tanh(\ell c)}{\pi^2\ \ell (2m+1)\ (2n+1)} \sin \left[\frac{(2m+1)\ \pi d}{2a}\right] \sin \left[\frac{(2n+1)\ \pi e}{2b}\right]$$

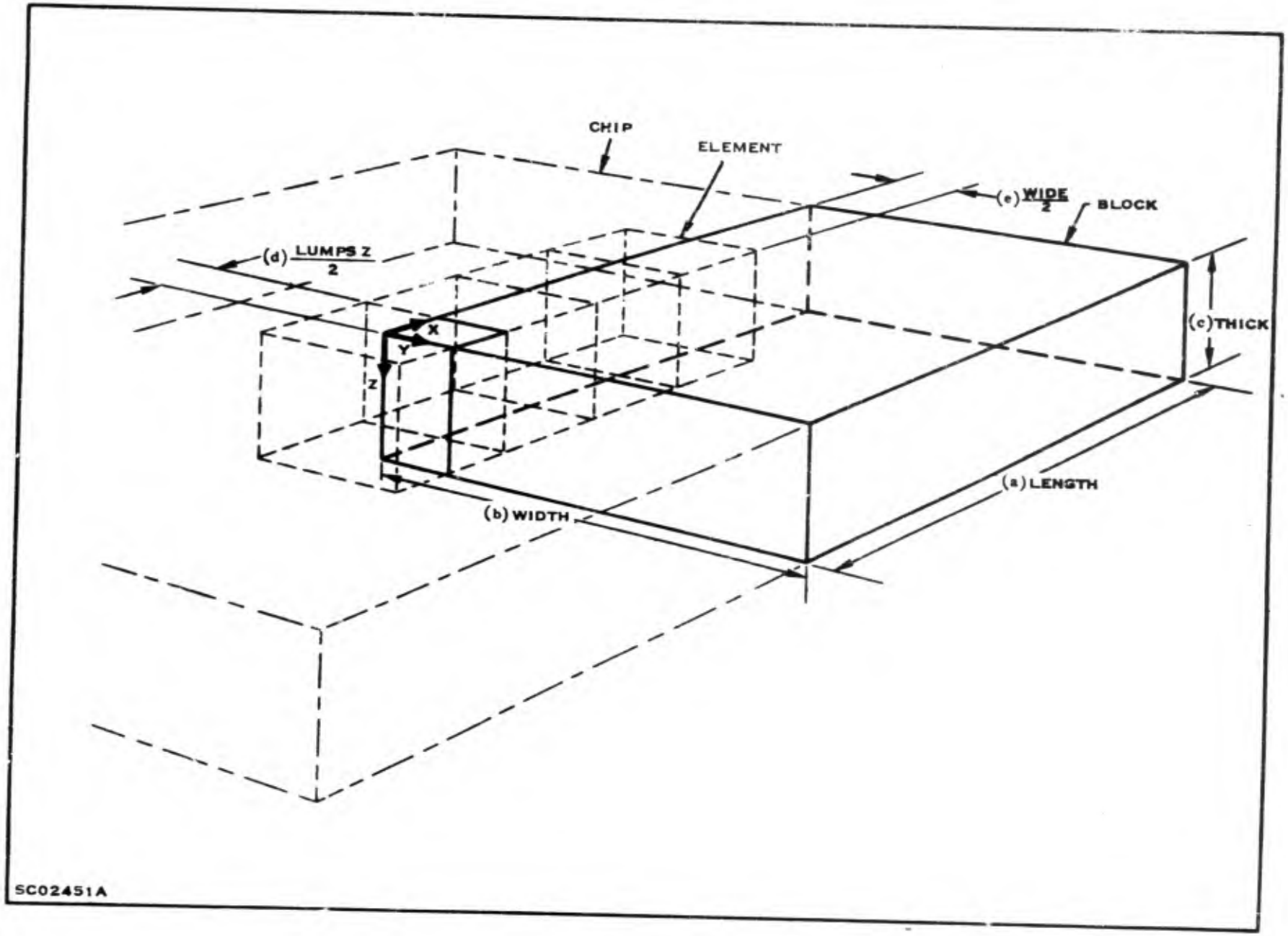

Figure H-2. Diagram of Model Geometry for FOURIB

However, we are only interested in solutions along the 'y' axis in the plane of the top face, where y = z = 0; the solution reduces to:

$$\sum_{m,n} a_{mn} \cos\left[\frac{(2m+1)\,\pi x}{2a}\right] = \sum_{m} A_m \cos\left[\frac{(2m+1)\,\pi x}{2a}\right]$$

where:

$$A_m = \sum_{n} a_{mn} = \frac{16}{(2m+1)\,\pi^2} \sin\frac{(2m+1)\,\pi e}{2b} \sum_{n} \frac{\tanh(\ell c)}{(2n+1)\,\ell} \sin\frac{(2n+1)\,\pi d}{2a}$$

The A_m are calculated as the A(M) where M = m+1 in the program, since FORTRAN does not permit zero subscripts. The individual terms in the sum change sign periodically in n, and the A_m will change sign periodically in m. The program is arranged to check the magnitude of the previous terms at each such sign change, and if they are small compared to the total value, to terminate the sum. Similar criteria are used to select the number of coefficients to calculate. An upper limit of 300 is set on both m and n.

The value of the function is calculated for a set of values of "x" by summing the terms to form

$$\sum_{m} A_m \cos\frac{(2m+1)\,\pi x}{2a}$$

for values of x given by

x = (n-1)d for n = 1 to 16.

This gives the 16 values of the function for unit gradient in the first element. By appropriate choice of parameters, this will give the "mutual resistance" for unit resistivity. These values are returned to the main program F173C. Multiplying by the appropriate constant, the mutual thermal or electrical resistance is obtained.

The FORTRAN listing is given in Table H-2.

4. MPLOT, PLTLIN, SCALES

The FORTRAN listings for these programs are given in Tables H-3, H-4 and H-5.

Table H-1. Computer Listing of E173C (Sheet 1 of 5)

```
E173C
BRADSHAW PETER D 03  TC                FORTRAN SOURCE LIST        E173C      09/23/66
  ISN       SOURCE STATEMENT

    0 $IBFTC E173C
      C
      C  A PROGRAMME TO SOLVE THE ONE-FINGER PROBLEM,INCLUDING THE EFFECTS OF
      C  COLLECTOR RESISTIVITY.
      C
    1         REAL  FLSCL(3),HEAT(16),I(17),ISUM,ITOT,ILAST(16),LEFTEG,LUMPSZ,
             1 LMPSZ1,TEMP(16),V(16),Y(16,3),LENGTH,FNT(32),FNE(16),FN(2),B(18)
             2 , HOLD(32,7),LMPSZL,VLAST(16)
    2         INTEGER CHAR(3) , SET1(17) , SET2(2)
    3         LOGICAL CHANG , PLOTAL , THIS(16) , LMPCHG , DO1MOR , TERMIN
    4         EQUIVALENCE (TEMP(1),Y(1,1)),(V(1),Y(1,2)),(I(1),Y(1,3)),(FNT(17)
             1 , FNE(1))
    5         DATA CHAR / 51,53,44 /, SET1 / 27,51,3,4,8,10,21,26,34,38,41,43,44
             1 ,50,54,55,56 /, SET2 / 51,21 /, LMPSZL / 0.0 /, WIDEL / 0.0 /,
             2 THICKL / 0.0 /, EPITXL / 0.0 /
    6   100 J3 = 0
    7         READ(5,210) J6,LMPSZ1,WIDE,THICK,EPITAX,THERM,ELEC,VCE,ITOT,PLOTAL
             1 , J7
   12   210 FORMAT(10H DATA SET ,I4,39H.UNITS-MICRONS,MV,MA,DEG.C.-INIT.LMPSZ.
             A , F7.1 , 11H FNGR.WDTH. , F7.1 / 9H0 THCKNS. , F7.1 , 12H EPITAX.
             BLYR. , F7.1 , 11H THERM.RES. , F7.4 , 12H ELECTR.RES. , F9.1  /
             C 12H0 APPL.VLTG., F9.0 ,11H TOT.CRRNT.,F9.2 ,13H ALL PLOTD.IS, L3
             D , 10H.STOP AT  , I3 ,  8H ITERNS.                )
   13         LENGTH = 20.0 * LMPSZ1
   14         WIDTH = 20.0 * WIDE
   17         J6INIT = J6
   20         WRITE ( 6,207 )
   21   207 FORMAT ( 50H1 THE DATA CARD JUST READ IN GIVES THE FOLLOWING-- /)
   22         WRITE(6,210)J6,LMPSZ1,WIDE,THICK,EPITAX,THERM,ELEC,VCE,ITOT,PLOTAL
             1 , J7
      C  TESTS IF LUMP PARAMETERS EQUAL PREVIOUS VALUES,KEEPS MUT.IMPS.IF SO.
   23         IF ( LMPSZL .EQ. LMPSZ1 .AND. WIDEL .EQ. WIDE .AND. THICKL .EQ.
             1 THICK .AND. EPITXL .EQ. EPITAX ) GO TO 104
   26         DO 102 N = 1 , 7 , 1
   27   102 HOLD (1,N) = 0.0
   31         LMPSZL = LMPSZ1
   32         WIDEL = WIDE
   33         THICKL = THICK
   34         EPITXL = EPITAX
   35   104 LUMPSZ = LMPSZ1
   36         WIDE = WIDEL
   37         LEFTEG = 0.0
   40         I(17) = 0.0
   41         HELP = 0.0
   42         J4 = 0
   43         J8 = 0
   44         DO 106 J = 1 , 16 , 1
   45         ILAST(J) = 0.0
   46         VLAST(J) = 2.5
   47         THIS(J) = .TRUE.
   50   106 I(J) = ITOT / 16.
```

SC05696

Table H-1. Computer Listing of E173C (Sheet 2 of 8)

```
E173C
BRADSHAW PETER D 03  TC                FORTRAN SOURCE LIST          E173C      09/23/66
 ISN      SOURCE STATEMENT

  52        E(2) = 100.
  53    108 N = INT ( ALOG10 ( LMPSZ1 / LUMPSZ + 0.1 ) / 0.3010 ) + 1
  54        LMPCHG = .FALSE.
  55        IF ( N .GT. 7 ) GO TO 160
  60        J5 = 0
  61        IF ( HOLD(1,N) .NE. 0.0 ) GO TO 112
  64        CALL FOURIB ( LENGTH,WIDTH,LUMPSZ,WIDE,THICK ,HOLD(1,N),16,PLOTAL)
  65        DO 110 J = 1 , 16 , 1
  66    110 HOLD(J+16,N1 = HOLD(J,N)
  70        IF ( THICK .NE. EPITAX ) CALL
           1     FOURIB (LENGTH,WIDTH,LUMPSZ,WIDE,EPITAX,HOLD(17,N),16,PLOTAL)
  73        IF ( .NOT. PLOTAL ) GO TO 112
  76        WRITE(6,203) LENGTH,WIDTH,LUMPSZ,WIDE,THICK,EPITAX,HOLD(1,N),
           1 HOLD(17,N)
  77    203 FORMAT ( 51H1 THE MUTUAL IMPEDANCES ARE PLOTTED NEXT FOR BLOCK ,
           A 2(F9.2,2H X),5H LUMP , 2(F7.2,2H X),F8.2,2H + ,F8.2,9H MICRONS
           B //
                                                    37H THE VALUES OF FNT(1)
           C AND FNE(1) ARE- , 1P1E10.3 , 4H AND , 1P1E10.3                  //)
 100        FN(2) = HOLD(18,N)
 101        FN(1) = HOLD(2,N)
 102        CALL MPLOT ( HOLD(1,N) , FN    , 16 , 2 , 2 , THIS , SET2 )
 103    112 DO 114 N1 = 1 , 32 , 1
 104    114 FNT(N1) = HOLD(N1,N)
     C   END OF THE FOURIER ANALYSIS SECTION,BEGINING OF ITERATION.
 106    116 WRITE(6,205)   LUMPSZ,WIDE,THICK,EPITAX,THERM,ELEC,VCE,ITOT,J6
 107    205 FORMAT( 60H1THE CURRENT DISTRIBUTIONS AT EACH ITERATION WITH PARAM
           AETERS ,F7.2,2H X,1F7.2,2H X,1F7.2,2H +,1F7.2,16H(EPITAX) MICRONS,
           B F7.4,12H DEG.C.M/UW. // 8H ELECTR.,F10.3,8H OHM.CM.,F10.3,2HMV,
           C F10.3,2HMA,33H ARE PLOTTED HERE BELOW.(DATA SET ,I4,2H )  /)
     C   THE TEMPERATURE SCALE ALLOWS FOR SOME INCREASE IN THE PEAK TEMP.
 110        FLSCL(2) = AMAX ( 220. , HELP + 130. )
 111        FLSCL(3) = ITOT
 112        VMIN = VCE
 113        CALL SCALES ( FLSCL(2) , 12 , 2 , SET1(2) )
     C   TO AVOID CONFUSION OF THE POINTS,THE PLOTTED VALUES ARE SPACED OUT.
 114        DO 118 J = 1 , 9 , 1
 115    118 B(J+2) = I(J) + FLSCL(3) / 50. * FLOAT(J-1)
 117        FLSCL(1) = FLSCL(2)
 120        B(1) = 100.
 121        CALL PLTLIN ( B , J4 , 11 , 3 , FLSCL , SET1 )
 122    120 VMAX = -1.0
 123        DO 124 J = 1 , 16 , 1
 124        V(J) = 0.0
 125        DO 122 J1 = 1 , 16 , 1
 126        J2 = IABS(J-J1) + 1
 127    122 V(J) = V(J) + I(J1) * FNE(J2) * ELEC
 131        V(J) = VCE - V(J) / ( LUMPSZ * WIDE )
 132        IF ( VMAX .LT. V(J) ) VMAX = V(J)
 135        IF ( VMIN .GT. V(J) ) VMIN = V(J)
     C   THE LOCAL COLL-EMITTER VOLTAGE IS PREVENTED FROM BECOMING NEGATIVE.
 140        IF ( V(J) / VCE .LT. 0.0 ) V(J) = VLAST(J) * 0.5
     C   AN ATTEMPT IS MADE TO REDUCE INSTABILITY PROBLEMS NEAR SATURATION.
 143        VLAST(J) = V(J)
     C   CORRECTION IS APPLIED FOR THE HEAT DISSIPATED IN THE EPITAXIAL LAYER.
 144    124 HEAT(J) = (VCE-(VCE-V(J))*EPITAX/(THICK*2.0))*I(J)/(LUMPSZ*WIDE)

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Table H-1. Computer Listing of E173C (Sheet 3 of 5)

```
E173C
BRADSHAW PETER D 03  TC                FORTRAN SOURCE LIST        E173C      09/23/66
  ISN       SOURCE STATEMENT

  146       ISUM = 0.0
  147       HELP = 0.0
  150       J4 = J4 + 1
  151       J5 = J5 + 1
  152       DO 128 J = 1 , 16 , 1
  153       TEMP(J) = 0.0
  154       DO 126 J1 = 1 , 16 , 1
  155       J2 = IABS(J-J1) + 1
  156   126 TEMP(J) = TEMP(J) + HEAT(J1) * FNT(J2) * THERM
  160   128 IF ( HELP .LT. TEMP(J) ) HELP = TEMP(J)
  164       DO 130 J = 1 , 16 , 1
  165       I(J) = EXP((TEMP(J)-HELP) * 0.0885 + 10.) * (1.0-EXP(-V(J)/26.0))
  166   130 ISUM = ISUM + I(J)
  170       CHANG = .FALSE.
  171       J = 0
  172       DO 132 J1 = 1 , 16 , 1
  173       I(J1) = I(J1) * ITOT / ISUM
      C  A SERIES OF INTERPOLATIONS ARE CARRIED OUT,AS NECCESSARY.
  174       IF ( J4 .NE. J5 ) I(J1) = ( I(J1) + ILAST(J1) ) * 0.5
  177       IF ( ABS(I(J1)-ILAST(J1)) .GE. ITOT*0.0002 ) CHANG = .TRUE.
  202       IF ( J4 .GE. J7/2 ) I(J1) = ( I(J1) + ILAST(J1) ) * 0.5
  205       IF ( VMIN .LT. 5.0 ) I(J1) = ( I(J1) + ILAST(J1) * 3.0 ) * 0.25
  210       B(J1+2) = I(J1) + FLSCL(3) / 50. * FLOAT(J1-1)
  211   132 IF ( I(J1) .GE. ITOT / 2.0 ) J = J1
  215       IF ( J4 .GT. J7 .OR. DO1MOR ) GO TO 158
  220       IF ( J4 .EQ. J7/2 ) WRITE(6,213)
  223       IF ( J8 .EQ. 0 .AND. VMIN .LT. 0.1 ) WRITE(6,213)
  226   213 FORMAT ( 7X , 2HI+ ,22(5H-----) , 1H+ / 7X ,114HII FUTURE VALUES F
           AOR 'I(J)' WILL BE INTERPOLATED WITH 'ILAST(J)'.THE RATES OF CHANGE
           B OF 'I(J)' MAY BE AFFECTED. I  / 7X , 2HI+ , 22(5H-----) , 1H+ )
  227       IF ( VMIN .LT. 0.1 ) J8 = 1
  232       B(2) = HELP + 100.
  233       CALL PLTLIN ( B , J4 , 11 , 3 , FLSCL , SETI )
  234       IF ( .NOT. CHANG ) GO TO 164
  237       IF ( VMAX .LT. 1.0 ) GO TO 156
  242       IF ( J4 .EQ. J7 ) GO TO 154
  245       IF ( HELP .GT. 400. ) GO TO 161
  250       IF ( J .EQ. 0 ) GO TO 134
  253       IF ( LUMPSZ * 32.0 .LT. AMAX ( WIDTH , LMPSZ1 ) ) GO TO 160
  256       IF ( I(J-1) .GT. I(J+1) ) J = J - 1
  261       J = MINO ( 9 , MAXO ( 0 , J-4 ) )
  262       GO TO 146
      C  NOW TEST IF ANY 8 ADJACENT LUMPS CARRY MOST CURRENT
  263   134 ISUM = 0.0
  264       IF ( LUMPSZ * 32.0 .LT. AMAX ( WIDTH , LMPSZ1 ) ) GO TO 140
  267       DO 136 J = 1 , 8 , 1
  270   136 ISUM = ISUM + I(J)
  272       J = 9
  273       MAXJ = 0
  274       MINJ = 0
  275   138 IF ( ISUM .LT. ITOT*0.03 ) MINJ = J
  300       IF ( MAXJ .EQ. 0 ) MAXJ = MINJ
      C  MINJ AND MAXJ ARE THE 'J' LIMITS FOR 8 OF THE I(J) TO BE NEGLIGIBLE.
  303       J = J - 1
  304       ISUM = ISUM + I(J+8) - I(J)

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Table H-1. Computer Listing of E173C (Sheet 4 of 5)

```
E173C
BRADSHAW PETER D 03  TC                FORTRAN SOURCE LIST        E173C      09/23/66
  ISN       SOURCE STATEMENT

  305         IF ( J .GT. 0 ) GO TO 138
  310         IF ( MINJ .NE. 0 ) GO TO 144
  313     140 DO 142 J = 1 , 16 , 1
  314     142 ILAST(J) = I(J)
  316         IF ( LMPCHG ) GO TO 108
  321         GO TO 120
  322     144 J = (MAXJ + MINJ) / 2 - 1
  323     146 IF ( LUMPSZ .GE. LMPSZ1 * 0.9 ) WRITE(6,213)
      C   NEW LUMPS ARE NEEDED.'J' GIVES THEIR POSITION.THE LUMP-SIZE IS HALVED
  326         IF ( J5 .GT. 5 ) WRITE(6,204) J6,LUMPSZ,WIDE,THICK,EPITAX,ITOT
  331     204 FORMAT ( 1H0/10H1 DATA SET ,I4, 9H.LUMPS OF , 2(1F7.2,2H X),1F7.2,
             A 2H / , 1F7.2 , 4H AND , 1F10.3 , 3H MA                    )
  332         LEFTEG = LEFTEG + ( LUMPSZ * FLOAT(J) )
  333         WRITE (6,200) LEFTEG
  334     200 FORMAT ( 54H0 THE LUMPSIZE IS BEING HALVED TO GIVE BETTER ACCURACY
             A  , 35H.THE LEFT EDGE OF THE NEW SET IS AT , 1F9.3 / )
  335         LUMPSZ = LUMPSZ / 2.0
  336     147 LMPCHG = .TRUE.
  337         IF ( J5 .EQ. 0 ) GO TO 148
  342         WRITE(6,202) J4 , J5
  343     202 FORMAT ( 72H  THE PLOT BELOW GIVES CURRENT,VOLTAGE AND TEMPERATURE
             A DISTRIBNS.AFTER , I3 , 9H ITERNS., , I3 ,18H AT THIS LUMP SIZE /)
  344         J5 = 0
  345         FLSCL(1) = HELP
  346         FLSCL(2) = VCE
  347         CALL MPLOT ( Y , FLSCL , 16 , 3 , 3 , THIS , CHAR )
  350     148 DO 150 J1 = 1 , 8 , 1
  351         J2 = J + J1
      C   THE NEW LUMP CURRENTS ARE PUT INTO'ILAST'AND TRANSFERED TO'I'.
  352         ILAST(2*J1-1) = ( 3.0 * I(J2)                 )/8.0
  353         IF ( J2 .LE. 1)  GO TO 150
  356         ILAST(2*J1-1) = ( 3.0 * I(J2) + I(J2-1) )/8.0
  357     150 ILAST(2*J1  ) = ( 3.0 * I(J2) + I(J2+1) )/8.0
  361         DO 152 J1 = 1 , 16 , 1
  362         VLAST(J1) = 2.5
  363     152 I(J1) = ILAST(J1)
  365         GO TO 134
  366     154 WRITE(6,217) J6
  367     217 FORMAT ( 79H1 THE ITERATION HAS REACHED THE SET LIMIT.TWO PLOTS AR
             AE GIVEN OF I,V,T.DATA SET , I4 //30H THE FIRST PLOT IS GIVEN HERE.
             B     /)
  370         DO1MOR = .TRUE.
  371         GO TO 168
  372     156 WRITE(6,211) J6
  373     211 FORMAT (  78H1 THIS ITERATION IS NO LONGER USEFUL,AS THE DEVICE IS
             A FULLY SATURATED.DATA SET,I4 / 75H0 THE CURRENT WILL BE HALVED AND
             B RERUN,OR A NEW DATA SET WILL BE READ IN                    /)
  374         GO TO 162
  375     158 WRITE(6,215) J6
  376     215 FORMAT (  78H1 THIS ITERATION HAS EXCEEDED THE SET LIMIT,AND IS BE
             AING TERMINATED.  DATA SET,I4 / 75H0 THE CURRENT WILL BE HALVED AND
             B RERUN,OR A NEW DATA SET WILL BE READ IN                    /)
  377         DO1MOR = .FALSE.
  400         GO TO 162
  401     160 WRITE(6,209) J6

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```

Table H-1. Computer Listing of E173C (Sheet 5 of 5)

```
E173C
BRADSHAW PETER D 03  TC                FORTRAN SOURCE LIST          E173C     09/23/66
  ISN       SOURCE STATEMENT

  402    209 FORMAT(  79HO THE ITERATION IS NO LONGER USEFUL,AS THE CURRENT IS
            ATOO CONCENTRATED.DATA SET,I4 / 75HO THE CURRENT WILL BE HALVED AND
            B RERUN,OR A NEW DATA SET WILL BE READ IN                        /)
  403        GO TO 162
  404    161 WRITE (6,221) HELP
  405    221 FORMAT ( 38H1 THE PEAK TEMPERATURE IS TOO HIGH AT , F8.1 , 36H AND
            A THE ITERATION IS BEING HALTED.  /  90HO ANOTHER ITERATION WILL BE
            C PERFORMED WITH AN ALTERED CURRENT,OR A NEW DATA SET READ IN.    /)
  406    162 IF ( J3 .NE. 0 ) J3 = J3 + 1
       C   J3 BEGINS AT 0,AND BECOMES 1 WHEN A STABLE SOLN.IS REACHED,2 IF A NEW
       C   LEVEL OF INSTABILITY IS REACHED.
  411        IF ( J3 .GT. 1 ) GO TO 166
  414        IF ( .NOT.DO1MOR ) ITOT = ITOT / 2.0
  417        GO TO 168
  420    164 WRITE(6,201) J4,LUMPSZ,WIDE,THICK,EPITAX,THERM,ELEC,VCE,ITOT,J6
  421    201 FORMAT ( 29H1THE SOLUTION IS STEADY AFTER ,I3, 27H ITERNS.FOR LUMP
            A DIMENSIONS , 2(F7.2,2H X) ,1H(,F7.2,2H /,F7.2, 20H) MICRONS,THERM
            B.RES.,F7.4,10H DG.C.U/UW // 10H COLL.RES.,F9.1,15H OHM.UM.,VOLTG.,
            CF9.2,21H MV.AND TOTAL CURRENT,F10.3,12H MA,DATA SET,I4,39H.CURRENT
            D,VOLTAGE,AND TEMP.DISTRIBNS.ARE  // 56H PLOTTED BELOW.THE CURRENT
            EWILL BE INCREASED AND RERUN.
  422        J3 = 1                                                        /)
  423        ITOT = 1.021 * ITOT
  424    166 IF ( J4 .LT. 15 .OR. J3 .EQ. 2 ) ITOT = 1.06 * ITOT / 1.02
  427        IF ( J4 .LT. 10 .OR. J3 .GT. 2 ) ITOT = 1.20 * ITOT / 1.06
  432    168 FLSCL(1) = HELP
  433        FLSCL(2) = VCE
  434        IF ( N .LT. 8 ) CALL MPLOT ( Y , FLSCL , 16 , 3,3 , THIS , CHAR )
  437        IF ( DO1MOR ) GO TO 140
  442        IF ( J3 .GT. 4 .OR. J6 - J6INIT .GT. 25 ) GO TO 100
       C  THIS SECTION OF PROGRAMME TRUNCATES 'ITOT' TO GIVE A ROUNDED VALUE.
  445        J8 = 0
  446    170 IF ( ITOT .LT. 100.01 ) GO TO 172
  451        ITOT = ITOT * 0.10
  452        J8 = J8 + 1
  453        GO TO 170
  454    172 IF ( ITOT .GE. 10.0 ) GO TO 174
  457        ITOT = ITOT * 10.0
  460        J8 = J8 - 1
  461        GO TO 172
  462    174 ITOT = 0.2 * AINT( ITOT * 5.0 + 0.9 )
  463        IF ( ITOT .GE. 25.0 ) ITOT = 0.5 * AINT( ITOT * 2.0 + 0.05 )
  466        IF ( ITOT .GE. 50.0 ) ITOT = AINT ( ITOT + 0.05 )
  471        ITOT = ITOT * 10.0 ** J8
  472        J6 = J6 + 1
  473        WRITE(7,210)J6,LMPSZ1,WIDE,THICK,EPITAX,THERM,ELEC,VCE,ITOT,PLOTAL
            1 , J7
  474        IF ( LUMPSZ .NE. LMPSZ1 ) GO TO 104
  477        DO 176 J = 1 , 16 , 1
  500    176 I(J) = ITOT / 16.
  502        B(2) = 100.
  503        J4 = 0
  504        J5 = 0
  505        J8 = 0
  506        GO TO 116

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```

Table H-2. Computer Listing of FOURIB

```
E173C
BRADSHAW PETER D 03  TC                FORTRAN SOURCE LIST        FOURIB    09/23/66
  ISN       SOURCE STATEMENT

    0 $IBFTC FOURIB
    1       SUBROUTINE FOURIB ( LENGTH,WIDTH,LUMPSZ,WIDE,THICK,FN,N4,PLOTAL)
      C  THIS SUBROUTINE FINDS THE FOURIER COEFFS.FOR A FUNCTION SATISFYING
      C  LAPLACE'S EQUATION IN THREE DIMENSIONS,FOR BOUNDARY CONDITIONS THUS
      C  'FN(X,Y,Z) = 0.0'FOR'Z = THICK','FOR'Y = WIDTH',AND FOR'X = LENGTH',
      C  'DFN(X,Y,Z)/DX = 0.0'FOR'Y = 0.0','DFN(X,Y,Z)/DY = 0.0'FOR'X = 0.0'
      C  'DFN(X,Y,Z)/DZ = 0.0'FOR'Z = 0.0,X.GT.LUMPSZ/2.0,Y.GT.WIDE/2.0'AND
      C  'DFN(X,Y,Z)/DZ = 1.0'FOR'Z = 0.0,X.LE.LUMPSZ/2.0,Y.LE.WIDE/2.0',AND
      C  FINDS'FN(X,0,0)'FOR'X = N*LUMPSZ,N = 1,N4,1'.
    2       REAL FN(N4),LENGTH,LUMPSZ,WIDTH,WIDE,THICK,SAVE(300),A(300),L
    3       REAL MT , NT
    4       INTEGER NTM(300) , GROUP
    5       LOGICAL PLOTAL
    6       GROUP = INT ( LENGTH / AMAX ( THICK , LUMPSZ ) ) / 100 * 2 + 1
    7       IF ( PLOTAL ) WRITE(6,204) LENGTH,WIDTH,THICK,LUMPSZ,WIDE,GROUP
   12   204 FORMAT ( 92H1THE FOURIER COMPONENTS FOR THE DISTRIBN.ON THE Y AXIS
          A ARE PLOTTED BELOW FOR A BLOCK SIZE OF  , F9.2,2H X,F9.2,2H X,F9.2
          B , 5H AND  // 14H LUMP SIZE OF , F7.2 , 2H X , F7.2 ,  39H MICRONS
          C.COMPONENTS GROUPED IN SETS OF  , I5                              /)
   13       AONE = 0.0
   14       N2 = 0
   15       ALAST = 1.0
   16       PI = 3.1415926535
   17       DO 177 M = 1 , 300 , 1
   20       MT = GROUP * ( 2 * M - 1 )
   21       A(M) = 0.0
   22       TLAST = 1.0
   23       TAREA = 0.0
   24       DO 175 N = 1 , 300 , 1
   25       NTM(M) = N
   26       L = SQRT(MT**2/LENGTH**2 + FLOAT((2*N-1)**2)/WIDTH**2)*PI / 2.0
   27       IF ( N .LE. N2 ) GO TO 171
   32       DO 170 N1 = N2 , N , 1
   33       NT = 2 * N1 - 1
   34   170 SAVE(N1) = SIN(NT * PI * WIDE / (4.0*WIDTH) ) / NT
   36       N2 = N
   37   171 TERM = SAVE(N) * TANH(L*THICK)/L
   40       TAREA = TAREA + TERM
   41       IF ( TERM * TLAST .GT. 0.0 .OR. 0.1 * TLAST .EQ. 0.0 ) GO TO 175
   44       A(M) = A(M) + TAREA
   45       TAREA = 0.0
   46       IF ( ABS ( TAREA / AMAX ( AONE,ABS(A(M))) ) .LE. 0.015 ) GO TO 176
   47   175 TLAST = TERM
   51   176 IF ( M .EQ. 1 ) AONE = ABS ( A(1) )
   54   172 A(M) = A(M) * 16.0 /(PI**2) * SIN(NT*PI*LUMPSZ/(4.0*LENGTH))/NT
   55       IF ( M .EQ. M / 10 * 10 ) NTM(M) = M * GROUP * 10
   60       IF ( M .EQ. 1 .OR. AMAXA.LT. ABS(A(M)) ) AMAXA= ABS(A(M))
   63       IF ( M .EQ. 1 ) A1 = A(1)
   66       IF ( M .EQ. 1 .AND. PLOTAL ) CALL SCALES ( A1 , 1 , 1 , 44 )
   71       IF ( PLOTAL ) CALL PLTLIN ( A(M) , NTM(M) , 1 , 1 , A1 , 44)
   74       IF ( A(M) * ALAST .GT. 0.0 .OR. 0.1 * ALAST .EQ. 0.0 ) GO TO 177
   77       IF ( AMAXA.LE. 0.025 * ABS(A(1)) ) GO TO 173
  102       AMAXA= 0.0
  103   177 ALAST = A(M)
  105     * M = 300
      C  THE 'A(M)' ARE THE FOURIER COMPONENTS OF THE FUNCTIONAL DISTRIBUTION.
  106   173 M = GROUP * M
  107       DO 174 N = 1 , N4 , 1
  110       FN(N) = 0.0
  111       DO 174 M1 = 1 , M , 1
  112       M2 = (M1-1) / GROUP + 1
  113   174 FN(N) = FN(N)+A(M2)*COS(FLOAT((2*M1-1)*(N-1))*PI*LUMPSZ/LENGTH/2.)
  116       RETURN
      C  THE FN(N) ARE THE MUTUAL IMPEDANCE RATIOS TO ALL LUMPS FROM ONE LUMP.
  117       END
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```

Table H-3. Computer Listing of Program MPLOT

```
BRADSHAW P.D.     03  TC          FORTRAN SOURCE LIST          MPLOT      04/01/66
ISN       SOURCE STATEMENT

  0 $IBFTC MPLOT
  1         SUBROUTINE MPLOT ( VALUE , FLSCL , N , M , M1 , THIS , CHAR       )
    C
    C   THIS SUBROUTINE PLOTS GRAPHS OF THE'VALUE(I,J' AGAINST'J'FOR'J 1 TO N'
    C   TO SCALES WHICH ARE SET AT THE NEXT AVAILABLE  ALUES ABOVE'FLSCL(M)'
    C   THE ARGUMENTS ARE AS ABOVE,AND'M'IS THE NO.OF  /ARIABLES,'M1'THE NO.OF
    C   SCALES,'THIS'IS A LOGICAL ARRAY GIVING THOSE SETS OF'I'TO BF PLOTTED
    C  'CHAR'CONTAINS THE DECIMAL VALUE OF THE SYMBOLS TO BF PRINTED.AS BELOW
    C         0         1         2         3         4         5         6
    C         01234567890123456789012345678901234567890123456789012345678901234
    C  CHS. 012345678$=*   +ABCDEFGHI+.)   -JKLMNOPQR-$*    /STUVWXYZ*,(
    C  NEG. -JKLMNOPQR-$*   /STUVWXYZ*,(   012345678$=*   +ABCDEFGHI+.)
    C
  2         REAL  VALUE(N,M) ,  FLSCL(M1)
  3         LOGICAL THIS(N)
  4         INTEGER   POINT( 102 ) , CHAR(M) , OVR(12)
  5         CALL SCALES ( FLSCL , M , M1 , CHAR )
  6         DO 150 J1 = 1,N ,1
  7         IF ( N .LT. 20 ) WRITE (6,207)
 12         DO 158 J = 2,101 ,1
 13    158  POINT(J) = -17 179 869 184
 15         POINT(1) = 26 843 545 600
 16         POINT(102 ) = -17 997 958 192
    C   THIS SETS POINT(1) TO'I',AND THE REST OF POINT TO BLANKS,INCL.POINT(102)
 17         IF ( J1 / 5 * 5 .EQ. J1 ) POINT(1) = -2
 22         IF ( J1 / 10 * 10 .EQ. J1 ) POINT(2) = -2
 25         K = 1
 26         IF ( N .LT. 10 ) WRITE (6,207)
 31         IF ( .NOT. THIS(J1) ) GO TO 150
 34         OVR(1) = -17 179 869 184
 35         K2 = 0
 36         DO 165 K1 = 1 , M , 1
 37         IF ( M .EQ. M1 ) K = K1
 42         J = ABS( VALUE(J1,K1) / FLSCL(K) * 100. ) + 1.5
 43         IF ( J .LE. 101 ) GO TO 159
    C   J IS TOO BIG TO PLOT,SO OVRFLW IS PLACED IN POINT(102),AND A LIST MADE
    C   OF THOSE CHARACTERS THAT OVERFLOWED,AND ALSO J IS REDUCED BY 100S.
 46         POINT(102) = -7 342 483 702
 47         J = J -(( J-1 ) / 100 ) * 100
 50         K2 = 1 + K2
 51         IF ( K2 .LE. 12 ) OVR(K2) = CHAR(K1) + 1 073 741 824
 54    159  POINT(J) = CHAR(K1) + 1 073 741 824
 55    165  IF ( VALUE(J1,K1) * FLSCL(K1) .LT. 0.0 ) POINT(J) = -POINT(J)
 61         IF ( K2 .GT. 12 ) K2 = 12
 64         WRITE(6,202) J1 ,( POINT(J2),J2 = 1,102, 1 ),( OVR(K1),K1 = 1,K2)
 75    150  IF ( .NOT. THIS(J1) ) WRITE(6,202)  J1 , POINT(1) , POINT(2)
101         IF ( N .GT. 1 ) WRITE(6,204)
104         RETURN
105    202  FORMAT ( 1H    ,I5 ,  1X  , 101A1 , 1A8 , 12A1 )
106    204  FORMAT (  7X , 1H1 ,20( 5H----- ) , 9H PLOT END   /)
107    207  FORMAT (  9H          I     )
    C   THIS IS THE END OF THE MULTIPLE PLOTTING SUBROUTINE,THE ARGUMENTS ARE
    C   RETURNED WITH ONLY'FLSCL'AND'CHAR'ALTERED .THESE HOLD THE CORRECTED
    C   VALUES OF THESE ARRAYS AS USED IN THE EXECUTION,AND NEED NOT BE RESET
110         END
```

Table H-4. Computer Listing of Program PLTLIN

```
PETER BRADSHAW   02  TC              FORTRAN SOURCE LIST          PLTLIN    02/23/67
  ISN       SOURCE STATEMENT

    0 $IBFTC PLTLIN
    1       SUBROUTINE PLTLIN ( VALUE , J1 , M , M1 , FLSCL , CHAR )
      C  THIS SUBROUTINE PRINTS ONE LINE WITH THE VALUES OF 'VALUE' INDICATED
      C  TO THE SCALE 'FLSCL' BY THE POSITIONS IN WHICH 'CHAR' ARE PRINTED.THE
      C  OTHER ARGUMENTS GIVE - 'J1' AN INTEGER TO BE PRINTED BESIDE THE AXIS,
      C  'M' THE NO. OF VALUES, 'M1' THE NUMBER OF SCALES ( = 1 OR M ),OR IF 0
      C  'M1' CAUSES A LINE WITH NO POINTS TO BE WRITTEN
    2       REAL VALUE(M) , FLSCL(M1)
    3       INTEGER POINT(102) , CHAR(M) , OVR(12)
    4       IF ( M1 .LE. 0 ) GO TO 166
    7       DO 158 J = 2,101 ,1
   10   158 POINT(J) = -17 179 869 184
   12       POINT(1) = 26 843 545 600
   13       POINT(102 ) = -17 997 958 192
      C  THIS SETS POINT(1) TO'I',AND THE REST OF POINT(102) TO BLANKS
   14       IF ( J1 / 5 * 5 .EQ. J1 ) POINT(1) = 17 179 869 184
   17       IF ( J1 / 10 * 10 .EQ. J1 ) POINT(2) = -2
   22       K2 = 0
   23       OVR(1) = -17 179 869 184
   24       DO 165 K1 = 1 , M , 1
   25       IF ( K1 .LE. M1 ) K = K1
   30       J = ABS ( VALUE(K1) / FLSCL(K) * 100. ) + 1.5
   31       IF ( J .LE. 101 ) GO TO 159
      C  J IS TOO BIG TO PLOT,SO OVRFLW IS PLACED IN POINT(102),AND A LIST MADE
      C  OF THOSE CHARACTERS THAT OVERFLOWED,AND ALSO J IS REDUCED BY 100S.
   34       POINT(102) = -7 342 483 702
   35       J = J -(( J-1 ) / 100 ) * 100
   36       K2 = 1 + K2
   37       IF ( K2 .LE. 12 ) OVR(K2) = CHAR(K1) * 1 073 741 824
   42   159 POINT(J) = CHAR(K1) * 1 073 741 824
   43   165 IF ( VALUE(K1) * FLSCL(K1) .LT. 0.0 ) POINT(J) = -POINT(J)
   47       IF ( K2 .GT. 12 ) K2 = 12
   52       WRITE(6,202) J1 ,( POINT(J2),J2 = 1,102, 1 ),( OVR(K1),K1 = 1,K2)
   63       RETURN
   64   166 WRITE(6,207)
   65       RETURN
   66   202 FORMAT ( 1H    ,I5 ,  1X  , 101A1 , 1A8 , 1X , 12A1 )
   67   207 FORMAT( 9H         I  )
   70       END
```

Table H-5. Computer Listing of Program SCALES (Sheet 1 of 2)

```
PETER BRA  'IAW   03  TC            FORTRAN SOURCE LIST        SCALES     02/23/67
  ISN       SOURCE S'ATEMENT

    0 $IBFTC SCALES
            SUBROUTINE SCALES ( FLSCL , M , M1 , CHAR )
      C
      C  THIS SUBROUTINE SETS THE SCALES 'FLSCL' AT THE NEXT AVAILABLE VALUE
      C  ABOVE THE SET ARGS.,AND MARKS OUT SCALES TO THESE VALUES.'M' CONTAINS
      C  THE NO.OF CHARACTERS IN 'CHAR',AND 'M1' THE NO.OF DIFFERENT SCALES.
      C 'CHAR'CONTAINS THE DECIMAL VALUE OF THE SYMBOLS TO BE PRINTED,AS BELOW
      C        0         1         2         3         4         5         6
      C        01234567890123456789012345678901234567890123456789012345678901234
      C CHS. 01234567890$='   +ABCDEFGHI+.)   -JKLMNOPQR-$*    /STUVWXYZ*,(
      C NEG. -JKLMNOPQR-$*    /STUVWXYZ*,(   01234567890$='   +ABCDEFGHI+.)
      C  THESE ARE INTERPRETED INTO THE CORRECT NOS.FOR PRINTING.
      C
    2         REAL FLSCL(M1) , RANGE , RATIO , TRY
    3         INTEGER CHAR(M) , POINT(102)
    4         IF ( M1 .GT. M ) WRITE(6,206) M , M1
    7         DO 161 K = 1 , M , 1
   10         IF ( CHAR(K) .LT. 0 ) CHAR(K) = 32 - CHAR(K)
   13     161 CHAR(K) = CHAR(K) - CHAR(K) / 64 * 64
   15         DO 164 K = 1 , M1 , 1
   16         RANGE = FLSCL(K)
   17         FLSCL(K) = ABS(RANGE)
   20         IF ( FLSCL(K) .NE. 0.0 ) GO TO 151
   23         WRITE(6,210) K , RANGE
   24         RANGE = 10.0
   25         FLSCL(K) = 10.0
   26         GO TO 153
   27     151 IF ( FLSCL(K) .LE. 100.01 ) GO TO 152
   32         FLSCL(K) = FLSCL(K)/10.
   33         GO TO 151
   34     152 IF ( FLSCL(K) .GT. 10. )  GO TO 153
   37         FLSCL(K) = FLSCL(K)*10.
   40         GO TO 152
   41     153 DIVN = 1.
   42         IF ( FLSCL(K) .GT. 16.67 ) DIVN = 2.
   45         IF ( FLSCL(K) .GT. 33.33 ) DIVN = 5.
   50         RATIO = RANGE / FLSCL(K)
   51         FLSCL(K) = DIVN * 100. / AINT ( DIVN * 100. / FLSCL(K) + 0.01 )
   52         DO 154 J = 1 , 101 , 1
   53     154 POINT(J) = -17 179 869 184
      C THIS SETS INITIAL BLANKS INTO THE PRINT POSN.
   55         DO 160  J1 = 1 , 21 , 1
      C  THE MAXIMUM NUMBER OF SCALE MARKS IS 21,INCLUDING THE ZERO MARK
   56         TRY = FLOAT(J1 - 1) * DIVN
   57         J = TRY / FLSCL(K) * 100. + 1.01
   60         IF ( J .GT. 101 ) GO TO 155
      C  THIS TESTS WHETHER ALL LABELS HAVE BEEN WRITTEN INTO POINT
   63         POINT(J) = TRY
   64         IF ( POINT(J) .LT. 10 ) POINT(J) = POINT(J) * 1 073 741 824
   67         IF ( POINT(J) .GT. 1000 .OR. J .EQ. 1 ) GO TO 160
   72         POINT(J-1) = POINT(J) / 10
   73         POINT(J) = (POINT(J) - POINT(J-1) * 10) * 1 073 741 824 + 2
   74         POINT(J-1) = POINT(J-1) * 1 073 741 824
   75     160 CONTINUE
   77     155 FLSCL(K) = FLSCL(K) * RATIO
```

Table H-5. Computer Listing of Program SCALES (Sheet 2 of 2)

```
PETER BRADSHAW   03  TC              FORTRAN SOURCE LIST          SCALES    02/23/67
  ISN       SOURCE STATEMENT

  100       WRITE(6,212) K , (POINT(J),J = 1,101,1) , RATIO
  105       POINT(102) = -17 179 869 184
  106       DO 156 J = 1, 101 , 1
  107       IF(POINT(J).NE.POINT(J+1).AND.POINT(J+1).EQ.(-17 179 869 184))
           1  GO TO 157
  112       POINT(J) = -32
  113       GO TO 156
  114   157 POINT(J) = 25 * 1 073 741 824
  115   156 CONTINUE
      C  THIS PUTS THE SCALE MARKS INTO POINT TO LINE UP WITH THE LABELS
  117       J1 = 0
  120       POINT(1) = 17 179 869 184
  121       POINT(102 ) = -17 997 958 192
  122       IF ( M1 .NE. 1 ) POINT(102) = 24 270 848 028 + CHAR(K) * 64
  125   164 WRITE(6,202) J1 , (POINT(J),J = 1,102,1)
  133       DO 167 K = 1 , M , 1
  134   167 IF (IABS(CHAR(K)) .GE. 32 ) CHAR(K) = CHAR(K) / 32 * 32 - CHAR(K)
  140       RETURN
  141   202 FORMAT ( 1H    ,I5 ,  1X   , 101A1 , 1A8 , 12A1 )
  142   206 FORMAT ( 46H THE VALUES OF 'M' AND 'M1' DO NOT COMPARE AT ,213    )
  143   210 FORMAT ( 24H THE VALUE GIVEN FOR THE , I3 , 25HTH SCALE IS TOO SMALL
          ALL AT , 1F10.3 , 26H.A VALUE OF 10 IS ASSUMED. ,       1X)
  144   212 FORMAT ( 1H    ,I5 ,  1X   , 101A1 , 1P1E8.1 )
  145       END
```

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Regis C. Hilow - Project Engineer	Rome Air Development Center (EMERR) Griffiss AFB, N.Y. 13440

13 ABSTRACT

Work performed under this contract is divided into two main parts: (1) a Test and Data Analysis program designed to produce a method for reliability screening; and (2) a Physics of Failure Program on fundamental mechanisms causing device degradation. The test program was divided into three parts, Preliminary, Main and Verification Test Programs. Results of each test program are discussed. Accelerated test results and comparison of fixed stress and step stress results are presented. A non-destructive screening procedure was developed and is contained in this report. Three computer programs, SERF, LINDA 1 and LINDA 2, were developed to assist in the development of the nondestructive screening procedure. The Physics of Failure Program consisted of studies of surfaces and oxides, noise, thermal effects and second breakdown. Extensive analyses of failures were also carried out. Surface studies included the development and analysis of techniques for the production of metal-oxide-silicon (MOS) systems that are electrically and thermally stable. This work is summarized in another volume of the final report (RADC-TR-66-776). Thermal studies include results of actual temperature measurements of operating transistors using an infrared (IR) microradiometer. Results of electrical and thermal techniques are compared as a tool for measuring thermal resistance. Models to calculate the current and temperature distributions in operating power transistors give results which are in agreement with experimental data. The second breakdown studies include a discussion of a model for thermal breakdown.

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14. KEY WORDS	LINK A		LINK B		LINK C	
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Test Programs						
Computer Program Development						
Thermal Studies						
Second Breakdown Studies						

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