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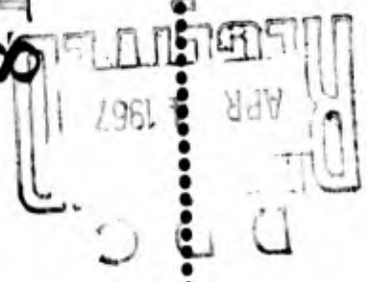

TECHNICAL REPORT ECOM-00109-F

LOW NOISE L-BAND TRANSISTOR AMPLIFIER

FINAL REPORT

By

Leslie Read

March 1967

ECOM

UNITED STATES ARMY ELECTRONICS COMMAND · FORT MONMOUTH, N.J.

Contract No.: DA 28-043 AMC-00109(E)

TEXAS INSTRUMENTS
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Technical Report ECOM-00109-F March 1967

LOW-NOISE L-BAND (WIDEBAND) TRANSISTOR AMPLIFIER

FINAL REPORT

1 June 1964 to 31 May 1966

Report No. 8

Contract No. DA28-043 AMC-00109(E)

DA Project No. IE6-22001-A-056, Task 04

Prepared by

Leslie W. Read

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For

U. S. Army Electronics Command
Fort Monmouth, New Jersey

ABSTRACT

This is the final report on the design and fabrication of a wideband microwave balanced amplifier. This amplifier, designed for the 1-2 GHz band, uses thin-film components on ceramic substrates. Circuit design of directional couplers and gain modules is discussed, amplifier performance is presented, and the thin-film processes used are explained.

It is concluded that this type of amplifier is extremely useful in microwave systems where low noise, low VSWR, and high reliability are desirable.

FOREWORD

A low-noise L-band transistor amplifier was developed, using stripline techniques on ceramic substrates, for the U. S. Army Electronics Command, Fort Monmouth, New Jersey, under Contract No. DA 28-043 AMC-00109(E), DA Project No. IE6-22001-A-056, Task 04. The work is part of Texas Instruments effort to develop microwave integrated circuits for radar and communications systems. For the amplifier development project, the author gratefully acknowledges the contributions of the following persons: Charlie White and Bernie Landress for supplying transistor chips; George Johnson for his personal interest and excellent supervision; Charlie Earhart for initiating the author into thin-films technology; Gary Policky for help in computer programming; and Bob Hawkins for the fabrication and evaluation of innumerable amplifiers and couplers

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SECTION I

INTRODUCTION

The idea of a wideband balanced amplifier using couplers to reduce terminal VSWR was first proposed by Eisele, Englebrecht, and Kurokawa [1] in February 1965. Subsequent articles gave more detailed information about the L-band amplifier originally described. [2,3] Use of the technique at S-band was presented in February 1966. [4]

This report covers design and construction of an L-band thin-film balanced amplifier on a ceramic substrate. It includes discussion of both the coupler and gain module design. Special emphasis is placed on the effect of coupler characteristics on amplifier performance and on the design limitations imposed by thin-film construction.

A basic schematic of the balanced amplifier is shown in Figure 1. When the coupling is exactly -3 dB and the transistors are identical, reflections from the transistors cancel at the input or output and a low VSWR is obtained. This permits simultaneous realization of optimum source for minimum noise figure and low VSWR, a condition not generally achievable without use of couplers.

This report first describes the L-148 germanium device and its electrical characteristics. Design of the gain module — the section of the amplifier which contains the transistor and the bias and gain compensation networks — is then reviewed. Next, the directional coupler's design is discussed. Finally, the report presents the performance of a prototype balanced amplifier using the gain modules and directional couplers.

The amplifier design objectives were

Gain	20.0 ± 0.5 dB
Bandwidth	1.0 to 2.0 GHz
Noise Figure	6.0 dB
VSWR	1.1
Phase Shift	± 6°

This performance was not achieved by the models constructed; 18 dB nominal gain, 7 dB noise figure, and 1.5:1 nominal VSWR were obtained from the six-stage model. Reasons for the deviation are discussed in the report.

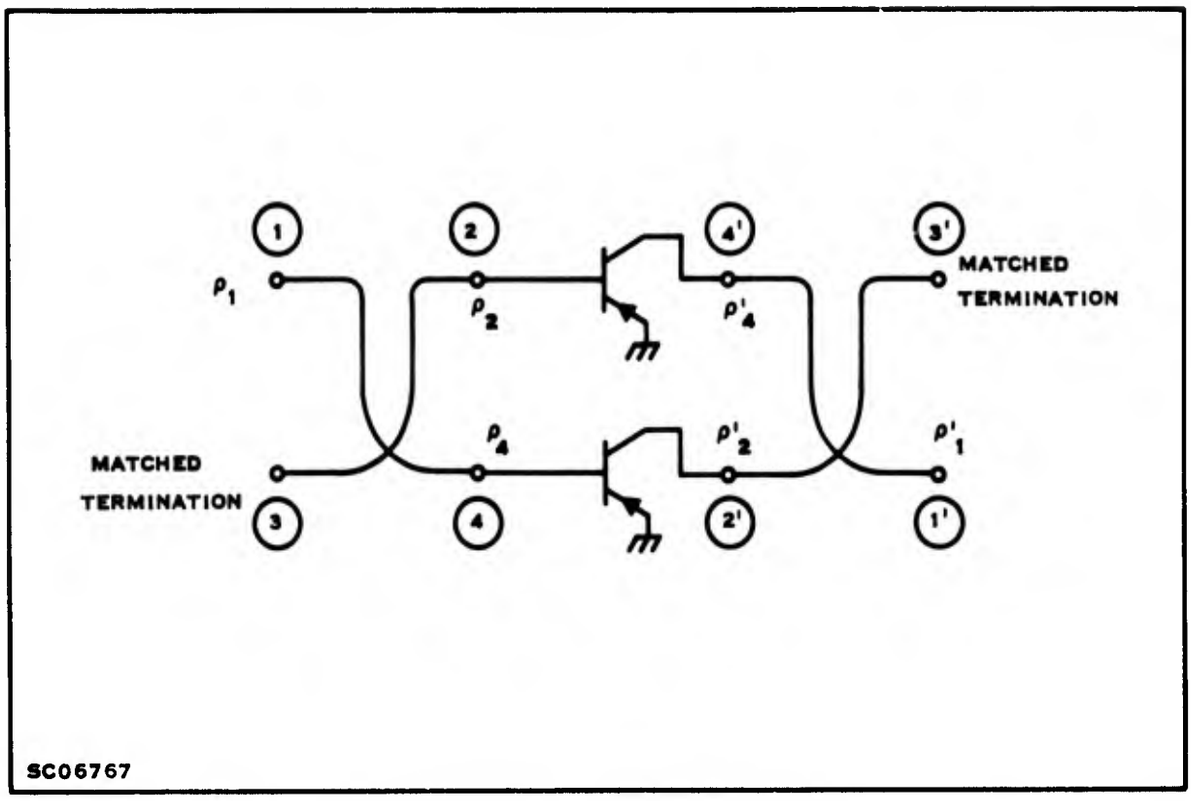


Figure 1. Single-stage-coupler Amplifier

SECTION II

TRANSISTOR

A. PHYSICAL DESCRIPTION

The transistor used in the amplifier is designated L-148. This is a germanium planar device designed for small-signal, low-noise, high-frequency amplifiers. Figure 2 shows the dimensions of the active areas. Figure 3 is a photograph of the active areas of the device.

B. ELECTRICAL CHARACTERISTICS

1. Measured Gain and Noise Figure

Electrical characteristics of the L-148 are shown in Figures 4 through 7. This transistor typically has 2 GHz f_t and 6 GHz F_{max}. Figure 4 gives the minimum noise figure, and the maximum gain attainable with that figure. Degradation caused by a 50-Ω source and conjugate load is seen in Figure 5, which shows gain and noise figure under that condition.

2. Optimum Source Admittance

The source admittance which gives this minimum noise figure is presented in Figure 6. This was measured by recording the lengths of the input double-stub tuner when the noise figure was at a minimum on the noise-figure test set. The tuner was then put on the automatic immittance plotter and the transistor source admittance plotted (after correcting for the reference plane shift in the test jig).

3. S-parameters

a. Discussion

It is desirable to have a set of terminal parameters in order to design an amplifier. This is true especially at microwave frequencies, where package and chip parasitics make an accurate equivalent circuit difficult to obtain.

Theoretically any set of parameters (h, y, z, etc.) can be used, but practically the S (scattering) parameters are best because they can be determined more

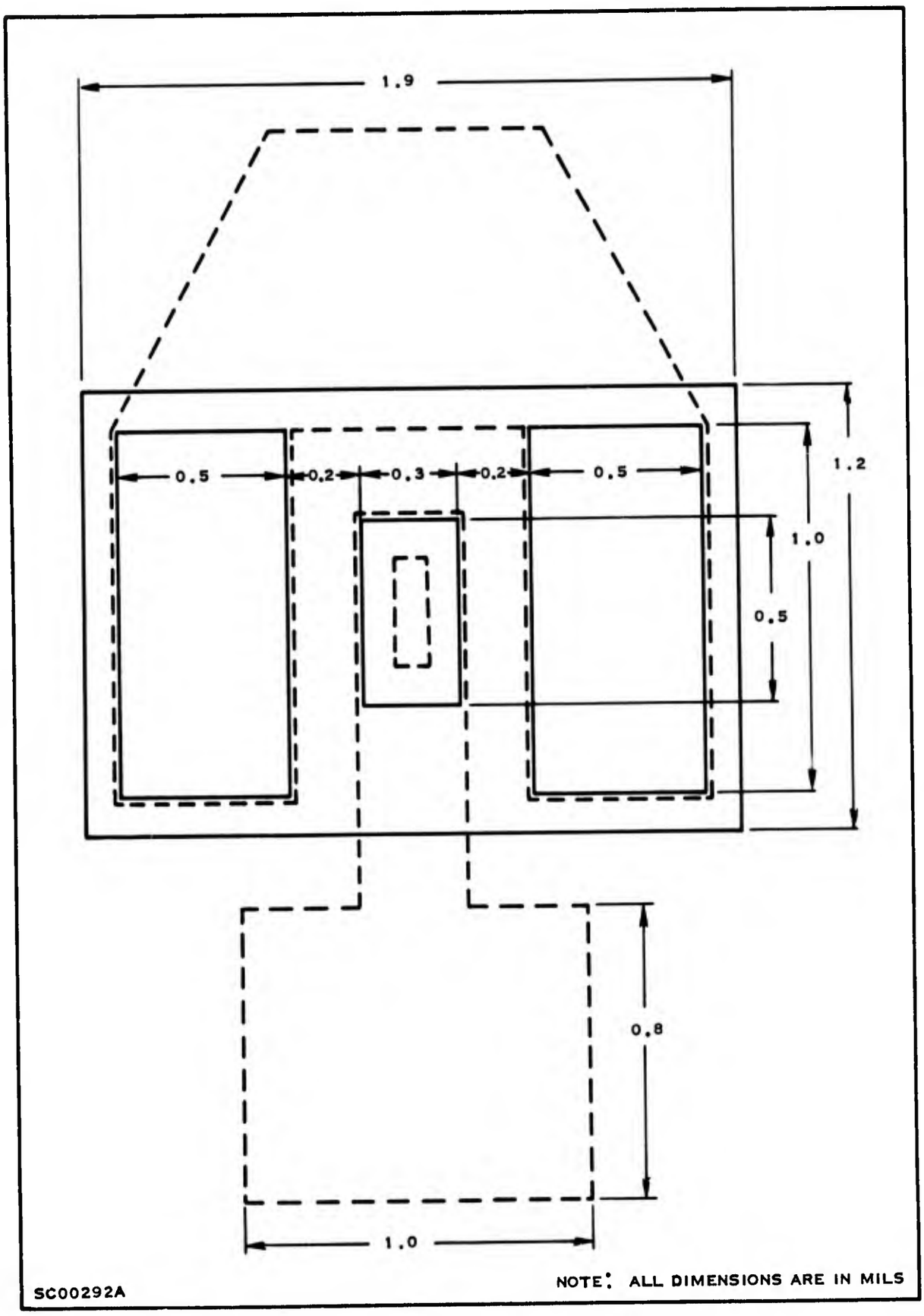


Figure 2. Critical Dimensions of L-148 Pattern

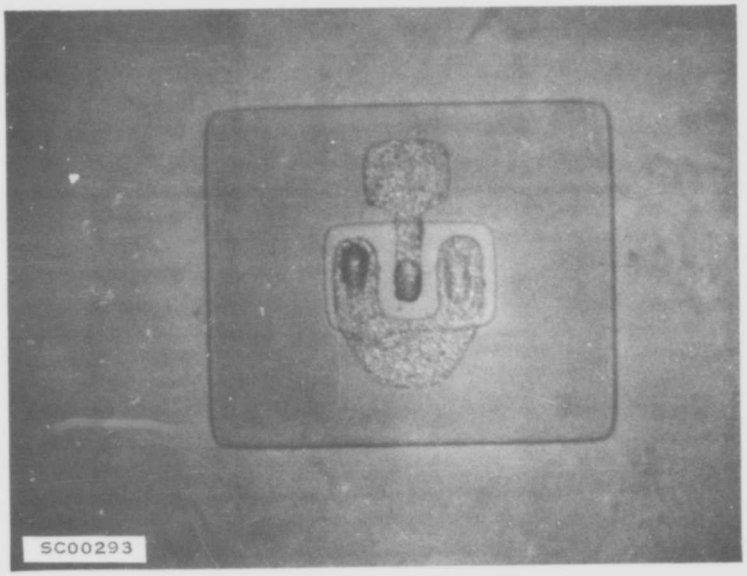


Figure 3. L-148 Device

accurately and they are more pertinent to microwave design. They are much easier to measure than short or open circuit parameters at microwave frequencies because the device under test can be terminated in 50 Ω at all ports, instead of maintaining a short or (worse yet) an open circuit at some ports. S-parameters are discussed in Appendix B.

b. Measured Parameters

S-parameters for L-148 at 9 V and 2 mA are shown in Figure 7 as a table and also on a reflection-coefficient chart. A Smith-chart outline is superimposed on the center to give some idea of the impedances the parameters represent.

It is interesting to notice that S_{12} and S_{22} do not appear to change with frequency. There is of course, a small variation, but so small that it is masked by errors in measurement and by device variations.

These S-parameters were used in the design of the gain modules.

4. Chip Selection for Amplifiers

Selection of chips actually to be used in the amplifier was a severe problem. Two solutions were proposed: 1) Measure the chip in a package, and then carefully

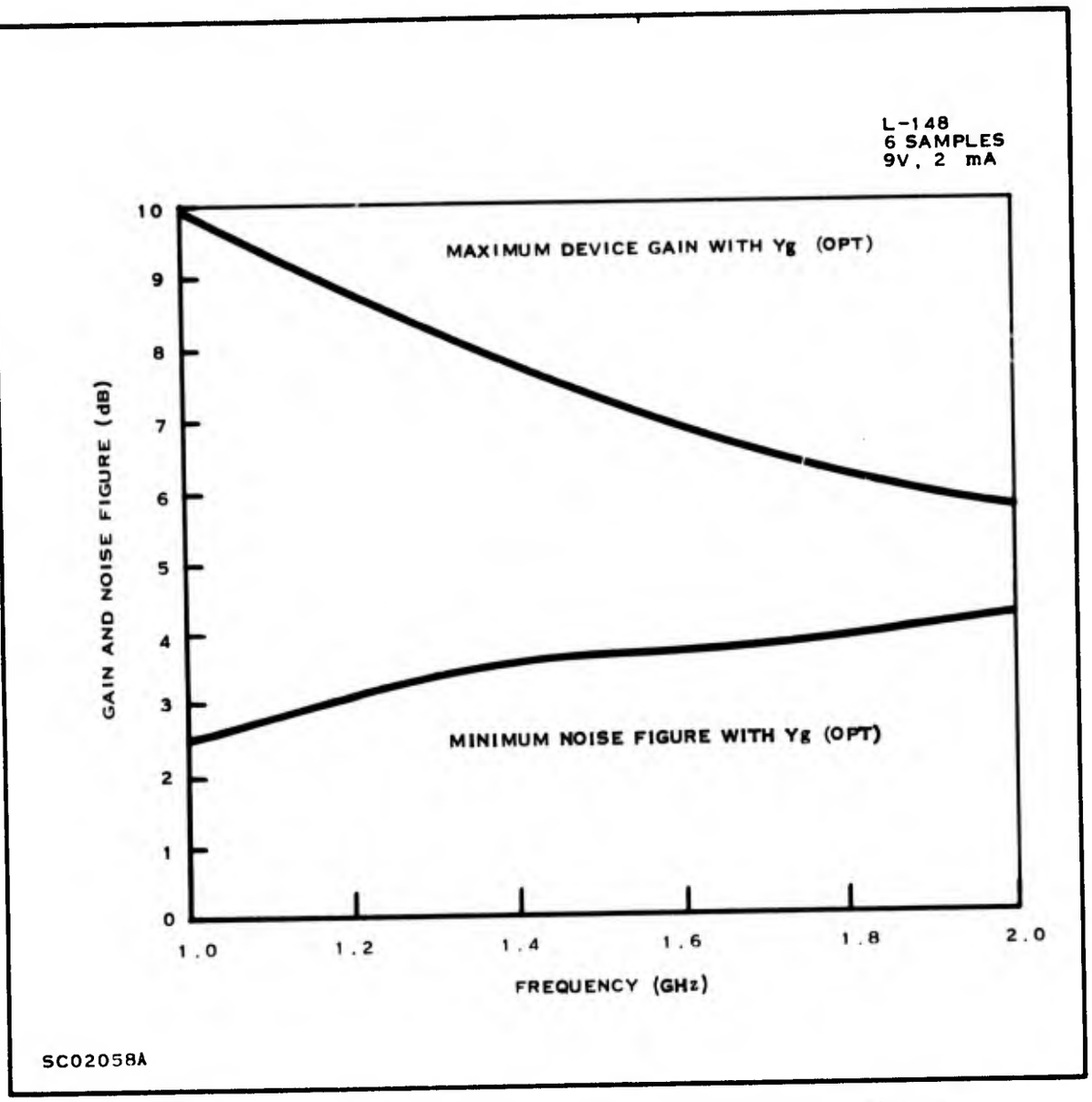


Figure 4. L-band Gain and Noise Figure of L-148 Transistors

remove the chip and put it on the circuits; or 2) measure the chip alone in a probe test set before mounting on the circuit.[5] The packaged chip can be characterized more completely for noise figure and S-parameters, but the chip can be ruined by too much handling. At this time, only 50 Ω insertion gain at 1.0 GHz, or thereabouts, can be measured on the unpackaged chip. However, this is a good figure of merit for the devices, and the bulk of the chip selection was done using 1.0 GHz gain as a criterion.

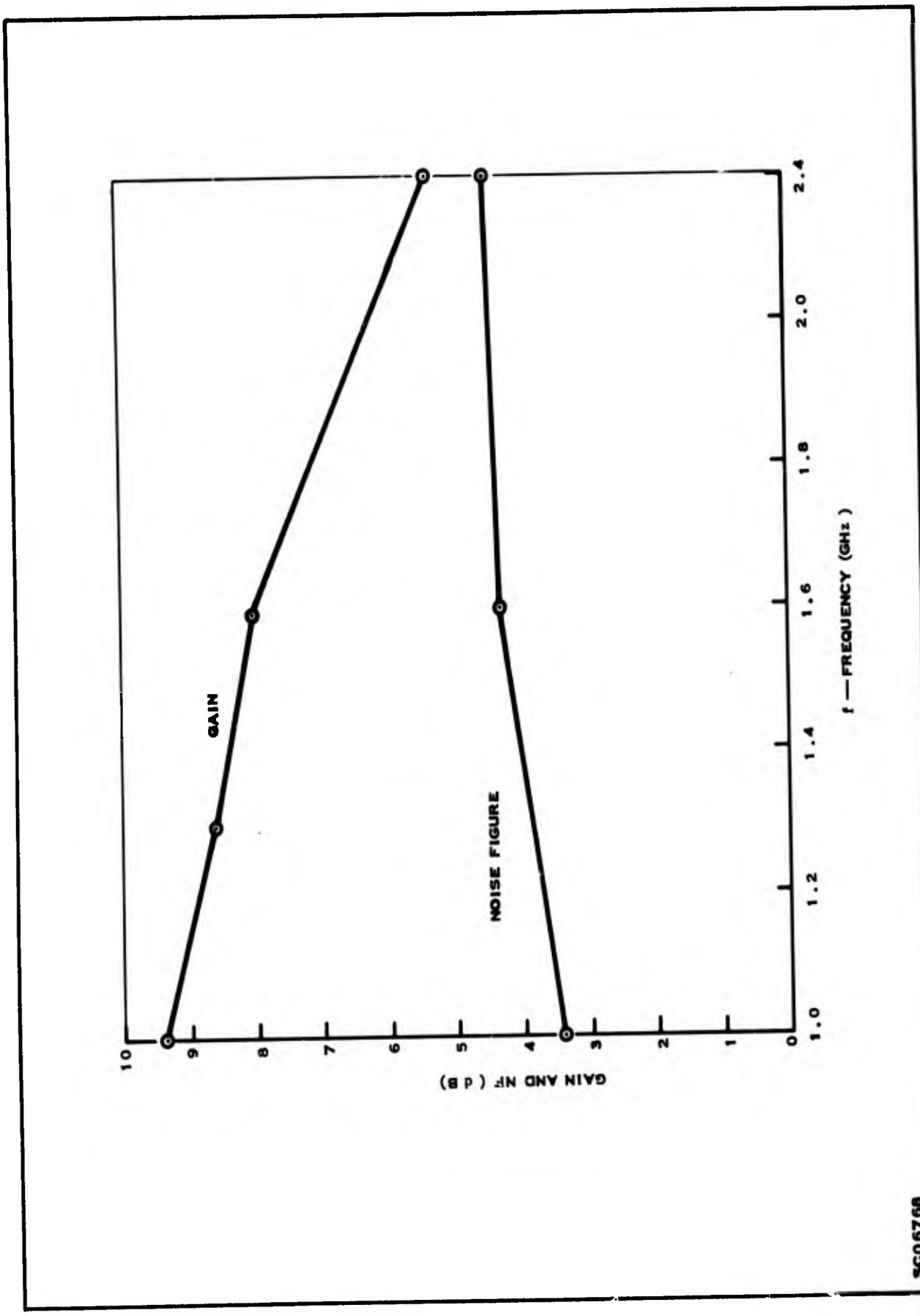


Figure 5. Noise Figure and Maximum Gain with 50-Ω Source Impedance and a Conjugate Load at Collector: L-148, 9 V, 2 mA

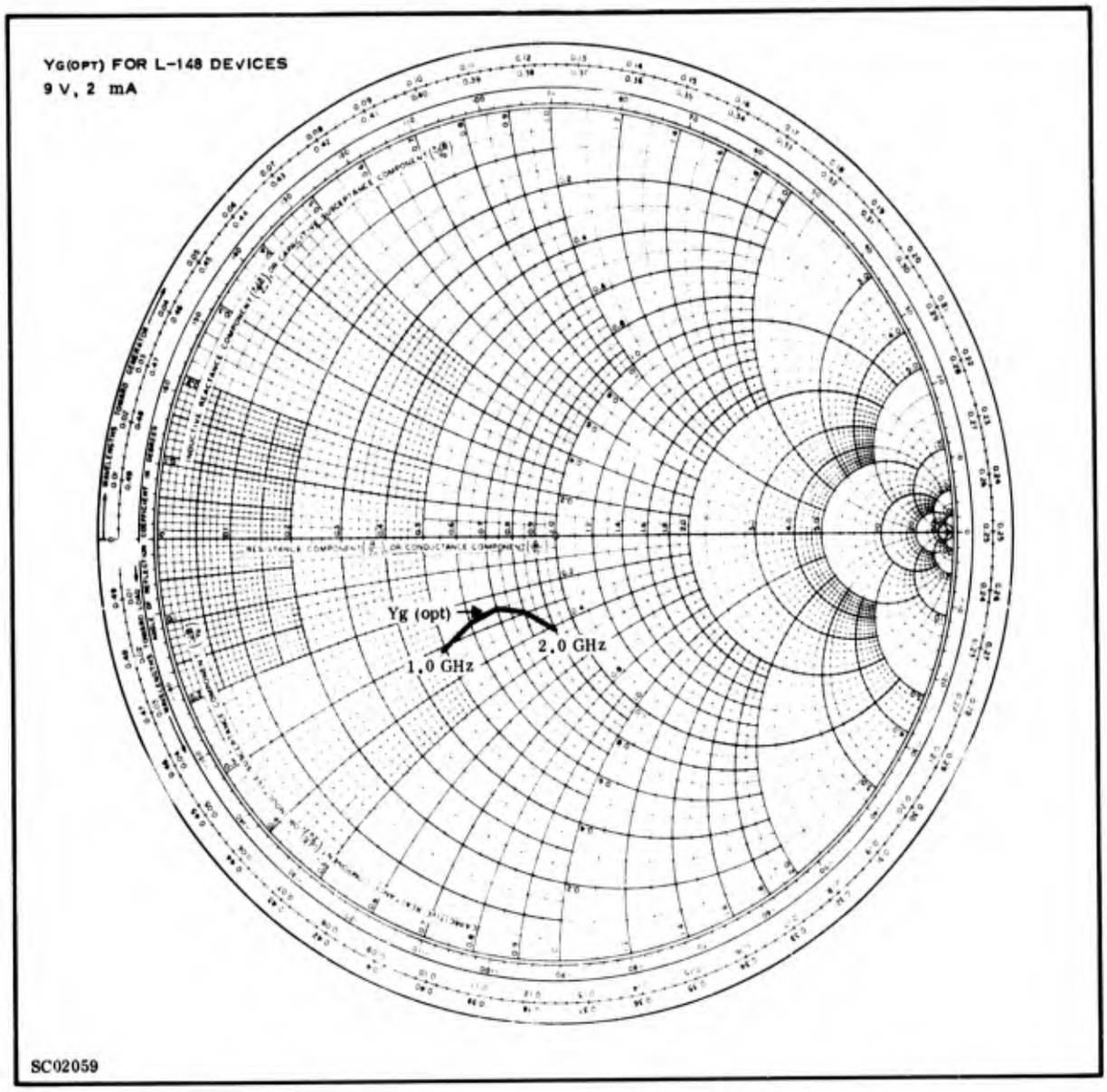
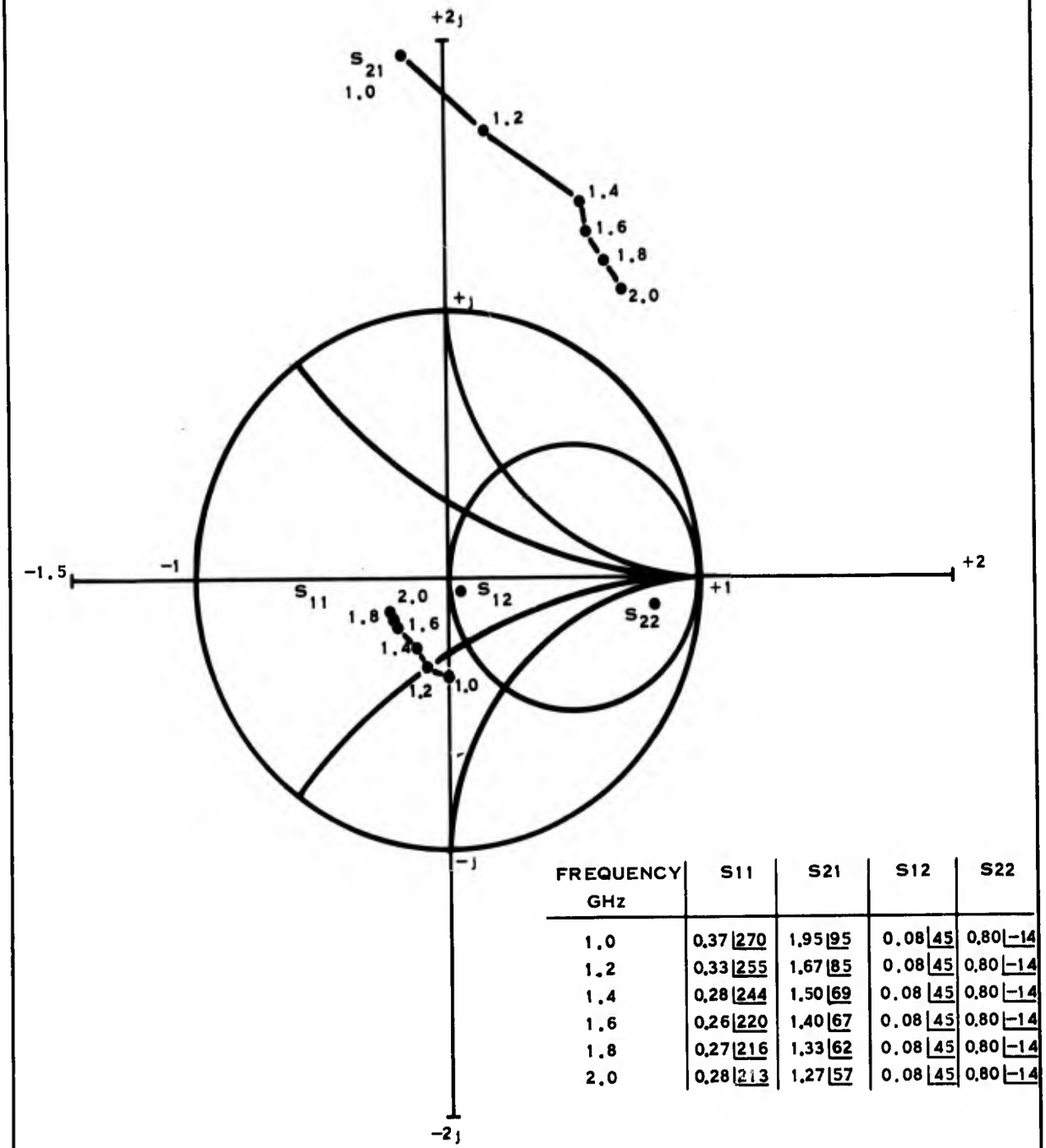


Figure 6. $Y_{g(opt)}$ for L-148 Devices



FREQUENCY GHz	S11	S21	S12	S22
1.0	0.37 | 270	1.95 | 95	0.08 | 45	0.80 | -14
1.2	0.33 | 255	1.67 | 85	0.08 | 45	0.80 | -14
1.4	0.28 | 244	1.50 | 69	0.08 | 45	0.80 | -14
1.6	0.26 | 220	1.40 | 67	0.08 | 45	0.80 | -14
1.8	0.27 | 216	1.33 | 62	0.08 | 45	0.80 | -14
2.0	0.28 | 213	1.27 | 57	0.08 | 45	0.80 | -14

Figure 7. L-148 S-parameters — 9 V, 2 mA

SECTION III

THIN-FILM TECHNIQUES

All of the passive linear components used in the amplifier transmission lines, resistors, and capacitors were formed by thin films deposited on a ceramic substrate. This section will discuss the methods used to form these elements.

A. METALLIZATION

Figure 8 gives a step-by-step illustration of the process of thin-film metallization. Tantalum is sputtered on a substrate and the line pattern photomasked so that the lines are covered. The tantalum is then selectively etched. Next a layer of chrome-gold is evaporated over the whole substrate. After the chrome-gold is deposited the pattern is again masked, this time with lines exposed, and the exposed lines are plated to the desired thickness ($\approx 200\ \mu m$). The chrome-gold is then etched away, leaving the desired plated lines.

The purpose of the tantalum is to provide good adhesion between the chrome-gold and the smooth ceramic surface. The chromium serves a similar purpose: it is a material to which both gold and tantalum adhere. Lines made in this manner normally have minimum width of 1.0-2.0 mils, although widths of 0.5 mils are possible for short distances. Narrowest line width of the amplifier discussed in this report was 2.5 mils.

B. RESISTORS

Resistors used in this amplifier are made by anodizing the tantalum to the desired resistivity. Figure 9 shows the process. Tantalum as originally sputtered has a certain sheet resistivity (given in ohms per square). This is determined by the thickness and sputtering technique. Anodization produces tantalum oxide, a dielectric material, and reduces the effective thickness of the conductor, thus increasing sheet resistance. Typically, one would start with sputtered tantalum having 20 $\Omega/\square$ and anodize until the resistance is 50 $\Omega/\square$. Resistances as low as 10 $\Omega/\square$ and as high as 100 $\Omega/\square$ are possible, but not as desirable. Resistors used in the amplifier ranged from 50 Ω to 4300 Ω.

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C. CAPACITORS

Capacitors are formed in the same manner as resistors, except that a top plate is formed by metallizing over the tantalum oxide dielectric (see Figure 10). The capacity values are approximately 0.5-1.0 pF/square mil of capacitor area. It is desirable that for highest breakdown voltage the top plate be negative and the bottom plate be positive; however, reverse polarity is possible at reduced voltages. Aluminum is used under the tantalum bottom plate to improve conductivity and reduce losses.

Tantalum capacitors have relatively high capacity for a given unit area. Where small capacitors are desired the areas become impracticably small. To make the areas feasible, silicon oxide can be sputtered on top of the tantalum to increase plate separation and reduce the capacity/unit area by a factor of 10 or more. Silicon oxide was not used in this amplifier as all capacitors were large-bypass capacitors and not critical.

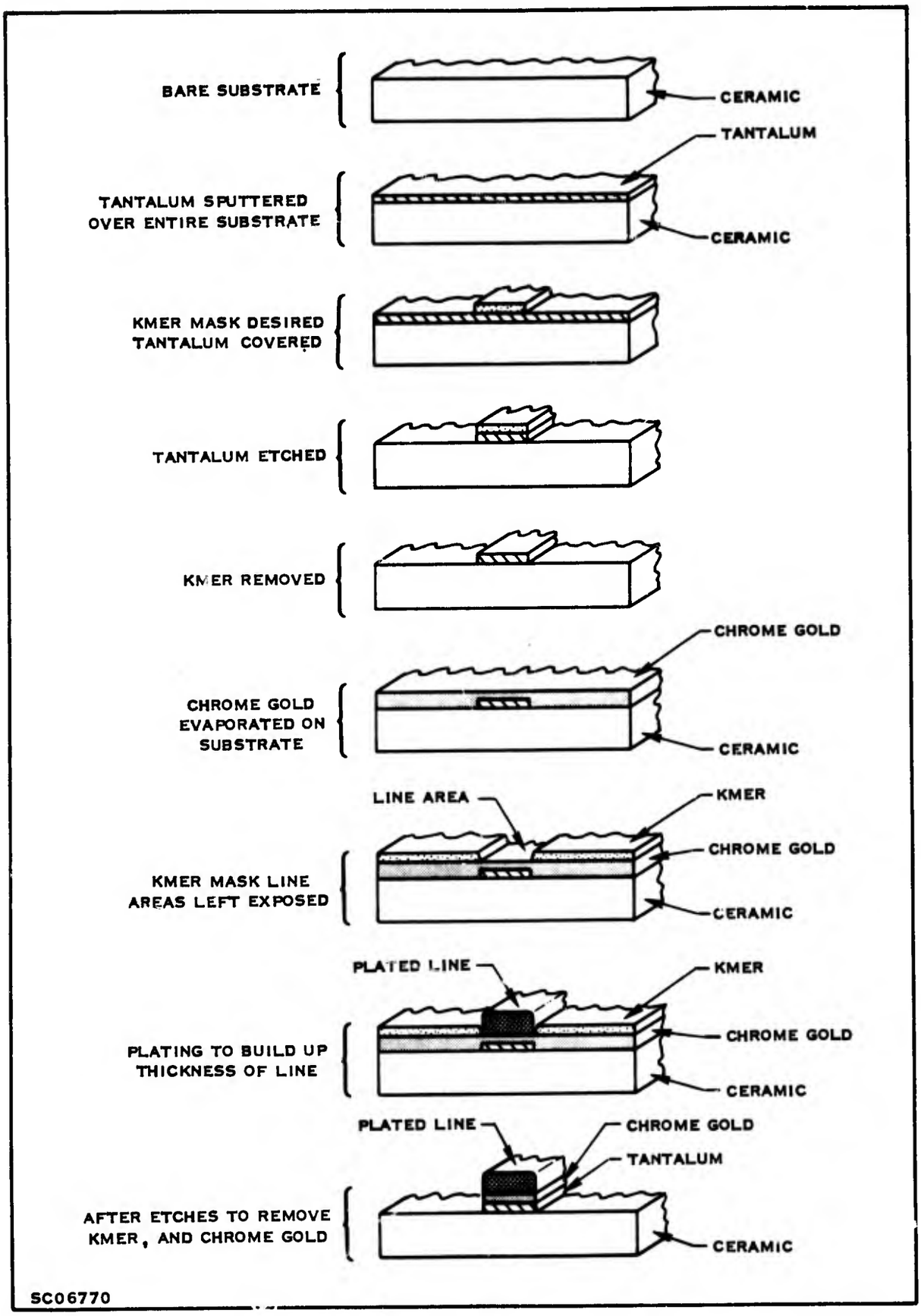

Figure 8. Formation of Lines

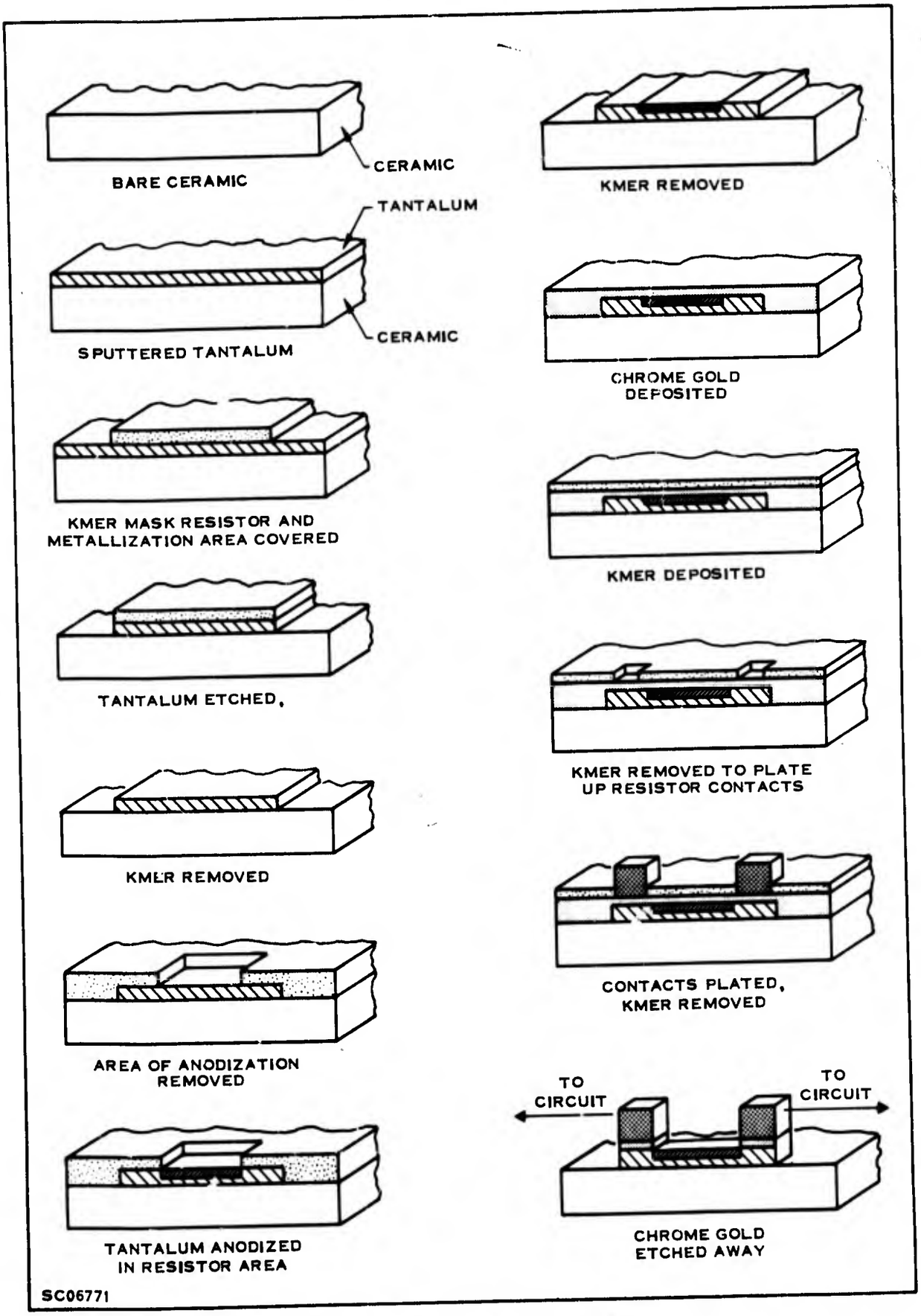

Figure 9. Resistor Formation

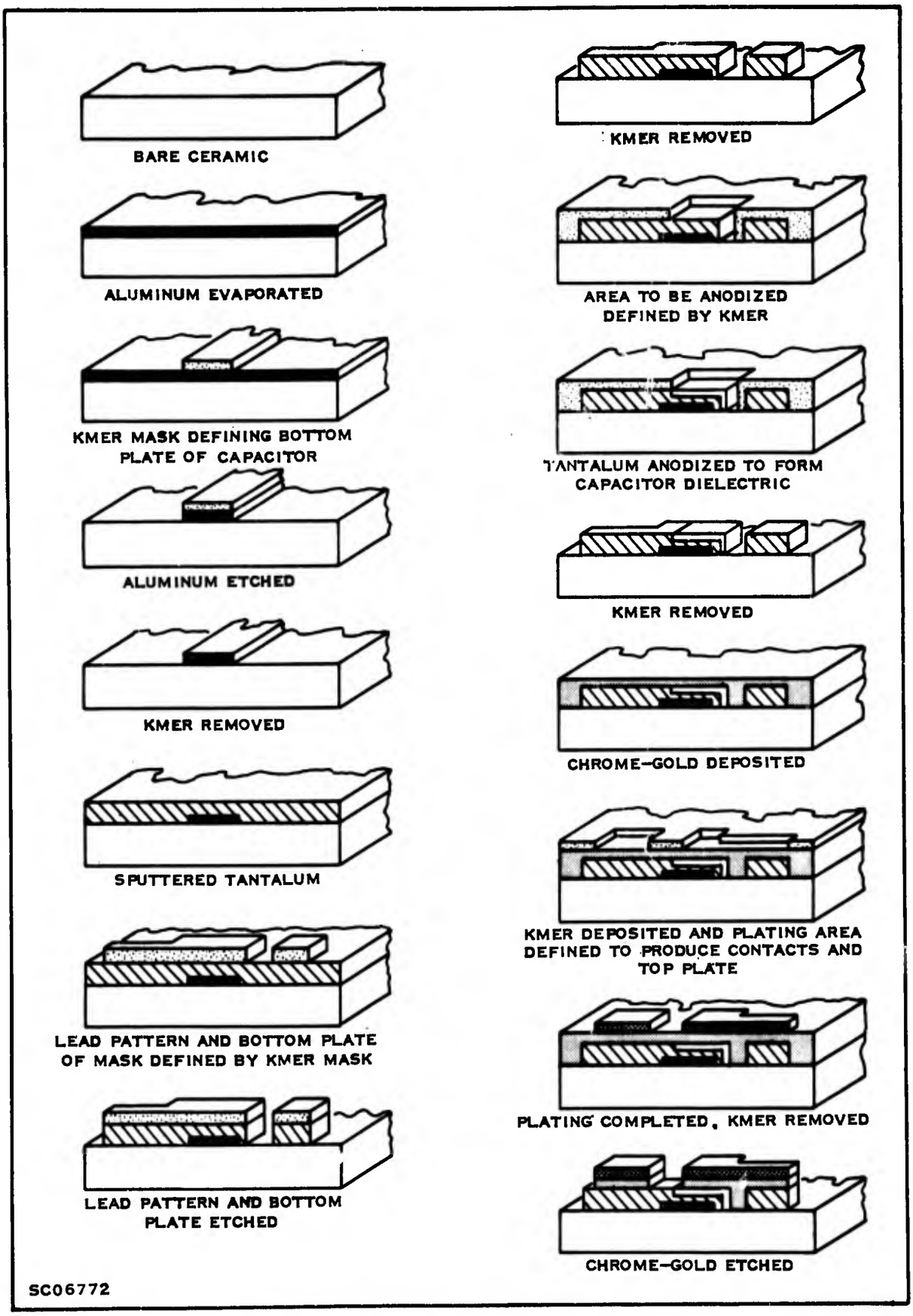

Figure 10. Capacitor Formation

SECTION IV

GAIN MODULE

Early in the program it was decided to design the amplifier in two simultaneous efforts: the directional coupler, and the gain module (containing the device, bias networks, and tuning elements). This section of the report covers the design of the gain module.

A. DESIGN OBJECTIVES

The gain module had the following design goals for 1-2 GHz:

Gain: 5 dB including coupler loss

Noise: 4.9 dB including coupler loss

Ripple: ±0.1 dB

In addition to the electrical goals, it was felt that the following guidelines would make the modules easier to fabricate and more reproducible:

1) The only capacitors would be bypass and coupling capacitors. These are all high value (≥ 500 pF) and do not need silicon oxide dielectric to reduce the capacity, thereby eliminating a processing step.

2) Both input and output networks would consist only of transmission lines of varying lengths and characteristic impedance. Resistors would be used only for biasing; amplifier response would then depend only on the dimensions of the metal lines, which can be precisely controlled, and the substrate properties.

3) The input network would be used to minimize noise figure. The output network is employed to flatten the gain by increasing the mismatch loss at the output. Normally, when designing an amplifier for low VSWR, one would either attempt to match to the transistor output across the band, or include a resistor in the output network. In a balanced configuration the mismatch reflections cancel in the directional coupler, and mismatch loss can be used to get flat gain at no sacrifice of VSWR.

4) The ripple figure of ±0.1 dB was difficult to achieve because of characterization limitations and device variations. Previously ±0.5 dB had been considered realistic accuracy for gain prediction. Consequently it was decided to trim the gain by adjusting supply voltage to each stage.

B. DESIGN TECHNIQUES

1. Bias

First step in the gain module design was the selection of a bias point; 9 V, 1.5 mA being selected as optimum because some devices showed a slight improvement in noise figure over the 9 V, 2 mA point.* Actually the optimum bias point is broad. It was experimentally noted that a device with higher gain would have that gain at higher current — sometimes as high as 2.3 mA. A device with low gain would "peak out" at lower current. The design bias network is shown in Figure 11.

2. Source Admittance

Next step was the selection of an input network. Its function is to furnish the transistors a source admittance approximating $Y_{g(opt)}$ (see Figure 6) as closely as is practical.

Several configurations were evaluated. Degradation in noise figure when the source is not $Y_{g(opt)}$ can be calculated from the equation.[7]

$$F = F_{min} + \frac{Rn}{Gg}\left[(Go-Gg)^2 + (Bo-Bg)^2\right]$$

where

F = numeric noise figure with source Yg - Gg +, Bg

F_{min} = numeric minimum noise figure with source $Y_{g(opt)}$ = Go +, Bo

R_n = constant — a function of frequency, device, and bias

Gg, Bg = real and imaginary admittance components of source being evaluated

Go, Bo = real and imaginary admittance components of optimum source

---

* Devices on the circuits biased at 9 V, 1.75-1.8 mA, which was the original bias level set in the PEM[6] specs for the devices. This is probably as close to an optimum bias as exists.

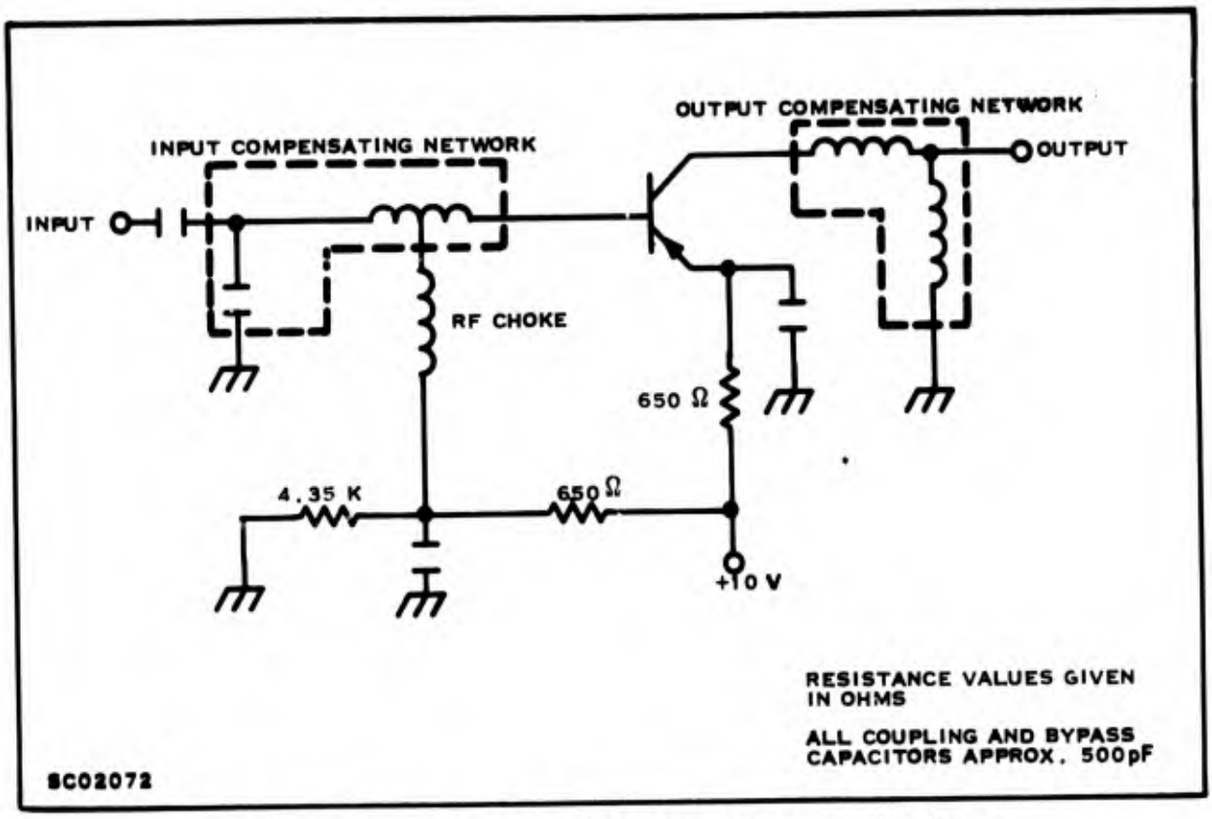

Figure 11. Schematic Diagram of Ceramic Amplifier

For L-148 devices it is approximately true in the 1-2 GHz region that

$$F = F_{min} + \frac{0.05}{Gg}\left[(Go-Gg)^2 + (Bo-Bg)^2\right]$$

if the admittances are in millimhos.

On the basis of the calculated noise figure, a capacitive stub placed a distance away from the base and transformed with a length of line was chosen as the input compensating network. The stub has a susceptance of j11 mmho at 2.0 GHz and is placed 0.166 wavelengths (at 2 GHz) from the base. A 60-Ω line 384 mils long is used between the stub and the base.* Bias was furnished by a high-impedance line (≈ 85 Ω) a quarter wavelength long at 1.5 GHz.

---

* A value of 2.5 was used for $\sqrt{\epsilon_r}$ because microstrip circuitry (one ground plane) is employed. If a top plate of ceramic were used, making the dielectric homogeneous, $\sqrt{\epsilon_r}$ would be 3.0. Since part of the field lines is in air which has $\epsilon_r = 1$, the effective dielectric constant is lower than it would be if dielectric were homogeneous.

Figure 12 shows dimensions of the complete input network. Figure 13 gives the calculated Yg of the input network and the actual measured Yg as measured on the Rantec plotter. In comparing the measured and calculated data it appears that the capacity added by the stub is more than the calculated value.

Calculated noise figure for this circuit, with F_{min} for comparison, is as follows:

Calculated NF		F_{min}
(GHz)	(dB)	(dB)
1.0	3.0	2.5
1.3	3.5	3.3
1.6	3.7	3.6
2.0	4.3	4.2

No significant degradation is apparent.

3. Load Admittance

a. Function

Function of the output network is to show the device a load impedance across the band that will keep the gain constant, given specified device characteristics and previously determined source conditions.

b. Basic Configuration — Initial Design

The initial question was the basic configuration of the network; at least one shorted section was mandatory to prevent low-frequency oscillations, and a high-impedance-series section was desirable to act as a broadband transformer. An L-section (shown in Figure 14), used on a teflon fiberglass prototype amplifier, gave fairly good results across the band.[8] This was done before accurate device parameters were available, and the best line dimensions were experimentally determined. On the basis of these teflon fiberglass boards, impedances and line lengths for the output circuit were measured. The ceramic circuit layout was initially made using these electrical dimensions. The layout was made, however, so that changes in line width or length could be made without extensive alterations. Thus the initial ceramic design was largely empirical, awaiting more accurate device characterization data.

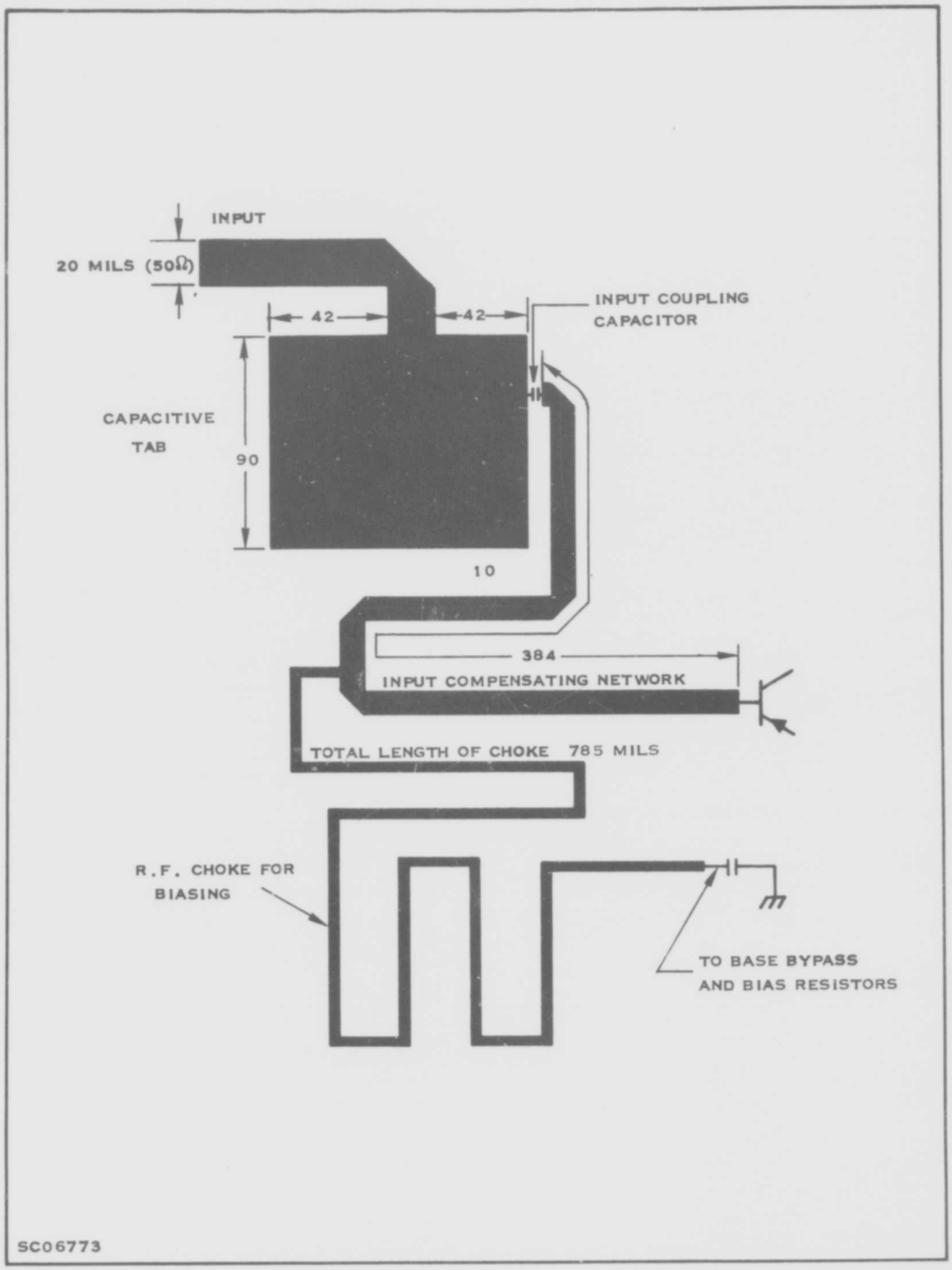

Figure 12. Input Circuit Used in Gain Module

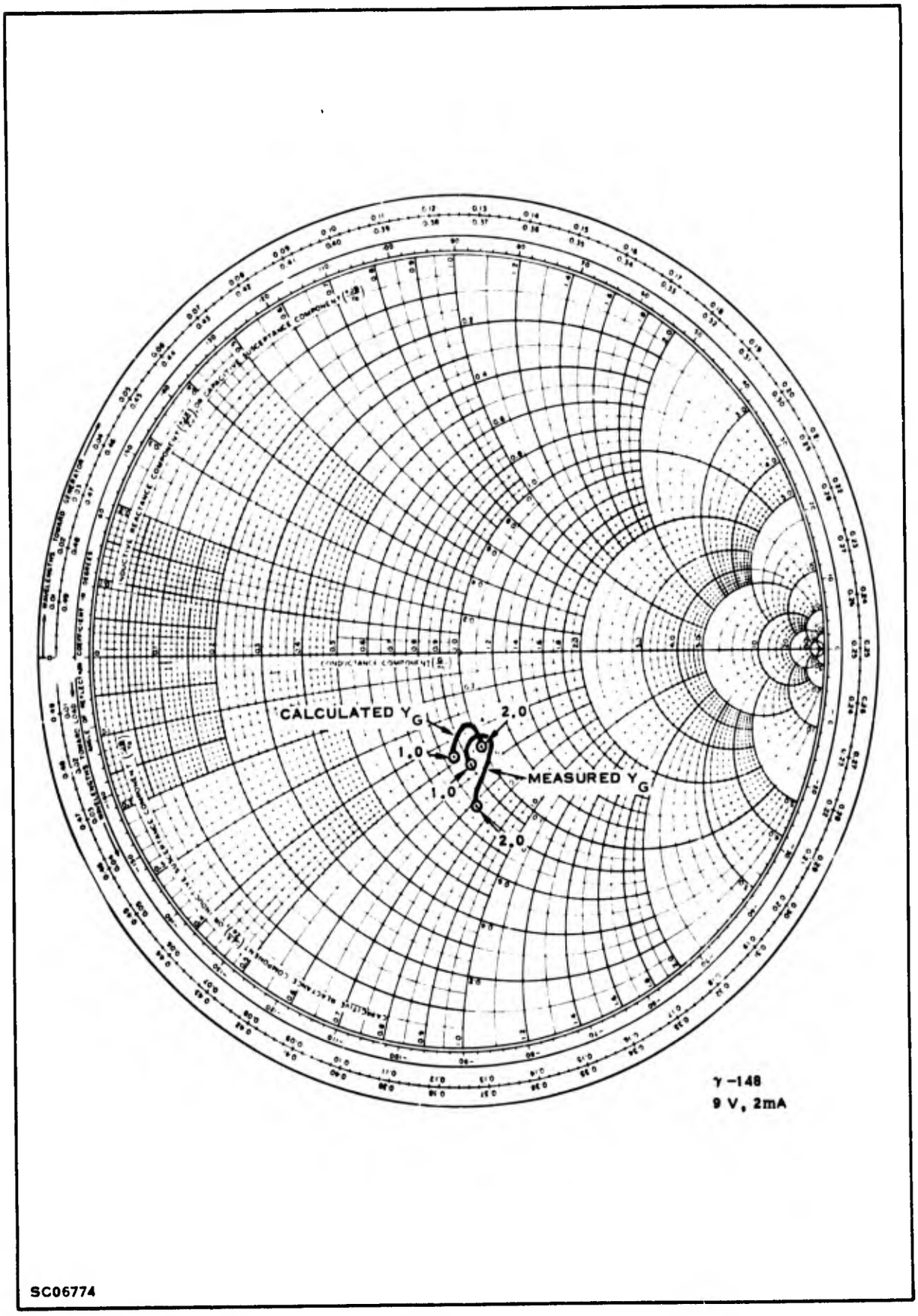

Figure 13. Measured and Calculated Source Admittance to Approximate $Y_{g(opt)}$

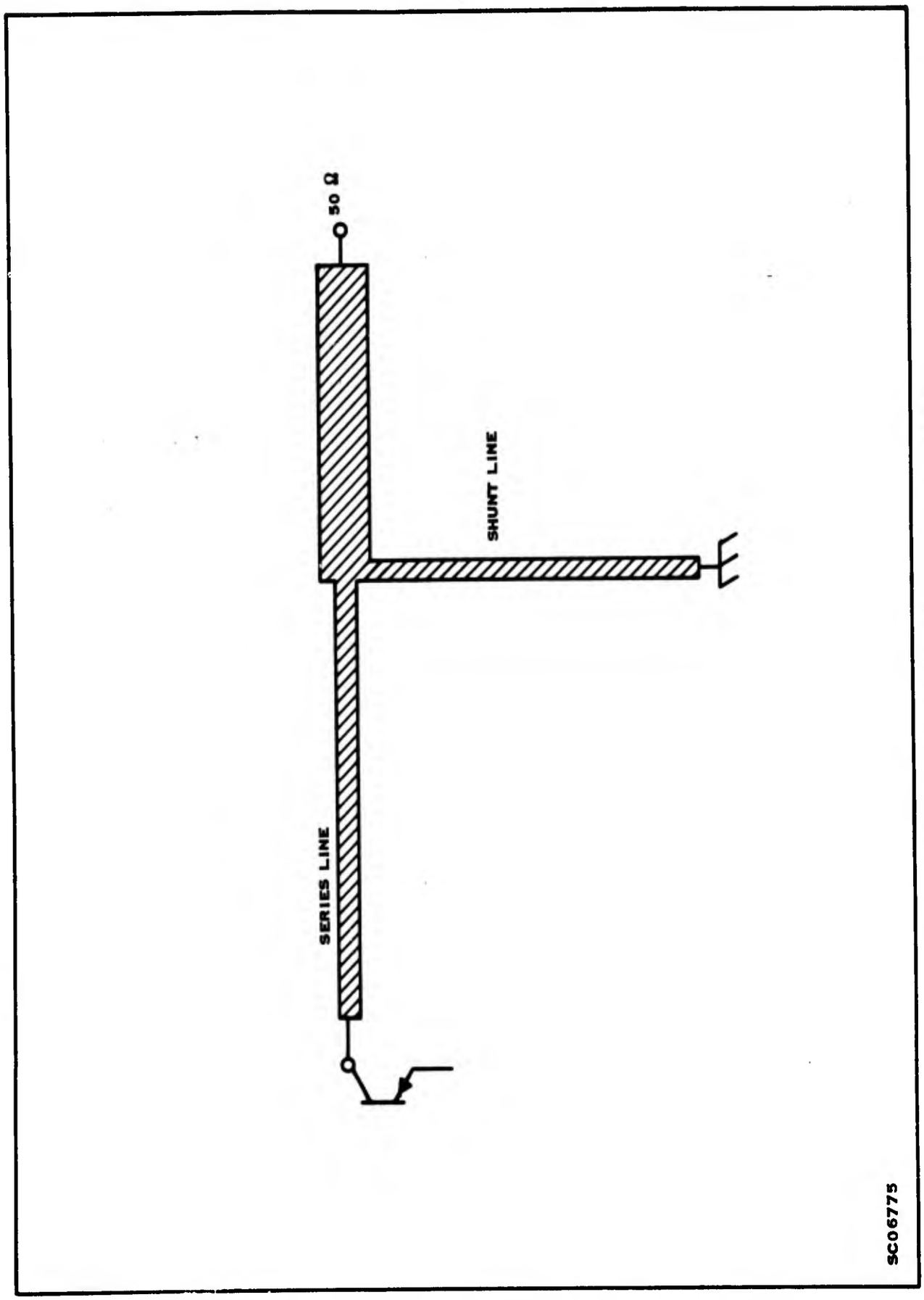

Figure 14. L-section Transformer Used in Output

c. Design Using S-parameters

As accurate device data became available it became apparent that S-parameters, rather than Y-parameters, should be used to design the amplifiers. Measurements were made in S-parameters, and modest errors in these parameters cause large errors in the Y's calculated from these parameters.

The transducer gain can be calculated directly from the S-parameters by using the following equations.[9]

$$G_t = G_{in} \cdot G_{out} \cdot |S_{21}|^2 \tag{1}$$

where

$$G_{in} = \frac{\left(1 - |r_g|^2\right)}{|1 - r_g S_{11}|^2} \tag{2}$$

$$G_{out} = \frac{\left(1 - |r_2|^2\right)}{(1 - r_2 S'_{22})^2} \tag{3}$$

$$r_g = \frac{Z_g - Z_o}{Z_g + Z_o} \tag{4}$$

$$Z_g = \frac{1}{Y_g}$$

$Z_o = \frac{1}{Y_o}$ = reference impedance at which S-parameters are measured

$$Z_L = \frac{1}{Y_L}$$

$$r_a = \frac{Z_L - Z_o}{Z_L + Z_o} \tag{5}$$

$$S'_{22} = \frac{S_{22} - R_g (S_{11} S_{12} - S_{32} S_{12})}{1 - r_g S_{11}} \tag{6}$$

Their interpretation is straightforward. Looking at Equation (1), one can see that the gain is made up of these three terms — the input mismatch loss G_{in}, the output mismatch loss G_{out}, and the square of the magnitude of the voltage gain with a 50-Ω source and load $|S_{21}|^2$.

Providing the terminal conditions to optimize the gain over a large bandwidth involves adjusting the lengths and impedances of the two output lines so that the gain most closely approaches the desired flatness. A computer was used, utilizing a recently developed optimization subroutine,[10] to calculate the dimensions of the best network. The optimization routine minimizes the sum of the squares of the difference between the calculated and the desired gain (6.0 dB), calculated at 25-MHz increments between 1.0 and 2.0 GHz.

d. Final Circuit

The computer predicted that the series line should be 85 Ω and 0.152 λ long at 2.0 GHz. The shunt line should be 85 Ω and 0.12 λ long. The impedance of 85 Ω is almost the maximum impedance available on 20-mil-thick ceramic. This limitation is caused by the line width of ≈ 2.5 mils. When translating electrical wavelength to physical wavelengths it is necessary to realize that the slowing factor (the square root of the effective dielectric constant) changes with line impedance — a characteristic of microstrip. Figure 15 gives the measured slowing factor versus line impedance. For 50-Ω lines it is 2.48; for 85-Ω lines it is 2.42.

Assuming that electrical and physical lengths are equal, the series line should be 0.945 cm long and the shunt line 0.77 cm long. Actually the series line is electrically about 12% shorter than the physical length. This shortening is believed to be due to coupling between the meandered sections. At present it cannot be accurately predicted from available theory; it must be estimated, based on circuit measurements. The shunt line appears to be about 0.1 cm longer than its physical length. This is probably caused by the path to ground over the edge of the ceramic. Physical lengths are therefore 1.07 cm for the series line and 0.67 cm for the shunt line.

The complete layout is shown in Figure 16, with the various elements described.

C. MEASURED RESULTS

1. Physical Description

Figure 17 is a photograph of a gain module approximately five times life size. The back side of the 0.020-inch ceramic was metallized to form a ground plane. The ground on the top plate was connected to the bottom ground plane by silver paint

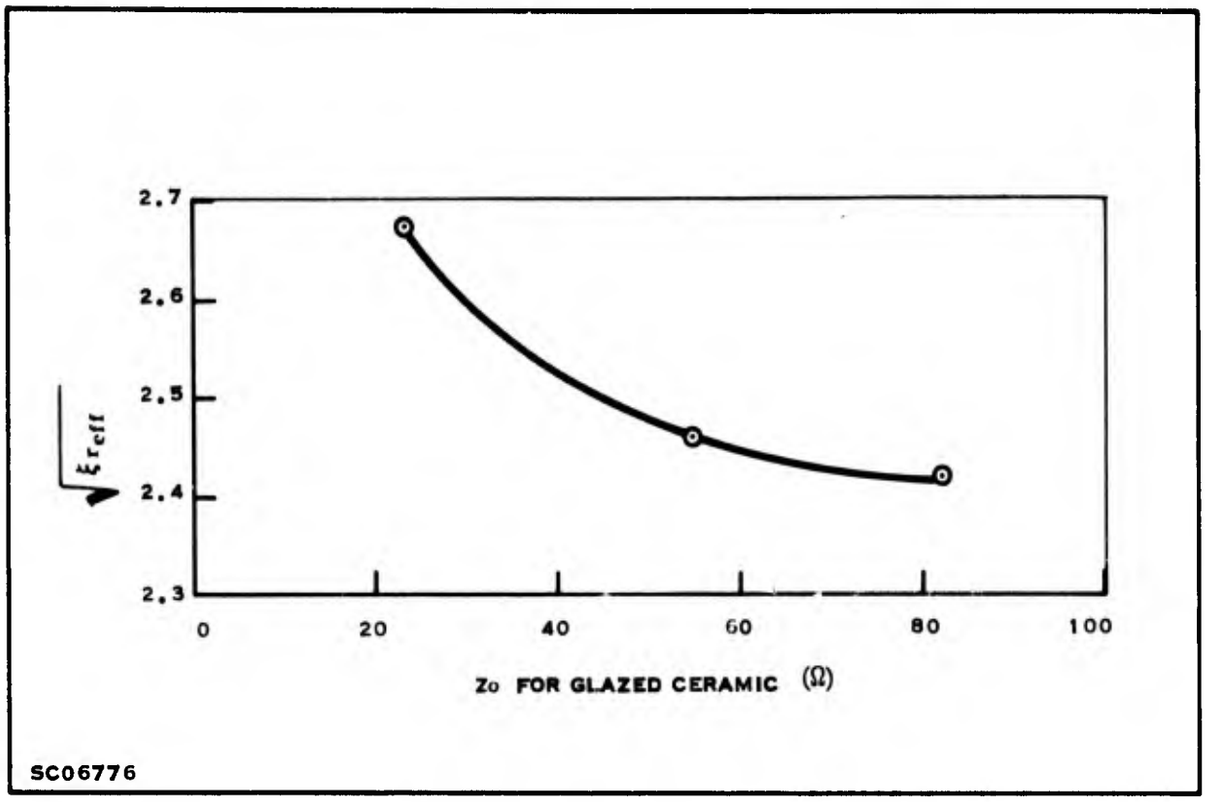

Figure 15. Slowing Factor on Glazed Ceramic Measured at 1.0 GHz

around the edge of the board. This furnished a ground for the emitter and base bypass capacitors. Locating the capacitors near the edge avoids the necessity of providing ground plane through holes in the ceramic substrate. Such holes can be provided quite simply, if necessary, by sand blasting. In production such holes can be provided in the original substrate.

2. Gain

The average gain versus frequency of twenty units is shown in Figure 18. This is somewhat lower than the predicted gain of 6.0 dB. It is felt that this is due to slightly poorer chips than were originally used in the design data. Also, emitter lead impedance to ground may have been larger than anticipated.

3. Mismatch Loss

Figure 19 is a plot of the measured mismatch loss of the amplifier modules; calculated output mismatch loss is also shown. The input mismatch is caused by attempts to show the device $Y_{g(opt)}$. As mentioned earlier, the output mismatch is due to the gain-flattening effects of the output compensating network; one can see that the loss is much higher at the low-frequency end, where the device has more available gain. Both the input and output approach a match at 2 GHz, where virtually all the available transistor gain is needed to meet circuit requirements.

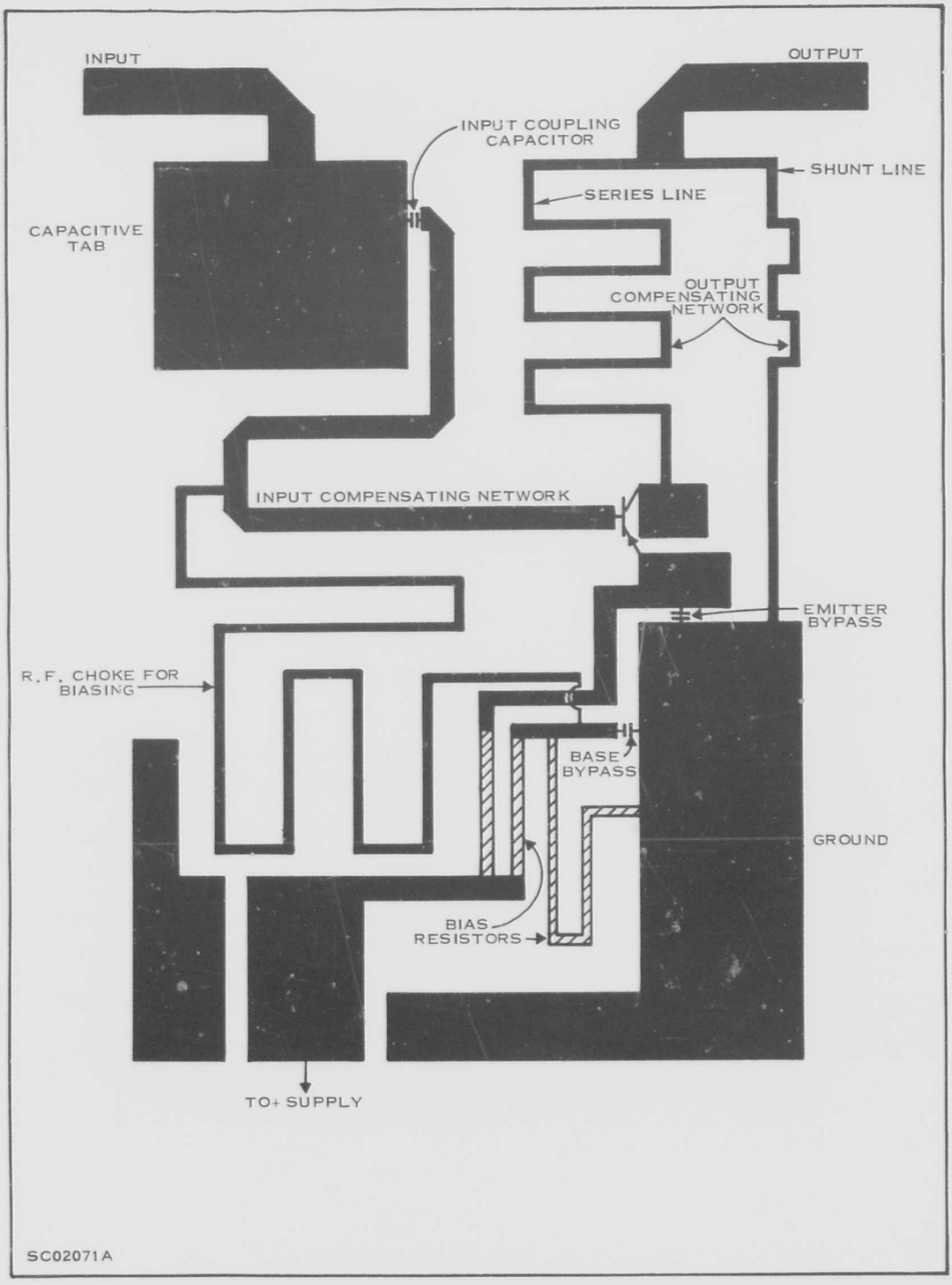

Figure 16. Physical Layout of Ceramic Amplifier

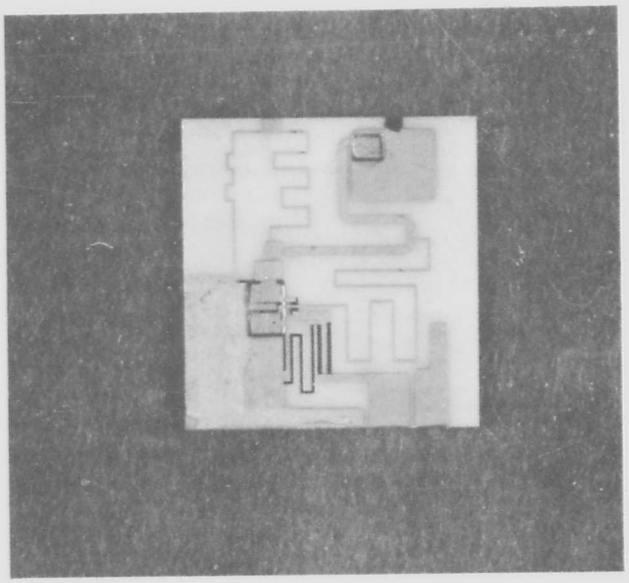

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Figure 17. Gain Module

4. Noise Figure

Figure 20 shows noise figure versus frequency of some gain modules. The noise figure is higher than the design objective. This is probably a result of inadequate selection of transistor chips.

5. Balance

Gain modules were balanced for input and output VSWR. A reflectometer system was used which gave direct readout of return loss versus frequency in the 1-2-GHz band. Output VSWR's were virtually identical in all chips. Input VSWR's varied more, and modules were selected on the basis of input mismatch equality. In most cases the gains were similar if the inputs were closely matched.

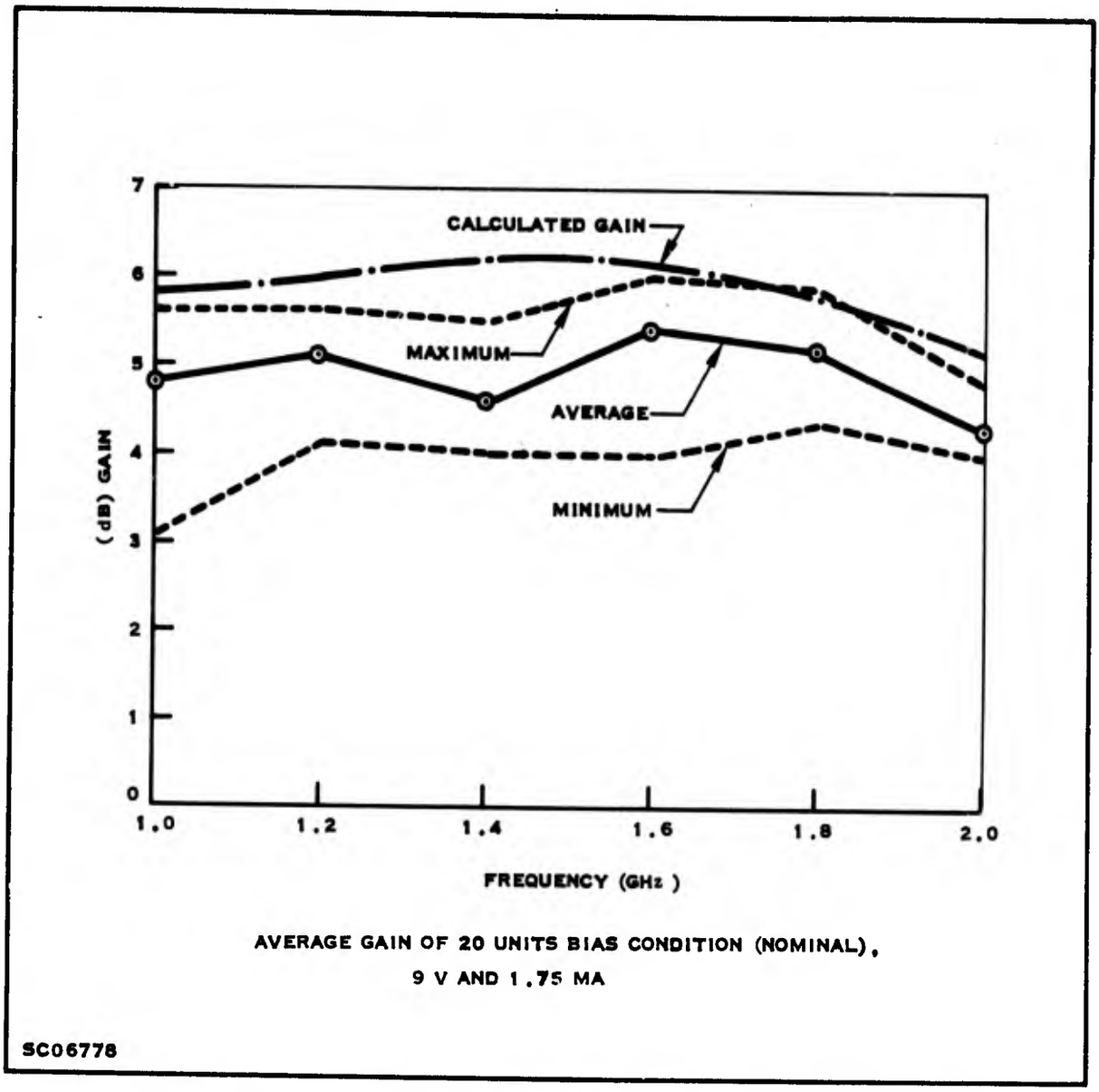

Figure 18. Calculated and Measured Gains of Gain Modules

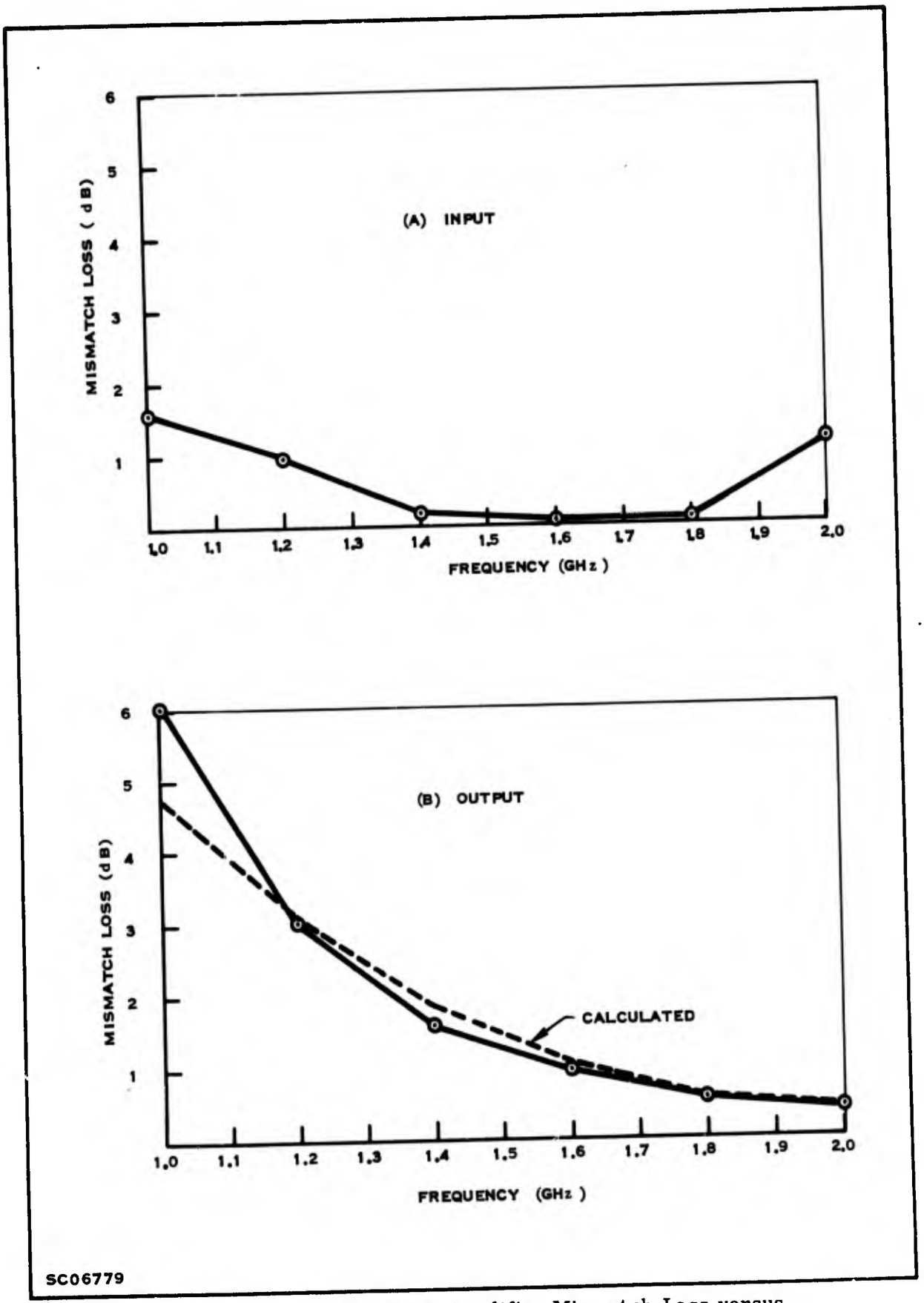

Figure 19. Single-stage Amplifier Mismatch Loss versus Frequency: L-148, 9 V, 1.75 mA

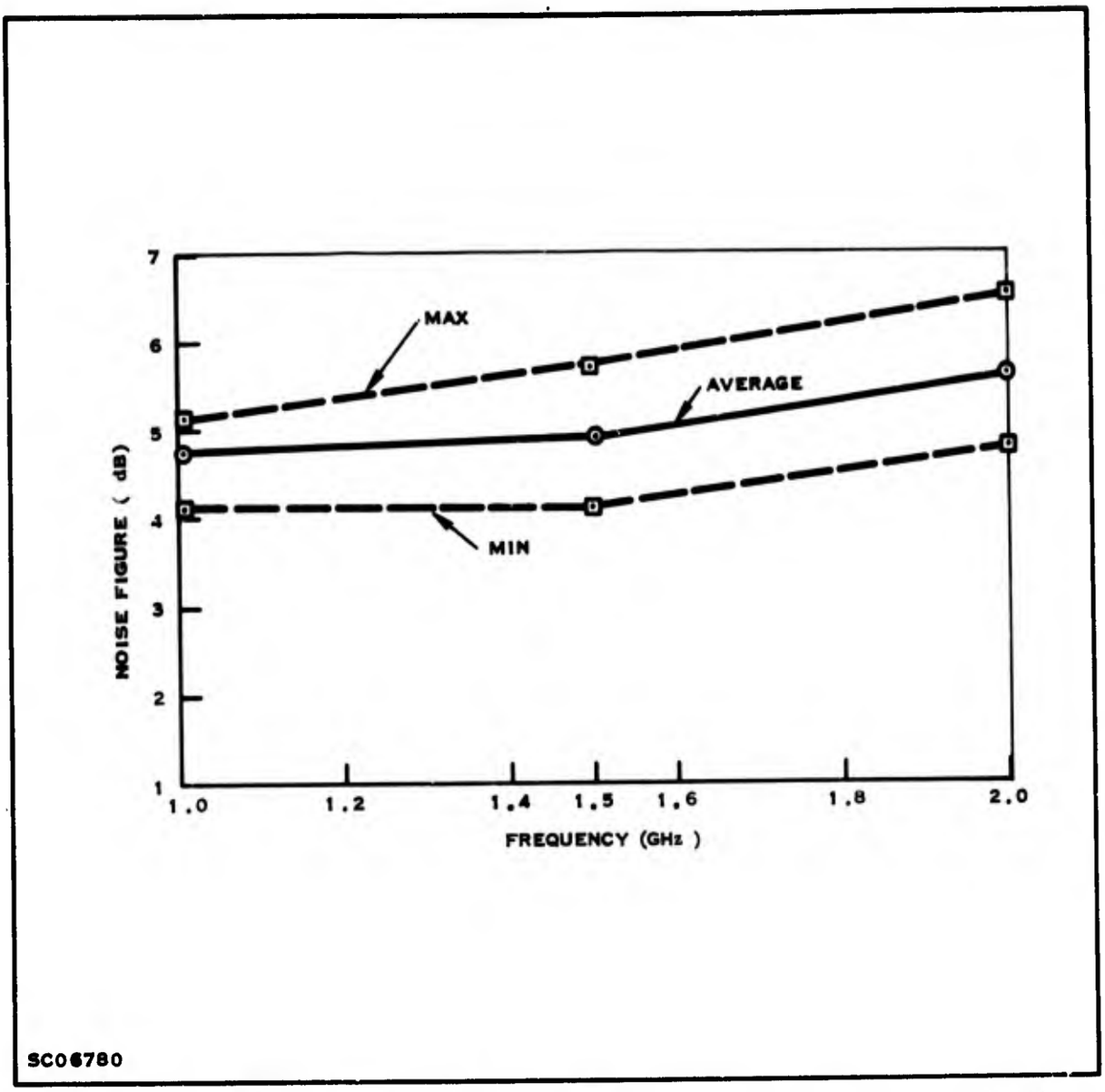

Figure 20. Measured Noise Figure versus Frequency: L-148, 9 V, 1.75 mA

SECTION V

DIRECTIONAL COUPLER

A. COUPLER DESIGN OBJECTIVES

The directional coupler was the second major area of effort in the amplifier design. The amplifier design objectives dictate in large part the coupler design objectives. The coupler should have balanced outputs, good isolation, low loss, and low intrinsic VSWR.

1. Imbalance

The 3-dB coupler is used to divide the power between the two transistors; the coupler reduces terminal VSWR and increases circuit-design flexibility. Ideally one would like a lossless coupler with exactly 3-dB power division across the band. In practice, however, the power will not divide equally. An imbalance will occur because of fabrication tolerance and the coupler's inherent frequency sensitivity. The effect of fabrication tolerances is difficult to evaluate analytically, but basic coupling characteristics have been analyzed to determine the limitations on coupling imbalance. The amplifier had a 1.1:1 terminal VSWR design objective; the calculations below show that the maximum imbalance allowable in a lossless, perfectly terminated 3-dB coupler is 0.44 dB across the band if the VSWR objective is to be met.

The analysis is as follows, with reference to Figure 21.

V_i and V_o represent the signals into and out of the respective ports of the coupler; ρ_2 and ρ_4 are the complex reflection coefficients of the transistors as seen from the coupler; ρ_1 is the reflection coefficient looking into the coupler at port 1. K_2 is the voltage-transfer function between port 1 and port 2; K_4 is the voltage-transfer function between port 1 and port 4. At center frequency $K_2 = K_4 = 0.707$ for a 3-dB coupler. The equations for V_{4_o} and V_{2_o} are:[11]

$$\frac{V_{4_o}}{V_{1_i}} = \frac{\sqrt{1 - C^2}}{\sqrt{1 - C^2 \cos\theta + j \sin\theta}} = K_4(\omega) \angle\varphi \qquad (7)$$

$$\frac{V_{2_o}}{V_{1_i}} = \frac{\sqrt{j\, C \sin\theta}}{\sqrt{1 - C^2 \cos\theta + j \sin\theta}} = K_2(\omega) \angle\varphi + 90^\circ \qquad (8)$$

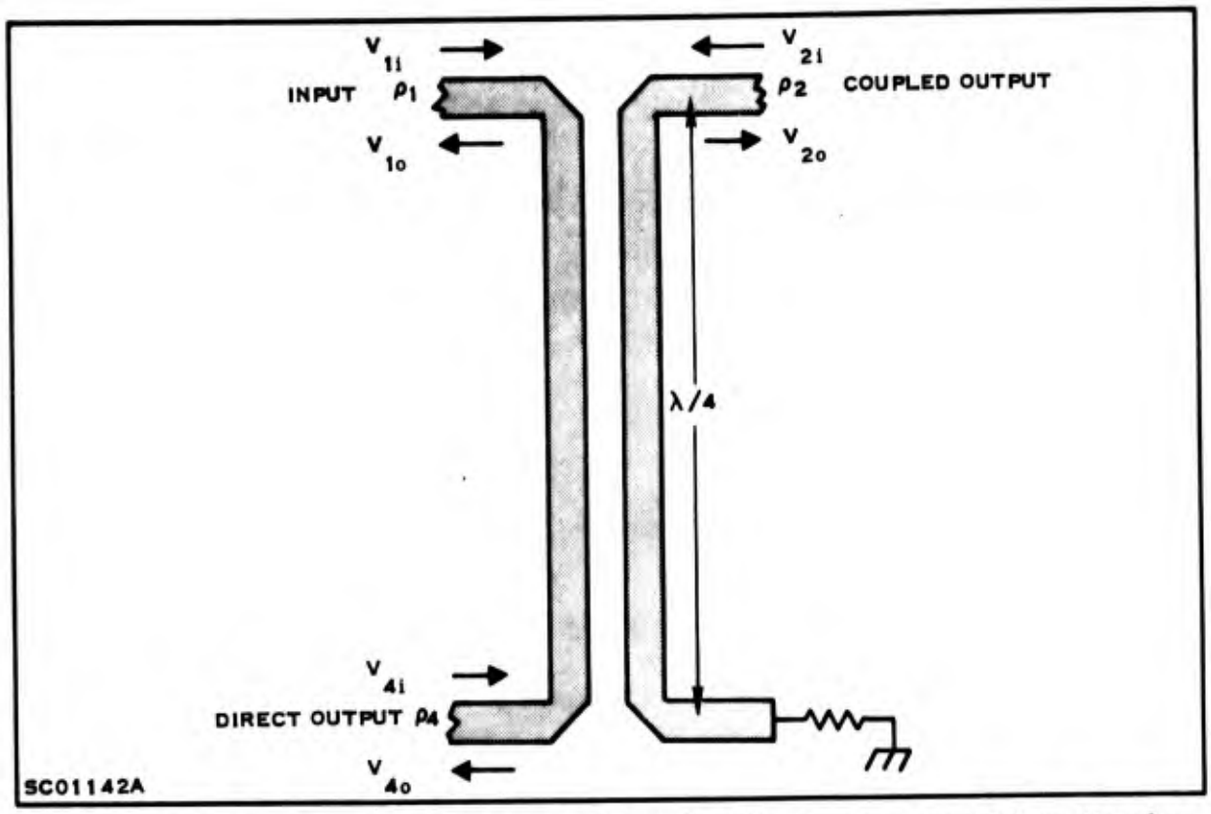

Figure 21. Single-section Directional Coupler Showing Input and Output Signals

C = the center frequency coupling coefficient, a constant for a given configuration;

θ = the electrical length of the coupler in radians ($\theta = 90°$ at center frequency);

ϕ = the phase shift between the input signal and the direct output.

The phase shift is a function of frequency; the 90° difference between V_{4_o} and V_{2_o} is constant, however. It is this fixed 90° difference which causes the reduction of reflections at port 1.

Reflections at port 1, represented by V_{1_o}, will be caused by the signals V_{2_i} and V_{4_i}, the reflected signals from the transistors. The signals incident on the transistors are V_{2_o} and V_{4_o}. Thus,

$$V_{2_o} = V_{1_i} K_2(\omega) \angle \phi + 90° \qquad V_{4_o} = V_{1_i} K_4(\omega) \angle \phi$$

$$V_{2_i} = \rho_2 V_{1_i} K_2(\omega) \angle \phi + 90° \qquad V_{4_i} = \rho_4 V_{1_i} K_2(\omega) \angle \phi \tag{9}$$

These reflections, coupled back to the input, appear as V_{1_o}. The portion of V_{1_o} caused by V_{2_i} is*

$$V_{2_i}K_2(\omega) \angle \phi + 90° = \rho_2 V_{1_i} K_2^2(\omega) \angle 2\phi + 180° \quad (10)$$

The portion of V_{1_o} caused by V_{4_i} is

$$V_{4_i}K_4(\omega) \angle \phi = \rho_4 V_{1_i} K_4^2(\omega) \angle 2\phi \quad (11)$$

The total V_{1_o} is the sum of the two contributions of V_{2_i} and V_{4_i}:

$$V_{1_o} = V_{1_i} \left[\rho_2 K_2^2(\omega) \angle 2\phi + 180° + \rho_4 K_4^2(\omega) \angle 2\phi \right] \quad (12)$$

$$\frac{V_{1_o}}{V_{1_i}} = \rho_1 \quad (13)$$

$$\rho_1 = \rho_2 K_2^2(\omega) \angle 2\phi + 180° + \rho_4 K_4^2(\omega) \angle 2\phi \quad (14)$$

The 180° phase angle in the first term simply indicates a phase reversal; the term can be multiplied by -1 and the 180° dropped. Thus,

$$\rho_1 = \rho_4 K_4^2(\omega) \angle 2\phi - \rho_2 K_2^2(\omega) \angle 2\phi \quad (15)$$

If $\rho_2 = \rho_4 = \rho_T$ (balanced transistors)

$$\rho_1 = \rho_T \angle 2\phi \left[K_4^2(\omega) - K_2^2(\omega) \right] \quad (16)$$

---

* It is obvious from symmetry that $\frac{V_{1_o}}{V_{2_i}} = \frac{V_{2_o}}{V_{1_i}} = K_2(\omega)$.

Thus, the transistor reflection coefficient is reduced by a factor equal to the difference of the squares of the direct and coupled voltage transfer coefficients. It can be shown from Equations 14 and 15 that

$$K_2^2(\omega) + K_4^2(\omega) = 1 \tag{17}$$

Thus,

$$\rho_1 = \rho_T \left[1 - 2K_2^2(\omega)\right] \tag{18}$$

This agrees with results published by Kurokawa.[3/]

Figure 22 is a plot of input VSWR versus output from the coupled port, assuming open or short circuit terminations ($\rho = \pm 1.0$) on the two output ports. The VSWR remains under 1.3 for coupling imbalance of ± 0.5 dB or less. Of course, if the terminations are not open or short circuits, but are still balanced, the VSWR will be lower for a given coupling imbalance.

The worst possible transistor ρ_T is ± 1.0, an open (or short) circuit. Since the amplifier has a design objective input VSWR of 1.1 ($\rho_1 = 0.05$), the limits of coupler ripple or imbalance can be calculated from Equation (19) to be:

$$0.05 = \pm 1 \left[1 - 2K_2^2(\omega)\right] \tag{19}$$

$$K_2^2 = 0.525 \text{ or } 0.475 \tag{20}$$

Then K_2 and K_4 vary from 0.6894 to 0.7246, or 3.23 dB to 2.80 dB. Maximum permissible deviation from 3-dB coupling is ±0.22 dB, or 0.44 dB total imbalance. This assumes perfect directivity, equal losses in both branches, and balanced transistors. The effect of transistor imbalance can be calculated using Equation (20) when K_2 and K_4 are assumed and different numbers are used for ρ_2 and ρ_4.

The 0.44-dB figure also assumes an open circuit ($\rho = 1$) for the transistors. This is certainly pessimistic for the input, but the output approaches this at low frequencies.

Coupler imbalance will also reduce the gain of the amplifier. Figure 23 shows the equations used to calculate the reduction. Figure 24 is a plot of the gain reduction as a function of the deviation from balanced output. This figure shows that the reduction is minimal (≤ 0.15 dB) for deviations of less than ±0.5 dB from balanced outputs.

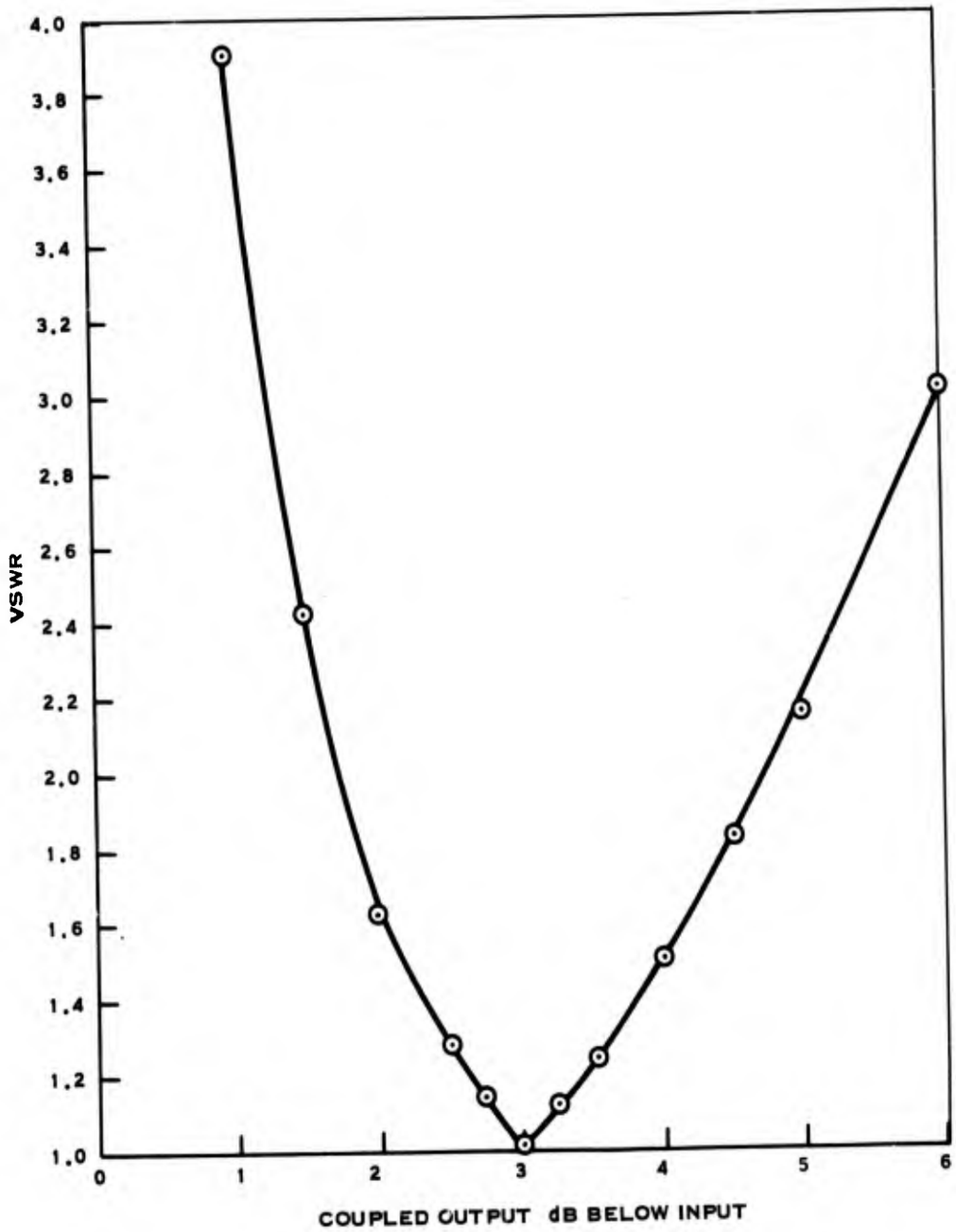

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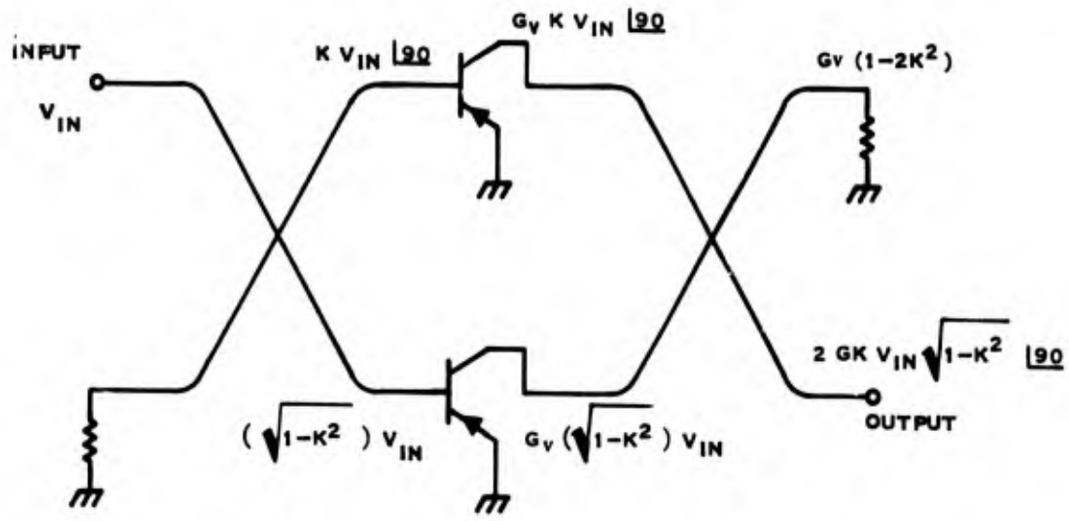
Figure 22. Coupler Input VSWR versus Output from Coupled Port (Assuming Open or Short Circuit Terminations on Coupled and Direct Port)



$$\text{Power Gain} = 20 \text{ Log } (2 G_V k \sqrt{1 - k^2})$$

k = The voltage coupling coefficient of the couplers

G_V = Transistor voltage gain

If $k^2 = 0.5$, Power Gain = 20 Log G_V

If $k^2 \neq 0.5$, the power is reduced by F, where

$$F = 20 \text{ Log } (2k\sqrt{1 - k^2})$$

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Figure 23. Calculation of Reduction of Power Gain Caused by Coupling Imbalance

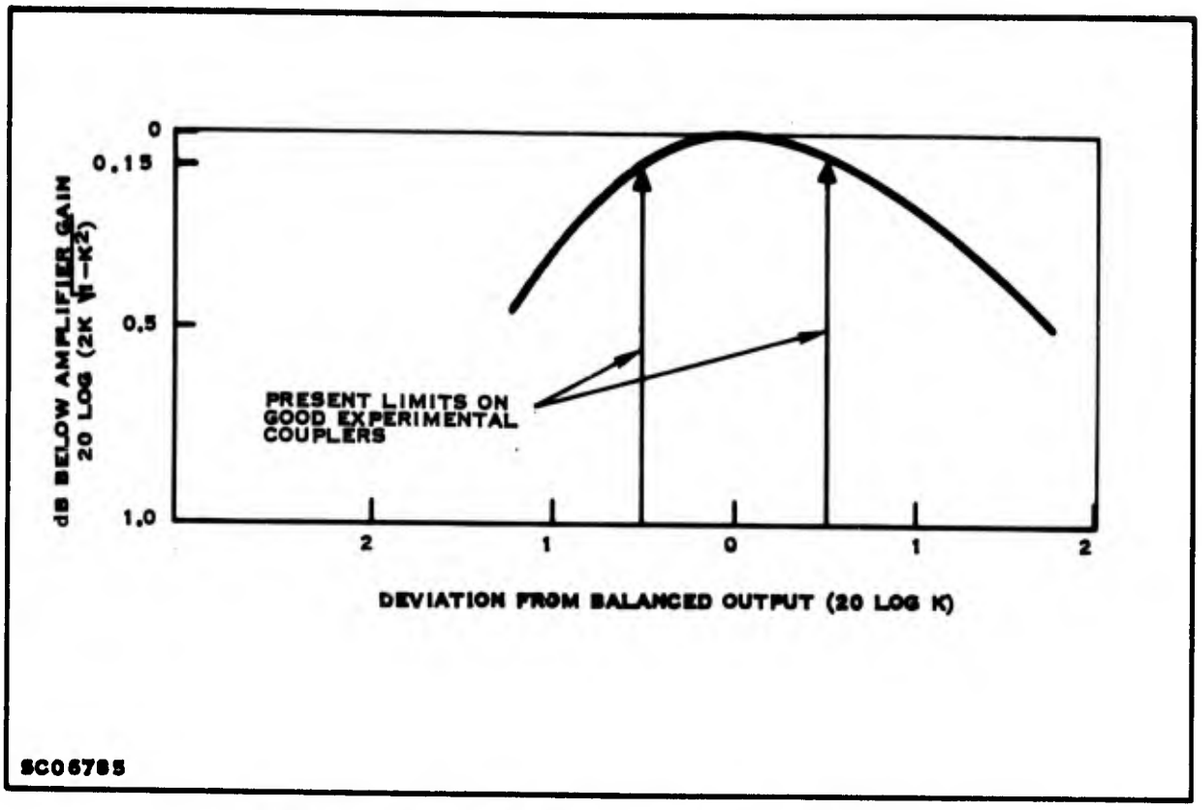


Figure 24. Gain Reduction versus Coupling Balance

2. VSWR of Isolated Port Termination

A poor termination on the coupler can affect the amplifier VSWR. The relation is given by Equation (21), derived in Appendix A.

$$\rho_{out} = \frac{\rho_R}{4} \left(\rho_{T_2} + \rho_{T_4}\right)^2 \angle 180° \tag{21}$$

ρ_{out} = Amplifier reflection coefficient

ρ_R = Reflection coefficient of coupler termination

ρ_{T_2}, ρ_{T_4} = Reflection coefficients of transistors terminating other two coupler ports

B. SELECTION OF CONFIGURATION

The couplers originally considered were branch-line couplers and coupled-line (TEM mode) couplers. Branch-line couplers were dropped from further consideration

because they were not capable of simultaneously meeting the VSWR and bandwidth objectives with a reasonable number of sections.[12]

The designs considered were single- and three-section -3 dB, and single- and three-section tandem 8.34 dB couplers. These will be discussed separately.

1. Single-section -3-dB Coupler

An ideal single-section -3 dB coupler cannot meet the ripple-VSWR requirements of the amplifier. A midband coupling factor of K = 0.525 (2.8-dB coupling at midband) is a good compromise. If this were used, the coupled output would be 3.44 dB down at band edge, and the VSWR would be 1.2. Discontinuities would probably degrade the performance even more.

2. Three-section -3-dB Coupler

A three-section -3 dB coupler, seen in Figure 25, can have the required coupling bandwidth characteristics.[13] The two outer sections have 17.2-db coupling; this can be realized with edge-coupled lines 8 mils wide, spaced 16 mils apart between 20-mil ceramic sheets (total ground plane spacing, 40 mils).[7] The center section required 1.76-dB coupling. The dimensions of such a coupler are difficult to calculate, and it cannot be built with edge coupling.

Broadside coupling is another possibility; in this case the conductors overlap completely for 1.76-dB coupling. Their spacing must be 0.0125 of the total ground plane spacing, and each conductor width must be 0.0324 of this spacing. If 40-mil spacing is used the overlapped lines must be 1.3 mils wide, separated by 0.5 mils. Two severe problems are caused by these dimensions: (1) keeping the 1.3-mil lines overlapped over the complete quarter wavelength (670 mils), and (2) the 0.5-mil ceramic. Because of these two problems it was felt that another approach with a re-entrant center section would be easier.[14]

However, the re-entrant coupler also requires impractical dimensions. For this reason, the 8.34 dB tandem coupler was evaluated. It is discussed in the next section.

3. Tandem 8.34-dB Coupler

The concept of a tandem coupler has been discussed by May;[15] Mosco;[16] and Shelton, Wolfe, and Van Wagoner.[17] This configuration, shown in Figure 26, uses couplers with looser coupling than 3 dB and connects them so that equal power division, with the required phase difference, occurs at the output. An analysis of the tandem coupler is straightforward.

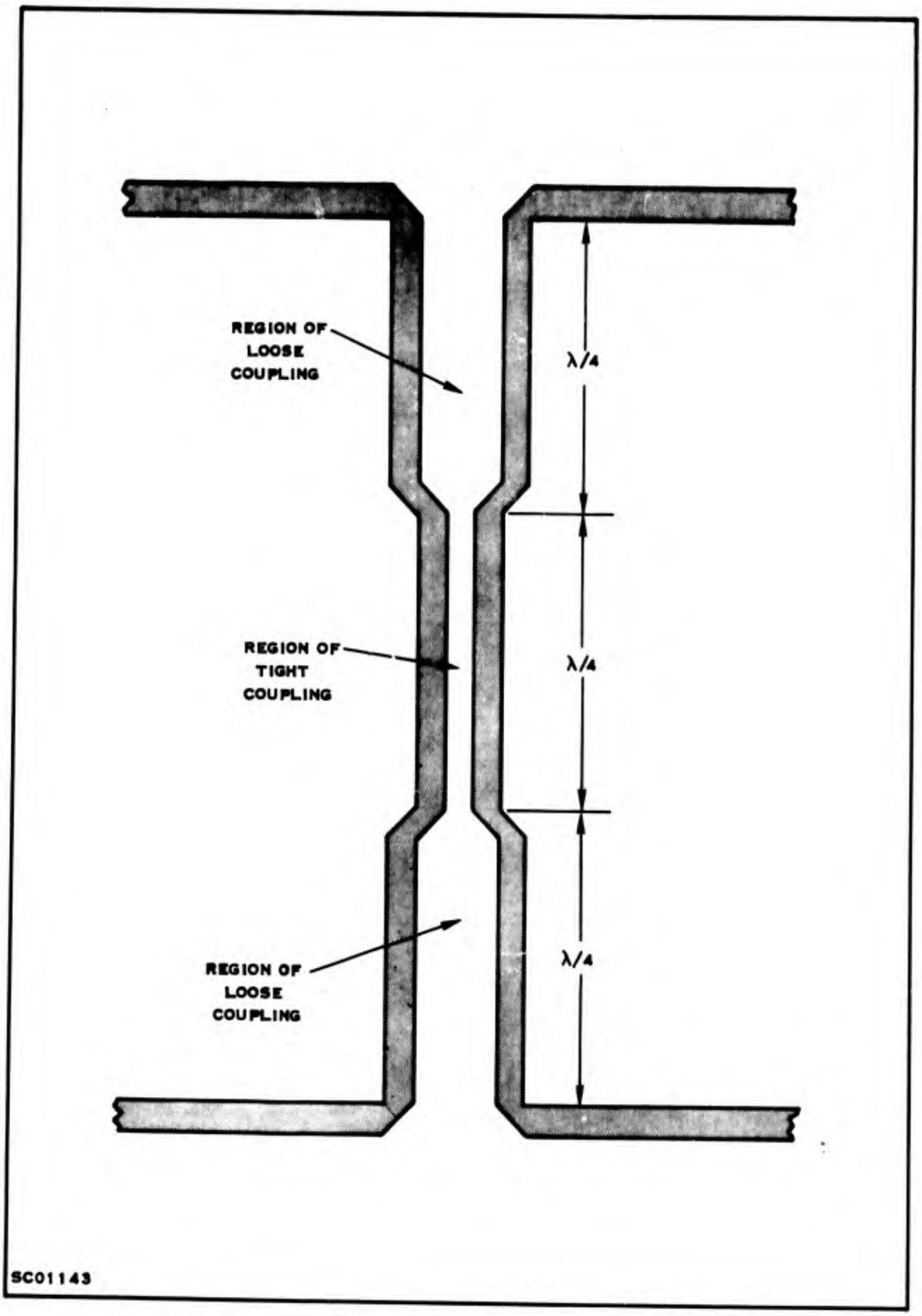


Figure 25. Three-section Cascaded Directional Coupler

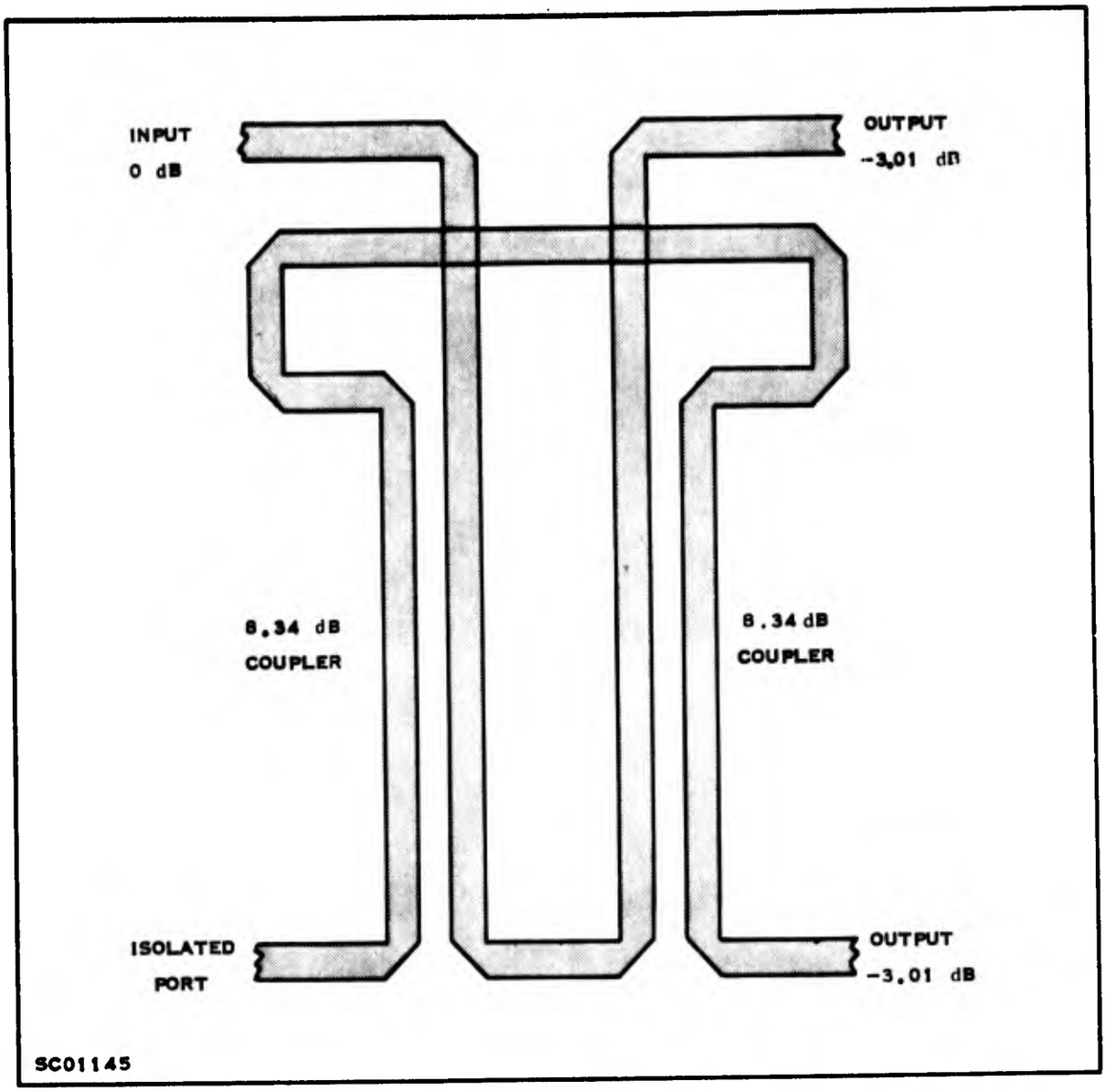


Figure 26. Tandem 8.34-dB Couplers Yielding -3.01-dB Overall Coupling

The output voltages can readily be calculated

$$\frac{V_2}{V_1} = \frac{1 - 2K^2 \sin\theta}{1 - K^2 \cos^2\theta} \tag{22}$$

$$\frac{V_4}{V_1} = \frac{2K\sqrt{1 - K^2}\sin\theta}{1 - K^2 \cos^2\theta} \tag{23}$$

K is the midband coupling coefficient of each section.

At $\theta = 90°$ (midband)

$$\frac{V_2}{V_1} = 1 - 2K^2 \tag{24}$$

$$\frac{V_4}{V_1} = 2K\sqrt{1 - K^2} \tag{25}$$

NOTE:

The 90° phase difference between V_2 and V_4 is maintained as in a single section -3 dB coupler.

Thus, we require the output voltages to be equal.

$$1 - 2K^2 = 2K\sqrt{1 - K^2} \tag{26}$$

$$1 - 4K^2 + 4K^4 = 4K^2(1 - K^2) = 4K^2 - 4K^4 \tag{27}$$

$$8K^4 - 8K^2 + 1 = 0 \tag{28}$$

There are two positive values of K that will satisfy this equation: K = 0.384 (8.34 dB coupling) and K = 0.935 (0.7 dB coupling). The tighter coupling is, of course, impractical. The 8.34 dB is realizable with edge coupling.

Putting single section couplers in tandem reduces the bandwidth by a factor of approximately 15%. This eliminates the single section tandem 8.34 dB coupler from consideration since its bandwidth is less than that of a single 3.0 dB coupler. However, according to Cristal and Young,[5] a three section 8.34 dB coupler can have the desired bandwidth and be compatible with thin film circuit technology.

The 8.34 dB equal ripple coupler needs a fractional bandwidth of

$$w = \frac{1.2}{}\left[\frac{f_2 - f_1}{f_o}\right] = \frac{1.2}{1.5} = 0.8 \tag{29}$$

f_1 and f_2 are the lower and upper frequencies of the equal ripple band edge; f_o is the arithmetic mean of f_1 and f_2. The factor 1.2 is an estimate of the excess bandwidth needed in each coupler so that the overall bandwidth is met. Thus, a bandwidth ratio of

$$B = \frac{f_2}{f_1} (1.2) = 2.4 \tag{30}$$

is necessary.

Referring to the tables by Crystal and Young,[5] it can be seen that an 8.34 dB three section coupler with 0.1 dB deviation from mean coupling has a w = 0.89 and B = 2.61. This will fill the requirements of the amplifier. The loosely coupled sections are to have 23.2 dB coupling and the tightly coupled section is to have 6.2 dB coupling. From the tables the even and odd mode impedances can be calculated for both types of sections.

For the loosely coupled sections,

$$Z_{oe} = 50 \times 1.074 = 53.8\ \Omega$$

$$Z_{oo} = 50 \times 1/1.074 = 46.6\ \Omega$$

The tightly coupled sections have

$$Z_{oe} = 50 \times 1.719 = 86\ \Omega$$

$$Z_{oo} = 50/1.719 = 29\ 1\ \Omega$$

Cohn's equations[18] were used to find the proper dimensions on 40-mil-thick ceramic (80 mils total ground plane spacing) to give these impedances. The loosely coupled lines are 18.0 mils wide and 44.3 mils apart. The tightly coupled lines are 11.2 mils wide and 3.2 mils apart. Dielectric constant was assumed to be 8.4 to take into account the silicon-oxide glaze (estimated to be 2 mils thick with $\epsilon_r = 4$). Figure 27 is a dimensioned drawing of the coupler. The junction between the regions of loose and tight coupling was designed to have 50 Ω ± 0.05 Ω characteristic impedance. Wires were soldered for crossovers.

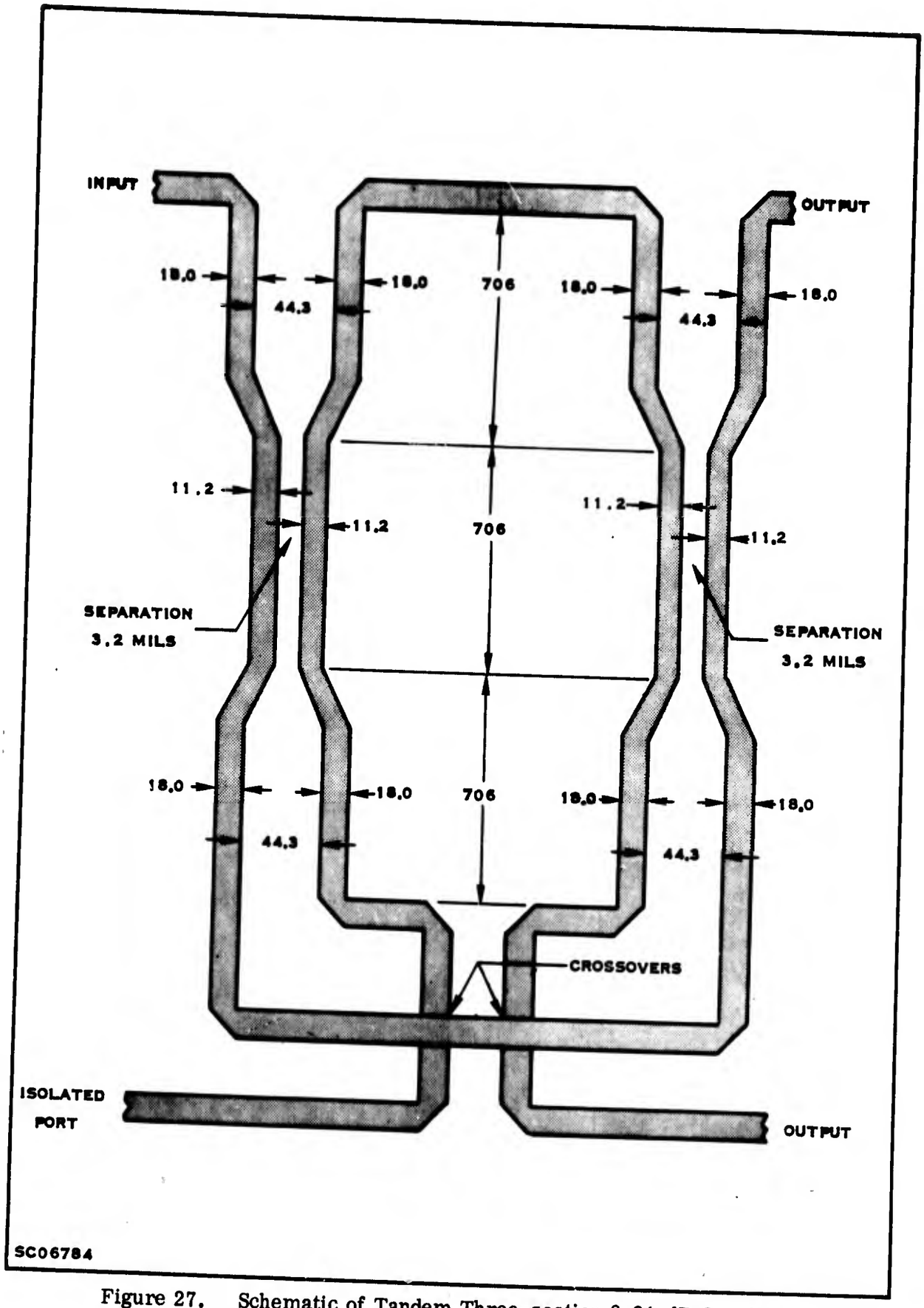


Figure 27. Schematic of Tandem Three-section 8.34-dB Couplers Showing Important Dimensions (in mils)

C. DESIGN PROBLEMS

Two problems which were inherent in this configuration were investigated: the effect of the crossovers, and the effect of a change of line dimensions caused by fabrication tolerances.

1. Crossovers

Crossovers were evaluated by computer analysis of a simplified equivalent circuit. The crossovers in the circuit were represented by assuming shunt stray capacity between the lines (see Figure 28). The scattering matrix was converted to an admittance matrix, the capacitor susceptance added, and the composite admittance matrix reconverted to scattering parameters. Figure 29 is a plot of the calculated response of a coupler (single-section tandem 8.34 dB) for various interline capacities. One can see that there is little change from 0 pF until the coupling capacity was higher than 0.25 pF. For $C \geq 0.5$ pF the response shifts considerably.

The capacity present in the physical circuit can be estimated fairly simply; if a 10,000Å layer of silicon oxide ($\epsilon_r = 4$) is the dielectric, and the capacitor area is 25 mils^2, the capacity is 0.57 pF. If mylar film is used with 1-mil thickness the capacity is 0.023 pF. The couplers actually used 3-mil-diameter gold wires for the crossover with 1-mil or greater air spacing. The capacity introduced by these is negligible.

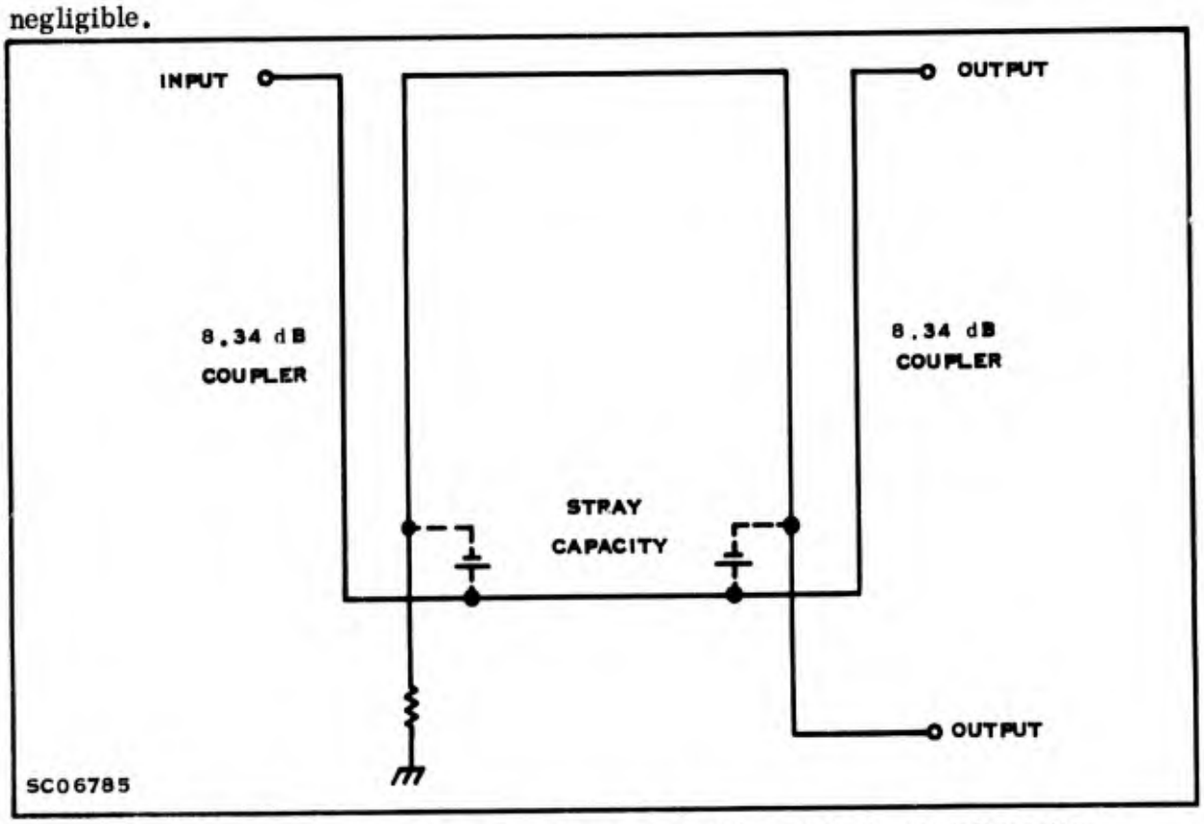


Figure 28. Coupler Diagram Showing Position of Estimated Capacity

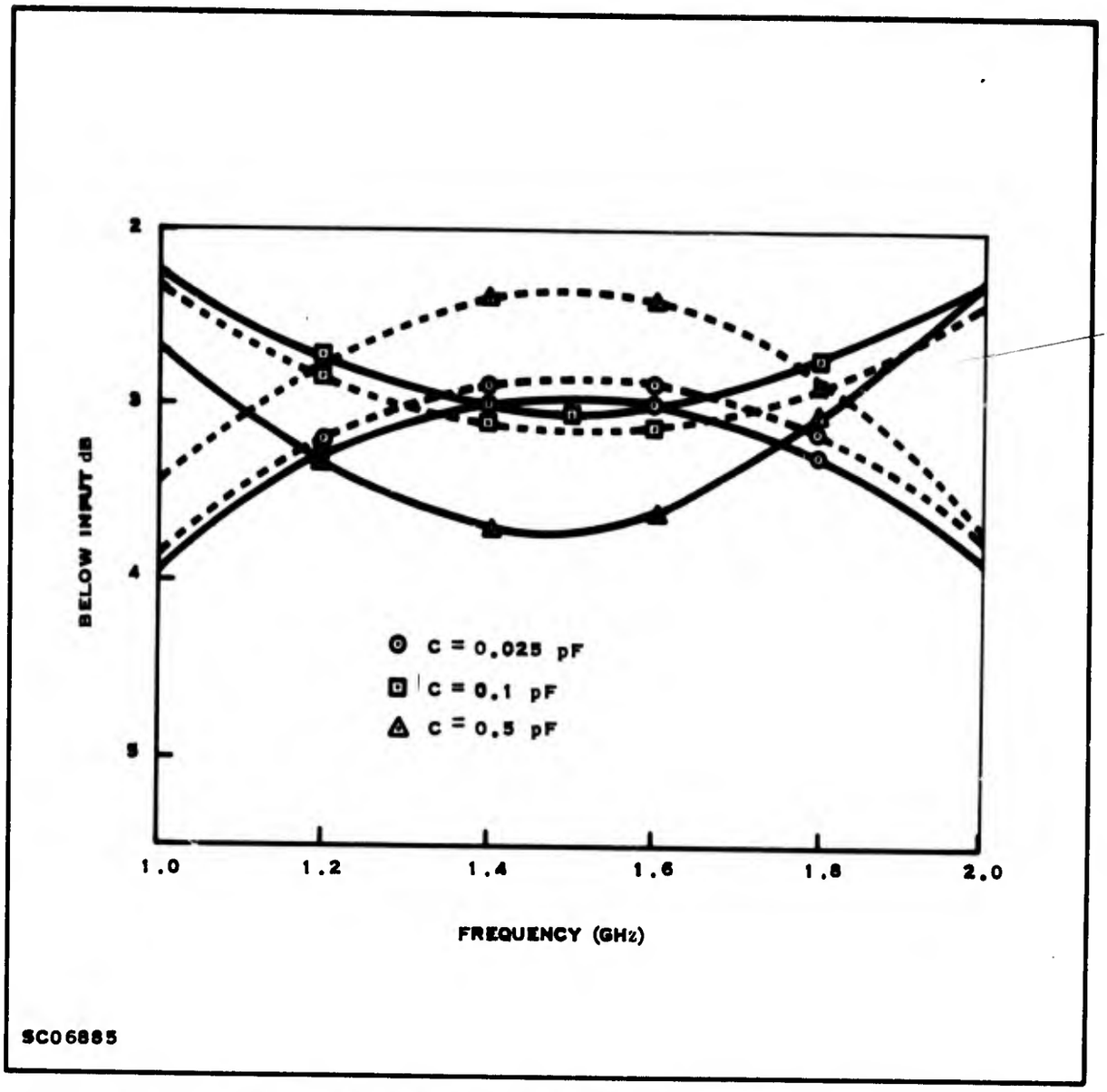


Figure 29. Change of Response of Single-section Tandem 8.34-dB Coupler Caused by Stray Interline Capacity at Crossover

2. Line-spacing Variation

The effect of line-spacing variation is most noticeable in the center section. Effect on the coupling caused by a variation in center spacing is shown in Figure 30. The coupling for the design center and for spacing ±0.25 and ±0.50 mils wider and narrower is shown. These data, calculated by computer, neglect any loss caused by impedance mismatch. We concluded from these calculations that the observed tolerance of ±0.2 mil (approximately) would be satisfactory. In practice it is possible to shape the response somewhat by a judicious application of dielectric filler, which is discussed later.

D. EXPERIMENTAL RESULTS

1. Physical Description

Tandem couplers were fabricated on 0.040-inch glazed ceramic. The terminating resistors were anodized tantalum, manually trimmed to 50 Ω ±10%. The cover plate was also 0.040-inch glazed ceramic with holes cavitroned for the crossover. Figure 31 is a photograph of the coupler without the cover plate.

2. Coupling Response

Figure 32 gives the outputs of the coupled and direct ports, with typically ±0.5 dB ripple and 1.0 dB imbalance. Figure 33 shows the measured VSWR of coupler input with 50-Ω terminations on all other parts. Although isolation could not be measured because the termination resistor was integral with the couplers, prototype couplers, made earlier, typically had 15 dB of isolation across the band; coupler loss was approximately 0.5 dB across the band.

3. Dielectric Filler

It was necessary to use a dielectric paste between the two plates to eliminate air pockets which cause discontinuities. The paste had a dielectric constant of approximately 9. It was composed of 25% titanium oxide and 75% Sylgard.® Even with this additional filler it is felt that unavoidable air gaps were a major contribution to the peaks in the coupler VSWR. Future designs which eliminate this would be desirable; further work is being done on couplers which can be used without need for a dielectric paste filler.

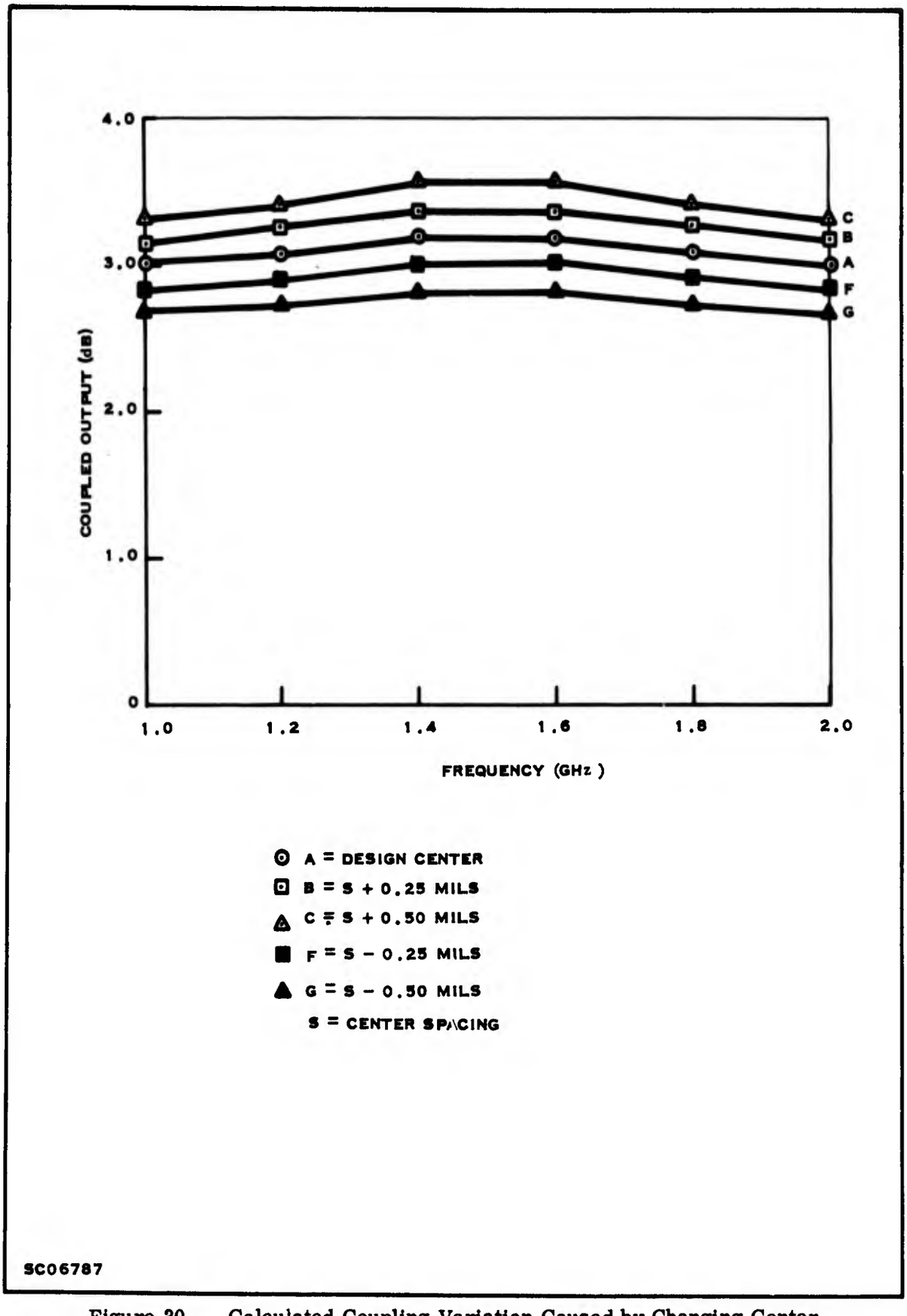


Figure 30. Calculated Coupling Variation Caused by Changing Center Spacing of Three-section Tandem 3-dB Coupler

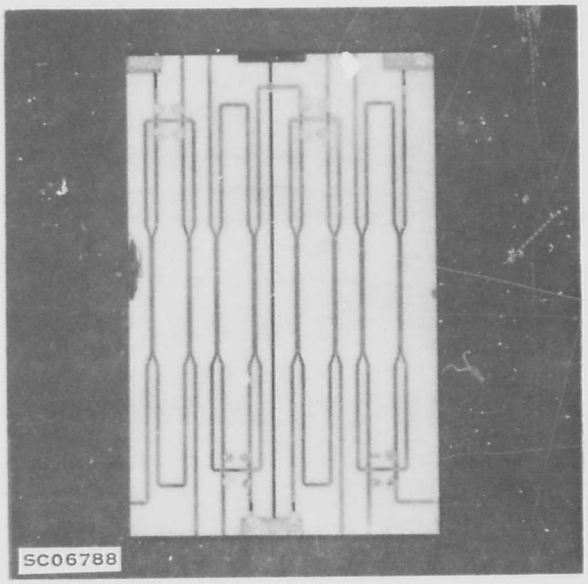


Figure 31. Ceramic Directional Coupler

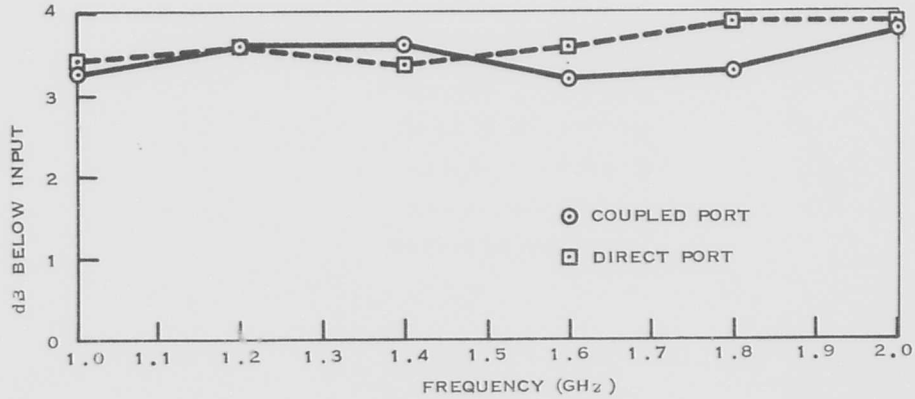


Figure 32. 3-dB Ceramic Directional Coupler Coupling versus Frequency

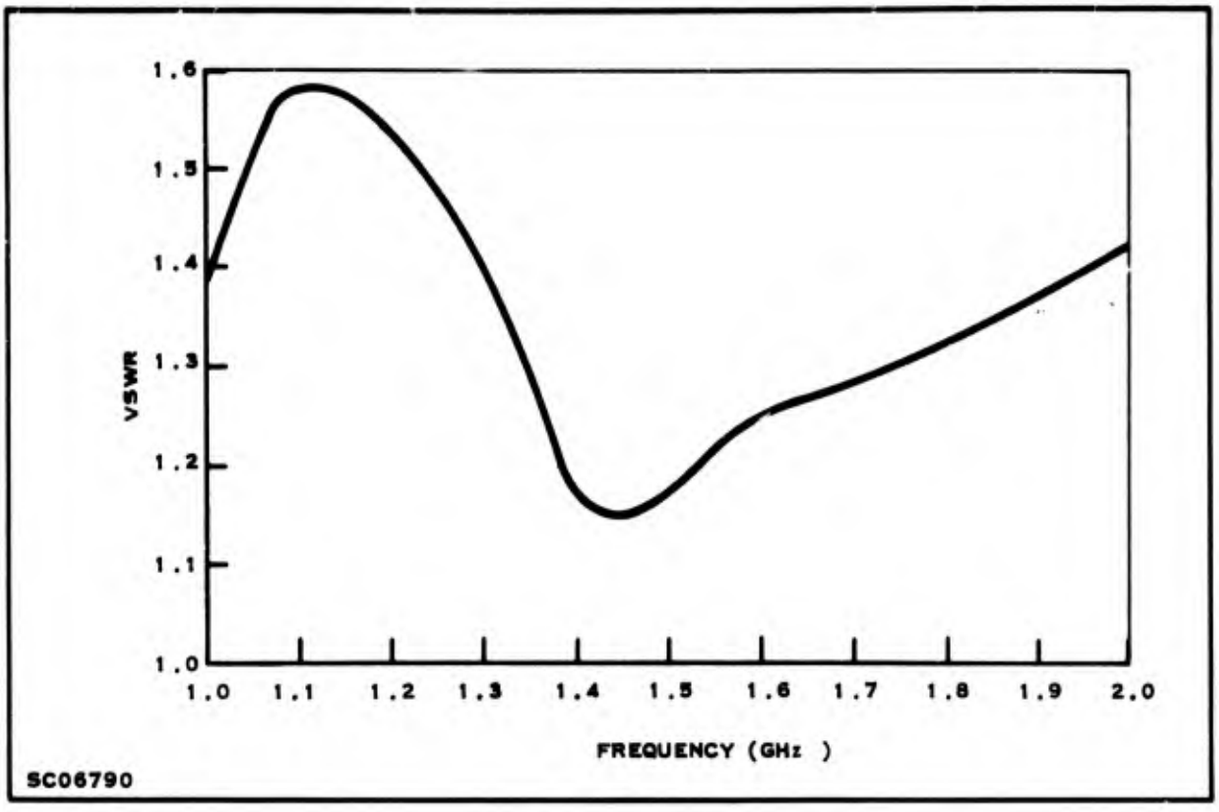


Figure 33. Input VSWR of Ceramic Directional Coupler versus Frequency

SECTION VI

AMPLIFIER PERFORMANCE

A. PHYSICAL DESCRIPTION

Selected gain modules and couplers were assembled to form one four-stage and one six-stage balanced amplifier. Figure 34 is the photograph of the complete six-stage amplifier; couplers have brass top plates in place; gain modules are shown on either side of the couplers. Couplers and modules are interconnected with short strips of gold soldered to each terminal; OSM connectors are used to make contact to the input and output terminals of the amplifier.

There were 17 solder connections to be made in the four-stage amplifier; 25 in the six-stage. Good solder contacts on the prototypes were difficult to maintain because of the small areas. It is desirable that the number of solder connections be as few as possible, to reduce fabrication time and improve reliability. The entire amplifier is mounted on a brass support board and packaged in a gold-plated brass box.

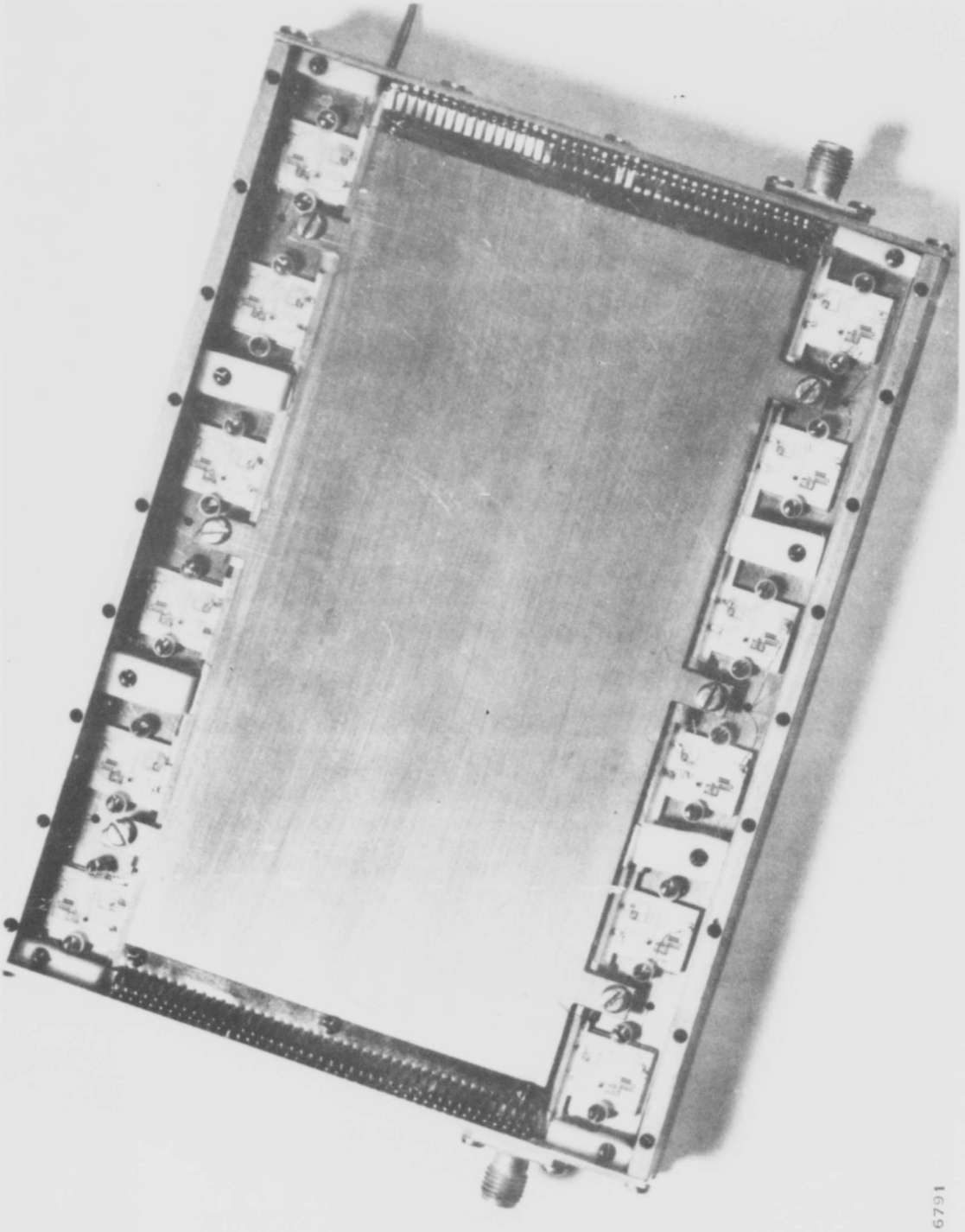
B. ELECTRICAL PERFORMANCE

Figures 35 through 41 show the amplifier's electrical performance. Figures 35 and 36 give the gain versus frequency for the four- and six-stage models. Figure 37 shows the noise figure versus frequency. Figures 38 and 39 give amplifier terminal VSWR versus frequency. Figure 40 presents the phase shift, and Figure 41 the gain versus input power of the amplifiers.

1. Gain

Figure 35 shows the gain measured and calculated for the six-stage amplifier. Gain was calculated by adding the gain of the individual modules, and assuming 0.5 dB loss for each coupler. The measured gain is below the calculated gain by about 8 dB, as calculated; the bandshape is basically the same.

The gain (calculated and measured) for the four-stage amplifier is shown in Figure 36. Again the shape of the two curves is similar, but there is still some serious discrepancy between the calculated and measured gain. Part of the difference is caused by compression. It is also possible that some of the discrepancy may be



SC06791

Figure 34. Complete Six-stage Amplifier

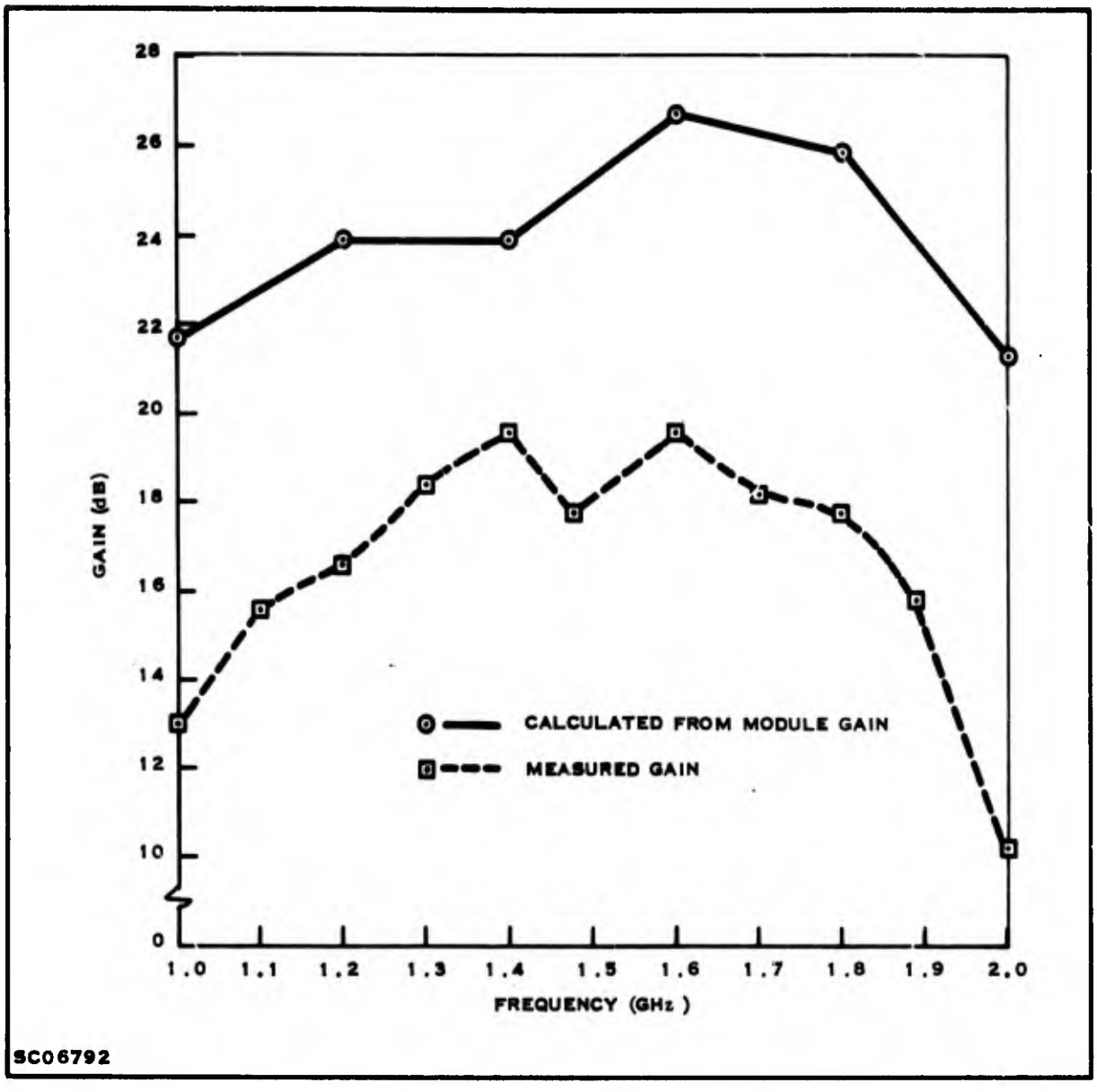


Figure 35. Six-stage Amplifier Gain

caused by the coupler's VSWR. The gain modules are measured with a 50-Ω load and source; however, the coupler VSWR can be as high as 1.5:1. Effect of the VSWR is to change the load seen at the module terminals, with undoubtedly a harmful influence upon the gain.

2. Noise Figure

The amplifier noise figure, shown in Figure 37, is typically 7 dB, going to 10 dB maximum for the four-stage amplifier and 10.8 dB maximum for the six-stage at 2.0 GHz. Design objective was 6 dB across the band, this requiring that the gain modules have 4.9-dB noise figure (including coupler loss). The modules, however,

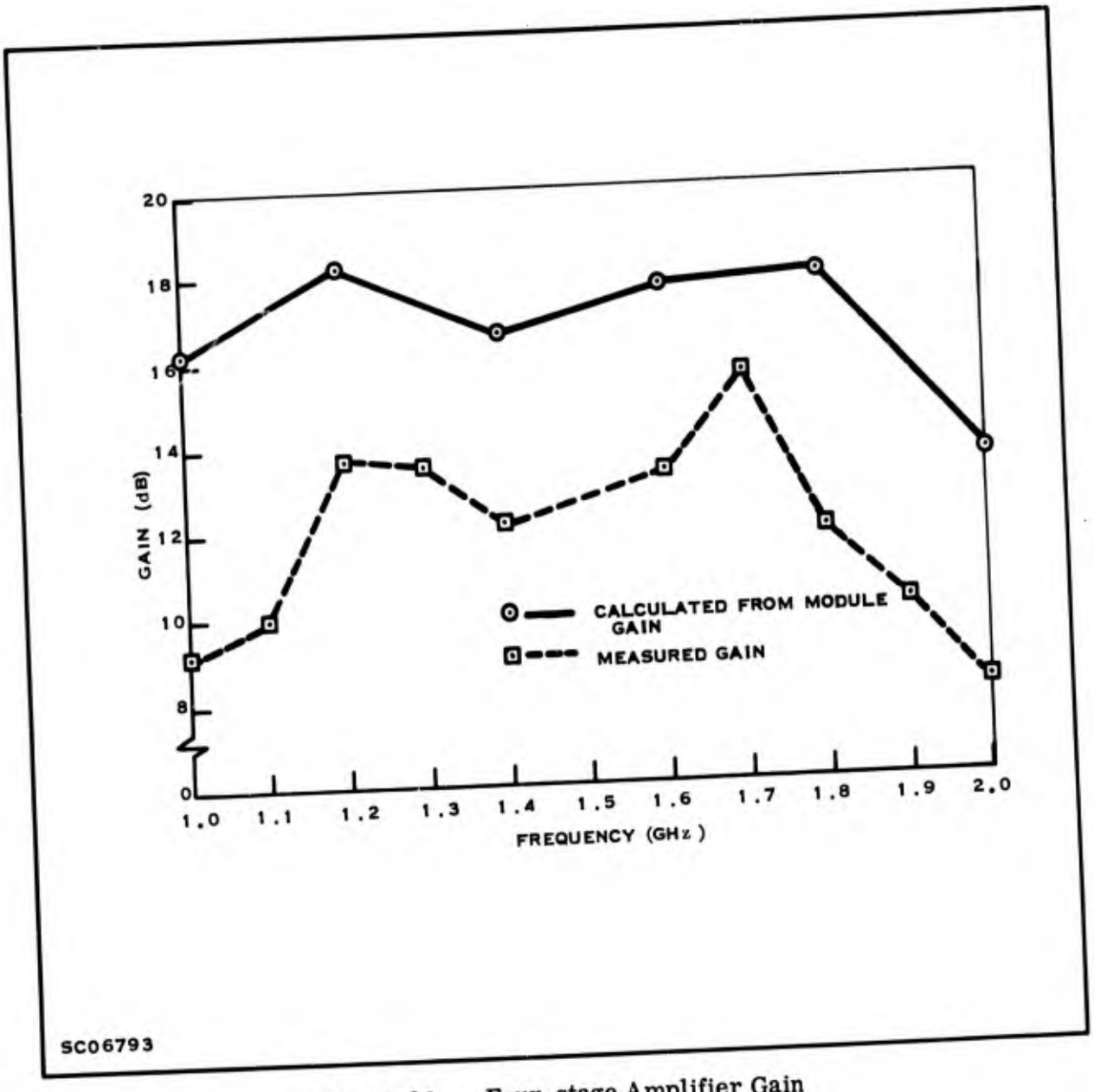


Figure 36. Four-stage Amplifier Gain

measured 4.1- to 6.5-dB noise figure (excluding coupler loss), the average being 4.7 at 1 GHz and 5.6 at 2 GHz.

If one assumes 4-dB gain/stage and 5.4-dB noise figure, including 0.5-dB coupler loss, the calculated amplifier noise figure is 7.0 dB. This agrees with the measurement over most of the band. At 2.0 GHz the lower amplifier gain and higher coupler loss cause even higher noise figure. Tuning the input of the gain modules with stub tuners did not improve the noise figure—suggesting that the transistors were seeing $Yg_{(opt)}$. Also the mismatch loss at 2.0 GHz measured on the gain modules was 1.1 dB, agreeing quite well with the loss occurring when similar transistors in

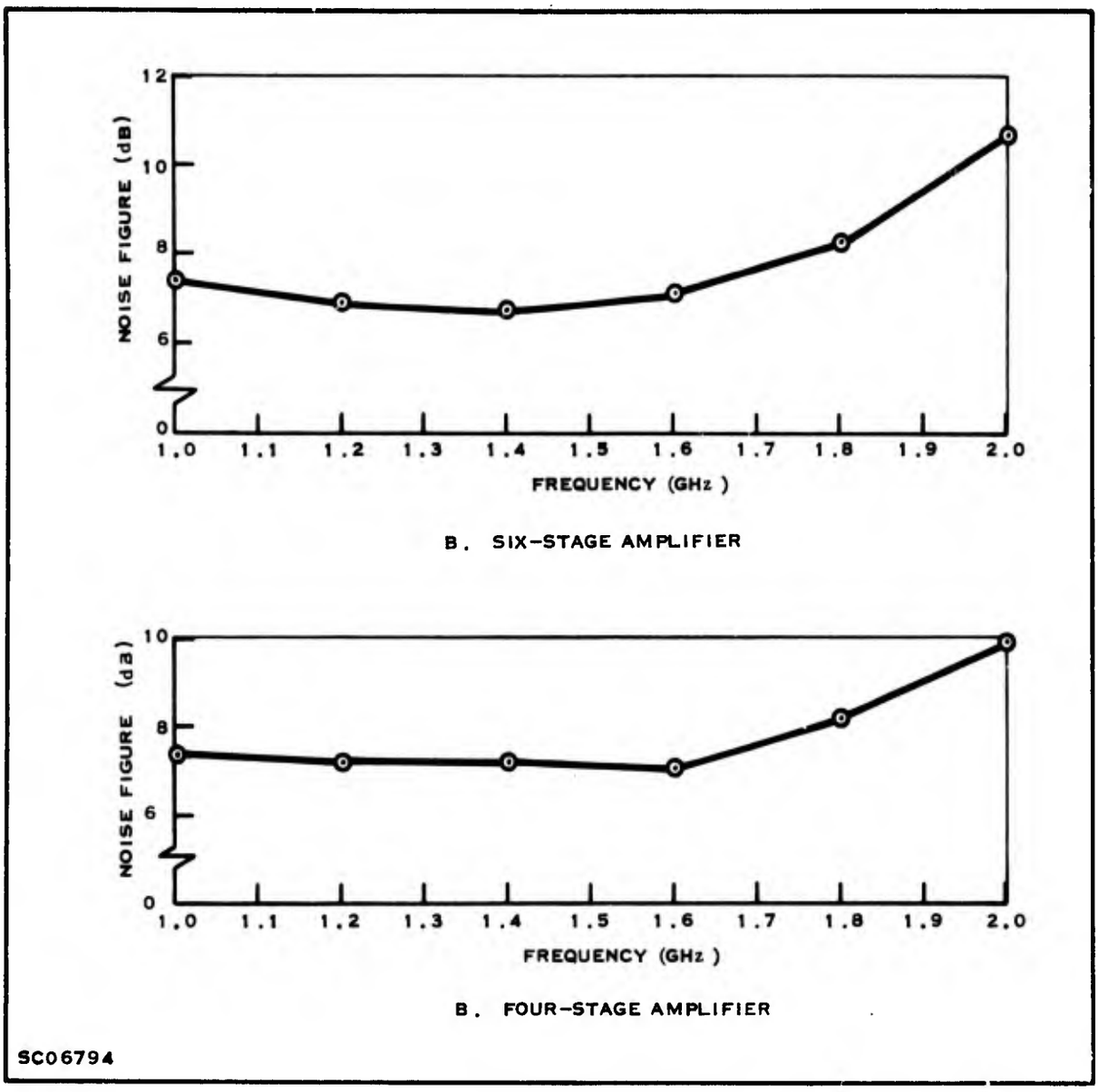


Figure 37. Six-stage and Four-stage Amplifier: Noise Figure versus Frequency

the TI-Line package show $Yg_{(opt)}$. At the time of amplifier construction it was impossible completely to characterize the actual chips used, and it is conceivable that they may have had higher noise figures than those characterized in the TI-Line package.

3. VSWR

Figures 38 and 39 show the amplifier input and output VSWR versus frequency. The VSWR of the modules alone is included. Reduction in VSWR caused by the couplers is strikingly apparent at the output. The reduction at the input is most

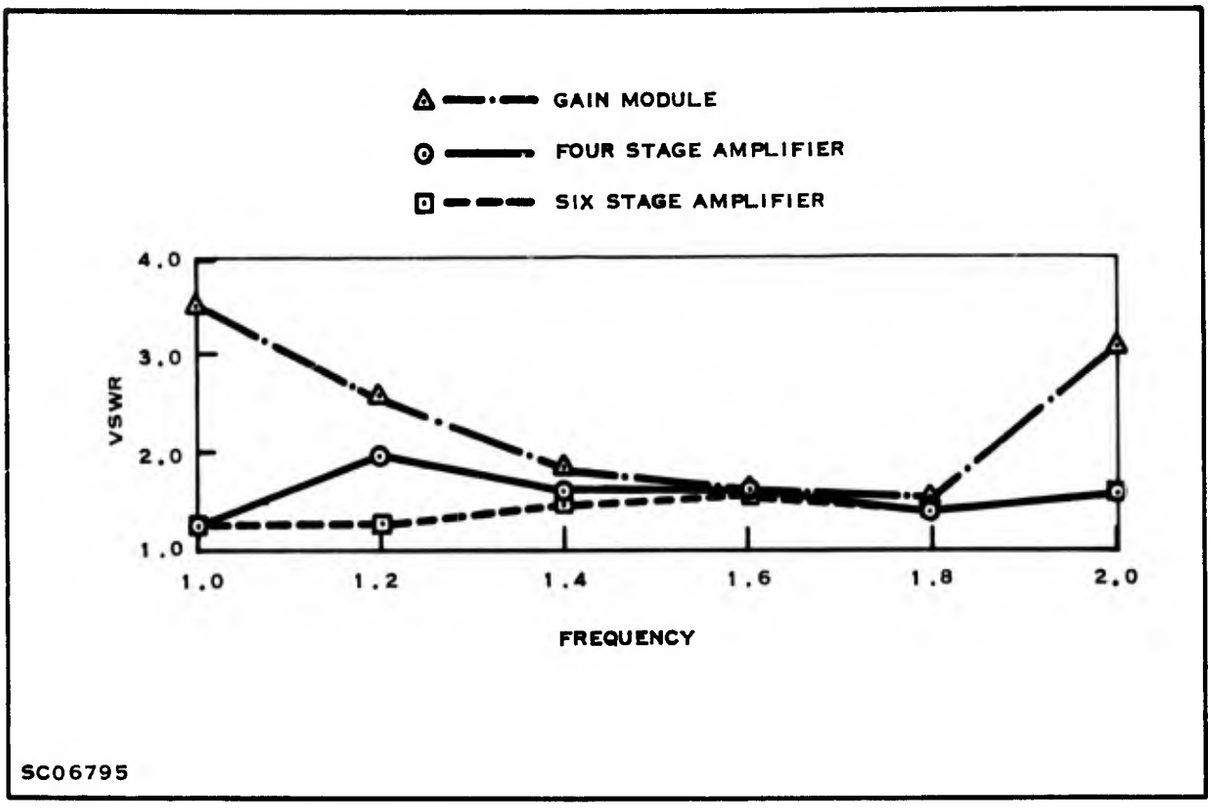


Figure 38. Input VSWR of Gain Module and Balanced Amplifier

evident at the band edges as the gain module was already quite well matched at band center. This reduction of VSWR and terminal reflections is one of the fundamental advantages of the directional-coupler approach. This approach permits the design in modular form and then allows cascading of the stages with little interaction. Also, as we mentioned before, it permits simultaneous noise figure and VSWR optimization, although, unfortunately, this was not observed here because of design and fabrication problems.

4. Phase Shift

Figure 40 shows phase shift variation versus frequency. Large variations can be noted, due mainly to gain variation across the band. In later amplifier models, when improved gain modules and couplers are used, the phase shift should be within the design objectives.

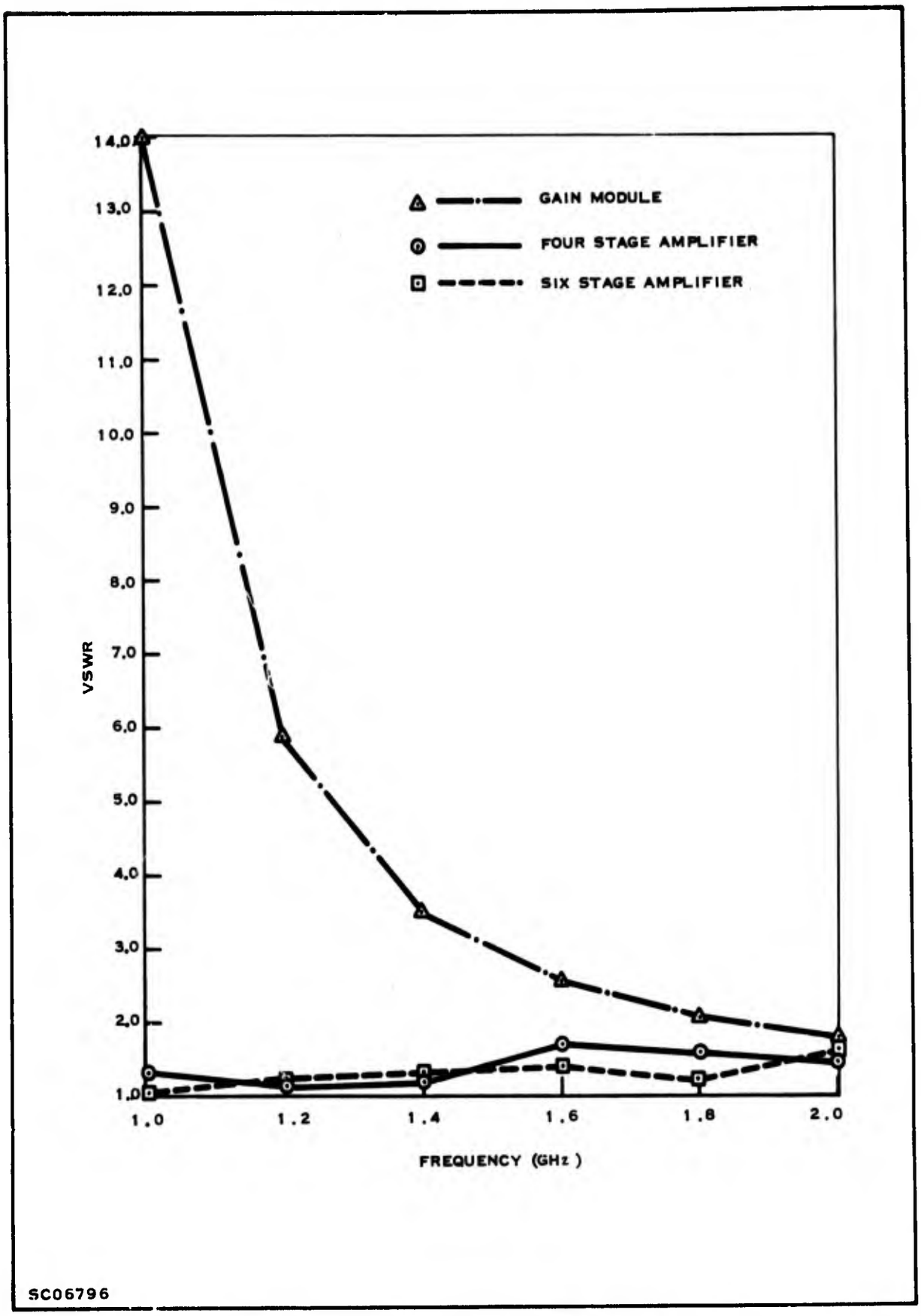


Figure 39. Output VSWR of Gain Module and Balanced Amplifier

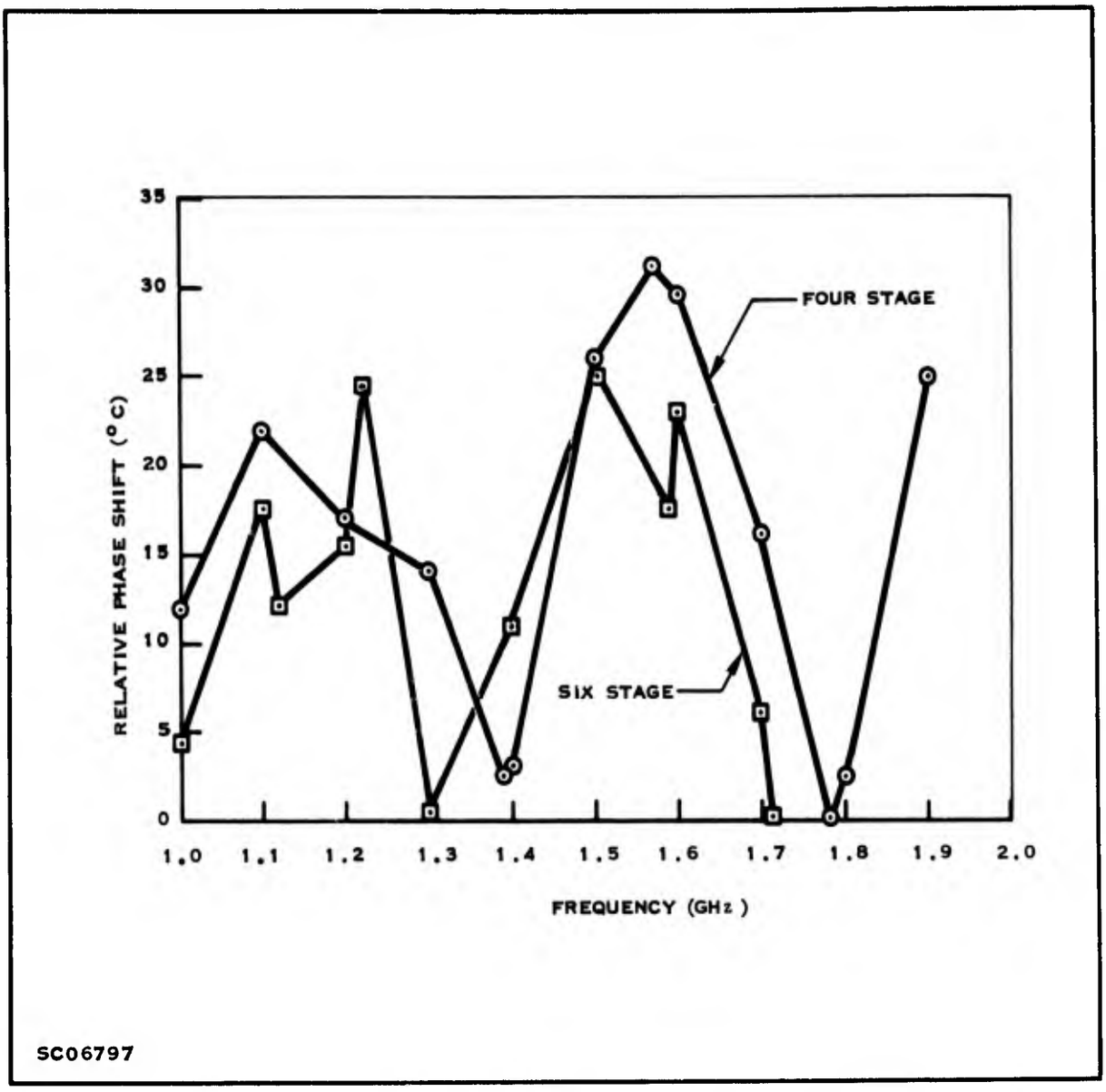


Figure 40. Balanced-amplifier Phase Shift versus Frequency

5. Gain Compression

Figure 41 shows gain versus input power for both the four-stage and six-stage amplifier. Since all stages were biased at the same point, the six-stage saturated first. The -1-dB compression point in both amplifiers occurs at approximately -5-dB output. The L-148 chip, not a large signal device, tends to compress at high signal levels. The performance of this amplifier could be improved by biasing the latter stages at higher currents, but the gain would be reduced. It is felt that ultimately silicon amplifiers in the final stages will give better performance.

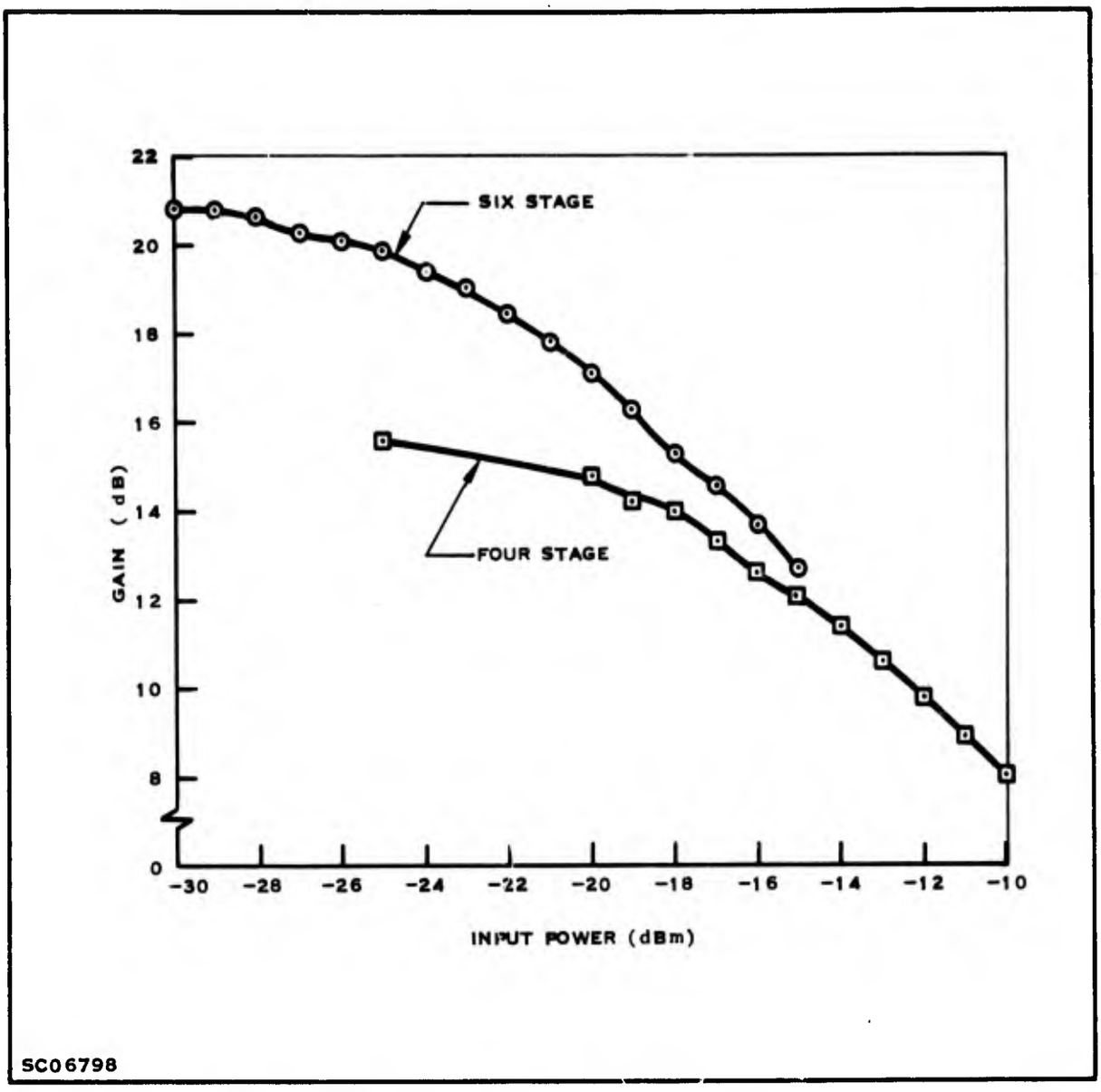


Figure 41. Gain versus Input Power

SECTION VII

CONCLUSIONS

The balanced amplifier is a useful configuration where low VSWR is a requirement. The balanced amplifier can provide a simultaneous low VSWR and minimum noise figure, unless coupler loss masks noise-figure improvement. There is also an improvement of 3 dB in power-handling capability.

The balanced amplifier necessarily requires more space than conventional amplifiers, because of the need for directional couplers and because twice the number of stages is used. The amplifier described here, and previously reported ones, have used couplers between each transistor. This builds up the gain in 4- or 5-dB modules; however, a four-stage amplifier will have 8 couplers. Coupler loss is not negligible in such situations, especially for the tandem three-section couplers used in this amplifier. This cumulative loss can be avoided by building up the gain in modules containing several stages of amplification and having couplers only at input and output. Recent computer programs have been successful in the design of conventional wideband amplifiers useable in systems like this. In fact the design of conventional thin-film amplifiers on ceramic is fairly well established at this time, both at Texas Instruments and elsewhere. Design of satisfactory ceramic directional couplers is not so well advanced. The tandem 8.34-dB coupler is a good start, and can give satisfactory results when carefully constructed. However, it is sensitive to air gaps, like all TEM couplers, and the material available to fill air gaps at present is not optimum. Work is continuing in this important area to develop a wideband coupler which is not degraded by an air gap.

SECTION VIII

SUMMARY

This report covers design and construction of an L-band thin-film balanced amplifier on a ceramic substrate. It includes discussions on the L-148 germanium planar transistor, design of a single-stage thin-film 1-2-GHz amplifier with 5-dB gain and 5-dB noise figure, and a ceramic directional 3-dB coupler with less than 1 dB coupling imbalance and 0.5 dB loss. Design details for the coupler and amplifier are given in the report. Two complete balanced amplifiers were constructed using the couplers and gain modules developed. Design objectives of the amplifier were not met, mainly, it is believed, because of construction problems in the directional couplers. The amplifiers had nominally 18-dB gain for the four-stage and 13-dB for the six-stage unit. Noise figure was typically 7 dB. Input and output VSWR were 2.0 maximum and under 1.6 for most of the 1-2-GHz band. It is concluded that the balanced configuration is effective in reducing VSWR over wide bandwidths. The chief difficulty is with the fabrication of satisfactory directional couplers; further work is being done to improve their producibility.

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APPENDIX A

EFFECT OF POOR TERMINATION

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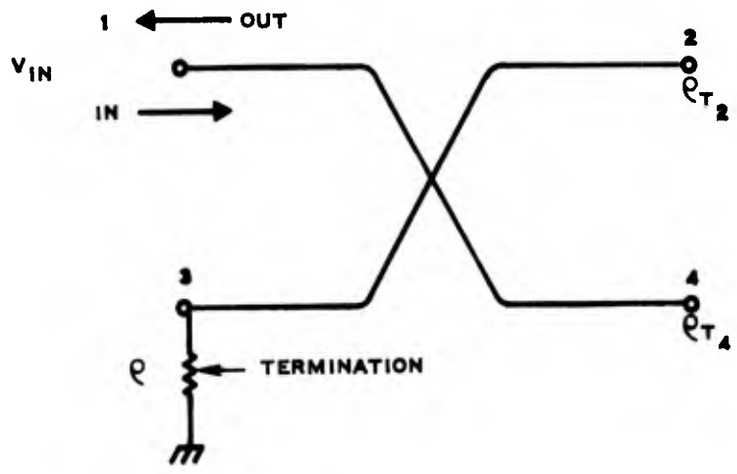
APPENDIX A

EFFECT OF POOR TERMINATION

Calculating effect of poor termination (assuming balanced coupler)



Incident Voltage

$$\text{At } 2 = \frac{V_{in}}{\sqrt{2}} \quad \angle 90$$

$$\text{At } 4 = \frac{V_{in}}{\sqrt{2}}$$

Reflected Voltage

$$\text{At } 2 = \rho_{T2} \frac{V_{in}}{\sqrt{2}} \quad \angle 90$$

$$\text{At } 4 = \rho_{T4} \frac{V_{in}}{\sqrt{2}}$$

Output Voltage At 3

$$V_{inc_3} = \frac{\rho_{T_2}}{2} \cdot V_{in} \angle 90 + \rho_{T_4} \frac{V_{in}}{2} \angle 90$$

Reflected Voltage At 3

$$V_{ref_3} = \rho_R \frac{V_{in}}{2} \angle 90 \quad (\rho_{T_2} + \rho_{T_4})$$

Voltage Coupled to Port 2 from 3 = $\frac{V_{ref_3}}{\sqrt{2}}$

Voltage Coupled to Port 4 from 3 = $\frac{V_{ref_3}}{\sqrt{2}} \angle 90°$

Voltage Out of 1 = $\rho_{T_2} \frac{V_{ref_3}}{2} \angle 90 + \rho_{T_4} \frac{V_{ref_3}}{2} \angle 90$

$$= \rho_R \frac{V_{in}}{4} \angle 180 \quad (\rho_{T_2} + \rho_{T_4}) (\rho_{T_2} + \rho_{T_4})$$

$$\frac{\text{Voltage Out}}{V_{on}} = \rho_{out} = \frac{\rho_R}{4} (\rho_{T_2} + \rho_{T_4})^2 \angle 180$$

APPENDIX B

S-PARAMETERS

APPENDIX B

S-PARAMETERS

S-parameters are ratios of emitted or reflected to incident voltage waves at the terminals of a device when it is inserted in a coaxial or waveguide system. The two terminal S-parameters give input and output immittance information; four terminal S-parameters provide transfer-function information. A two-terminal S-parameter is the complex reflection coefficient; a four-terminal S-parameter is the complex ratio of the voltage wave-out of one port to the wave into another port of a multi-port network.

Figure 42 illustrates the concept of a scattering matrix for a two port network.

The a's represent incident waves; that is, waves travelling into the network under test. The b's represent waves reflected (or emitted) from the network.

The scattering equations for Figure 42 are:

$$b_1 = S_{11} a_1 + S_{12} a_2$$

$$b_2 = S_{21} a_1 + S_{12} a_2 \qquad \text{(B-1)}$$

or, in matrix form

$$\begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} = \begin{bmatrix} b_1 \\ b_2 \end{bmatrix} \qquad \text{(B-2)}$$

S_{11} is the input voltage reflection coefficient when the output is terminated in 50 Ω; S_{22} is the output voltage reflection coefficient when the input is terminated in 50 Ω; S_{21} is the voltage ratio of the output to the input voltage and is a measure of the gain of the device. The quantity $10 \log/S_{21}/^2$ is simply the insertion gain of the device with 50 Ω source and load. This is easily measured with ordinary gain measuring techniques. The quantity S_{12} is the voltage gain (loss) in the reverse direction.

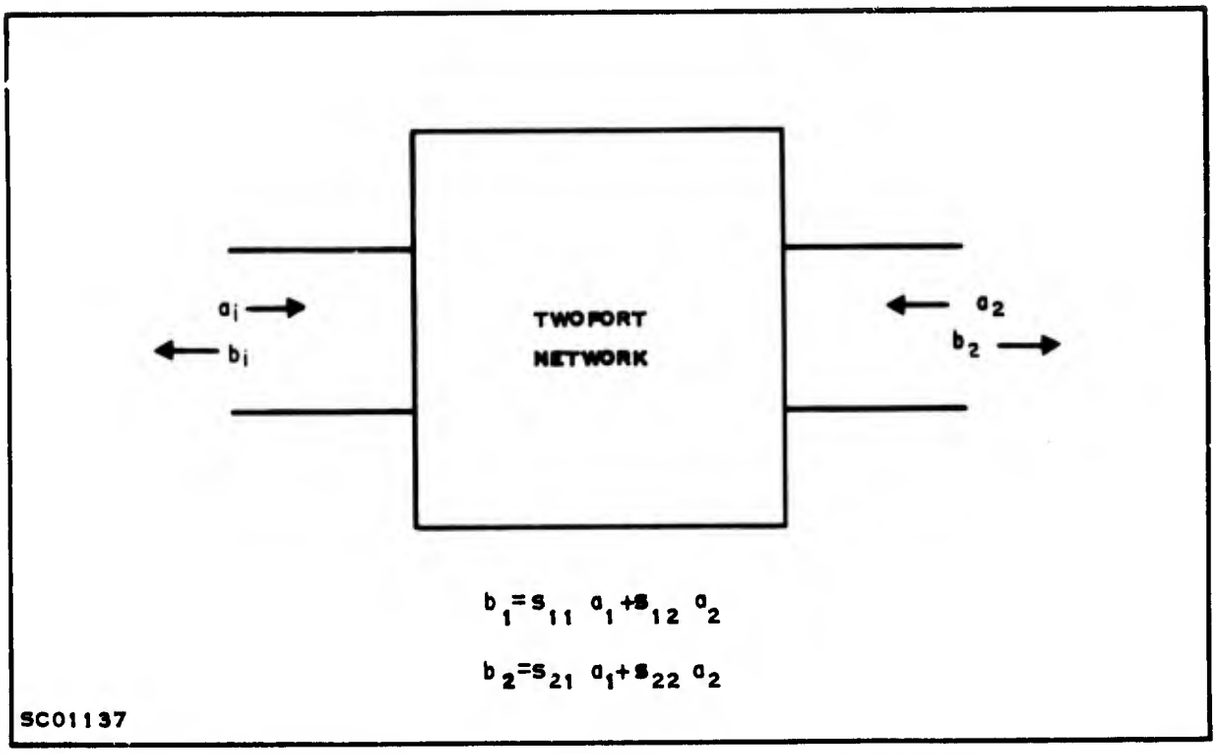


Figure 42. Network Characterized by Scattering Parameters

The S-parameters can be converted to Y-parameters by using the following relations:

$$Y_{11} = Y_o \frac{1 - S_{11} + S_{22} - \Delta S}{1 + S_{11} + S_{22} + \Delta S} \qquad \text{(B-3)}$$

$$Y_{12} = Y_o \frac{-2S_{12}}{1 + S_{11} + S_{22} + \Delta S} \qquad \text{(B-4)}$$

$$Y_{21} = Y_o \frac{-2S_{21}}{1 + S_{11} + S_{22} + \Delta S} \qquad \text{(B-5)}$$

$$Y_{22} = Y_o \frac{1 + S_{11} - S_{22} - \Delta S}{1 + S_{11} + S_{22} + \Delta S} \qquad \text{(B-6)}$$

where

$$\Delta S = S_{11} S_{22} - S_{12} S_{21} \qquad \text{(B-7)}$$

These equations were programmed on a computer so the Y-parameters could be calculated from the measured S data. It should be noted that small errors in the S-parameters can cause large errors in the Y-parameters when converted. This is one of the major reasons for doing the amplifier design in S-parameters.

The system used to measure the parameters is shown in Figure 43. In this system the input RF signal is divided into two paths: one path becomes the reference branch, the other becomes the test branch where the network under test is inserted. The signal in this branch is modulated with 1000 Hz and attenuated before application to the network under test. The reference and the test branch signals are then applied to a phase discriminator which produces 1000 Hz outputs proportional to the real and imaginary parts of a signal. These are synchronously detected to give a dc output proportional to the 1000 Hz input. An oscilloscope can be used to display complex return loss, gain, or impedance on a Smith chart. The frequency can be swept with some reduction in accuracy.

SUPPLEMENTARY

INFORMATION

TAB No. 70-1 1 January 1970

DISTRIBUTION AND AVAILABILITY CHANGES

IDENTIFICATION	*FORMER STATEMENT*	*NEW STATEMENT*	*AUTHORITY*
AD-810 483 Texas Instruments Inc. , Dallas. Semiconductor-Components Div. Rept. no. 8 (Final), 1 Jun 64-31 May 66. Rept. no. ECOM-00109-F Mar 67 Contract DA-28-043-AMC-00109(E)	No Foreign without approval of Commanding General, Army Electronics Command, Attn: AMSEL-KL-SM, Fort Monmouth, N. J.	No limitation	USAEC ltr, 1 Oct 69