PRELIMINARY DESIGN OF ROCKET-BORNE CRYOGENIC DEWAR AND SIGNAL ELECTRONICS

Carl R. Bohne, et al

Honeywell Radiation Center

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The preliminary design or a cryogenic, rocket-borne dewar and associated signal electronics are described. The design and testing of two cryogenically cooled test dewars are also described. This instrumentation is to be used in connection with rocket probe measurements of the infrared emissions of the airglow and aurorae.

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PRELIMINARY DESIGN OF ROCKET-BORNE CRYOGENIC DEWAR AND SIGNAL ELECTRONICS

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November 1973

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AIR FORCE CAMBRIDGE RESEARCH LABORATORIES
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ABSTRACT

Dewars for the development testing of interferometer components at liquid nitrogen and liquid helium temperatures under simulated sounding rocket shock and vibration loading were designed, built, and tested. Support provided for the cryogenic testing of these components is described. Preliminary design of a helium dewar and signal electronics for flight implementation of the interferometer into a measurement program utilizing a Black Brant VC sounding rocket is included.

The following scientific personnel participated in this effort:

Harold W. Robinson, Jr. - Program Manager

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Pat Dunbar

Leland Peters

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Kenneth Lang

William Corker

Roger Coda

Anthony DeLuzio

Eben Hiscock - AFCRL

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SECTION 1

INTRODUCTION

The Dewar Assemblies program involved design, manufacture, test, and usage support of test dewars for development testing of cryogenic interferometer components. In addition, tasks were included for preliminary design of a flight dewar and flight electronics to support utilization of a cryogenic interferometer in a sounding rocket launched measurement program. The results of these latter tasks have been reported separately, copies of which have been included as appendixes for completeness.

This report describes the design and qualification testing of the two interferometer test dewars and a component test dewar which were required to support the cryogenic testing of prototype flight interferometers and associated components. The two interferometers were developed separately by Idealab and Block Engineering. A basic dewar design was derived and with minor modifications was implemented for each of the two interferometers.

Initially, program requirements called for two interim liquid nitrogen interferometer dewars to circumvent suspected longer development times associated with helium dewars. Vendor deliveries for either dewar were equivalent, hence the nitrogen and helium test capability was incorporated into a single dewar.

The test dewars had as major performance requirements the following two criteria:

(a) Provide a cold environment for the interferometer and its supporting components. Capability for testing at liquid nitrogen and liquid helium temperatures was required.

(b) Provide for testing of the interferometer to the environmental levels (shock and vibration) to be expected from a sounding rocket launch vehicle.

It was found that both requirements could be met by upgrading a readily available commercial dewar design.

An additional task called for the support of concurrent testing and qualification of individual components for the prototype

1<

flight interferometer. Ultimately the environmental qualification of the components was completed in the interferometer test dewars; however, a substantial amount of prior component cold testing was required. For this purpose a small optical component dewar, again utilizing liquid helium, was obtained.

The dewars were fabricated and did support development testing of beamsplitters, monochromatic reference sources, white light reference sources, the interferometer slide assembly, focal plane assembly, V-cube alignment, and ultimate qualification of complete interferometer assemblies.

2<

SECTION 2

TEST DEWARS - PERFORMANCE CRITERIA AND DESCRIPTION

2.1 COMPONENT TEST DEWAR

For the low temperature testing of interferometer components a small laboratory dewar was necessary. This dewar was required to have the following capabilities:

(a) Small size for compatibility with optical test setups;

(b) Liquid helium operation;

(c) Rapid turnaround time;

(d) Optical access to couple radiation in or out.

A commercial liquid nitrogen shielded helium dewar was available and with minor modifications met the above operating criteria. This was designated as a Model RD-1534 research dewar by the manufacturer, Janis Research Company, and is shown in Figure 2.1.

This dewar has a capacity of two litres of helium providing six hours of test time at operating temperatures of 5 - 20 °K and 1.25 cubic inches of test volume is available at 5 °K which may be increased to 5 cubic inches at 10 - 20 °, with the addition of the tail piece assembly. A nominal cooldown time of one hour has been experienced. Empty weight of the dewar and its mounting fixture is 35 pounds.

2.2 INTERFEROMETER DEWARS

2.2.1 General

A standard Cryogenics Associates dewar design Model IR 104 was chosen as the basis for the interferometer test dewar. This was a unit which had been proven successful by its manufacturer for liquid helium testing of large components. To adapt this dewar specifically for the considerations of this program the following were required:

(a) Provide for 6 to 8 hours testing time at operating temperature between helium fills;

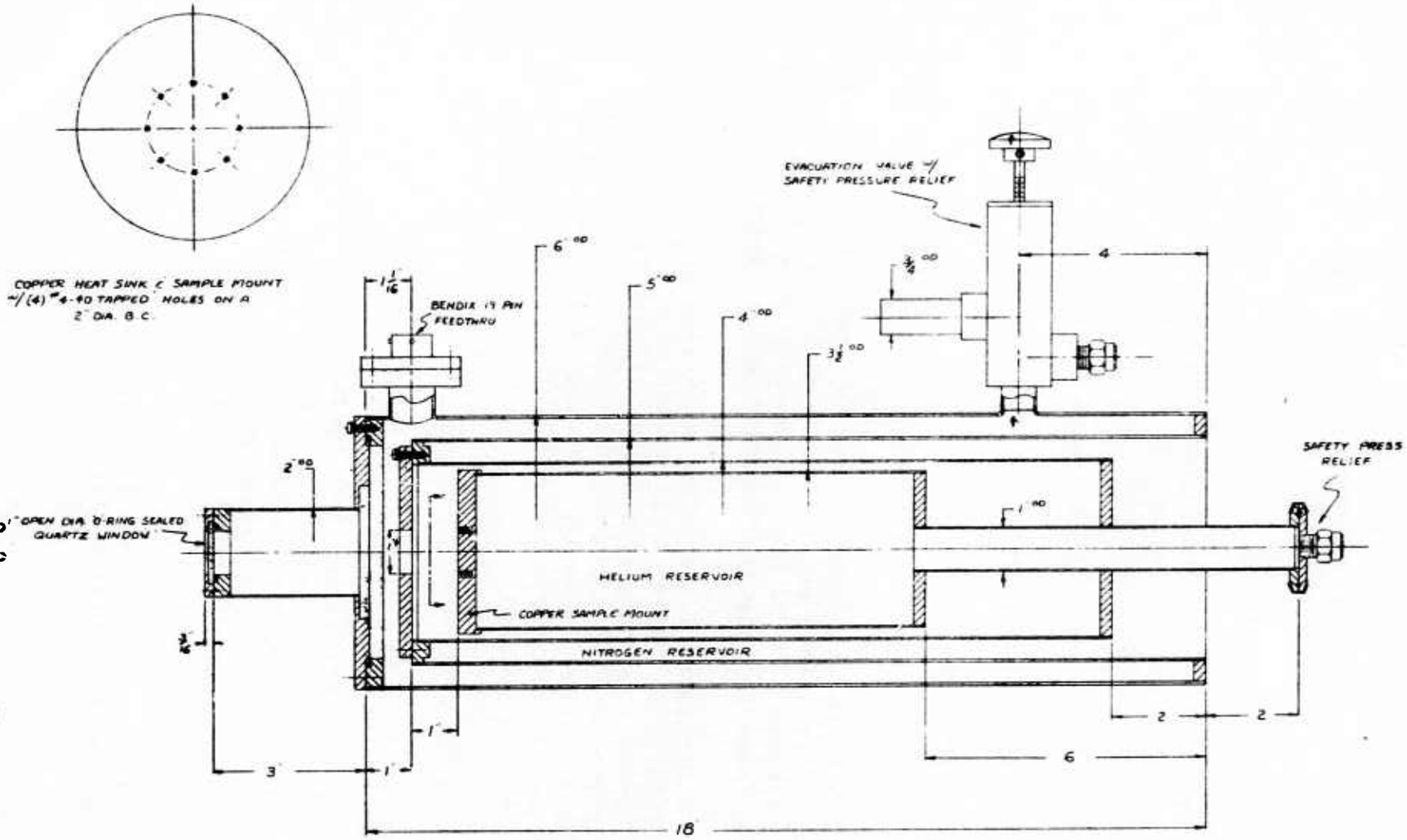

Figure 2.1 MODEL RD-1534, RESEARCH DEWAR

(b) Provide capability for vertical or horizontal operation;

(c) Provide an internal volume capable of holding the interferometer and relay optics;

(d) Provide optical access for visual observation or an external laser input;

(e) Provide capability for running interferometers in a vacuum or cold gas environment using either helium or nitrogen;

(f) Include capability for shock and vibration testing of the cold interferometer to the Black Brant VC launch environment.

The final design is as shown in Figures 2.2 and 2.3 incorporating modifications described in HRC engineering specification 2100 8067. Specifically, this is the model which was provided to Block Engineering Co., and was designated as a Model IR118 by the manufacturer. This is typical for both dewar models. Each dewar has a capacity of 10 litres of liquid helium and weigh 100 pounds empty. The features unique to each design are discussed separately in sections 2.2.2 and 2.2.3.

2.2.2 Idealab Test Dewar

The Idealab interferometer test dewar is identical to the unit shown in Figure 2.2 with minor exceptions. Principally, these include two versus one optical windows, and location of the helium vent connection closer to the dewar evacuation valve. During operation this orientation caused freezing problems with the valve and its location was moved in the Block unit to eliminate this problem.

The dewar contains 10 litres of liquid helium capable of providing 6 - 8 hours of test time at temperature. Internal volume is sufficient to mount the prototype flight interferometer such that its optical axis may be co-aligned with one of the optical ports. Cooldown time to an operating temperature at the test fixture of 15 °K is 14 hours using an A-2 steel interferometer as the thermal loading. Eight to ten hours of pumping are required prior to cooling. The interferometer mounting fixture is shown in Figure 2.4 and represents the flight design devised to minimize vibration amplification to critical optical components such as the beam

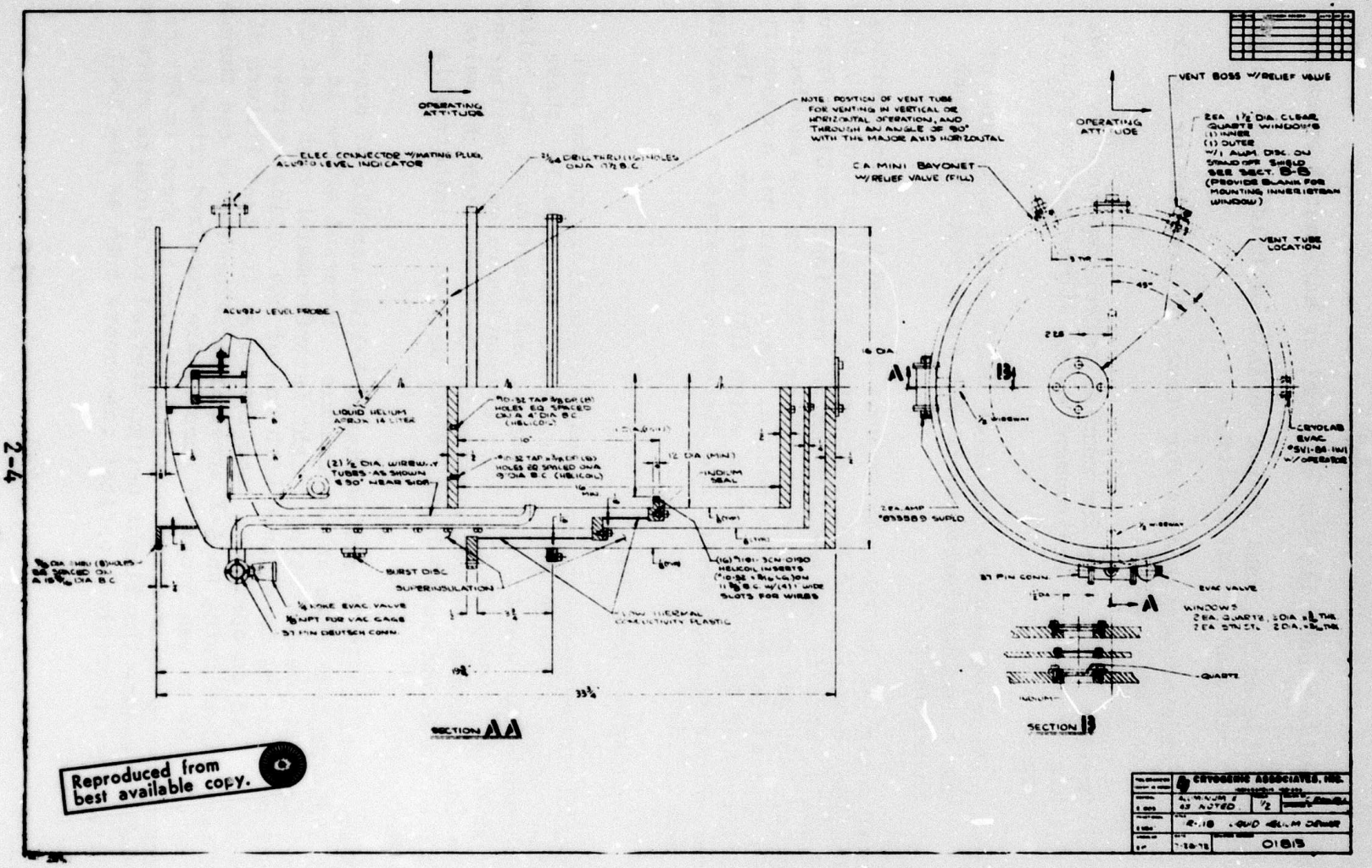

Figure 2.2 LIQUID HELIUM DEWAR

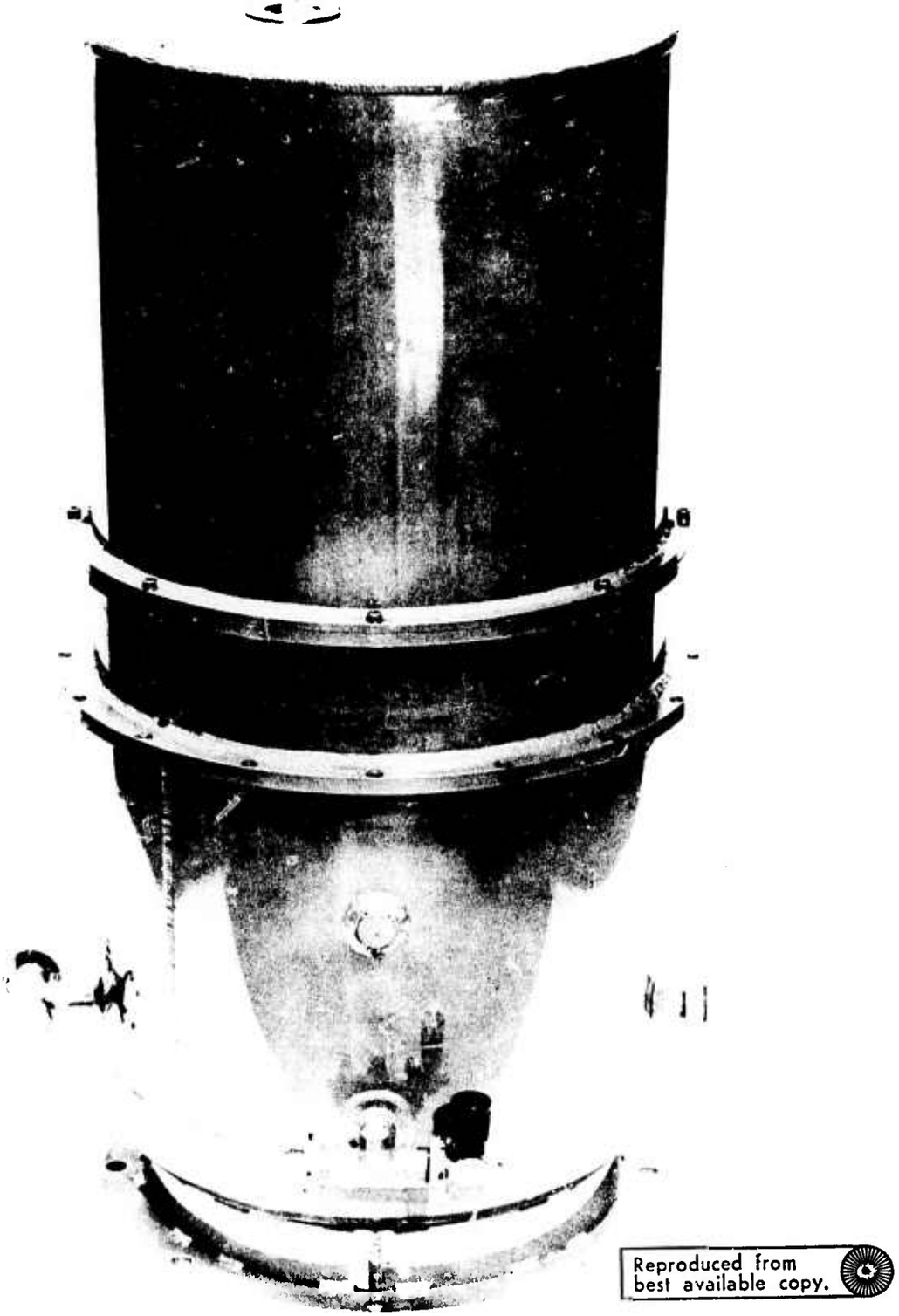

Figure 2.3 INTERFEROMETER TEST DEWAR

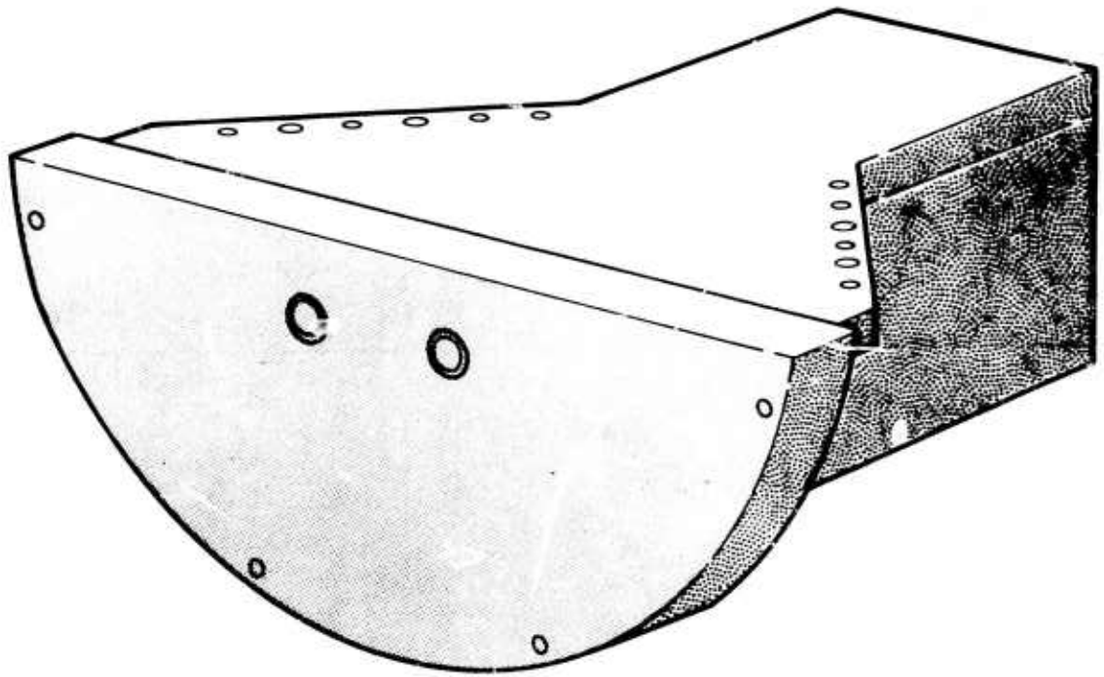

Figure 2.4 INTERFEROMETER MOUNTING FIXTURE

splitter and slide assembly. A dewar vibration test fixture was designed and fabricated by Acton Environmental Testing Laboratories and is shown in Figure 2.5.

A resonant search was performed in accordance with environmental specifications (Appendix B) on this dewar to identify any potentially troublesome modes prior to testing the interferometer. A 48 pound copper weight was fastened to the interferometer mount to simulate the interferomecer loading. A liquid helium fill time of six hours was experienced in this configuration. The results of this resonance survey are contained in Acton Environmental Test Report No. 9624. The test was conducted on a warm dewar. Leak checks were performed after the test. No adverse resonances were encountered and the dewar was considered suitable for use. (Figure 2.6)

A failure of the on board liquid level gauge was noted upon completion of the resonant search. This was attributed to the method of securing the gauge within the helium container and was corrected in the unit supplied to Block Engineering. The loss of this gauge made necessary the use of weighing techniques in all subsequent filing operations.

Considerable environmental as well as static laboratory testing using this dewar was subsequently performed. This is further discussed in Section 3. The dewar proved to be completely adequate for all test purposes.

2.2.3 Block Engineering Test Dewar

The Block Engineering test dewar is the more recent of the two versions and incorporates minor improvements dictated by the experience gained from using the Idealab unit.

A redesigned mounting for the level probe Model ACL-920 was incorporated. This satisfactorily withstood the loads imposed during the proof environmental testing. This mounting scheme, proprietary with Cryogenics Associates, Inc. was also incorporated in the HIRIS flight dewar design. We therefore had the opportunity to develop this technique prior to its utilization in the flight program.

The only operational differences between the Block and Idealab versions of the dewar was in the number and location of windows and electrical feedthroughs. Neither of these is critical to the dewar and thus the Block Engineering version only is shown as being

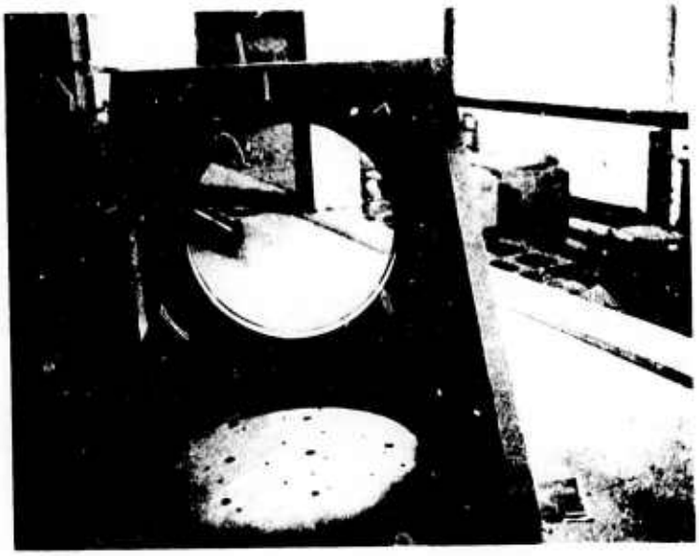

Figure 2-5 DEWAR VIBRATION FIXTURE

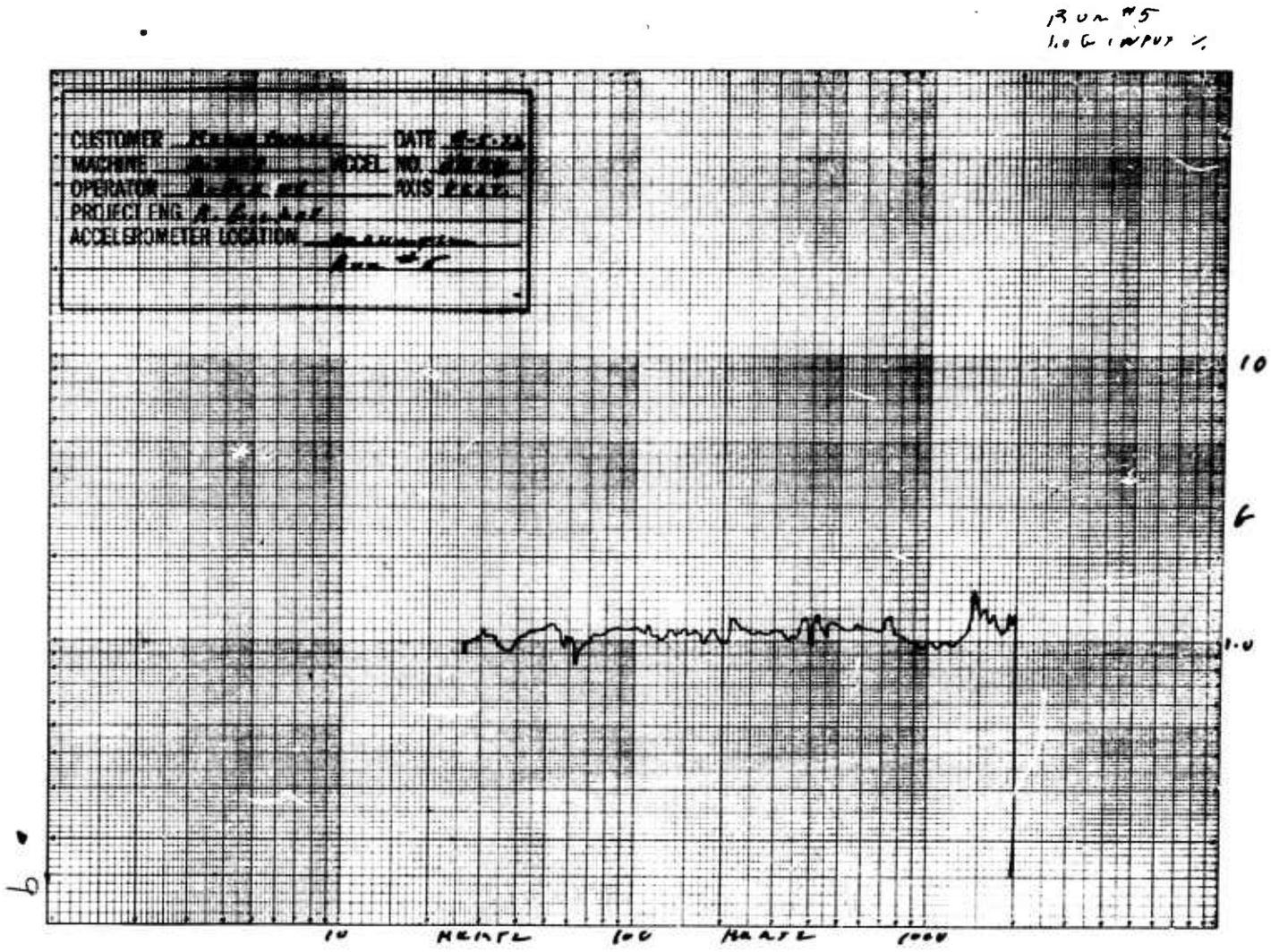

Figure 2.6 IDEALAB TEST DEWAR - SINE SWEEP (AMBIENT)

representative of that required for cold interferometer testing.

Both warm and cold environmental tests were made of the dewar. A 39 pound mass was mounted on the dewar to simulate interferometer loading. Accelerometers were mounted in each of the three test axes on the dummy mass mount. The results of these tests are contained in Acton Environmental test reports number 9702 and 9702-1. The dewar was leak checked following each test. No adverse resonances were observed and the dewar was found suitable for its intended use. Performance of this dewar was similar to the Idealab dewar (Figures 2.7 through 2.10).

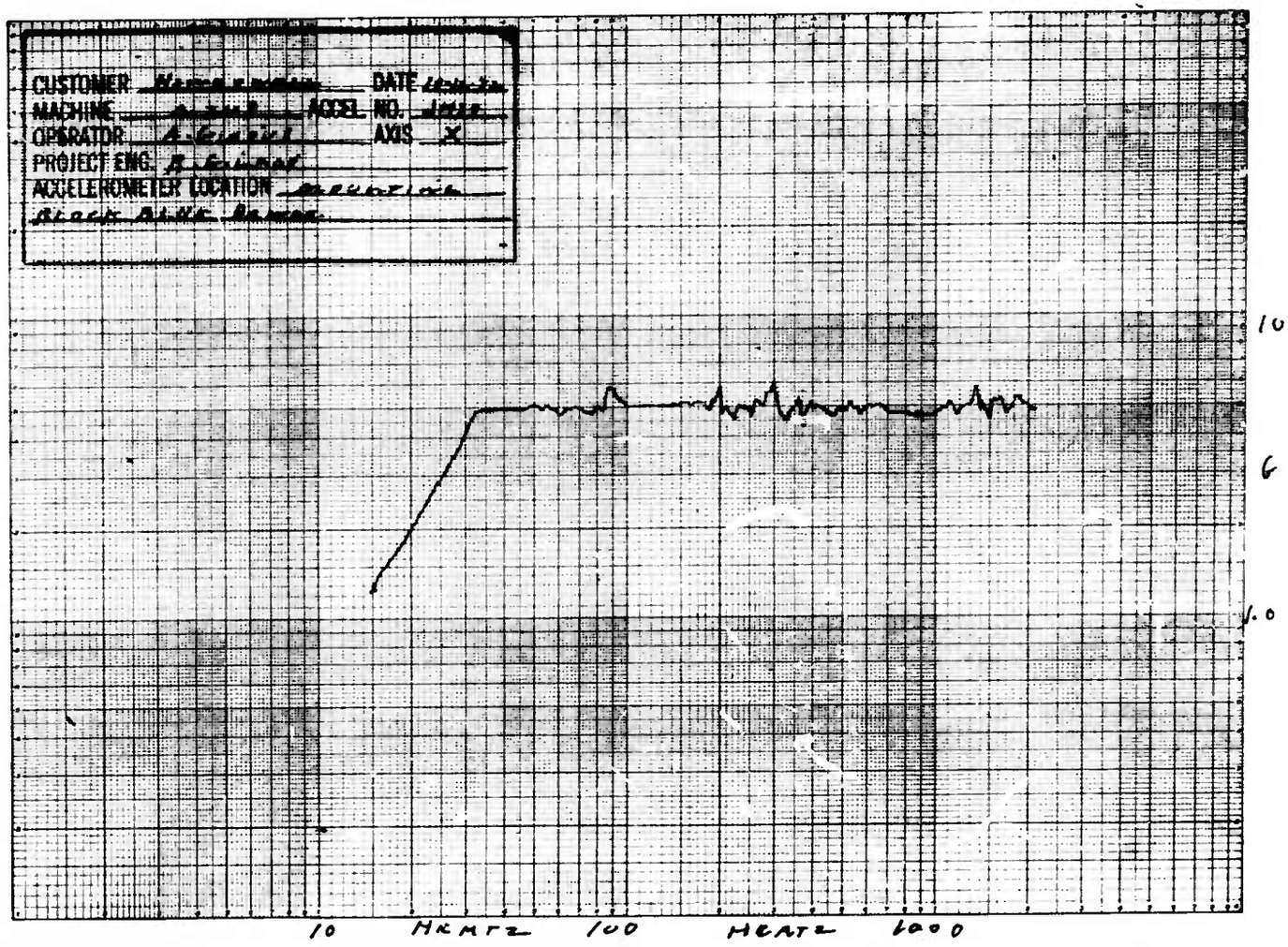

Figure 2.7 BLOCK TEST DEWAR - SINE SWEEP (AMBIENT)

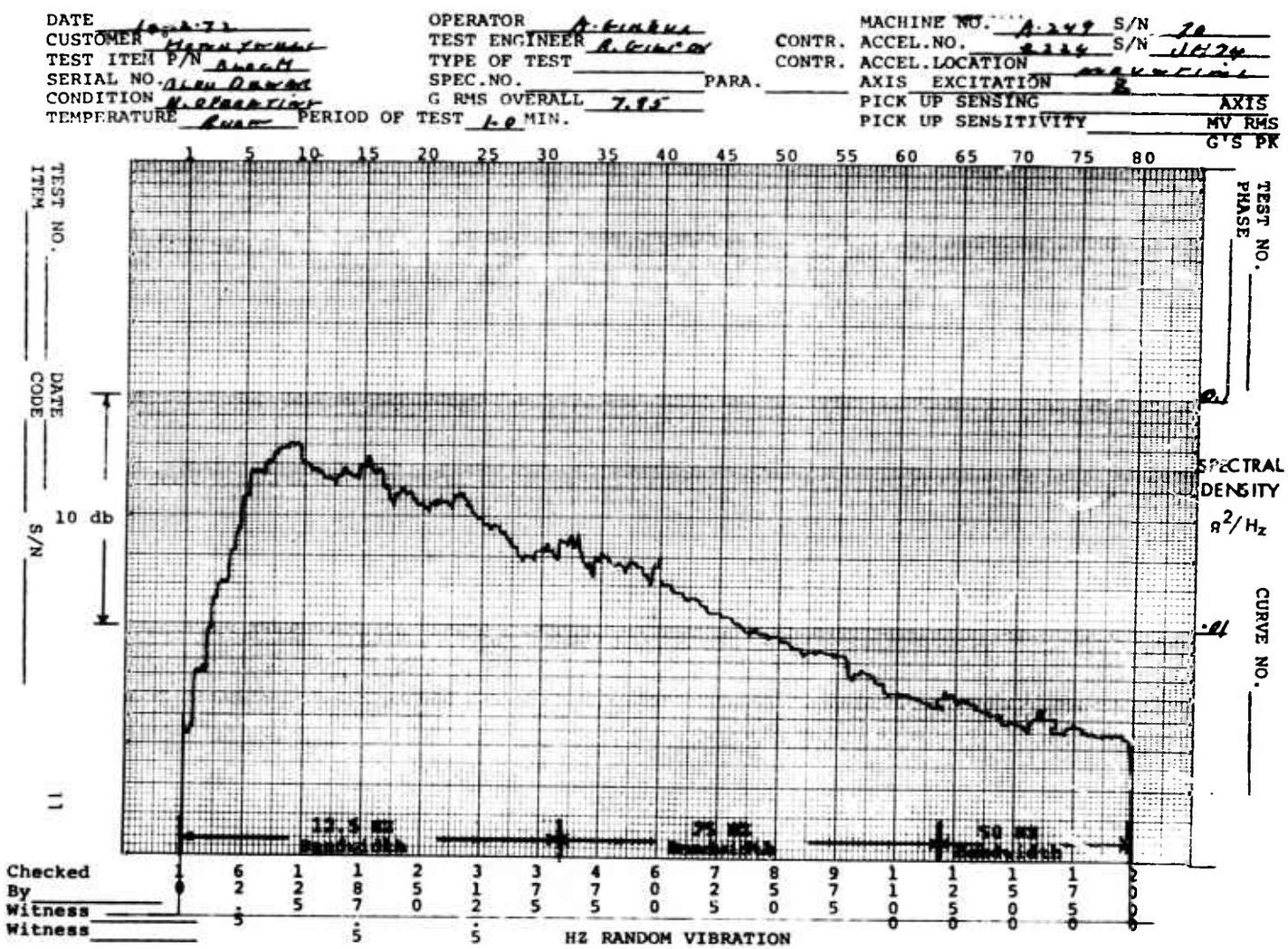

Figure 2.8 BLOCK TEST DEWAR - RANDOM SHAKE (AMBIENT)

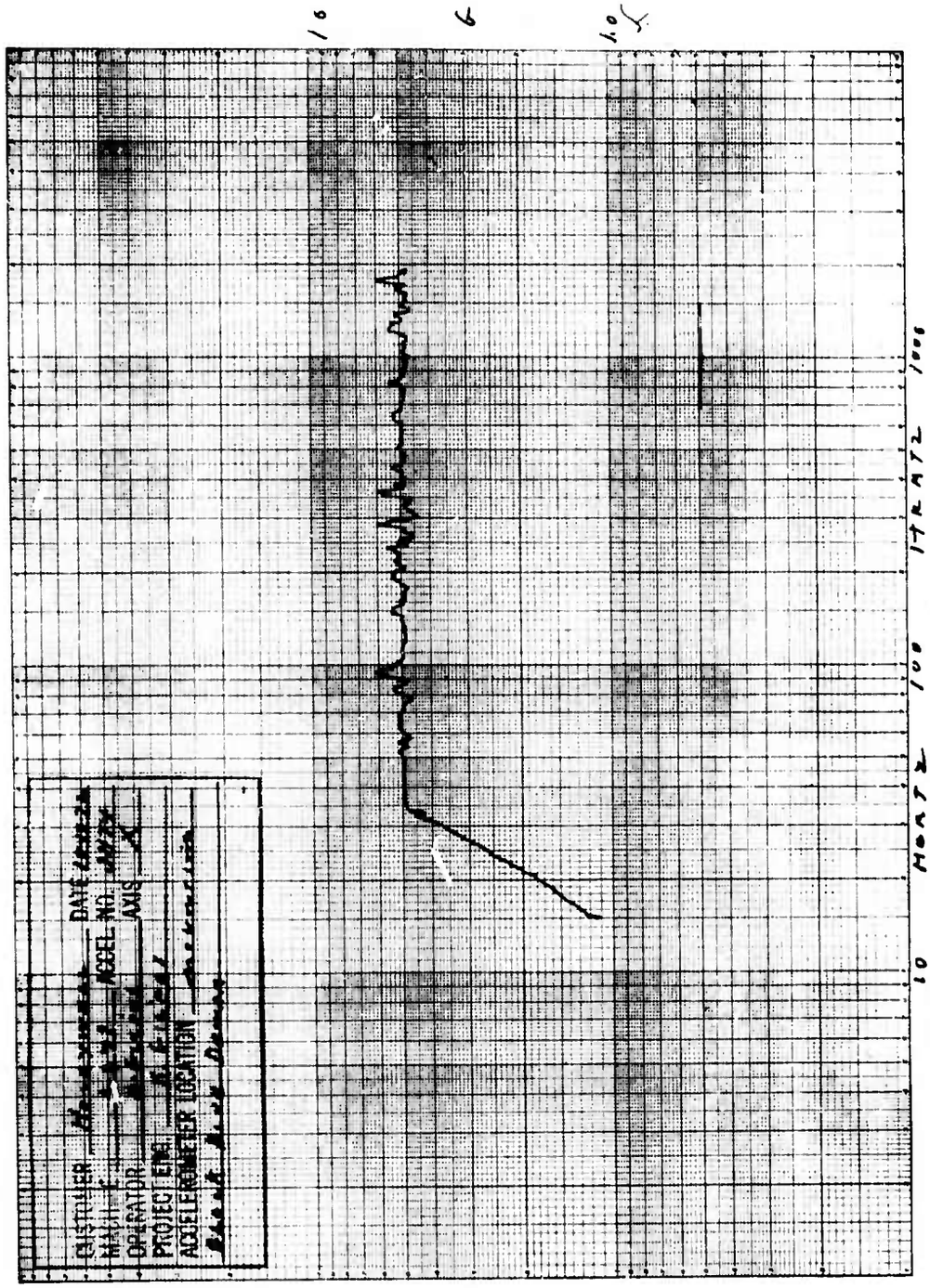

Figure 2.9 BLOCK TEST DEWAR - SINE SWEEP (COLD)

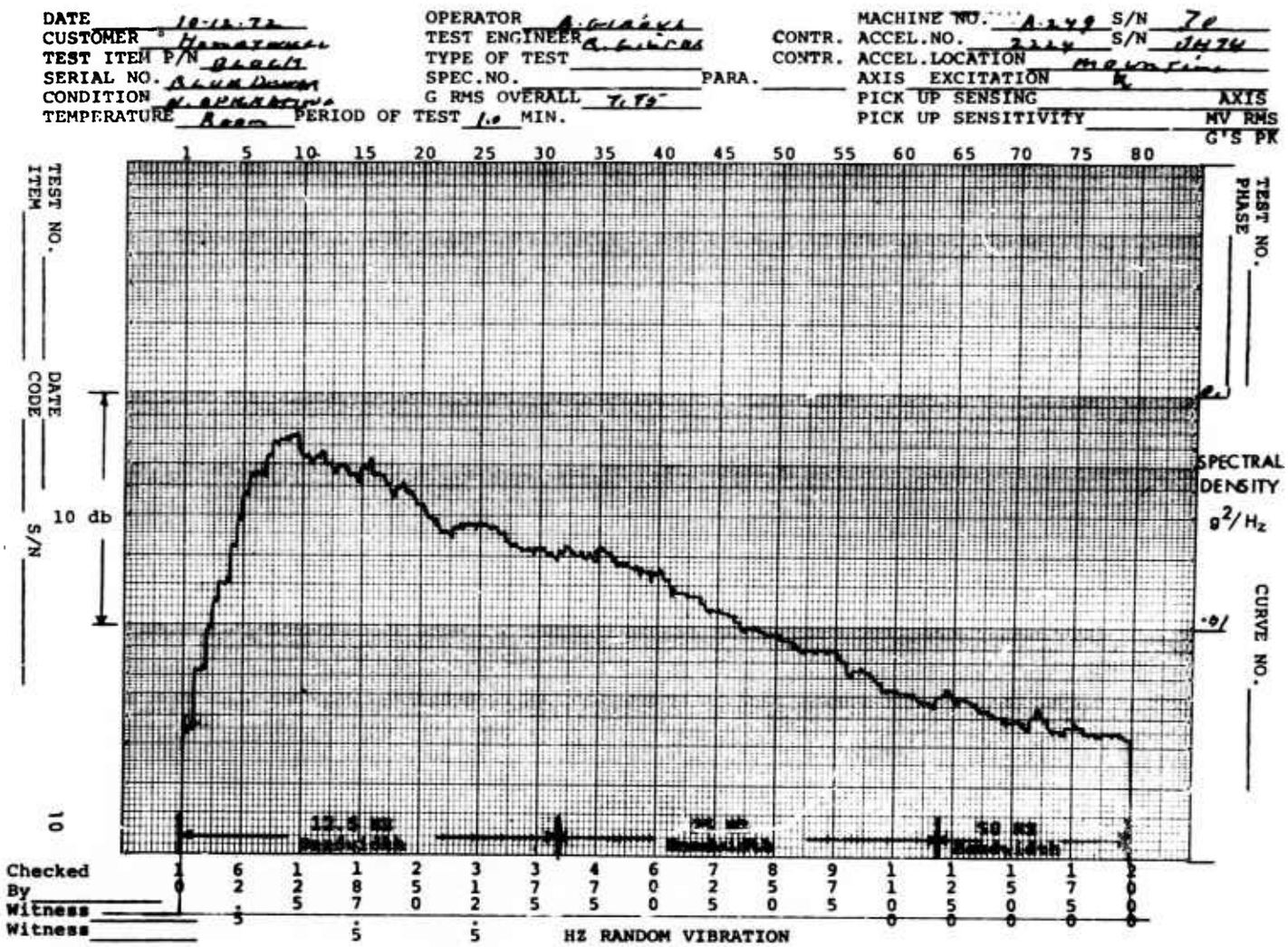

Figure 2.10 BLOCK TEST DEWAR - RANDOM SHAKE (COLD)

SECTION 3

LIQUID HELIUM TESTING SUPPORT

During the HIRIS flight interferometer development phase the test dewars were extensively utilized for low temperature testing of various components. These tests consisted of the following for the individual items as required.

(a) Low temperature operation

(b) Low temperature compatibility

(c) Qualification for environmental loads (shock and vibration)

(d) Determining effect of temperature on performance

(e) Calibration of low temperature thermometers

A listing of the major testing sequences which were supported using each of the dewars is listed below. In general this listing is representative only because in many cases more than one test was performed and both dewar designs, (interferometer and component test dewars) were utilized.

(a) Interferometer test dewar (Idealab)

1. Interferometer cold test and alignment
2. Interferometer qualification to shock and vibration
3. Environmental testing of detector focal plane
4. Focal plane response
5. Beam splitter thermal, shock and vibration testing
6. Interferometer slide test (servo-controlled slide velocity linearity)
7. White light shock, and vibration qualification

(b) Interferometer test Dewar (Block Engineering)

This dewar was delivered to Block Engineering for use

in their facility. No liquid helium testing support was required for this dewar.

(c) Component test dewar

1. White light developmental testing

2. Neon bulb and band pass filter cold testing

3. Laser diode cold performance testing

4. Interferometer system electronics performance testing

Since the objective of this effort was to provide cryogenic test support to interferometer and component developers, the reporting of results and evaluation of this testing will be left to these developers.

APPENDIX A

TEST DEWAR ENGINEERING SPECIFICATION

21008067

INTERPRET DRAWING IN ACCORDANCE WITH MIL-D-1000, FORM 3

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	[illegible]	3 May 72	[illegible]

HONEYWELL PART NO.
21008067 -101

APPROVED SOURCE OF SUPPLY

CRYOGENIC ASSOCIATES INC

INDIANAPOLIS, INDIANA

SHEET	1	2	3
REV	A	A	A

TOLERANCES UNLESS NOTED OTHERWISE	
.X ±.020	ANGLES ±
.XX ±.010	
.XXX ±.005	
EPA	
FINISH—SEE NOTE	
MATERIAL PURCHASED — SEE NOTES	

DRAFTSMAN	P.S.	30 Apr 72
CHECK	[illegible]	3 May 72
PKG ENG		
DEV ENG	[illegible]	3 May 72
PROJ ENG	C.R. Baine	
RELIABILITY		
ELEC ENG		
ENGRG RCD RLSE		
CONTRACT NO.		

HONEYWELL INC.
RADIATION CENTER
LEXINGTON, MASS.

INTERFEROMETER TEST DEWAR - (ICE CAP)

SIZE	CODE IDENT NO.	DRAWING NO.
A	81395	21008067

SCALE /	WT	SHEET 1 OF 3

HRC9-71

20<

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	[illegible]	3 Feb 72	[illegible]

INTERFEROMETER TEST DEWAR - (ICE CAP)

Modifications for Cryo. Assoc. Dwg. 01724A

1. 10" Dia. -- make 12" Dia. (14" Dia. ⟶ as req'd)

2. 14" Min. -- make 16" min. (length dimension)

3. Optical access - (2)-2½ clear diameter aperture, provided in outer shell, radiation shield and inner vacuum can. Outer to be "O" ring sealed; inner to be indium sealed. Provide extra set of blank inner flanges to be future machined for another Material (Irtron II or VI). Provide blank (screw fastened) aluminum covers for the radiation shield. Access ports to be 2 1/16 inches either side of dewar center line (4 1/8 inches between). Provide quartz windows with dewar. Dewar to be checked (LN_2 or helium) for cold seal of window. For either case Vendor is to guarantee vacuum integrity of liquid helium temperature of inner windows. (Quartz material only)

4. Bolting patterns of dewar components and sensor mounting ring shall have a common center line with the optical access. Bolting patterns shall be a multiple of 8 (eight) holes.

5. The liquid helium vent line shall be positioned to allow for vertical or horizontal operation. In addition the dewar shall be operable when rotated through an angle of 90° with the major axis horizontal. In all operating modes (as stated) the liquid helium hold time must not be already effected.

6. The following points are further identified on the enclosed marked up print.

   a. Extend fiberglass support ring for dewar mounting. Ring to be 1" wide. Provide (16) clearance holes for 5/16 dia. bolts.

   b. Sensor mounting ring with mounting holes.

   c. Mating operator for cryolab valve.

SIZE	CODE IDENT NO.	21008067
A	81395	
SCALE	WT	SHEET 2 OF 3

REVISIONS			
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d. Specifications for indium seal wire also spare wire for initial cap replacement.

e. Anchor radiation shield to bottom stand-off.

f. Provide (2) "O" ring sealed demountable feed thrus Bendix Pygmy #(PT1H-14-15 P) or equal.

g. Provide Veeco Vacuum Valve (3/8 size) with tube extension 1 1/2 inch long.

h. Change mounting hole pattern on the base.

i. Provide blind tapped holes (w.helicoil inserts) in helium flange bottom plate.

j. (1/8 NPT) coupling in electrical access line for vacuum gage.

7. Provide outline drawing of transfer hose. Hose is to terminate in 90° bend with a 3/8 inch diameter by 58 inch long dip tube end.

8. Provide details of Model ACL-920 level probe including electronics.

SIZE	CODE IDENT NO.	21008067
A	81395	
SCALE	WT	SHEET 3 OF 3

HRC10-71

APPENDIX B

FLIGHT DEWAR SHOCK AND VIBRATION

SPECIFICATION 22913ES01

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NRC 1-71

CODE IDENT NO. 81395

ENGINEERING SPECIFICATION NO. 22913 ES01

THIS ENGINEERING SPECIFICATION IS FOR: ☐ SYSTEM ☐ DEVICE ☐ ASSEMBLY ☐ OTHER

LIST DEVICE AND/OR SUBASSEMBLY

FLIGHT DEWAR SHOCK AND VIBRATION SPECIFICATIONS

SIGNATURES		DATE
PREPARED BY	W. K. Taylor	6/23/72
APPROVED BY PROJECT ENGR.	C. R. Bolme	6/23/72

REVISIONS

LTR	DESCRIPTION	DATE	APPROVAL	LTR	DESCRIPTION	DATE	APPROVAL
A	ENGINEERING CONTROLLED RELEASE	6/26/72	JM				

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CODE IDENT NO. 81395

ENGINEERING SPECIFICATION NO. 22913ES01

1.0 TEST CONDITIONS

1.1 Install the mass mock-up of the interferometer, baffles and the front cover assembly into the dewar. The mock-up of the interferometer and baffle assembly, with supports, will weigh 40 lbs. The front cover assembly will weigh 12 lbs.

1.2 The dewar will be evacuated to 10^{-6} Torr and subjected to the qualification levels described in the subsequent sections - 2.0, 3.0 and 4 0

1.3 The dewar will be then evacuated to 10^{-6} Torr and then cooled with liquid helium until the cryogen tank is filled at which time the system will be switched to operation in the super critical mode. Upon reaching stable operating conditions the dewar will be subject to the pre-flight levels described in subsequent sections - 2.0, 3.0 and 4.0.

2.0 SINUSOIDAL VIBRATION

2.1 Sweep

Each sinusoidal vibration test will be based upon a single logarithmic sweep with a total duration of 115 seconds at the rate of 3.7 octaves/min.

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2.2 Axes

A test will be performed with the instrument oriented on each of the three mutual orthogonal axes. These will be:

a. Longitudinal axis (thrust direction)

b. 2 lateral (radial) axes which will be specified relative to the radiometer interface.

2.3 Levels

2.3.1 Qualification Levels - Longitudinal and lateral directions 0.1 in D.A. from 15-31 Hz and then 5.0 g, 0-peak, from 31-2000 Hz.

2.3.2 Pre-flight Levels - Longitudinal and lateral directions .06 in D.A. from 15-31 Hz and then 3.0 g, 0-peak, from 31-2000 Hz.

3.0 RANDOM VIBRATION

3.1 Duration

a. Qualification levels - 1 minute/axis

b. Pre-flight levels - 1/2 minute/axis

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3.2 Axes

See 2.2

3.3 Levels

3.3.1 Qualification Level 7.75 g (RMS)

Frequency	Spectral Density (RMS)
20 Hz	.0125 g^2/Hz
20 - 80 Hz	+3db/octave
80 - 140 Hz	.05 g^2 Hz
140 - 2000 Hz	-3db/octave
2000 Hz	.0034 g^2/Hz

3.3.2 Pre-flight Levels 6.5 g (RMS)

Frequency	Spectral Density (RMS)
20 Hz	.0085 g^2/Hz
20 - 80 Hz	+3db/octave
80 - 140 Hz	.035 g^2/Hz
140 - 2000 Hz	-3db/octave
2000 Hz	.0024 g^2/Hz

4.0 SHOCK

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ENGINEERING SPECIFICATION NO. 22913ES01

4.1 Configuration

A shock test will be performed on each axis. The pulse shape will be Terminal-Peak Sawtoothed Shock Pulse per MIL-STD-810. The peak value of acceleration and the duration will be 20 g and 11 milliseconds respectively (Procedure I, basic design for Flight Vehicle equipment). Testing to this pulse will be done on qualification and pre-flight testing.

4.2 Axes

See 2.2

4.3 Levels

Testing to 4.1 will be done on qualification and pre-flight tests.

5.0 ACCELERATION

5.1 Duration

30 seconds for each axis

5.2 Levels

Longitudinal axis (thrust direction) 15 g. Lateral axis 5 g (about spin axis) for both axes.

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ENGINEERING SPECIFICATION NO. 22913ES01

6.0 ACCEPTANCE CRITERIA

6.1 If it appears that a failure has occured during testing, the tests will be stopped and the dewar examined. A failure shall consist of broken or cracked parts, loss of vacuum, hold time, or cryogen. Repair and modification will then be performed to insure that the failure will not re-occur. The unit will then be subjected to the full environmental test requirement again.

6.2 Upon completion of each stage of testing (evacuated, warm per para. 1.2 and evacuated, cold para. 1.3) the removeable parts will be disassembled and inspected for failure. Such a failure will be treated per para. 6.1.

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APPENDIX C
FLIGHT DEWAR DESIGN REPORT

FLIGHT DEWAR DESIGN REPORT

Contract No. F19628-72-C-0325

Project No. FY71217203351

Task No. Sub-Line Item 0001AA

Design Report No. 1

4 December 1972

Prepared For

Air Force Cambridge Research Laboratories
Air Force Systems Command
L. G. Hanscom Field
Bedford, Massachusetts

Contract Monitor: Dean F. Kimball (OPR)

Prepared by: William R Corker
W. R. Corker

Approved by:
H. W. Robinson, Jr.

This report is intended only for the internal management use of the contractor and the Air Force.

HONEYWELL RADIATION CENTER
HONEYWELL INC.
Lexington, Massachusetts

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INTRODUCTION

This report describes the design, development and analysis of the HIRIS flight dewar. This information will be presented in three parts:

1. Dewar design
2. Thermal Analysis
3. Structural analysis

The HIRIS Flight dewar was designed to house a cold (30° K) Idealab Inc. Michaelson interferometer within a Bristol Aerospace Corporation Black Brant V C rocket payload for purposes of auroral measurements in the infrared. In order to accomplish this, a cryogenic dewar was designed to meet the following requirements:

1. Ability to withstand the launch environment of the Black Brant rocket.
2. Cooling to be done by liquid or supercritical helium.
3. A front cover containing a lid capable of being opened and closed in flight with the ability of containing a high vacuum with negligible leakage. The position of the lid opening must be such that it can be used with the HIRIS and SPHIRIS experiments (the latter including a high off-axis rejection telescope with the interferometer).
4. A dewar design which is common for the HIRIS and the Utah State Hademard spectrometer experiments, and capable of being converted to the requirements for the SPHIRIS experiment by substituting longer dewar extensions onto the cryogenic assembly.

Originally it had been decided to use a dewar similar to that used on the HRC Earth Limb Sensor experiment which utilized a trunnion type of cryogenic support. The configuration of the dewar and the support system, however, did not lend itself to the HIRIS requirements. At this juncture two important decisions were made. First, it was decided to develop a dewar based on the Utah State University CVF dewar which was manufactured by Cryogenic Associates of Indianapolis, Indiana. The second decision was to go to a supercritical helium, forced, method of cooling.

1.0 FLIGHT DEWAR DESIGN

The HIRIS dewar (Figure 1) design was based upon the Cryogenic Associates IR104A, a modification of which had been previously purchased for interferometer environmental testing. The outside diameter of the Model 104A flanges is 15.5 inches with the pressure vessel outer diameter being 14 inches. It contains a liquid helium tank in the base which is integral with the inner cold shield. The cold shield is terminated at a flange to which a front extension is bolted. A radiation shield surrounds the cold shield and is terminated in like manner. An exhaust tube from the helium tank is wrapped around the radiation shield for several turns before exiting through the pressure vessel. The pressure vessel is flanged at the base for mounting purposes and at the front for attaching the pressure vessel extension.

A plumbing schematic of the HIRIS dewar showing the cryogen tank, the cold shield, the radiation shield, a fill vent and a normal vent is shown in Figure 2. Also included in the schematic is an absolute pressure valve, set at 3 atmospheres, and a 50-watt heater attached to the normal vent to prevent frosting. The cryogen tank has been sized to contain 10 liters of helium which can be transformed into the supercritical condition by a series of heater wires wrapped around the outside of the tank. Inside the tank is a honeycomb matrix to insure good heat conduction through the gas. Therefore, by controlling the heat flow into the tank, it is possible to vary the flow of the cold gas through the heat exchangers and out the absolute pressure exhaust valve. This, in turn, controls the temperatures of the cryogenic components; namely, the focal plane and the cold shield.

The flight dewar is required to fit within a minimum payload inner diameter of 15.63 inches. Therefore, the maximum flange diameter was limited to 15.0 inches. The pressure vessel diameter also had to be limited, in this case to 14 inches, to allow sufficient room for bolting together the outer flanges of the dewar extensions and for mounting the front cover. Overall length, including the dewar extensions and the front cover mechanism, is 48 inches not including a 6.0-inch deep envelope below the base for fittings and electronics boxes.

The following information was provided to Cryogenic Associates, the dewar vendor:

1. A layout drawing of the dewar showing general dimensions, the cryogenic plumbing and mounting flanges.

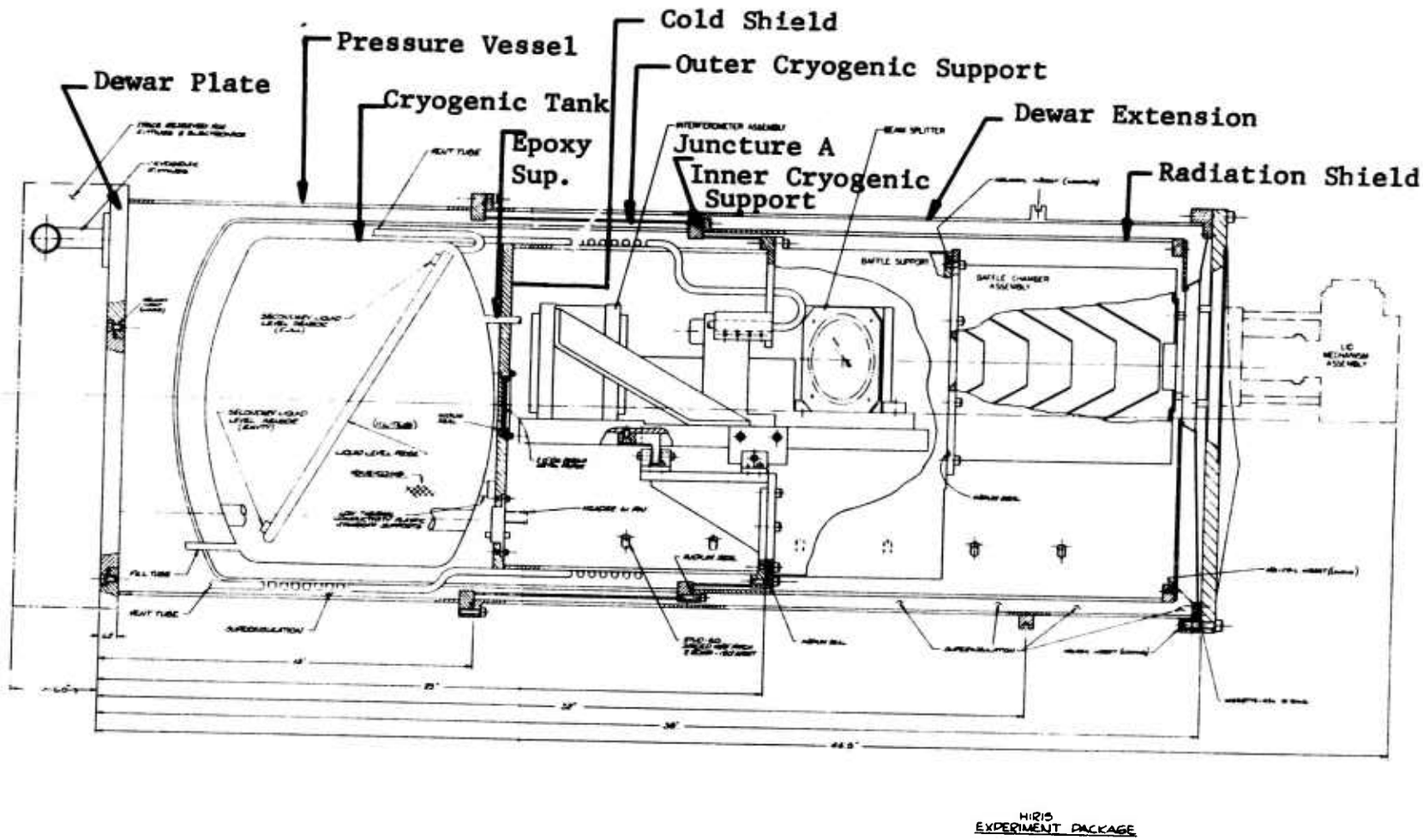
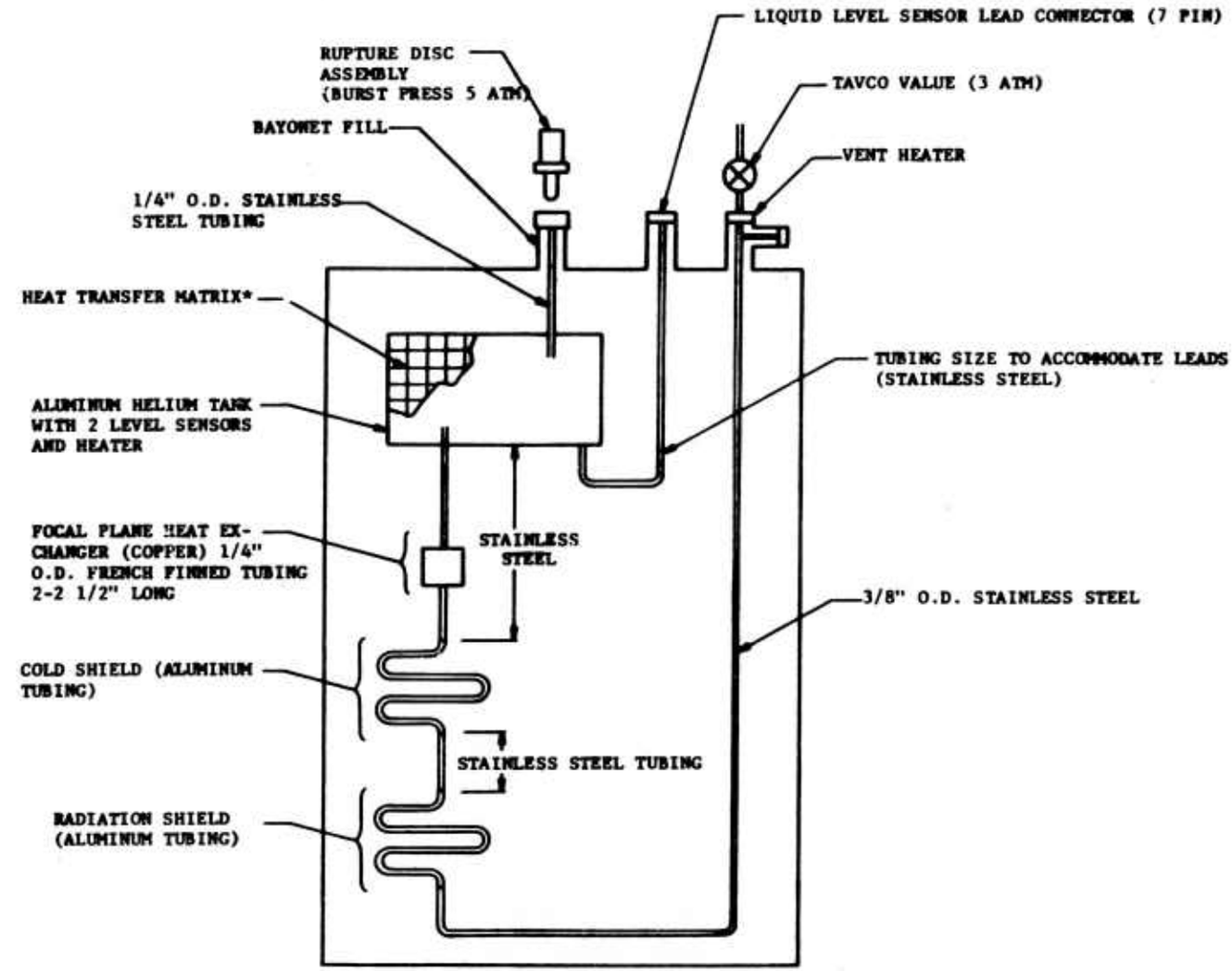


Figure 1 . HIRIS FLIGHT DEWAR



*HEAT TRANSFER MATRIX: ALUMINUM HONEYCOMB TYPE 3003 1/4" CELL .003" FOIL GUAGE HEXCEL CORP. DUBLIN, CALIFORNIA OR EQUIVALENT

Figure 2 HELIUM LINE SCHEMATIC

2. A schematic drawing of the supercritical cryogenic system.

3. A layout of the cruciform payload service module which was to be used for determining the accessibility of the vacuum and cryogenic fittings which are mounted to the base of the dewar.

4. A drawing of the internal electrical feedthrus used in the ELS dewar and proposed for the HIRIS dewar.

A supercritical system was selected rather than a liquid system for the following reasons:

1. Gaseous cryogen is not susceptible to changes in the "g" field.

2. A greater change in enthalpy of the cryogen can be used prior to venting.

3. The flow of cryogen can be controlled by temperature sensors mounted at critical locations which control a heater on the cryogen tank.

A review of the plumbing schematic showed that a separate fill vent was not necessary if the normal vent was increased to 3/8 in. OD tubing although the heat exchanger lines could remain at 1/4 in. OD. The fill vent line remained as shown in the schematic, but is now used solely to bring out the leads from the liquid level sensor and carbon resistor temperature sensors which terminate at a connector mounted to an external flange on the tubing.

The TEE valve on the normal vent line was eliminated leaving a mini-bayonet fitting with a TEE connection to the pressure relief valve.

After filling is completed a cap will be placed on the bayonet connection to detour the flow through the absolute pressure valve. A heater is mounted as close to the pant leg as possible to keep the connection and valve from frosting.

The cleanliness requirements were met by sealing off the areas between the radiation shield and the optical compartment. Vacuum grease from the O-ring grooves is kept from entering the optics compartment with the exception of the O-ring on the front cover of the dewar. In this instance an indium O-ring was used which will not require grease. However, the number of bolts required on the front cover had to be doubled in order to insure an adequate indium seal.

The porous metal filters attached to the back of the dewar optical compartment are to act as dust filters without impeding the ability of the chamber to be pumped down to a high vacuum. Sealing around the edge of each filter is accomplished with an indium washer squeezed between the filter and the cold wall and retained by an aluminum flange piece which will allow the filters to be removed for cleaning.

The cryogen tank is made of formed and welded aluminum sheet 12 inches in diameter to provide a minimum cryogen capacity of 10 liters. It will be proof tested to 6 atmospheres. Fill and exhaust lines are brought out through pant legs on the base and terminated at mini-bayonet fittings which are located in the two upper quadrants of the dewar base. The tank is supported from the optical compartment through an adaptation of standard Cryogenic Associates cryogenic support techniques utilizing four glass epoxy, thin wall cylinder supports, epoxied to deep grooves in the tank and the optical compartment wall.

In order to cool the detector adequately, it is necessary to extend the cooling line close to the detector location and then loop it back to the cold shield with a sufficient length of tubing beyond the detector to insure that conduction from the cold shield wall would not heat up the detector. A means of supporting the tubing without increasing cold losses was devised. Also included is a copper mounting block on the tubing which is used to fasten the copper strap for cooling the detector.

Cryogenic Associate's preliminary dewar design was reviewed by Honeywell and Utah State University on 16 June 1972. The following decisions were made at this meeting.

1. The cryogenic fittings will be mounted next to each other in the horizontal position.

2. All fittings in the base will fit within a maximum diameter of 13.63 inches. The area beyond this diameter was reserved for the payload integrator to bolt and seal the base to the service module of the Black Brant payload.

3. For wiring purposes it is easier to provide a large access plate in the dewar base and to weld tubes into the helium tank for carrying the leads into the optical compartment. This will make it possible for the wiring to be done after the dewar had been built and delivered rather than have the wires permanently installed at the

vendors. Otherwise, wiring changes or broken wires would require that the dewar be sent back to the vendor and the weld broken to gain access to the wires.

At the launch facility it will be necessary to bleed off the helium pressure from 3 atmospheres to 1 atmosphere before the transfer lines can be reconnected in order to refill the cryogen tank prior to attaining readiness for launch. Therefore, a by-pass line with a manual valve was included with the normal exhaust line. This necessitated a change in the piping and a relocation of the absolute pressure relief valve.(APRV).

FRONT COVER

The front cover design (Figure 3) is similar to that which was developed for the HRC Earth Limb Sensor. It consists of a cover for the pressure vessel, a deployable lid and a lid mechanism. The lid is sealed to the front cover by the use of two O-ring seals, a face seal and a conical seal.

Upon command the lid is drawn straight up, a specified distance, to break the seal, and is then rotated 180 degrees out from the front of the dewar. See Figure 4. This actuation is accomplished through the use of a dc torque motor which operates opposing ball screws which cause linkages attached to the ball nuts, and the lid, to move out from the center of the ball screw housing and structure; thus raising the lid (See Figure 5). After the ball nuts have moved approximately 1/3rd of an inch, the outer ball nut forces the latch to unlock. Simultaneously, the inner ball screw has caused a geneva mechanism to be engaged. This action is transmitted through an epicyclic gear train to induce the beam to rotate, carrying the lid away from the front cover opening. Upon reaching the full open position, a limit switch is actuated which shuts off the motor. To close the lid the above sequence is reversed.

2.0 FLIGHT DEWAR THERMAL ANALYSIS

The thermal design criteria for the HIRIS Flight dewar is as follows:

A. Cryogen - Supercritical helium pressurized to 3 atmospheres absolute

B. Operating temperatures
   1. Focal plane 10° K
   2. Optical components & cold shield 25° - 30° K

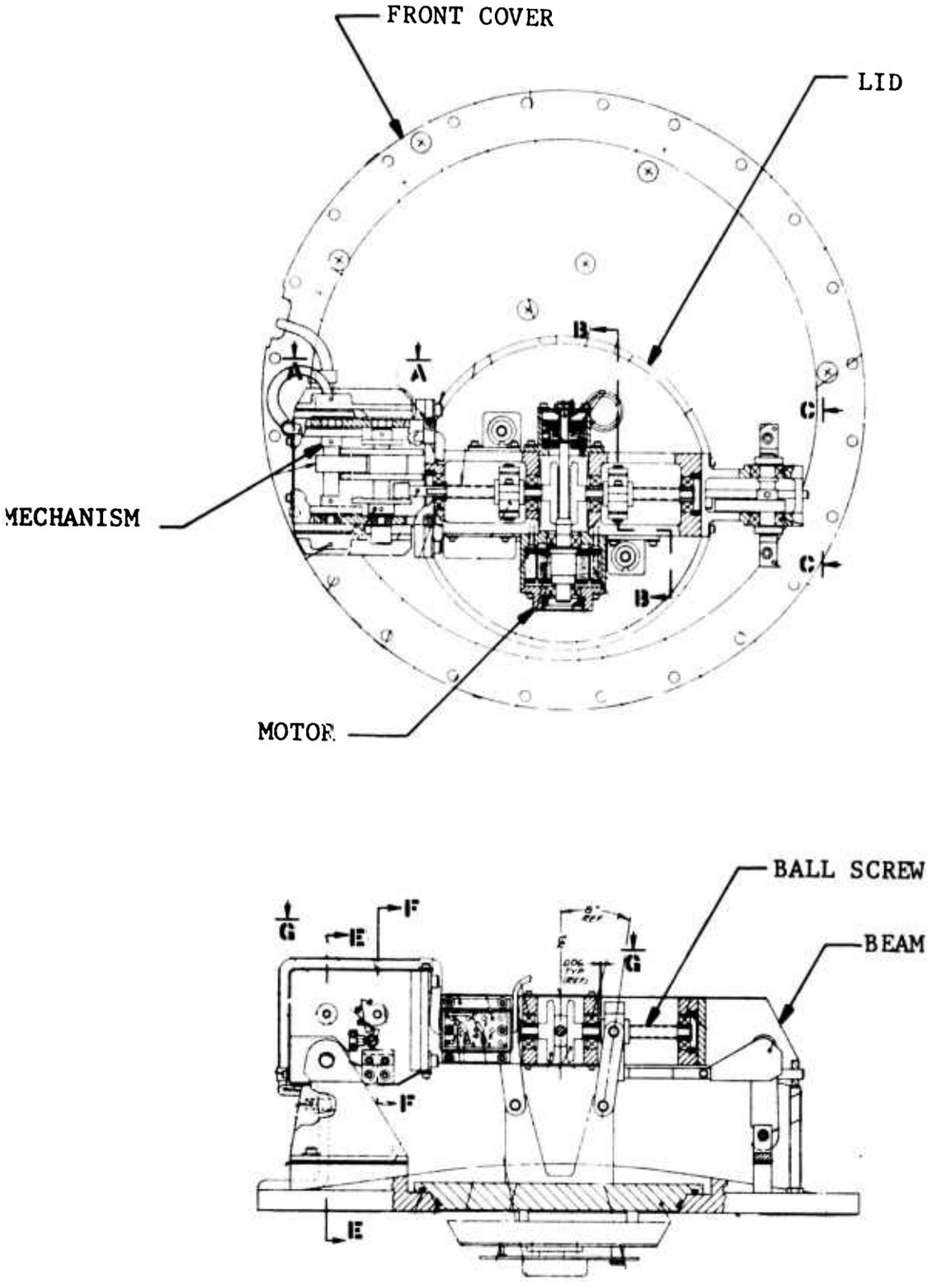


Figure 3 FRONT COVER

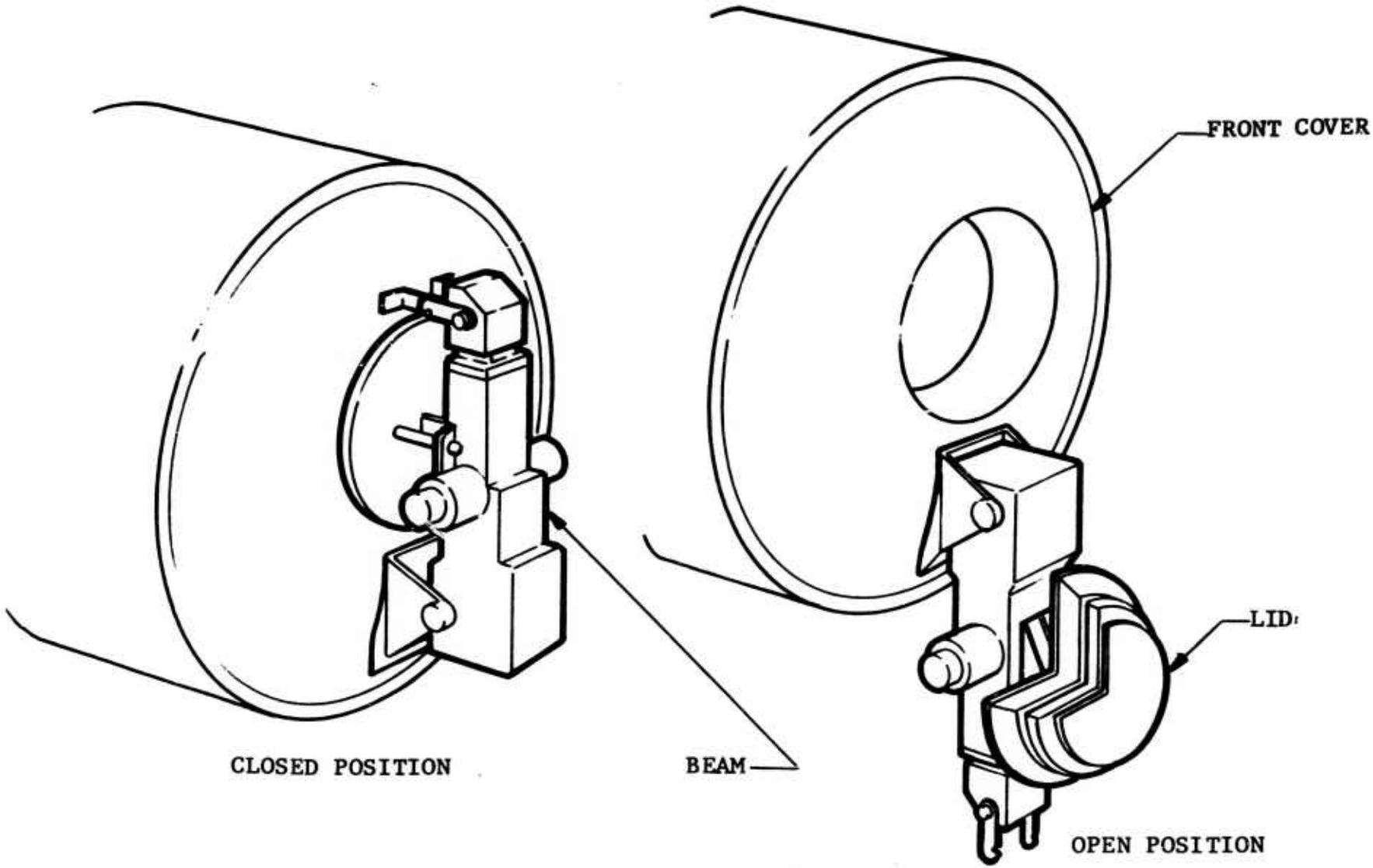


Figure 4 DOOR MECHANISM

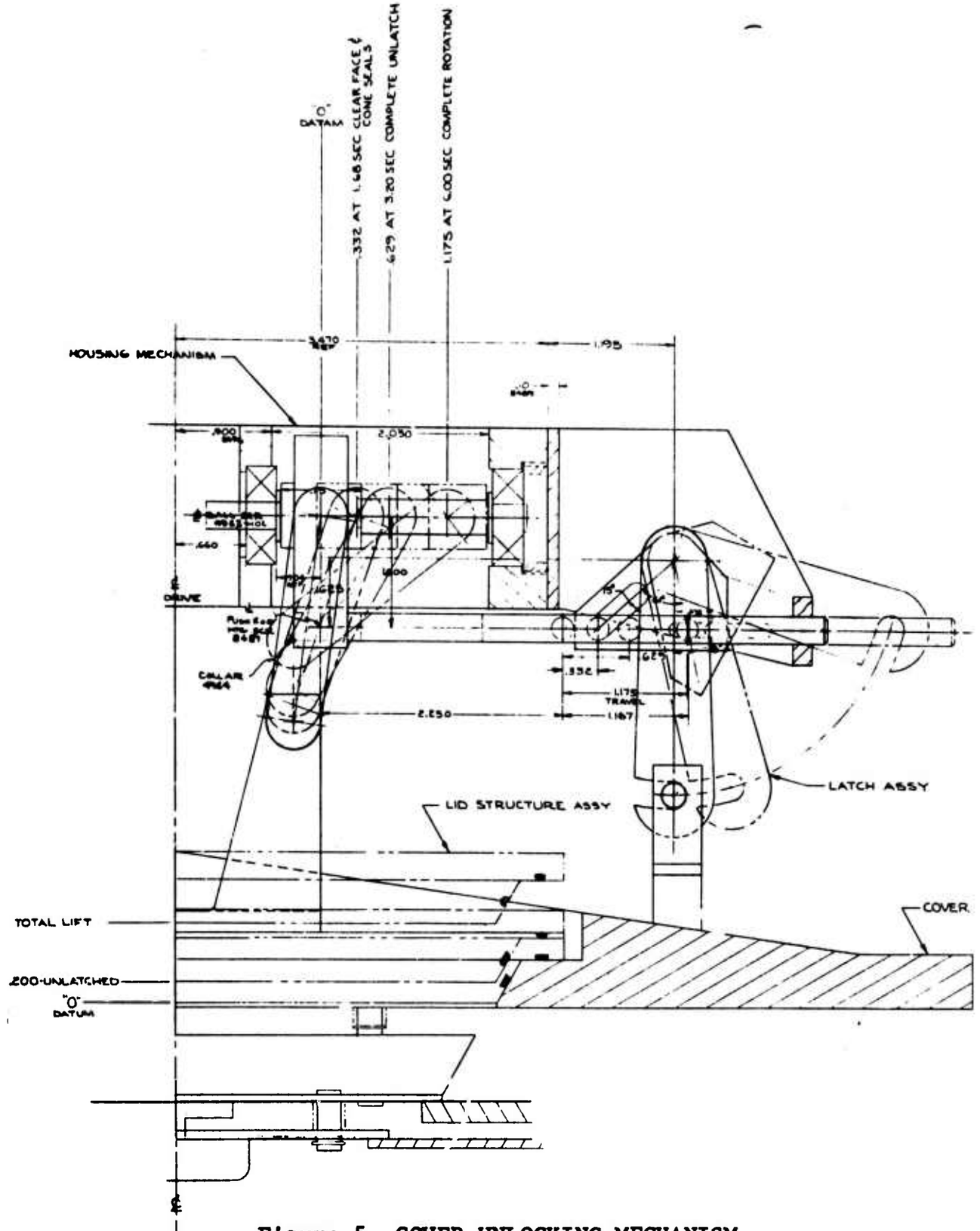


Figure 5 COVER UNLOCKING MECHANISM

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3. Radiation shield 90° - 95° K

C. Operating durations
   1. Hold time 6 hour ground hold
   2. Flight time 6 - 8 minutes

A thermal analysis of the preliminary design of the HIRIS flight dewar has been made. This analysis was performed in order to determine the amount of cryogen (Helium at 3 atm pressure absolute) needed for a six-hour ground hold period plus a 550-second flight period. In addition, the heat loads for the entire dewar, along with operating temperatures and tank and vent heater sizes, were determined in order to provide the necessary information for the final flight design.

The thermal analysis consisted of dividing the flight dewar into isothermal nodes, which represented various parts of the dewar, such as the pressure vessel, the radiation shield, the cold shield, the interferometer, etc. Each node was assigned the proper value of thermal capacitance. These nodes were then thermally tied to each other with the appropriate resistances for the radiation and conduction modes of heat transfer. Where heat sources, such as the calibration and the reference sources exist, these were represented in the model. The refrigeration due to the helium flow through the venting system was also incorporated. The effects of temperature on the various thermal properties were included.

The analysis employed the use of two control loops to maintain the operating temperature of the cold shield and of the radiation shield at their respective temperature ranges of 25-30° K and 90-95° K. Each control loop is set up to monitor the temperature of, for example, the radiation shield, and use this output to determine the amount of energy to be supplied to the tank heater. The control loops are set up to operate in the either/and mode and are expected to do the same in the actual flight dewar.

Results of this analysis for the configuration shown in Figure 1 are presented in the attached tables. Table I presents the heat load summary on all important areas of the flight dewar. Table II presents the flight dewar helium weight breakdown.

The results shown in Table II show that the amount of helium used during a six-hour hold period is 506 grams with 267 grams left for flight. If the hold period were increased to eight hours, then the amount of helium used for the ground hold period is 675 grams with 98 grams left for flight. Previous experience

TABLE I

HIRIS FLIGHT DEWAR HEAT LOAD SUMMARY

	SOURCE		HEAT LOAD (Watts)
1.	RADIATION SHIELD (92° K)		
	A. Penetrations		3.06
	B. Support System		2.89
	C. MLI		2.09
	D. Calibration Sources		2.00
		Total	10.04
2.	COLD SHIELD (20-30° K)		
	A. Penetrations		.014
	B. Radiation		.118
	C. Support System		1.076
		Total	1.208
3.	INTERFEROMETER (20-30° K)		
	A. Cold Plate Support		.069
	B. Radiation		.271
	C. Reference Sources		.600
		Total	0.940
4.	FOCAL PLANE (10° K)		
	A. Support System		.020
	B. Detector Bias		.015
	C. Wires		.010
		Total	0.045
5.	HELIUM TANK (5.5° K)		
	A. Penetrations		.081
	B. Radiation		.087
	C. Support System		.006
	D. Heater		.392
		Total	0.566

TABLE II

HIRIS FLIGHT DEWAR HELIUM WEIGHT BREAKDOWN

			Helium (grams)
a)	Tank Size (10 liters) (100% fill)		1212
b)	For 80% fill		967
c)	16% ullage		194
		NET	773
d)	Ground Hold Requirement (6 hr at 0.0234 gm/s)		506
e)	Subtotal left for flight, etc		267

with dewars, such as the one analyzed, indicates that this amount of helium is adequate.

In addition to the previous results, it was also determined that the helium tank heater size should be 10 watts. This heater will be used to convert the liquid helium to the 3 atm monophase fluid and to provide the necessary refrigerant flow in order to maintain the flight dewar within acceptable temperature limits. The required vent heater size is 50 watts to prevent frosting by the cold helium gas and to guard the TAVCO valve (absolute pressure relief valve) from freezing up.

An analysis was conducted to determine what happens thermally to the baffle plate, blackbody and blackbody plate when the HIRIS dewar door opens to take flight data. The two areas of concern are: what happens to the baffle plate after the door opens and how long does it take to cool down the baffle plate to a temperature of 30° K after the door closes?

A transient thermal analysis was performed in order to answer the above questions. The analysis considered the following assumptions:

1. Blackbody and light emitting diode (LED) are turned off at the time the door begins to open.
2. The blackbody and LED are not turned on until 10 seconds after the door is closed.

The analysis considered the changes of thermal material properties with temperature, namely specific heat and thermal resistance. Primary heat sources applied to the two plates are:

1. The rocket skin and pressure used are at 350° K.
2. Earth emission at a flux of 0.0209 W/cm^2.
3. The blackbody initially at 200° K.

Heating by aerodynamics viscous forces, by aurora emission and gas condensation were not considered in this analysis.

Results of this analysis are presented in Table III below. The analysis showed that the baffle plate, which returned to 30° K within 3 seconds and to 20° K within 5 seconds, had met the 10-second time limit. Temperature results and times for the radiation shield plate and blackbody are also presented.

TABLE III

COMPONENT	DURING 315 s Door Open Period		AFTER DOOR CLOSES	
	Initial Temp (°K)	Final Temp (°K)	Initial Temp (°K)	Time (s)
Radiation Shield Plate	92	102	92	20
Baffle Plate	20	52	20	5
Blackbody	200	174	173	20

3.0 DEWAR STRESS ANALYSIS

3.1 Description of Structure

The dewar is of welded construction, fabricated from an aluminum alloy (6061-T6) which is heat treated to a T-62 condition. The dewar assembly weighs approximately 58 lb, is 44.5 inches long with front cover, and has a maximum flange diameter of 15 inches. Figure 1 shows the primary elements of the flight dewar and its three separate assemblies; namely, a) the cryogenic assembly, b) the dewar extensions and c) the front cover. This configuration will be mounted in a Black Brant VC Rocket probe and must be capable of surviving the environmental conditons encountered during the rocket flight.

The primary structural components within the cryogenic assembly are the inner and outer cryogenic supports, the radiation shield, and the cryogenic tank and its mounting to the cold shield.

The cryogenic tank was designed to contain 11 liters of liquid helium and is pressurized to 3 atmospheres. It is attached to the cold shield by four bonded glass epoxy supports.

A pressure vessel extension is provided, which, when attached to the cryogenic assembly, extends the dewar length to 38 inches prior to mounting the front cover. Attached to the top of the pressure vessel extension is a shallow conical shell which supports the front cover and seals the pressure vessel.

Provisions have been made to attach the interferometer either at the cold shield or ring juncture, both of which are connected to the inner cryogenic support. The enclosed analysis investigates the latter case.

The inner cryogenic support is made from a low thermal conductivity material (glass epoxy) and connects the optical compartment to the radiation shield which is fastened to the outer cryogenic support (also glass epoxy) at a ring or flange juncture. The The connection of the inner and outer glass epoxy shells to the aluminum ring is accomplished by employing an epoxy bonding agent.

This joint or juncture received considerable analytical attention because it was expected that the eccentricity of load path inherent in the design would a) appreciably influence the total dynamic response of the structural system, and b) induce local stresses in the edge zones of the attached shells. Also of interest analytically was the front cover plate and assembly.

Structurally (except for local discontinuities) the system is statically determinant consisting of telescopic cantilever beams in series fixed at the dewar plate. Each beam is a thin cylindrical shell flanged at either end.

Dynamic loads arising within the front cover assembly are carried by the pressure vessel extension which is attached to the main pressure vessel supported by the dewar plate.

Loads arising dynamically in the optical compartment are transferred either to the cold shield or ring juncture (A) (option) thence into the inner cryogenic support, over to the outer cryogenic support and into the pressure vessel which is supported by the dewar plate.

The dynamic effects of the cryogenic tank are transferred to the cold shield and then follow the identical path cited above for optical compartment loads.

The upper and lower radiation shields are jointly supported at ring juncture (A) and transfer their dynamic loads to said juncture thence into the outer cryogenic shell over to the pressure vessel and into the dewar plate.

The aluminum pressure vessel, which must support a differential pressure of one atmosphere, and dewar base provide the final links in the primary load path for the optical bench.

Note that a ring or flange is provided at each transfer station to alleviate the effects of eccentric loading resulting from attaching shells of varying radii (telescoping).

In addition to dynamic loads, thermal loads and stresses will arise at each ring juncture since the thermal strains at 20° K are not compatible for aluminum and glass epoxy. (The inner and outer cryogenic supports are made of glass epoxy).

3.2 ANALYTICAL APPROACH

The primary function of the analysis was to adequately predict the dynamic behavior of the dewar assembly resulting from the random excitations imposed during the rocket flight, and to qualitatively determine its probability of acceptable performance.

The primary structural tool utilized to evaluate the total dynamic performance of the structural assembly was the Stardyne Program, which is based on the finite element technique. The program was developed by Mechanics Research Inc. of Los Angeles, California and is available at all Control Data Corp. and Cybernet Data Centers.

When utilizing any program based on the finite element technique, the key to the accuracy of the predicted response lies in the adequacy of the structural model chosen by the analyst to realistically represent the physical system. For the dewar assembly under consideration it was apparent that the built-in eccentricities, inherent in the telescoping cryogenic design, could appreciably influence the total behavior of the physical system.

In addition, "local" shell stresses could arise at each ring juncture. Hence, an appropriate structural model would have to account for these local effects. Two approaches were possible: a) A complex finite element model utilizing many elements and nodes which would be expensive, somewhat unwieldy, and not necessarily as accurate with respect to local stress conditions as b) a simplified structural model coupled with an analytical technique to account for local effects. The latter approach was chosen because it involved less computer time without sacrificing accuracy in the determination of lower frequency modes and local stress conditions. To accomplish this a separate theoretical investigation was undertaken which resulted in the development of two small computer programs called ARA and ASSA.

Of primary importance in the analysis was the determination of the maximum expected stresses resulting from the random excitations encountered during the rocket flight. In addition, the structural assembly is also expected to meet all loading environments listed in Table IV.

Because bulkheads and rings are provided at the ends of each short cylindrical shell, all "shell modes" (variations with respect to the circumferential coordinate, θ) were neglected.

The structural system was, therefore, idealized as a series of telescoping beams interconnected by springs (equivalent beams) located at each ring juncture. The stiffness of each spring was determined utilizing program ARA, which also computed maximum "local shell stress" resulting from lower mode (beam bending) configurations. Thus, the Stardyne model was simplified to an 11 and 33-degree of freedom system.

After the structural model shown in Figure 7 was finalized, a modal extraction analysis was performed utilizing the STAR option of the Stardyne system. Note that the inertia effects of the interferometer assembly, the cryogenic tank, and front cover assembly were accounted for in the analysis through the use of masses lumped at their respective locations.

The STAR Program lumps distributed masses internally. The output (first five modes) of the modal extraction analysis is given in Table V.

The specified shock spectra (a 20-g sawtoothed cut-off at 0.019 seconds) was then input utilizing the Dynre 1 option of the Stardyne program. As expected, a maximum acceleration of 40 g's was computed at a few nodes. The results of this analysis are given in Table VI.

A separate 20-g axisymmetric shell stress analysis was also generated utilizing program ASSA to determine local shell stress at ring junctures. The results of this analysis appear in Table VII.

To investigate the expected excitation of the structural assembly encountered during the rocket flight; a random vibration analysis was performed, utilizing the Dynre 3 option of the Stardyne program and the specified power spectral density curve.

Since the results of a random vibration analysis can be appreciably affected by the percentage of critical damping inherent in

TABLE IV

HIRIS DEWAR ENVIRONMENTAL REQUIREMENTS

A. SINUSOIDAL VIBRATION - 3 AXES, 4 OCTAVES/MIN

I. QUALIFICATION LEVEL (warm, evacuated)
0.1 D.A. 15-31 Hz
5.0 g (0-peak) 31-2000 Hz

II. PREFLIGHT LEVEL (cold, evacuated)
0.06 D.A. 15-31Hz
3.0 g (0-peak) 31-2000 Hz

B. RANDOM VIBRATION - 3 AXES

I. QUALIFICATION LEVEL (warm, evacuated)
7.75 g (rms) 1 minute/axis

II. PREFLIGHT LEVEL (cold, evacuated)
6.5 g (rms) 1/2 minute/axis

C. SHOCK - 3 AXES

TERMINAL PEAKED SAWTOOTH - 20 g PEAK
11 MILLISECOND DURATION

D. ACCELERATION - 30 SECOND DURATION

I. LONGITUDINAL - 15 g

II. LATERAL (2 axes) - 5 g

TABLE V

HIRIS DEWAR VIBRATION ANALYSIS

MODE	TYPE	FREQUENCY	MAX. DISPLACEMENT
1	Bending	60 Hz	Front-Rad. Shield
2	Bending	96	Rear-Rad. Shield
3	Bending	141	Front Cover
4	Bending	239	Helium Tank
5	Axial	259	Helium Tank

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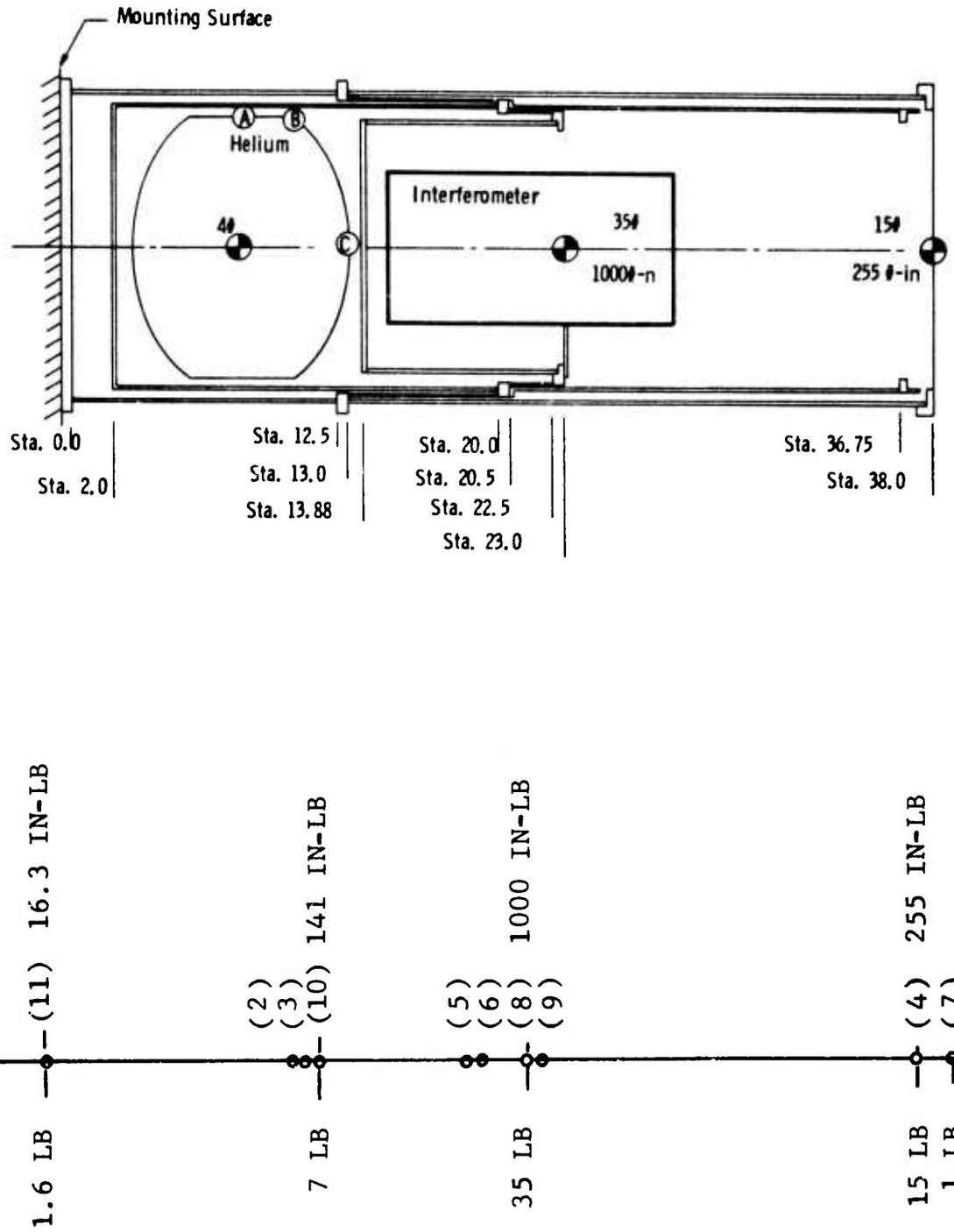

Figure 7 STRUCTURAL MODEL WITH LUMPED WEIGHTS AND WEIGHT INERTIAS

TABLE VI (a)

DYNAMIC SHOCK RESPONSE (0.5% CRITICAL DAMPING)

NODE	AXIAL 20 g SHOCK			LATERAL RANDOM VIBRATION		
	DISPLACEMENT	VELOCITY	ACCEL. (g)	DISPLACEMENT	VELOCITY	ACCEL. (g)
2	0.312×10^{-3}	0.726	6.55	0.387×10^{-2}	1.98	20.44
3	0.671×10^{-3}	1.558	13.91	0.637×10^{-2}	3.18	20.67
4	0.890×10^{-3}	2.261	21.92	0.535×10^{-1}	24.90	25.90
5	0.148×10^{-2}	2.937	19.84	0.239×10^{-1}	9.21	22.07
6	0.174×10^{-2}	3.53	21.61	0.264×10^{-1}	9.86	22.20
7	0.177×10^{-2}	3.57	23.32	0.711×10^{-1}	32.30	40.00
8	0.193×10^{-2}	4.04	22.12	0.323×10^{-1}	11.80	22.64
9	0.203×10^{-2}	4.28	25.54	0.340×10^{-1}	12.00	22.82
10	0.205×10^{-2}	4.33	26.29	0.136×10^{-1}	9.68	22.38

TABLE VI (b)

DYNAMIC RANDOM RESPONSE (0.5% CRITICAL DAMPING)

NODE	AXIAL 20 g SHOCK			LATERAL RANDOM VIBRATION		
	DISPLACEMENT	VELOCITY	ACCEL. (g)	DISPLACEMENT	VELOCITY	ACCEL. (g)
2	6.19×10^{-4}	1.11	7.21	2.05×10^{-3}	1.62	12.53
3	1.33×10^{-3}	2.40	15.38	3.61×10^{-3}	2.77	20.45
4	1.49×10^{-3}	3.19	27.35	1.58×10^{-2}	9.61	15.89
5	3.84×10^{-3}	6.27	26.67	9.46×10^{-3}	5.71	10.14
6	4.65×10^{-3}	7.60	32.14	1.04×10^{-2}	6.30	10.43
7	4.70×10^{-3}		32.51	2.07×10^{-2}	12.30	20.50
8	5.21×10^{-3}	8.52	36.14	8.03×10^{-3}	4.86	8.40
9	5.50×10^{-3}	9.00	38.39	7.99×10^{-3}	4.83	8.56
10	5.58×10^{-3}	9.12	38.96	2.94×10^{-2}	18.00	29.59
11	4.73×10^{-3}	1.72	32.66	4.43×10^{-2}	26.80	42.79

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TABLE VII

HIRIS DEWAR STRESS ANALYSIS
(0.5 PERCENT CRITICAL DAMPING)

JT	Station	Material	Thermal		Ther. + 20g's Axial		Random Vibration: Ther. + 2σ* Axial		Random Vibration: Therm. + 2σ * Lateral		
			σ_x	σ_θ	σ_x	σ_θ	σ_x	σ_θ	σ_x	σ_θ	τ
1	0 + 00	ALUM			366		1140		1618		574
2	0 + 12.5	ALUM	1454	347	3166	347	8834	347	23118	347	574
3	0 + 13.0	PLAST	12894	7310	13648	7310	15828	7310	18250	7310	206
3	0 + 13.0	ALUM	2716	347	4153	347	9136	347	23690	347	240
5	0 + 20.0	PLAST	11502	6310	12287	6310	14436	6310	14788	6310	206
5	0 + 20.0	ALUM	608	475	2218	475	7210	475	13118	475	200
6	0 + 20.5	PLAST	12805	7077	13474	7077	15387	7077	15819	7077	320
6	0 + 20.5	ALUM	1118	475	2723	475	7694	475	13424	475	78
8	0 + 23.0	PLAST	10730	6516	11508	6516	12510	6516	11852	6516	320
8	0 + 23.0	ALUM	2907	1978	5360	1978	5317	1978	6327	1978	224

* 4% CHANCE OF EXCEEDING 2σ VALUES

ROOM TEMPERATURE MECHANICAL PROPERTIES

MATERIAL	STRESS ALLOWABLES			MOD. OF ELASTICITY	
	Fty	Fcy	Fsu	Ex	E
ALUMINUM (6061-T62)	36000	35000	27000	10×10^6	10×10^6
GLASS EPOXY (G10)	50000	50000	27000	2.5×10^6	2.4×10^6

the structure, the choice of this parameter is significant.

However, without sufficient test data at cryogenic temperature, the proper choice of this important variable is somewhat impractical. Thus, for the purpose of an initial investigation, an overly conservative and perhaps somewhat unrealistic estimate of 0.5 percent critical damping was used in the analysis. Fortunately, the structural system using 0.5 percent critical damping, as is shown in Table VII, proved to be capable of sustaining the specified power spectral density (PSD) input.

Because the random vibration response was far more severe than the specified shock spectra, maximum combined thermal and dynamic stresses are only reported for the random condition. Since the PSD input is a vector which can be applied in any direction, stresses are reported for both an axial and lateral input in Table VII.

3.3 PROGRAM ARA (Antisymmetric Ring Analysis)

The primary load path in the dewar consists of a series of cylindrical shells, of differing radii, interconnected by rings. Inherent in the dewar construction, therefore, are eccentricities which may or may not effect the total behavior of the structural system, depending upon the stiffness of the rings.

Program ARA deals with the antisymmetric behavior of a juncture ring due to an applied moment. The ring is treated as a circular plate having an inner radius (a), and an outer radius (b); and loaded along its inner edge by a line load q $\frac{lb}{in.}$ which varies sinusoidally from $0 = 0°$ to $0 = \frac{\pi}{2}$.

The line load q, arises from the internal dynamic moment which exists at a ring juncture, and may be determined from beam theory.

3.4 PROGRAM ASSA - AXISYMMETRIC SHELL STRESS ANALYSIS

At a typical ring juncture in the flight dewar, shells of differing radii and material are joined. Hence, at cryogenic temperatures a thermal strain differential exists which gives rise to local axisymmetric discontinuity shell stresses. In addition to these thermal stresses, axisymmetric shell stresses may arise (because of the built-in eccentricities inherent in the dewar design) from any axisymmetric loading condition, such as axial shock or random vibration. These stresses are local, generally

restricted to an edge zone and exponentially dissipate away from that zone. Local stresses resulting from shock and vibration can be controlled through the use of "rigid rings". Thermal stresses, however, are more difficult to control. In either case, the magnitude of these stresses is very sensitive to the relative flexibilities existing at that joint.

Program ASSA was written for the purpose of determining the stress condition existing at a ring juncture due to an axisymmetric loading. The program is capable of solving a juncture consisting of up to four shells of varying material and geometry.

In addition to computing edge stresses, the program determines the "beam equivalent" extensional stiffness of the juncture to be used in the Stardyne model; thus accounting for the effect of ring rotation on axial flexibility and natural frequency.

3.5 STABILITY ANALYSIS OF PRESSURE VESSEL

The pressure vessel is a cylindrical shell fabricated from 6061 aluminum heat treated to a T-6 condition. It is approximately 45" long, has an outside pressure vessel diameter of 14" and a 1/8" wall thickness. Prior to launch the pressure vessel must sustain an external hydrostatic pressure of 1 atmosphere without buckling. It was found that the classical critical hydrostatic buckling pressure of the vessel is 3.75 atmospheres. Considering the conservatism employed in the analysis (effect of mid-span rings neglected), the safety margin of the vessel against buckling is quite high even if small imperfections exist in the cylindrical shell.

3.6 CRYOGENIC TANK ANALYSIS

The cryogenic tank was designed to operate at three atmospheres internal pressure and must sustain a test pressure of five atmospheres. It consists of a short cylindrical shell attached to a spherical cap by a small toroidal section as shown in Figure 8.

The analysis of the cryogenic tank was performed utilizing the MARC program which is available at Control Data Corporation. MARC-CDC is a general purpose finite-element program designed primarily for non-linear analysis of structures with large displacements. The program can effectively be used, however, for linear analysis.

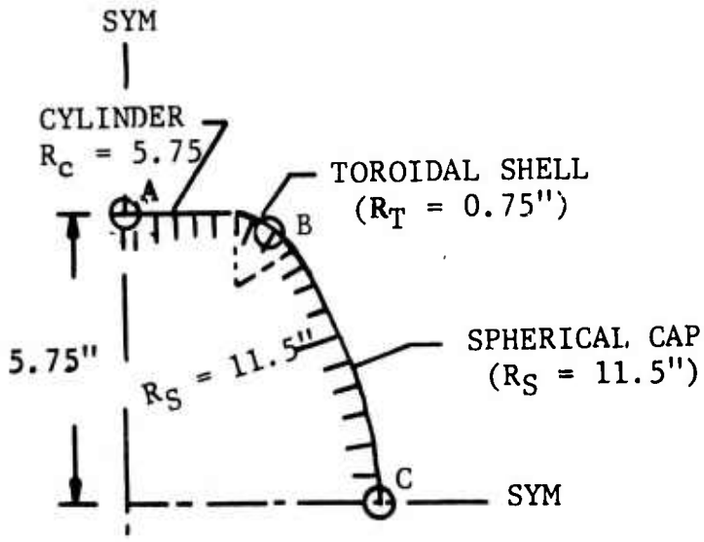


Figure 8 STRUCTURAL MODEL

A basic two-node axisymmetric shell element was used to model the cryogenic tank. The structural model is shown in Figure 8. The maximum stresses computed for an internal pressure of 5 atmospheres and their respective locations are listed in Table VIII, which shows that the stresses are well below the yield stress of the tank material, 6061-T6 aluminum alloy.

3.7 FRONT COVER ASSEMBLY

The front cover assembly consists of three basic sections:

1) Main Cover
2) Lid Assembly
3) Lifting Mechanism

The main cover is a conical shell structure which is bolted to the dewar and provides the primary seal of the front end. The door assembly is attached to the main cover and is automatically controlled to open and close the front aperture at the required times during the flight interval. This is accomplished utilizing the lifting mechanism which breaks the front seal and then swings the door out of the line-of-sight. The sequence is performed in reverse order when resealing the front door.

At launch the interior of the dewar is under vacuum conditions which is the worst stress design condition. Initially, a flat plate was considered because of the ease of fabrication and the fact that weight was not a factor. The maximum stress was found to be in the order of 10,000 lb/in.^{2} which is acceptable for this particular application. However, review of the deflections around the door opening indicated that the out-of-flat condition would not be acceptable to insure proper "O" ring function. The internal vacuum must be maintained while the unit is in a launch state.

A shell type of structure was then considered as a possible means of meeting the deflection requirements without requiring an excessively thick structure. The geometry limitations of the overall package are such as to permit only a shallow shell. The configuration allowed is not a particularly good shell type since the stresses are greatly influenced by bending which can approach that of a flat plate. Within the limitations provided, a conical shell was analyzed using the EASE computer program. For a 1/2-inch thick shell under a 1-atmosphere pressure the results are:

TABLE VIII

HIRIS DEWAR
MISCELLANEOUS STRESS SUMMARY

Item	Material	Location	Condition	Maximum Stresses σ_x	σ_θ	Buckling Allow
CRYOGENIC TANK	ALUM (6061-T6)	A	5 ATM	+ 2520	+4320	N/A
CRYOGENIC TANK	ALUM (6061-T6)	B	5 ATM	+12300	-8100	N/A
CRYOGENIC TANK	ALUM (6061-T6)	C	5 ATM	+ 3520	+3520	N/A
PRESSURE VESSEL	ALUM (6061-T6)		1 ATM	565	1130	3.75 ATM

1) Maximum out-of-flatness of "O" ring support is 0.0043 in.

2) Maximum stress values

tensile = 3360 lb/in.^{2}

compressive = 2740 lb/in.^{2}

A further analysis was made combining the front cover, the door, and the lifting mechanism into one model. The loading consisted of a one atmosphere pressure on the cover (less the door opening) and on the door as suspended from the lifting mechanism. The door and the cover were assumed to be independent structures in the analysis. The results indicate that the lifting mechanism is structurally sound and that the door as connected to the lifting mechanism is more flexible than the shell structure. This means that atmospheric pressure would force the door against the "O"-Ring seal and further insure against a leak developing.

The results of this analysis are:

1) Maximum bending stress in door ..... 3898 lb/in.^{2}

2) Maximum shear stress in door..... 1118 lb/in.^{2}

3) Maximum bending stress in lifting mechanism..... 2123 lb/in.^{2}

4) Maximum shear stress in lifting mechanism..... 1575 lb/in.^{2}

3.8 CONCLUSIONS

Based on the results of the stress and dynamic analysis contained herein, no structural damage is expected for any primary structural component of the flight dewar when subjected to the environmental requirements listed in Table IV.

It is recommended, however, that to insure adequate performance of the structural system, a bumper system should be introduced between the cryogenic tank, the radiation shield and the dewar base plate to minimize peak vibrational amplitudes at these locations. (Random vibration analysis indicates maximum acceleration of 42 g's occurs at Mode 11).

APPENDIX D

ELECTRONIC PRELIMINARY DESIGN REPORT

PRELIMINARY DESIGN OF A FLIGHT INTERFEROMETER DATA PROCESSING SYSTEM

Honeywell Radiation Center
2 Forbes Road
Lexington, Massachusetts 02173

Contract No. F19628-72-C-0325

Project No. FY71217203351

Task No. 0001 AB

Design Report No. 2

Scientific Report No. HRC 73-28

September 1973

Contract Monitor: Dean Kimball, OPR

Prepared
for

AIR FORCE CAMBRIDGE RESEARCH LABORATORIES
AIR FORCE SYSTEMS COMMAND
UNITED STATES AIR FORCE
BEDFORD, MASSACHUSETTS 01730

ABSTRACT

The preliminary design and specifications for a flight interferometer data processing system is described. Included are the AC and DC amplifiers, gain switching logic, PCM encoder, housekeeping commutator and elements of the ground station involved in go no-go decision making.

The following scientific personnel participated in this effort:

HONEYWELL RADIATION CENTER:

Harold W. Robinson, Jr. - Program Manager
Carl R. Bohne - Project Engineer
Lloyd Harkless
Elton Dunbar
Kenneth Lang

VECTOR:

Henry Kaplan
John McManus
Demir Hakimoglu

TABLE OF CONTENTS

SECTION 1

INTRODUCTION

This report describes the design, development and test of the Signal Processing Electronics units for the High Resolution Interferometer Spectrometer (HIRIS) flight system. This system consists of a liquid helium cooled interferometer spectrometer to be flown on a Black Brant VC sounding rocket for the purpose of measuring enhanced atmospheric emissions in the 5-22 micron spectral interval during periods of auroral activity.

Specifically, the elements of the electronic system include the signal processor, pulse code modulation encoder and housekeeping commutator. Following this is a short description of the PCM decommutator and the prelaunch decision processing. The signal processor is required to amplify and filter the signal from the interferometer detector-TIA to levels suitable for both FM/FM and PCM telemetry. The signal processor is required to be linear over a design detector dynamic range of 20,000:1.

The PCM encoder is required to digitally encode analog interferometer data and housekeeping data; then multiplex it with synchronizing codes, housekeeping channel identification codes, interferometer sweep identification codes, idling codes and status bits into a continuous serial bit stream.

The housekeeping commutator sequentially samples conditioned signals from 64 sensors of various types and connects them to the housekeeping input of the PCM encoder. A 6-bit binary channel identification code is developed in the commutator and is also connected to the PCM encoder to permit selection and identification of data from each sensor.

SECTION 2

REQUIREMENTS

2.1 ELECTRICAL

The signal processor, PCM encoder and housekeeping commutator are part of an instrument payload to be launched on a high-altitude research rocket. Figure 2.1 is a block diagram showing the interconnection of these three units and the input/output signal specifications.

2.2 ENVIRONMENTAL SPECIFICATIONS

ER-69538 "Environmental Specifications for Black Brant Payloads and Instrumentation", dated 25 March 1971, by Bristol Aerospace Limited, describes the environmental conditions which the signal processing electronics will experience. Briefly, the entire instrument payload is required to operate to full performance standards under any combination of the following:

Temperature:	0°C to 60°C operating -50°C to 60°C storage
Vibration:	a) 7.5g peak 2000 to 27 Hz b) 0.2 inch double amplitude displacement for 27 to 15 Hz c) A 115 per second logarithmic sweep in any axis, starting at the high-frequency end and having no dwell time during the sweep.
Spin:	5 rps, 8 inch radius for 16 minutes
Altitude:	Sea level to 250 kilometers
Acceleration:	50g for one minute, any axis

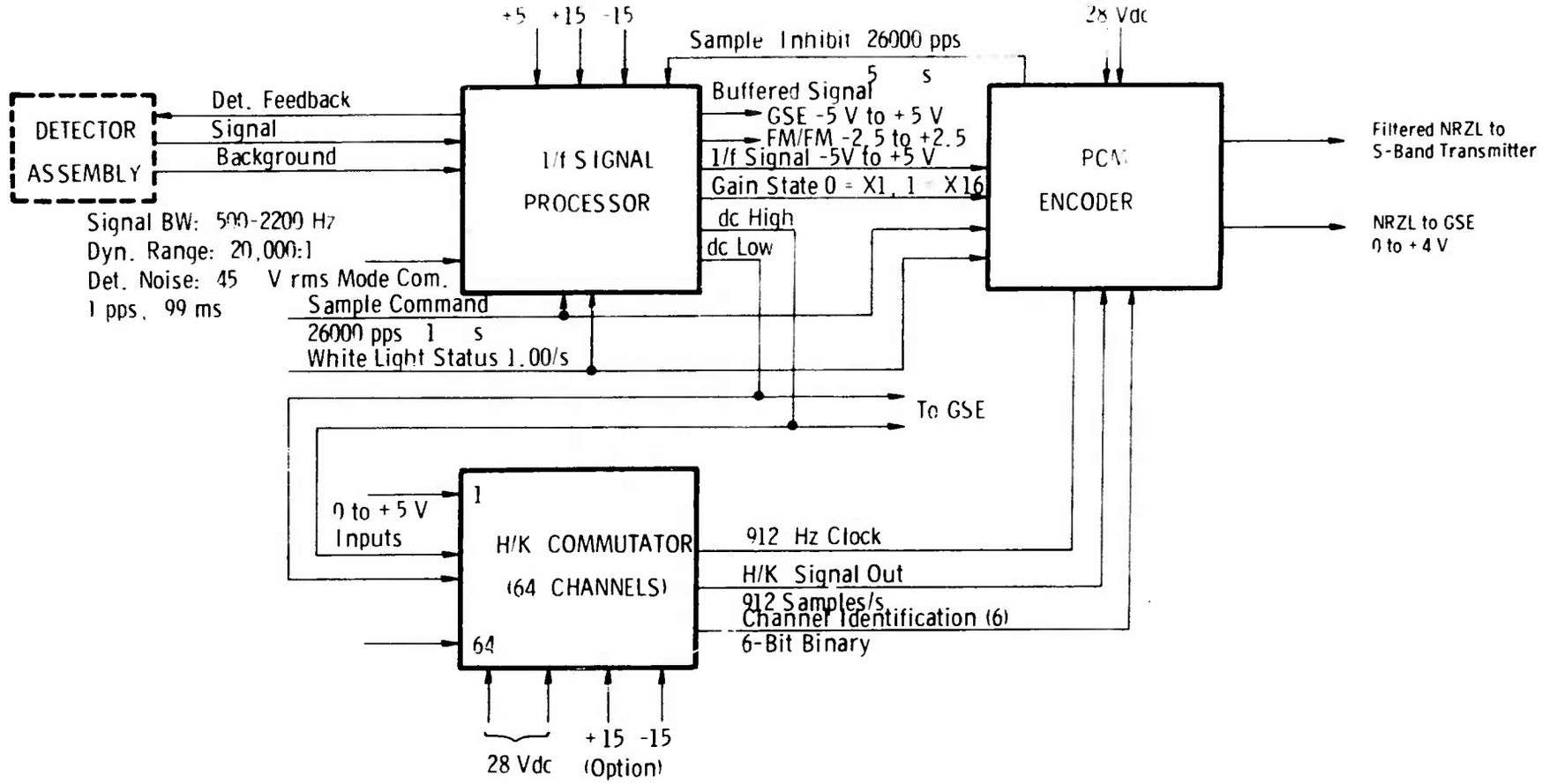


Figure 2.1 INTERCONNECTION DIAGRAM

2.3 MECHANICAL

The mechanical requirements on these units are dictated by the configuration of the payload and experiment. It is impossible to operate any of the electronics at the cryogenic temperatures inside the dewar, but it is highly desirable to locate them as close to the dewar as possible in order to minimize cable lengths. The selected design located the electronic modules in a service module adjacent to the dewar where they plug into the cable harness and attach to the frame of the service module with machine screws.

SECTION 3

INTERFEROMETER SIGNAL PROCESSOR

The Interferometer Signal Processing Electronics board performs the following functions:

1. Interfaces with the infrared detector electronics in the dewar.

2. Amplifies the interferometer signal with minimum phase shift in the signal passband.

3. Provides a gain-switched output to the PCM encoder.

4. Provides a fixed-gain analog signal output to ground support equipment and the FM/FM telemetry system.

5. Provides control logic for the gain-switched output.

6. Provides the d-c component of the interferometer signal to two housekeeping data channels.

7. Provides a logic level to the PCM encoder indicating the switched amplifier gain state.

3.1 REQUIREMENTS

Figure 3.1 is a block diagram of the interferometer signal processing electronics. It can be partitioned into three functional units: the dc amplifier, the ac amplifier and the gain-switching control logic. The requirements are listed in Tables 3.1, 3.2 and 3.3, respectively.

TABLE 3.1

DC Amplifier Requirements

First Stage Gain	-4.0
First Stage Output Amplitude.....	0 to +5V
Second Stage Gain.....	128
Second Stage Output Amplitude.....	0 to +5V
Power Supply Voltages.....	+15, -15V

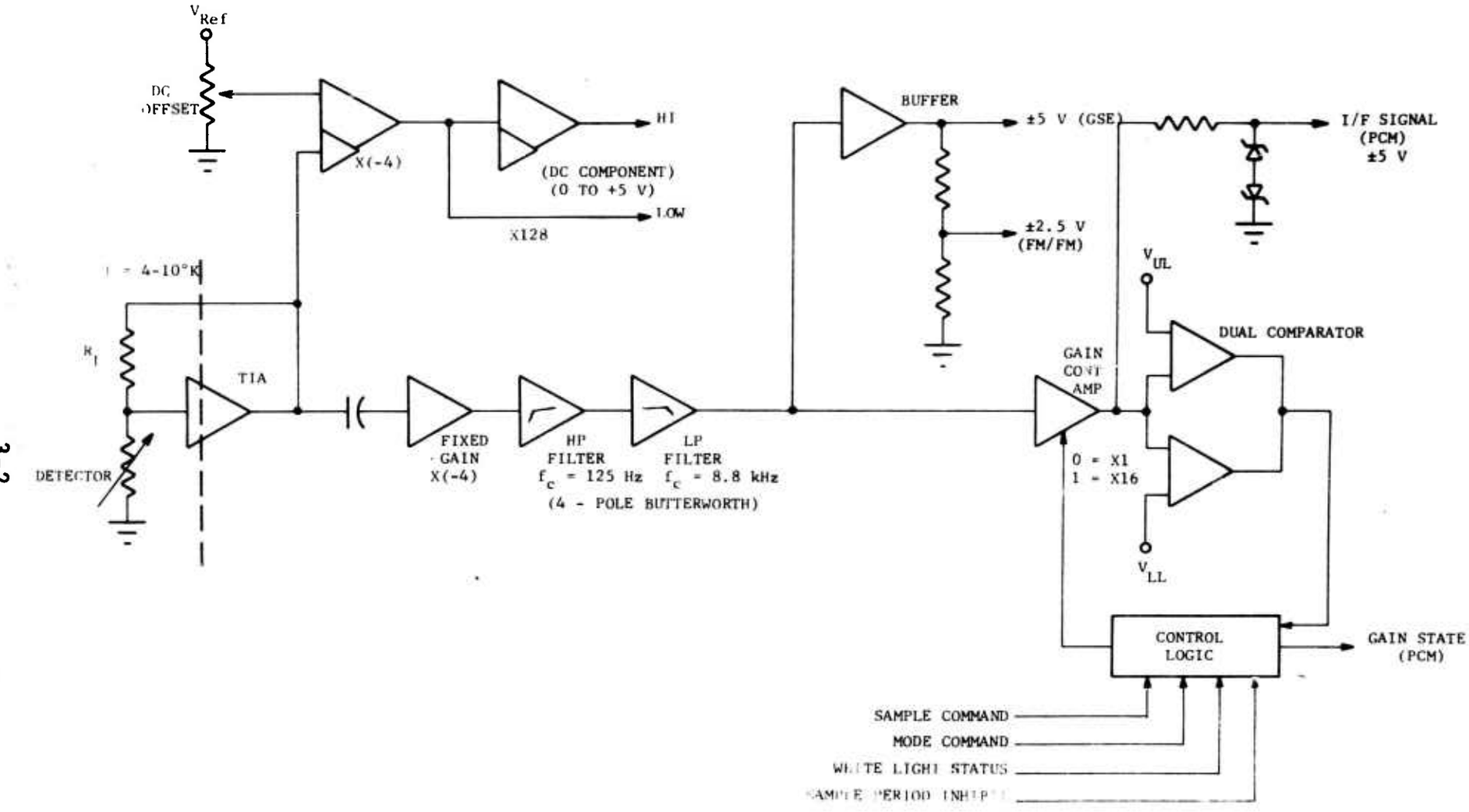


Figure 3.1 I/F SIGNAL PROCESSING ELECTRONICS BLOCK DIAGRAM

TABLE 3.2

AC Amplifier Requirements

Fixed Stage Gain.....	-4.0
Fixed Stage Bandwidth.....	125 to 8800 Hz
Fixed Stage Filter types.....	4-pole Butterworth
Fixed Stage Output Amplitude - GSE..	-5 to +5V
Fixed Stage Output Amplitude-FM/FM..	-2.5 to +2.5V
Switched Stage Gain - Lo Gain.....	1.0
Switched Stage Gain - Hi Gain.....	16.0
Switched Stage Output Amplitude-PCM.	-5 to +5V
Input noise level.....	~45 μV
Logic Drive to Gain Switched Amp....	TTL, 0=Lo, 1=Hi
Power Supply Voltages.....	+15, -15, +5V

TABLE 3.3

Gain-Switching Control Logic

Type of Logic Elements	Standard TTL
Input Signals	
Sample Command	1 μs, 26 KHz positive pulse
Sample Period Inhibit	5 μs, 26 KHz positive pulse
Mode Command	99 ms, 1 Hz positive pulse
White Light Status	0 to 1 transition, center of scan
I/F Signal	-5 to +5V Analog
Output Signals	
Gain Control	Logic 0=Low, 1=Hi
Gain State	Logic 0=Low, 1=Hi
Power Supply Voltages	+5V

3.2 DESIGN DESCRIPTION

The signal processing electronics is one of three contained in the detector dewar electronics package. It contains the detector-TIA, ac and dc signal amplifiers and the gain switching control logic. The circuit diagram is shown in Figure 3.2. Figure 3.3 shows the physical configuration of the detector dewar electronics assembly.

3.2.1 AC Signal Component Amplifier

This circuit takes the signal from the detector-TIA, which has a noise level of approximately 45 μV, a signal bandwidth of 500-2200 Hz and a specified dynamic range of 20,000, and amplifies it with appropriate band-limiting to levels compatible with the GSE, FM/FM telemetry voltage control oscillator (VCO) and PCM encoder. It is comprised of AR1, AR2, AR3, AR4 and AR5 (reference Figure 3.2).

Amplifier AR2 is an ac coupled, inverting stage. The dc gain is zero and the high-frequency gain approaches $-R_{10}/R_9 = -4.0$. The lower cutoff frequency is:

$$f_c = \frac{1}{2\pi R_9 C_3} = 12.5 \text{ Hz}$$

AR3 and AR4 are unity-gain high-pass and low-pass filters respectively. Both units have 4-pole Butterworth response characteristics to give minimum phase shift across the signal bandwidth of 500 to 2200 Hz. The corner frequency for the high-pass filter AR3 is 125 Hz. The corner frequency for the low-pass filter AR4 is 8800 Hz. The band edge attenuation slope is 24 dB/octave for both units.

AR1 is a voltage-follower which buffers the signal to the GSE and an attenuator which furnishes the signal to the FM/FM VCO. AR5 is the gain-switched amplifier. This unit is capable of rapid switching between programmed gains of one and sixteen under control of a digital logic signal.

The amplifier is switched to the high-gain (X16) state at the beginning of each interferometer scan. It remains in this state until the output signal exceeds a preset threshold. The amplifier

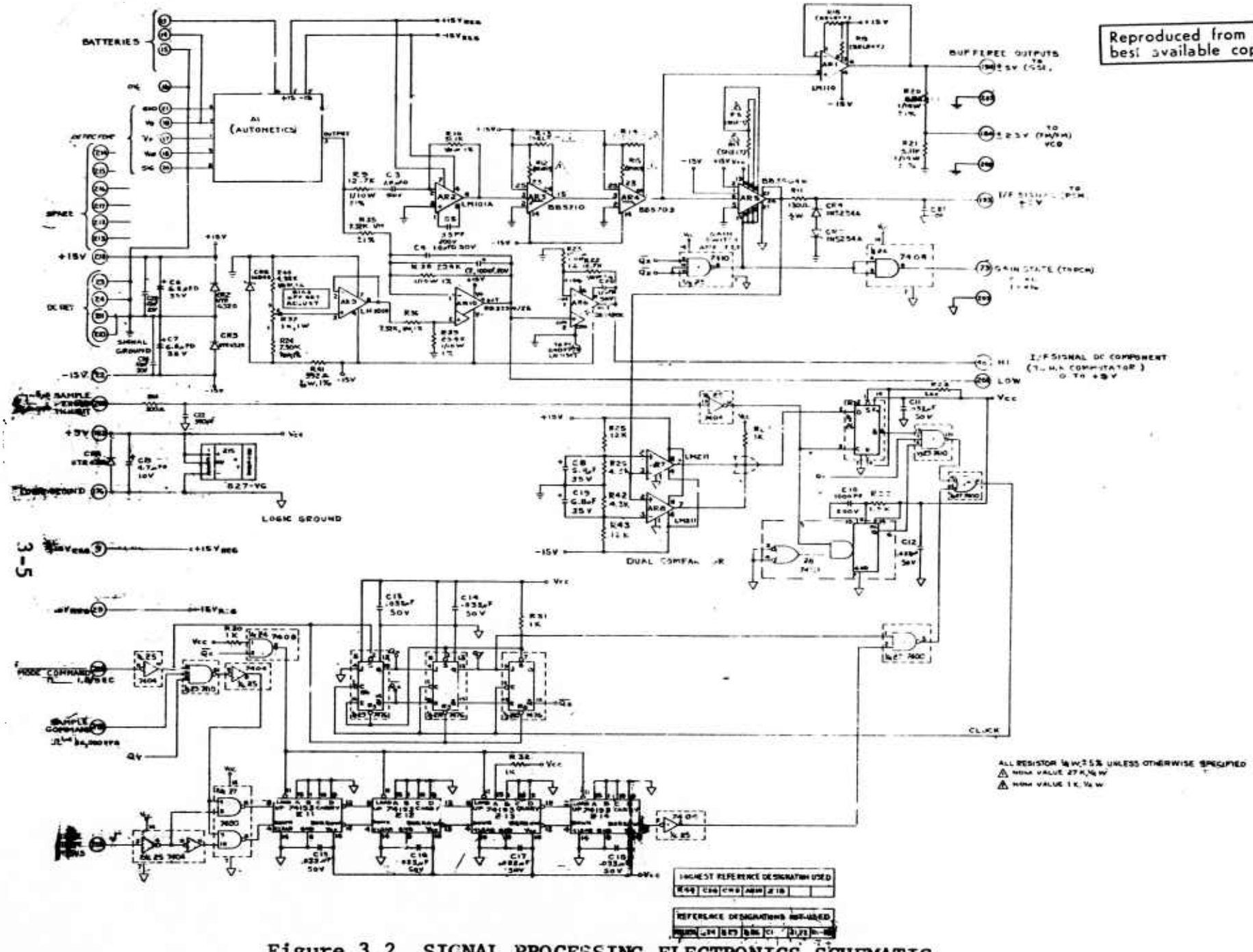
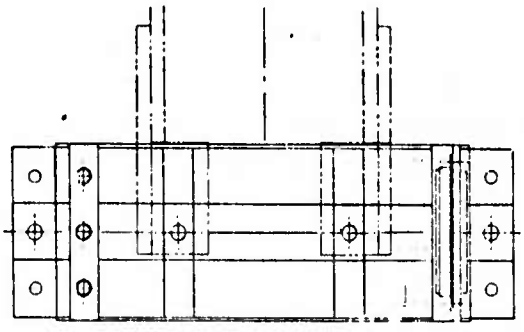
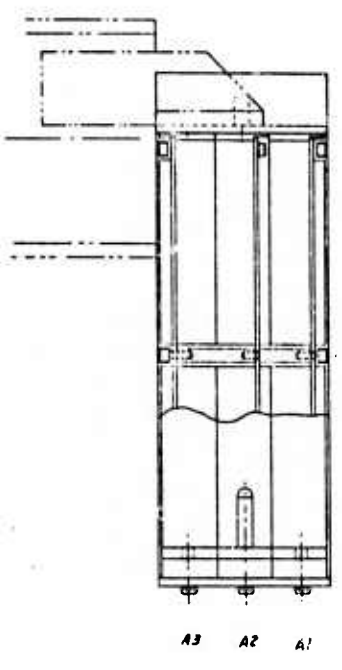


Figure 3.2 SIGNAL PROCESSING ELECTRONICS SCHEMATIC

DETECTOR DEWAR ELECTRONICS

A1 1/F SIGNAL PROCESSOR
A2 MIRROR SERVO
A3 WHITE LIGHT LASER EL





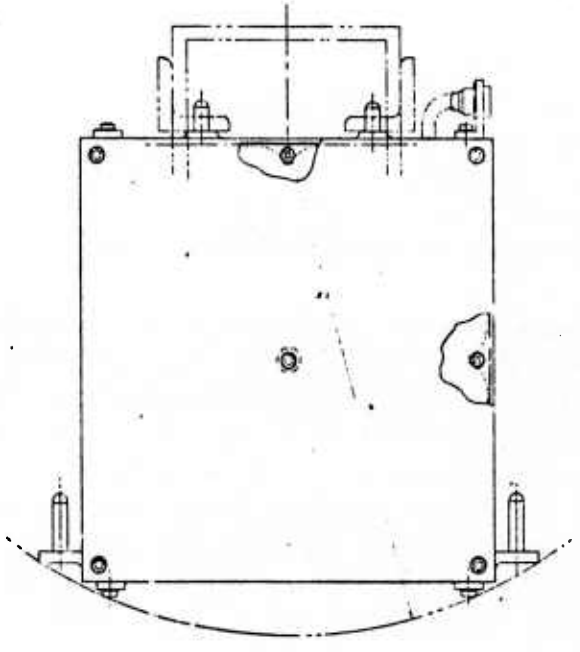


Figure 3.3 DETECTOR DEWAR ELECTRONICS

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is then switched to the low-gain (X1) state and a timer is started. When the White Light Status Signal, indicating the center of the interferometer scan, or zero retardation, is received, the timer is stopped and programmed to gener a slightly longer time interval than the one it measured. When this time has elapsed, the amplifier is again switched to the high gain state for the remainder of the scan.

The output of AR5 is connected to the comparator and to a limiter composed of R11, CR4 and CR5. The limiter clips signals which are greater than ±7 volts. Its output is connected to the PCM encoder.

3.2.2 Gain-changing Logic

The gain-changing logic consists of digital logic for controlling and indicating the gain state of the gain-switching amplifier during each scan of the interferometer. It consists of a dual signal comparator, an up-down counter timing circuit, sequence controller and a circuit to inhibit gain-changing during the 5-μs sample period of the PCM encoder.

The dual signal comparator is comprised of two voltage comparators, AR7 and AR8. These compare the instantaneous output signal amplitude with two fixed threshold voltages of +3.9 and -3.9. The two outputs are wire OR'd via R27 to the logic supply voltage to provide a compatible logic signal to the control logic. The response characteristic of the dual comparator is shown in Figure 3.4. If the signal level is between the two thresholds, the output is a logic HIGH. If the signal level exceeds either of the threshold levels, the output is a logic LOW.

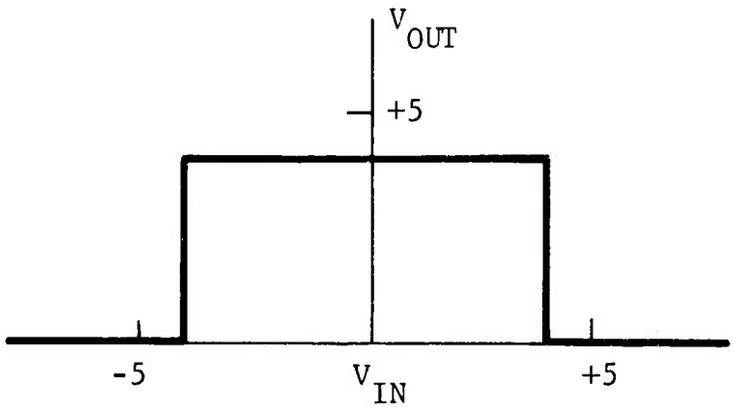

Figure 3.4 RESPONSE CHARACTERISTICS OF DUAL COMPARATOR

The sequence controller consists of three J-K flip-flops (Z9A, Z10A, Z10B) whose outputs are designated Qx, Qy and Qz. It is basically a shift register with three permissible states of the XYZ flip-flops; 100, 010 and 001. It is forced to the 100 state by the MODE COMMAND signal during the interferometer flyback period. In this state, $\overline{Qx}$ is LOW and is applied to pin 9 of Z3 and pin 2 of Z4. The output of Z3 is then HIGH and causes the gain-switched amplifier, AR5, to be in the high-gain state during flyback and the initial part of the active scan period. Pin 3 of Z4 is also LOW and forces a predetermined count (256) to be loaded into the up-down counter and held. Qx also enables pin 1 of Z3 which ultimately passes a clock pulse from Z8, which switches the controller to the next state. This pulse only occurs if the dual comparator senses that the signal amplitude is greater than one of the fixed thresholds. If neither of the thresholds is exceeded, the controller remains in the 100 state and the gain-switched amplifier remains in the high-gain state of the entire scan.

If the signal exceeds one of the thresholds (usually prior to the center of the interferometer scan) and causes the generation of a clock pulse, the sequence controller is shifted to the 010 state. The first stage is constrained to load only zero's on this and subsequent clock pulses by hard wiring the J-input to a logic LOW and the K-input to a logic HIGH. The one which was in the first stage is shifted to the second stage, by the clock pulse. Simultaneously, the zero in the second stage is shifted to the third stage, and the zero in the third stage is shifted out.

With the controller in the 010 state, both $\overline{Qx}$ and $\overline{Qz}$ are HIGH and the output (Pin 8) of Z3 is LOW. This forces the gain-switched amplifier, AR5, to the low-gain state. Also, Qy enables pin 5 of Z3 so that 26 kHz Sample Command pulses are passed to the up-down counter. When Qx goes LOW, $\overline{Qx}$ goes HIGH and the LOAD input to the counters is also HIGH, allowing them to count the Sample Command pulses.

Prior to the center of the interferometer scan, the White Light Status level is LOW and the Sample Command pulses are gated to the UP input of Z11 and the entire counter counts up from the preset count. When the center of scan is sensed by the white light detector, White Light Status goes HIGH and the Sample Command pulses

are gated to the DOWN input of Z11. The counter commences to count down from whatever count it had reached toward zero. Since there was a preset count in the counter and the Sample Command pulses occur at a fixed rate, it takes slightly longer to reach zero, than it takes to count from the instant the signal exceeds the threshold to the center of scan. This allows for some asymmetry in the interferogram.

When the counter reaches zero, a Borrow pulse is gated out of pin 13 on Z14. This clocks the controller to the 001 state. In this state, $\overline{Qz}$ switches AR5 back to the high-gain state for the remainder of the scan. Qy is Low and Sample Command pulses are inhibited from the counter. Also, the controller is inhibited from advancing to any other state. The system remains in this condition until the flyback portion of the MODE COMMAND signal resets it. If flyback is reached before the counter times out, the controller and counter are reset immediately for the next scan.

Gain switching is inhibited from occurring during the 5-μs sample period of the PCM encoder when switching from the high-gain to the low-gain state by Z6 and Z8. Z6 is a type D flip-flop. It will change only on a positive clock edge at pin 3. The D input at pin 2 is normally High and the output at pin 6 is Low. If the signal exceeds the threshold, the comparator output and the D input of Z6 to Low. If it is still low on the next clock transition, $\overline{Q}$ at pin 6 will go High. The 5-μs Sample Period Inhibit pulses from the PCM encoder are inverted and applied to both the C input of Z6 and pin 5 of Z8. Z8 generates a 1-μs pulse on the trailing edge of each Sample Period Inhibit pulse. If pin 6 ($\overline{Q}$) of Z6 is High and the controller is in the 100 state (Qx High), a pulse will be gated through to advance the controller to the 010 state. When switching from the low-gain to the high-gain state after the center of scan, the switching occurs at the beginning of the Sample Period Inhibit pulse, since one of the Sample Command pulses is gated trhough the counter to become the Borrow pulse.

3.2.3 DC Signal Component Amplifier

The intensity of the source being measured by the interferometer may vary during each scan due to motion of the instrument payload along its trajectory and time variance of the source intensity. Some time after the design of the signal processing electronics had started, a requirement to monitor the dc component of the signal was included.

The dc output of the TIA has a relatively large steady offset component, which is due to the applied detector battery potentials, TIA MOSFET characteristics, etc. The dc component of the interferometer signal is added to this. It has a magnitude of 1/2 the peak to peak amplitude of the ac signal.

The dc signal component amplifier consists of a stable voltage reference source (zener diode CR6 and voltage follower AR9) to reduce the dc component and two chopper stabilized amplifiers (AR10 and AR6) to provide the required gain.

3.2.4 Power Circuits

The signal processing electronics board incorporates reverse polarity protection diodes on +15, +5 and -15 volt power supply inputs. In addition, an overvoltage crowbar Z15 is connected to the +5 volt input to protect the digital logic. The TIA and first signal amplifier receive power from separate +15 and -15 volt regulators, which are located on another board.

3.3 PERFORMANCE

Figure 3.5 shows the frequency response of the ac channel amplifier. It has the required flat top and 24 dB/octave slope of the two 4-pole Butterworth filters.

Initially, the ac amplifier was designed with a gain of 29.4 on the input stage and a gain of 8 in the high-gain state of the output amplifier. Figure 3.6 shows the gain characteristic for this configuration. The calculated NEP and the 14-Bit A/D converter limits are plotted on the axes. Operation is along the upper curve until the instantaneous output voltage exceeds the 3.7 V threshold. Operation is then switched to the lower curve until the logic control circuitry times out. Presumably, by this time the signal amplitude is again below the threshold and operation is again along the upper curve.

Subsequently, the detector load resistor value and some of the system parameters were changed. This necessitated changing the gain of both the input and output amplifiers to the values listed in Table 3.2. Figure 3.7 shows the predicted gain characteristic for the final configuration. Operation is the same as described for the preceeding figure.

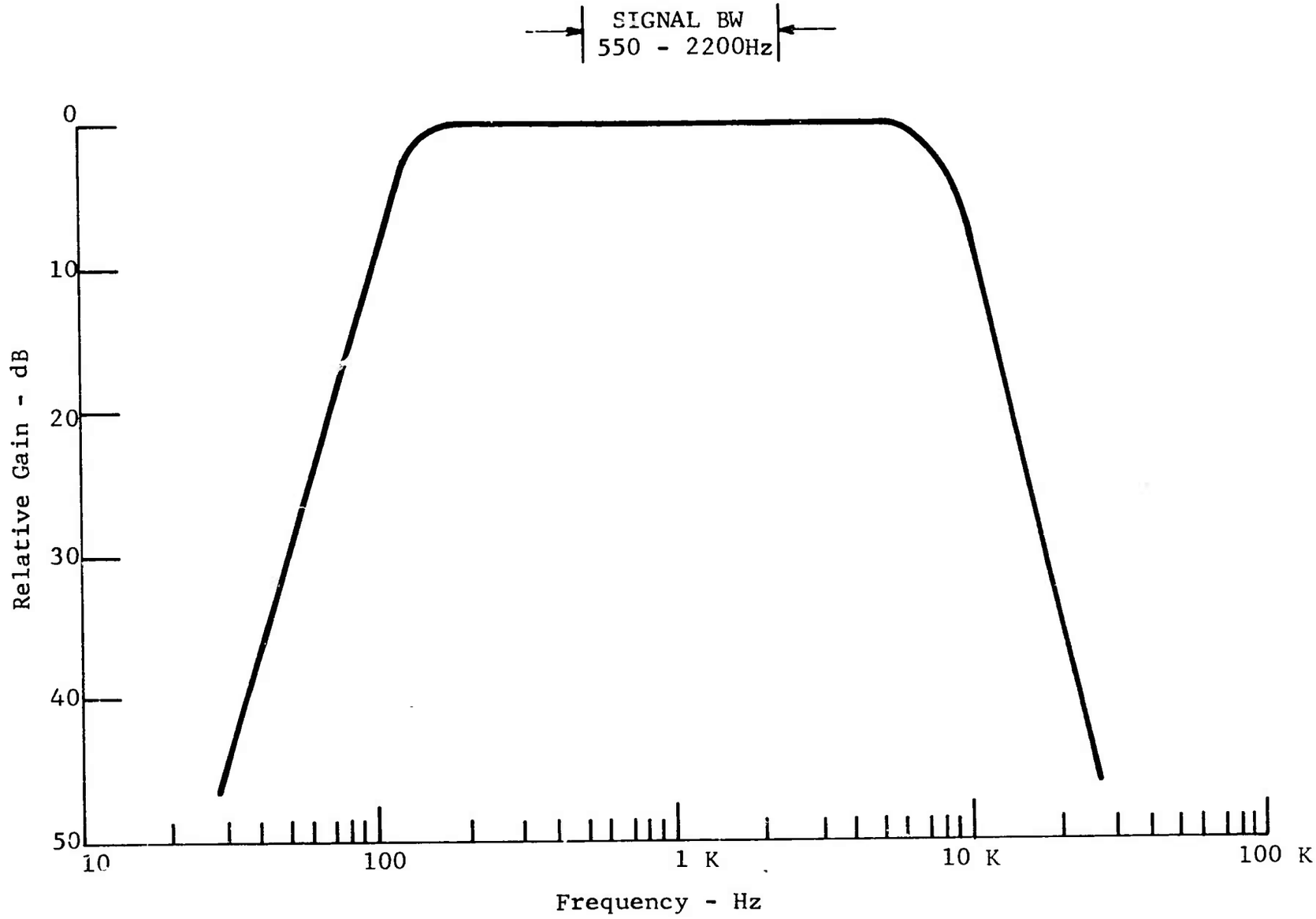

Figure 3.5 SIGNAL PROCESSOR A-C CHANNEL FREQUENCY RESPONSE

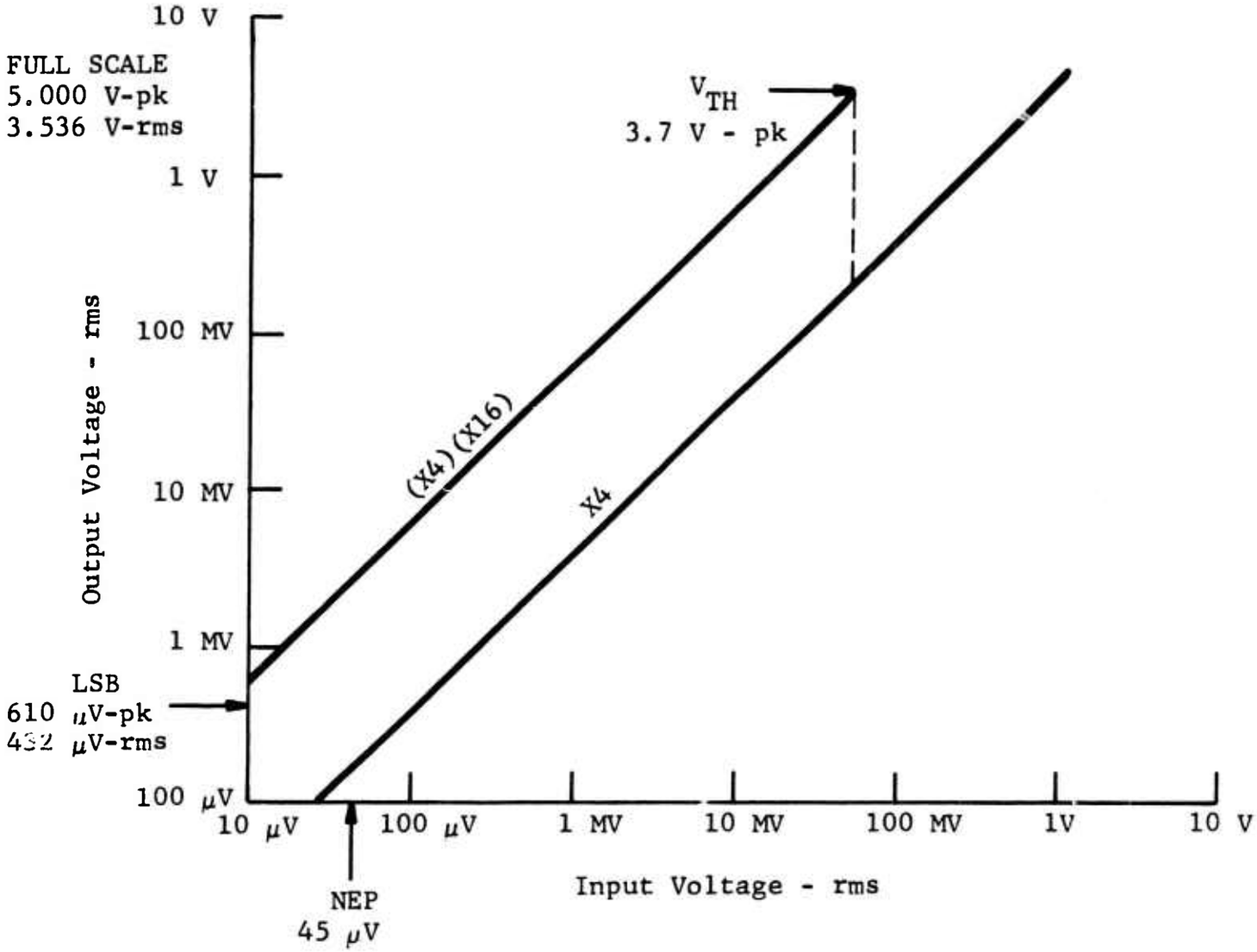

Figure 3.6 AC AMPLIFIER GAIN CHARACTERISTIC
INITIAL CONFIGURATION

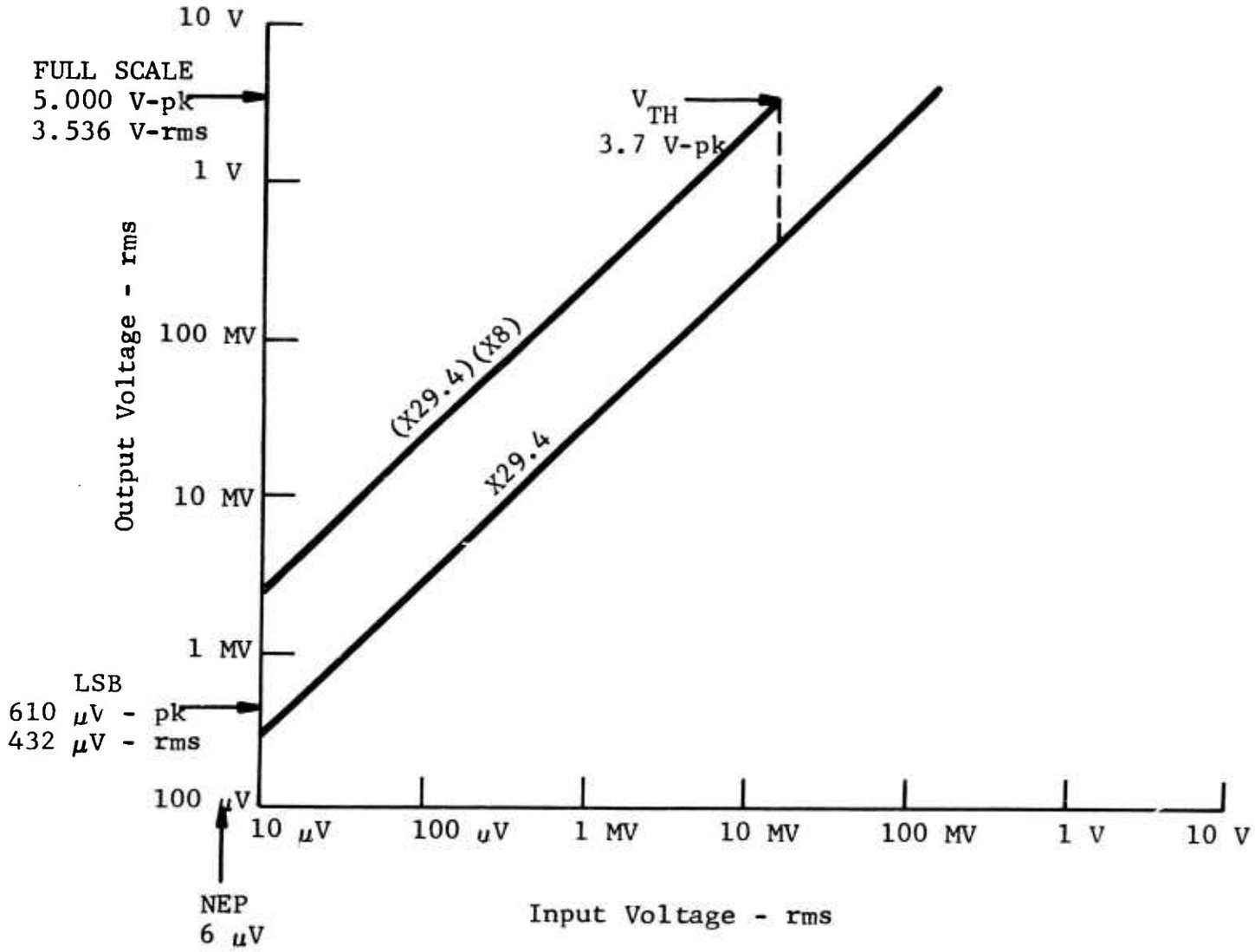

Figure 3.7 AC AMPLIFIER GAIN CHARACTERISTIC
FINAL CONFIGURATION

Figure 3.8 shows the ac amplifier output noise characteristics. The two solid curves were measured. The dashed curve was extrapolated. Spiking at harmonics of the 60 Hz line frequency was observed, but was not plotted in this figure.

Table 3.4 lists the manufacturer's specifications on the gain-switched amplifier. These units function very well, but require considerable care in handling since the logic input pins are connected to unprotected MOSFET's.

The dc channel amplifier exhibited the required gain characteristics, but the approach taken is generally unsatisfactory and this circuit is slated for redesign. Specific problems are:

1. The shift in the steady dc value due to changes in background are greater than anticipated. The high gain requires a comparatively small value potentiometer, which then restricts the signal range which can be balanced out.

2. Shifts in the dc level of signal require a reference which follows the average value of the signal rather than the fixed reference employed.

3. If the differential input signal is large enough to cause either the output amplifier or both to saturate, the chopper noise increases considerably and gets into the ac channel.

4. Better lowpass filtering is required to keep the ac signal components out of the dc channel.

5. The housekeeping A/D converter in the PCM encoder accepts unipolar 0 to +5.12 V signals. Means to insure that the dc component is within this range are required.

The gain-changing logic has performed satisfactorily during bench tests.

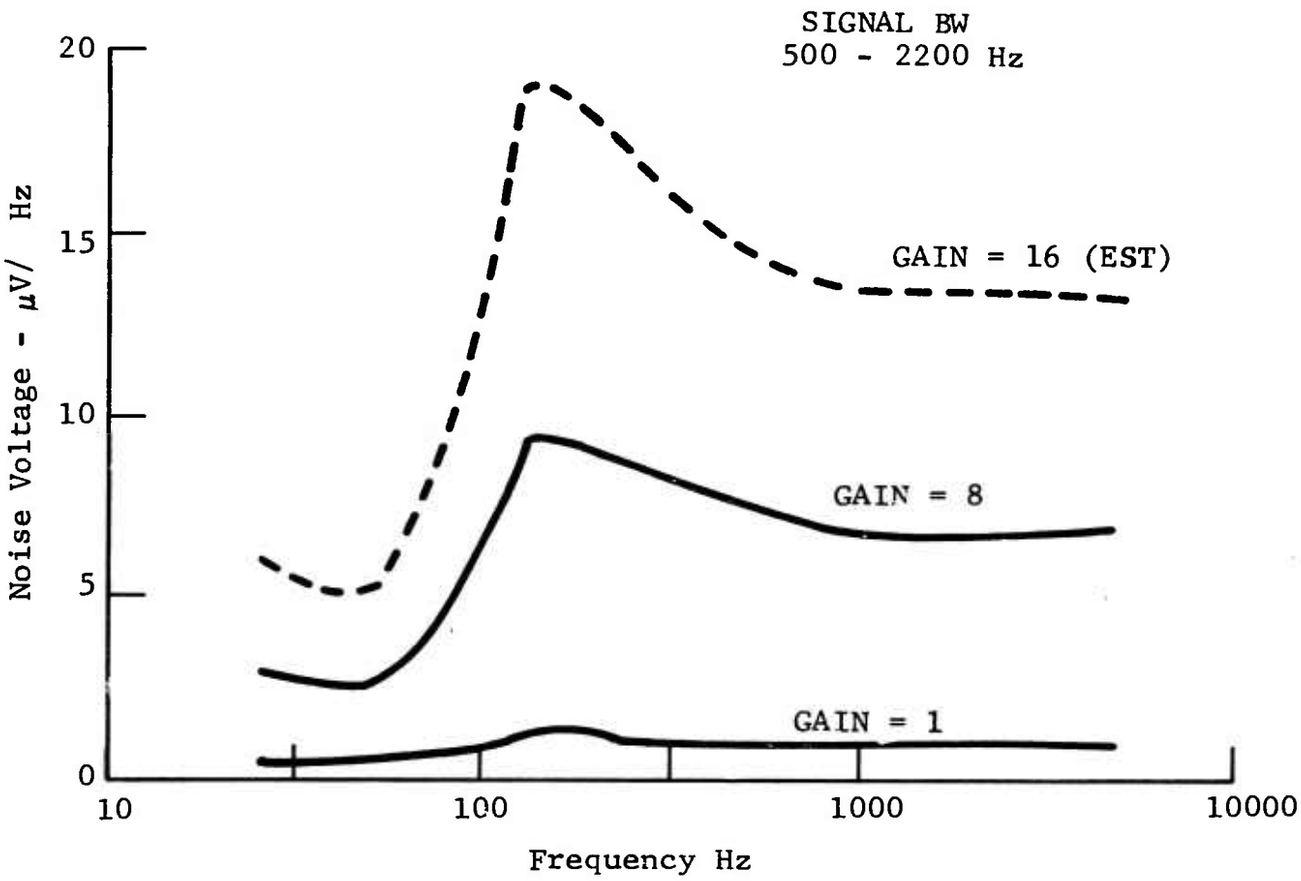

Figure 3.8 SIGNAL PROCESSOR OUTPUT NOISE SPECTRUM

Table 3.4

GAIN-SWITCHING AMPLIFIER REQUIREMENTS

ELECTRICAL SPECIFICATIONS Typical at 25°C and with rated supplies unless otherwise noted.

MODELS	3604K
GAIN	
Gain Steps	1,2,3, . . . , 15, 16
Gain Accuracy	
at 25°C, max.	±0.1%
vs. Temperature	±0.001%/°C
Nonlinearity, max.	
Up to ±5 V Input	±0.01%
Up to ±10 V Input	±0.02%
OUTPUT	
Rated Output	±10 V, ±20 mA
Output Impedance	
at Maximum Gain	0.5 ohm
at Minimum Gain	0.05 ohm
INPUT	
Input Impedance	10^{11} ohm
Input Voltage Range	±10 V
OFFSETS AND NOISE	
Offset Voltage (referred to input)	
at 25°C, max.	±1 mV
vs. Temperature, max.	±30 µV/°C ±10 µV/°C
vs. ±15 V Power Supply	±100 µV/V
Input Bias Current, max.	10 pA
Input Noise (RTI) at Max. Gain	
0.01 Hz to 10 Hz	5 µV p-p
10 Hz to 1 kHz	50 µV rms
DYNAMIC RESPONSE	
Small Signal Response (±3 dB)	
at Maximum Gain	100 kHz
at Minimum Gain	500 kHz
Slew Rate	10 V/µs
Settling Time to Within ±1 mV	
of Output Final Value	
at Maximum Gain	20 µs
at Minimum Gain	5 µs
GAIN SWITCHING (TTL Logic Levels)	
Gain Control Logic Inputs	
Logical 1	+2 V min.
Logical 0	+0.8 V max.
Loading	1 TTL Load
Settling Time to Within ±1 mV of	
Output Final Value	25 µs (at all gains)
POWER SUPPLY REQUIREMENTS	
Analog Supply	
Rated Supply Voltage	±15 Vdc
Supply Range	±14 Vdc to ±16 Vdc
Supply Drain	
at Quiescent	+18 mA, -9 mA
at Rated Output	+38 mA, -29 mA
Digical Logic Supply	
Rated Supply Voltage	+5 Vdc
Supply Range	+4.8 Vdc to +5.2 Vdc
Supply Drain	
at Quiescent	30 mA
TEMPERATURE RANGE	
Specification	0°C to +70°C
Storage	-55°C to +100°C

SECTION 4

PCM ENCODER

The functions of the PCM encoder are:

1. Convert the analog signal from the interferometer to a 14-bit digital signal at the Sample Command rate of 25,930 ± 2% conversions per second during the scan period of the interferometer.
2. Convert the analog signal from the housekeeping commutator to an 8-bit digital signal at the 912 Hz frame rate at the PCM encoder.
3. Associate logic levels representing the i-f signal processor gain state and the White Light Status with the corresponding 14-bit digital words representing signal amplitude.
4. Associate the 6-bit Channel ID code with the corresponding 8-bit digital word representing the housekeeping signal amplitude.
5. Provide a 2,048 word X 16 bits/word buffer memory to compensate for variations in the sample rate and the fixed telemetry output rate.
6. Provide an internal 10-bit counter which is incremented for each interferometer sweep.
7. Provide a 22-bit Barker frame synchronizing code.
8. Provide an idling pattern of ones and zeros in the data words during the interferometer flyback period.
9. Digitally multiplex all of the above digital signals in accordance with the specified frame format.
10. Convert the multiplexed parallel digital words to a continuous serial digital data stream at the specified bit rate (466,944 bits/second).
11. Filter the serial digital output for proper modulation of an S-band PCM telemetry transmitter.

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12. Provide unfiltered serial digital outputs for the GSE decommutator or for a digital tape recorder.

13. Generate all the necessary clock and timing signals for formatting the data.

14. Develop all operating voltages required from the 28V payload battery supply.

The PCM encoder is defined in HRC Specification No. 21008493 which is included as Appendix A and is under development by Vector Aydin. It incorporates two unique features. The first is the inclusion of a 2,048 word, 16 bits/word solid state buffer memory to compensate for variations in the data sampling rate, formatting and the fixed output telemetry rate. The original specification was for a 512 word memory. Studies indicated that this capacity was marginal and the specification was changed. A new static RAM integrated circuit (Intel 2102) became available at this time and made it possible to package the 2,048 word buffer in the same volume as the original 512 word buffer. The second feature is the 14-bit high-speed A/D converter. The speed and resolution requirements exceed the capabilities of most available commercial A/D converters. There are some relatively complex laboratory instruments capable of this performance, but smaller modules are just becoming available.

4.1 REQUIREMENTS

The electrical requirements for the PCM encoder are summarized in Table 4.1.

4.2 DATA FORMAT

The data format of the PCM encoder is shown in Figure 4.1. The basic frame consists of 32 sixteen-bit words. There are 64 of these frames to each subframe.

The 16 bits of word No. 1 and the first 6-bits of word No. 2 in every frame are encoded with the 22-bit Barker synchronizing code. The last 10 bits of word No. 2 are encoded with the output of a 10-bit binary sweep counter which is incremented once for each interferometer scan.

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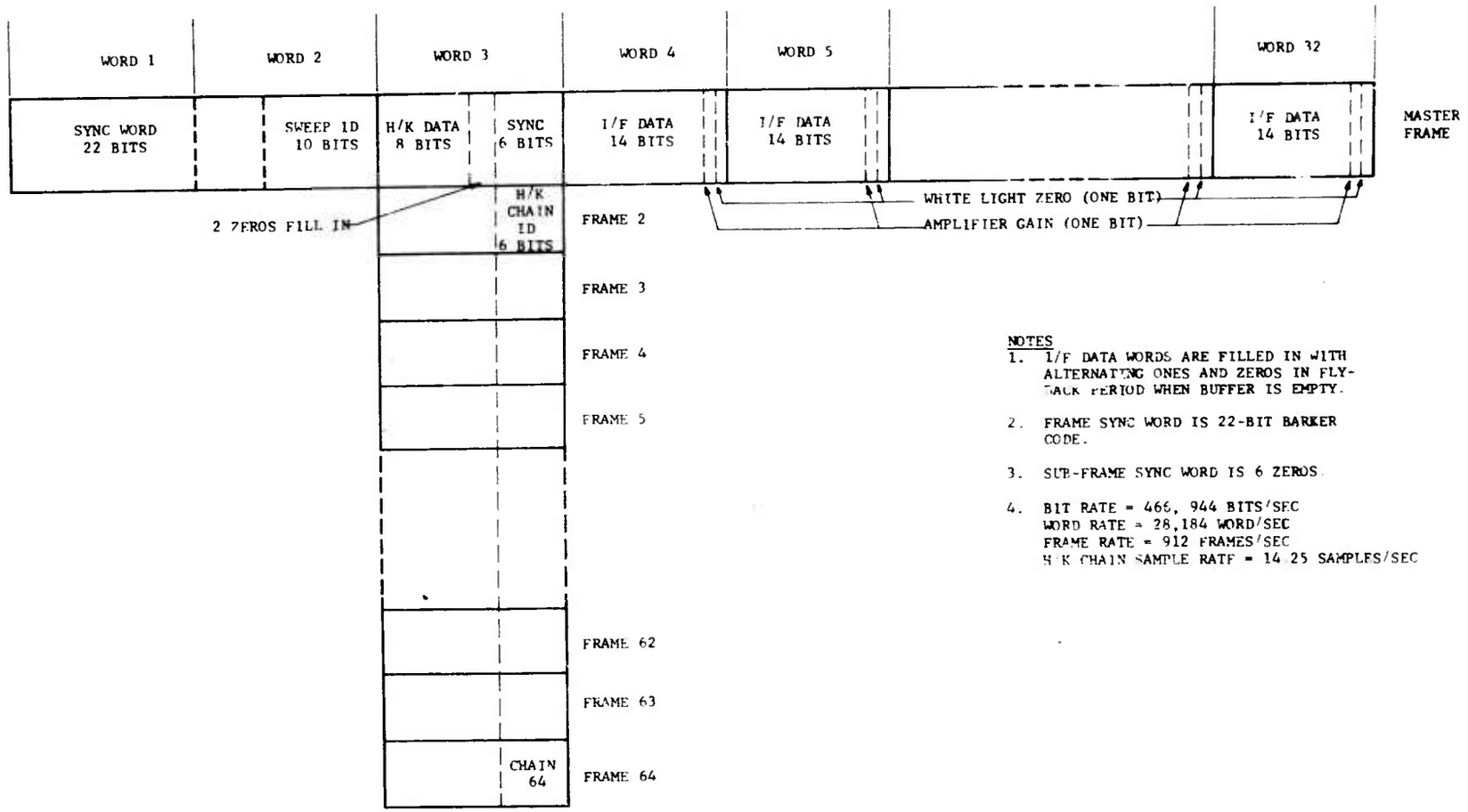

Figure 4.1 PCM FRAME FORMAT

Table 4.1

PCM ENCODER REQUIREMENT

INTERFEROMETER SIGNAL	Sample rate: 25,500 - 26,450 per second A/D Conversion: 14 bits, ±0.1% absolute accuracy, ±.01% nonlinearity Signal Input: 500-2200 Hz, ±5V
HOUSKEEPING SIGNAL	Signal Input: 0-5V, commutated at 912 Hz A/D conversion: 8 bits, ±0.5% absolute accuracy, ±.5% nonlinearity Channel ID: 6 bits
OTHER INPUTS	I/F processor gain state: logic 0 or 1 White Light Status: logic 0 or 1 Sample trigger: 25,500 - 26,450 pps Mode Command: 1.000 Hz
BUFFER MEMORY CAPACITY	2048 - 16 bit words
PCM OUTPUT	Serial digital stream NRZ-L mode 16 bits per word, 32 words per frame, 22 bit Barker code sync, 10 bits sweep count Clock rates: 466,944 bits/second 29,184 words/second 912 frames/second
PRIME POWER	28 Vdc at 1.2 A
PACKAGE	100 cubic inches - direct plug-in to rocket section-7 pounds

The first 8 bits of word No. 3 are encoded with the output of the housekeeping A/D converter. The input to this converter is multiplexed by the housekeeping commutator (a separate unit) at the 912 Hz frame rate, so that these bits in each frame represent the output of a different housekeeping sensor. Some sensors are supercommutated so that their outputs appear several times in each subframe. The last 6 bits of word No. 3 are encoded with the output of a counter in the housekeeping commutator which identifies the input channel which is encoded in the first six bits. This code may be used for a subframe synchronizing code in a PCM decommutator. Initial plans were to incorporate a 10-bit A/D converter in the unit for housekeeping, but this was changed to 8 bits. Bits 9 and 10 of word No. 3 were then strapped to encode two zeros.

The remaining 29 words of each frame are all structured alike. When there is data in the buffer during the interferometer scan period, the first 14 bits of each word are encoded with the output of the 14-bit A/D converter. The last two bits indicate the amplifier gain state and white light status associated with that sample. When the buffer is empty, the last 29 words of each frame are encoded with an alternating one-zero pattern.

4.3 DESIGN DESCRIPTION

Figure 4.2 is a block diagram of the PCM encoder. The digital elements have been implemented with TTL logic.

The interferometer signal from the signal processor electronics is connected to the i-f data sample/hold and 14-bit A/D converter. Initially, a dual sample/hold circuit was considered to allow more time to acquire the signal amplitude on each sample, but due to the complexity of associating the amplifier gain state and white light status with each sample, a single sample/hold circuit was employed. It acquires the signal amplitude in approximately 5μs. The A/D converter is of the successive approximation type and operates at a speed of about 2μs/bit. When a conversion is complete, the 14 bits of data and two associated status bits are strobed into the buffer memory. The A/D converter has a signal range of -5.0 to +5.0 volts and encodes the data in the binary two's complement code.

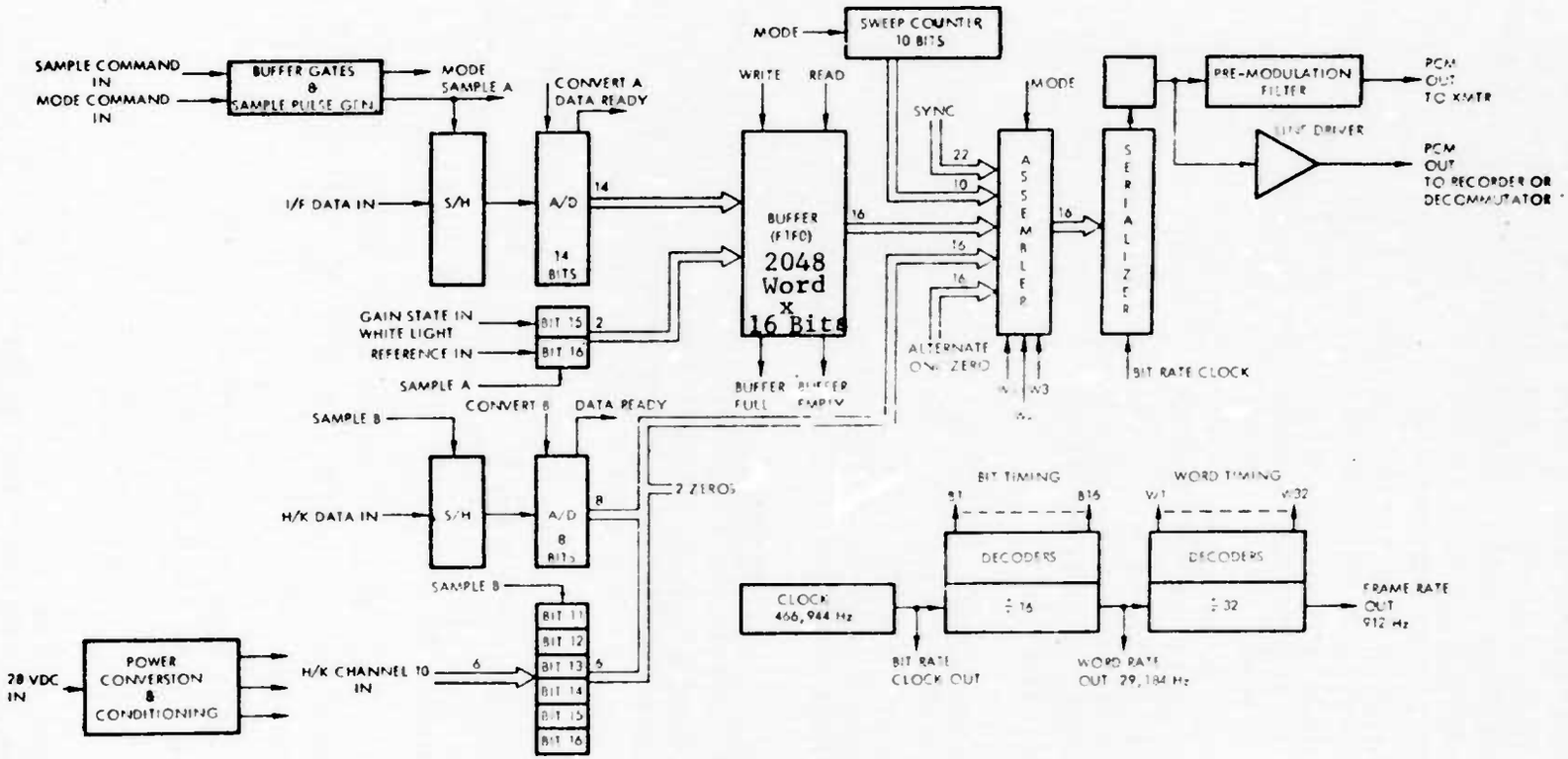

Figure 4.2 PCM ENCODER BLOCK DIAGRAM

The buffer memory has a capacity of 2,048 words at 16 bits/word. Each time the A/D converter completes a conversion, it initiates a Write cycle in the memory. The word is stored and the Write Address Counter is incremented. The Write cycle may be inhibited momentarily if the buffer is in a Read cycle. Assuming that the buffer is empty at the beginning of a scan and the encoder is outputting the alternating one-zero pattern in the data words, as data is received and digitized, it is stored in the buffer until some preset number of words are stored. Then it is connected to the data multiplexer and Read cycles are initiated. Each time a data word is read, the Read cycle counter is incremented. At the end of a scan, data is no longer written into the buffer, but reading continues until the last data word is read out. At this time the encoder reverts back to filling data words with the alternating one-zero pattern.

A separate Sample/Hold and 8-bit A/D converter is employed for Housekeeping Data. This operates in synchronism with the Housekeeping Commutator at the 912 Hz frame rate. The A/D converter has a range of 0 to +5.12 V (20 mV/bit) and encodes in straight binary.

The signal multiplexer connects the various data sources to the serializer to accomplish the desired output format. It is under control of a counter chain driven by a crystal oscillator at the bit rate. The serializer converts the 16-bit parallel words into a continuous serial bit stream.

The serializer output (NRZ-L) is connected to a line driver which buffers the digital output to GSE. A premodulation filter shapes the digital output to make it compatible with the S-band telemetry transmitter.

The PCM encoder includes its own power conditioner to develop the required voltages from the 28 volt battery power furnished. The inverter is synchronized with the sample rate during scan to minimize the effects of switching transitions. It also includes circuitry to prevent damage due to reverse polarity of the input 28 V dc power.

4.4 PERFORMANCE

Acceptance testing of the PCM encoder was accomplished in accordance with acceptance test procedures required by the design specification. Briefly, these tests measured power

requirements, various interface signal characteristics, data formatting, static encoding accuracy of both the 8-bit and 14-bit A/D converters at 0°C, at ambient and at 60°C. Data Sheets (Figures 4.3 through 4.6) show that the unit performs well within specifications over the temperature range.

The PCM encoder was also tested dynamically by connecting a ramp generator to the analog input and a decommutator, D/A converter and scope to the output. The reconstructed ramp was observed as the input sample rate was varied. Figure 4.7 shows that performance exceeded the ±1% specification. Subsequently, the buffer capacity was increased from 512 words to 2048 words. This should increase the specification on sample rate to 26,000 ±4% pulses/second.

The PCM encoder has also been successfully operated with the interferometer, PCM decommutator, GSE control and computer.

DATA SHEET

Ref. Paragraph	Category	Ambient	0 °C	±60 °C	Specification Requirement
6.1.1	Ground Isolation	OK	-------	----------	Mutually Isolated Grounds
6.1.2	Reverse Voltage	OK	-------	----------	No Damage
6.1.3	Input Power Current Drain				1.2 A Maximum
	Voltage: +28 Vdc	0.89 Amps	0.81 Amps	0.82 Amps	
	+33 Vdc	0.88 Amps	0.81 Amps	0.82 Amps	
6.1.4	Bit Clock Fre.	466,962 Hz	466,965 Hz	466,921 Hz	466,944 Hz ±0.1%
6.1.6.1	Frame Rate Clock	50% Duty Cycle	50%	50%	50% Duty Cycle:
6.1.5.2	Word Clock "0" =	0.0 Volts	0.1 Volts	0.4 Volts	Logic 1 = 2.4 to 5 volts
6.1.5.3	Bit Clock "1" =	3.8 Volts To 4.3 Volts (Word Clock)	3.2 Volt To 3.5 Volts	3.4 Volts To 3.8 Volts	Logic 0 = 0 V + 0.5 V -0.0 V
6.1.5.4	Buffered NRZ-L 50 ohm Load	Logic "1"=3.2V Logic "0" = 0.15 V	"1" = 2.7 V "0" = 0.2 V	"1" = 2.8 V "0" = 0.1 V	NRZ-L code; with 50 ohm load
	1TTL Gate Load	Logic 1 = 3.6 V	"1" = 3.0 V	"1" = 3.2 V	Logic 1 = 2.4 to 5 volts
		Logic 0 = 0.75 V	"0" = 0.7 V	"0" = 0.6 V	Logic 0 = 0 V ±0.5 V- 0.0 V
	1.2 K Load	Logic 0 = 0.4 V	"0" = 0.4 V	"0" = 0.4 V	
6.1.5.5	Filtered NRZ-L	5.2 Vpp or ±2.6 Vpp	4.6 Vpp or ±2.3 Vpp	4.7 Vpp or ±2.35 Vpp	±2.5 volts peak to peak ±10%
6.1.5.6	Sample Command	5.2 us	5.4 us	5.0 us	5.2 ±0.5 micro seconds
		Logic "1" = 3.8 V	"1" = 3.2 V	"1" = 3.4 V	
		Logic 0 = 0.1 V	"0" = 0.1 V	"0" = 0.0 V	Voltage levels same as logic levels for clock outputs

DATA SHEET

Ref. Paragraph	Category	Ambient	0 °C	+60 °C	Specification Requirement
6.1.5.7	Short circuit protection against damage	OK All Outputs checked	---	---	No damage
6.1.6.1	Word 1	OK	OK	OK	MSB LSB 111 100 110 110 101 0
6.1.6.2	Word 2	OK	OK	OK	MSB Bit 1 Bit 6 000 000 - Bit 7 through bit 16 Status of Sweep Counter
6.1.6.3	Words 4 through 32 and sub-frame 1 through 99	OK	OK	OK	Flyback Words MSB LSB 010 101 010 101 010 1 I/F Words: Depends on analog input
6.1.6.4	Bit 15 and 16	OK	OK	OK	Under control of switches on I/F signal simulator
6.1.6.5	H/K Channel I.D.	OK	OK	OK	H/K word content agrees with programming at H/K commutator inputs

INTERFEROMETER ENCODING ACCURACY

Input Voltage	Bit 1 2 3 4 5 6 7 8 9 10 11 12 13 14
+5.000	0 1 1 1 1 1 1 1 1 1 1 1 1 0
+4.500	0 1 1 1 0 0 1 1 0 0 0 1 1 0
+4.000	0 1 1 0 0 1 1 0 0 1 1 1 0 1
+3.500	0 1 0 1 1 0 0 1 1 0 0 1 1 0
+3.000	0 1 0 0 1 1 0 0 1 1 0 0 1 1
+2.500	0 1 0 0 0 0 0 0 0 0 0 0 0 0
+2.000	0 0 1 1 0 0 1 1 0 0 1 1 0 1
+1.500	0 0 1 0 0 1 1 0 0 1 1 1 0 1
+1.00	0 0 0 1 1 0 0 1 1 0 0 1 1 1
+0.500	0 0 0 0 1 1 0 0 1 1 0 0 1 1
0.000	0 0 0 0 0 0 0 0 0 0 0 0 0 0
-0.500	1 1 1 1 0 0 1 1 0 0 1 1 0 1
-1.000	1 1 1 0 0 1 1 0 0 1 1 1 1 0
-1.500	1 1 0 1 1 0 0 0 1 1 1 1 1 1
-2.000	1 1 0 0 1 1 0 1 0 0 1 1 0 0
-2.500	1 1 0 0 0 0 0 0 0 0 1 1 0 0
-3.000	1 0 1 1 0 0 1 1 0 0 1 1 0 1
-3.500	1 0 1 0 0 1 1 0 0 1 1 1 1 0
-4.000	1 0 0 1 1 0 0 1 1 1 0 0 1 1
-4.500	1 0 0 0 1 1 0 0 1 1 0 1 0 0
-5.000	1 0 0 0 0 0 0 0 0 0 0 1 0 1

Nominal NRZ-L Output in Two's

For Linearity Calculation Record Voltages for

Full Scale 0 1 1 1 1 1 1 1 1 1 1 1 1 1

Full Scale 1 0 0 0 0 0 0 0 0 0 0 0 0 1

Ambient

Bit 1 2 3 4 5 6 7 8 9 10 11 12 13 14	Error
0 1 1 1 1 1 1 1 1 1 1 1 1 0	0
0 1 1 1 0 0 1 1 0 1 1 1 1 0	+2
0 1 1 0 0 1 1 0 0 1 1 1 1 1	+2
0 1 0 1 1 0 0 1 1 0 0 0 0 0	+2
0 1 0 0 1 1 0 0 1 1 0 1 0 0	+1
0 1 0 0 0 0 0 0 0 0 0 0 0 1	+1
0 0 1 1 0 0 1 1 0 0 1 1 1 0	+1
0 0 1 0 0 1 1 0 0 1 1 1 1 1	+2
0 0 0 1 1 0 0 1 1 1 1 1 1 0	
0 0 0 0 1 1 0 0 1 1 0 0 1 1	+1
0 0 0 0 0 0 0 0 0 0 0 0 0 1	+1
1 1 1 1 0 0 1 1 0 0 1 1 1 1	+2
1 1 1 0 0 1 1 0 0 1 1 1 1 1	+1
1 1 0 1 1 0 0 0 1 1 1 1 1 1	+1
1 1 0 0 1 1 0 1 0 0 1 1 1 0	
1 1 0 0 0 0 0 0 0 0 1 1 0 0	+1
1 0 1 1 0 0 1 1 0 0 1 1 0 1	+2
1 0 1 0 0 1 1 0 0 1 1 1 1 0	+1
1 0 0 1 1 0 0 1 1 1 0 0 1 1	+1
1 0 0 0 1 1 0 0 1 1 0 1 0 0	+1
1 0 0 0 0 0 0 0 0 0 0 1 0 1	0

Measured NRZ-L Output
Actual Voltage +4.9985
-5.0002

0 °C

Bit 1 2 3 4 5 6 7 8 9 10 11 12 13 14	Error
0 1 1 1 1 1 1 1 1 1 1 1 1 0	0
0 1 1 1 0 0 1 1 0 1 1 1 1 0	+1
0 1 1 0 0 1 1 0 0 1 1 1 1 0	0
0 1 0 1 1 0 0 1 1 0 0 0 0 0	0
0 1 0 0 1 1 0 0 1 1 0 1 0 0	0
0 1 0 0 0 0 0 0 0 0 0 0 0 0	0
0 0 1 1 0 0 1 1 0 0 1 1 1 0	0
0 0 1 0 0 1 1 0 0 1 1 1 1 1	+1
0 0 0 1 1 0 0 1 1 1 1 1 1 0	-1
0 0 0 0 1 1 0 0 1 1 0 0 1 1	0
0 0 0 0 0 0 0 0 0 0 0 0 0 0	0
1 1 1 1 0 0 1 1 0 0 1 1 1 1	+1
1 1 1 0 0 1 1 0 0 1 1 1 1 1	+1
1 1 0 1 1 0 0 0 1 1 1 1 1 1	0
1 1 0 0 1 1 0 1 0 0 1 1 1 0	0
1 1 0 0 0 0 0 0 0 0 1 1 0 0	0
1 0 1 1 0 0 1 1 0 0 1 1 0 1	+2
1 0 1 0 0 1 1 0 0 1 1 1 1 0	+1
1 0 0 1 1 0 0 1 1 1 0 0 1 1	+1
1 0 0 0 1 1 0 0 1 1 0 1 0 0	+1
1 0 0 0 0 0 0 0 0 0 0 1 0 1	0

Measured NRZ-L Output
Actual Voltage +4.9997
-5.0003

+60 °C

Bit 1 2 3 4 5 6 7 8 9 10 11 12 13 14	Error
0 1 1 1 1 1 1 1 1 1 1 1 1 0	0
0 1 1 1 0 0 1 1 0 1 0 0 0 0	+4
0 1 1 0 0 1 1 0 0 1 1 1 0 0	+3
0 1 0 1 1 0 0 1 1 0 1 0 0 1	+3
0 1 0 0 1 1 0 0 1 1 0 1 1 0	+3
0 1 0 0 0 0 0 0 0 0 0 0 1 1	+3
0 0 1 1 0 0 1 1 0 0 1 1 0 1	+3
0 0 1 0 0 1 1 0 0 1 1 1 0 1	+4
0 0 0 1 1 0 0 1 1 1 0 1 0 1	+2
0 0 0 0 1 1 0 0 1 1 0 1 1 0	+3
0 0 0 0 0 0 0 0 0 0 0 0 1 0	+2
1 1 1 1 0 0 1 1 0 0 0 1 0 1	+4
1 1 1 0 0 1 1 0 0 1 1 1 0 1	+3
1 1 0 1 1 0 0 0 1 1 0 1 0 1	+2
1 1 0 0 1 1 0 1 0 0 1 1 0 1	+2
1 1 0 0 0 0 0 0 0 0 0 1 1 1	+3
1 0 1 1 0 0 1 1 0 0 0 1 0 1	+4
1 0 1 0 0 1 1 0 0 1 1 1 0 1	+2
1 0 0 1 1 0 0 1 1 1 0 1 0 1	+2
1 0 0 0 1 1 0 0 1 1 0 1 1 1	+3
0 0 0 0 0 0 0 0 0 0 0 1 0 1	+2

Measured NRZ-L Output
Actual Voltage +4.9976
-5.0012

Specification Limits
±0.1% of Full Scale: ±10 mV or ±16 bits of nominal

HOUSEKEEPING A/D ENCODING ACCURACY

	Input Voltage Volts dc	Nominal NRZ-L Output In Binary MSB LSB	Decimal Equivalent	Measured NRZ-L Output			Specification Limits
				Ambient	0 °C	+60 °C	
	0.00	0 0 0 0 0 0 0 0	0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	±0.5% of full scale
	0.02	0 0 0 0 0 0 0 1	1	0 0 0 0 0 0 0 1	0 0 0 0 0 0 0 1	0 0 0 0 0 0 0 1	±1/2 LSB
*	0.50	0 0 0 1 0 0 0 1	25	0 0 0 1 1 0 0 1	0 0 0 1 1 0 0 1	0 0 0 0 0 0 0 1	= ±35 m volts
	1.00	0 0 1 1 0 0 1 0	50	0 0 1 1 0 0 1 0	0 0 1 1 0 0 1 0	0 0 1 1 0 0 1 0	
	1.50	0 1 0 0 1 0 1 1	75	0 1 0 0 1 0 1 1	0 1 0 0 1 0 1 1	0 1 0 0 1 0 1 1	
	2.00	0 1 1 0 0 1 0 0	100	0 1 1 0 0 1 0 0	0 1 1 0 0 1 0 0	0 1 1 0 0 1 0 0	
	2.50	0 1 1 1 1 1 0 1	125	0 1 1 1 1 1 0 1	0 1 1 1 1 1 0 1	0 1 1 1 1 1 0 1	
	3.00	1 0 0 1 0 1 1 0	150	1 0 0 1 0 1 1 0	1 0 0 1 0 1 1 0	1 0 0 1 0 1 1 0	
*	3.50	1 0 1 0 1 1 1 1	175	1 0 1 0 1 1 1 1	1 0 1 0 1 1 1 1	1 0 1 0 1 1 1 1	
	4.00	1 1 0 0 1 0 0 0	200	1 1 0 0 1 0 0 0	1 1 0 0 1 0 0 0	1 1 0 0 1 0 0 0	
	4.50	1 1 1 0 0 0 0 1	225	1 1 1 0 0 0 0 1	1 1 1 0 0 0 0 1	1 1 1 0 0 0 0 1	
	5.00	1 1 1 1 1 0 1 0	250	1 1 1 1 1 0 1 0	1 1 1 1 1 0 1 0	1 1 1 1 1 0 1 0	
	5.10	1 1 1 1 1 1 1 1	255	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	

H/K Channel No. 2

Serial No. 001

Data Sheet

Figure 4.7

Ref. Paragraph	Category	Ambient	0 °C	+60 °C	Specification Requirement
6.1.6.8	Dynamic Test of I/F Sub-	±1% OK 26,497 25,700	±1% OK	±1% OK	Test results indicated in paragraph 6.1.6.8

0 °C to 60 °C performance tests completed 10-19-72.

SECTION 5

HOUSEKEEPING COMMUTATOR

The housekeeping commutator multiplexes the conditioned signals from 64 monitor and control sensors installed on the instrument to the housekeeping signal input of the PCM encoder. The commutator also furnishes a six-bit parallel binary channel identification signal to the PCM encoder to identify each sensor as it is sampled. The housekeeping commutator is defined in HRC Specification No. 21008505 and is under development by Vector Aydin. It is a modified version of Vector's CSV-100 series of airborne commutators.

5.1 REQUIREMENTS

Figure 5.1 is a conceptual block diagram of the housekeeping commutator. The principal performance requirements are listed in Table 5.1.

TABLE 5.1

HOUSEKEEPING COMMUTATOR REQUIREMENTS

		REF: HONEYWELL SPEC 21008505 MFGR. - VECTOR PROD.
1.	Number of Input Channels	64
2.	Number of Poles	Single Pole
3.	Commutation Rate	912 Hz (frame rate clock from PCM)
4.	Input Signal	0 to +5V
5.	Linearity	Less than .05% Deviation from BSL
6.	Gain	.9950 to 1.0000
7.	Crosstalk	±0.1% Max.
8.	Prime Power	28 $^{+5}_{-0}$ Vdc, 0.1 A or +15V, -15V Regulated System Power
9.	Package	20 Cubic Inches 1 Pound

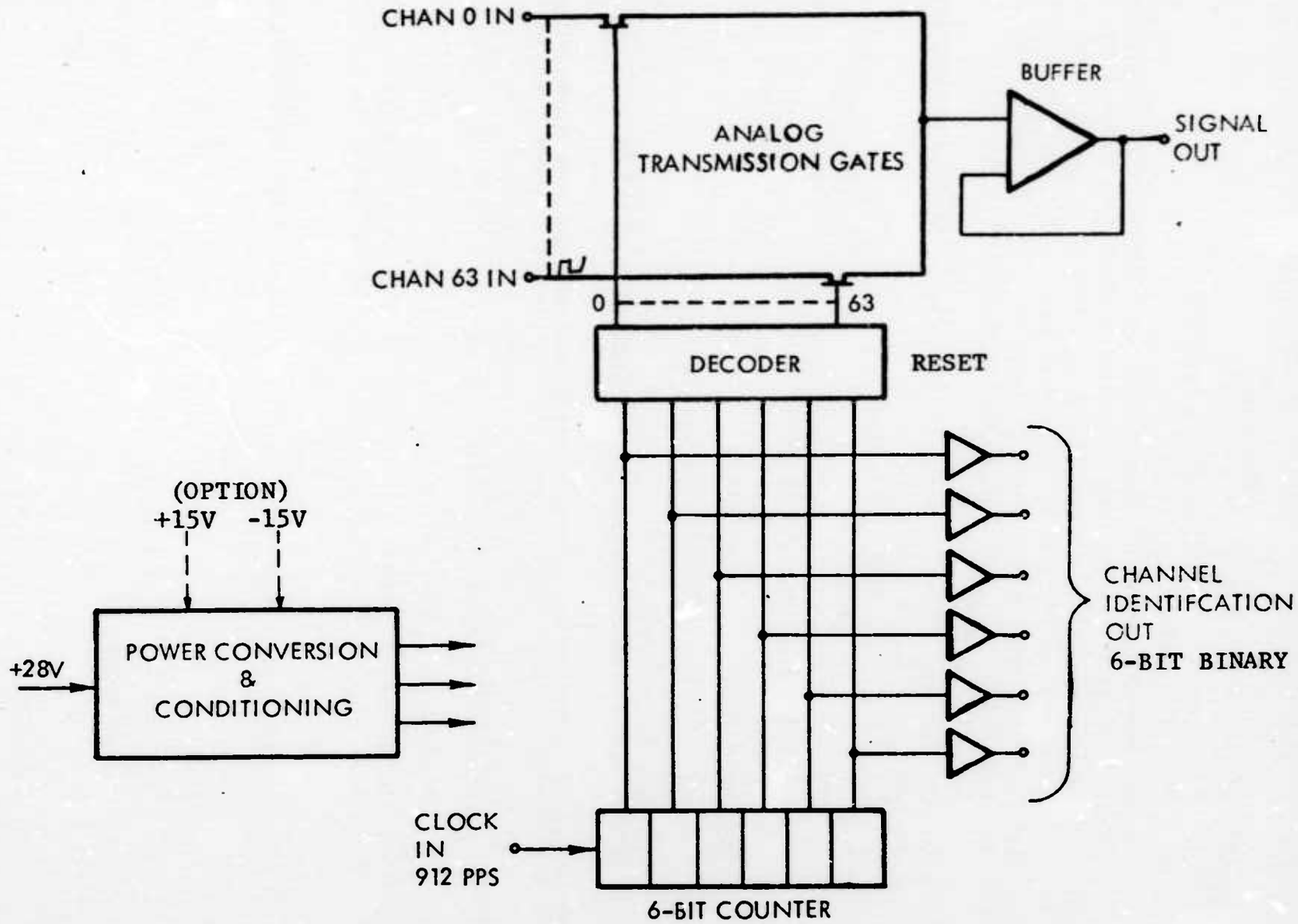

Figure 5.1 COMMUTATOR BLOCK DIAGRAM

5.2 DESIGN DESCRIPTION

The Housekeeping Commutator consists of a digital counter and decoder driving an array of 64 analog transmission gates. Conditioned input signals in the 0 to +5 V range are gated sequentially to the output buffer amplifier. The switch counter is advanced by the 912 Hz frame-rate clock from the PCM encoder.

Simultaneously, a six-bit binary channel identification counter is also driven by the 912 Hz square-wave. The parallel digital output of this counter provides the six-bit channel identification input to the PCM encoder. This permits easy association of the analog output signal at any instant with a particular sensor. This counter is maintained in synchronism with the switch counter by periodic reset pulses.

Normally, the unit develops its operating voltages using an internal power converter and conditioner from the 28 V payload batteries. However, provisions have also been incorporated to bypass the converter and to operate the commutator from the regulated +15V and -15V system supplies. This feature was included to provide an alternate power source for use in the event that the switching noise from the internal dc converter was too large.

Table 5.2 lists the various functions which are monitored by the housekeeping electronics. The photometer signal is supercommutated by strapping it to every fourth input channel so that it is sampled 16 times per commutator cycle. Since the normal channels are sampled 14.25 times per second, this results in the photometer channel being sampled 228 times per second.

Table 5.2

HOUSEKEEPING ASSIGNMENTS

	Qty.		Qty.
Dewar Cryogenic Temperature	8	Close Cover Command	1
Electronic Pkg. Temperature	2	Calibrate Command	1
Cover Position	1	ACS - Yaw	1
Dewar Vacuum	1	ACS - Pitch	1
Photometer Signal (one signal supercomm.)	16	ACS - Fine Yaw	1
		ACS - Fine Pitch	1
Photometer High Volt. Monitor	1	ACS - Roll	1
		ACS - Pressure	1
Photometer Temp. Monitor	1	Magnetometer	1
Tank Heater Control	1	Accelerometer	1
I/F Signal dc Component Lo	1	Housekeeping - Vehicle	10
I/F Signal dc Component Hi	1	Blackbody Temperature	1
28 Vdc Battery Monitor	1	Unassigned	3
+15 Vdc Monitor	1		
-15 Vdc Monitor	1	Total =	64
+5 Vdc Monitor	1		
Slide Rest Command	1		
Slide Lock Command	1		
Open Cover Command	1		

5.3 PERFORMANCE

Figures 5.2 and 5.3 summarize the performance of the housekeeping commutator. Satisfactory operational tests with the housekeeping electronics and the PCM encoder have also been conducted.

DATA SHEET FOR PAM COMMUTATOR Figure 5.1

Test	Results
Input Power & Starting	Nom 28 Vdc, 37 mA Starting Accept.
Wavetrain	Sync. Pulse: N/A O&FS Output Accept Duty Cycle: N/A Noise: Accept. Pulse Rise & Decay Time; Accept
Channel Count & Sequence	Accept;
Linearity	Step No. / Output Level (Vdc) / Step No. / Output Level (Vdc) 1 0.000 4 3.000 2 1.000 5 4.000 3 2.000 6 5.000 Linearity = ±0.00% BSL
Wavetrain Parameters vs Input Power Variations	Supply Voltage (Vdc) / Output Level (Vdc) Zero / Full / Freq. (CPS) Nom; 28 0.000 5.000 N/A Low; 24 0.000 5.000 N/A High; 33 0.000 5.000 N/A
Back Current	Microamps 0.01
Channel Scatter	±1 Millivolts
Pedestal Level	N/A Volts dc

Figure 5.2

DATA SHEET FOR CHANNEL COUNT AND
SEQUENCE MEASUREMENT OF PAM COMMUTATOR

ALL DATA CHANNELS ACTIVE
AND IN PROPER SEQUENCY: _____Accept_____

BINARY CHANNEL IDENTIFICATION OUTPUTS:

2^0 _____Accept_____

2^1 _____Accept_____

2^2 _____Accept_____

2^3 _____Accept_____

2^4 _____Accept_____

2^5 _____Accept_____

SECTION 6

GROUND SUPPORT EQUIPMENT

In order to control and monitor the experiment during prelaunch and flight phases, some data recovery facilities have been included in the HRC ground support equipment. Figure 6.1 is a block diagram showing the configuration of the system for implementing these functions.

Prior to launch the GSE control console is connected to the experiment via an umbilical cable. Any of the housekeeping sensors may be selected and monitored, the interferometer slide and cover mechanisms may be operated and the calibration sources may be turned on and off by means of this cable. The PCM encoder output is also available and is connected to a PCM decommutator. The system computer scans the reconstructed housekeeping data, compares each channel with preset limits and drives a go/no-go display. The interferometer data may be assembled to display and record an interferogram of a calibration source.

In the launch phase, the umbilical is disconnected and the PCM output is picked up on the S-band PAM telemetry link. The system computer is still able to scan the housekeeping channels, drive the go/no-go display and record the signal amplitudes on all channels, as well as assemble and record interferograms. The instrument is controlled by an on-board timer.

A Model 1023A single channel PCM decommutator was obtained from Monitor Systems. This unit is compatible with the system data format (Section 4.2) and is briefly described in the following section.

6.1 PCM DECOMMUTATOR

The Monitor Model 1023A single channel PCM decommutator offers reliability and performance consistent with the rapidly increasing sophistication of PCM requirements and provides flexibility for future expansion of additional capabilities. The Model 1023A is portable, offers single channel capability with respect to binary, decimal, and analog displays, and utilizes integrated circuits wherever possible.

6.1.1 Functional Description

As shown in Figures 6.2 and 6.3, the PCM decommutator is comprised of the following functional groups:

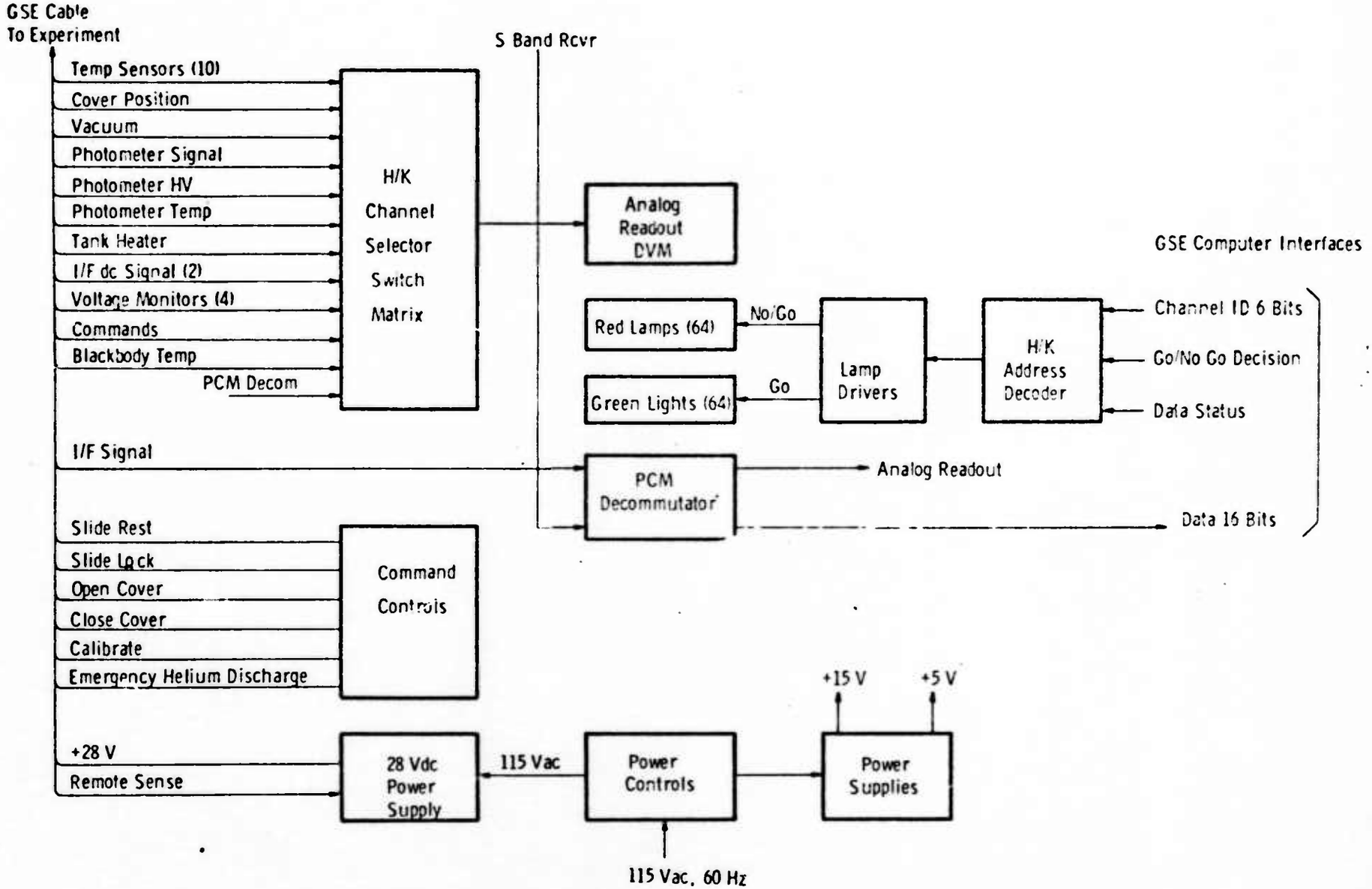

Figure 6.1 EXPERIMENT CONTROL & MONITOR

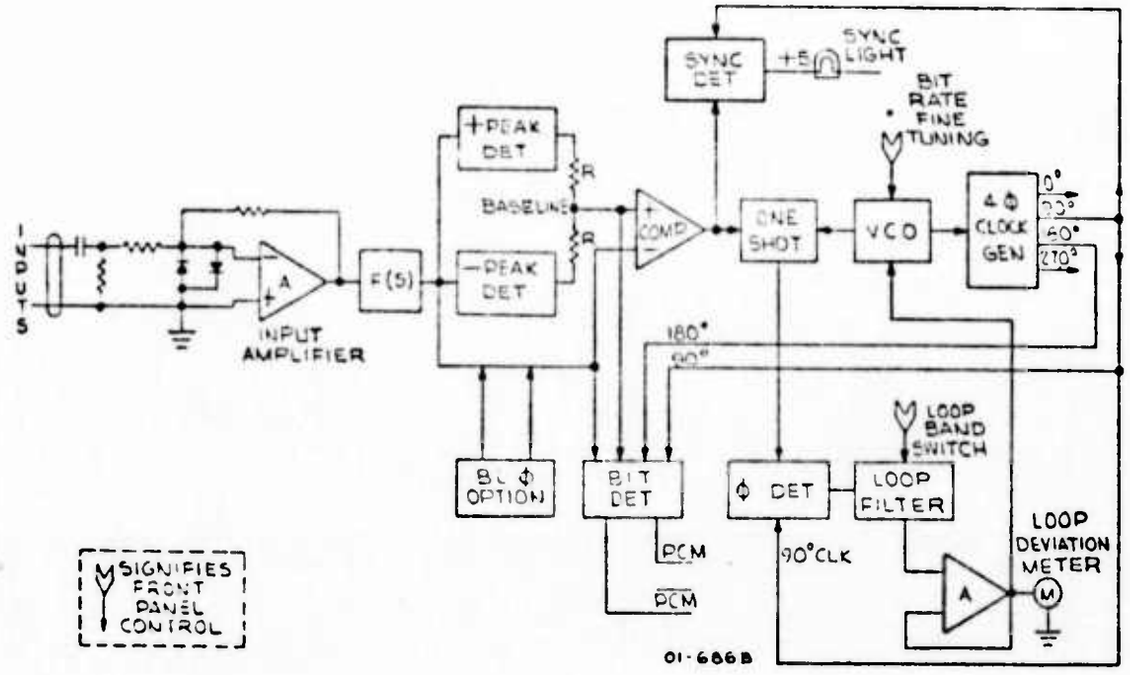

Figure 6.2 BIT SYNCHRONIZER SUBSYSTEM

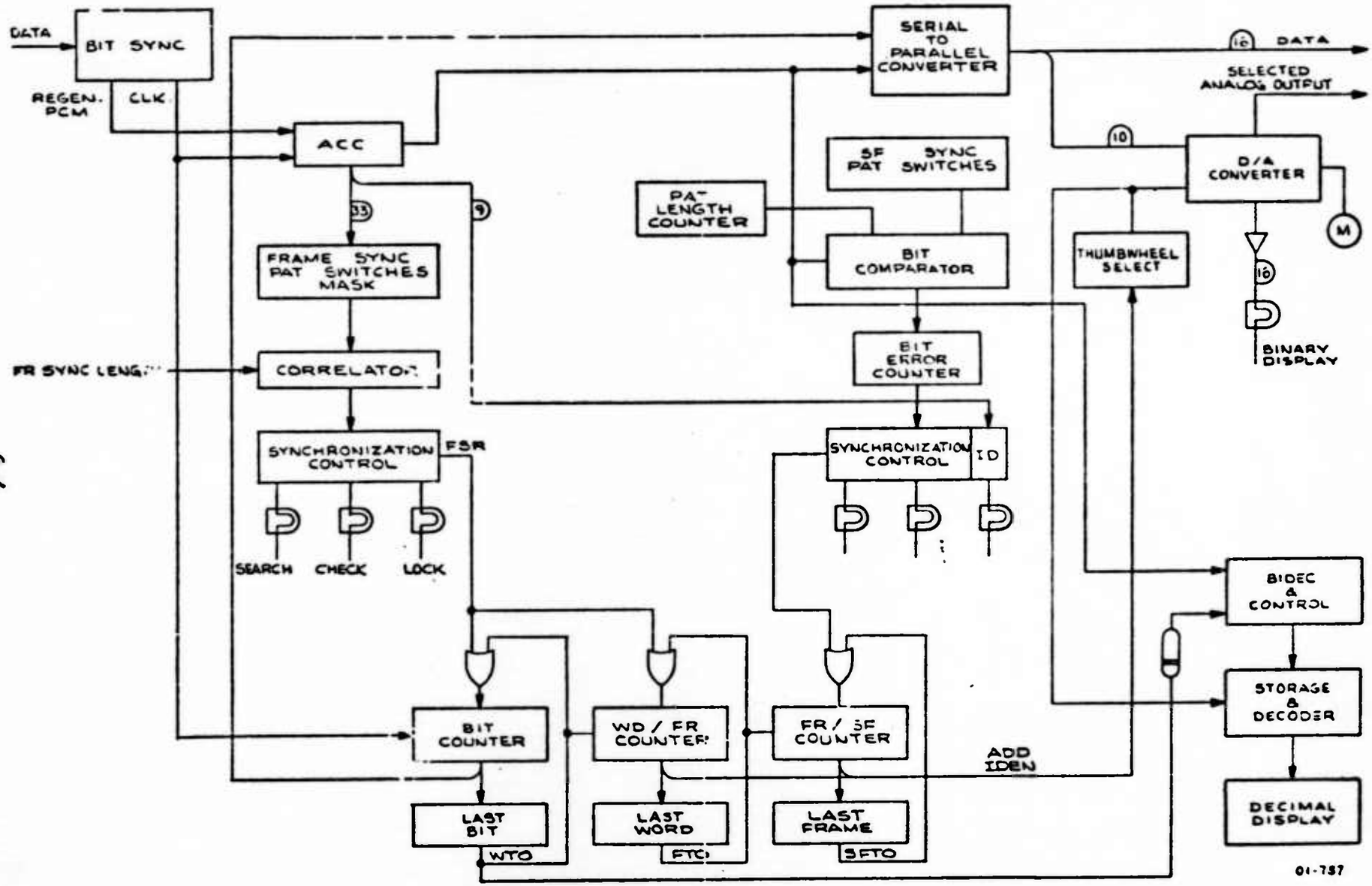

Figure 6.3 FUNCTIONAL BLOCK DIAGRAM

- Bit synchronization
- Format synchronization
- Serial-to-parallel conversion
- Single channel display
- D/A conversion

The Bit Synchronizer accepts a serial PCM input from a commutator, tape recorder, or simulator. This input is regenerated and a coherent clock is reconstructed from it. The synchronizer accepts NRZ or Bit serial data at customer specified bit rates. The output clock and data are presented to the format synchronizer. No additional plug-in units are required for operation.

The format synchronizer accepts the conditioned serial PCM data and clock signals at the input bit rate. The unit synchronizes the output data with the vehicle commutator by recognizing predetermined patterns in the data. The format synchronizer compensates for noise in the transmission line by synchronization flywheel circuitry, with error tolerance selectable. The Format Synchronizer presents a parallel bus of up to 24 bits, either MSB or LSB justified, along with identifying time slots of frame and subframe.

By means of front panel thumbwheel switches, a selected data channel is stripped and routed to front panel displays. A sixteen-bit binary, a three-digit decimal and an analog display are provided.

Digital and analog data outputs are provided at the rear connector.

6.1.2 PCM DATA AND CLOCK REGENERATION SUBSYSTEM

The operation of the system is as follows: the input signal first passes through a unity gain buffer amplifier which provides the necessary input impedance and also the drive for the filter. The peak detection circuitry establishes the true signal baseline at midway between the peak-to-peak signal. The filter output is then compared against the true signal baseline and the comparator output supplies a +5 volt logic level for signals above the baseline and ground level for signals below the baseline. The comparator output, therefore, has transitions every time the input crosses its true baseline. Figure 6.2 depicts the functional logic flow of the Bit Synchronizer Subsystem.

The latter transitions are used for two purposes. The first usage is for establishing the phase-locked clock sync. The transitions trigger a one-shot multivibrator which is compared against the local clock. The phase error is fed through the loop filter and controls the VCO frequency to establish Lock. The VCO center frequency is tuneable over a 29% range by a front panel potentiometer. Either a wide or narrow loop band can be selected for handling jittery signals or long data gaps, respectively. The transitions are also compared against the local clock in the sync detector circuitry and a statistical average of in-phase and out-of-phase transitions yields the in- or out-of-sync signal. The phase-locked clock is then used in the bit detection circuitry to determine if the bit value is a "one" or "zero". A full bit Bit option is also incorporated in the bit detector.

6.1.3 FRAME SYNCHRONIZER

Figure 6.3 shows the general data flow of the frame synchronizer. Except for the frame sync correlator, all techniques of corresponding functions are essentially the same as those employed in MONITOR's field-proven line of PCM Decommutation Systems.

The serial NRZ-L Data from the bit synchronizer is presented to a 33-bit accumulator which is used exclusively in conjunction with the frame sync pattern detector. Also, this data is available for input to the recycle and ID subframe synchronizer, as described below.

The criteria for frame synchronization are determined via the frame sync correlator which has, as its inputs, both programmed and data dependent parameters. The correlator incorporates a technique which is entirely digital, and includes pattern detection during the Search mode which is characterized by the occurrence of that pattern with the highest correlation to the programmed sync code.

When the synchronizer is in the Search mode an analysis is performed which occupies less than 200 nanoseconds (worst case). Processing within the correlator is essentially asynchronous, depending wholly upon gate delays.

When the synchronizer is in the Check or Lock mode, the strategy for achieving and maintaining Lock is determined by front panel controls. The total number of allowable bit errors may be pro-

grammed independently in each mode of operation. Up to nine patterns may be examined in the Check mode before a decision is made to switch to the Lock mode and up to nine sequential erroneous patterns may be allowed in the Lock mode before a decision is made to revert back to the Search mode.

The handling of recycle subframe synchronization (Search, Check, and Lock mode) is very much the same as for frame sync. Because the location of the sync pattern is "known" via the frame sync address, the comparison is made on a bit-by-bit basis.

Counters are provided to determine when the wavetrain should be examined for synchronization codes and to provide time slot information to accompany the output data. These counters are 1 to 33 bits-per-word, 1 to 999 words-per-frame and 1 to 512 frames-per-subframe counter. The modulus of each counter is programmed by front panel thumbwheel switches.

6.1.4 DATA OUTPUTS AND DISPLAYS

Front panel displays are provided and controlled by thumbwheel switches. Data is selected and displayed by sixteen incandescent indicators. The same data value is converted to decimal, for display with a maximum count of 9999. The equivalent value is also displayed on the analog meter.

The output of the data value is converted to analog and presented at a type BNC connector on the rear panel. Digital data is available in a multi-pin connector, also located on the rear panel.

The analog output voltage levels are 0 to +10 vdc, with a resolution of eight or ten bits for the data value. Output drive capability is 10 ma at full scale (100 ma optionally available). Logic levels for the digital outputs are 0 and +4.5 volts ±1 volt.

Frame and subframe synchronizer patterns, pattern word length, and data length are programmed by means of toggle switches which are available on a mini panel, located on top of the unit. Access to this panel, when the unit is rack-mounted, may be accomplished by partially withdrawing the unit from the rack (about five inches).

TABLE 6.1

PCM DECOMMUTATOR SPECIFICATIONS

INPUT

Input Data Code	Serial NRZ or Biφ
DC Offset	Up to 100% of peak-to-peak signal amplitude
Data Level	1-20 volts peak-to-peak without adjustment
Bit Rate	1-512 Kbps (customer specified)
Input Impedance	15 K ohms shunted by 150 pF
Loop Bandwidth	0.1% narrow 3% wide

FORMAT

Sync Word Lengths	1-33 bits
Data Word Lengths	1-31 bits
Frame Length	2-999 words
Subframe Length (Pattern)(Optional)	2-999 frames
Subframe Length (ID) (Optional)	2-512 frames
Frame Sync Length	Any binary pattern up to 33 bits
Frame Sync Types	Normal and alternating complementary patterns
Modes	Search, Check and Lock
Subframe Sync Pattern Length	Up to 33 bits
Synchronization Types	Frame code complement Unique recycling patterns - Frame counting (ID) sync, up to 9 bits, start at "0" or "1" count

DISPLAYS

Binary	Up to 16 bits
Decimal (Optional)	9999 maximum reading 3 or 4 digit option
Analog (Optional)	Meter indication
Accuracy	8-bit D/A converter 10-bit D/A optional
Selection	Thumbwheel type front panel switches

Table 6.1 (cont)

OUTPUTS

Data	(1)	16-bits parallel, NRZ-L positive true, MSB or LSB justified. (24-bit option)
	(2)	Serial NRZ-L, positive true.
Data Identifier		12-bit word number 12-bit frame number All outputs BCD, positive true.
Timing Pulses	(1)	Bit Rate Clock, 1/4-bit wide, positive true
	(2)	Word Rate
	(3)	Frame Rate
	(4)	Subframe Rate
		(All of above are one bit wide, positive true, coincident with last bit of format element).
Levels		0 volt to 0.5 volt negative level - +4.5 volts ±1 volt positive level

PHYSICAL SPECIFICATIONS

Mounting	Slide Mounts in standard 19-inch panel opening
Dimensions	5 1/2" x 19" x 23"
Input Power	108 to 132 volts, 57-63 Hz, 2 amp 57-400 Hz option.
Temperature	Operating: 0°C to +60°C Non-operating: -40°C to +85°C
Weight	45 pounds

6.2 GSE COMPUTER INSTALLATION

Figure 6.4 is a pictorial sketch of the GSE computer installation. The Digital Equipment Corp. PDP-11 computer rack contains the PDP-11 central processor with 32k of core memory, a dual DECTAPE unit, Direct Memory access unit DR11-13, and 3 general purpose interface cards DR11-A.

A Tektronix 4010-1 display scope and keyboard is used to control the PDP-11 and provides fast displays of computer output. A Tektronix 4610 Hard Copy Unit in the rack provides page size copies of any computer generated displays desired.

In addition to driving the go/no-go display panel, the computer can provide a display of the values of all housekeeping functions on command. It can also record a complete interferogram from either the internal calibration sources or external sources during flight. These may be plotted on the display scope in their entirety or selected segments may be enlarged and plotted. On command an FFT of the interferogram may be computed and plotted. Again the entire spectrum or a selected segment may be displayed.

Figure 6.5 is a flowgraph of the GSE Software developed for the experiment.

The GSE computer and its software may be used for data reduction of the recorded telemetry data after the flight is completed.

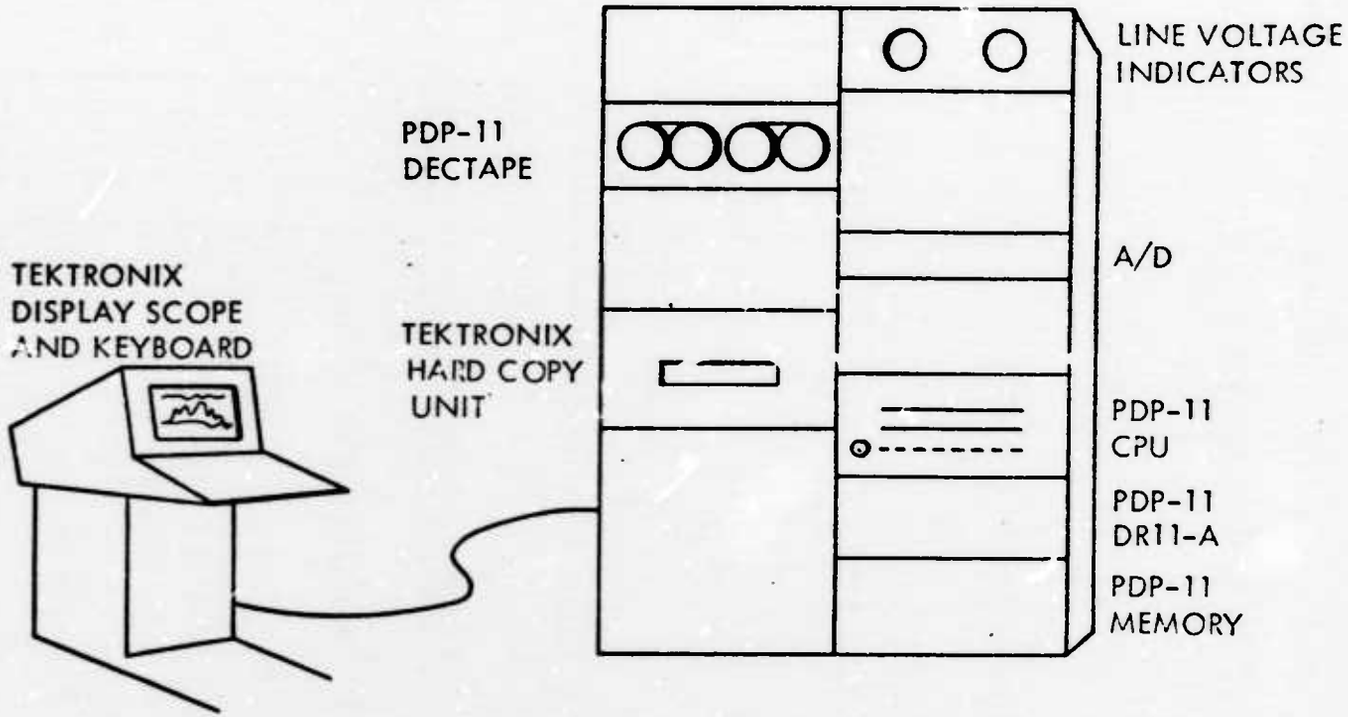

Figure 6.4 GSE COMPUTER INSTALLATION

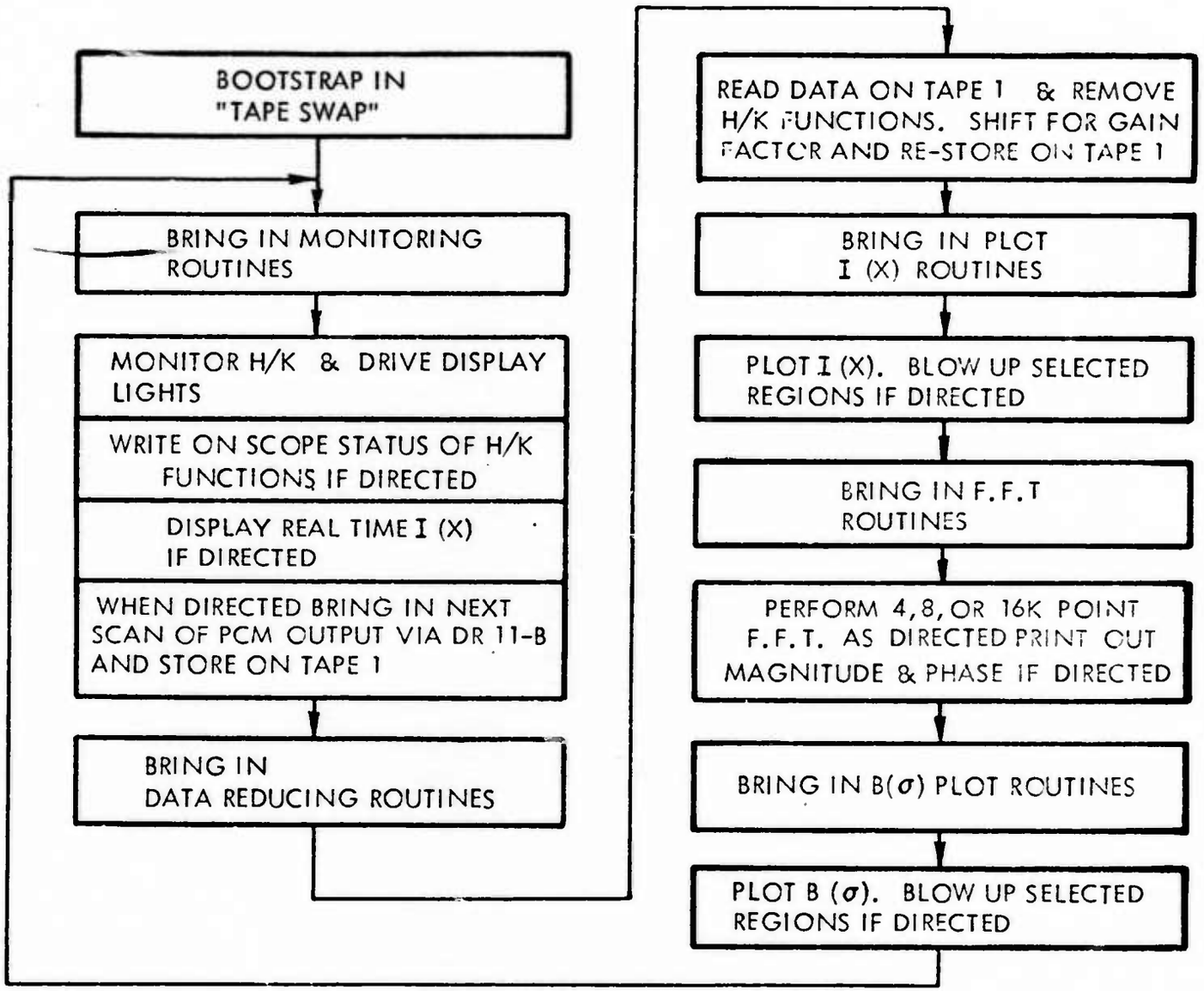

Figure 6.5 GSE SOFTWARE FLOW GRAPH

APPENDIX A

PCM ENCODER SPECIFICATION

INTERPRET DRAWING IN ACCORDANCE WITH MIL-D-1000, FORM 3

HONEYWELL PART NO.

21008493-101

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	[illegible]	6/15/72	[illegible]
B	REVISED PER MARKED PRINT	10 Jan 73	[illegible]
C	REVISED PER MARKED PRINT	[illegible]	[illegible]
D	REVISED SHTS 4, 10 & 11	2 Jan 73	[illegible] LBH
E	RELEASED TO LEVEL B	6/28/73	[illegible] LBH
F	REV SHTS 4,5,6,7,14&17	13 Mar 74	4-222

SIZE	A	A	A	A	A	A	A	A	A	A	A	A	A	A	B	B	E
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
REV	F	E	E	F	F	F	F	E	E	E	E	E	E	F	E	E	F

TOLERANCES UNLESS NOTED OTHERWISE				
X ±.1	ANGLES	DRAFTSMAN	[illegible]	6/15/72
XX ±.02	±	CHECKER		
XXX ±.010		PKG ENGR		
		DEV ENGR	E. DUWEMA	6/15/72
EPA		PROJ ENGR	[illegible]	6/15/72
FINISH—SEE NOTE		RELIABILITY	[illegible]	[illegible]
MATERIAL		ELEC ENGR	L. Hankins	6/15/72
		ENGRG RCD RLSE	Cannon	8/28/73
		CONTRACT NO.		
		HIRIS		

HONEYWELL INC.
RADIATION CENTER
LEXINGTON, MASS.

PCM ENCODER

SIZE	CODE IDENT NO.	DRAWING NO.
A	81395	21008493

SCALE	/	WT		SHEET 1 OF 17

HRGD-71

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A		6/15/72	
E	UPGRADED TO LEVEL B	8/28/73	

1.0 SCOPE

This document establishes the requirements for a Pulse Code Modulation (PCM) Encoder. The PCM Encoder, referred herein as the encoder, consists of sample and hold, A/D conversion, buffer, gate, clock, and serializer type functions.

2.0 APPLICABLE DOCUMENTS

MIL-STD-454B	Standard General Requirements for Electronic Equipment, dated 10 June 1968
MIL-STD-461A	Electromagnetic Interference Characteristics, Requirements for Equipment, dated 1 August 1968
ER-69538	Environmental Specifications for Black Brant Payloads and Instrumentation, dated 25 March 1971, Bristol Aerospace Limited

3.0 REQUIREMENTS

3.1 Description and Intended Use

The encoder shall accept analog input signals from an infrared interferometer and its housekeeping sensors, sample these signals at 26,000 samples per second, convert to 14 bit binary, insert coding, and arrange the output into a continuous digital pulse stream of 466,944 bits per second in 16 bit word format for telemetering. The NRZ-L output waveform from the encoder is fed to a S-Band telemetry transmitter. The encoder shall include all necessary timing and power conversion circuitry.

SIZE	CODE IDENT NO.	
A	81395	21008493
SCALE	WT	SHEET 2 OF

HRC10-71

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A E	RELEASED TO LEVEL B	6/15/72 9/28/73	

The encoder is part of an instrument payload for the Black Brant V high altitude research rocket. The rocket will be launched from an Arctic environment.

3.2 General Design Requirements

The encoder shall be as free as feasible of any defects in materials, processes, manufacture, or design which could conceivably degrade the performance or reliability of the encoder Wherever possible, the encoder shall utilize existing circuits and components which have proven performance and reliability in similar applications. Where new design is required, MIL-STD-454 shall be used as a guide in selecting materials, parts, and processes. All selections shall be compatible to the intended use of the encoder.

3.3 Design Review

A design review shall be held at the suppliers' facility with Honeywell representatives, to review design features, interfaces, and expected performance. All interfaces shall be frozen at this time. This review shall be scheduled by the supplier to occur prior to any significant commitment of manufacturing labor or material. One week notice is required.

3.4 Electrical Requirements

3.4.1 Encoder Block Diagram

Figure 1 is a conceptual block diagram of the encoder showing the essential elements. This is furnished for reference only as an aid to describing the encoder requirements and should not be construed as a requirement on the actual structure.

SIZE	CODE IDENT NO.	
A	81395	21008493
SCALE	WT	SHEET 3 OF

HAC10-91

120<

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A		6/15/72	
B	REVISED PER MARKED IT	10 Jan 73	
C	0.67 WAS 0.9		LH
D	2048 WAS 512	2 Jan 73	LBH
E	RELEASED TO LEVEL B	8/28/73	
F	PARA 2 0.9 WAS 0.67	13MAR74	4-222

Basically, the encoder shall convert the input interferometer (I/F) data to a 14 bit parallel binary digital signal under control of an external signal (Sample Command In) and shall include means such as a 2 bit storage register for storing the logic level of two input signals existing during the sample interval of the Sample/Hold element and for associating these 2 bits with the converted digital word representing that sample.

An asynchronous Buffer Memory shall be provided which is capable of compensating for expected variations in the 26,000 Hz sample rate during each 0.9 second I/F data Period. This buffer shall have a memory capacity of 2048 16 bit words.

The encoder shall also convert the input housekeeping (H/K) data to an 8 bit parallel binary digital signal under control of an internally generated command once per 32 word frame and shall also include means such as a 6 bit storage register for storing the 6 bit binary channel identification from the housekeeping subcommutator and for associating these 6 bits with the converted digital word representing that sample. Two zeros shall be loaded in, to complete the 16 bit word.

A 10 bit binary Sweep Counter shall also be provided. This counter will be incremented on the positive going transitions of the Mode Command signal.

A Bit Rate Clock operating at 466,944 Hz shall be provided. Suitable binary divider chains and decoders shall also be provided to develop the necessary Word Rate and Frame Rate signals and internal control and gating pulses. These counters shall be of the synchronous type to minimize spurious output from the decoders and possible clock skew problems.

An assembler shall be provided in the encoder which will format the digital data as specified in paragraph 3.4.4.2.

SIZE	CODE IDENT NO.	
A	81395	21008493
SCALE	WT	SHEET 4 OF

HAC16-91

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A C E	REVISED PER MANUAL POINT RELEASED TO LEVEL B	6/15/72 12-4 8/28/73	[illegible] 11/LH
F	LAST PARA 2ND LINE 2,200 WAS 3100	13 Mar 74	4-222

A serializer shall be provided to convert the 16 bit parallel binary words to a continuous serial binary signal. This will be appropriately filtered and buffered to provide the PCM Output signals for the transmitter and recorder/decoder.

Power conversion and conditioning circuits shall be included in the encoder. Nominal 28-volt battery power will be supplied.

3.4.2 Logic Interfaces

All digital input and output control and timing signals are required to be compatible with TTL logic. The encoder shall present only one standard TTL logic load to each digital input signal and each digital output line shall be driven by a separate buffer. The remaining system components will be similarly buffered and will present only one standard TTL logic load to each digital output line from the encoder.

The bi-level data values are assumed to be:

Binary "0" = 0 V $\pm \begin{matrix} 0.5 \text{ V} \\ 0 \text{ V} \end{matrix}$

Binary "1" = 24 V to 5 V

3.4.3 Input Signal Characteristics

3.4.3.1 Interferometer Analog Data

Amplitude: -5 to +5 volts

Data Bandwidth: The encoder shall process input analog data in the frequency range from dc to 2,200 Hz with no degradation beyond the limits of this specification.

SIZE	CODE IDENT NO.	
A	81395	21008493
SCALE	WT	SHEET 5 OF

NAC10-91

1224

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A C E	.754 WAS 1, 0 67 WAS 0.9 & 0.084 WAS 0.1 RELEASED TO LEVEL B	6/15/73 12-4 8/28/73	[illegible]
F	1.0 WAS .754; 36.7 WAS 37.8; 41.5 WAS 39.2; 0.9 WAS 0.67 & 0.1 WAS 0.084	13 MAR 74	4-222

Active Period: 90% of each 1.0 second scan of interferometer

Signal Preamp Output Impedance: less than 1 ohm

3.4.3.2 Housekeeping Analog Data

Amplitude: 0 to +5 volts

Bandwidth: Slowly varying DC voltages from numerous sensors attached to experiment package. Commutated continuously at telemetry output frame rate.

Commutator Output Impedance: 500 ohms

3.4.3.3 Sample Command

This is a positive logic trigger pulse used to initiate the sample/hold and A/D conversion sequence. Nominal pulse width is one microsecond. Pulse spacing is derived from the zero crossings of a laser reference signal during the I/F data period and may vary between 36.7 and 41.5 microseconds. Nominal spacing is 38.5 microseconds (PRF of 26 kHz). Sampling and conversion is to be initiated on the leading edge of each pulse.

3.4.3.4 Mode Command

This is a digital control signal used to switch the system from the Interferometer Scan Mode to the Flyback Mode. The logic one state corresponds to the I/F scan mode and the logic zero state corresponds to the F/B mode. This signal will nominally be in the I/F scan mode approximately 0.9 seconds and the F/B mode 0.1 second, but may also be locked in the F/B mode for tests on the housekeeping electronics.

SIZE	CODE IDENT NO.	
A	81395	21008493
SCALE	WT	SHEET 6 OF

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A C E	ENGINEERING CONTROLLED RELEASE 0.67 WAS 0.9 RELEASED TO LEVEL B	6/15/72 12/[illegible] 8/28/73	[illegible]
F	2nd Pass Level 4 0.9 was 0.67	13 Mar 74	4-222

3.4.3.5 Gain State

This is a logic signal indicating one of two possible gain states for the signal processing amplifier. The amplifier and this signal are inhibited from switching during the encoder sample time. The logic level of the signal is to be strobed into an auxiliary register during the sample time, and is part of the digitized output word corresponding to that sample (bit 15).

3.4.3.6 White Light Reference Status

This is a logic signal which is used to indicate detection of the reference signal during the I/F scan period. It switches from a logic zero level to a logic one level near the center of the I/F scan period (0.9 sec). It is reset to a logic zero level during the F/B interval.

This signal level is also strobed into an auxiliary register during the sample time and becomes bit 16 of the PCM data word representing that particular sample.

3.4.4 Output Signal Characteristics

The encoder shall provide two types of output signals: (1) specific rate signals from the internal counter chain, and (2) the serial binary signal for the telemetry transmitter. Protection shall be provided on all output signal lines to prevent damage if an output is shorted to ground.

SIZE	CODE IDENT NO.	
A	81395	21008493
SCALE	WT	SHEET 7 OF

NRC10-71

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	ENGINEERING RELEASED	6/12/72	
B	REVISED PER MARKED PRINT	10/ /72	
C	±2.5V WAS LOGIC LEVELS	2/ /73	
E	RELEASED TO LEVEL B	8/28/73	

3.4.4.1 Logic Clock Signals

The encoder shall provide the following clock signals as symmetrical square wave outputs with the positive transitions corresponding to the leading edge of the event:

Bit Rate	466,944 Hz
Word Rate	29,184 Hz
Frame Rate	912 Hz

3.4.4.2 PCM Output Signal

The output signal for telemetry shall first pass through a pre-modulation filter, having a -3 db response at 327 kHz and a roll-off of 36 db/octave to 60 db down. The signal shall be at ±2.5 V and shall correspond to the NRZ-L mode.

Figure 2 illustrates the required format of the PCM output signal.

Each frame will consist of 32 binary words of 16 bits. The synchronizing character at the beginning of each frame is a 22 bit Barker code sequence. This extends into the second word. The remaining 10 bits of the second word are from the 10 bit Sweep Counter arranged with the most significant bit (MSB) first and least significant bit (LSB) last. The third word in each frame is a sub-commutated housekeeping channel and contains the 8 bits from the housekeeping A/D converter, MSB first, followed by two filled-in zeros, followed by the 6 bits of sub-channel identification, MSB first.
The remaining twenty-nine words in each frame are interferometer data. The first 14 bits of each word are from the 14 bit A/D converter arranged MSB first. Bit 15 is the amplifier gain bit and bit 16 is the white light zero reference bit associated with that sample.

SIZE	CODE IDENT NO.	
A	81395	21008493
SCALE	WT	SHEET 8 OF

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	ENGINEER[illegible] RELEASED	6/15/72	
B	REVISED PER MARKED PRINT	10[illegible]	
C	REVISED PER [illegible] PRINT	12[illegible]	
E	RELEASED TO LEVEL B	8/28/73	

There are 64 sub-channels which are commutated in word three. Each channel is sampled 14.25 times per second by the housekeeping sub-commutator.

When the system has switched from the scan mode to the flyback mode and the data buffer is empty, the 29 data words are each filled with 16 alternating ones and zeros. All even bits shall be ones, and all odd bits shall be zeros. These fill-in characters are sent until the system has again switched to the scan mode and the data buffer has been loaded.

3.4.4.3 Buffered PCM Output Signal

This output shall be identical to the signal used for telemetry, except that it bypasses the pre-modulation filter and has a line driver capable of driving a 50 ohm coaxial cable.

3.4.4.4 Sample Pulse

The logic control pulse defining the "ON" period of the actual sample operation of the I/F data sample/hold amplifier shall be provided as an output.

3.4.5 Accuracies and Tolerances

In addition to the tolerances and levels already discussed, the encoder shall meet the following performance levels.

3.4.5.1 Absolute Accuracy: ±0.1% of the full scale set point referenced to the NBS voltage standard for the I/F data, and 0.5% for the H/K data.

3.4.5.2 Encoding Accuracy: ±0.5 LSB

3.4.5.3 Linearity: I/F linearity, less than ±0.01% departure from BSL.

H/K linearity, less than ±0.5% departure from BSL.

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REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	ENGINEERING RELEASE	6/16/72	
B	REVISED PER MARKED PRINT	10 Jan 73	
C	REVISED PER MARKED PRINT	12 Jan 73	
D	DELETED ¶ 3.4.7 & 3.4.7.1	26 Jan 73	
E	RELEASED TO LEVEL B	8/28/73	

3.4.5.4 Temperature Coefficient: Less than 10 μv/°C referenced to the input.

3.4.5.5 Bit Rate Stability: At least ±0 1% at the 466,944 Hz clock.

3.4.5.6 Crosstalk: Less than .02% of full scale between the I/F and H/K data inputs, if the same A/D converter is used.

3.4.6 Prime Power and Grounding

The encoder shall operate to full performance specification when connected to a power source of 28 VDC $^{+5}_{-0}$ VDC. Current drain shall not exceed 200 ma. Reverse polarity protection shall be provided on the 28 V line. Signal, power, and chassis grounds shall be mutually isolated.

3.5 Mechanical Requirements

3.5.1 Size and Weight

The encoder shall occupy less than 100 cubic inches, and shall weigh less than 7 pounds (goal). The exact dimensions and configuration shall be agreed upon at the design review, but shall comply with space allocation limits shown in Figure 3.

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REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	ENGINEERING RELEASE	6/15/72	
C	REVISED PER MARKED PRINT	12/27/72	
D	P3.5.4 - SENTENCE WAS "IRRIDITE COATING"	2 Jan 73	LH
E	RELEASED TO LEVEL B	8/28/73	LH

3.5.2 Connectors

All external connectors shall be mounted on one side wall of the encoder. Each connector shall be noninterchangeable with the others. Selection and application of connectors shall comply with Requirement 10 of MIL-STD-454. Connector part numbers and pin assignments shall be agreed upon at the design review. Mating connectors shall be provided for all external connectors on the encoder. The mating connectors, cable harness type, shall be delivered to Honeywell at least two weeks prior to delivery of the encoder.

3.5.3 Mounting

The encoder shall be designed to mount directly into the rocket instrumentation section by complying with the interface requirements shown in Figure 3.

3.5.4 Finish

Black anodize, appropriately masked.

3.5.5 Marking

Each external connector shall be given a reference designation. A nameplate shall be mounted on the top surface of the encoder, and shall include at least the following information:

PCM Encoder
Mfgr and P/N
Honeywell P/N
Serial Number and Date

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3.5.6 Workmanship

As a minimum, workmanship shall comply with Requirement 9 of MIL-STD-454. The encoder shall be assembled to workmanship standards consistent with flight hardware.

3.6 Environmental Conditions

The encoder shall be designed and constructed to operate to full performance standards under any combination of the following environmental conditions:

3.6.1 Temperature: 0 °C to +60 °C operating
-50 °C to +60 °C storage

3.6.2 Vibration: a) 7.5 g peak 2000 to 27 Hz
b) 0.2 inch double amplitude displacement for 27 to 15 Hz.

A 115 second logarithmic sweep in any axis, starting at the high frequency end and having no dwell time during the sweep.

3.6.3 Spin: 5 rps, 8 inch radius, for 16 minutes

3.6.4 Altitude: sea level to 250 kilometers

3.6.5 Acceleration: 50 g for one minute, any axis

Environmental behavior of the Black Brant series of rockets is detailed in ER-69538, referenced herein as a guide.

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A	81395	21008493
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REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	ENGINEERING CONTROLLED RELEASE	6/15/72	
E	RELEASED TO LEVEL B	8/28/73	

3.7 Electromagnetic Interference (EMI)

The encoder shall be designed and fabricated to pass the interference and susceptibility requirements for Class ID of MIL-STD-461. Undesired switching transients and timing pulses shall be removed from input and output lines. Shielded wire shall be used where applicable. Any nonconductive finish shall be suitable masked under mating surfaces to maintain good metal to metal contact. EMI control techniques shall be thoroughly reviewed at the design review.

4.0 PRODUCT ASSURANCE PROVISIONS

4.1 General

The supplier shall apply a quality control system in the inspection and testing of this device which will result in high assurance of compliance with all requirements of this specification.

4.2 Acceptance Test Plan (ATP)

An informal test plan shall be submitted to Honeywell for approval at least three weeks prior to test. This plan shall delineate test conditions, test techniques and test criteria for demonstrating the performance requirements in paragraph 3.4 herein. In the event the PCM Decoder and/or the Housekeeping Commutator are also procurred from the same supplier, he shall further test the group as a subsystem, prove compatible integration, and provide test plan for doing same.

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A E	ENGINEERING RELEASED TO LEVEL B	6/15/72 8/28/73	
F	ADDED 5.0	13 Mar 74	4-222

4.3 Pre-Shipment Acceptance Testing

The encoder shall be source inspected at the suppliers' facility by Honeywell personnel. One week notice is required. The approved ATP shall be demonstrated to Honeywell's satisfaction. Environmental and EMI testing is not required; however, Honeywell reserves the right to reject the equipment if it is later proven not to comply with all requirements of this specification. Mechanical requirements will be visually inspected or verified from earlier inspection records. Three copies of all test and inspection data shall be delivered with the hardware.

5.0 NOTES

Approved Vendor: Vector Aydin
Newtown, PA
Moeel EMV-113

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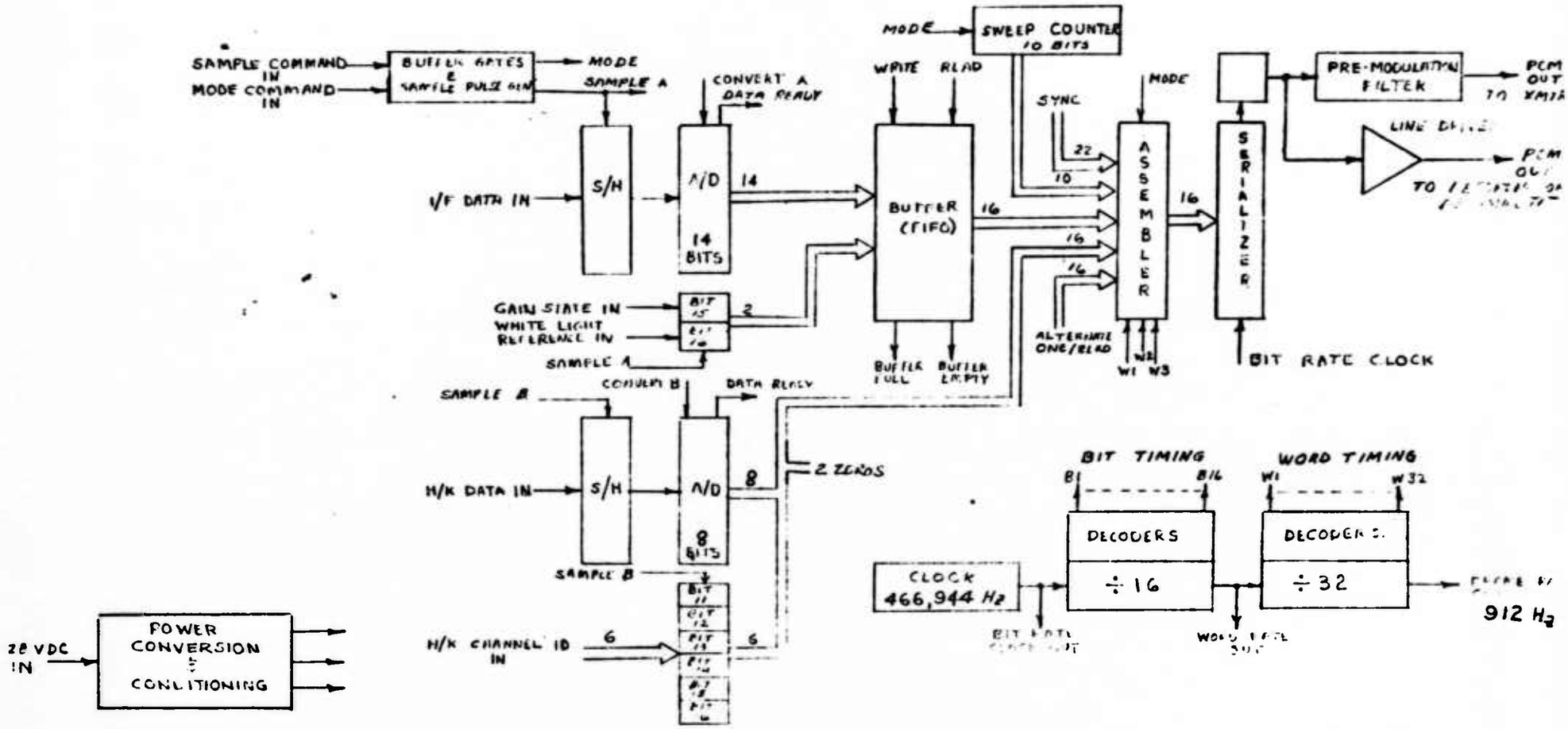
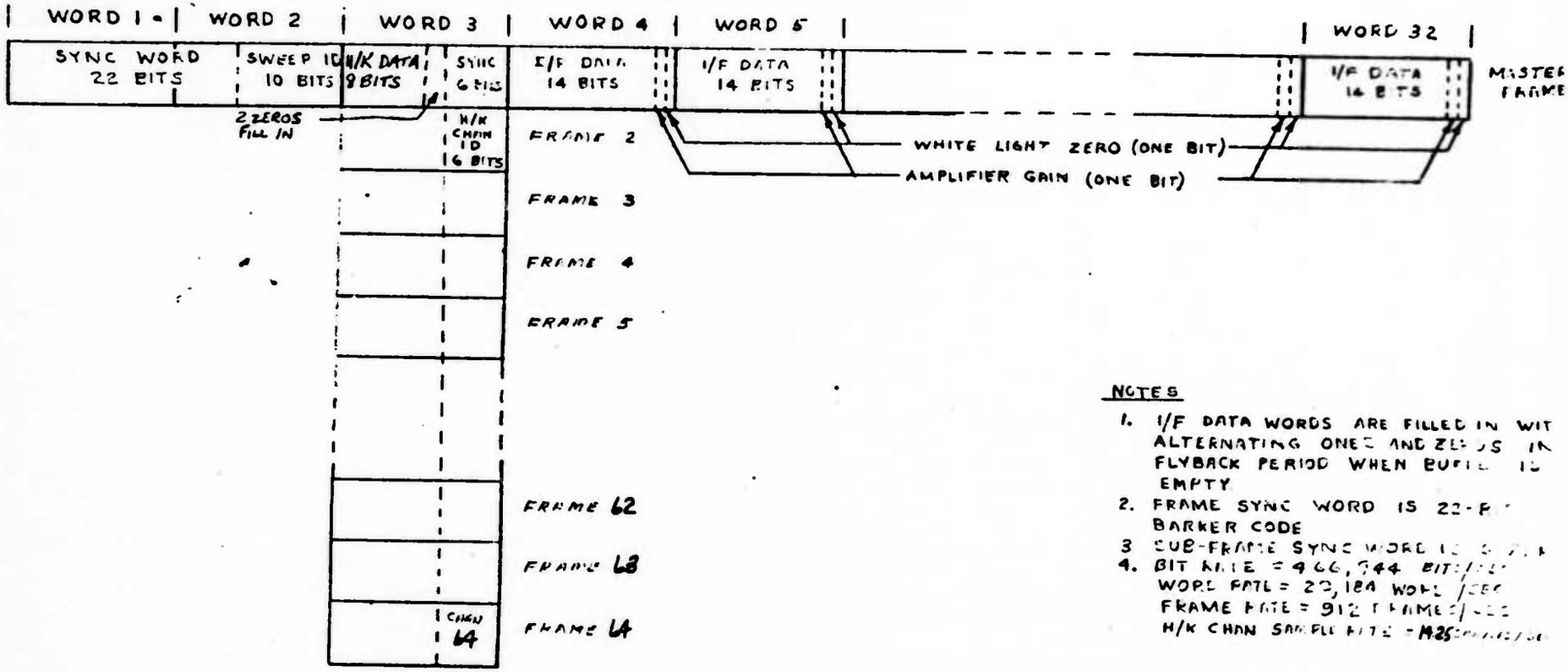


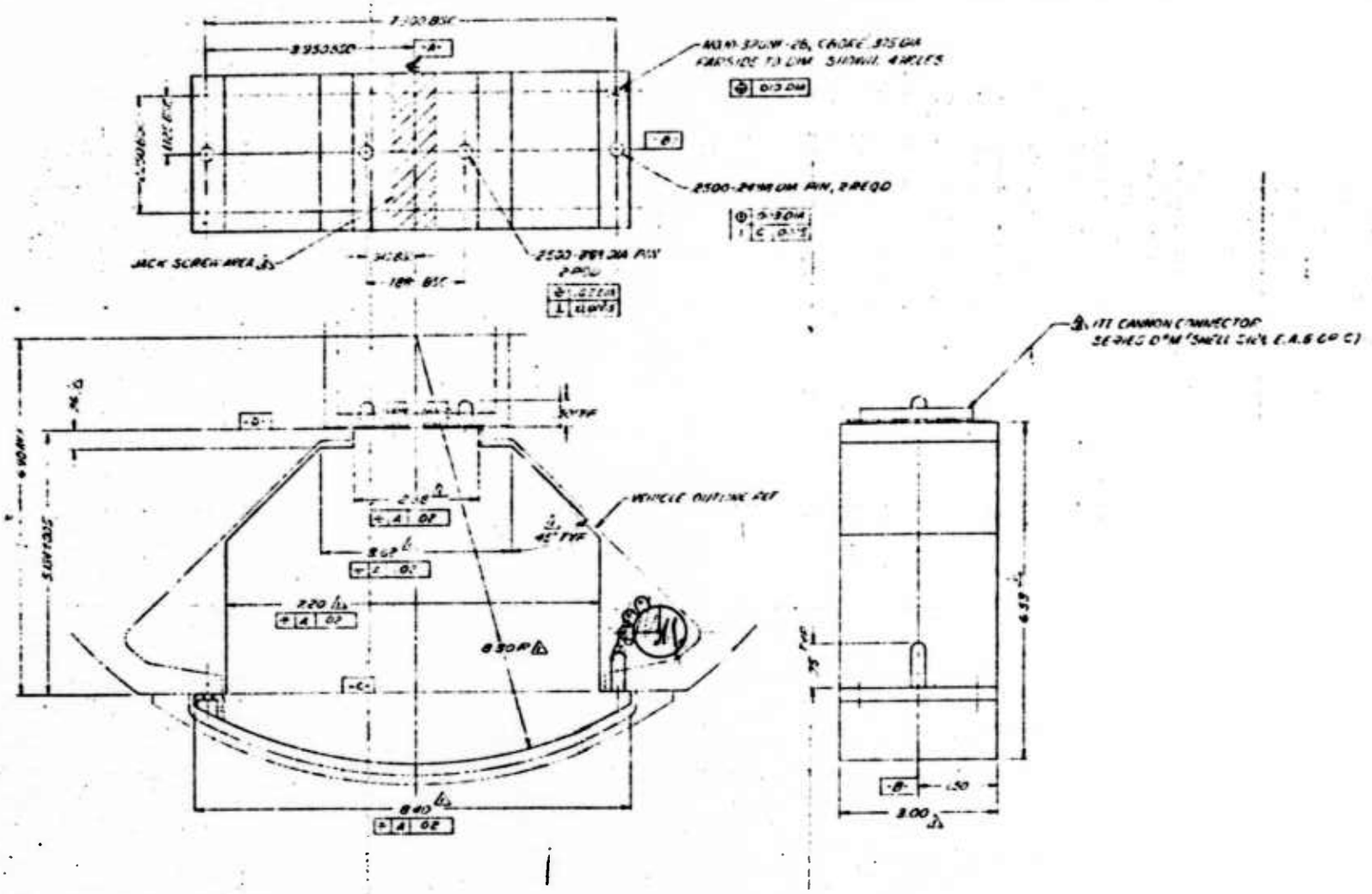
Figure 1 REFERENCE BLOCK DIAGRAM



NOTES

1. I/F DATA WORDS ARE FILLED IN WIT ALTERNATING ONES AND ZEROS IN FLYBACK PERIOD WHEN BUFFER IS EMPTY
2. FRAME SYNC WORD IS 22-BIT BARKER CODE
3. SUB-FRAME SYNC WORD IS [illegible]
4. BIT RATE = 466,944 BITS/SEC
   WORD RATE = 23,184 WORDS/SEC
   FRAME RATE = 912 FRAMES/SEC
   H/K CHAN SAMPLE RATE = 14.25 SAMPLES/SEC

Figure 2 PCM FRAME FORMAT



⚠ THE NUMBER AND SIZE OF CONNECTORS TO BE DETERMINED BY VENDOR.

⚠ IF PACKAGE 11 SECTION FORCE EXCEEDS 37.5 LB A MECHANICAL ASSIST MUST BE PROVIDED IN THE AREA (CROSSHATCH) INDICATED.

⚠ PACKAGE MAY VARY FROM FORM SHOWN BUT MUST NOT EXCEED BOUNDARIES DEFINED BY THESE DIMENSIONS

Figure 3 SPACE ALLOCATION PCM ENCODER

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APPENDIX B

HOUSEKEEPING COMMUTATOR SPECIFICATION

INTERPRET DRAWING IN ACCORDANCE WITH MIL-D-1000, FORM 3

HONEYWELL PART NO.
21008505 -101

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A			
B	REVISED PER [illegible]	[illegible]	
C	RELEASED [illegible] B	8/28/73	

SIZE	A	A	A	A	A	A	A	A	A	A	B
SHEET	1	2	3	4	5	6	7	8	9	10	11
REV	C	C	C	C	C	C	C	C	C	C	C

TOLERANCES UNLESS NOTED OTHERWISE		DRAFTSMAN		
.X ±.1	ANGLES ±	CHECKER	[illegible]	21 June 72
.XX ±.02		PKG ENGR		
.XXX ±.010		DEV ENGR	E. Dunbar	21 June 72
		PROJ ENGR	A.P. Bakos	6/21/72
		RELIABILITY	[illegible]	8/2/72
EPA 22916		ELEC ENGR		
FINISH—SEE NOTE		ENGRG RCD RLSE	Bannon	8/28/73
MATERIAL		CONTRACT NO.		
		H.I.R.I.S		

HONEYWELL INC.
RADIATION CENTER
LEXINGTON, MASS.

HOUSEKEEPING COMMUTATOR

SIZE	CODE IDENT NO.	DRAWING NO.
A	81395	21008505

SCALE 1 | WT | SHEET 1 OF 11

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REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A C	[illegible] B	21 June 72 8/28/73	

1.0 SCOPE

This document establishes the requirements for a Solid State Electronic Commutator for multiplexing the outputs of up to 64 housekeeping sensors into one channel for a PCM Telemetry System. The commutator consists of FET analog transmission gate, binary counter, analog buffer and digital buffer functions. An external clocking signal will be provided.

2.0 APPLICABLE DOCUMENTS

MIL-STD-454B	Standard General Requirements for Electronic Equipment, dated 10 June 1968
MIL-STD-461A	Electromagnetic Interference Characteristics, Requirements for Equipment, dated 1 August 1968
ER-69538	Environmental Specifications for Black Brant Payloads and Instrumentation, dated 25 March 1971, Bristol Aerospace Limited
21008493	PCM Encoder

3.0 REQUIREMENTS

3.1 Description and Intended Use

The commutator shall sequentially select analog voltages from various temperature, voltage, pressure, vacuum and position sensors and connect them to the housekeeping input

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channel of an associated PCM Encoder. Indexing from one input channel to the next will be under the control of a clock pulse from the PCM Encoder. The commutator shall provide a 6-bit binary channel identification signal to the PCM Encoder.

The commutator is part of an instrument payload for the Black Brant V high altitude research rocket. The rocket will be launched from an Arctic environment.

3.2 General Design Requirements

The commutator shall be as free as feasible of any defects in materials, processes, manufacture, or design which could conceivably degrade the performance or reliability of the commutator. Wherever possible, the commutator shall utilize existing circuits and components which have proven performance and reliability in simular applications. Where new design is required, MIL-STD-454 shall be used as a guide in selecting materials, parts, and processes. All selections shall be compatible to the intended use of the commutator.

3.3 Electrical Requirements

3.3.1 Commutator Block Diagram

Figure 1 is a conceptual Block Diagram of the commutator showing the essential elements. This is furnished for reference only as an aid to describing the commutator requirements and should not be construed as a requirement on the actual structure.

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A	ENGINEERING CONTROL RELEASE	2 Jan 73	
B	REVISED PER ECP [illegible]	1 [illegible]	
C	RELEASED TO LEVEL B	8/28/73	

The commutator shall include means for sequentially selecting one of 64 analog input signals and for connecting the selected signal to an output signal bus. An analog amplifier shall be provided for the purposes of buffering and internal gain adjusting of the signal output.

The binary count representing the number of the selected channel shall be made available through buffer gates.

Means for conditioning and converting the 28 Vdc power to the levels required by the analog and digital circuits in the commutator shall also be provided.

3.3.2 Number of Channels

The commutator shall provide 64 input channels. Supercommutation shall be obtainable by external cross-strapping.

3.3.3 Number of Poles

The commutator shall be single pole.

3.3.4 Sampling Rate

The sampling rate is 912 samples per second and is determined by an external clock pulse from the PCM Encoder.

3.3.5 Input Signal Characteristics

The input signal voltage range shall be 0 to +5 Vdc. Each channel shall be capable of sustaining an over-voltage in the range of -15 to +15 Vdc with no effect on accuracy of

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C			

other channels and no permanent damage. Back current shall be limited to ±0.5 microamperes during sampling and ±0.2 microamperes during non-sampling over the temperature range. Channel input impedance shall be greater than 5 megohms when the channel is on, and greater than 10 megohms when the channel is off.

3.3.6 Logic Interfaces

All digital input and output signals are required to be compatible with TTL logic. The commutator shall present only one standard TTL logic load to each digital input signal and each digital output line shall be driven by a separate buffer. The PCM Encoder will be similarly buffered and will present only one standard TTL logic load to each digital output line from the commutator.

3.3.6.1 Clock In

This signal from the PCM Encoder is a 912 Hz symmetrical square wave and represents the frame rate derived from timing logic in the encoder. Each pulse advances the commutator to the next channel.

3.3.6.2 Channel Identification Out

The logic levels on these six output lines indicate the channel number which the commutator is sampling in straight binary code.

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3.3.7 Output Characteristics

Output impedance shall be nominally 500 ohms and no permanent damage shall result if the output is shorted to ground.

3.3.8 Accuracies and Tolerances

In addition to the tolerances and levels already discussed, the commutator shall meet the following performance levels.

3.3.8.1 Offset

±5 millivolts maximum (common to all channels)

3.3.8.2 Scatter

±1 millivolt maximum (channel to channel variation)

3.3.8.3 Crosstalk

±0.1% including the case with over-voltage on adjacent channels

3.3.8.4 Linearity

Less than 0.05% deviation from best straight line

3.3.8.5 Gain

+0.9975 ±0.0025

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3.3.8.6 Output Format

NRZ (100% duty cycle)

3.3.8.7 Output Limiting

Outputs corresponding to channels where over-voltages exist shall be limited to a maximum of 1.0 volt above full scale for a positive over-voltage and to a maximum of 1.0 volt below zero for a negative over-voltage.

3.3.9 Prime Power and Grounding

Thecommutator shall operate to full performance specification when connected to a power source of +28 $^{+5}_{-0}$ Vdc. Current drain shall not exceed 100 milliamperes. No permanent damage shall result when the polarity of the input power is reversed. Signal logic, power and chassis grounds shall be mutually isolated and brought out on separate connector pins. There shall be at least 6 signal ground pins for the input signal channels.

In lieu of an external clock signal to synchronize power converters, provisions shall be made to bypass the internal power converter and to operate the unit with externally applied +15 VDC and -15 VDC.

3.4 Mechanical Requirements

3.4.1 Size and Weight

The commutator shall occupy less than 20 cubic inches, and shall weigh less than 1 pound. The supplier shall furnish Honeywell a dimensioned outline and interface drawing within 2 weeks ARO.

3.4.2 Connectors

All external connectors shall be mounted on one side wall of the commutator. Selection and application of connectors

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C		8/28/73	

shall comply with Requirement 10 of MIL-STD-454. Mating connectors shall be provided for all external connectors on the commutator. The mating connectors, cable harness type, shall be delivered to Honeywell with the commutator.

3.4.3 Mounting

Two mounting flanges shall be provided. The exact configuration shall be shown on the suppliers interface drawing.

3.4.4 Finish

Nickel Plate

3.4.5 Marking

Each external connector shall be given a reference designation. A nameplate shall be mounted on the top surface of the commutator and shall include at least the following information:

Commutator
Mfgr and P/N
Honeywell P/N
Serial Number

3.4.6 orkmanship

As a minimum, workmanship shall comply with Requirement 9 of MIL-STD-454. The commutator shall be assembled to workmanship standards consistent with flight hardware.

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3.5 Environmental Conditions

The commutator shall be designed and constructed to operate to full performance standards under any combination of the following environmental conditions:

3.5.1 Temperature

0 °C to +60 °C operating
-50 °C to +60 °C storage

3.5.2 Vibration

7.5 g peak 2000 to 27 Hz
0.2 inch double amplitude displacement
for 27 to 15 Hz.

A 115 second lagarithmic sweep in any axis, starting at the high frequency end and having no dwell time during the sweep.

3.5.3 Spin

5 rps, 8 inch radius, for 16 minutes

3.5.4 Altitude

Sea level to 250 kilometers

3.5.5 Acceleration

50 g for one minute, any axis

Environmental behavior of the Black Brant series of rockets is detailed in ER-69538, referenced herein as a guide.

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A B C	REVISED TO [illegible] RELEASED TO LEVEL B	21 June 73 1 Aug 8/28/73	[illegible]

3.6 Electromagnetic Interference (EMI)

The commutator shall be designed and fabricated to pass the interference and susceptibility requirements for Class ID of MIL-STD-461. Undesired switching transients and timing pulses shall be removed from input and output lines. Shielded wire shall be used where applicable. Any nonconductive finish shall be suitably masked under mating surfaces to maintain good metal to metal contact.

4.0 QUALITY ASSURANCE PROVISIONS

4.1 General

The supplier shall apply a quality control system in the inspection and testing of this device which will result in high assurance of compliance with all requirements of this specification.

4.2 Pre-Shipment Inspection

Prior to shipment, the supplier shall visually and electrically inspect the commutator to confirm that it complies with manufacturing drawings, meets the electrical performance requirements, and is constructed to meet the intended use. Honeywell may, at its option, witness these inspections. In any event, 3 copies of certified test data shall accompany the deliverable hardware.

5.0 NOTES

5.1 Approved Source

Vector Products
Newtown, Pa.
Model CSV-100-64-1EXT-PAM-NRZ

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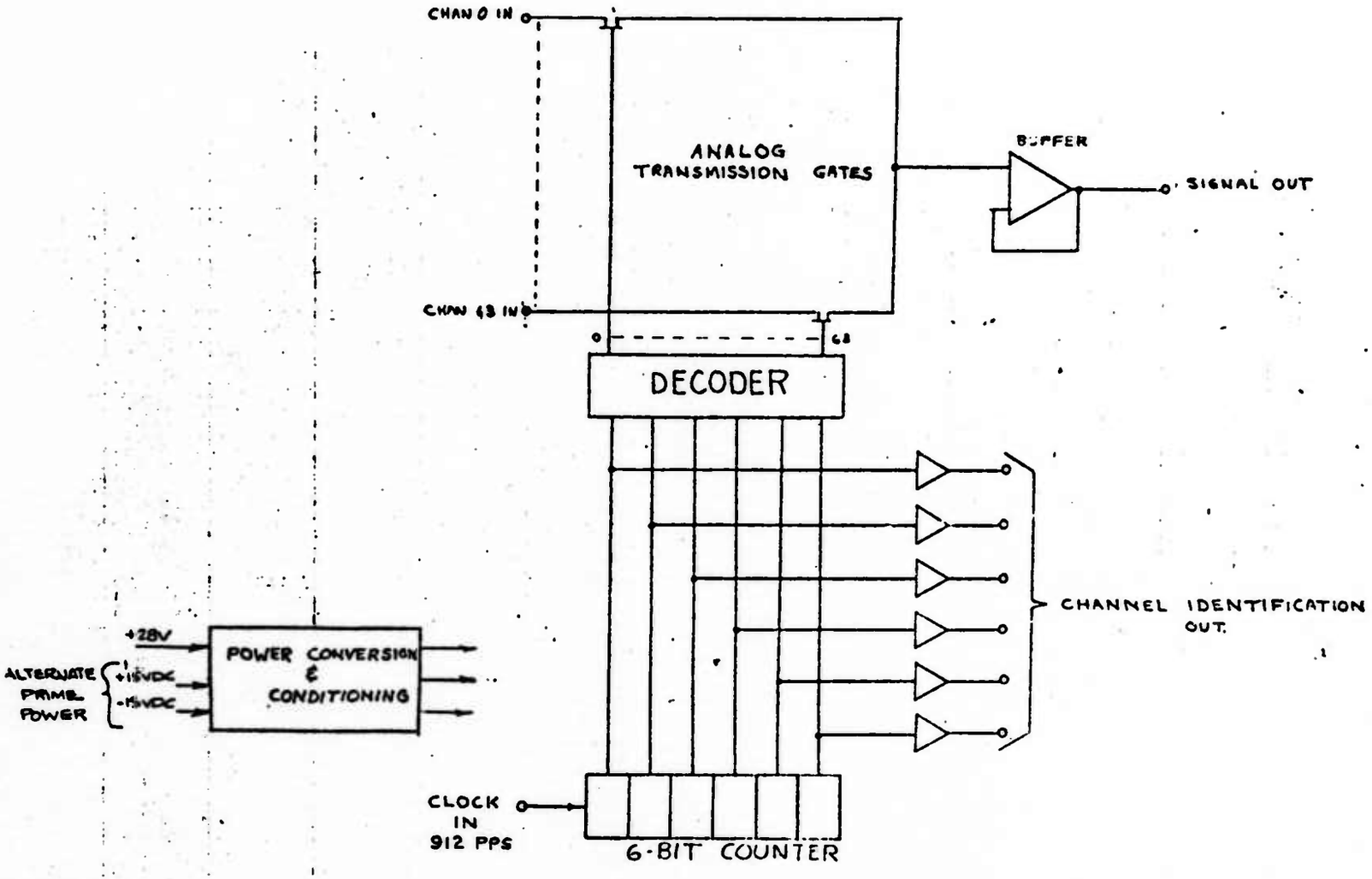

Figure 1 COMMUTATOR BLOCK DIAGRAM