THE BULK FILTERING, ACQUISITION, AND TRACKING SYSTEM (BATS)

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In this report, bulk filtering refers to simultaneous measurement of the velocity of all objects in a radar beam, and the automatic rejection of those with a velocity less than some specified amount. The Bulk filtering, Acquisition, and Tracking System (BATS) is a signal processor used with the TRADEX radar for experiments in the bulk filtering of ballistic-missile tank fragments. BATS is a part of the Designation and Discrimination Engineering Program which studies ABM radar system functions crucial to the design of future ABM systems. A detailed description of the signal-processing equipment designed and constructed for this program is presented in this report.

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Accepted for the Air Force
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Chief, ESD Lincoln Laboratory Project Office

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ILLUSTRATIONS

PREFACE

The purpose of this report is to describe, both in general and in moderate detail, the various parts of BATS. It is intended to serve many types of readers, each looking for different types of information.

For those desiring merely an overall system description, Secs. I through III are most appropriate. Those interested in the equipment and system details should consult the information given in Secs. IV and V. Complete details of the BATS Signal Processor are contained in the Operations and Maintenance Manuals prepared by General Electric and designated as Lincoln Manual 106 (7 volumes).

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GLOSSARY*

ABM	Antiballistic Missile
ALCOR	C-Band KREMS Radar
ALTAIR	UHF/VHF KREMS Radar
ATG	Analog Test Generator
BATS	Bulk Filtering, Acquisition, and Tracking System
BCAP	BATS Calibration and Alignment Program
BMF	Burst Matched Filter
BSP	BATS Signal Processor
CFAR	Constant False Alarm Rate
D&DE	Designation and Discrimination Engineering
DSCP	Digital Subsystem Checkout Programs
DSS	Digital Subsystem
ICC	Intercomputer Controller
KREMS	Kiernan Re-entry Measurements Site
LIDAR	A Designation for the Wideband L-Band Signal
prf	Pulse Repetition Frequency
PRI	Pulse Repetition Interval
RAM	Random Access Memory
RDSS	Range Discriminator Subsystem
REDD	Re-entry Designation and Discrimination
ROM	Read-Only Memory
RSS	Root of the Sum of the Squares
RTI	Real-Time Interface
SC	Simulation Controller
SIMPAR	Simulated Perimeter Acquisition Radar
SSP	SIMPAR Signal Processor
STC	Sensitivity Time Control
TADCO	Timing and Data Collection
TD	Tunnel Diode
TRADEX	L/S-Band KREMS Radar
VSCI	Velocity Selection and Channel Identification
ZCD	Zero-Crossing Detector
ZRT	Zero Range Trigger

* See also Figs. V-1 through V-3 for additional acronyms used only in the computer system.

THE BULK FILTERING, ACQUISITION, AND TRACKING SYSTEM (BATS)

I. INTRODUCTION

The Bulk filtering, Acquisition, and Tracking System (BATS) is part of the Designation and Discrimination Engineering (D&DE) Program and is used with the TRADEX radar for experiments in bulk filtering of tank fragments. The D&DE Program studies those antiballistic-missile (ABM) radar system functions crucial to the design of future ABM systems meant to counter sophisticated threats. The main goal of the D&DE Program is to conduct both simulated and radar on-line real-time experiments in target designation and discrimination. This program is in support of and sponsored by the Advanced Ballistic Missile Defense Agency (ABMDA). Data gathered by the KREMS radars are the bases of these experiments.

In the context of this work, discrimination is defined as the process of assessing whether or not a given object should be considered a threatening one (warhead). This process is generally applied to individual objects. Because discrimination is usually quite costly, in terms of radar and data-processing resources, it is desirable to reduce the number of objects to which the discrimination process must be applied – this is called designation. Given a large number of objects, the designation process attempts to categorize these into two classes, one of which (the largest) contains no threatening objects. This class then requires no further consideration. The remaining class contains all threatening objects, as well as some nonthreatening ones, and the process of discrimination is applied only to these. In particular, a large number of fragments from booster tanks come within the radar field of view, so a bulk filtering based on velocity measurements is needed to eliminate radar returns from objects that are not possibly threatening ones. In this report, bulk filtering refers to the simultaneous measurement of the velocity of all objects in a radar beam and the automatic rejection of those that have a velocity less than some predetermined value. In general, for sophisticated threats, an object is considered nonthreatening if it has slowed down early in re-entry. A simple sketch of the bulk-filtering problem is shown in Fig. I-1.

The graph illustrated in Fig. I-2 shows velocity as a function of altitude for various β objects in one particular trajectory. (β is the ratio of the mass of an object to the drag area.) Heavy or sleek objects (warheads) have a high β, and light or irregular-shaped objects (fragments) have a low β. For the example shown in this figure, it can seen that, above 80 km, all objects have about the same velocity. At about 45 km altitude, significant differences in velocity begin to appear between low β fragments and high β objects designed to survive to a lower altitude. Bulk filtering makes use of this velocity difference.

A. OVERVIEW OF THE D&DE PROGRAM

In order to show how the BATS effort fits into the overall D&DE Program, this section presents a very brief summary of the D&DE system. Implementation of the D&DE Program is at both Lexington and the Kiernan Re-entry Measurements Site (KREMS) in the Marshall Islands. Simulated real-time testing of software is accomplished at Lexington, using a computer identical to that installed at KREMS. For simulation exercises, actual KREMS radar data from many targets are assembled in appropriate fashion on magnetic-tape files. These tapes are

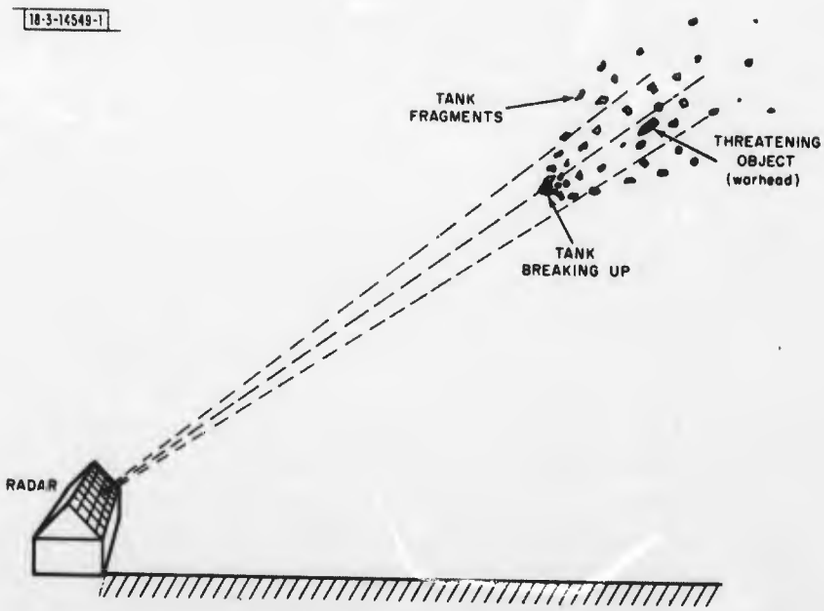


Fig. I-1. Bulk filtering.

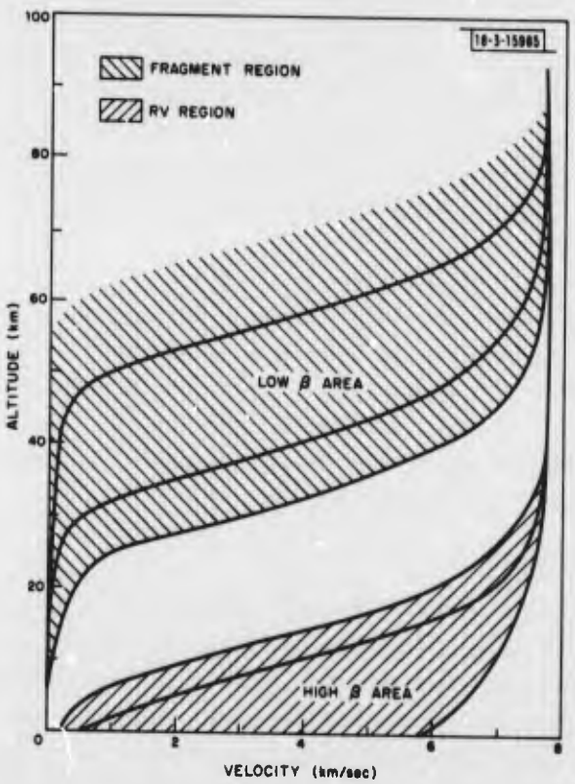


Fig. I-2. Slowdown curves for constant β objects.

then played back and the data are presented to the computer as though gathered by a radar. The computer processes the radar data, designates and tracks targets, and applies appropriate discrimination algorithms to reject as early as possible targets which cannot constitute a threat.

This same process is also carried out in real-time experiments on re-entry targets viewed by the KREMS radars – TRADEX, ALCOR, and ALTAIR. Although these radars are able to illuminate only a limited number of targets during late exo- and endoatmospheric flight, important tests in designation and discrimination can be performed in a real-time environment.

A program for the simulation of a perimeter acquisition radar (SIMPAR) is another phase of the D&DE effort. UHF target detection, verification, designation, and tracking are accomplished using the ALTAIR radar in the role of the perimeter acquisition radar. However, SIMPAR will not be discussed in this report.

The part of the D&DE program that makes use of the data gathered from the TRADEX radar is called the REDD system. The REDD system hardware at the KREMS site consists of the following major elements:

Computer	CDC 6600, complete with peripherals
Radar	TRADEX (with Sigma 5 computer)
Interfaces	RTI for CDC 6600 computer TADCO system ICC BA'S
Simulation	SC

These parts of the system and their relationship to each other are shown in Fig. I-3.

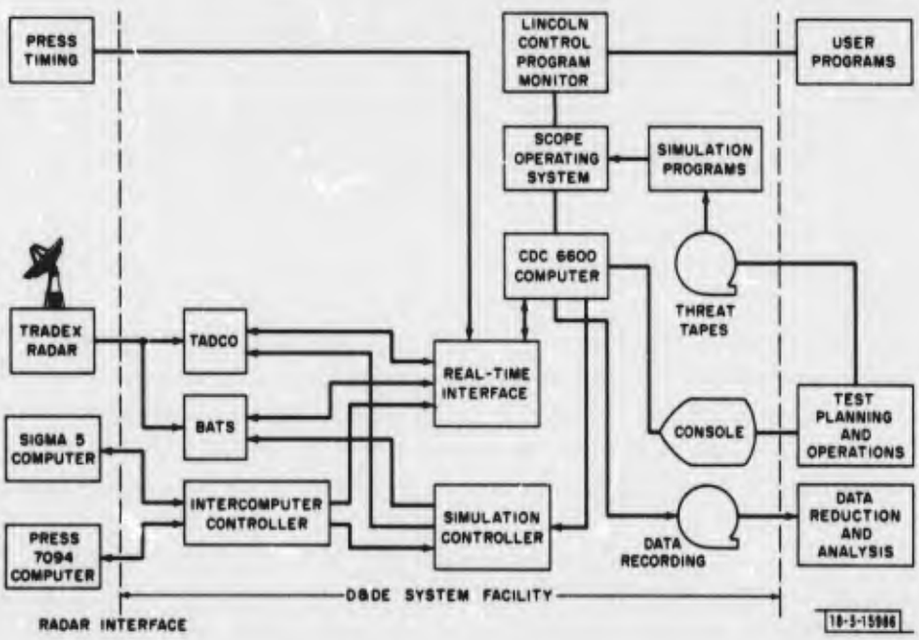


Fig. I-3. Major elements of REDD system.

1. TRADEX Radar

The TRADEX radar provides the data for most of the REDD system including the BATS equipment. TRADEX is a two-frequency radar having a large parabolic-reflector antenna. Monopulse tracking is done at L-band through a 5-horn feed; S-band signals are radiated and received through a single, circular horn mounted in the center of the L-band feed structure. TRADEX transmits a variety of chirped (linearly modulated) pulses of differing lengths and bandwidths, at both S- and L-bands. Pulses can be radiated in a uniform train, as pulse pairs or in variable-length bursts. A number of time multiplexed modes (combinations) of waveforms are selected under computer control. Right-circular (RC) polarized energy is radiated, and both right- and left-circular (LC) polarization are received. The radar pulse repetition frequency (prf) can be varied over a range from less than 100 to above 2000 pps.

TABLE I-1
BASIC TRADEX RADAR PARAMETERS

	L-Band	S-Band
Transmitter frequency (MHz)	1320	2950
Peak power (MW)	4	4
Average power (kW)	300	110
Prf	Up to 1500	Up to 3000
Range resolution (m)	150, 15	15, 4.5
Nominal S/N ratio (dB) (−30 dBsm target at 150 km)	34	32
Beamwidth (deg)	0.65	0.25
Angle tracking	5-horn monopulse	No capability

TRADEX's control computer is an XDS Sigma 5 which exercises all radar-control functions, including tracking where a Kalman estimator is used on TRADEX's principal target. Up to five additional targets can be tracked, using a polynomial estimator, in range only. Additional parameters of the TRADEX radar are summarized in Table I-1.

2. Computer

The CDC 6600 computer, which is the central component of the D&DE system, is a large, fast, general-purpose machine capable of executing about 2.7×10^6 instructions per second. The machine is furnished with 131,000 words of 60-bit memory. Standard I/O is performed with the aid of ten peripheral processors each having 4096 words of 12-bit memory. In addition, there are standard tape drives, drum and disk storage, a line printer, a card reader, and an interactive display.

The 6600 computer calls for and receives radar data on various targets. Data-gathering may be initialized by a simulated state-vector handover or by means of a radar scan. Targets are placed in track under computer control, and additional data are collected and processed as appropriate for the experiment. Results of the experiments are recorded by the computer for post-mission analysis. The interfacing between the CDC 6600 computer and the real-time signals

necessitated the development of four specific types of interface devices. These are described briefly in the following section.

3. Interfaces

a. RTI

Real-time operation of the radar-computer complex implies the ability to output instructions from the computer and to receive radar information into the computer at high speed and with little delay. Especially built to interface the CDC 6600 computer with a network of external devices by way of eight multiplexed 60-bit data paths, the RTI provides the capability of transferring blocks of data under channel control between external devices and the 6600 central memory. The RTI consists of a multiplexer, an interval timer, and three data-channel pairs with expansion capability to four. The multiplexer is basically a direct-memory-access device which transfers 60-bit data words into and out of the 6600 central memory. Provision is made for reception of interrupts from external devices, for transmission of interrupts to external devices, and for device control lines. Provision is also made for keeping track of channel and external device status.

b. TADCO System

The TADCO unit was designed to enable the gathering of pulse-by-pulse radar data under instruction from the CDC 6600, without requiring the radar to be under the control of D&DE software. In order to achieve independence from the radar's own data-collection process, TADCO includes logarithmic amplitude detectors, phase detectors, analog-to-digital converters, sampling control circuitry, and a 64-bit-wide, 512-word, IC memory. The sampling rate can be selected from 5- to 1275-m range intervals in increments of 5 m. A simplified block diagram of the TADCO unit is shown in Fig. I-4.

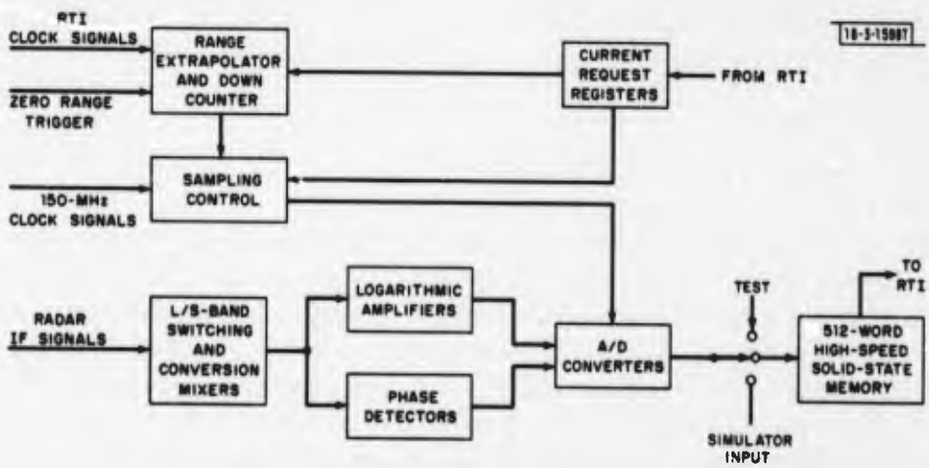


Fig. I-4. Block diagram of TADCO unit.

Data requests are generated in the 6600 by the software, and are transmitted to TADCO, via an RTI channel, in the form of short messages. A message will request either track or wake data; the message is predicted upon a priori information having been supplied to the 6600 concerning the current mode and waveform being transmitted by the radar. Included in the

data request are the extrapolated target range, range rate, and time of validity of these items, as well as a specification of the desired sample pattern. At the time of validity, the range is extrapolated until a proper trigger is received from the radar. The range is then counted down using a 150-MHz clock to control the positioning of the sample window. When the range has been counted down, A/D converters are strobed to sample the radar-detected returns at the rate specified in the data request. The sampled data are accumulated in high-speed buffer storage, and are then transferred via the RTI into the CDC 6600 central memory.

c. ICC

The ICC is a buffering unit operating between the RTI and the various KREMS computers; it operates as a device on two channels of the RTI. The ICC provides two 128-word storage buffers (24 bits each) for each computer with which the CDC 6600 communicates. Normal message transmission involves loading the message into the appropriate ICC buffer, and setting a flag in an associated status register. A priority message mode is also provided which permits transmission of messages, directly through the ICC without complete message buffering.

d. SC

The SC provides a mechanism whereby the D&DE software can control the flow of simulated radar data (digitized) taken from threat tapes through the radar interfaces (TADCO, BATS, or ICC) into the 6600 computer in the same way as if the data were coming directly from the radar or the radar computer. In a simulation mode, the system operates exactly as a real-time mission except that the clock is shut off during periods of data accessing. Also in this mode, the interfaces to the radar (TADCO or BATS), and radar computer accept data from the SC rather than the radar. Requests generated by the software are routed to the SC, which then obtains suitable "replies" from the recorded threat data (which have been stored on a drum). Transfers from the drum to the SC are carried on under control of a pair of peripheral processors. The SC, in turn, routes the replies to the appropriate interface device, and transfer then takes place through the RTI into 6600 memory exactly as for live, real-time data.

4. System Software

The CDC 6600 software can be separated into four categories: Supervisory programs, user programs, simulation software, and diagnostic routines.

Supervisory programs control the utilization and the environment of the computer as it executes user programs. SCOPE (Supervisory Control of Programming Environment) is a multiprogramming supervisor designed and modified by Control Data Corporation to a version called Real-Time SCOPE VI (RTS VI) in which certain jobs, designated as "real-time" jobs, are given priority use of the computer resources. Lincoln Control Program (LCP) is a central processor monitor program which interfaces to the RTS VI. LCP is central memory resident; it manages files, handles interrupts, and controls the execution of user tasks.

User programs refer to the real-time software package which performs the basic D&DE functions during a mission. Thus, the term "User Programs" encompasses the REDD programs, bulk-filtering programs, the SIMPAR real-time programs, and any other experimental packages which become a part of the D&DE experimental program.

The simulation software is that set of programs which enables the user programs to be tested in simulation. Both digital and analog simulators are included, driven in either case by

the CDC 6600 software. The simulation process requires a threat tape as a source. This is a magnetic tape in which the parameters of a target threat are stored. Threat tapes are made off-line using, as a base, either previously recorded radar signals or synthetically generated signals. During a simulation exercise, the CDC 6600 operates in a dual role, simultaneously controlling the accessing of the threat data while executing the instructions of the software package (user programs) under test.

Diagnostic routines are programs designed especially to check performance of the interface hardware including the RTI, ICC, and various signal processors (TADCO, BATS, SSP).

5. REDD Functions

REDD experiments constitute one phase of the overall D&DE program. REDD tests are performed using TRADEX as a signal source, and TADCO or BATS as the interface and processor. The objectives are to validate the performance of a variety of algorithms in a live, real-time environment. Included are tracking, impact-point prediction, and several discriminants or designation algorithms applicable over various altitude regions.

The REDD software is a collection of programs assembled and organized in such a way as to carry out a live engagement process without human intervention. As presently implemented, the software does not have provision for automatic target acquisition; instead, it depends upon "handover" of targets already in track by TRADEX. Handover messages are transmitted to the CDC 6600 via the ICC. Based on these messages, the software requests track data from TADCO or BATS from which a track estimator is formed in the computer. Three different track estimators are available for use depending upon target altitude and the precision required to perform target discrimination. Other major REDD software components are:

Impact Prediction – use of track data to estimate impact point and time.

Discriminants – algorithms yielding estimates of target mass.

Threat Estimation and Ordering – a means of combining results of discrimination measurements and impact prediction to estimate and rank targets in accordance with the magnitude of threat possessed by each one.

Resource Allocation – the control of radar and computer resources among the various targets in such a way as to optimize system performance.

Sigma 5 Message Handler – directs programs necessary for the interchange of information with the TRADEX Sigma 5 computer.

B. BULK-FILTERING TECHNIQUES AND WAVEFORMS

There are various ways of performing bulk filtering, and many radar waveforms to accomplish the intended results. The choice depends on many factors, including effective utilization of transmitter power, performance in a dense target environment, and the complexity and cost of the signal-processing hardware. This section will discuss, very briefly, just a few of these techniques.

Some of the possible radar waveforms that can be used for bulk filtering are illustrated in Fig. I-5. The two basic classifications are coherent and noncoherent. A noncoherent waveform measures the range of a target at two or more different times and computes the rate of change of the range. A coherent waveform makes use of the Doppler shift of the moving target to

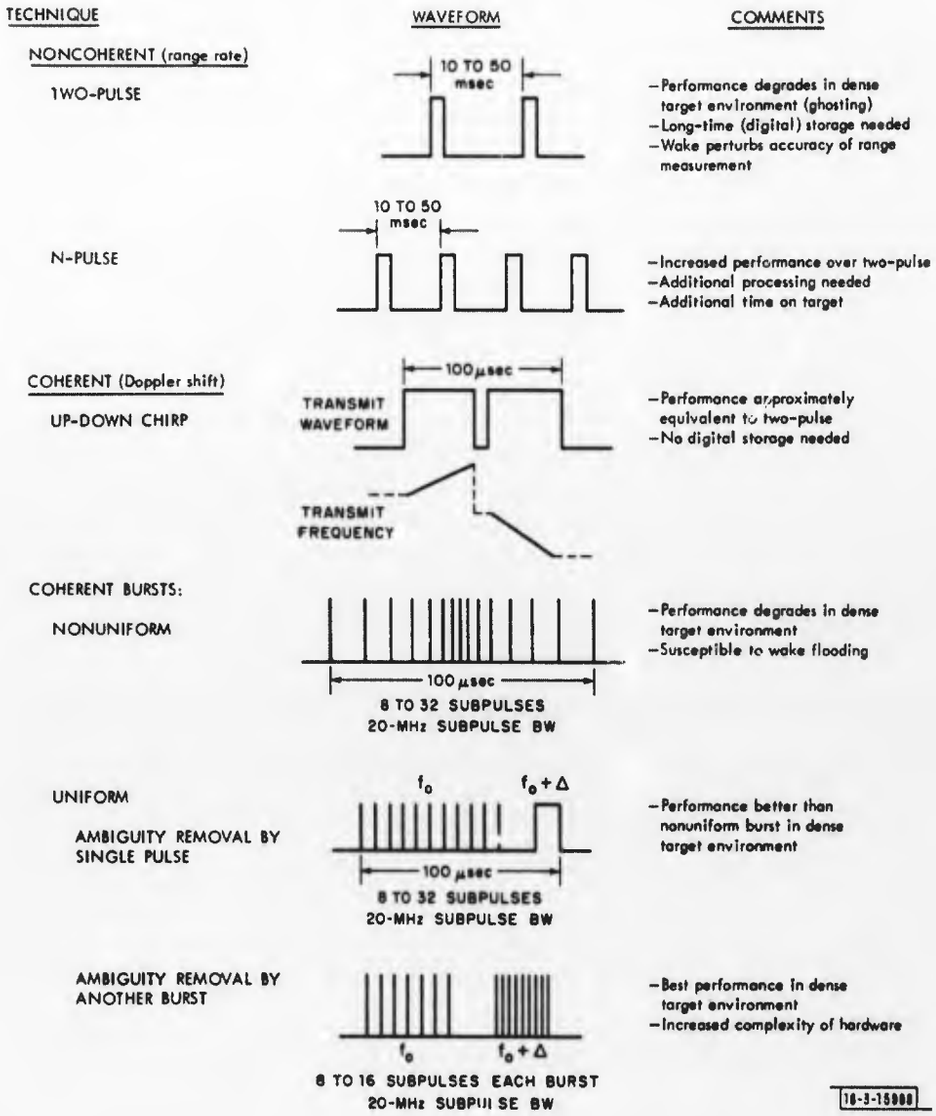


Fig. I-5. Approaches to bulk filtering.

measure its radial velocity. Some of the important factors in the noncoherent technique are the velocity measuring accuracy and the ghosting and traffic-handling capability. The measurement accuracy for this technique can be very good, but the performance degrades in a high traffic environment. Alternatively, the controlling factors for coherent methods are the resolution capability and the sidelobe (and/or ambiguity) levels. The coherent methods may not (in practice) provide as much velocity measuring capability as can be attained by noncoherent measurements but, with proper design, can provide good rejection of most fragments.

The noncoherent approach involves the transmission of a single chirp search pulse and the detection and range marking of each target in the acquisition window. An identical verification pulse, some 10 to 50 msec later, is then sent out. Those targets that have moved enough in this time to fall within acceptance gates, suitably timed with respect to the search returns, are designated as threatening objects. A sketch of this procedure is shown in Fig. I-6. Additional transmissions can be used to improve the accuracy and to build up a state vector for track initiation purposes.

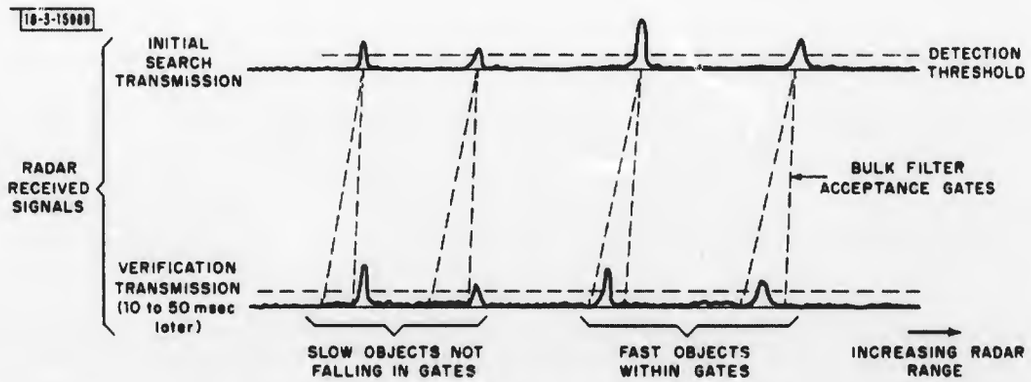


Fig. I-6. Noncoherent bulk filtering (two-pulse).

The width and placement of the acceptance gates depend on the time interval between the search and verify pulses as well as on the elevation angle, target range, and re-entry velocity. Although the separability between the high-velocity (or range-rate) and low-velocity targets increases with this time interval, so also does the gate width required to accept the spread of high-velocity targets. This increases the probability that a low-velocity ghost will be accepted. (A ghost is defined as a target entering a gate established for another target, giving the impression that one of the objects was a high-velocity one.) Accurate range estimation is, of course, required with this approach, and performance improves directly with signal bandwidth; but the perturbing effects of wakes on the range measurement can be a serious problem.

The waveforms illustrated in Fig. I-5 show some of the possibilities in the coherent category. The first one shown is the up-down chirp. This makes use of the range Doppler coupling effect in pulse-compression systems. Two chirp pulses are transmitted, on different center frequencies – one increasing with time and the other decreasing with time. Upon reception, coincidence gates are placed at the output of two radar receivers and their timing adjusted so that only targets with a given velocity are passed. The up-down chirp approach to bulk filtering gives a range-rate measurement capability less than that of the two-pulse noncoherent approach, but has the advantage that it is essentially a single waveform.

Shown next in Fig. I-5 are some burst waveforms. A burst waveform consists of a number of pulses that are spaced sufficiently close together so that the unambiguous Doppler interval encompasses all expected velocities. For bulk-filtering purposes, this means that the spacing is so small that the radar cannot receive echos between transmissions of the subpulses in any one burst. The burst returns are coherently processed in a bank of matched filters tuned to span the range of all possible target radial velocities.

Some of the many parameters that must be considered in the design of a burst waveform for use as a bulk filter are: number of pulses, type (uniform/nonuniform), pulse spacing, and amplitude and phase weighting. It is these parameters that (for a given radar frequency) determine the placement of the range and Doppler ambiguities and the magnitude of the sidelobe levels of the ambiguity function. Burst systems have the advantage that they do not detect low-velocity fragments and are not as susceptible to the ghosting problem. They also are less perturbed by targets with large wakes.

When one considers the use of the burst waveform in a multiple-target environment, it is necessary to examine the effect of the range and Doppler sidelobes (ambiguities) on the overall filter performance. For a uniform burst, one can apply amplitude and/or phase weighting on either the transmitted waveform, the received waveform, or both to achieve very low Doppler sidelobe levels. While this approach provides very good rejection of the low-velocity fragments, it yields many ambiguous range returns from the high-velocity objects. The ambiguities must be resolved by another transmission immediately following or interleaved with the burst. The second transmission could be either another burst with a different pulse spacing or a single chirp pulse transmitted and received at a slightly different center frequency to avoid interference with the initial burst.

One other approach is to use a burst design in which the range ambiguities are eliminated by selecting the spacings between the pulses in a nonuniform way. It is possible to select the number of pulses in the burst to permit reasonable range sidelobe rejections. Doppler performance, however, is generally poor and little improvement in the Doppler sidelobes can be obtained by the application of amplitude or phase weighting with this type of waveform.

To summarize, the primary advantage of the two-pulse noncoherent filter is its good velocity accuracy. The primary disadvantages are the number of additional pulse transmissions required, the probability of ghosting which increases rapidly with fragment density, and the perturbing effect of wakes on the range estimates. The primary advantage of the burst waveforms is that they afford rejection of the lower-velocity fragments on a single transmission basis. However, the range ambiguities must be resolved with another transmission. Finally, the up-down chirp gives a velocity resolution that is comparable to that of the burst waveform. However, it is susceptible to the ghosting problem but does not suffer from the range ambiguities of a burst.

C. INITIAL TESTS AND DESIGN OF BATS EQUIPMENT

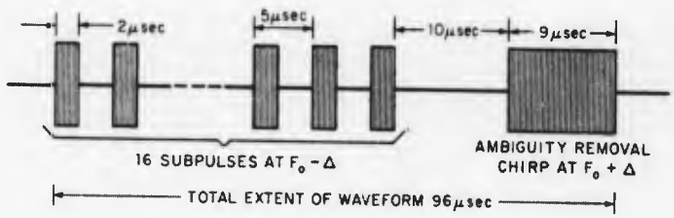
As an initial test of the noncoherent bulk-filtering technique, experiments were performed using the TADCO interface and an addition to the REDD software programs. While this did show the feasibility of the noncoherent approach, it had two basic limitations. One is that the TADCO processor can only sample a very limited range extent. The sampled video from TADCO must then be processed in the software to produce estimates of the range of all targets in the acceptance window. The unpacking of sample data, thresholding, and range marking require about

100 msec worth of CPU time for each 12 km in the acceptance window. This is unacceptable in a real-time situation in the light of other requirements placed on the CPU.

It is clear that, in order to run experiments in bulk filtering, a signal processor was needed to accomplish the following basic goals:

(1) Automatic detection of targets
(2) Range marking (measurement) of all targets
(3) Measurement of target cross section, length, and monopulse angle error
(4) Receiving and match-filter processing the burst waveform
(5) Interfacing with the CDC 6600 computer and TRADEX radar.

For the coherent type of experiments with TRADEX, it was decided to implement a uniform-burst waveform and processor. This choice is based on the fact that the uniform burst provides good rejection of slowly moving dense clutter. The waveform is shown in Fig. I-7. It consists of 16 subpulses and provides unambiguous Doppler resolution at S-band. Each subpulse has a 2-μsec envelope and is linearly frequency-modulated over 20 MHz. The range ambiguities are removed by a standard TRADEX chirp pulse following the burst, transmitted at a different center frequency so that the burst and chirp echos can be separated in the receiver. This method of ambiguity removal by a noncoherent chirp transmission rather than by another burst has been chosen for simplicity, and not for optimum performance in any tactical system. The ambiguity removal chirp pulse could be replaced at a later time by a second burst. To reduce the Doppler sidelobe level, weighting is employed in the receiver. An amplitude taper across the transmitted burst could further improve the dense-clutter rejection, but it is not being implemented at this time.



BURST PARAMETERS

Number of subpulses	16	Range resolution (R)	15 m
Subpulse bandwidth	20 MHz	$\dot{R}$ resolution (unweighted)	625 m/sec
Subpulse duration	2 μsec	$\dot{R}$ ambiguity	10 km/sec
Subpulse spacing	5 μsec		
Burst length	77 μsec		

18-3-14124-2

Fig. I-7. BATS burst.

The anticipated use of BATS in D&DE experiments is roughly as follows. It will be used first to support D&DE acquisition and tracking. The thresholding equipment and procedures will be evaluated along with the range mark and amplitude measurement functions. Comparisons will be made with TADCO data and the software range estimator.

Use of the noncoherent bulk-filter algorithm will then be exercised using the BATS equipment output, rather than TADCO and the software sample processor. The performance of the two will be compared and will be used to validate simulations. The data gathered will be used to generate additional threat tapes for simulation purposes.

Once the coherent (burst) system is in operation, experiments will be run to demonstrate the performance of this technique. With the two processes operating simultaneously, the performance of bulk filtering in the coherent mode then can be compared directly with the noncoherent mode. These data will also be used to validate simulations. Once an experimental body of data is gathered and analyzed, it will be used to determine ways of achieving better performance with less data-processing time.

II. EQUIPMENT SUMMARY

In addition to the BATS signal processor (BSP) and its peripherals, the entire BATS includes other equipment to permit the testing of coherent bulk-filtering techniques. The standard TRADEX 9-μsec, 17.6-MHz, S-band chirp pulse is used as the waveform for the noncoherent bulk filter, and the coherent bulk filter uses the uniform burst waveform. The burst is collapsed in real time using an IF burst matched filter (BMF) and the range ambiguities, inherent in the use of the uniform burst, are suppressed by a circuit that reports only coincidences between the burst's central response and the response to a single TRADEX chirp pulse.

A. OVERALL SYSTEM LAYOUT

Figure II-1 is a block diagram showing the relationship of all the equipment connected with the BATS. The equipment shown in the heavy lines indicates the new BATS-related equipment that was recently installed at the site. In the TRADEX building, new pulse-compression/expansion equipment was added for the generation and reception of the uniform burst subpulse. Additional equipment and modifications to TRADEX were also needed to frequency translate the input and output of the expansion-compression networks and to generate the timing for the burst. However, no major transmitter or receiver modifications were found to be necessary.

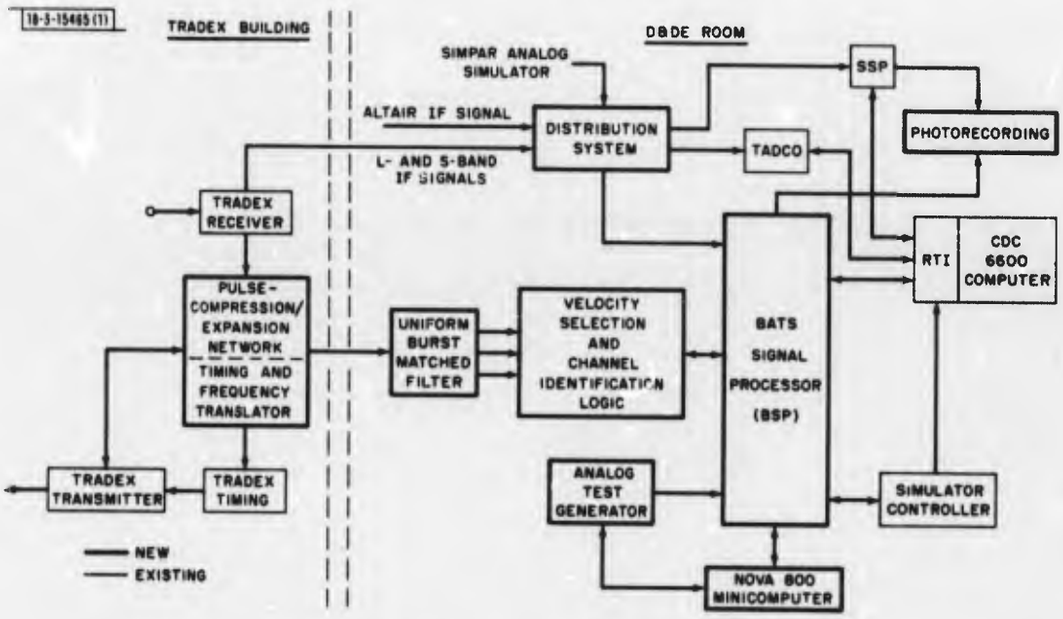


Fig. II-1. BATS and related equipment.

Located in the D&DE equipment room is the BSP which will provide the adaptive threshold computation, and the range marking and other parameter estimation circuitry. Auxiliary equipment consisting of a minicomputer and an analog test generator has been provided to test, calibrate, and maintain the system. A photorecording system was also designed and installed whose purpose is to monitor the system during missions and to serve as a post-mission diagnostic tool.

The compressed L- and S-band IF outputs from TRADEX go first to a distribution system which feeds and isolates the various processors. A set of outputs from this system goes to the

BSP. The output from the new pulse-compression equipment goes to the uniform burst matched filter, which consists of a set of 16 ultrasonic delay lines to collapse the burst and an IF Butler-type phase matrix having 16 outputs. These outputs go to the velocity selection and logic equipment, which detects the 16 outputs and passes to the processor only the output of the channel having the greatest signal. It is then compared for time coincidence with the regular TRADEX chirp pulse and the parameter estimation and range marking functions are accomplished.

The output (in digital form) from the processor is passed along to the RTI of the D&DE 6600 computer. The correlation function between successive pulses in the noncoherent bulk-filtering mode is handled by the 6600 computer in software.

Also shown in Fig. II-1, but not directly related to BATS, is the TADCO unit presently in use at the site and the SIMPAR signal processor (SSP). The simulator controller that is used with TADCO and BATS is also shown.

B. BATS SIGNAL PROCESSOR (BSP)

The main part of the BATS equipment centers around the BSP built by General Electric, Heavy Military Electronics Systems Division (G. E. HMES), Syracuse, under subcontract to Lincoln Laboratory. This signal processor is controlled by the CDC 6600 D&DE computer and delivers to the latter the parameters of detected targets through a digital buffer and control system. Because the BSP performs target detection and range- and angle-error estimation, it can also be used in the target-tracking mode of the REDD system. This would eliminate the need to process TADCO-sampled data in software for track-error estimation. However, TADCO would continue to be used to sample data for the wake-processing algorithms.

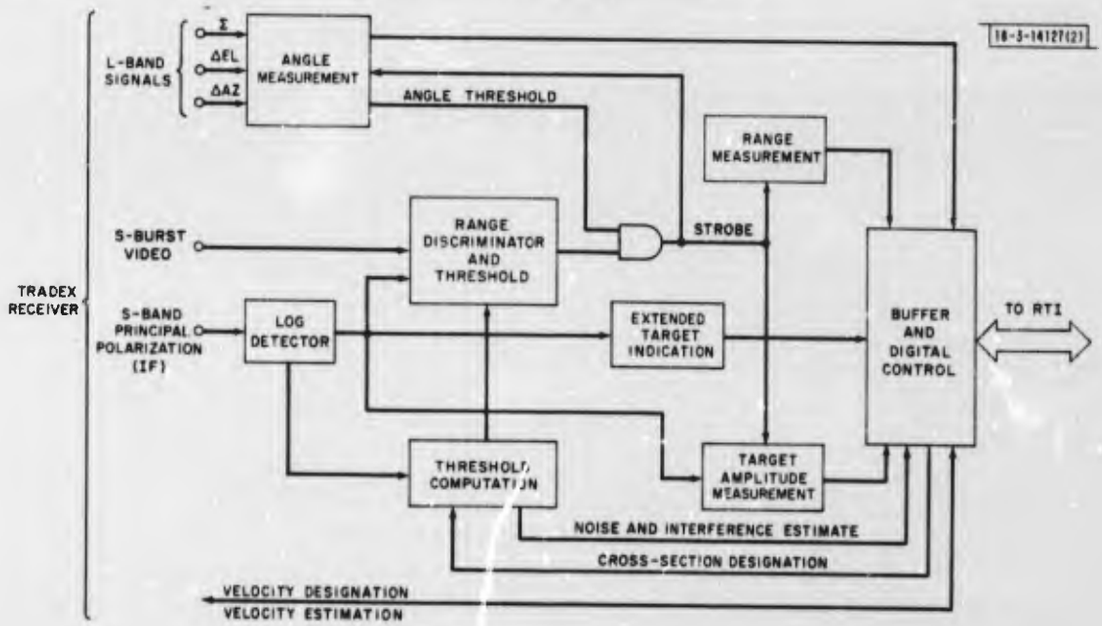


Fig. II-2. BSP simplified functional block diagram.

A simplified block diagram of the BSP is shown in Fig. II-2. The specific functions of this equipment can be summarized briefly as follows:

(1) Establish a range acquisition window based on computer input data.

(2) Estimate the noise and clutter power in the neighborhood of the acceptance range gate and set a time-varying threshold for the detection of targets in this acceptance window. This threshold will be based on:

  (a) An estimate of interference level (range sidelobes from large targets near the area under examination)

  (b) A measurement of received (or jammer) noise in the area of the acquisition window

  (c) The minimum target cross section to be observed and/or a designated level above the measured noise and interference level

  (d) A dynamic radar range (R^4) correction (STC)

  (e) The TRADEX receiver gain control setting.

(3) Measure the range (from the beginning of the window) to the centroid or leading edge of each target.

(4) Measure the peak amplitude for each target.

(5) Measure the elevation and azimuth angle error for each target.

(6) Estimate and report the noise or interference power in the S-band principal polarization and the L-band reference channels.

(7) Distinguish between a point or an extended target, and modify the range estimator system accordingly.

(8) Provide an indication of interference from a second target in the L-band beam, but not in the S-band beam.

(9) Reject measurements taken on targets in the mainlobe beam, outside of prescribed angular limits.

(10) Buffer, format, and transfer all measured data to the D&DE 6600 computer via the RTI.

This complete system is installed at KREMS. A digital-only portion of the equipment was also built and installed at the Lexington D&DE facility. This is used in the digital simulation mode with the simulator controller.

C. ANALOG TEST GENERATOR (ATG)

An ATG is used to provide test outputs of known characteristics for the checkout and alignment of the BSP's detection and parameter estimation circuits. The generator is capable of generating two 120-MHz test pulse signals of known amplitude and time position to check out the S-band portion of the equipment. Simultaneously, it produces three 60-MHz output signals to feed into the L-band channels. The ATG is controlled by a Data General Corporation Nova minicomputer delivered as part of the equipment. The system is also capable of adding in noise and varying the test pulse width to be able to test many of the features of the BSP.

D. DIGITAL TEST UNIT

The same minicomputer used in the ATG is used to check out the digital portion of the BSP. While this can be done via the CDC 6600 computer, little time is available on the computer to do

this. Hence, the stand-alone capability with the minicomputer is necessary. It greatly facilitates checkout of the system, for both debugging and periodic maintenance.

E. TRADEX MODIFICATIONS

The modifications to TRADEX to transmit and receive the new burst waveform consist of new expansion-compression equipment, a burst pulse generator, mixing circuits, and changes in the transmitter timing.

The burst subpulse compression and expansion system is triggered from a burst timing generator which, when enabled, accepts a trigger from TRADEX and produces burst triggers coherently related to the TRADEX frequency standard. A surface wave pulse expansion line, with its associated electronics, generates the 2-μsec duration, 20-MHz linear FM expanded subpulses. A similar surface wave compression line collapses the subpulses upon reception and provides weighting for range sidelobe reduction.

F. DISTRIBUTION SYSTEM

The signal distribution system accepts all the 60- and 120-MHz IF signals from TRADEX (and ALTAIR) and distributes them to the various processors in the D&DE equipment room. It also accepts and distributes the outputs from all the associated digital timing and mode signals as well as the SIMPAR signal simulator. It terminates the signals coming from the various sources and gives the various processors the capability of independently selecting from either of any two input sources.

G. UNIFORM BURST MATCHED FILTER

The uniform burst matched filter delays the received burst subpulse signals appropriately and adds them, with various phase shifts, in an IF Butler-type matrix. In this way, 16 filter outputs are formed, each sensitive to a different Doppler frequency. This is shown in simplified form in the block diagram, Fig. II-3, and is described in more detail later in this report.

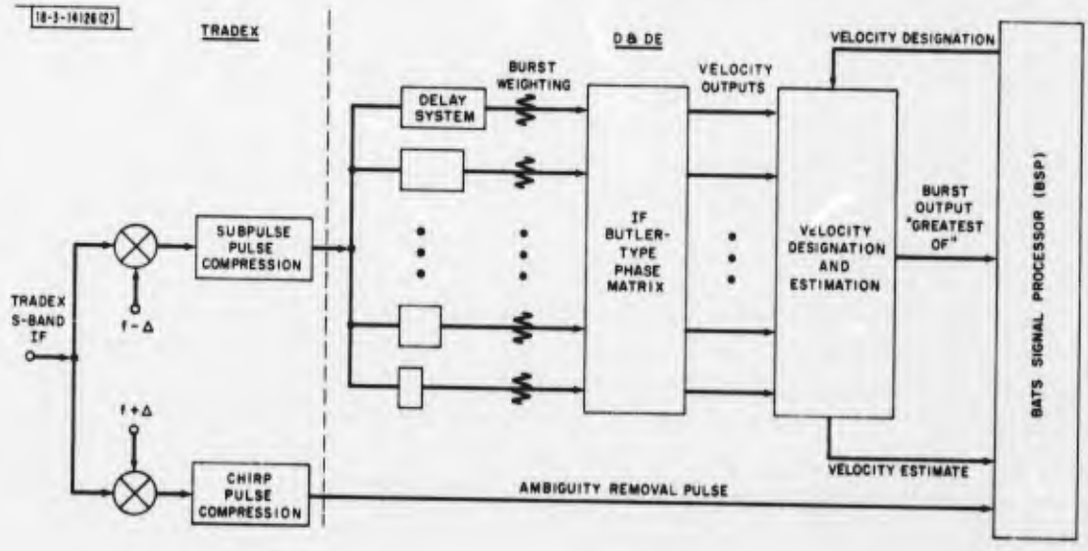


Fig. II-3. Uniform burst processor.

H. VELOCITY SELECTION AND CHANNEL IDENTIFICATION (VSCI) CIRCUITRY

This equipment accepts and terminates the 16 outputs from the burst matched filter. At any given time, the output channel that has the greatest output is an indication of the instantaneous target velocity. Consequently, the function of this equipment is to detect all the IF filter signals and compare them to find out which is the largest. If this indicates that the target is within a Doppler acceptance band designated by the 6600 computer, the signal is passed along to the BSP. It is then tested for coincidence with the regular TRADEX chirp pulse output to eliminate ambiguous detections.

I. PHOTOGRAPHIC RECORDING

A photorecording system was designed and built for use with the BATS and the SIMPAR signal-processing systems. The equipment includes various types of A-scope displays to enable an operator to monitor system performance and to diagnose problems in either processor. The equipment is flexible enough to be able to handle other diagnostic-type recording needs of the D&DE system.

III. BATS SIGNAL PROCESSOR (BSP) ORGANIZATION

The main part of the BATS is the signal processor which will be described in this section and in detail in Sec. IV-A. This portion of the system accepts signals from TRADEX as well as from the new coherent filtering equipment added to TRADEX. It receives instructions through the RTI from the D&DE computer and generates range strobes on targets detected in a range acquisition window, estimates target parameters, and buffers these data for transmission to the D&DE computer. The specific functions of the system were summarized previously in Sec. II. The organization of the signal processor subsystems is shown in Fig. III-1. Figures III-2 through III-4 are photographs of the equipment as installed at KREMS.

The complete system shown in Fig. III-1 is broken down into eight cabinets and six subsystems. In order to equalize the amount of equipment in each cabinet, boundaries of various subsystems were adjusted slightly so that system functions may not necessarily fall into the most logical cabinet. Each one of these cabinets and its functions will be described in Sec. IV. In this section, only system concepts will be considered with little discussion of specific equipment realization.

A. BSP OPERATION

The operation described here assumes that a mission has been planned so that TRADEX will be operating in modes which can provide appropriate data to the D&DE system at frequent intervals. TRADEX may be scheduled to accomplish its primary mission independent of the data called for by the D&DE computer. TRADEX transmits its planned schedule to the D&DE computer via the Intercomputer Controller (ICC) approximately 100 msec prior to execution of the schedule.

Using this a priori knowledge of the schedule, the computer can plan to gather data from TRADEX by means of BATS. Before the actual collection of data, the external device select lines of the RTI call up BATS (or other equipment which shares the same RTI input and output channels), depending on the nature of data required. In the case of BATS, the control words generated by the computer are loaded into the BATS designation registers. Because the TRADEX PRI (pulse repetition interval) is asynchronous with the D&DE clock, these control data must be transferred prior to the PRI in which the data are to be collected. The control data include a validity time to indicate to BATS when to act on the instructions. BATS starts to operate at the time of the next TRADEX pretrigger after the validity time. At a given time after the zero range trigger, which is also designated in the control instructions, BATS enables the acquisition logic. This logic remains enabled for a period of time designated in the control word as the acquisition window.

Figure III-5 is a functional block diagram of the BSP equipment. Its intent is to show in the clearest way the general signal flow and how the signals are modified and combined. The actual grouping of hardware elements, the relative complexity of the various parts, and the test paths are not indicated in this diagram.

The BATS target-detection process requires that the S-band chirp (and burst matched filter) outputs exceed a threshold level. The established threshold level is based on the noise level measured in a noise window prior to the acquisition window, a minimum cross-section designation from the computer, a maximum allowable false-alarm probability, and a level from the range sidelobe (estimator) circuit. The BATS automatically adjusts the threshold for changes in RF attenuator setting.

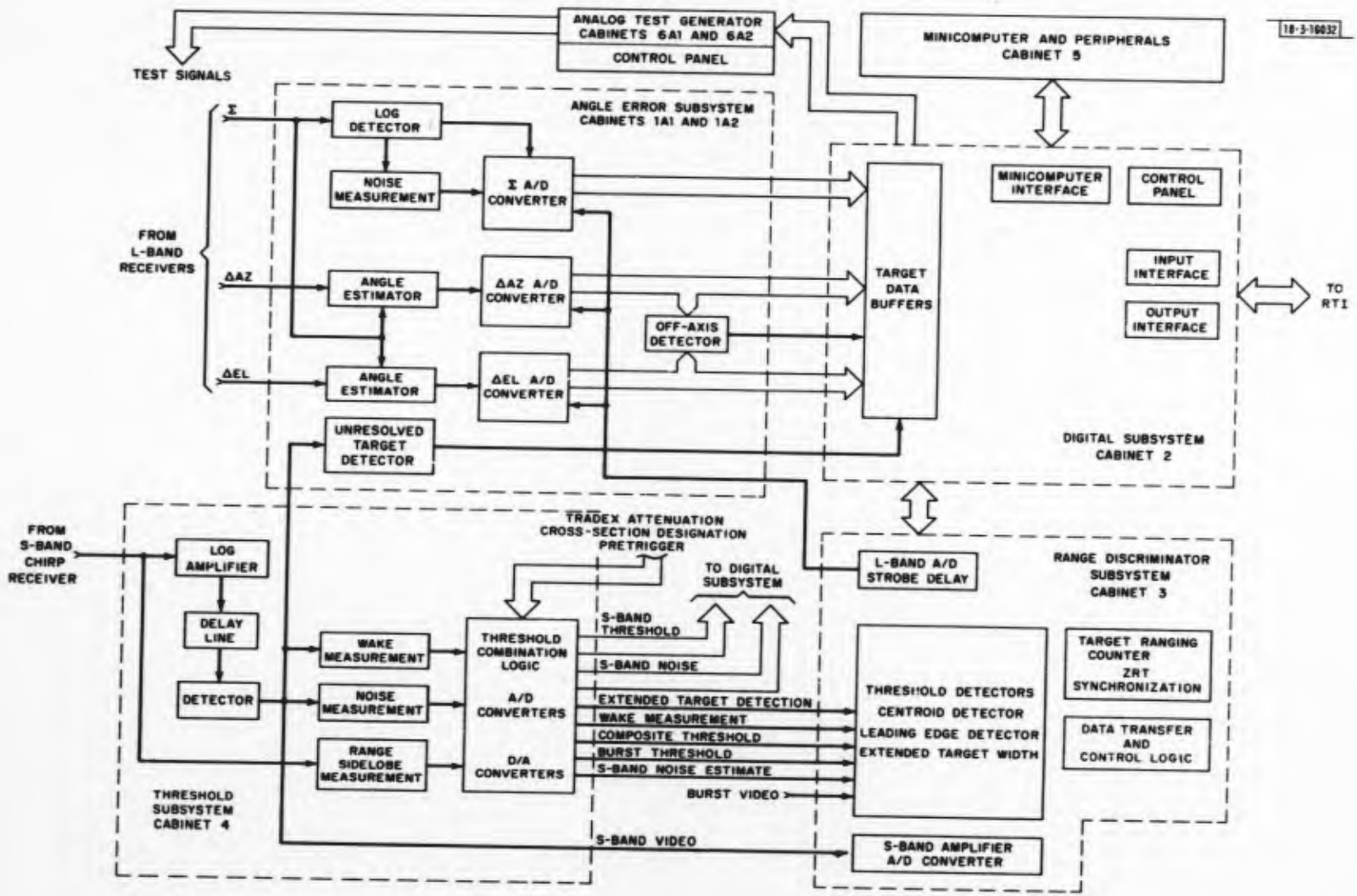


Fig. III-1. BSP subsystem organization.

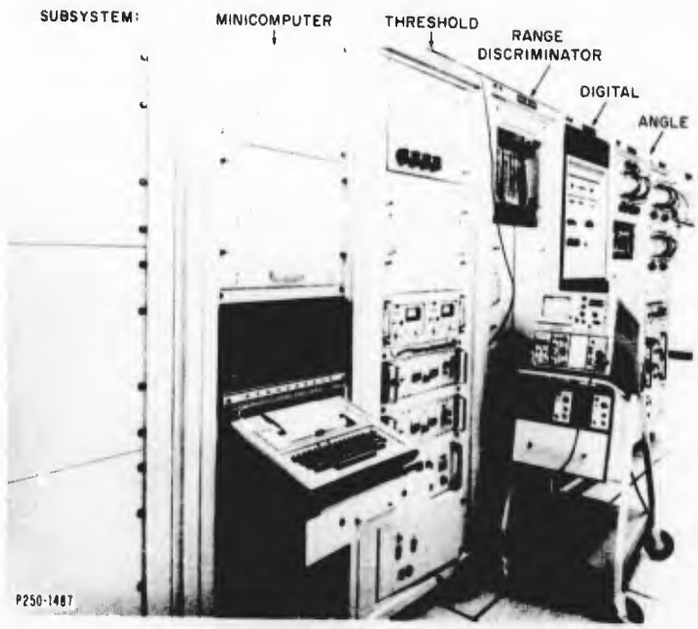


Fig. III-2. BATS SP equipment – front view.

Fig. III-3. BATS SP equipment – rear view.

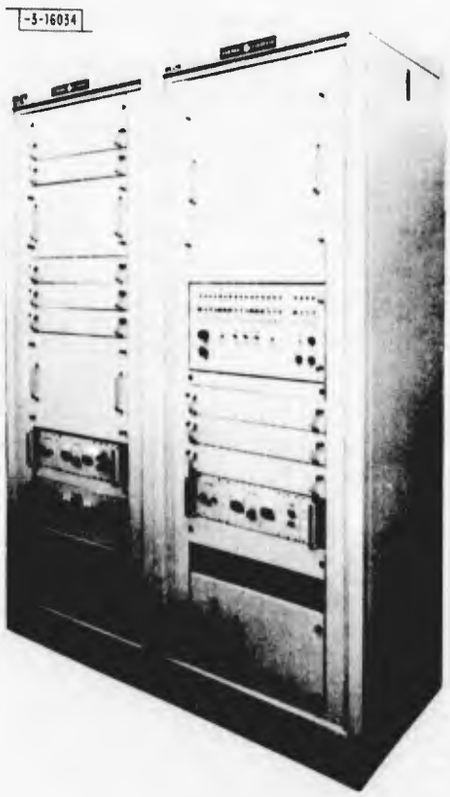


Fig. III-4. BATS analog test generator (ATG).

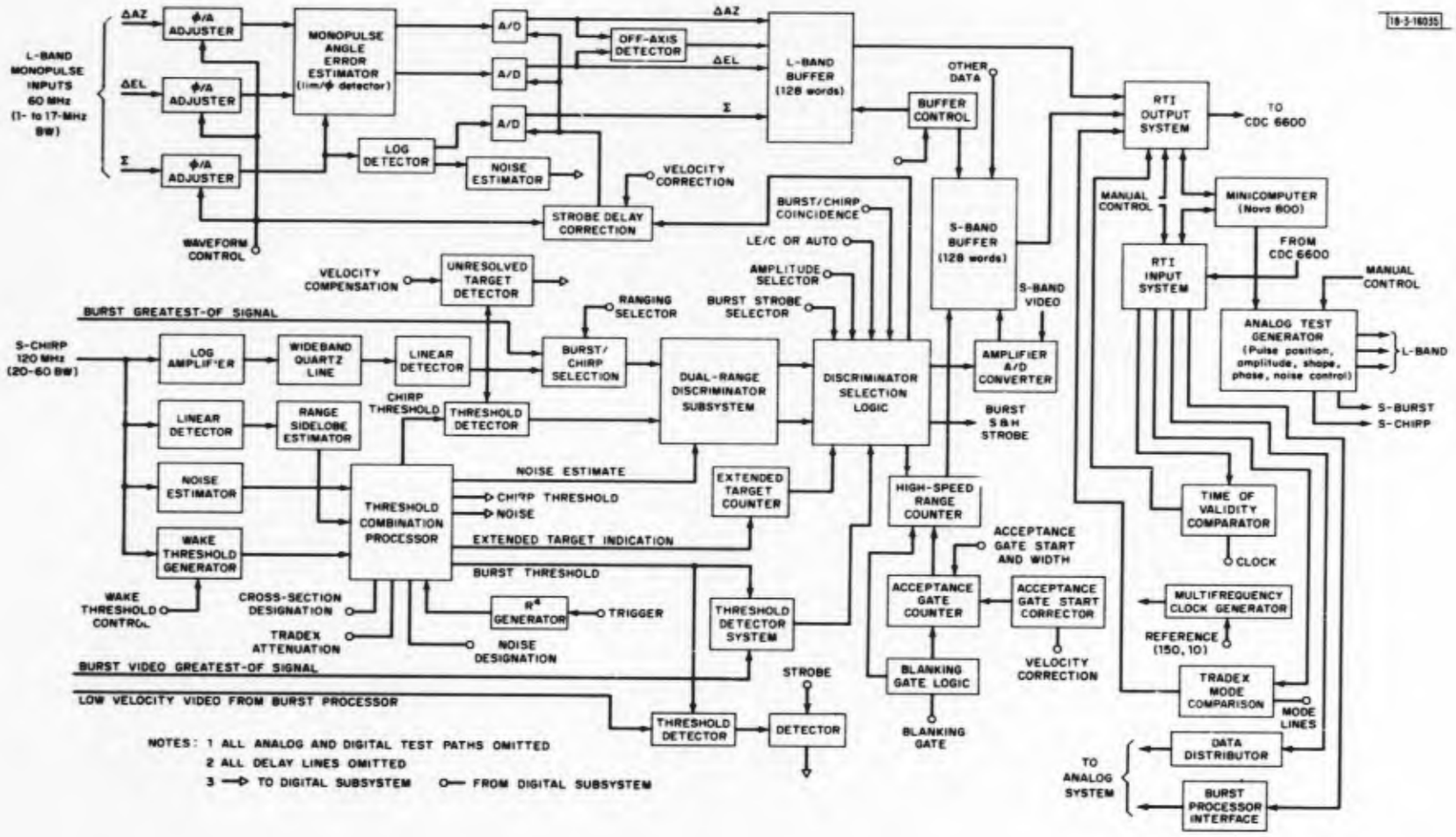


Fig. III-5. BATS SP functional block diagram.

Upon detection of a target, the BATS samples target amplitude, angle errors, noise levels, sidelobe level, and L-band interference, and tests for extended target conditions. The sampled data are held and the angle-error data are processed to see if they meet the off-axis angle threshold requirements. On-axis target data are transferred to the IC buffer memory and any off-axis data are dropped. The BATS can detect up to 128 targets per acquisition window, with a minimum target separation of 100 nsec. The system compensates for the difference in range-Doppler coupling between the S- and L-band signals by inserting more or less delay in the L-band angle error strobe path. Range-Doppler coupling compensation up to ±8 km/sec is required.

The measurements are formatted and stored in the buffer until read out by the RTI of the CDC 6600 computer. The RTI can call for data in any order from BATS or TADCO and return and read out the data in any order at any arbitrary time later. However, once having called for a readout from one of the equipments, the output remains connected to that equipment until readout is complete.

As shown in Fig. III-1, radar data inputs consist of the S-band chirp, a burst video output, and the L-band azimuth, elevation, and reference signals plus numerous triggers, mode, and timing signals. In interfacing the various TRADEX receivers to the BATS, IF delays have been added to assure time coincidence under zero Doppler conditions. Signal coincidence is an important prerequisite for the BATS detection and parameter measurements. The threshold subsystem receives the 120-MHz IF signal (after pulse compression) from TRADEX. In this subsystem, the signal is logarithmically amplified, delayed, and detected. The various parts of the threshold are generated and combined and outputs from this subsystem go to all the other subsystems.

The range discriminator subsystem receives the S-band video and the composite thresholds for both burst and chirp. The actual threshold comparison is made in this subsystem, and range strobes are produced for each detected target. All the high-speed (greater than 10 MHz) ranging and counting circuitry is located in this subsystem. The S-band A/D converter is also in this cabinet, as well as the L-band strobe delay circuitry.

The digital subsystem communicates with the RTI, minicomputer, and the rest of the BSP. It contains the 128-word target buffer, as well as the header and designation word registers; it also houses the manual control panel which can check the operation of the digital system. The minicomputer is tied in closely to the digital subsystem, but is housed in another cabinet. Its purpose is to automatically check out the digital subsystem and to control the operation of the analog test target generator in collecting test data.

The monopulse angle error cabinets receive 60-MHz IF signals derived from the L-band portion of the TRADEX radar. Angle-estimation circuitry takes measurements on the L-band signals when commanded by a suitably delayed S-band range strobe. An L-band amplitude measurement is also taken along with an estimate of the L-band noise. An additional circuit gives an indication of the presence of closely spaced targets that are resolved in S-band but not with L-band chirp, thereby invalidating the L-band measurement. Another circuit indicates if a target is substantially outside the S-band beam and will flag or inhibit the measurement.

In performing its functions, BATS requires mode and control inputs from TRADEX. The antenna azimuth and elevation are received through the RTI and reported with the target data, even though they are not presently used. The TRADEX receiver attenuator settings are also received through the RTI and are utilized in determining the proper threshold setting. TRADEX mode signals and gates are received directly to determine the proper selection of receiver

signals. An interrupt system is provided which checks the validity of the computer designation vs the TRADEX operating mode. A failure of this mode check results in an abort of the data request.

B. OVERALL SYSTEM TIMING

System timing and alignment are critical in the operation of BATS, which depends on close time coincidence of multiple-signal processing channels and thresholding circuits. The alignment problem is complicated by the use of inputs from differing pulse-compression networks having diverse range-Doppler coupling effects as a function of target velocity. The timing of the S-band chirp signal path is maintained as the reference time since it is utilized as the primary means for target detection and range measurement which, in turn, is referenced to TRADEX timing.

In accomplishing the detection and target parameter sampling functions, the BATS requires a real-time target threshold adjustment. The range sidelobe desensitization system used in this adjustment imposes the maximum time delays on the signal-processing path because of the need to adjust detection thresholds for range sidelobes which precede large amplitude targets. Hence, a delay is inserted into the signal paths to maintain the video time coincident with threshold processor output. The system delay requirements are discussed in more detail in the various sections of this report, but are briefly summarized here.

It can be seen from the system timing diagram (Fig. III-6) that the timing actually begins when the Time of Validity (T_o), that has been set by the designation word, comes true. After this time of validity mark, the system waits for the next TRADEX ZRT. The start of the acquisition window will be changed, depending on this waiting time, to compensate for anticipated target movement. This range extrapolation is stopped at the pre-ZRT trigger pulse and the value

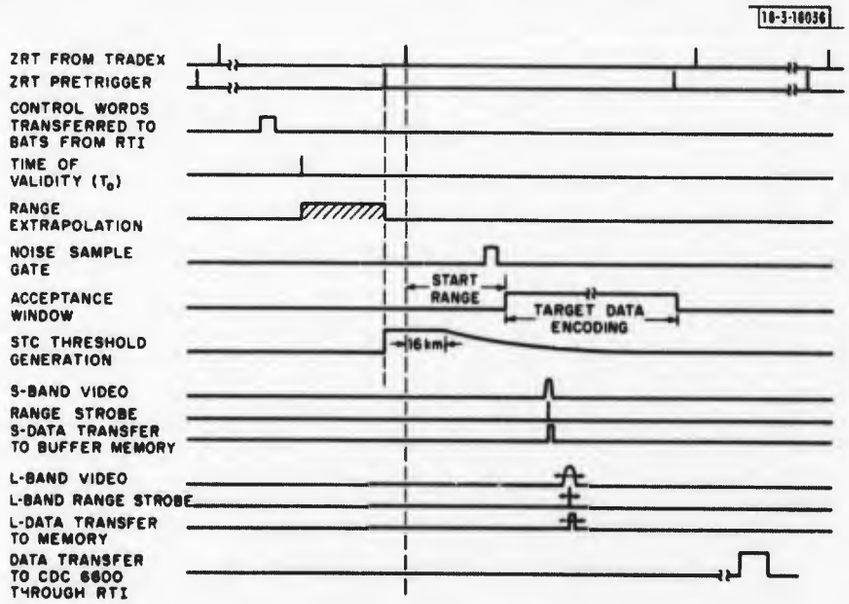


Fig. III-6. Basic timing diagram.

is loaded into the acquisition window counter. The acquisition range window counter starts at ZRT. Around 13 μsec before the start of the window, a noise measurement is made using the noise sample gate. The STC generator is also started at the ZRT time to provide automatic R^4 correction for a constant target cross section. A single S-band received target and its associated strobe pulse are shown in Fig. III-6. This strobe pulse, after range-Doppler correction, is also used to strobe the L-band data. After the close of the acceptance window, the data are ready to be transferred on command to the 6600 computer through the RTI.

In addition to the data exchange interface, the RTI also provides timing signals to the BSP so that operations may be synchronized and data may be time tagged. These timing signals are transmitted on two lines and include a 1.0-MHz clock and a reset line. The reset pulse occurs some time before the beginning of the mission (lift-off). The clock provides an unambiguous interval of slightly over 1 hour with its 32-bit binary counter. The D&DE computer stores the relationship between the time of day and the binary time. The T_o is the binary time at which the data in the request message are valid. A comparator is provided to compare T_o with the binary clock and, if binary time is greater than T_o, the request data are considered stale and an interrupt condition is set. If this condition is not masked, the BATS will send an interrupt to the RTI and will inhibit processing of the request. If T_o is greater than binary time, the BATS will wait until binary time equals T_o and then will commence operating on the data request. The binary clock is read at the ZRT time and this then becomes part of the output message header word.

IV. EQUIPMENT DESCRIPTION

Section A below describes the BATS signal processor (BSP) equipment, broken down into the six subsystems. The remaining parts of the BATS-related equipment will then be described in Secs. B through F.

A. BATS SIGNAL PROCESSOR (BSP)

1. Digital Subsystem (DSS)

a. Introduction

The DSS includes the computer interface, timing and control synchronizing, data buffering, and some target ranging functions required in BATS. An input- and output-control interface unit communicates with the CDC 6600 computer through a QSE 6158 RTI in order to transfer control instruction words from the CDC 6600, and to provide the capability to selectively read data from various portions of BATS. Mode control logic guides the data to the various control registers under normal mission mode operation, and throughout the rest of the digital system when in a test mode. A simplified block diagram of the DSS is shown in Fig. IV-1. The data paths and modes in the system are specified by the RTI Key Controls and by an operational control word. The digital portion of BATS is similar in concept to the TADCO unit at KREMS. The BATS and the TADCO will share a common RTI input and output line – channels 0 and 1, respectively.

Various gates and strobes required to control BATS are also provided in the DSS including generating an acceptance window gate corrected for target motion. Target data sampled by the Analog Subsystem are stored in a 128-word, 60-bit Random Access Memory (RAM) as each target

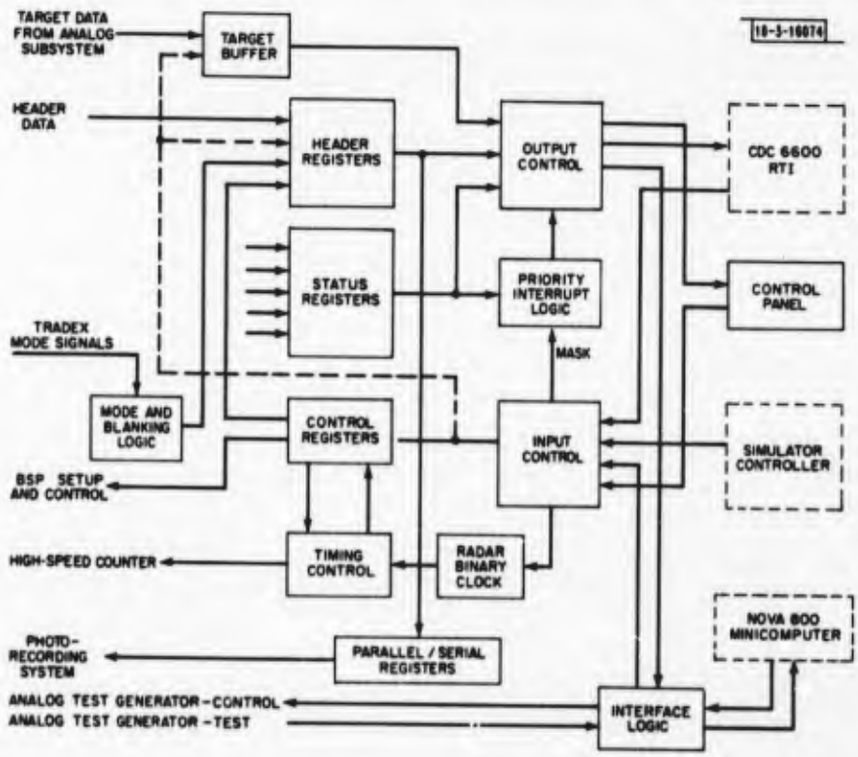


Fig. IV-1. Simplified block diagram of DSS.

detection is received. Header registers provide a collection point for additional data gathered at various times in the operation cycle. Once the operation cycle is completed, the RTI can initiate a request to read the buffer starting with the three header words first and then the target words.

In addition to the Analog Subsystem target data input, the BATS DSS accepts target data through an interface to the Simulator Controller. When in a simulate mode, BATS does not gather data from TRADEX. Instead, simulated target digital data from the computer are supplied to the BATS DSS, stored in the data buffer, and then transferred back to the CDC 6600 via the RTI.

Two methods of reporting status or errors to the CDC 6600 are provided. The External Device (ED) Status is reported from the RTI transmit and receive interfaces when BATS is selected. An interrupt interface is also provided to report any system operation errors which may halt BATS operation. A computer-generated mask is stored in a masking register to override (if desired) the status bits which generate these interrupts to the 6600. A status register also collects overall BATS operational status for reporting through the normal data channel upon request by the 6600.

Extensive testing paths can be selectively established within the DSS to allow manual fault location from the Manual Control and Test Panel. Data can be loaded into registers, counters, and the target buffer and then displayed. An interface with the Nova 800 minicomputer and analog test generator is provided to allow calibration and alignment of BATS, as well as automatic testing of the DSS data paths. A communication path is also provided between the CDC 6600 RTI and the Nova 800 minicomputer.

b. RTI (6600 Computer) Interface

In normal system operation, BATS interfaces with an input and an output channel of the RTI (0 and 1). Each of these is a simplex channel by which the RTI transmits data requests to the BATS input interface and receives the resultant data from the BATS output interface. The data requests include the control words and control data to operate BATS in any of the mission, calibration, or computer-controlled test modes. The input and output interfaces are similar in operation, and the device selection procedure and data control and transfer modes are very much the same for both channels. The CDC 6600 channel programs provide for independent operation of the input and output channels of the RTI for device selection and timing of the selection.

Each RTI channel interface contains a 3-bit address for device selection which is designated as ED (External Device) Select. Each channel also contains three Control Key lines to control the mode or the operational procedure of that device. Sixty data lines in each channel provide the means of transmitting the designation data and receiving the device response. Data transfer in either direction does not exceed 300 kHz. Lines for transmitting the SOM (Start of Message) and the EOM (End of Message) define the bounds of the data set. In addition to these are the "handshaking" signals in each channel that control the device responses and the data exchange between the external device and the RTI. The following outlines the operation of this interface.

c. RTI Input Control (Channel 0)

The RTI channel 0 selects BATS input control by placing the SELECT control line at a logic "1" along with the three EXTERNAL DEVICE SELECT lines in a 011 (BATS) state. The CONTROL KEY lines from the RTI are sampled and loaded into a holding register. BATS then responds (within 10 μsec) with a DATA REPLY level (logic "1"). Following this selection, the RTI sends

the first 60-bit data word with a DATA READY level. BATS accepts these data and decodes the control keys, provided that channel 1 (output channel) is not processing mission information; otherwise, the DATA READY is not accepted until mission data gathering is completed. The DATA READY is responded to by a DATA REPLY from BATS which drops when the DATA READY drops. This process is repeated until all words of the message have been transferred. The first data word of a message is accompanied by a SOM signal, and the last word is accompanied by an EOM signal. (A one-word message is accompanied by both SOM and EOM signals.) The BATS DSS deselects on the occurrence of the EOM by resetting the select control flip-flop. Channel 0 can be locked out either by manual selection from the DSS Control Panel or by the SIMULATE MODE control line being raised from the Simulator Controller. Once the input has been selected, a complete data transfer takes place. If, for any reason, deselection of BATS occurs, the sequence must be completely re-initiated from the beginning.

The BATS input timing and control system delays the BATS Data Reply to the RTI messages of selection and data to allow sufficient time for setting control flip-flops and Key code storage during selection, and for storing and distributing control words during data transmission. Approximately 1.5 μsec are required to store received data, and the average time taken by the RTI to transmit data is approximately 3 μsec/word.

d. RTI Output Control (Channel 1)

The RTI channel selects BATS output control by placing the SELECT control at a logic "1" along with the three ED Select lines in a 011 (BATS) state. BATS then responds (within 10 μsec) with a RESUME level. Following this selection, the BATS DSS sends a DATA READY and a SOM when it has the first 60-bit data word on the lines to the RTI. (If this is a one-word transfer, an EOM is also present.) The EOM accompanies the last DATA READY for the last word to be transferred, and the DSS then deselects. If deselection of BATS takes place prior to processing the full data-transfer sequence, the memory address counters are reset back to zero.

e. Control Keys and Status Signals

The Control Key signals are employed to control the BATS operating modes or perform other functions as assigned for the particular interface channel. They consist of a 3-bit interface each for both the input and output channels. Out of the eight possible conditions, five are used and defined for the input channel and three for the output channels. Details are given in the RTI Interface Specifications, Sec. V-C.

The ED Status signals are employed to notify the RTI, upon selection of BATS, as to its operational state. It is a 3-bit interface and indicates whether or not BATS is in an operational state or in a local mode.

f. Designation and Operational Control Words

Three designation words are transferred to the BATS DSS in a mission mode. They control all the timing and setup operations within BATS. The operational control word is transferred to the BATS DSS only under Control Key 001. It configures the data paths within the DSS, as well as defining the operational modes. These words are defined in the RTI interface specifications, Sec. V-C.

g. Status Words

A 30-bit status register is provided to collect status as defined in the RTI specifications. An interrupt signal is generated which goes to the RTI with each new status bit setting, provided that the group mask bit is not set by the operational control word. Removing the mask does not cause an interrupt to be generated even though the bit may be already set. The mask does not inhibit the setting and storing of the status bits. The status register may be reset only by the reading of its contents, by turning the power on, or by local control panel operations. The INTERRUPT is a level sent to the RTI which drops with receipt of INTERRUPT RESUME signal from the RTI.

A 1.0-MHz signal is sent to the DSS from the RTI which is utilized to drive the BATS Radar Binary Clock for system synchronization. A reset signal is sent to the DSS from the RTI to set the 32-bit Binary Radar Clock to zero.

h. Header Registers

The BATS output data buffer includes the message header register, the target data buffer, the interim storage buffers, and the data control logic required in data handling. Various portions of the header data are generated throughout the data-gathering cycle, and access to the various sections is required when the data become available. The header register is therefore kept separate from the target data buffer. The details of each header word are outlined in Sec. V-C.

Data from the analog equipment are loaded into the three DSS header registers during the operational cycle. Individual load strobes load the various fields at appropriate times. Test data may also be cycled from the various input sources (RTI, MANUAL, Minicomputer). In addition, the simulator controller can also load three header words into these registers when in the simulate mode. Data are sampled once during the operational cycle, and no new data can be loaded until the registers are read or a master clear is received. At the time of data transmission to the RTI, the three header words are transmitted first, followed by the variable-length target data message from the target buffer.

i. Target Buffer

The target buffer is capable of loading 60-bit target words at a maximum rate of 9.375 MHz. The target buffer loads data into three separately addressed sections at different times; the three sections are: L-band, S-band, and Target Extent, as indicated in Fig. IV-2 which shows the buffer organization. Each 128-word section is addressed as two independent 64-word sections for even/odd word loading. All load strobes are generated by the High Speed Data Transfer logic located in the Range Discriminator.

The target buffer contains a 7-stage S-BAND Address Counter (SBAC) and an L-BAND Address Counter (LBAC) of 7 stages. Both counters are cleared to zero at the start of an operation. When the ACCEPTANCE WINDOW opens, the SBAC is incremented with each S-BAND LOAD STROBE (SBLS) and S-BAND data are written into the memory. This continues as long as SBLSs occur or until 128 addresses are loaded. Any further SBLSs cause an OVERFLOW status interrupt to be set and additional S-BAND data locked out. When the ACCEPTANCE WINDOW closes, SBLSs are inhibited.

Extended Target information is loaded into a separate section of the buffer in an address corresponding to S-BAND target data. An EXTENDED TARGET FLAG (Wake Indicator) will

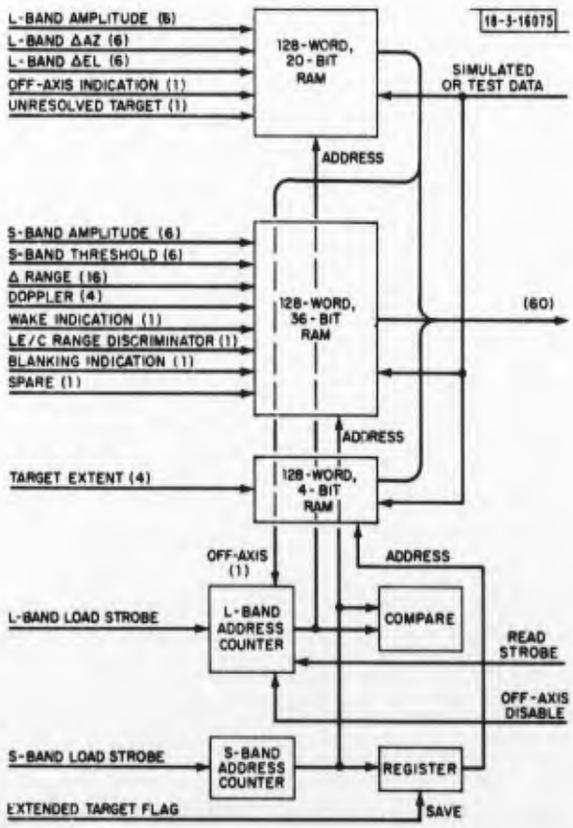


Fig. IV-2. Target buffer organization.

occur within 100 nsec of a previous SBLS. The SBAC address is saved from that SBLS with an EXTENDED TARGET FLAG occurrence. When the EXTENDED TARGET FLAG drops, the 4 bits of Target Extent will be loaded into that address in the Target Extent section of the buffer memory. Any additional SBLSs occurring with the EXTENDED TARGET FLAG will be handled by loading the S-BAND section of the RAM. Therefore, only the first Target Word in the buffer for each EXTENDED Target will contain the Target Extent information.

Provision is made for the L-BAND section of the memory to receive data up to 63 μsec after the S-BAND data. The LBAC operates independently of the SBAC. When the ACCEPTANCE WINDOW closes, the LBAC is allowed to accept LBLSs until it equals the SBAC number or until a 63-μsec timeout occurs. When the LBAC equals the SBAC target word, data are lined up in the RAM. Status/Priority Interrupts will occur when: LBAC $\neq$ SBAC 63 μsec after the ACCEPTANCE WINDOW has closed (data incomplete) or SBLSs or LBLSs occur when the RAM is full (overflow). When a Data Incomplete occurs, S-BAND data will still be sent to the RTI.

When all the data have been stored, the SBAC contents are transferred to the Header Registers as a TARGET COUNT. When the RTI initiates a transfer or read of the memory contents back to RTI channel 1 , the LBAC is cleared and the SBAC holds the last data address. The LBAC now simultaneously addresses all memory sections to read target data words until the LBAC = SBAC which generates an EOM indication.

Off-Axis data are identified by bit 55 in the Target Word. The OAE (bit 41) of Designation Word 2 specifies an Off-Axis Enable when equal to a logic 0, and target words will be transferred uninhibited. If the OAE bit is set to a logic 1, then target words with bit 55 set are discarded and not returned to the RTI.

j. Simulator Controller Interface

When simulate mode is designated by the CDC 6600 computer, the BATS no longer will gather data from TRADEX. Instead, simulated data will be generated by the 6600 and supplied to BATS in digital form via the Simulator Controller Connection. These simulated data are sent directly to and stored in the data buffer and then transferred back to the 6600 via the RTI exactly as though they were real data. The Simulator Controller interface with BATS uses the identical input control logic as the RTI channel 0. The Simulator Controller replaces RTI channel 0 input when the SIMULATE level is a logic 1 from the Simulator Controller. It remains at a logic 1 for the entire simulate operation during which all output signals to the analog equipment are deactivated and all inputs from the analog equipment are locked out. All data transfers are made to the header registers and the target buffer, with the first three words being transferred into header registers 1, 2, and 3. The remaining transfers are all made to the target buffer. The ED status is the same as for the RTI, but the meanings of the control keys are changed as outlined in the Interface Specifications, Sec. V-C.

k. TRADEX Interface

The Digital Subsystem receives the TRADEX Mode signals listed in the interface specifications (Sec. V-A). These signals are decoded and held, and compared with the R-mode field in Designation Word 1. If the mode does not compare, the request is aborted and a status bit is set generating a priority interrupt. The modes are only checked when in a normal mission mode or a modified mission mode (computer mode A).

The following TRADEX mode signals are also used to set a status bit if they occur during a mission (or modified mission) mode, if present with a valid ZRT pretrigger:

L-Band Dropped Pulse
S-Band Dropped Pulse
S-Unscheduled Dropped Pulse
L-Unscheduled Dropped Pulse

The blanking gate is passed on from the high-speed logic which receives it from the TRADEX radar. This gate is compared against the acceptance window and two bits stored in the header register, Word 2. They indicate if the leading edge of the window is in the blanked region, if the trailing edge is in the blanked region, or if the entire window is encompassed by the blanked region. A target word is also sent from the Range Discriminator to mark the range of the blanking gate transition if it occurred during the acceptance window.

l. Control Registers

In a normal mission mode, data received from the RTI through the Input Control Interface are loaded into three control registers. From this point the setup data, such as TRADEX L-Band and S-Band Attenuation, Cross-Section Designation, Threshold Designation, Range Rate, and Track Designate are sent directly to the IF and Analog Subsystems. In addition to normal mission mode, other computer modes exist for special test functions and are established by the Operational Control (OC) Word which is loaded into the OC Register. A summary of the OC Words and their use is presented in Sec. V-C.

m. Range Control

One of the designation parameters in BATS operation is the Acceptance Gate Start. This gate start is in reality a range which is valid at time T_o. If T_o could be designated such that it occurred a short time before ZRT, the error of the gate start could be kept quite small. If, for example, T_o were within 100 μsec of ZRT, the error for a target with a range rate of 8 km/sec would be less than 1 m. However, the time uncertainty of the ZRT is much greater than this because the radar prf is asynchronous with respect to time. The time uncertainty of a ZRT with respect to a given T_o may be equal to the PRI of the radar. In the lowest prf band, this time difference between T_o and the next ZRT can be as much as 10 msec. This means that the designated range to the start of the acceptance gate could be in error by 80 m for a target range rate of 8 km/sec if the range is not modified for target motion. The range control logic provides the capability for the range to be updated to correct for target motion between T_o and ZRT. T_o is sent to a comparator for comparison with the 32-bit Binary Radar Clock (LSB = 1 μsec). If the clock time is greater than T_o, the request is considered stale and an interrupt condition is set. If it is not greater, the Acceptance Gate Start time is loaded into a counter which provides the capability to correct the designated acceptance gate start range for target motion between the occurrence of T_o and ZRT. This is accomplished according to the Target Range Rate parameter stored in the control register.

Upon receipt of a ZRT Pretrigger from TRADEX, the Extrapolation Rate Control is halted and the corrected Acceptance Window Start Range is loaded into the Header Register. At ZRT, the Binary Radar Clock Time is also loaded into the Header Register. The corrected Acceptance Window Start time, 16 bits, is also loaded by the High Speed Target Ranging logic located in the Range Discriminator subsystem into the window counter. The Window Start Counter starts counting down to set the time of the beginning of the Acceptance Window. Pre-acceptance Window signals such as the Noise Sample Gate (10 μsec) are decoded off the Window Start Counter by the DSS logic.

When operating with the minicomputer, an artificial ZRT pretrigger and ZRT are generated by comparing the Test ZRT field in the OC register with the Radar Binary Clock.

n. Minicomputer Interface

A general-purpose interface (Input-Output) between the DSS and the minicomputer cabinet allows communication between the minicomputer and one of each of three areas for test purposes. The three areas are: Digital Subsystem (DSS), Analog Test Generator (ATG), and Real-Time Interface (RTI). Communication occurs with only one interface at a time.

The minicomputer interface is manually selected from the control panel locking out the RTI interface. The minicomputer then can control BATS in a manner identical to the RTI. A command word is first sent to the DSS to set up the Input and/or Output Control Keys. Other control bits establish the communication interface. The BATS DSS can be set up to operate in mission mode or Computer Modes A through E. All data transferred from the minicomputer are packed into the 60-bit RTI word format in the DSS. Conversely, 60-bit words transferred to the minicomputer are unpacked to provide 16-bit words.

By proper selection of the command word, the system has the option of running on a continuous cycle, resetting at the end of the ACCEPTANCE WINDOW, or not sending data back to the minicomputer. The cycle will allow checking the BATS Analog Equipment until it is commanded to stop. Status is read from the DSS with an Interrupt to the minicomputer in the same fashion as the RTI.

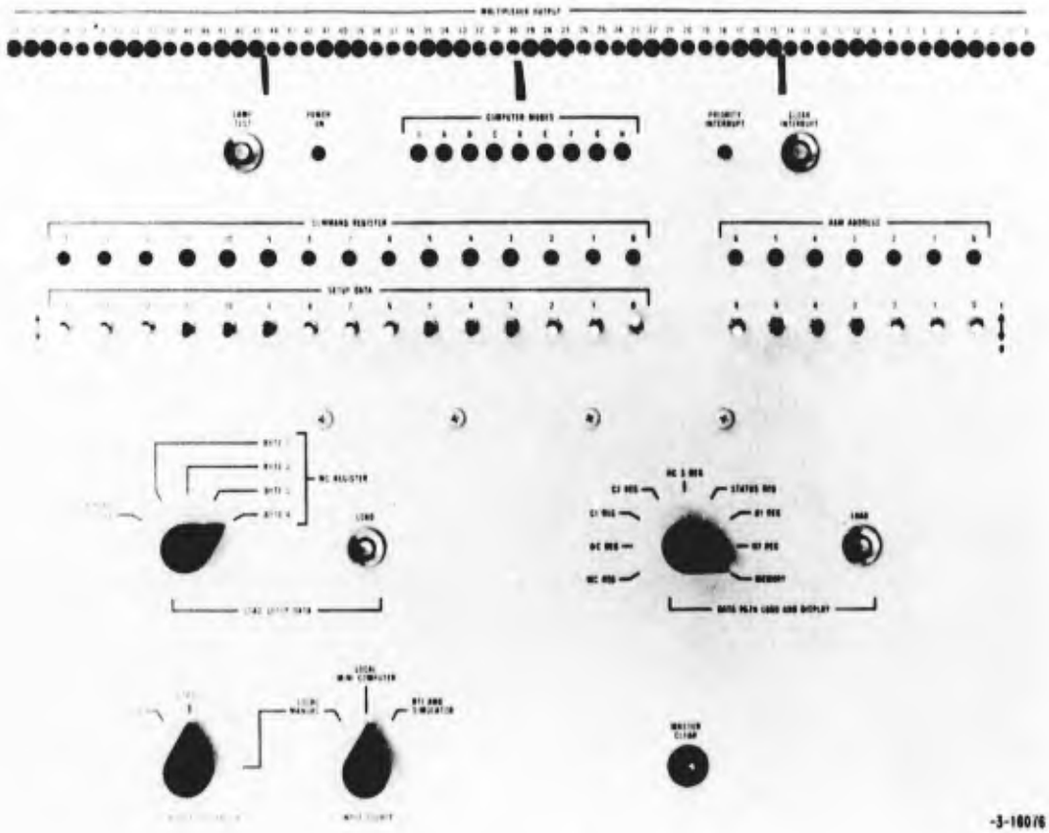


Fig. IV-3. DSS Control and Test Panel.

When the ATG is connected, it receives all control information from the minicomputer through the DSS. Its interface is selected when the manual control panel selects the minicomputer. The RTI can also initiate transfer from or to the minicomputer (Computer Modes G and H).

o. Control and Test Panel

The DSS Control and Test Panel contains the necessary switches and indicators to allow troubleshooting of the DSS independent of any other source. The provision to statically load and display critical registers within the DSS is provided in LOCAL operation. An automatic cycling feature is also provided in order to provide some dynamic testing in local operation. Manual switches can be activated only while in LOCAL MANUAL Operation.

A photograph of the control panel is shown in Fig. IV-3. A summary of the controls follows:

Power On/Off Indicator	Indicates prime power on.
Master Clear Pushbutton	Clears the DSS to make it ready for operation.
Mode Indicators	Eight lamps to indicate which of 8 modes the DSS is in.
Multiplexer Output Display	Sixty lamps display the contents of a manually selected register as determined by the Data Path Load and Display Switch Position.
RAM Address Display	Seven lamps display the RAM Address Counter output.
RAM Address Toggle Switches	Seven toggle switches control the RAM starting address during LOCAL-MANUAL operation.
Setup Data Toggle Switches	Fifteen toggle switches representing 1 byte of 4 in a 60-bit word, load the MC Register or give a 15-bit command. These switches are used in conjunction with the Load Setup Data push button.
Load Setup Data Rotary Switch	Used to select which byte the Setup Data Toggle switches represent to be loaded into the Memory Control (MC) register. When in the CMD REG position, it causes the SETUP DATA to be loaded into the minicomputer command register.
LOAD (SETUP Data) Push Button	Causes the state of the sixteen setup data toggle switches to be loaded into the position of the MC register selected by the associated rotary switch or the CMD register.
Data Path Load and Display Switch	A 10-position rotary switch selects the source of the 60 data lamps when in the Local-Manual mode. It also selects which source the MEMORY CONTROL register is to be loaded into when depressing the Data Path Load push button.
Data Path Load Push Button	Causes a 60-bit data transfer to take place from the MC register to the selected Data Path destination.

Interrupt Display Lamp	Displays the state of the DSS priority interrupt request.
Interrupt Resume and Clear Push Button	Supplies an Interrupt Resume pulse and clears the status register when in the local manual mode.
Input Source Selection Rotary Switch	Controls the DSS communication source and designation. The three positions are: (a) RTI and Simulator Controller (b) Local Minicomputer (c) Local Manual. Only Local Manual will enable any of the other panel switches.
Local Manual Operation Rotary Switch	A two-position switch selecting an Input and Output Control Dynamic operation when in CYCLE position, and a Static register operation when in STATIC position.

The CYCLE position starts a looping operation as determined by a previous statically selected mode. The mode is determined by manually storing Control Keys into the MINI-COMMAND Register and also loading an Operational Control Word into the appropriate register while in the STATIC position of this switch. When subsequently switching to a CYCLE position, the DSS will begin the dynamic test. Stopping this operation takes place when this switch is turned back to the STATIC position. In any case, the RAM address is derived from the seven RAM address switches and not the OC Word. In dynamic test, the RAM address was the starting address when it was in STATIC position. It is the address to be written into and displayed if selected by the Data Path Load and Display switch.

2. Threshold Subsystem

a. Introduction

The BATS Threshold Subsystem provides for generation of the threshold values which are used in the detection of targets. Additional functions are also included, as was shown in Fig. III-1. The Threshold Subsystem receives inputs from the TRADEX radar, the Digital Subsystem, Analog Test Generator, and Range Discriminator. It sends outputs to the Digital Subsystem and the Range Discriminator.

The equipment in the Threshold Subsystem cabinet provides the following basic functions:

Delays and log detects the S-band chirp signal.
Generates dynamic thresholds.
Generates a priori thresholds.
Combines the dynamic and a priori thresholds.

The threshold computation is based on the following seven factors.

(1) Noise Level from the radar receiver. An estimate is made of the noise level in the receiver system prior to the start of the acceptance window.

(2) Range-Sidelobe Interference. The threshold increases when the sidelobes from a large target near in range are estimated to be above the established threshold level.

This prevents the system from producing range marks on the range sidelobes of a large target.

(3) Wake. A special threshold is established for extended (waking) target conditions. When this threshold exceeds the threshold for noise plus range-sidelobe level, the wake threshold is automatically enabled.

(4) RF Attenuation. The threshold automatically changes to compensate for changes in the TRADEX RF attenuator settings. This can maintain the threshold at a fixed target cross section no matter how the TRADEX attenuators are set.

(5) Minimum Cross Section. This designates a minimum target cross section. The value will include a TRADEX calibration constant.

(6) Threshold Designation. Sets the threshold at a specific number of decibels above the measured noise and estimated sidelobe level.

(7) Target Range. A STC is applied as a function of range to correct for the R^4 variation in target amplitude.

b. CFAR Considerations

The BATS is designed to have a controlled false-alarm rate to prevent excessive false target reports that could prevent detection of valid targets by overloading the target buffer. At short ranges, the minimum target cross-section designation will be considerably above the noise level so that it will prevent false target reports. At longer ranges, the noise and range-sidelobe interference level will have the greatest effect on the number of false target reports unless a high target cross-section designation occurs.

The detection threshold is a combination of many signals and can be broken down into two main components, (1) cross-section or a priori thresholds, and (2) noise and interference or dynamic threshold. The BSP uses the greater of the two signals as the detection threshold. For the cross-section contribution, the 6600 computer specifies a minimum acceptable radar cross section that is correct at a specified range. The BSP uses this value and also corrects for the R^4 variation and changes in the TRADEX attenuator settings.

The noise and interference contribution is more complex. The noise level is measured by a noise gate, and a designated level is added to the measured noise value to set the detection threshold. However, when a strong point target is present, the sidelobes of the target might be above the noise level. This range-sidelobe level is estimated and a signal added to the threshold to raise it above the sidelobe level to prevent excessive false alarms. Furthermore, if the wake threshold is enabled, an additional signal is added to the detection threshold so that only the beginning of an extended target (waking target) is allowed above the detection threshold. Typical received signals and thresholds are illustrated in Fig. IV-4. Also shown are the range marks expected, including some possible false marks on the trailing edge of the extended target. This diagram shows the threshold rising in the presence of range sidelobes, and the action of the wake threshold.

c. Log Detection and Delay

One of the functions included in the Threshold Subsystem is to logarithmically amplify the 120-MHz TRADEX IF signal, delay it by 35.2 μsec, and then detect the signal. By performing

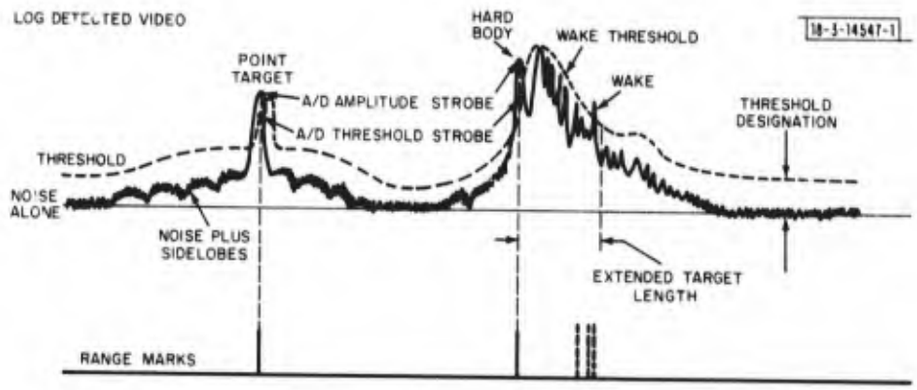


Fig. IV-4. Typical BATS received signals and measurements.

these functions in this order, a greater dynamic range is achieved than if the signal was delayed before being log-detected. The IF delay line has a spurious level of −50 dB, which would limit the dynamic range to this level if the signal was not log-compressed before passing through the delay line.

This special IF logarithmic amplifier was designed and constructed at Lincoln Laboratory and has the following characteristics:

Center frequency	120 MHz
Log range	0 to −70 dBm
Log accuracy	±1 dB
Log slope	≈14 mV/dB
Rise time	20 nsec/20 dB
Fall time	40 nsec/20 dB
Input and output impedance	50 ohms

The delay line used in this application is a nondispersive, quartz ultrasonic type whose characteristics are as follows:

Center frequency	120 MHz
Bandwidth	±15 MHz ± 0.5 dB
	±30 MHz ± 1.0 dB
Nominal delay	35.2 μsec ± 0.01
Delay dispersion	Less than ±2 nsec over ±30 MHz
Delay stability	±1 nsec
Attenuation	42 dB
Attenuation stability	0.2 dB
Spurious response	50 dB

The envelope detector used in this application is a specially designed unit at 120 MHz having a linear range of 40 dB. It is used both in this application and as the detector preceding the range-sidelobe estimator circuit. This combination of log amplifier, delay, and linear detection provides for the least amount of signal degradation.

d. Range-Sidelobe Estimation

The time- (range-) sidelobe level on nearby targets must be estimated so that the threshold can be adjusted. Targets (and their wakes) will have time sidelobes that may overlap desired targets. The threshold must be raised above these sidelobes to prevent false alarms on the sidelobes and still allow a reasonable detection probability of a desired target. The time sidelobes for a compressed chirp waveform extend out to approximately the uncompressed pulse length and, therefore, the time-sidelobe level estimate should extend to that range.

When more than one target exists within the sidelobe region, the time-sidelobe estimates of these targets must be combined in a way to provide a reasonable estimate of the resultant time-sidelobe level. The actual sidelobes of multiple targets add vectorially. An exact sidelobe estimate, however, cannot be calculated for a multiple-target situation. All that is known is that the vector sum of the sidelobes is less than the sum of the magnitudes of the component vectors. However, the sum of the sidelobe power levels is used in the BSP as an approximation to the actual sidelobe level.

For a well-designed linear FM pulse-compression system, the envelope of the time-sidelobe pattern is a slowly varying function of time; that is, the peaks of several adjacent time sidelobes will have essentially equal values. Figure IV-5 shows the theoretical envelope of the sidelobes for the TRADEX radar. The envelope of the sidelobe pattern can be estimated with a small number of delay-line elements. An 8-step (4 on either side of the compressed pulse) approximation to the sidelobe envelope provides a reasonable match (2 dB) to the actual sidelobe envelope.

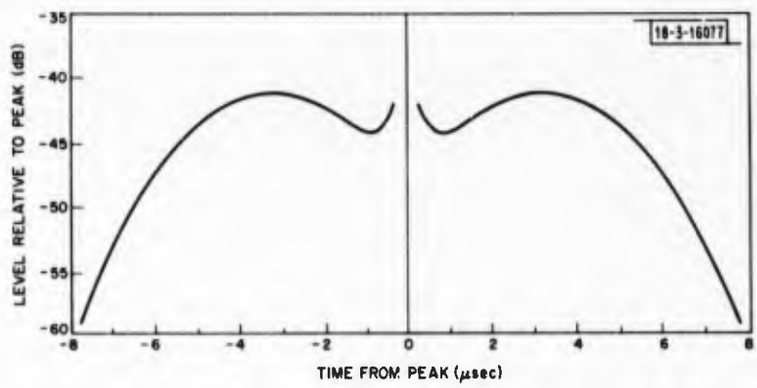


Fig. IV-5. Peak range-sidelobe level.

The range-sidelobe estimation technique shown in Fig. IV-6 uses linearly detected target returns to generate the target sidelobe estimate. The 120-MHz IF input is detected, filtered, and sent down a tapped delay line. To provide an RSS (Root of the Sum of the Squares) sum of the time-sidelobe envelope for any target distribution, an input filter first stretches the input signal and provides the RSS sum of all targets that were received during a 1.6-μsec interval (tapped delay line spacing). The filter implementation uses a succession of four individual delay lines, each delay matched to the 3-dB width of its input signal. The output of each delay line is RSS combined with the undelayed signal. Consequently, the resultant output for a single target is a pulse whose duration is 16 times the input pulse width. This signal is sent to the 11.2-μsec tapped delay line. Each delay line tap of 1.6 μsec has an individual gain adjustment to allow final tailoring of the resultant time-sidelobe envelope to the actual time-sidelobe pattern

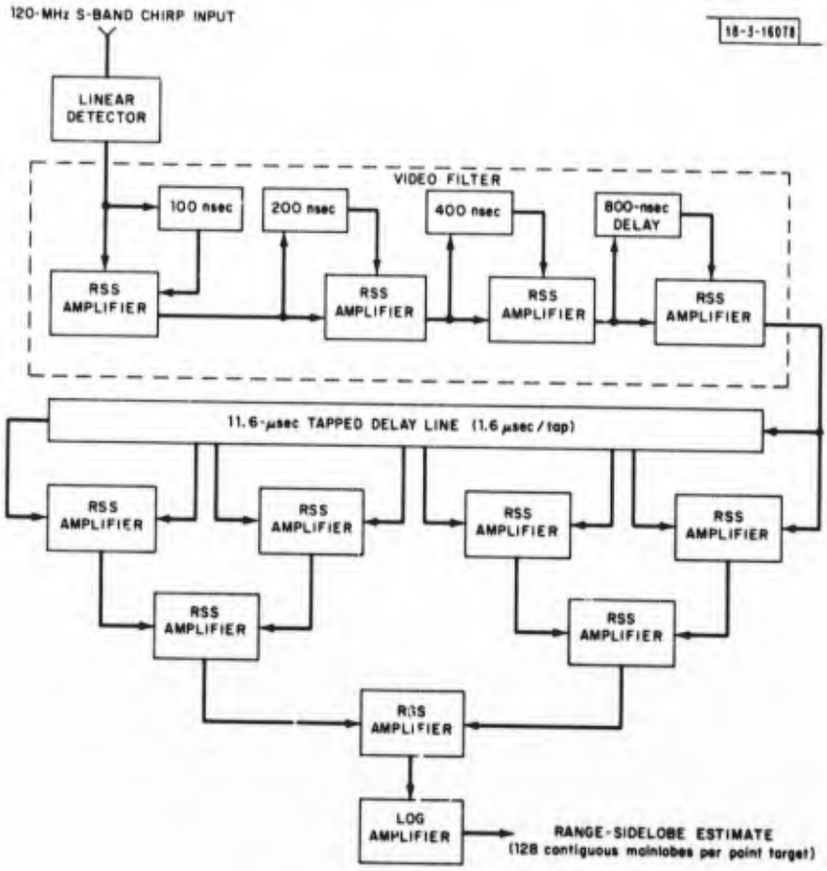


Fig. IV-6. Range-sidelobe estimator.

of the radar. These eight gain-adjusted signals are sent to a RSS circuit tree to provide the combination which is an approximation of the RSS of the signals. A final video log amplifier converts the signal to a log form for use in the threshold combination.

e. Noise Measurement

As a part of the threshold control, an estimate of the thermal noise level is required to prevent excessive false alarms when high receiver noise exists. This estimate ideally should be taken within a range interval that contains no targets. Since there can be no guarantee that a target will not occur within the noise measurement gate, the noise measurement must be implemented so that it minimizes the effect of a target in the noise gate. At the input of the noise measurement circuit, a 70-dB range of signals is possible. When log detected noise is averaged, at least 57 range cell samples are required to keep the error to within 1 dB in the presence of a single strong interfering target.

At least 31 independent samples of noise have to be averaged to assure a noise estimate good to 1 dB in a noise-only environment; to reduce the error to 0.6 dB would require about 100 samples. For a linear FM pulse at bandwidth B and with Hamming frequency weighting, an independent sample of noise occurs each 2.11/B sec. To be independent, the spacing between the samples must be equal to or greater than the spacing required for the autocorrelation function of noise to drop to 10 percent of the peak value. For a B of 17.6 MHz, an independent noise sample will

occur each 0.120 μsec. A noise-averaging interval of 10 μsec will provide for the equivalent of 83 samples, and this is the value that has been implemented.

The thermal noise estimation circuits are shown in the Threshold Subsystem block diagram (Fig. IV-7). During the 10-μsec noise sample gate interval preceding the acceptance gate window, 30 dB of gain is added to provide an increase in noise power to the detector system, thus insuring it is in its logging range. The noise gate occurs 13 μsec prior to the start of the acceptance window to allow 3 μsec for the gate transients to settle out. The integrator is reset before each acquisition window.

f. Combination of Measured Thresholds

The S-band noise estimate and the range-sidelobe estimate are the two measured signals which must be combined to produce the composite threshold for detection of targets. The noise- and sidelobe-estimate inputs to the A/D converters are both log signals. The noise A/D converter is sampled at the end of the noise gate and the noise estimate is stored in a holding register. Consequently, at the beginning of the acquisition window, the holding register contains the S-band noise estimate to be used during the entire acquisition interval. The output of the register goes to an adder where the threshold designate is added to the noise estimate. Another A/D converter samples the range-sidelobe estimate video at a 1.17-MHz rate and places the encoded data in a 6-bit shift register. The sampling rate is sufficient to reproduce the bandwidth of the filtered sidelobe estimate. The value contained is continuously updated and then delayed 26 μsec by the shift register.

The threshold cannot be set at the greater of the noise threshold or sidelobe levels as the false-alarm probability would go to about 50 percent when the sidelobe level exceeded the noise level. Since the noise and sidelobe levels are available as log signals, a nonlinear combination of the threshold and the peak signal levels is required.

The measured noise plus threshold designate and the range-sidelobe samples are combined digitally by selecting the greatest of the two and adding a correction as a function of the difference. A 256-bit ROM generates the required correction factor. It slightly exceeds the desired correction so that the false-alarm rate is always lower than the desired value. The final summation results in a 7-bit word (LSB is 1/2 dB).

g. Computation of A Priori Thresholds

The minimum target cross section of interest is known prior to the acceptance window and is inputted to BATS from the RTI via Designation Word 2. Before it can be used to establish an absolute voltage value for the threshold level in BATS, the cross-section value must be modified by the range to the target and the TRADEX receiver attenuator settings. The TRADEX attenuation value is subtracted from the target cross-section designation to provide a zero range target value. To this is added the STC function to provide a threshold that matches the R^4 reduction in target signal level with range.

The R^4 correction factor is the only time-varying part of the a priori threshold. It is an approximation of 40K log R/R_o, and is generated as shown in Fig. IV-8. The function 40K log R/R_o increases by 12.04 dB every time R/R_o doubles. Therefore, binary-related range increments along the R^4 attenuation curve have a 12.04-dB amplitude differential. The 12.04-dB increments in the logarithmic curve may be approximated from a single set of numbers which are read out at progressively slower binary rates. In the first range segment (16.384 to 32.768 km),

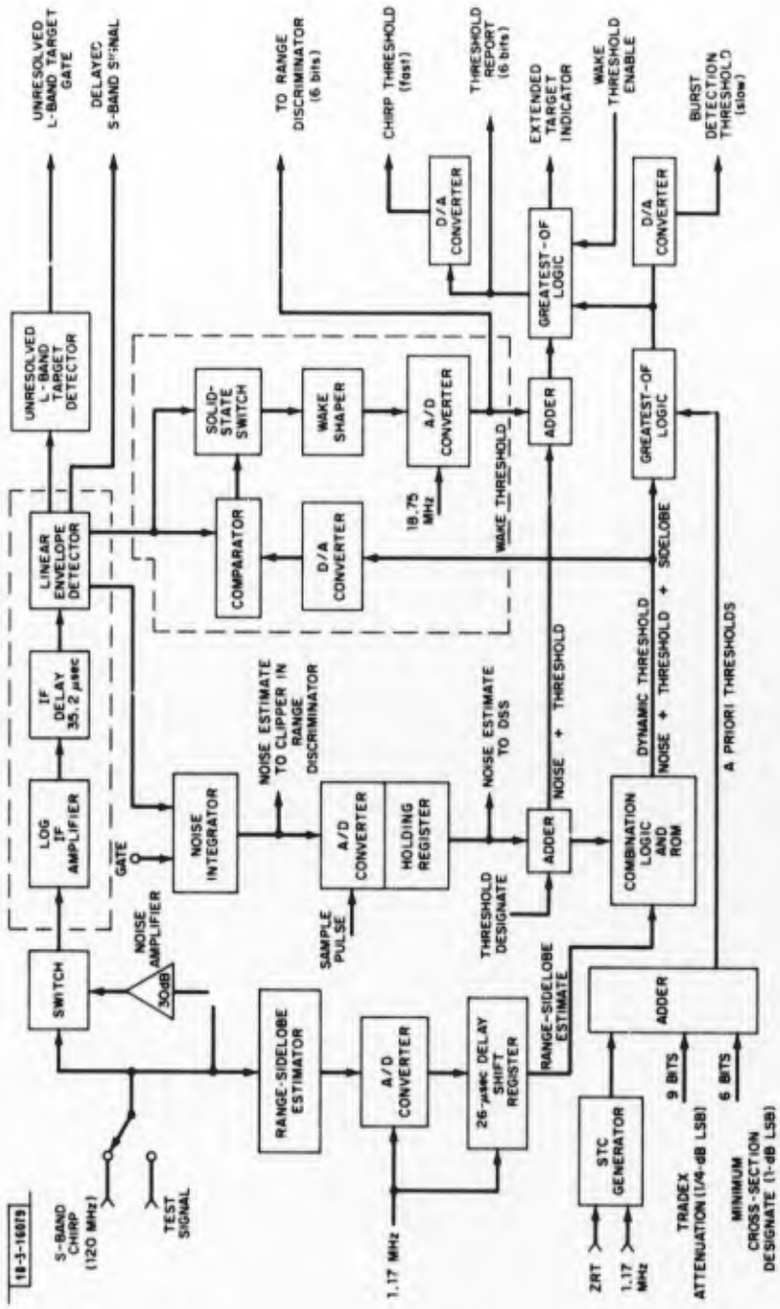


Fig. IV-7. Threshold Subsystem block diagram.

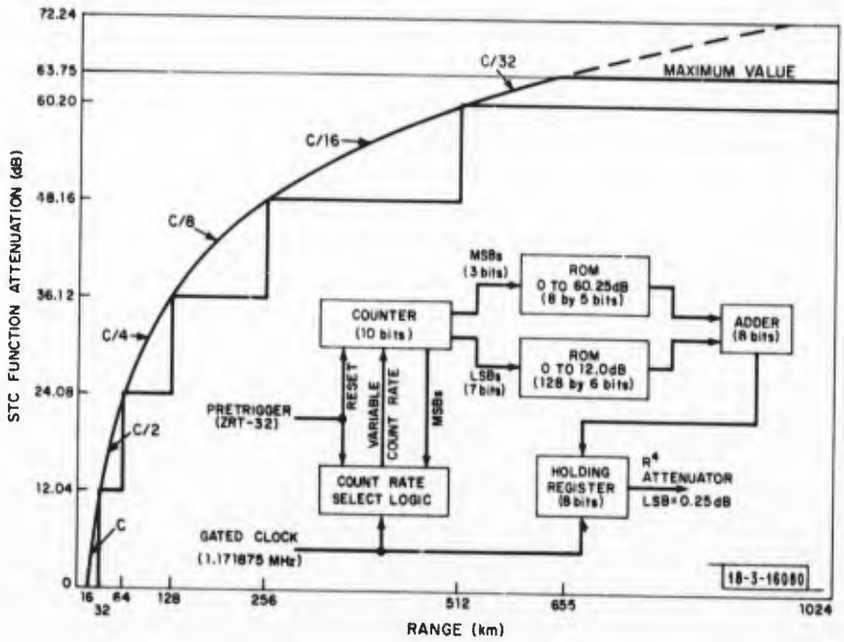


Fig. IV-8. STC generation.

the clock rate is 1.171875 MHz. This provides for 128 amplitude values (in decibels) at a 128-m spacing. The same 128 amplitude values are in the second range segment but are now at a 256-m spacing, produced at a clock frequency of 1.172/2 MHz. This sequence is repeated for a total of six 12.04-dB range segments, giving a maximum possible range coverage from 16 to 1024 km.

The output of the STC holding register is combined with the attenuator and cross-section threshold inputs to produce the range dependent target threshold as shown in Fig. IV-7 as the a priori threshold.

h. Wake Threshold Generation

A dynamic threshold, called the Wake Threshold, is generated and included with the noise and sidelobe threshold to prevent excessive range marks on extended (waking) targets. This is shown in dashed lines in Fig. IV-7. The solid-state switch in the wake threshold section is closed when the S-band log-detected signal exceeds the combined noise plus threshold designate and sidelobe value. If this is the first time the signal has exceeded the noise and sidelobe threshold, the output of the wake shaper will initially be zero. The output of the wake shaper rises until the output exceeds the input. At that time the switch opens, the input signal is disconnected, and the output falls. The rise time of the wake shaper is about 300 nsec and the fall time about 600 nsec. However, both values are adjustable over a 3:1 range. The wake-threshold voltage is A/D converted and added to the Noise + Threshold Designate signal. This is compared with the Noise + Sidelobe + Threshold Designate signal and when the wake threshold is greater than the noise and sidelobe threshold, it is used as the final detection threshold.

Since the rise and fall times of the wake circuit are longer than the rise and fall times of a log-video pulse from a point target, the wake threshold does not reach its maximum value for a point target. This permits detection of closely spaced point targets of equal cross section.

When a waking target is present, the wake-threshold signal tends to reach its maximum value, which is approximately the average value of the log-video. Since the peaks of the wake return are greater than the average of the wake return, the Noise + Threshold Designate value is added to the wake signal to obtain the final wake threshold used.

The wake-threshold voltage that is A/D converted is also sent to a comparator in the Range Discriminator where it is used as one of the decision criteria to select the range discriminator used. The automatic selection is performed by examining the slope of the wake signal following a target detection. For a point target, the wake signal should be decaying and thus a negative slope, while for a waking target the wake signal is still rising (positive slope).

i. Final Threshold Combination

The largest of the three thresholds (a priori threshold, sidelobe and noise threshold, and wake threshold) is selected by the greatest-of logic circuits as shown in Fig. IV-7. Two separate thresholds are formed – one for the chirp waveform and one for the burst waveform. Since the signals coming from the Burst Processor have no wake, the greatest of the a priori or sidelobe thresholds is used. However, the S-band chirp signal does contain target wakes and, therefore, the threshold used for this signal is compared with the wake-threshold estimate and the greatest of these is used for the threshold. The two thresholds are D/A converted and low-pass filtered to provide the analog signals for the actual threshold detectors. A bit set by the designation word is used to enable the final greatest-of selection between the wake and burst thresholds. Unless this input is enabled, the wake-threshold estimate is ignored in generating the chirp threshold.

The criteria for identifying an extended target condition is defined as the case when the wake-threshold estimate exceeds all the other thresholds. The final greatest-of logic circuit also provides a single-bit output which is set for the duration of the wake. This signal is sent to the extended target counter for determination of the approximate range extent of the wake. The final digital 6-bit composite S-band threshold output is sent to the S-band target data buffer where it is stored for sampling by appropriate range strobes. This threshold value is then reported as part of each target data word. A summary of the threshold system equations is shown in Table IV-1.

3. Range and Amplitude Measurement Subsystem

a. Introduction

The range and amplitude measurement portion of the BSP provides single-hit measurements of all targets which meet a predetermined threshold criterion within the computer-designated acquisition gate. The system can perform this target detection and range measurement function on up to 128 targets which may appear within the acquisition gate. The actual range tracking and target bookkeeping is performed within the CDC 6600 computer. In order to perform this function, the system was designed to be capable of handling a wide variety of target conditions from single-point targets to extended and multiple targets over a wide dynamic range.

A tapped delay line type of centroid range discriminator with tunnel diode zero crossing detectors is used in this system. The estimator provides an output pulse coincident in time with the centroid of any video signal which passed through it. This discriminator output pulse is used to generate the required L- and S-band data sample pulses and to obtain a range measurement

TABLE IV-1
SUMMARY OF THRESHOLD EQUATIONS

Burst Threshold (slow threshold)

$$B_T = \text{greatest of } \Big(\{\text{greatest of } [(N + T) \text{ or } RSL] + C\} \text{ or } M - A - S + K\Big)$$

Chirp Threshold (fast threshold for S-band waveform detection)

$$C_T = \text{greatest of } [B_T \text{ or } (W + N + T)]$$

Extended Target = "1" if $(W + N + T) > B_T$

where:

Wake-threshold estimate	= W	0 to 63 dB, LSB = 1 dB
Range-sidelobe estimate	= RSL	0 to 63 dB, LSB = 1 dB
Noise estimate	= N	0 to 31.5 dB, LSB = 1/2 dB
STC (R^4 correction)	= S	0 to 63.75 dB (0 dB at 16 km), LSB = 1/4 dB
Minimum cross section	= M	0 to 63 dB (–50 to +14 dBsm), LSB = 1 dB
Attenuator setting	= A	0 to 72 dB, LSB = 1/4 dB
Threshold designation	= T	0 to 32 dB, LSB = 1 dB
Constant	= K	~50 dB

$$C = 20 \log_{10} \left[\frac{10^{RSL/20} + 10^{(N+T)/20}}{\text{greatest of } (10^{RSL/20} \text{ or } 10^{(N+T)/20})} \right]$$

by strobing a range counter. If target widening occurs due to wakes, causing a mismatch of the video signal to the delay-line length, this condition is noted and a separate, leading-edge type of discriminator is used. The system therefore combines centroid and leading-edge discrimination techniques to provide a range sample pulse which is adaptive to varying target widths across the acquisition window.

Independent ranging and amplitude measurement of either chirp or burst waveforms is provided. Multiple range strobes are not allowed with less than 106-nsec separation. The range strobe determines the target Δ range to 16 bits (LSB = 2 m) with an error of about 4 nsec (rms) including the quantization error of the range counter.

An extended target indication circuit is built into the system and is triggered by the output of the wake-threshold detector. The number of contiguous range cells the signal amplitude stays above the threshold is measured by this extended target counter. The presence of a waking or extended target also enables selection of either range strobe, indication of the strobe selected, and measurement of the extended pulse width. The width measurement is made up to 3200 nsec with 200-nsec granularity. The leading-edge strobe is chosen if the wake threshold, at time T_2, is positive or zero compared with that at time T_1. T_1 and T_2 are set approximately to 100 and 300 nsec, respectively, after the peak of the video pulse. The presence of low Doppler output (wake) from the BMF is also detected and sets a bit.

A range strobe pulse is sent to the burst processor for its sample-and-hold circuit, which subsequently provides the Burst "Video A" signal. Another function of this subsystem is to note the presence of a TRADEX blanking gate transition during the acceptance window and take a

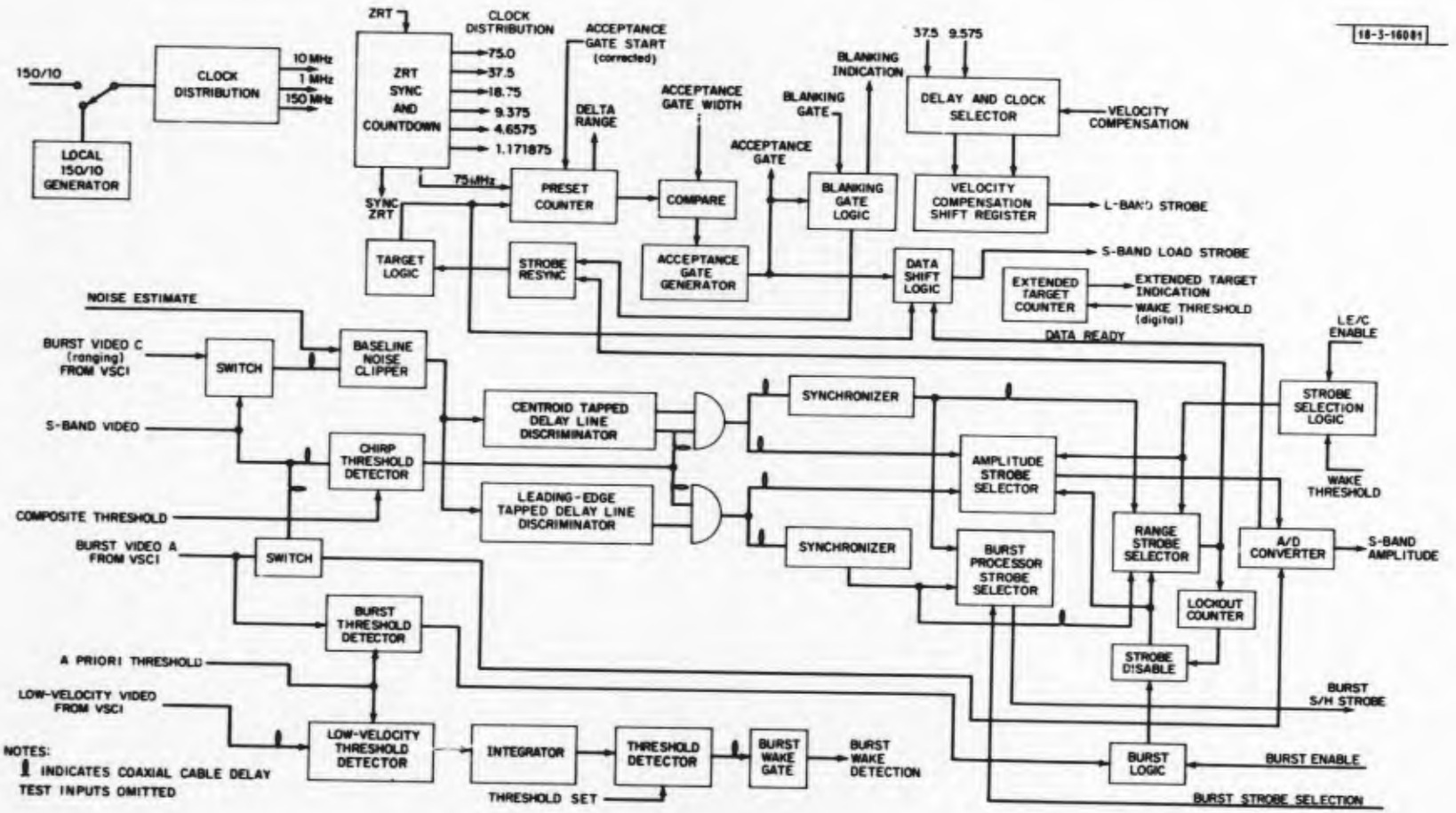


Fig. IV-9. Range discriminator simplified block diagram.

Δ range measurement. This is sent to the buffer memory, indicating the range of the beginning or ending of the radar blanking gate.

A single amplitude measurement is made on all detected targets. The strobe pulse to the A/D converter taking this measurement is obtained from the range discriminators. When the unit is in the centroid tracking mode, the strobe will be at the center of the received pulse; and when there is an extended target, the detector will provide a single reading at the beginning of the extended target. Amplitude is measured with a Computer Labs VHS-630 6-bit A/D converter, strobed within about 2 nsec of the pulse centroid. The strobes for the L-band A/D converters are also generated from the S-band range strobe by insertion of the proper delay. This is determined by 4 bits of velocity compensation data and the appropriate chirp or LIDAR indication.

The subsystem also contains equipment which accepts the TRADEX 150-MHz composite clock signal and from this generates all the required subclocks, test signals, and other timing signals. These timing signals include a resynchronized ZRT and the acceptance window gate. An internally generated composite clock is also provided and can be selected when the external clock signals are not available.

The block diagram for this subsystem is presented in Fig. IV-9. The implementation includes not only the analog discriminator but digital data transfer, control logic, and the high-speed logic assembly which contains the target ranging and clock derivation functions. It is included in this subsystem to minimize the high-speed signal interfaces with the other subsystems.

b. Range Discriminators

The input to the range discriminators, via the noise clipper, may be either chirp or burst video. A remotely operated switch is used to select either the burst or chirp video to be digitized in the A/D converter. These signals are delayed such that their peaks are coincident with the A/D converter strobe pulse.

One of the basic assumptions in the implementation of BATS is that only targets of reasonably large S/N ratio (10 dB or greater) will be considered. Thus, it is possible to clip and remove a portion of the video noise (base line) ahead of the discriminator. For instance, clipping at a 2σ (standard deviation) noise level would remove almost all the noise input to the discriminator while still passing a 10-dB S/N target more than 99 percent of the time. The clipping level is set relative to the rms noise measurement made over the noise gate interval preceding the acquisition gate, and is not modified by the other threshold factors.

Threshold detectors are provided to eliminate return signals (and noise) that have not met the threshold criterion established by the threshold subsystem. The system delays are adjusted to provide properly delayed video such that the target video signal itself is utilized to gate through the appropriate range discriminator crossover pulse when it meets the target detection threshold criterion. The threshold detector has hysteresis built into it so that it will not turn off until the input signal stays below the threshold for a predetermined amount (= 0.1 μsec). Separate threshold detectors are provided for the chirp and burst waveforms. The chirp is set by the composite threshold and the burst by the a priori threshold. The threshold signals are scaled to match the operating characteristics required by the threshold circuits. The output of the threshold detector is a digital type of signal and it is used to gate the tunnel-diode (TD) zero-crossing detectors (ZCDs).

Range accuracy analysis for tapped delay line estimators is available in the literature* where it is shown that range error σ_r normalized to range resolution ΔR can be written as

$$\frac{\sigma_r}{\Delta R} = \frac{\sqrt{1 + 4/N_t^2}}{2\sqrt{2S}}$$

where N_t = number of taps, and S = S/N power ratio.

The above equation is for a matched rectangular video pulse under large S/N ratio conditions and is derived from the slope of the discriminator error characteristic at zero crossover. The maximum loss due to tap quantization is about 3 dB for $N_t = 2$ as compared with large N_t. If N_t is allowed to approach infinity, the range error equation becomes equivalent to the range accuracy equations developed by Manasse.†

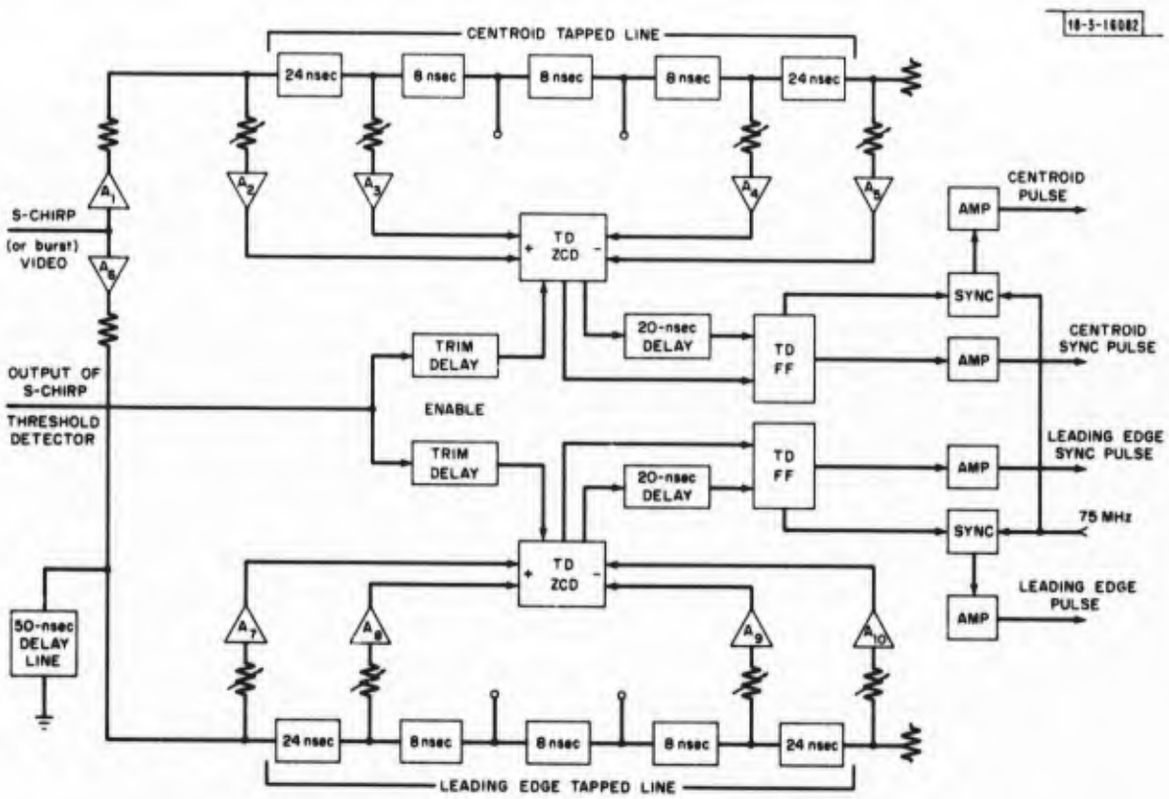


Fig. IV-10. Range discriminator.

A four-tap delay line range discriminator, shown in Fig. IV-10, is used in BATS for generation of peak detection sample pulses. The tapped delay line length approximates the video pulse width. The taps are weighted, and the early and late taps are summed separately and subtracted at the input to the ZCD which produces an output pulse when the early and late tap

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*J. K. Hartt and J. J. Kovaly, "The Attainable Range Accuracy with a Tapped Delay Line Estimator," IEEE Trans. Aerospace Navigational Electron. ANE-11, 92 (1964).

†R. Manasse, "Range and Velocity Accuracy from Radar Measurements," Group Report 312-26, Lincoln Laboratory, M.I.T. (3 February 1955), DDC AD-236236.

voltages are equal. Consequently, the leading edge of the output pulse represents the time occurrence of the center of the input signal.

When the input signal pulse length exceeds the delay line length, the slope of the discriminator response flattens out and the crossover point becomes noisy and indeterminant. (This problem is common to all split-gate trackers.) The means of range marking extended length targets is implemented by a leading edge discriminator. This is accomplished by first generating a synthetic video pulse of proper width coincident with the target leading edge through differentiation of the video, and then range marking the resultant synthetic video with a centroid discriminator. The technique used and shown in Fig. IV-10 approximates the differentiation process through the use of a shorted delay line whose length is equal to half of the desired pulse width. A pulse passed down a shorted delay line is inverted and reflected back to the source so that for a pulse greater in width than the two-way travel time of the shorted delay line, cancellation is experienced. The differentiation method has a loss in S/N because the input noise is folded in twice, causing what is called a "collapsing" loss. For linear video, this collapsing loss is equivalent to almost 3 dB in effective S/N ratio. For the log video used in this case, the problem is more severe since low-level signals and/or noise are emphasized by the log characteristic, thus significantly increasing the collapsing loss over the linear case. The collapsing loss, however, is partly eliminated by clipping and removing much of the noise base line with the noise clipper as discussed previously.

The differentiated output of the shorted delay line is sent to a separate tapped delay line discriminator which generates a zero-crossing detection whose leading edge corresponds to the centroid of the differentiated input. The negative signal that results from the differentiation of the pulse trailing edge is inhibited in the ZCD. The enable inputs provide a high-level output from the threshold detectors and are enabled only for signals that exceed the threshold detection criterion. It is possible for the ZCD to be set by an input noise spike to a mode where it does not recognize a legitimate target zero crossing. A set/reset unit resets the TD at the start of each threshold detection to prevent this from occurring.

Taps have been provided on the discriminator delay lines for future adjustment, and provision has been made for the addition of a 15-nsec shorted line in the leading edge discriminator to accommodate the possible future addition of a wideband waveform. The zero-crossing detection output is synchronized with a 75-MHz clock to maintain the rms delay variation to within 4 nsec. Once the signals are synchronized, there is no cumulative multistage error added to the basic 3.85-nsec rms error of the 75-MHz clock period.

c. Data Transfer and Control Logic

The data transfer and control logic was shown as part of Fig. IV-9. The inputs to this portion of the equipment include both the synchronous and asynchronous range strobes and various logic inputs for determining extended target conditions and range strobe selection. Automatic strobe selection normally takes place but can be overridden by the computer selection of either the centroid or leading edge strobes via the enable lines.

The criteria for the automatic selection of either the centroid or the leading edge range strobe are as follows:

Burst Input to Range Discriminator	The centroid range discriminator is always used since there is no wake present in the burst processor Doppler filtered output.
Chirp Input to Range Discriminator	When the sidelobe or a priori (slow) threshold is largest, the centroid range discriminator is selected because the ranging will be on point targets.
	When the wake (composite) threshold is larger than the a priori (slow) threshold and is also increasing, the leading edge discriminator is used since it indicates an extended target.
	When the wake threshold is larger than the a priori threshold but is decreasing, the centroid discriminator is selected.

There is a circuit to compare the wake threshold at two points in time separated by approximately 200 nsec to see whether it is increasing or decreasing. The comparison is made after the leading edge range discriminator generates a range strobe. If the signal return is from a point target, the wake threshold will be decreasing when the comparison is made. As a result, the output of the comparator will select the range strobe generated by the centroid range discriminator as the one with best accuracy. On the other hand, if the return is from a strongly waking target, the wake threshold will be increasing when the comparison is made. This time the range strobe from the leading edge range discriminator will be chosen as the one with the best accuracy.

There are two range strobe data transfer paths. One handles the synchronous target range strobe, while the other one performs the desired logic functions on the A/D converter strobes. Synchronous range strobes are not used for target amplitude measurement because of the amplitude error introduced by the 13-nsec synchronous strobe ambiguity. The signal amplitude samples are taken as close to the center of the pulse as possible, and this is achieved by using the asynchronous strobe.

The burst inhibit circuits are used to inhibit the transfer of range strobes when the system is in the burst mode of operation unless certain conditions are met. (Inhibits are not used in the S-band chirp operating mode.) The burst range strobe is inhibited unless all the following are true:

TRADEX is in burst mode.
Burst enable is received from RTI.
Burst threshold occurs in BATS.
Burst wake detection signal comes from burst processor.

Strobe selection (leading edge or centroid) is controlled by the Designation Word RDO parameter,* but this parameter has no effect on the burst strobe selection. While the strobe selection is normally done automatically, the RDO parameter permits the computer to override this automatic selection. The BSS parameter* in the Designation Word controls selection of the strobe sent to the burst processor (VSCI). This parameter selects either the centroid or leading edge strobe for the burst processor sample-and-hold (S/H) strobe.

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*See Sec. V for the RTI interface specifications.

The input to the extended target indicator is a pulse signal received from the threshold subsystem. The time extent of this signal is measured by the 4.6875-MHz (32-m) extended target counter. It measures target extent from 0 to 480 m with a 32-m granularity.

d. Operation with Burst Waveform

The A/D converter must have both a video signal and an encode strobe. To obtain burst video rather than chirp video for amplitude data, the BEA parameter* in the Designation Word must be enabled. The burst video source is the burst processor S/H Video A output (or the ATG log video when testing). This S/H Video A is present only if the burst processor S/H strobe is present. The ZCDs are enabled by a chirp video composite threshold crossing. Therefore, strobes can be generated only if a chirp signal is present.

Range and amplitude strobes are generated by the input to the ZCD detectors of either chirp signal or a burst S/H Video A signal. Therefore, strobes can be generated from burst signal provided there is a chirp signal to enable ZCDs and generate thresholds. The BER parameter* in the Designation Word selects either burst or chirp video for strobe generation.

e. Signal Detection and L-Band Strobe Timing

The S-band chirp signal is also used to derive sample strobes for the L-band radar returns and for the burst processor outputs. Figure IV-11 shows the relative time delay between the various signals. The S-band signal must be delayed to establish time coincidence with the S-band threshold. The bulk of the necessary delay is provided by a 35.2-μsec quartz delay line. This part of the system was discussed in the Threshold Subsystem section (Sec. IV-A-2).

The additional delay needed in the threshold path for time alignment between the threshold estimate and the detected video is accomplished with a 26-μsec shift register. Delay trims are built in to allow for final time coincidence adjustments.

The S-band chirp signal arrives at the BATS equipment 35.3 μsec prior to the arrival of the ZRT, as shown in Fig. IV-11. The S-band path delay is composed of 35.2 μsec of quartz delay and approximately 0.880 μsec of circuit delay. Additional strobe delay of 0.842 μsec is required to line up the strobe and LIDAR signal, and 8.132 μsec of strobe delay is needed when the L-band chirp waveform is used. The delay is adjustable to permit compensation of the range/Doppler coupling effect on the L- and S-band chirp waveforms and to accommodate changes in final circuit delays.

The LIDAR strobe delay is implemented with a 72-stage shift register clocked at 37.5 MHz (26.6-nsec increments) providing a total delay of 1.920 μsec. The delay numbers indicate that 32 stages are required for the zero Doppler compensation case with ∓4 counts each side of the 32 needed for maximum velocity compensation. However, an adjustable delay of −36 stages (0.960 μsec) and +28 stages (0.745 μsec) was built to accommodate different circuit delays.

The L-band waveform should be sampled within 1.5 dB of the peak amplitude. Therefore, the sample strobe must be within 26.6 nsec for LIDAR and 0.5 μsec for chirp. The L-band chirp strobe delay could be clocked at a 1.17-MHz rate for ±0.432-μsec spacing with a 1.2-dB maximum sample error. However, the S-band strobes occur at a minimum spacing of 106 nsec and the digital subsystem expects a 1-to-1 correspondence between L- and S-band samples. Consequently, the

*See Sec. V for the RTI interface specifications.

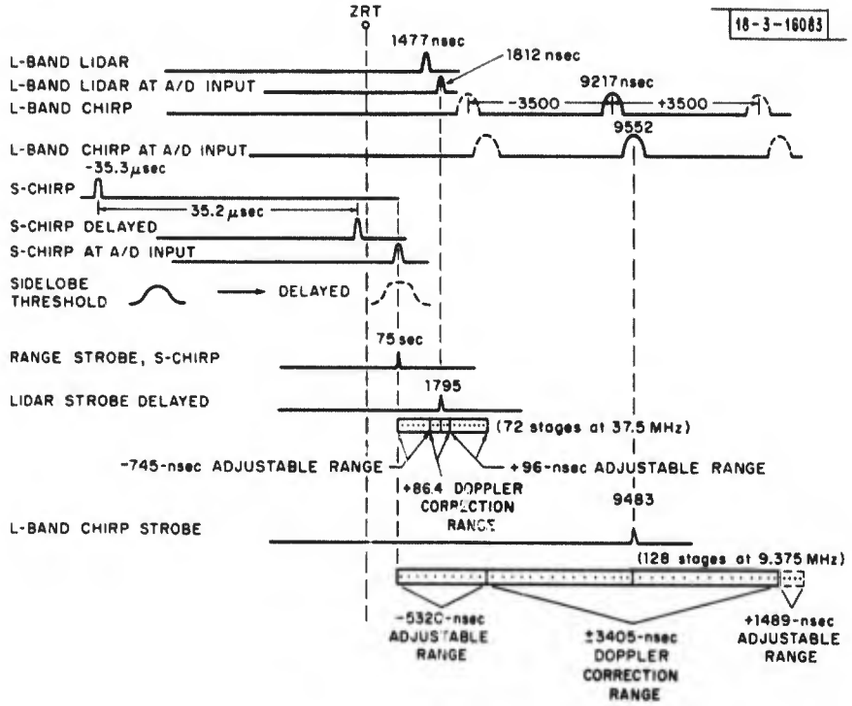


Fig. IV-11. BATS timing diagram.

L-band data strobe is clocked at a 106-nsec rate (9.375 MHz) and is implemented with 128 stages. This provides sufficient delay for range/Doppler compensation and for variation in the circuit delays. The Doppler compensation requires ±3.53 μsec of delay change. This is done with 0.865-μsec granularity by controlling the shift register in groups of 8 stages. This is sufficient resolution to insure sampling the waveform within 1.2 dB of the peak. It is also convenient as only ±4 groups need to be switched, which is accommodated with the same 4-bit code used with the LIDAR waveform.

4. Angle Error Subsystem

a. Introduction

A measurement of the angle error from the antenna boresight is needed to provide a means of telling exactly where a detected target is in the beam. This provides a means of automatic adjacent beam suppression, and a means for the computer to correct measured cross section on offset targets.

A problem peculiar with the TRADEX radar system is that monopulse angle error information is only available at L-band, and not at S-band where targets are detected. There are three major problems associated with taking monopulse data at a different frequency and pulse width:

(1) The L-band beamwidth is larger than S-band. Hence, interfering targets may appear in the angle channels but not in the S-band channel, and may corrupt the angle data.

(2) The L-band compressed pulse length may be an order-of-magnitude greater than the S-band. Hence, two targets close together may be resolved and detected at S-band, but may not be resolved in range for the L-band angle measurements.

(3) Because of the different FM slopes and center frequencies, the range/Doppler coupling is different in S- and L-bands. Hence, the relative delay from one to another will change as a function of target velocity.

The angle data subsystem, shown in the block diagram (Fig. IV-12), takes into account the problems associated with this two-frequency type of measurement. The L-band sum and difference signals* are sent to analog circuitry which computes a voltage proportional to the angle error (Δ/Σ). This voltage is digitized at each target detection and sent to the target buffer. The outputs of the angle channels are thresholded to provide an indication of when the target is within prescribed limits of the S-band beam. The off-axis flag generated by this circuitry is sent to the data buffer for transfer to the RTI. If desired, this flag may be used to inhibit the transfer of data that are outside of preset S-band beam limits.

The strobe for the L-band A/D converters is derived from the S-band target range strobe. This strobe is delayed by a variable delay unit to compensate for the range/Doppler coupling effects of either the L-band chirp or LIDAR waveforms and provide waveform sampling within 1 to 2 dB of the peak of the target return. A circuit is provided for estimating whether or not there are two targets that are resolved in range at S-band but not at L-band.

The noise level at L-band may be different from the S-band level which is being measured. (The TRADEX L- and S-band RF and IF attenuators may not work simultaneously.) A circuit to estimate the noise level of the L-band receiver separately is implemented in the same way as the S-band noise estimator.

b. Monopulse Angle Estimation

The angle error system provides instantaneously normalized, monopulse angle error estimates over a 70-dB dynamic range. Quadratic rejection type of circuitry is incorporated to reject quadrature signal components and to provide a 3-dB enhancement in S/N ratio.

Quadrature components in the monopulse signals are those portions of the monopulse error signal that have a phase angle of either ±90° with respect to the monopulse reference signal. These quadrature components are due to precomparator phase errors and noise.

The precomparator phase error partially determines the depth of null of the monopulse error beam pattern. If the precomparator phase error is Θ, the error to reference ratio, Δ/Σ, at the null is approximately $\Theta/2$ when Θ is in radians. The TRADEX L-band dish has a depth of null from about 15 to 30 dB depending on many factors including the return signal polarization. It is reasonable to expect the precomparator phase errors to be up to around 10°. This precomparator phase error will cause a shift in the position of the null and will result in a quadrature signal.

A plot of the expected Δ/Σ ratio for the TRADEX L-band antenna is shown in Fig. IV-13. If the quadrature components due to the precomparator phase errors are not rejected, the minimum angle estimate will correspond to the error to reference ratio at the null. The minimum

*The TRADEX antenna has a 5-horn monopulse feed system. The reference signal comes from the fifth (center) horn and is not derived in the usual way by summing the 4 horns. However, in this report, the terms reference signal and sum signal (Σ) are used interchangeably.

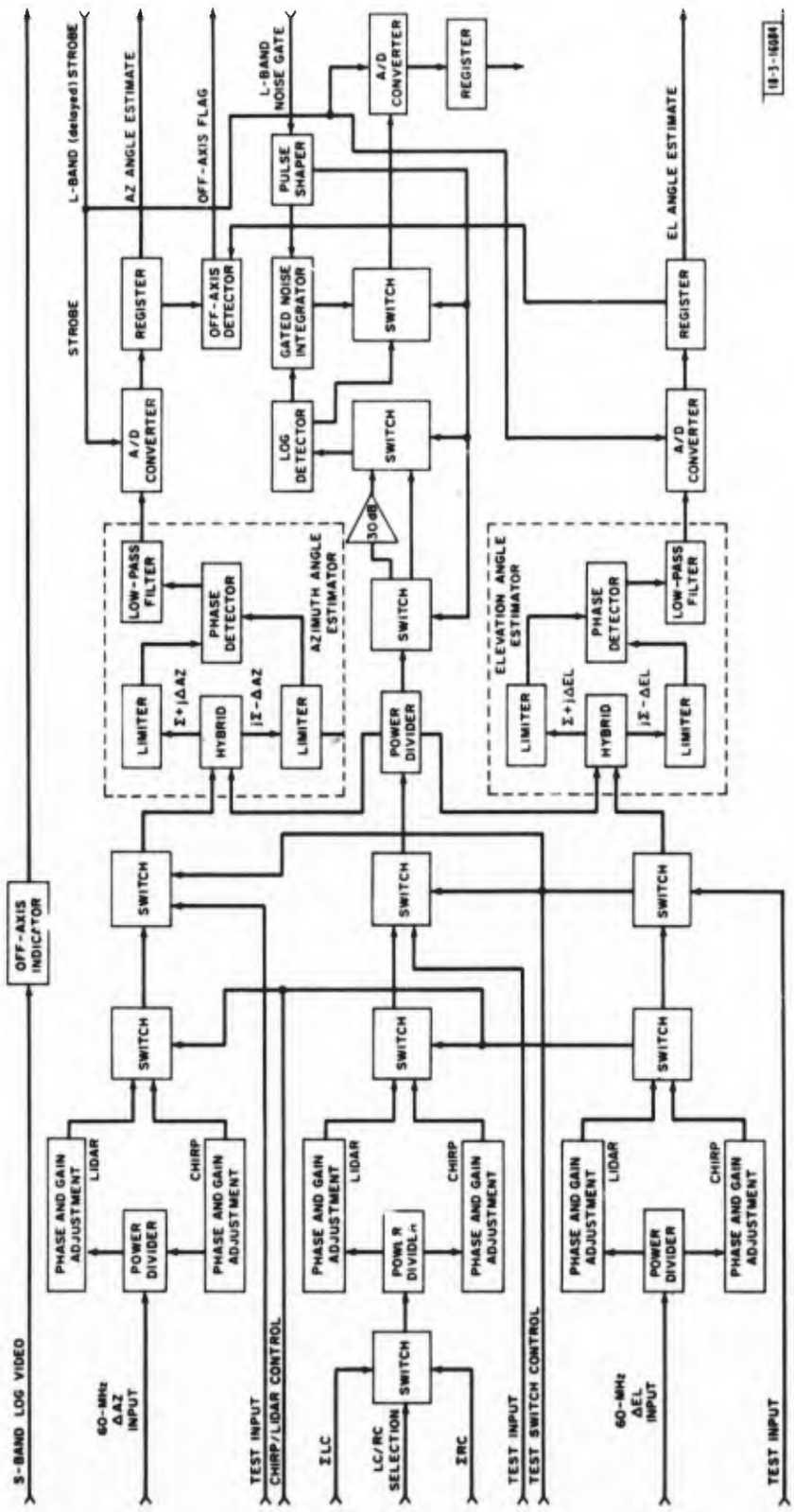


Fig. IV-12. Block diagram of angle error subsystem.

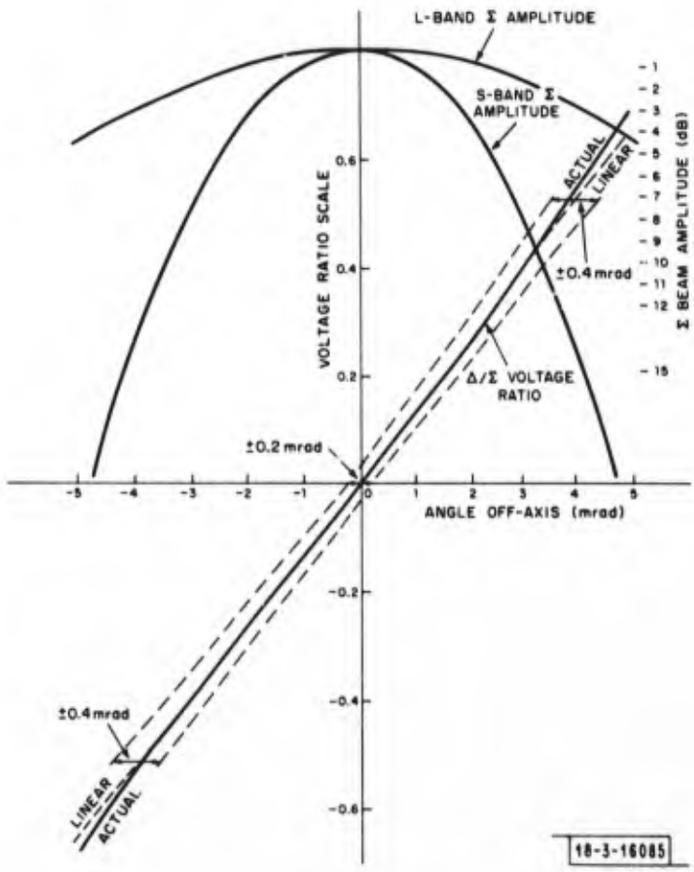


Fig. IV-13. TRADEX antenna beams and monopulse outputs.

angle estimates for various depth of nulls are as follows if quadrature error components are not rejected:

Depth of Null (dB)	Minimum Angle Estimate (mrad)
20	0.80
25	0.44
30	0.25

Also, the angle error due to noise is 3 dB smaller when quadrature components are rejected. For a 30-dB S/N ratio in the reference channel at beam center, it was calculated that the rms noise error in the angle estimate for targets off-axis by 4 mrad would be 0.23 with quadrature rejection and 0.32 with no quadrature rejection. A small improvement is therefore gained in this regard by using a quadrature rejection system. Consequently, in general, the use of a quadrature rejection type of angle error estimator reduces the effects of the shallow null depth and errors due to noise.

The effects of cross-coupling between azimuth and elevation channels in the feed and the effects of target returns having a random polarization limit the angular accuracy. The errors introduced by the angle estimator in the BATS itself are kept small compared with the errors that

are introduced by the RF monopulse comparator and feed. The BATS monopulse estimator does not contribute more than about 0.2-mrad error at boresight, degrading to 0.4 mrad for targets off-boresight.

c. Angle Error Subsystem Implementation

The angle error subsystem implementation is shown in Fig. IV-12. The inputs consist of the LC and RC sum inputs and test signals from the ATG. The appropriate signals are switched by a set of solid-state switches. Phase and amplitude adjustment is provided for both the LIDAR and the chirp waveforms. Adjustment is needed for each waveform to insure proper calibration and operation of the angle estimator system.

The angle estimator system is a type similar to that described in the book "Introduction to Monopulse"* as Type III. It consists of a hybrid, two limiters, and a phase detector. Inputs to the hybrid are the L-band sum and delta signals. The hybrid combines the signals and produces two outputs with the phases shifted as shown in Fig. IV-12. These two signals are then limited to remove amplitude information and compared in a phase detector system. The specifications for this are summarized in Table IV-2. The output signal, after passing through a low-pass filter of about 5 MHz, is then sent to the input of the A/D converter. This signal is proportional to the ratio of the delta to sum signal which is proportional to the angle error. This is a linear relationship for signals near-boresight, but does deviate from the linear relationship off-boresight as was shown in Fig. IV-13.

TABLE IV-2
BATS LIMITER PHASE DETECTOR SPECIFICATIONS

Center frequency	60 MHz
Input amplitude range	0 to −70 dBm
Output	±1 V for ±90°, DC coupled
Linearity	±3 percent over ±60°
Phase tracking	±2° over 70-dB dynamic range for equal amplitude signals
Rise or fall time	Less than 44 nsec (10 to 90 percent) for an input pulse having a 20-nsec rise or fall time
Overshoot or undershoot	Less than 4 percent for 80 nsec, and 1 percent thereafter
Noise figure	Less than 15 dB
DC stability	Less than ±8-mV long term at zero phase over a temperature range of 75 ± 5°F

The strobe signal for the A/D converter is derived from the S-band detection system and is suitably delayed to compensate for differences in range/Doppler coupling from S- to L-band. The output of the A/D converter is held in a register and then transferred to the target buffer memory system.

d. Range/Doppler Coupling Correction

The range/Doppler coupling problem arises from the basic characteristic of the pulse compression filters within the radar receivers. When the average frequency of the received pulse

* D. R. Rhodes, Introduction to Monopulse (McGraw-Hill, New York, 1959), pp. 49-57.

is shifted, due to Doppler effect, the delay characteristic of the filter causes a time position change in the compressed output pulse. This requires compensation between L- and S-band chirp, the L-band LIDAR, and S-band burst returns due to the differing waveforms and delay slopes. Both positive and negative velocities need compensation.

The time shifts for maximum velocities are:

Waveform	Time Shift at 8 km/sec Relative to a Stationary Target (nsec)
L-band LIDAR	7.0
L-band chirp	3530.0
S-band chirp	81.4
S-band burst	18.4

The angle error value, derived from the L-band chirp or LIDAR input, is sampled with a delayed S-band strobe pulse. This sample is taken within 1 or 2 dB of the peak of the L-band return. In order to be no more than 1 dB down, sampling must occur within ±0.4 μsec of the L-band chirp return peak. If a maximum velocity of 8 km/sec is considered, the number of selectable delays required to meet a 1-dB down requirement is ±4 with a 0.8-μsec spacing. The requirement to compensate for either positive or negative Doppler requires that the hardware have the ability either to advance or retard the L-band video sample relative to the S-band return. This is accomplished by the delay in the S-band channel, which is more than the maximum velocity advance shift that will be required in the L-band video sample. The total delay adjustment is more than is needed, which allows fine timing of the system at the site.

The delay of the L-band strobe is designated by the velocity compensation (VC) input from Designation Word 1. The actual spacing is 0.88 μsec for the L-band chirp. This results in an rms error in the sampling time of 0.25 μsec or an rms error off the peak amplitude of about 0.5 dB with a maximum error of 1.3 dB. The delay for the LIDAR waveform provides for similar performance, but the LIDAR delay step is only 26 nsec.

The actual digital hardware to accomplish this delay function is located in the range discriminator cabinet. It consists of a counter which is preset by the velocity compensation valve. The count rate is set at 1.17 MHz for the chirp waveform, and at 37.5 MHz for the LIDAR waveform.

e. Off-Axis Detection Threshold

The angle error subsystem provides for the generation of an off-axis flag for identification of targets that are within the L-band beam but significantly off the axis of the S-band beam. The error to reference (Δ/Σ) ratio for the TRADEX dish at L-band vs off-axis angle was plotted in Fig. IV-13 indicating the expected round-trip amplitudes in one plane for the S-band system. It is desired to accept targets that are within the 12-dB points on the S-band round-trip beam. The maximum off-axis angle is therefore about 4 mils. If the azimuth and elevation errors are individually restricted to these off-axis angle limits, the S-band signal return could be lower when both angles are at their maximum value. To correct for this, a circular angle window is used. It is implemented digitally and allows for a local switch selection of the angle threshold from about 2.7 to 4.5 mrad.

To generate the circular window, the square root of the sum of the squares (RSS) of the azimuth and elevation errors should be less than T, the preset angle threshold. A good digital

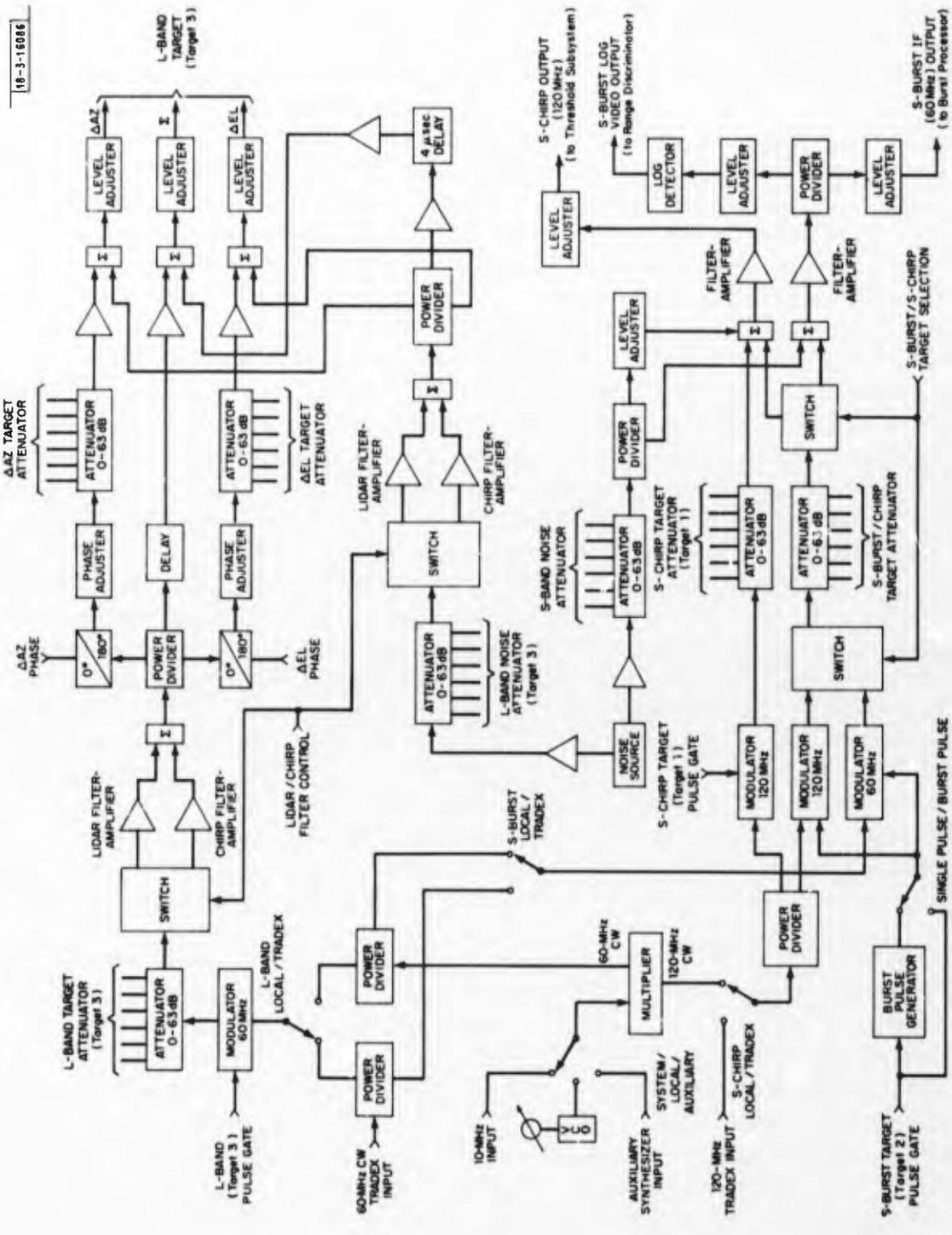


Fig. IV-14. Block diagram of analog portion of ATG.

approximation to the RSS of two signals is the greater of $[|e_1| + 0.5|e_2|]$ or $[0.5|e_1| + |e_2|]$. In the system used, the magnitudes of the two angle errors are determined. The sums of one error magnitude plus half the other are developed, and the greater of these two sums is the desired output. If either sum exceeds T, the output bit for that target is set. This can either set a flag or inhibit the transfer of data to the computer. This selection is made by the computer in Designation Word 2.

f. Unresolved Target Detector

If there are two targets that are resolved in range at S-band but not at L-band (when in the chirp mode), the L-band angle data on each target will probably represent a poor measurement. This condition is measured and reported to the computer along with the other data. It is accomplished by taking the S-band signals and generating a synthetic signal having the resolution of the L-band channel. The amplitude of this synthetic L-band signal is then compared with the original signal. If it is larger than the original signal, it indicates that a second signal is close in range and that the angle estimate may not be valid. This function is implemented by taking the log-detected S-band waveform, delayed by 1.5 μsec, as one input to a comparator. The same waveform is simultaneously converted to a synthetic L-band signal by stretching it with multiple combinations of the outputs of a 2.7-μsec tapped delay line. This signal establishes the threshold for the comparator, and its level is adjustable for any desired threshold value. The output from this comparator is reported as bit 59 of each target word. The equipment to do this is located in the Threshold Subsystem cabinet.

5. Analog Test Generator (ATG)

a. Introduction

The ATG provides the required test and control signals to permit independent operation, test, and calibration of the BSP functions. It generates simulated signals at IF for insertion in the signal detection and measurement circuits. Control of the ATG, along with simulation of the RTI interface, is provided by the Nova 800 minicomputer. A control panel is also provided in the ATG cabinet for local, manual operation of the ATG.

Figure IV-14 is a block diagram of the analog portion of the ATG which is composed of three target- and noise-generation channels. Two target-generation channels provide S-band test signals and one target generator provides L-band test signals. The S-band test signals consist of a 120-MHz S-band chirp signal, a 60-MHz S-band burst signal (16 pulses with adjustable Doppler offset), and a log-detected single-pulse/burst test video. The L-band test output is a single 60-MHz channel split to provide three simulated monopulse signals (sum, ΔAz, and ΔEl).

Independent control of target amplitude, noise amplitude, and target range within the acquisition window is provided for all test target signals. Variable pulse widths in steps of 53.3 nsec from 0.0533 to 5.0 μsec are selectable from the control panel for all three target generators. The ATG uses either an internal 10-MHz crystal oscillator or CW signals from TRADEX to generate the 60- and 120-MHz reference signals. A voltage controlled oscillator (VCO) is also provided to simulate Doppler shift.

b. Analog Section

In the L-band test generator section, the 60-MHz CW reference signal is pulse modulated and the pulse output signal passed through a 0- to 63-dB step attenuator (solid state) to provide

amplitude control of the test target signal. The pulse is amplified and filtered, to simulate a point target return. There are two switch selectable filters – one with a 10-MHz bandwidth for simulating a LIDAR pulse, and one with 1-MHz bandwidth for simulating the L-band (50-1) chirp pulse. The signal is then divided into three channels. The amplitude of the two delta channels is controlled by a 6-bit solid-state step attenuator (0 to 63 dB, 1-dB steps). The phase can be adjusted by a manually controlled phase shifter and a 180° phase reversal can be accomplished by a control signal to simulate positive and negative angle error signals. Noise is summed into each channel before it is finally sent to the BATS signal processor. A small delay line is inserted in the sum channel to match the delays in the delta channel.

The noise generator utilizes a special noise diode as a source of wideband noise. This is stabilized with a feedback loop incorporating a relatively long time constant to maintain a constant average noise level with a stability in the order of ±0.3 dB. The wideband noise is amplified and filtered in individual amplifiers for both the 60- and 120-MHz channels. The noise level in either channel is controlled by a solid-state step attenuator. In the L-band (60-MHz) system, it is passed through either a narrowband or wideband filter to simulate the chirp or LIDAR bandwidths. In the sum channel, the noise is delayed by 4 μsec, decorrelating it from the delta channels to more realistically simulate radar receiver noise.

The S-band test target generator is similar to the L-band generator, as shown in Fig. IV-14, except it is built at 120 MHz. An S-band test burst system provides both a 60-MHz IF output and a log-detected video simulated burst signal of 16 pulses. The pulse train is generated by an Atec 4192 burst pulse generator. A similar pulse generator is used to generate the burst in TRADEX. The IF output is sent to the burst processor to simulate the TRADEX pulse compressed burst IF input at 60 MHz. The video output is used for testing the VSCI equipment which is part of the burst processor. The ATG IF signal source is adjustable in frequency by a VCO over a narrow range to simulate a nonzero Doppler signal. This adjustment enables one to place the test target in any desired Butler matrix output channel.

c. ATG Control Logic

The digital portion of the ATG includes the DSS interface utilizing the Nova 800 minicomputer, the RDSS interface, timing and control synchronizing, holding registers, and timing counters for pulse gate generation. Two timing counters provide programmable strobes and gates to facilitate system calibration and alignment. Operation of these functions is under control of the Digital Subsystem via the minicomputer when in the automatic mode or by the ATG control panel switches when in the local (manual) mode.

The ATG interfaces with the DSS to facilitate BATS calibration and alignment by means of the minicomputer. Signals generated by the DSS interface command the initiating sequence and ATG setup data transfers. Data transfers from the DSS are determined by the minicomputer operating speed. The ATG receives all control data information from the minicomputer through the DSS. The high-speed logic assembly in the RDSS generates the necessary timing signals and control gates for developing the ATG pulse gates and test strobes for system calibration and alignment.

Figure IV-15 is a simplified block diagram of the control logic. Generation of test target pulses is always referenced to the start of the acquisition window. The logic contains 13 holding registers for setup data required by the pulse gate generation logic, attenuators, test strobes,

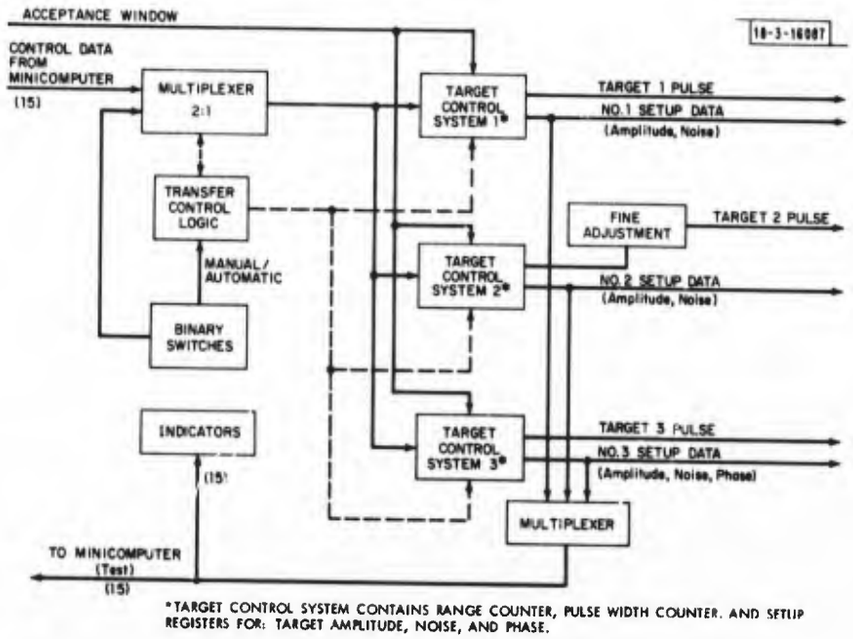


Fig. IV-15. ATG control logic.

and target selection. These registers are loaded from the minicomputer in the automatic mode or by front panel switches in the manual mode. In the automatic mode, a 13-word (16-bit per word) message is transferred via 16 data and 2 control lines to update the computer-controlled setup data. (See Sec. V-D for details of the control words.) Sequential addressing of the holding registers is accomplished using a 4-bit counter which is initialized at the leading edge of the message begin/end signal, and a word count error check is made at the end of each message.

In the manual mode, the holding registers are updated on an individual basis by setting up the register address and desired data on front panel switches and manually entering the data via a push button. Verification of data entered and the ability to read out the contents of the holding registers are provided on 16 indicators on the panel showing the contents of the holding register currently addressed.

Three 14-bit binary counters, clocked at 18.75 MHz and gated with the acquisition window, provide a range count used to determine the range at which each of the test target pulses and strobes will be initiated. There are also three target pulse width counters (7-bit), one each associated with its respective target range counter and also clocked at 18.75 MHz. The binary number is loaded into each of the counters in two's complement and the clock signal started. When each counter has incremented to its maximum value (all ones), it produces a pulse at a time directly related to the number loaded into the counter.

A fine range control is provided on Target 2 to allow its positioning with respect to Target 1 to at least a 10-nsec granularity. This fine range control is obtained by selecting the desired delay from a tapped delay line. Targets 1 and 3 have a range granularity of 53.3 nsec and can be positioned anywhere within the acquisition window. Pulse width is controllable on all three targets in 53.3-nsec steps to a maximum width of 5 μsec. Using the acquisition window gate for target generation control allows generation of test targets in any mode of operation where the acquisition window is produced. Generation of test targets can be locked out by setting the target width counter to zero.

Holding registers are provided for control of the S- and L-band attenuators as designated in the ATG word formats. There are also two timing counters (14-bit binary) clocked at 18.75 MHz whose functions are to provide programmable strobes to the Range Discriminator Subsystem. Generation of these strobes is also under software control.

Associated with each target counter and timing counter is a holding register to preset the desired starting values into their respective counters prior to the occurrence of the selected window start time. When the DSS is in the continuous-run mode and the ATG data interface selected by the DSS, the block of 13 data words generated by the minicomputer supplies the ATG operation parameters. Only the initial data from the minicomputer are required to start the continuous-run mode operation by the ATG, thus releasing the minicomputer for other tasks. The ATG counter functions then continue to operate based on the DSS timing controlled only by the acceptance window time.

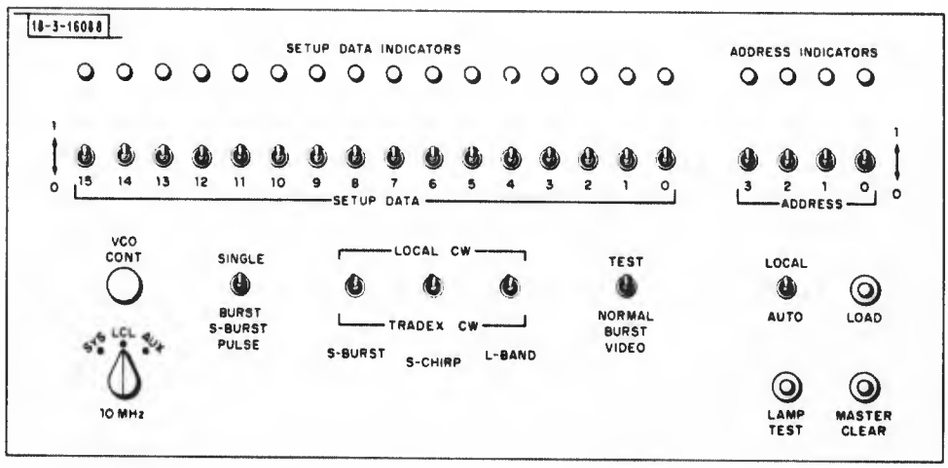


Fig. IV-16. ATG manual control panel.

d. Control and Test Panel

The control panel contains the following controls and indicators as shown in Fig. IV-16:

Master Clear Push Button	Clears the ATG to ready it for operation.
Local/Auto Toggle Switch	Selects the operational mode of the ATG. When in the LOCAL position, the setup data switches on the control panel provide the data as selected. When in the AUTO position, setup data from the DSS are enabled.
Setup Data Toggle Switches	Sixteen toggle switches provide setup data to be loaded into the 13-word registers for ATG operation when in the LOCAL mode. These switches are used in conjunction with the LOAD push button switch.
Address Toggle Switches	Four toggle switches control the address at which the setup data are loaded when in the LOCAL mode.
Load Push Button	Causes the state of the data switches to be loaded into the register word selected by the address switches.
Setup Data Indicators	Sixteen lamps to indicate the state of the setup data held in the register word as selected by the address counter.

Address Indicators	Four lamps to indicate the state of the address counter.
Lamp Test Push Button	Causes all display lamps to light as a maintenance feature.
10-MHz Input Selector	A SP3T switch allowing various local 10-MHz sources to be used to generate the 60- and 120-MHz CW when the TRADEX 60- and 120-MHz CW is unavailable or undesired.
VCO Control	Provides the adjustment for a voltage controlled crystal oscillator. When the 10-MHz input is in the local (LCL) position, the frequency may be varied to simulate the effects of Doppler shift.
S-Burst Pulse Input Selector	A SP2T switch allowing either a single pulse to the S-burst outputs or a burst of 16 pulses every time a Target 2 pulse is received from the ATG logic.
Local/TRADEX CW Input Selectors	Three SP2T switches allowing either 60/120-MHz CW from TRADEX or internally generated signals to be used as the CW reference in generating the S-burst pulses, the S-chirp pulses, or the L-band pulses.
Burst Video Selector	A SP2T switch sending a logic signal to the BATS Range Discriminator Cabinet which switches the Burst Video Source.

6. Minicomputer Subsystem

a. Introduction

A Nova 800 minicomputer and its peripherals are used to control off-line testing for BATS. The minicomputer cabinet interfaces only with the Digital Subsystem. Through that interface, it can check the Digital Subsystem by cycling data patterns through the logic, and control the ATG for checkout and calibration of the BSP. Also, through the Digital Subsystem, the CDC 6600 RTI has two-way communication with the minicomputer.

Alignment and calibration of BATS is accomplished by using the ATG and a series of minicomputer calibration programs. These programs accept data encoded from TRADEX test signals or the ATG and compute the mean and variance of the sample points to produce calibration data. This set of calibration data is stored in the minicomputer and can be transferred to the CDC 6600 via the RTI. Calibration data that exceed specification limits are tagged to notify the operator that corrective action may be necessary. The Digital Subsystem checkout is provided by both the manual control and test panel and by the Digital Subsystem Checkout Software Package to be described in Sec. IV-A-6-c-(2). (The control panel was described in Sec. IV-A-1-o.)

The Nova 800 test programs are used as the primary checkout means. The subtests are performed using software control to generate Command Words, Designation Words, Operational Control Words, and Data Words (patterns and ATG control). The programs perform comparisons on the returned data. Both normal and abnormal transfer conditions are established to check status and priority interrupts. The software causes error messages and applicable actual vs expected printouts for each error that occurs during the tests. If errors do not occur during a particular subtest, then a message is printed that the subtest is complete and the results are satisfactory. Where operator inputs are required for subtest setup and/or performance, the software requests the inputs, waits for operator action, and then proceeds to run the test. Provisions are also made for the software to loop on a subtest and generate the correct clearing functions in the equipment. A single-step mode is also available at the operator's request and will run even with program/hardware interface failures.

b. Minicomputer Hardware

One cabinet (No. 5) houses the Nova 800 minicomputer and its peripherals, and interfaces with the Digital Subsystem. A general-purpose Nova wiring board is used to implement the BATS I/O channel. The board is mounted in the top slot of the Nova 800 and contains a two-channel data I/O, a command output, and a status input.

The component parts of the minicomputer are:

Nova 800	Minicomputer (jumbo chassis)
Nova 4016A	Medium-Speed Card Reader (225 cpm)
Nova 4012A	Paper Tape Punch (63 cps, 8 channel)
Nova 4011A	Paper Tape Reader (300 cps, 8 channel)
TI 730	Teletype (30 cps)

(1) Summary of Nova 800 Minicomputer Specifications

Model	8282
Word length	16 bits
Memory cycle time	0.8 μsec
Memory size	8K
Accumulators	4
Index registers	2 hardware
	16 memory
I/O word length	16 bits
DMA channel	Standard
Maximum word transfer rate (DMA)	1.25 MHz
Priority interrupt levels	16
Response time to interrupt	11.0 μsec
Maximum number of I/O devices addressable	62
Total subassembly slots	17

(2) Selected Options

Part No.	Description
8203	4K core memory (2)
8207	Multiply/divide
8208	Auto-program load
4010	TTY control
4011	PTR control
4012	PTP control
4016	Card reader control
1023	G. P. wiring board subassembly
4007	I/O interface subassembly
4036	Card reader subassembly
4045	Connector (slot 17)

(3) BATS/Nova Input/Output Card

A specially designed interface card provides a separate input and a separate output channel to the BATS Digital Subsystem from the minicomputer. The interface logic is mounted on a standard 15-inch-square wirewrap board (Model 1023), which slides into the Nova 800 chassis and plugs into its backpanel. Each channel contains a separate address and word counter to allow intermixing of input and output data. A 16-bit input register and a 16-bit output register connect to the common 16-bit Nova 800 data bus. The maximum data rate is 1.25×10^6 words per second with the Direct Memory Access (DMA) channel of the Nova 800. Both the input and output data channels interface with separate priority interrupts to the Nova program transfer and DMA channel logic.

The output data channel specifies when a word being sent to BATS is a 16-bit data word or a 16-bit command word. The command word specifies control functions in the BATS equipment. A separate status channel with separate program priority interrupt logic allows the DSS to gain program attention when it has a fault status word ready to be read by the input data channel. The minicomputer first sends a Command word to the DSS to read the Status Word and then follows this by an input data channel transfer sequence. A self-test feature is provided to allow the Nova 800 to self-test the interface card. All signal levels are TTL compatible.

c. Minicomputer Software

(1) BATS Calibration and Alignment Program (BCAP)

The BCAP is designed to calibrate the BATS equipment, to print out the calibration data, and to store these data for transfer to the CDC 6600. It is also possible to perform alignment functions on the BATS equipment using this program. The total requirement for BCAP has been divided into a control subprogram and eight processing subprograms, namely:

(a) S-Band and L-Band Noise Estimate Subprogram
(b) S-Band Sidelobe Estimate Subprogram
(c) S-Band Chirp Amplitude Calibration Subprogram
(d) S-Band Burst Amplitude Calibration Subprogram
(e) S-Band Chirp Range Estimate Calibration Subprogram
(f) S-Band Burst Range Estimate Calibration Subprogram
(g) L-Band Signal Amplitude Calibration Subprogram
(h) L-Band Angle Error Estimate Calibration Subprogram.

The object program is organized in such a way that the basic program and the control subprogram are loaded initially. Prior to loading the first processing subprogram, a message is printed giving the operator all information and/or instructions necessary to run calibration and/or alignment. The first processing subprogram is then loaded and executed. After this subprogram has finished, the next processing subprogram is loaded and executed. This process continues until all the processing subprograms have been executed. The control subprogram then loads the dump to CDC 6600 subroutine which checks to see if the last processing subprogram was run in the calibration or alignment mode. If the subprogram was in the calibration mode, this subroutine sets up the calibration file for transfer to the CDC 6600 and initiates an output command; if in the alignment mode, this subroutine exits back to the control subprogram.

Each processing subprogram consists of three subroutines:

STRIP	Extracts information from the BATS reply word block and stores it in a temporary buffer. Only information needed for the particular test is retained.
COMPUTE AND STORE	Computes mean and variance on the data stored in the temporary buffer; checks data for within-limits condition, prints the data, and stores the mean, variance, and the out-of-limits flag in the calibration file. Each value printed on the TTY is followed by a * if it is out of limits.
CYCLE AND WRAP UP	This subroutine checks to see if this test is complete. It sets a flag word indicating if the test should be cycled again or stopped. If the test is not complete, it alters the parameters for the next pass.

In addition to the three subroutines, data parameters and a parameter table are loaded with each subprogram. The parameter table is used to store the needed pointers, current value, and limits (or range of possible values if a bit pattern is to be inputted) of the parameters the operator is allowed to alter.

Control Subprogram:– This subprogram contains all program parameters and storage areas common to the processing subprograms prior to loading each subprogram. It loads each processing subprogram, and asks the operator if he wishes to run in the calibration or alignment mode or to skip this test. If the operator wishes to skip this test, the next subprogram is loaded; if he wishes to run in the alignment mode, the program will type out each parameter, defined by this subprogram as being under operator control, and give the operator an opportunity to select its value. This sequence continues for all such parameters. After all parameters are entered, the program starts collecting data, computing mean and variance, and typing these values on the TTY by controlling the execution of the strip, the compute and store, and the cycle and wrap up routines of the current subprogram. This sequence will continue until the operator directs the program to stop, at which time he is given the choice to input new values for the operator-controlled variables or to continue to the next processing subprogram. If the operator wishes to run in the calibration mode, the predetermined test sequence is executed. The control subprogram directs the execution of the routines of the current subprogram.

(a) S-Band and L-Band Noise Estimate Subprogram:– This test sequence measures the performance of the noise estimator circuitry in the Threshold Subsystem. When used for calibration, a 60-MHz noise signal from the ATG is sent to the L-Band channel, a 120-MHz noise signal is inserted into the S-Band chirp input, and the BATS output (L-Band noise and S-Band noise) is measured. 128 samples are taken and the mean and variance (m, σ^2) are calculated for both the L-band and S-band noise. If these values are out of limits, they are flagged. The values (m, σ^2) are stored in the calibration file and each of the values is printed out with an out of limits flag if appropriate. This procedure is repeated for six different noise levels. When in the alignment mode the operator can select any noise level.

(b) S-Band Sidelobe Estimate Subprogram:– This test measures the amplitude of the time sidelobe estimate generated in the Threshold Subsystem. The ATG pulse train enable is set to output 17 test strobes at a 0.85-μsec (1.17-MHz clock) spacing. The strobes are positioned so that the ninth strobe is centered on the target return. This produces 8 strobes

symmetrically spaced on each side of the test target. These test strobes appear to the range discriminator as target strobes and strobe the threshold estimate A/D converter, producing a set of samples of the sidelobe estimate value. These values appear in the BATS output data word as the S-band threshold level.

A total of 128 samples are taken for each of the 17 estimates, and the mean and variance are computed. Each value is checked for out-of-limits condition and, if out of limits, it is flagged. These values are available for output to the TTY and storage in the calibration file. When this subprogram is used for alignment, the operator has the option of selecting certain parameters and cycling continuously through the test. The mean and variance then are not saved in the calibration file.

(c) S-Band Chirp Amplitude Calibration Subprogram:– This test is run by inputting a calibrated test signal from the ATG to the BSP and evaluating the amplitude measurement output. The ATG is nominally set up to generate a 100-nsec S-band chirp target. This test pulse is initially set to full scale (63 dB) and 128 samples are taken for the mean and variance computation. The ATG target attenuator is then decremented by 1 dB and another 128 samples are collected. This sequence is repeated over the full range of signal-level control. The results present the calibration and deviation from linearity of the S-band target amplitude system.

When this subprogram is used for alignment, the operator has the option of selecting the parameters and collecting data for selected ATG target attenuator levels.

(d) S-Band Burst Amplitude Calibration Subprogram:– This sequence is run by sending a calibrated test signal to the BSP burst input and evaluating the digitized amplitude measurement output. It can be accomplished using either a single pulse or a burst of pulses. The ATG is set up to generate a single 100-nsec log video pulse. The range discriminator is set to use the burst video for A/D conversion (BEA = 1). The target is initially set to full scale (63 dB) and 128 samples are taken for mean and variance computation. The ATG target attenuator is then decremented by 1 dB and another 128 samples are taken. This sequence is repeated over the full range of signal-level control.

In a burst test, the ATG is set up to generate a Doppler offset burst IF output using the burst pulse generator. The ATG is also set up to generate a 100-nsec chirp IF output to enable strobe generation in the range discriminator. The proper time delay must be used between the burst and chirp ATG outputs to provide time coincidence between the A/D analog input and A/D encode strobe. The data-gathering cycle is the same as described for the single pulse. When this subprogram is used for alignment, the operator has the option of selecting the parameters.

(e) S-Band Chirp Range Estimate Calibration Subprogram:– This test calibrates the S-band chirp target ranging subsystem. It is implemented by the ATG sending the BSP a simulated S-band chirp target (pulse width of 100 nsec and amplitude from 0 to 63 dB). The mean output of the BATS target ranging counter is then compared with the known input target range for each signal level. In the calibration mode, the test is run as described by taking 128 range samples at each of 64 attenuation values. The output represents the accuracy of range measurement over all possible values of target amplitude.

Mean and variance are computed in meters and each value is checked for out-of-limits condition. These values are available for output to the TTY and storage in the calibration file. When this subprogram is used for alignment, the operator has the option of selecting certain parameters and cycling the test indefinitely.

(f) S-Band Burst Range Estimate Calibration Subprogram:– This test is designed to calibrate the S-band burst target ranging function. It is implemented by sending a simulated S-band burst target with known parameters to the BSP and comparing the mean output of the BATS target ranging counter with the known input target range. It can be done either with a single video pulse or a burst of pulses.

The ATG IF signal source is set to come from the VCO which is adjusted so that the resulting 60-MHz ATG output has sufficient Doppler frequency offset and the signal appears in one of the burst processor Doppler filters within the Doppler designation band. The ATG is set up also to generate a 100-nsec S-band chirp IF output to enable strobe generation in the range discriminator at the proper time (range).

The cycle is similar to that described before, and 128 samples are collected at each attenuator setting for mean and variance calculations. This program can also be cycled for alignment purposes.

(g) L-Band Signal Amplitude Calibration Subprogram:– This test is run by sending a calibrated 60-MHz signal from the ATG to the L-band Angle Error Subsystem. Two test modes are available. One uses an L-band test strobe generated by the ATG, and the other derives the L-band strobe in the normal fashion from the S-band chirp signal. The test procedure is the same as for the S-band amplitude calibration.

(h) L-Band Angle Error Estimate Calibration Subprogram:– This sequence measures the performance of the L-band angle error estimation circuitry. It is run by sending calibrated sum, delta azimuth, and delta elevation signals into the respective L-band channels and evaluating the resulting delta/sum output ratios. In the calibration mode, 7 sum values are used and for each sum value 21 delta values are used. Data are collected for both the chirp and LIDAR modes resulting in a total of 294 data points each for the elevation and azimuth angle error calibrations.

At each of the 588 Δ/Σ data points, 128 samples are taken for computing mean and variance which are stored in the calibration file and printed out on the TTY. This program can also be run continuously for alignment purposes.

(2) Digital Subsystem Checkout Programs (DSCP)

The total digital checkout software requirement has been implemented using eight programs which are described below.

(a) Register Test – DSCP 1

DSCP 1 performs tests on the computer I/O board, runs the DSS I/O loop test, and checks all the DSS registers. Ten separate tests are implemented, and in each test the input and output words are compared to insure they match. If a match does not occur, an error message is printed. Each test can cycle through using any defined bit pattern.

Computer I/O Board Test	Transfers 524 15-bit (131 60-bit) data words through the I/O board back into the computer.
DSS I/O Loop Test	Transfers four 15-bit (one 60-bit) data words through the DSS.
Operational Control Word Register Test	A word (one 60-bit/four 15-bit) is sent to the operational control word register, read by the minicomputer, and compared.

Register C1 Test	Performs a check on register C1 using four 15-bit (one 60-bit) words.
Register C2 Test	Four 15-bit (one 60-bit) words are sent to register C2.
Register HC3 Test	Performs a check on register HC3 using four 15-bit (one 60-bit) words.
Register H1 Test	Four 15-bit (one 60-bit) words are sent to register H1.
Register H2 Test	Four 15-bit (one 60-bit) words are sent to register H2.
Register Status Test	Four 15-bit (one 60-bit) words are sent to the status register.
Sequence Registers Test	This test performs a check on registers C1, C2, HC3, H1, and H2 in sequence. Twenty 15-bit (five 60-bit) words are used and stored in the registers in sequence.

(b) Status Test – DSCP 2

Tests the capability of the status logic in the DSS to generate priority interrupts once an interrupt bit is set in the status register.

(c) Memory Test – DSCP 3

Tests the operation of the 128-word, 60-bit target buffer.

(d) Timing Test – DSCP 4

Performs tests to verify the operation of the BATS timing control.

(e) Output Control Test – DSCP 5

This program accepts an input from the operator, via the TTY, and outputs signals to the DSS allowing them to be checked with an oscilloscope.

(f) Priority Interrupt Test – DSCP 6

Checks the ability of the DSS to cause a priority interrupt and set the proper status bit.

(g) ATG Test – DSCP 7

Sends data to the ATG through the DSS to verify the operation of the interface.

(h) Minicomputer/RTI Test – DSCP 8

This test consists of two programs, one in the minicomputer and one in the CDC 6600. These two programs are used to verify the interface between the minicomputer and the CDC 6600 via the DSS.

(3) Special Tests

I/O Board Interrupt Test (IBIT):– This program checks the capability of the computer I/O board to initiate a priority interrupt on the "data output," "data input," and "status" channels when in the local test mode.

General-Purpose Calibration Alignment Program (GCAP):– This is a basic calibration alignment program allowing the operator to define any or all of the Designation Word

parameters, ATG parameters, and the TZRT parameter of the OCW. On command, GCAP executes the output sequence and puts the equipment in a continuous-run mode.

Burst Wake Detection Test (BWDT):- This test checks the burst wake detection circuitry in the range discriminator. It is implemented by sending to the BSP an extended pulse, log detected, ATG output. The signal is varied in width and amplitude and the burst wake detection bit (WI) is checked, indicating a wake detection has occurred.

Slow Threshold Test (STT):- This test measures the performance of the a priori threshold circuitry. No noise is added in, assuring that the S-band detection threshold is only a function of the cross-section designation, STC function, and TRADEX attenuator setting. The ATG is set to generate 128 load strobes at a 1.17-MHz rate within the 16- to 32-km range segment. This is the first range segment over which the STC function is operable. For each load strobe, a threshold estimate is taken and 128 values outputted by the TTY. The TRADEX attenuation value and the STC have 0.25-dB LSB, but the threshold estimate is only 1-dB LSB. Therefore, many sample steps will be taken before the threshold output value changes. The transition point is changed by incrementing the TRADEX attenuation value in 0.25-dB steps.

Off-Axis Flag Test (OAFT):- The OAFT program outputs a series of ATG and Designation Words, each time examining the returned value in the OAI field of the Target Word. OAFT outputs the ATG and Designation Words for all the specified values of DEA (Delta Elevation Attenuator) and DAA (Delta Azimuth Attenuator). The program then will print a graph, marking an "x" at each point where the received OAI bit is 1. This graph shows in two dimensions where the off-axis flag limit value is set.

Two-Target Range Discriminator and Unresolved Target Test (TTRU):- This test checks the effect of target spacing and amplitude on the following functions:

Unresolved target flag
Target extent
Wake indication
Leading edge/centroid control
Target count
106-nsec lockout
Range discriminator computer overrides

Single-Target Range Discriminator and Unresolved Target Test (STRU):- This program checks the following functions:

Unresolved target flag (URT)
Target extent (E)
Leading edge/centroid control (LEC)

This is done with the ATG by outputting different combinations of the Target Attenuator (SCTA), and Target Width (SCTW) and examining the proper bits of the target word.

B. PHOTORECORDING SYSTEM

1. Introduction

The D&DE photorecording system is a radar A-scope type of photorecording system. It is designed to satisfy the A-scope photorecording needs of both the SSP and the BATS. It is capable

of tying-in with the TADCO photorecording system already existing at the site, but this has not been implemented at the present time. The system is designed to be general enough in concept and implementation to accommodate changes in the D&DE photorecording needs as they arise.

2. Main Features of the Photorecording System

The main features of the photorecording system are summarized below. A simplified block diagram is shown in Fig. IV-17.

Input Video Switching System – able to interconnect output signals from the various processors to any photorecording input. The system is capable of both local and remote control.

Camera System – consisting of a 16-mm framing camera able to be synchronized to an external signal at a rate up to 40 frames per second.

Oscilloscope System – consisting of two dual-beam scopes optically multiplexed to provide four simultaneous beams to be recorded. Sweep speed is under system control.

Numerical Display – able to write characters (TOD, Mode, Altitude) on the film. This is accomplished by an LED type of numerical display for TOD, and a character generator for the additional information.

Delay and Sweep Speed Control Units – able to accept input triggers and generate or control the various sweep speeds and start-of-sweep times.

Signal Control Units – whose function is to control the trace brightness and the baseline position.

Control System – able to accept input commands from a Nova minicomputer and set up the operating functions. Photo-system integration and timing are controlled from this subsystem.

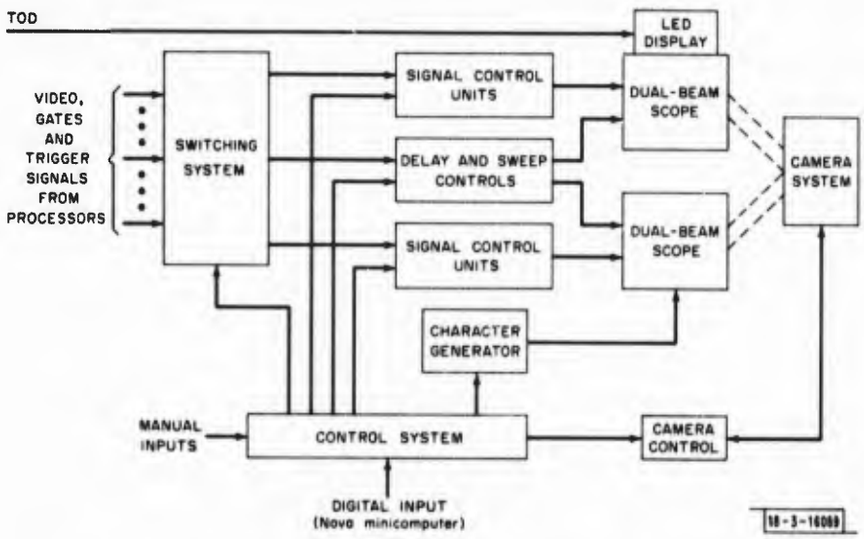


Fig. IV-17. Simplified block diagram of photorecording system.

3. Use of Equipment

Three basic features of the system that are considered essential for D&DE needs and have not been incorporated in previous KREMS photorecording systems are:

(a) Multiple independent traces (4) on one frame.
(b) Ability to change recording formats during a mission.
(c) Single-sweep synchronized operation.

The purpose of the multiple-trace feature is to be able to compare the various output events with the input signals. In this way, the BATS or the SSP can be checked for proper operation. In order to gather and process the radar data to hand over to the CDC 6600, there are many internal circuits or functions in BATS or SSP that make decisions based on measurements (or a priori knowledge) and adjust the processor controls accordingly (e.g., Threshold Subsystem, L- to S-band Doppler delay adjustment, etc.). There is no way of knowing how these internal functions are operating without looking at their output with a definite time correlation (same PRI) on one piece of film. Some of this information is not sent to the computer and recorded, so it would be lost if not recorded on film. Hence, one purpose of photorecording is as a diagnostic tool for the processors. It will also serve as a post-mission editing aid to help interpret the BATS and SSP digital outputs.

BATS and SSP will have various functions during a mission. The BATS functions will be:

(a) Acquisition (range gate opened wide)
(b) Tracking (range gate narrowed on one or more targets)
(c) Noncoherent bulk filtering (wide range gate)
(d) Coherent bulk filtering (wide range gate, additional velocity outputs to be recorded)
(e) Hybrid bulk filtering (simultaneous noncoherent and coherent filtering).

The SSP has a similar set of operations, including search and track. One recording format for the entire BATS mission and one for SSP would not suffice. To be useful, different information is needed for each mode of operation. These modes, of course, would be modified between missions depending on experience factors and mission objectives. Also, because the scopes have a limited number of resolvable elements (250 in this case), sweep speeds and the other parameters must be chosen with care to get useful information on film. Hence, the need for the control of recording parameters.

a. Use with BATS

Since the BATS is primarily a technique development rather than a measurement tool, the philosophy is to record data, not for the reconstruction of the environment, but for the assessment of the performance of the system, the determination of failure mechanisms, and a data-editing aid. Film recording is able to provide an estimate of system performance that is not available from the digital tape.

One suggested display for BATS recording is shown in Fig. IV-18(a-b) which shows a suggested format for both a coherent and a noncoherent mode of operation. Also shown are typical characters that might be photographed with the oscillographic display, to provide the associated PRI data. The most important signals to be recorded on film include chirp log video, threshold, S-band burst video, and angle error signals. Other data, such as Doppler channel reports which identify the source of the burst video, also could be recorded.

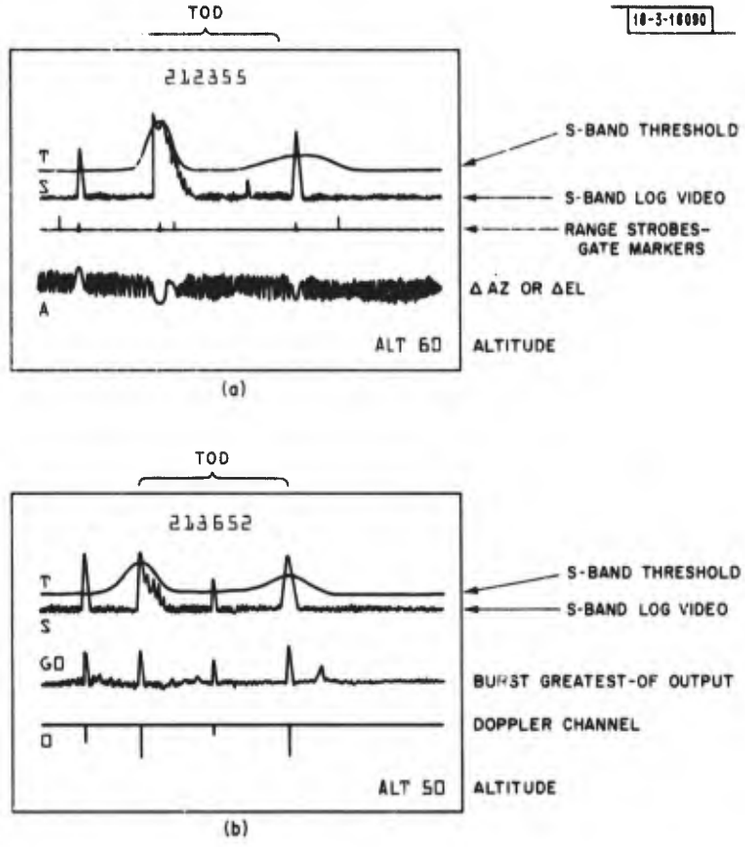


Fig. IV-18. Examples of BATS recording configurations: (a) noncoherent processing (chirp mode), and (b) coherent processing (burst mode).

b. Use with SIMPAR

The SIMPAR program will make use of the photorecording system during performance evaluation exercises of the SSP as well as during missions. During the evaluation exercises, the signals to the SSP may be derived from an analog target simulator or the ALTAIR radar. Possible signal configurations to be photographed are similar in some ways to BATS and are shown in Fig. IV-19(a-b). The signals of interest would be the outputs of the monopulse angle error detectors, log detector, threshold signals, A/D sample patterns, and event strobes. The numerical display would also be used for mode identification and periodic TOD notation.

4. System Description

A detailed block diagram (Fig. IV-20) should be used as a general reference for this entire section.

a. Oscilloscope System

The photorecording system design is based on the use of two Tektronix 556 Dual-Beam Oscilloscopes with 1A2 dual-channel amplifiers and P11 phosphors. The scopes have been modified to enable remote selection of sweep speed and a means of summing signals in the X, Y, and Z axes.

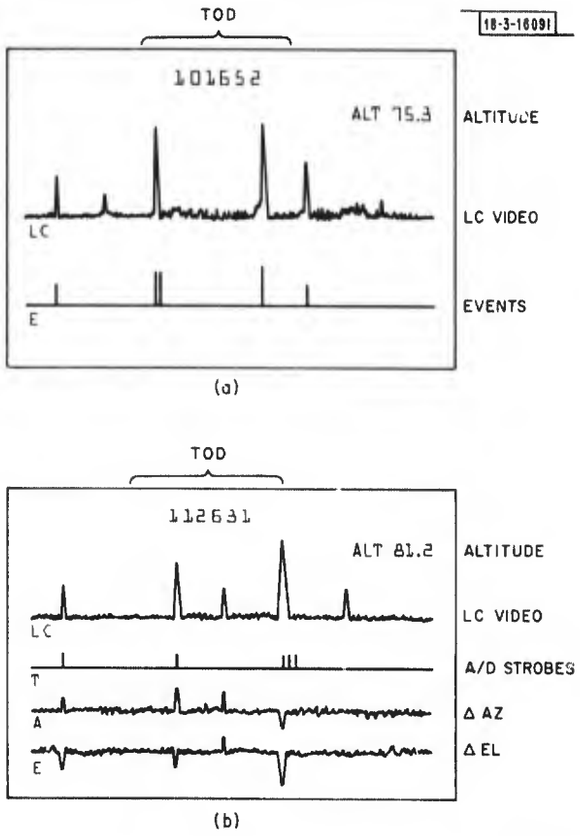


Fig. IV-19. Examples of SSP recording configurations: (a) search mode, and (b) track mode.

The dual-beam feature is essential since the information to be recorded is all present at the same time, and hence as much as possible must be recorded simultaneously.

The faces of the dual-beam oscilloscopes are combined by use of mirrors to form a single display. While this places a considerable amount of information on a single frame, it is anticipated that one would examine only occasional selected frames in detail to determine significant events in a mission. A cine playback of the film is important, but probably would only be done to get a quick-look summary of a mission or to data of interest.

Means are provided to drive at least one remote (up to 50-foot) display from both scopes. This includes take-off points for the X, Y, and Z inputs of each oscilloscope. Hence, an additional display can be added at a later date.

b. Camera System

The 16-mm framing camera chosen for the system is capable of being synchronized to an external trigger. While the radars operate with prf's up to about 3000, BATS and SSPs will have effective prf's of only up to about 40. It is desired to have the capability to record only a single PRI on each frame to avoid ambiguous data.

Since it is anticipated to use the system for both SIMPAR and BATS, a recording time of up to 30 minutes is desirable to allow for some safety and for additional calibration information. Hence, 1000 feet of film capacity is needed for an average frame rate of 25 fps. A Wollensak

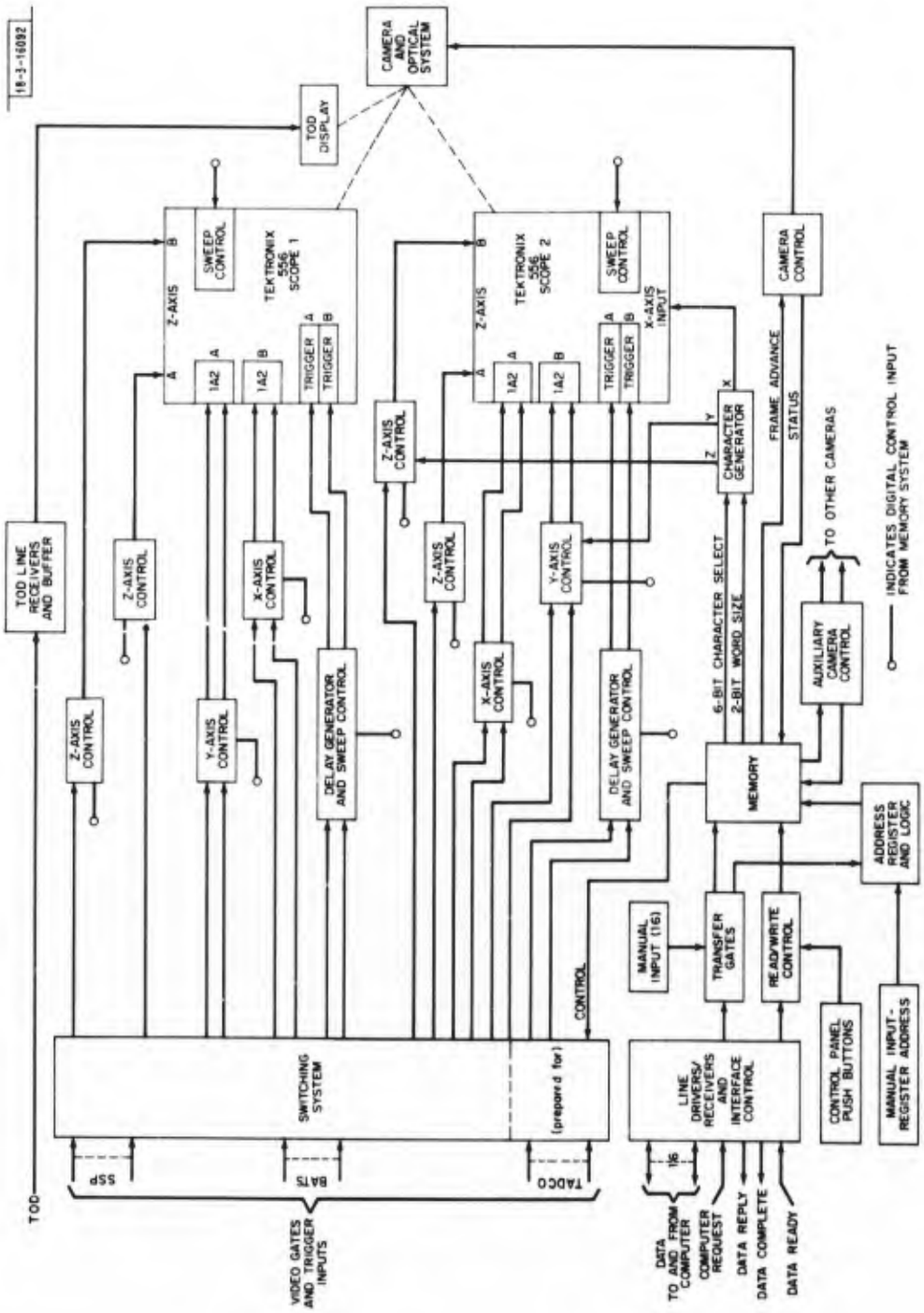


Fig. IV-20. Block diagram of D&DE photorecording system.

Model 306-3 Computer Output Microfilm (COM) camera is used in the system; this camera utilizes a DC motor and digital encoder system to drive a capstan, and film tension sensing servos to control the supply and takeup systems. With the equalized film tension system, the film position in the gate follows the adjacent capstan very precisely. As a result, excellent frame-to-frame registration accuracies are achieved without sprockets or registration pins. However, since accumulative errors would gradually show, an optical perforation sensor is utilized to provide final positional information. The perforation sensor is located in the aperture and consists of an IR source and sensor bank that averages, differentially, the position of the two perforation edges and provides control information to position the film in a similar manner to register pins. The source has a 9000-Å emission frequency permitting utilization of both standard and extended red films.

The camera accepts a trigger for pull down and returns a camera-ready pulse which is compatible with TTL or DTL logic. There is no shutter in the camera, and one must rely on the scope face being dark before advancing the film.

c. Input Switching System

The switching system is made up of coaxial relays which will connect the outputs from the various processors to the oscilloscope inputs. This system can be under the control of either a manual input system located in the photorecording system or by connection to a minicomputer. Choice of either control is switch selectable. Designated words are stored in registers to set up the switching system. Provision is made for limiting the switch duty cycle, since a possible digital circuit malfunction could cause premature failure of the switching matrix by issuing switch commands at an excessive rate.

d. System Control

It is desired to be able to control the various devices and set up the inputs to the photorecording system in an optimum configuration by means of remote and local controls. This gives the option of changing inputs and some formats during a mission, depending on what was being tracked and what data were being collected.

Six different configurations, designated as Modes A to F, can be preset into the device. Local or remote control will select the one to be used depending on the mission events. Some different configurations needed might be envisioned as follows:

SSPS – search
SSPS – track (and search)
BATS – acquisition or noncoherent
BATS – track
BATS – coherent

The various configurations are stored in part of the memory in the unit. This memory can be set up by use of front-panel switches or by the computer input.

For more flexible control, the system connects to a Nova minicomputer interface permitting the system to be changed and controlled by the Nova. The minicomputer is able to advance the frame, select mode, sweep speed and delay, and write up to 32 characters on the screen per data frame. Additional characters can be added by successive data frames if the film is not advanced.

The minicomputer interface consists of 16 data lines (bidirectional) and 5 control lines. Data blocks of up to 32 control words and up to 32 character generator words will be transferred at any rate established by the computer. The expected rate is a block of data for each camera frame advance. Each of the control words or character generator words is preceded by a 16-bit address word, of which only the 6 LSBs are used. The address words and data words are interleaved, with each address word preceding each data word.

e. Sweep Delay Generator and Sweep Counter

A sweep delay generator will delay the trigger input signals in accordance with the control word. This logic will operate when the delay word and sweep count word are loaded into their respective counter. Each input trigger will freeze the delay word and then allow the delay counter to count from the complement of this word up to full count. Full count is decoded, and the decode pulse becomes the delayed trigger output to the oscilloscope.

The sweep counter counts the number of sweeps and locks out the sweep circuit after a predetermined number. When the camera frame advance is enabled, the sweep count word is frozen and the sweep counter and delayed trigger outputs are enabled. Each delayed sweep trigger is counted. When the predetermined number of sweeps has been generated, a flip-flop is reset which disables the trigger output for the remainder of the exposure interval and returns the sweep counter to its initial state.

f. Signal and Intensity Controls

The signal control unit is capable of accepting two input signals (video and pedestal) and adding them together. For position control, the two video signals will be summed with the output of a 4-bit D/A converter and fed to the "Y" input of the oscilloscope. This will allow the position of the video signal on the oscilloscope face to be controlled by the computer. Additionally, a pedestal waveform can be summed with the video signal to provide additional operational information.

The Z-axis control unit is used to control the trace intensity. The video input enables an input gate signal to be used to intensify a portion of the trace. A 3-bit control word is used to control the average intensity. To allow a nonlinear conversion from a digital number to intensity, the 3 bits are decoded and used to selectively drive a 6-bit D/A converter so that the output is one of eight selected voltage levels. These levels are summed through an operational amplifier along with the video intensity control signal and routed to the Z-axis input of the scope.

g. Character Generator

This device will provide the means for presenting alphanumerical information anywhere on the face of the CRT. Besides mode and altitude, other information might be velocity, attenuator settings, length of range gate, etc. A further use might be to label each trace so that one could positively identify the source of video and other control parameters. This system augments the LED display of TOD which is implemented directly from the existing Astrodata clock. The character generator accepts digital inputs and generates the required X-Y position and video data to form the characters. The specified word is as follows:

Alphanumeric characters	6 bits (ASC11 code)
X-position	6 bits (64 positions)
Y-position	4 bits (16 positions)
Size of character	2 bits (4 sizes)

The requirements were satisfied by a direct, stroke-writing character generator which creates small vectors (vector summations of ΔX and ΔY) to produce the desired characterizations. In this system, implementation of any character on a CRT requires establishing spot position during blanking time and generating unblanking signals coincident with the required vector summations. The entire system consists of a buffer decoder for decoding character information, deflection information, and size information. It also includes a ROM-type character generator, the D/A converters required to produce the incremental deflections, and the D/A converters required to produce position offsets.

A complete unit that does most of the necessary functions was purchased as the Monitor Systems 8041. It provides the character selection and distribution, character orientation, character size, timing and control, incremental D/A conversion (ΔX, ΔY), and blanking (video). The characters are generated using up to 22 strokes and can be written in 6 μsec or less. The total throughput of the system will average 15 μsec/character (3 μsec for the character generator, 2 μsec data transfer from memory, 10 μsec D/A settling time). Hence, all 32 characters can be written in about 480 μsec.

C. DISTRIBUTION SYSTEM

The IF and trigger signal distribution system was added to facilitate the addition of the BATS equipment, to provide for any future growth, and to accommodate the needs of SSP. The IF distribution system terminates the IF signals coming from both the TRADEX and ALTAIR radars and the analog target simulator, and distributes these signals to BATS, TADCO, and the SSP. The system consists of 40 separate amplifiers housed in a cabinet next to TADCO. Each of the amplifiers has a single input and four isolated outputs. Through a set of patch cables, these outputs can go either directly to the signal-processing system or to a set of electronic switches housed in the same cabinet. These SPDT switches can switch the processors to either radar or the simulator signal source.

Adjacent to the IF distribution system is a card cage containing a set of line receivers and drivers to fan out the TRADEX digital mode signals. These units are all TTL integrated circuit modules. A special card exists for the ZRT signal which has a rise time of about 10 nsec. This particular signal is received and distributed as a balanced 100-ohm system.

1. List of IF Input Signals

TRADEX	ALTAIR
L-band Sum LCP	UHF: Lightweight LCP
L-band Sum RCP	LCP
L-band Delta Az	RCP
L-band Delta El	Delta Az
60-MHz Reference	Delta El
S-band LCP	Uncompressed LCP
S-band RCP	VHF: LCP
120-MHz Reference	RCP
S-band Burst	Delta Az
10/150-MHz Reference	Delta El
	60-MHz Reference

Analog Target Simulator

UHF: LCP
RCP
Delta Az
Delta El
Lightweight LCP
Uncompressed

2. IF Distribution Amplifier Specifications

a. Inputs

Frequency range (nominal)	
Unit 1	40 to 80 MHz
Unit 2	80 to 160 MHz
Unit 3	5 to 160 MHz
Input signal	Up to +12 dBm maximum
Impedance	50 ohms
VSWR	1.1:1 over the frequency range from 50 to 70 or 90 to 150 MHz; 1.2:1 elsewhere. 1.5:1 for Amplifier 3.
Noise figure	8 dB or less from 50 to 70 MHz, and 9 dBm or less elsewhere.
Quantity of Units	
Unit 1	36
Unit 2	4
Unit 3	2

b. Outputs

Number of isolated outputs	4
Impedance	50 ohms
VSWR (looking into the output port)	1.2:1 from 50 to 70 or 90 to 150 MHz; 1.4:1 elsewhere.
Gain	From input to any output port, 0 ± 1 dB adjustable by screwdriver adjustment on each output port located on front face. Gain stability ±0.1 dB over the temperature range.
Signal level	+13 dBm maximum output with <0.5-dB gain compression at any frequency in the nominal range.
Intermodulation distortion	The third-order intercept point is >+28 dBm for two equal level signals anywhere in the nominal frequency range.
Linearity	From input to any output, 0.1 dB over the range from +7 to −73 dBm.
Isolation	When three of the four output ports change from a terminated to an unterminated condition, the output of the fourth port should change <0.05 dB. When one output port is short circuited, the other output ports change <0.2 dB. Signals within the frequency and power level range of the unit injected into one output port appear at least 60 dB down at all other ports.

Frequency response	Each output is flat within ±0.1 dB from 50 to 70 MHz, or ±0.2 dB from 90 to 150 MHz (Amplifier 3, ±1.5 dB).
Stability	Amplifier is stable with any load impedance attached to any of the output ports.
Phase shift	The phase shift through each amplifier is linear to ±3° (i.e., constant time delay) over the frequency ranges from 50 to 70 MHz and 90 to 150 MHz. The phase shift at 60 or 120 MHz varies no more than ±10° from amplifier to amplifier and ±3° from one output port to another on the same unit. The phase shift is stable to ±1° over the temperature range of the unit (or for any other cause). Phase shift does not vary more than ±1° over the full dynamic range (up to +10 dBm).
Tilt	Each amplifier has a control (screwdriver) to adjust the tilt of the bandpass characteristic to compensate for long cable runs. It is capable of adjustment from no tilt (flat response) to a maximum of 0.25 dB/10 MHz (rising with frequency).

3. Electronic SPDT Coaxial Switch Specifications (Daico No. 100C0461)

Frequency range	40 to 150 MHz
Isolation	80 dB
Insertion loss	<0.5 dB; repeatability ±0.1 dB
VSWR	50 ohms
40 to 80 MHz	1.1:1
90 to 150 MHz	1.2:1
Amplitude flatness	±0.25 dB
Phase linearity	±1.0°
Signal level	1-dB compression, +27 dBm
Switching speed	To within 0.25 dB of full on, 3 μsec
In-band transients	−70 dBm
Input switching signal	TTL logic levels

D. BURST MATCHED FILTER (BMF) AND BUTLER MATRIX

The BMF, constructed at Lincoln Laboratory, provides real-time Doppler discrimination for bulk filtering. A matched filter is required for each resolvable radial velocity (≈900 m/sec) which is expected to occur. The realization of this filter bank is simplified by sharing elements common to the individual filter channels. In this BMF, the pulse burst is first "collapsed" using delay lines common to all Doppler filter channels. Each individual filter channel is then generated with a set of vernier delays which represent the additional time shifts caused by the particular Doppler shift. The number of elements required is significantly reduced by sharing of the vernier delays in a Butler-type of phase matrix.

Figure IV-21 shows a simplified schematic of the BMF. The system input is the pulse compressed, weighted burst from TRADEX. There are 16 pulses in the burst, each 100 nsec wide and spaced 5 μsec apart. The input signal at 60 MHz is mixed in two steps to a center frequency of 37 MHz (dictated by the delay line) and then divided into 16 similar channels. Each channel has a delay line with delays of $T = T_o + (n - 1)\,5$, where $n = 1, 2, \ldots, 16$ and T and T_o are in

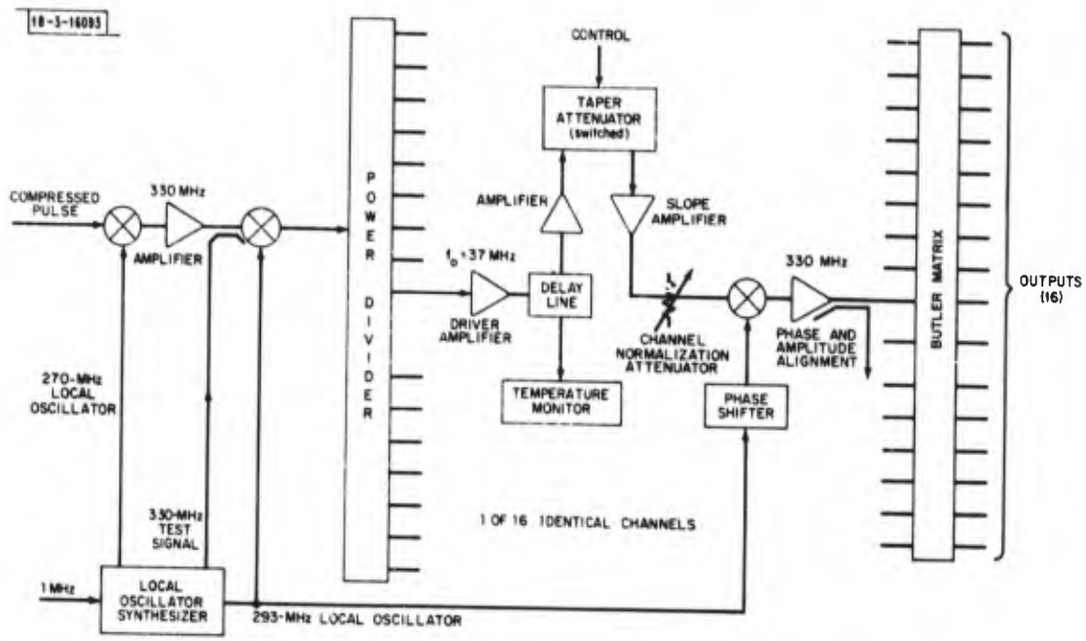


Fig. IV-21. Simplified schematic of BMF.

microseconds. T_o is about 10 μsec. The acoustic delay lines are constructed of zero temperature coefficient (ZTC) glass and are enclosed in ovens to maintain a ±0.5° phase stability. The delayed burst is then mixed up to a 330-MHz IF and the channel outputs are Doppler filtered in the Butler matrix. A variable attenuator in each channel allows channel-to-channel normalization. A phase shifter in the 293-MHz input to the mixer provides phase alignment capability.

The operation of a matched filter for a uniform burst signal waveform can be understood by assuming a zero Doppler shift, and delay lines that are trimmed to be exact multiples of the IF period. The pulses will add coherently to a maximum value when more than one pulse is present at the same time in the output combiner. Therefore, a maximum occurs when one pulse from each channel is in the combiner at the same time. However, when a Doppler shift is present, the delay lines are no longer an integral number of periods long for the new frequency. The IF pulses in each channel experience a phase shift relative to those in another delay channel which is proportional to both the Doppler shift and the time delay in the given channel. Therefore, a uniform phase variation from channel to channel exists, and the pulses no longer add to a maximum when summed.

A Doppler filter can be constructed which is matched to any given Doppler shift by adding vernier time delays (phase shifts) in each channel that produce a phase slope which just cancels the Doppler-created phase slope. Such a filter is provided by the Butler matrix. The 16 × 16 Butler matrix employed in the present design is shown in Fig. IV-22. The BMF channel outputs (1 to 16) feed the matrix inputs at the top of the diagram. The squares marked with an H represent IF hybrids. The circles denote coax phase shifts at the IF in units of 360/16 = 22.5°. The outputs at the bottom are labeled according to the number of resolvable Doppler cells they are removed from zero Doppler for positive frequency shifts (incoming targets).

An ambiguous Doppler velocity will occur when there is a 360° phase shift of the pulse in the first delayed channel. For this system, the overall ambiguous velocity corresponds to

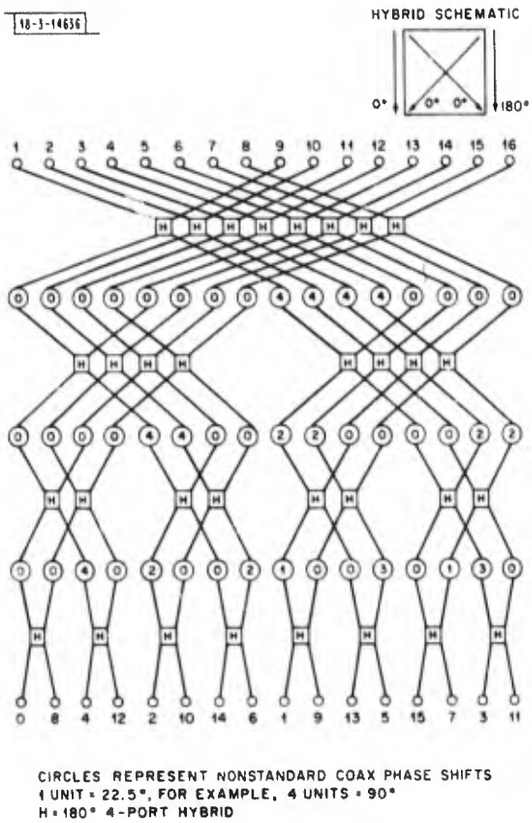


Fig. IV-22. 16-port Butler matrix.

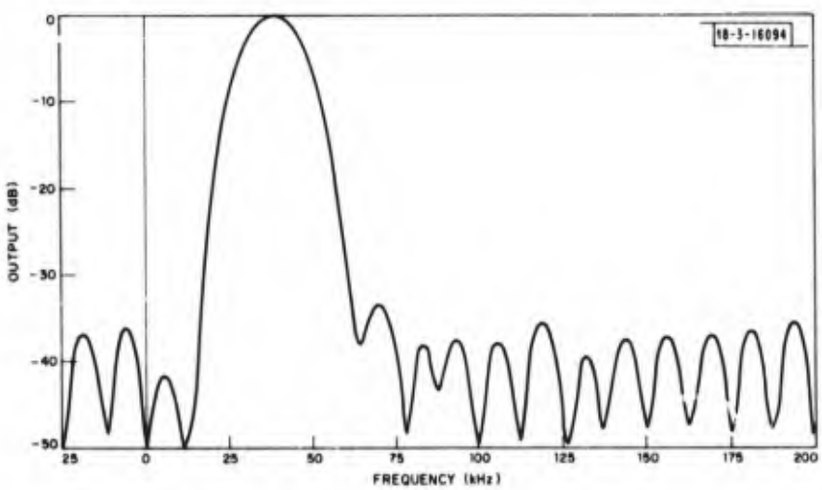


Fig. IV-23. Typical Doppler channel output (weighted).

a Doppler shift of 200 kHz for the 5-μsec pulse spacing. Assuming a transmitted signal about 3 GHz, this corresponds to a velocity of 10 km/sec with each Doppler cell in the Butler matrix having a resolution of 625 m/sec. Weighting is applied across the matrix to reduce the Doppler sidelobes. When this is done, the resolution degrades to about 900 m/sec but the Doppler sidelobes are reduced to −35 dB. A plot of the actual Doppler response of one of the channels in the system is shown in Fig. IV-23. This indicates a 6-dB bandwidth of 20 kHz and shows the peak sidelobe at −33 dB.

Fig. IV-24. Front view of cabinets comprising BMF system.

Figure IV-24 shows the front of the two cabinets comprising the BMF system. The 16 subchannels are packaged into 8 drawers, and the Butler matrix into one large drawer. The other drawers contain power supplies, test equipment, and an LO frequency generator.

E. VELOCITY SELECTION AND CHANNEL IDENTIFICATION (VSCI) SYSTEM

The function of the VSCI circuitry is to detect and process the output of the BMF and to send the information to the BSP. It accepts any 8 contiguous channels from the 16 available from the BMF. It log detects these signals, selects the largest, and passes this video signal to the BSP. The video signals are also sampled and held and the largest is passed to the BSP along with a binary number identifying the channel in which it occurred. It further accepts from the BSP two binary numbers designating the upper and lower limits of the Doppler channels to be processed, as well as a gate which determines sample time and initiates data transfer. A block diagram of the VSCI system is shown in Fig. IV-25.

Incoming signals from the BMF are at a center frequency of 330 MHz. These signals are processed in a set of log detectors. These units have a 3-dB bandwidth of 40 MHz, a log accuracy of ±0.5 dB, and a dynamic range of 70 dB.

The video output of each of the eight log detectors is split. One of the outputs goes directly to the circuitry which selects the largest video signal. The other output is first delayed in video

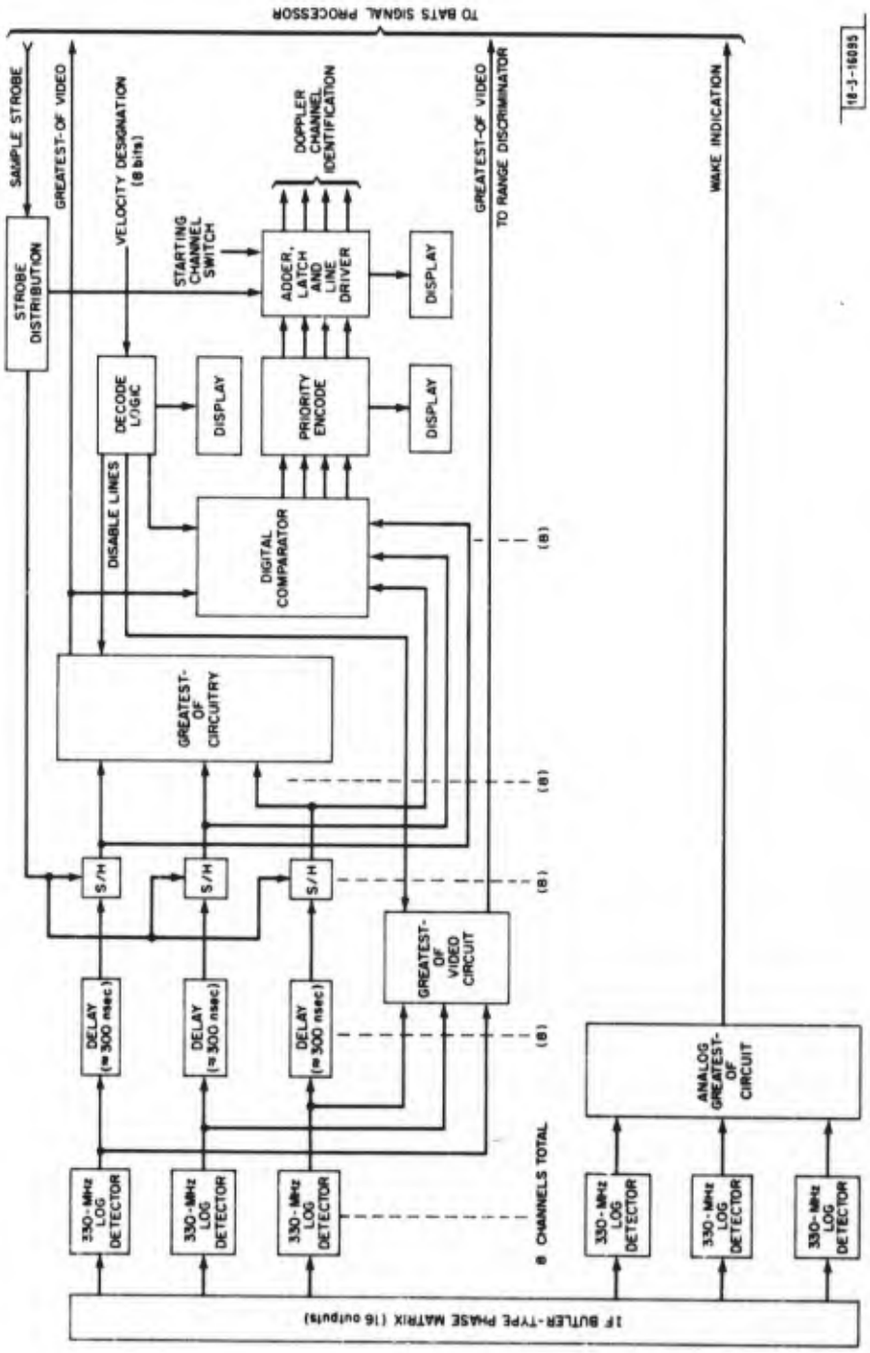


Fig. IV-25. VSCI system.

delay lines. There are two such lines in series, the first having a fixed delay of 250 nsec and the second a total delay of 100 nsec with taps each 10 nsec to permit adjustment. It is necessary to delay the video in order to match the delay in the BSP; that is, the delay is adjusted so that the video arrives at the sample-and-hold module at the same time as the sampling strobe.

The video "greatest-of" circuitry consists of eight wideband (MSK 760) operational amplifiers in a unity gain configuration, each driving, through a diode, a common load. The largest signal cuts off the diodes in the outputs of the other operational amplifiers. This largest signal is inverted in a ninth operational amplifier on the same board and acts as a line driver to transmit this signal to the BSP. The BSP indicates which Doppler channels are to be disabled. This is done by small reed relays which can connect the summing junction of the operational amplifiers to −5 V when so instructed by the decoding logic.

The eight sample-and-hold units which accept the delayed video and the sampling gate are Data Device VSSH-F-3 and have an aperture time of less than 300 psec.

From the sample-and-hold units, the signals go to another group of greatest-of circuits. In this circuit, the amplifier with the largest signal drives current into the summing junctions of the other amplifiers so that they do not function as amplifiers and the "greatest" level exists at the common point. With the diodes in the feedback loop, diode differences are minimized by the open-loop gain of the amplifiers. This circuit provides a higher accuracy than the other greatest-of circuit.

The outputs of the sample-and-hold modules also go to one input of eight comparators. The other input to the comparators is the inverted "greatest" analog level, offset by approximately 30 mV to avoid the oscillations occasioned when comparators are given nearly equal inputs. Thus, only one comparator will have an input signal greater than the video analog level and it will output a TTL logic signal. The signal is OR'd with an output of the channel disable circuit to permit shutting off unwanted channels. The outputs of the OR gates go to a priority type of decimal-to-BCD logic chip. The priority feature means that in case of equal values the BCD output will always be the larger number of the two.

The outputs of the comparators go to light-emitting display chips to visually indicate the channel number containing the largest signal. This is useful both in troubleshooting and alignment. The BCD outputs are inverted and brought to a 4-bit adder. The other input to the adder comes from a manual switch in which can be set the number of the highest channel of the sixteen available which is not being used. The BCD number next goes to a latching circuit, then to line drivers, and finally out to the BSP. Also included on this board is an LED numeric display to indicate the actual channel number. The gate for the latching circuit is derived from the sample strobe. This strobe is time expanded, delayed, and sent to the latching circuit to permit data transfer.

A special decode logic board develops the signals to perform the channel enable/disable function. The BSP sends to the VSCI circuitry two BCD numbers, one of which indicates the highest channel and the other the lowest channel it wishes to process. The logic works such that when an upper channel number is received, that channel is enabled along with all other lower channels down to and through the channel number indicated in the lower Doppler estimate. A light display indicates the enabled channels for use in troubleshooting and alignment.

Also shown on Fig. IV-25 is the wake indicator circuitry. This consists of three log detectors connected to the lowest three Doppler channels. It is from these that a wake indication is expected. The 3-input greatest-of circuit determines the output to be sent to the BSP for determination of the presence of wake on a given target.

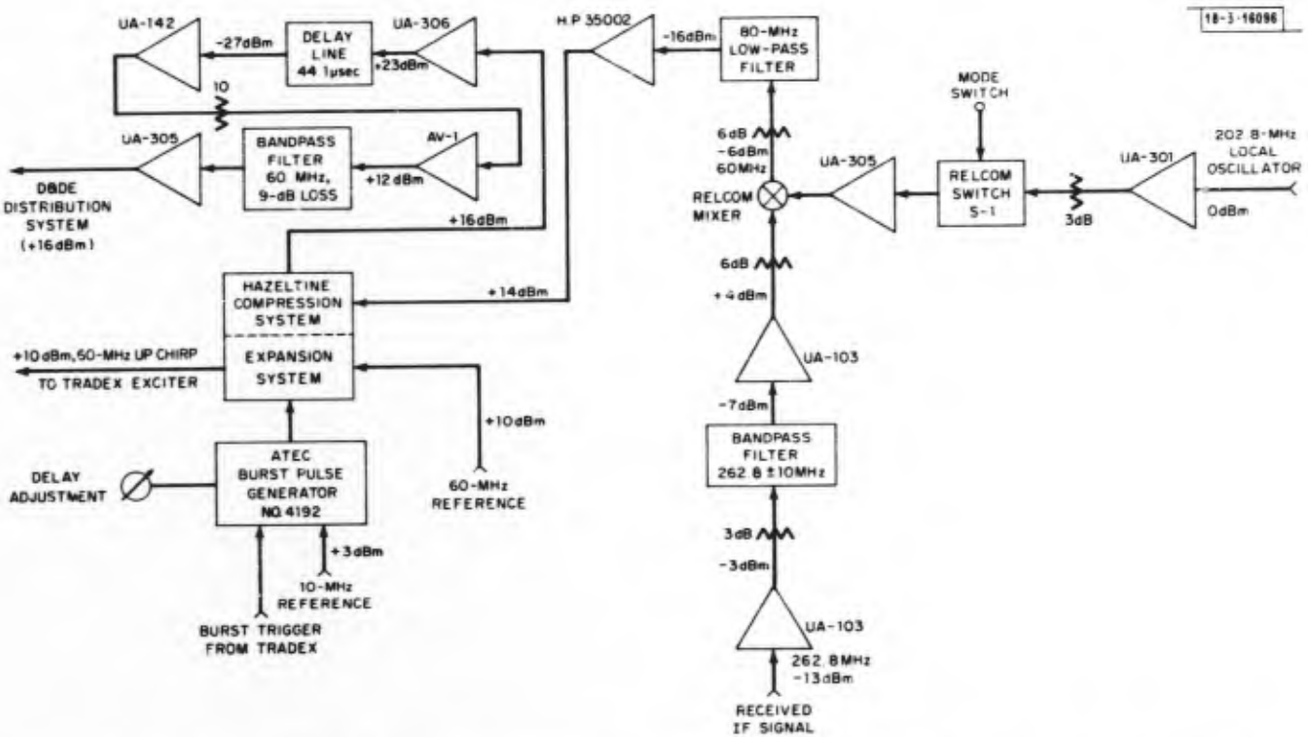


Fig. IV-26. TRADEX/BATS receiver-exciter equipment. Note: All amplifiers are Avantek unit type unless otherwise noted; all power levels are maximum.

F. TRADEX/BATS RECEIVER-EXCITER MODIFICATIONS

A block diagram of the equipment added to TRADEX to generate and compress the burst pulse waveform is shown in Fig. IV-26. This contains a special burst pulse generator which, after receiving a start trigger from the TRADEX timing system, generates 16 trigger pulses synchronous with a 10-MHz CW signal. These pulses are used to trigger the pulse expansion network producing the burst signal sent to the TRADEX transmitter. This equipment taps off of the TRADEX receiver system at an IF frequency of 262.8 MHz. This is then mixed down to a 60-MHz IF, and sent to the Hazeltine pulse-compression system. After compression, a delay line is inserted to time align the received signals in the BATS equipment. The delay line is a quartz type housed in a temperature-controlled oven and has a spurious level of −55 dB. The output of the pulse-compression system goes through a long semirigid cable to the IF distribution system in the D&DE equipment room.

1. Pulse-Compression/Expansion Equipment

The Hazeltine Expansion Unit accepts the burst generator triggers and a 60-MHz CW reference signal. Its output is an expanded RF pulse signal which has a rectangular envelope for a duration of 2 μsec. This pulse is generated as the impulse response of a surface wave dispersive line which has a dispersion of 2 μsec over a bandwidth of 20 MHz. The instantaneous frequency at the center of the pulse is 60 MHz, and the RF carrier phase is coherent with the 60-MHz CW reference. An expanded pulse is generated for each trigger which may have a minimum spacing of 3 μsec, although at present the spacing is 5 μsec.

Expanded Pulse Characteristics

Pulse width	2.0 ± 0.5 μsec between −6-dB points
Pulse rise and fall times	60 nsec maximum between 10- to 90-percent voltage points
Pulse flatness	±0.1 dB over ±0.8 μsec from pulse center
Pulse delay	2.62 μsec (nominal) between trigger and leading edge of expanded pulse
Pulse jitter	0.5 nsec rms (maximum)
Center frequency	60 MHz
Modulation	Linear FM; upchirp; 10 MHz/μsec
Amplitude	+10 dBm
Output impedance	50 ohms
Output VSWR	1.3:1 maximum, 40 to 80 MHz
Signal to noise	40 dB minimum
Signal to spurious	50 dB minimum

The Compression Unit is the matched filter for the expanded pulse. Compression is obtained by the use of a surface wave line having an opposite-slope dispersive characteristic. Back-to-back operation of the Expansion and Compression Units results in a weighted compressed pulse which has a 6-dB width of less than 0.1 μsec and sidelobe levels which are greater than −33 dB down.

Compressed Pulse Characteristics

Pulse width	0.09 μsec at the −6-dB points
Pulse sidelobe level	−33 dB maximum over ±2-μsec compressed pulse interval
Spurious output	−40 dB maximum beyond ±2-μsec compressed pulse interval
Gain	30 dB (nominal)
Dynamic range	Compression <1 dB for +20-dBm output signal level
Output noise	<−60 dBm (input terminated)
Center frequency	60 MHz
Phase jitter	<1.0° rms over an observation interval of 0.1 sec
Input and output impedance	50 ohms
Input VSWR	1.2:1 maximum (40 to 80 MHz)
Output VSWR	1.3 maximum (40 to 80 MHz)

a. Expansion Unit

A simplified block diagram of the Expansion Unit is shown in Fig. IV-27. The unit is divided (as shown by the dashed lines on the diagram) into four sections comprising:

(1) Spectrum Generator
(2) Trigger and Gate Electronics
(3) Surface Wave Expansion Line
(4) Output Circuits.

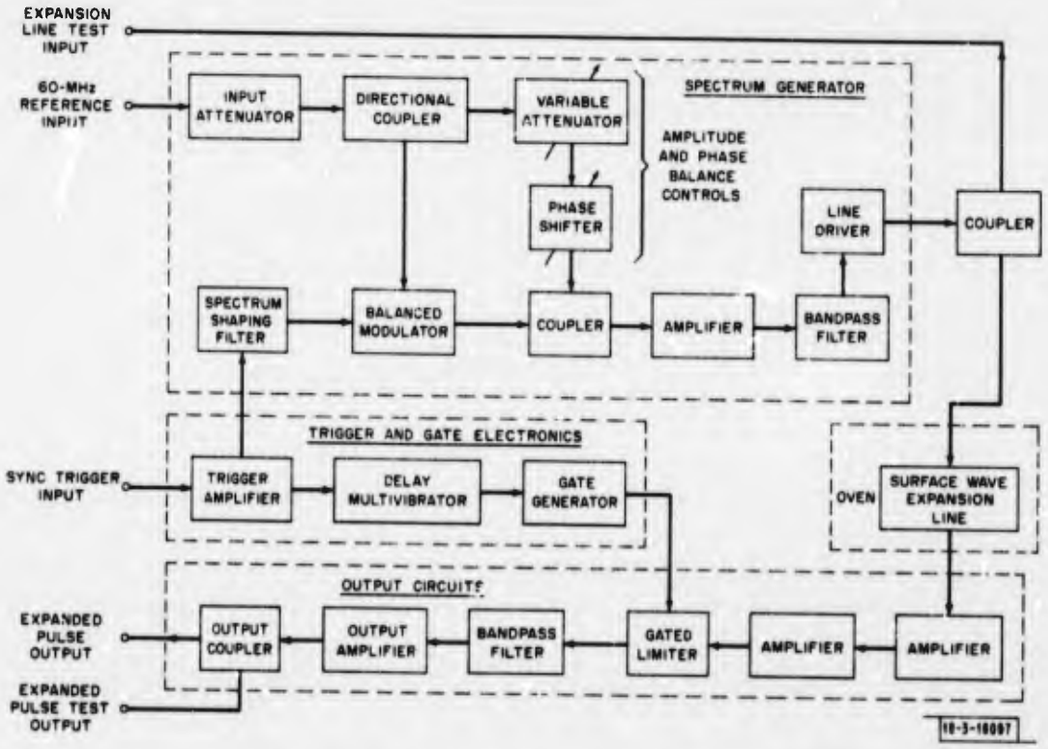


Fig. IV-27. Expansion Unit block diagram.

The spectrum generator accepts the sync trigger and the 60-MHz reference and produces a generally rectangular spectrum which has a bandwidth of about 40 MHz centered at 60 MHz. The waveform is an RF pulse with a time duration of about 25 nsec. This pulse is used as the input to the surface wave dispersive (expansion) line. The time output of the spectrum shaping filter is a video waveform which is approximately the impulse response of the filter.

A 40-MHz spectrum centered at 60 MHz is obtained by modulation of the 60-MHz reference by the output of the spectrum shaping filter in a doubly balanced diode modulator. The modulator has a carrier balance of about 35 dB which is improved by coupling a sample of the 60-MHz reference, which is 180° out of phase with the carrier residue, into the signal path after the modulator. The directional coupler provides a −15-dB sample of the reference. Amplitude and phase control of the sample are provided by a constant impedance variable attenuator and a phase adjuster. The sample is coupled into the main signal path by a second −15-dB directional coupler.

The output of the balanced modulator is an RF pulse which has a carrier frequency of 60 MHz and a pulse duration equal to the reciprocal of the 40-MHz bandwidth, or 25 nsec. This signal is amplified, filtered, and amplified again. The delay gate is generated by monostable multivibrators. To allow for a fast repetition rate (up to 300 kHz) and a pedestal delay of approximately 2.5 μsec, the delay portion of the gate is implemented using two multivibrators. The first half allows for a delay of approximately 1.5 μsec, and the second half allows for the remaining delay. The third multivibrator generates the 2-μsec gate. The output gate is fed to a double-balanced diode modulator which is used as a gated limiter for the expanded pulse.

A surface wave dispersive line is used to generate the linear FM expanded pulse. The input to the line is the output from the spectrum generator line driver. The surface wave line is configured on a 1-inch-long piece of Y-cut, Z-propagating lithium niobate. This material is piezoelectric which permits the generation of an elastic surface wave by an electric signal.

An interdigital transducer is used to couple electromagnetic energy to a surface wave, and vice versa. The interdigital transducer is comprised of a metalization pattern on the surface of the substrate. This pattern consists of two sets of interleaved electrodes (or fingers). An impulse applied to the input transducer generates, by piezoelectric action, an elastic wave on the surface of the substrate. The induced surface wave consists of a wave-packet having crests and troughs determined by the acoustic half-wave spacing of the metalization pattern. A charge is induced in the output transducer by piezoelectric action as the surface wave passes beneath the output transducer metalization pattern. If the length of the input transducer is short compared with the length of the output transducer, then the electrical output waveform carrier cycles correspond to the acoustic half-wavelength spacing of the metalization pattern. The fingers are spaced quadratically, and the output signal is a linear FM waveform. Matching networks are used at the input and output of the line to obtain a match to 50-ohm coaxial cable. The entire assembly is hermetically sealed and is contained in a DC proportional-control oven.

The line has a total insertion loss of about 52 dB. This loss consists of a CW insertion loss of 33 dB, an expansion loss of 16 dB, and an additional 3 dB due to the 40-MHz input-spectrum bandwidth which is reduced by the line to the 20-MHz signal bandwidth. The output of the expansion line is first amplified and then gated and limited. The gated-limiter consists of a double-balanced diode mixer. The diode balance results in about 40-dB suppression in the absence of an input gate from the gate generator. When the 2-μsec gate from the gate generator is present, the diode bridge is unbalanced which results in an output signal. The input drive is sufficient to drive the diodes into limiting, and the unit thus operates as a gated-limiter. Insertion loss is

about 6 dB. The output of the gated-limiter (mixer) is fed to a 40-MHz-wide bandpass filter and sent to an output amplifier.

b. Compression Unit

The compression unit also operates at a carrier frequency of 60 MHz. It is designed for 30-dB gain where the gain is defined as the ratio of the peak expanded pulse input to the peak compressed pulse output. The absolute maximum input signal level is −10 dB which thus corresponds to a +20-dBm compressed pulse output. The noise output of the unit for a terminated input is −72 dBm. The Compression Unit uses an acoustic surface wave line to collapse the 2-μsec expanded pulse. Amplitude response of the line is weighted to reduce the sidelobes associated with the compressed pulse to below −33 dB. Weighting broadens the compressed pulse and also results in a small mismatch loss of 1.25 dB.

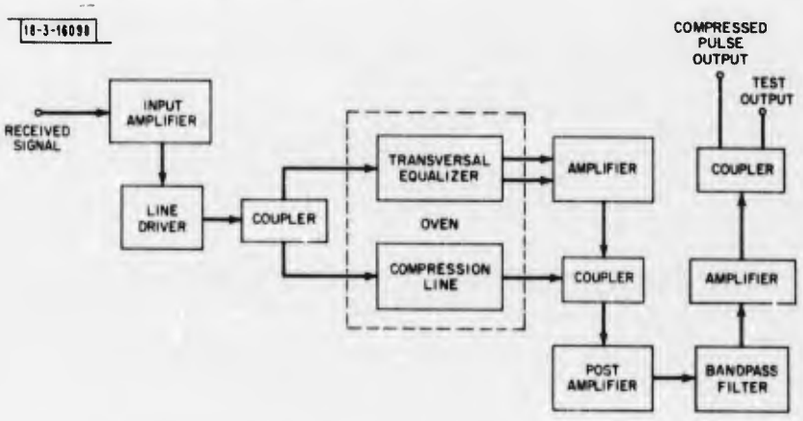


Fig. IV-28. Pulse Compression Unit block diagram.

A block diagram of the compression system is shown in Fig. IV-28. The line driver output is fed to the acoustic surface wave compression line. Construction of this line is similar to that of the expansion line which was described previously. The line differs from the expansion line in two respects:

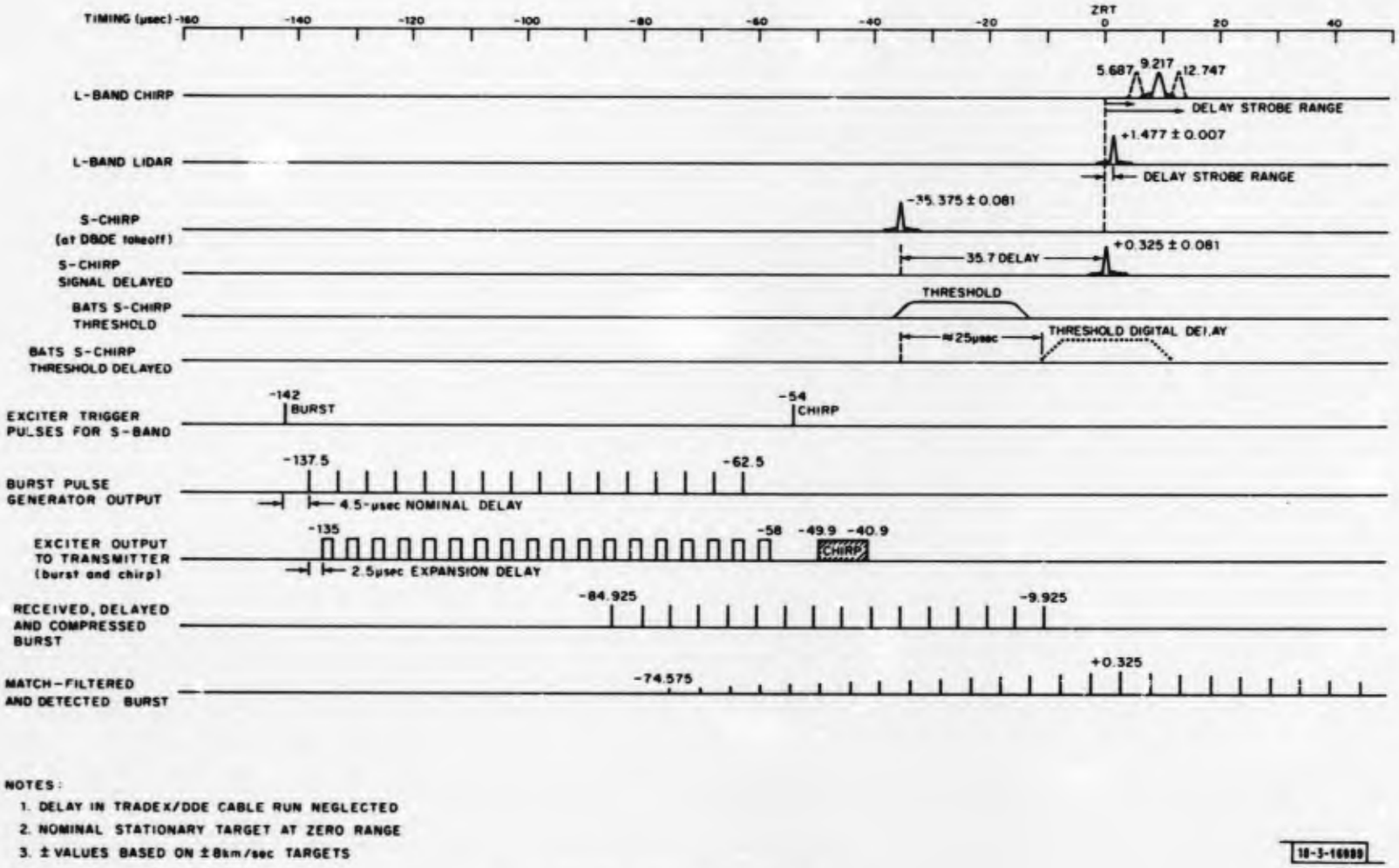
(1) The dispersive interdigital pattern is reversed. The impulse response of the line is a down-chirp pulse which is the time inverse of the instantaneous frequency vs time function of the expanded signal. Thus, the compression line is the matched filter for the expanded pulse and the output is a short pulse whose time duration is approximately the reciprocal of the signal bandwidth.

(2) Weighting is incorporated in the compression line to reduce the sidelobe level of the collapsed signal. Normally, this would be achieved by a filter having a bell-shaped frequency response. A similar effect is achieved in the surface wave implementation by varying the overlap of the interdigital fingers. The loss in the compression line is comprised of the insertion loss of the surface wave line, which is about 26 dB, and the loss due to the finger apodization, which is an additional 5 dB. These losses are partially negated by the compression gain of 16 dB, so the net loss is 15 dB.

A parallel transversal equalizer is used to reduce the near-in sidelobe level to −33 dB. The equalizer is comprised of two 15-dB directional couplers, a two-tap surface wave compression line, a resistive summing network, and an amplifier. The equalizer operates to provide two replicas of the compressed pulse properly displaced in time and 180° out of phase with the distortion echoes which exist in the main signal. These echoes are added to the main signal in the second 15-dB coupler to cancel the distortion echoes. The output of the surface wave line is fed to a low-noise amplifier followed by a filter and an output amplifier.

2. TRADEX Timing

The timing of the burst, normal S-band chirp, and L-band is critical for the proper operation of BATS. Figure IV-29 is a summary of this timing, showing the relationship of the trigger pulses, transmitter output, receiver signals, and match filtered pulses. The two adjustments to the system that are available are the burst pulse generator delay (nominally 4.5 μsec) and the L-band delay strobe (up to 10 μsec for chirp, and 1 μsec for LIDAR). The reference to which all timing is set is always the S-band chirp pulse.



NOTES:

1. DELAY IN TRADEX/DDE CABLE RUN NEGLECTED
2. NOMINAL STATIONARY TARGET AT ZERO RANGE
3. ± VALUES BASED ON ±8km/sec TARGETS

18-3-16999

Fig. IV-29. BATS/TRADEX timing.

V. SUMMARY OF INTERFACE SPECIFICATIONS

A. TRADEX/BATS

1. IF

L-Band (ΔAz and ΔEl, LC and RC Sum)

Center frequency	60 MHz
Bandwidth (weighted)	Chirp, 450 kHz; LIDAR, 12 MHz
Noise level	See Tables V-1 and V-2
Maximum signal	+10 dBm
Impedance	50 ohms, 1.3:1 maximum VSWR

S-Band (LC)

Center frequency	120 MHz
Bandwidth (weighted)	Chirp, 12 MHz; wideband burst, 40 MHz
Noise level	See Table V-3
Maximum signal	+10 dBm
Impedance	50 ohms, 1.3:1 maximum VSWR

60-MHz CW Reference

Frequency	60 MHz
Level	+14 dBm (±1 dB)
Form	CW coherent with 10-MHz range zero reference
Terminating impedance	50 ohms, 1.5:1 maximum VSWR

120-MHz CW Reference

Frequency	120 MHz
Level	+9.6 dBm (±1 dB)
Form	CW coherent with 10-MHz range zero reference
Terminating impedance	50 ohms, 1.5:1 maximum VSWR

BATS Burst

Center frequency	60 MHz
Bandwidth (weighted)	12 MHz
Terminating impedance	50 ohms, 1.3:1 maximum VSWR
Maximum signal level	+10 dBm
Noise level	−50 dBm ± 12 dB

TABLE V-1

L-BAND LIDAR (2-20)

TRADEX Attenuator Setting		Noise Level (dBm) at BATS	Maximum Dynamic Range (dB)	Approximate Signal Level (dBm) for −30-dBsm Target at 150 km
RF	IF			
0	0	−51.7	62	−2
0	8	−58.8	69	−10
0	16	−63.4	73	−18
0	24	−64.9	75	−26
0	32	−65.3	75	−34
32	8	−57.4	67	−42
32	16	−62.8	73	−50
32	24	−64.8	75	−58
32	32	−65.2	75	−66
32	40	−65.3	75	–

TABLE V-2

L-BAND CHIRP (50-1)

TRADEX Attenuator Setting		Noise Level (dBm) at BATS	Maximum Dynamic Range (dB)	Approximate Signal Level (dBm) for −30-dBsm Target at 150 km
RF	IF			
0	0	−57.2	67.2	+6
0	8	−63.7	73.7	−2
0	16	−67.3	77.3	−10
0	24	−68.0	78.0	−18
0	32	−68.2	78.2	−26
32	8	−62.4	72.4	−34
32	16	−66.7	76.7	−42
32	24	−68.0	78.0	−50
32	32	−68.4	78.4	−58
32	40	−68.5	78.5	−66

TABLE V-3

S-CHIRP (9-17.6)

TRADEX Attenuator Setting		Noise Level (dBm) at BATS	Maximum Dynamic Range (dB)	Approximate Signal Level (dBm) for −30-dBsm Target at 150 km
RF	IF			
0	0	−46	56	−14
0	8	−52	62	−22
0	16	−54.7	65	−30
24	0	−43.9	54	−38
24	8	−50.6	61	−46
24	16	−54.2	64	−54
24	24	−55.2	65	–
24	32	−55.4	65	–
24	40	−55.5	65	–

2. Timing Signals

10-MHz Range Zero Reference

Level	2.3 V peak-to-peak
Terminating impedance	50 ohms, 1.5:1 maximum VSWR at center frequency
Transmission	Mixed with 150 MHz

150-MHz CW Reference

Level	2.4 V peak-to-peak (+11 dBm)
Form	CW coherent with 150 MHz and ZRT
Terminating impedance	50 ohms, 1.5:1 maximum VSWR

Zero Range Trigger (ZRT)

Terminating impedance	50 ohms (appears as balanced 100-ohm line)
Level	−0.8 + 0.1/−0.5, −1.7 ± 0.15 V (push-pull) at the driver
Timing	Phase coherent with L-band range start
Pulse width	100 nsec; rise time, 20 nsec

3. Digital Mode Signals

Electrical characteristics of all the digital mode signals are: terminating impedance = 75 ohms to +4.5 V; level = 0 ± 0.45, +3.7 ± 1.0 V; rise time is less than 0.2 μsec (logical one = +4 V). Signals are updated each PRI at ZRT − 200 μsec (except signals 14, 15, 16, and 17) except during the 100-msec control and update interval when it occurs at about −130 μsec.

Signal List

1-6 L-band mode

D&DE Designation						
CW	WBX	D	C	B	A	
0	0	0	0	0	0	Chirp
0	0	0	0	1	0	Chirp extended sampling
–	1	0	1	0	0	LIDAR
–	1	0	1	0	1	LIDAR LC extended sampling
–	1	0	1	1	0	LIDAR RC extended sampling
–	1	1	0	0	0	Burst A (32 at 14 μsec)
–	1	1	0	1	0	Burst B (16 at 14 μsec)
–	1	1	0	0	1	Burst C (32 at 28 μsec)
1	0	0	0	0	0	
1	0	0	0	1	0	50 μsec CW
1	0	Any code				

7 L-band dropped pulse (scheduled)

8-12 S-band mode

D&DE Designation					
NCX	D	C	B	A	
0	0	0	0	0	Chirp (NB)
1	0	0	0	1	Pulse pair
0	0	0	1	0	NB chirp extended sampling
1	0	0	1	1	Pulse pair extended sampling
1	0	1	0	0	NB burst
1	0	1	0	1	PRI pulse pair
1	0	1	1	0	PRI pulse pair extended sampling
1	0	1	1	1	WB chirp
1	1	0	0	0	WB burst
1	1	0	0	1	NB chirp – frequency jump
1	1	0	1	0	NB chirp – FJ – extended sampling
1	1	1	0	1	Pulse pair – FJ
1	1	1	1	0	Pulse pair – FJ – extended sampling
1	1	0	1	1	Burst – frequency jump
1	1	1	0	0	BATS burst

13 S-band dropped pulse (scheduled)

14 ZRT pretrigger (updated at ZRT – 32 μsec)

15 Start of table (first ZRT before new pulse schedule)

16 S-unscheduled dropped pulse (availability time, transmitter fault) approximately at ZRT but within blanking gate

17 L-unscheduled dropped pulse (similar to 16)

18 Blanking gate (duplexer gate) – once per PRI covering interference region

B. BSP/VSCI INTERFACE

1. Sample-and-Hold Video (Burst Video "A")

The burst signal that BSP uses for target amplitude data.

Bandwidth	DC to 20 MHz
Level	
Maximum	2.048 V
Minimum	0.128 V
Impedance	93 ± 3 ohms
VSWR (maximum)	1.3:1

2. Greatest-of Video (Burst Log Video "C")

The burst processor output that BSP uses to generate target range data and burst processor S/H strobe. (The S/H strobe may also be generated from chirp video.)

Bandwidth	DC to 20 MHz
Level	
Maximum	2.048 V
Minimum	0.128 V
Impedance	93 ± 3 ohms
VSWR (maximum)	1.3:1

3. ATG IF Test Signal to Burst Processor

A train of 16 coherent IF pulses at 60 MHz. The pulses are generated by the Atec burst pulse generator and the IF switch. Provision is made for offsetting the IF frequency to simulate target Doppler.

Bandwidth	20 MHz
Center frequency	60 MHz
Frequency control	±6 kHz
Output impedance	50 ohms
VSWR (maximum)	1.5:1
Pulse spacing (synchronous with 10-MHz clock input)	5 μsec
Pulse width (adjustable)	100 to 200 nsec
Output level (maximum)	+7 dBm

4. Doppler Estimate

A 4-bit binary coded signal indicating Doppler cell containing the greatest signal.

Impedance	50 ohms
Level	
Maximum	1.6 ± 0.150 V
Minimum	−0.8 + 0.1, −0.5 V
Timing	Asynchronous 10-MHz rate during acquisition window

5. Doppler Designation

An 8-bit binary coded signal indicating maximum (DDU) and minimum (DDL) expected target Dopplers (4 bits each for maximum and minimum Doppler). This signal is sent to BATS via RTI and is then sent to the burst processor.

Impedance	75 ohms returned to +4.5 V
Level	0 ± 0.45, 3.7 ± 1.0 V
Rise time	0.2 μsec
Number of lines	8

6. Range Strobe

Originates in BSP and is transmitted to burst processor.

Impedance	93 ohms
VSWR	1.5:1 maximum
Level	TTL compatible
Pulse length	20 nsec
Rise time	6 nsec

C. BATS/RTI INTERFACE

1. Introduction

The BSP may operate in any of the following ten mutually exclusive modes:

(a) Normal Mission Mode
(b) Computer Mode A (Modified Mission Mode)
(c) Computer Mode B (Loop Test)
(d) Computer Mode C (Register Test)
(e) Computer Mode D (Memory Test)
(f) Computer Mode E (Timing Test)
(g) Computer Mode F (Simulate Mode)
(h) Computer Mode G (RTI to Minicomputer)
(i) Computer Mode H (RTI from Minicomputer)
(j) Computer Mode J (RTI to ATG).

The Normal Mission Mode and Computer Mode A (Modified Mission Mode) will be used in connection with real-time mission operation. Computer Mode A is used to set a mask on the BATS status register to disable setting of RTI Interrupt Request 11 assigned to the BATS equipment. In Computer Mode F (Simulate Mode), the BSP input is disconnected from the RTI, Channel 0, and connected to the SimController for use in REDD simulations. The remaining BATS modes are used for test and calibration. The sources of control for Modes A through E are the RTI, minicomputer, or the local control panel. Mode F is only available when not under minicomputer or panel control. Mission Mode and Computer Mode A are the only modes where the analog equipment receives all control signals.

a. Normal Mission Mode

In Normal Mission Mode, BATS is operated by software residing in the CDC 6600 computer. BATS receives its instructions from the 6600 by way of the RTI. To operate BATS, the user must select BATS with External Device (ED) Select Code 011 along with the Control Key 000 designating Normal Mission Mode. Three 60-bit Designation Words must be transferred to BATS to specify its operation. After BATS has completed its assigned task, it has available to the 6600 three 60-bit Header Words and a maximum of 128 Target Words. If BATS fails to respond to a select, the user may check that the RTI ED status lines on Channel 0 read 000, indicating that BATS is ready for RTI operation. If ED status on Channel 0 is 001 from BATS, it is in a local operational mode and the select from the RTI is ignored. Other unexpected BATS operations may be determined by reading the BATS Status Register.

b. Computer Mode A (Modified Mission Mode)

This mode is used to mask the Status Register. The mode is identical with the Normal Mission Mode except that the proper Operational Control (OC) Word, with the mask, is first transferred on RTI Channel 0 with Control Key 001. The three Designation Words are then transferred to the BSP using Control Key 010. Thereafter, operation continues as in Normal Mission Mode.

c. Computer Mode B (Loop Test)

This mode is used to connect the RTI Channel 0 to RTI Channel 1 inside the BSP. The proper OC Word is first transferred on RTI Channel 0 using Control Key 001, the test word sent to the BSP using Control Key 010, and the same word is read back on RTI Channel 1 using Control Key 011

d. Computer Mode C (Register Test)

This mode is used to write/read BSP registers OC, C1, C2, HC3, H1, H2, and Status as determined by the Path Control bits of the OC Word. The proper OC Word is first transferred to the BSP on RTI Channel 0 using Control Key 001, the correct number of test word transfers are sent using Control Key 010, and the registers are read back by selecting the BSP on RTI Channel 1 with Control Key 010. No other Control Key on RTI Channel 1 (other than Status) is accepted until the BSP mode is changed or a BSP Master Clear is initiated.

e. Computer Mode D (Memory Test)

This mode is used to test the BSP target buffer. The starting address of the target buffer cell is specified in the OC Word. Words are then written in the target buffer using Control Key 010 up to the maximum of 128 locations. The last word written will have an EOM written at that location. The words can be read back on RTI Channel 1 by using Control Key 010.

f. Computer Mode E (Timing Test)

This mode checks the operation of the extrapolation of the Acceptance Gate Start Range.

g. Computer Mode F (Simulate Mode)

This mode is activated by the SimController rather than the OC Word. Thereafter, the BSP will receive its instructions from the SimController instead of RTI Channel 0. Data from the BSP are read on RTI Channel 1 using Control Key 000. The only other key allowed is Control Key 001 (Write Status by the SimController or Read Status by the RTI).

h. Computer Mode G (RTI to Minicomputer)

This mode is for transferring data from the RTI Channel 0 to the minicomputer. The proper OC Word is transferred on RTI Channel 0 to the BSP using Control Key 001, the data are transferred using Control Key 010, and the minicomputer stores the data in its core memory. This mode requires the user to supply a minicomputer program for accepting the data from the RTI.

i. Computer Mode H (RTI from Minicomputer)

This mode is for receiving data from the minicomputer on RTI Channel 1. The proper OC Word is transferred to the BSP on RTI Channel 0, and data from the minicomputer are received

on RTI Channel 1 using Control Key 100. The user must supply the minicomputer program to initiate the data transfer.

j. Computer Mode J (RTI to ATG)

Tnis mode is used to transfer the 13 control words to the ATG. RTI Control Key 110 is used to transfer the words. The user then proceeds with Computer Mode A or E. The 13 control words are described in the section on the Nova minicomputer to ATG Control (Sec. V-E). Only the 16 lowest-order bits of each 60-bit word are used.

2. Operational Control (OC) Word

Transferred to the BSP on RTI Channel 0 using Control Key 001, the OC Word is used for defining all modes of BSP operation except Normal Mission Mode. If the OC Word specifies word transfers on RTI Channel 0 (all modes except Computer Mode H), the word transfers must take place on RTI Channel 0 using Control Key 010.

MASK (0-7)

Mask – (8 bits) specifies the mask to be applied to the 30-bit status register to inhibit a RTI priority interrupt. The following bit convention is used:

OC Word Bit No.	masks	Status Request Bit No.
0		0-3
1		4-7
2		8-11
3		12-15
4		16-19
5		20-23
6		24-27
7		28-29

MEMORY ADR (17-23)

Memory Address – (7 bits) selects the starting address of the Target Buffer memory cell for a read/write operation. This field is used only under Computer Mode D (Memory Test).

PATH CTL (24-26)

Path Control – (3 bits) specifies which register or register sequences are to be read or loaded:

Path CTL Bits			
26	25	24	Register
0	0	0	OC
0	0	1	Seq. C1, C2, HC3, H1, H2
0	1	0	C1
0	1	1	C2
1	0	0	HC3
1	0	1	H1
1	1	0	H2
1	1	1	Status

MODE (27-29)

BATS Mode – (3 bits) specifies the mode of operation of the BATS equipment:

Bit 29	Bit 28	Bit 27	Mode
0	0	1	Computer Mode A
0	1	0	Computer Mode B
0	1	1	Computer Mode C
1	0	0	Computer Mode D
1	0	1	Computer Mode E
1	1	0	Computer Mode G
1	1	1	Computer Mode H

Note that Computer Mode F (Simulate Mode) is not called by the OC Word.

CR (30)

Continuous Run – (1 bit) specifies that the ATG is to continuously generate ZRTs when BATS is in Computer Mode E (Timing Test). No target data are collected by BATS but the Header Words can be read.

TEST ZRT (48-59)

Test ZRT – (12 bits, LSB = 1 μsec) specifies the time of generation of a ZRT Pretrigger with respect to the BSP Radar Binary Clock for test purposes. A ZRT is generated 32 μsec after the Pretrigger. This field is used with Computer Mode E (Timing Test).

3. BATS Control and Reply Words

The following is a listing of the Designation, Header, and Target Words that are received or sent by the BSP. It should be noted that the basic range interval for TRADEX is determined by a 150-MHz Range Clock. The least-significant bit of all range integers, in communication with BATS, is an integral multiple of $c/3 \times 10^8$ sec^{-1} where c is in meters/second. This is only approximately 1 m. Therefore, all ranges in BATS Requests and Replies are specified in units of TRADEX Range Counts (TRCs) rather than in meters, to avoid misunderstandings with true range. Range Rate is similarly designated. The ranges used in the Threat Assessment Software computations and in data interchange between computers are in meters. Consequently, the LSB of range integers in state vectors and the Sigma 5 messages are in true meters.

Designation Word 1 (see Fig. V-1)

T_o (0-31)

Time of Validity – (32 bits, LSB = 1 μsec, maximum value = 4295 sec) gives the (Astrodata) Radar Binary Clock reference time for the Acceptance Gate Start.

AGS Range (36-53)

Acceptance Gate Start Range – (18 bits, LSB = 8 TRCs, maximum value = 2,097,146 TRCs) specifies the range from ZRT to the opening of the acceptance window. Assumes

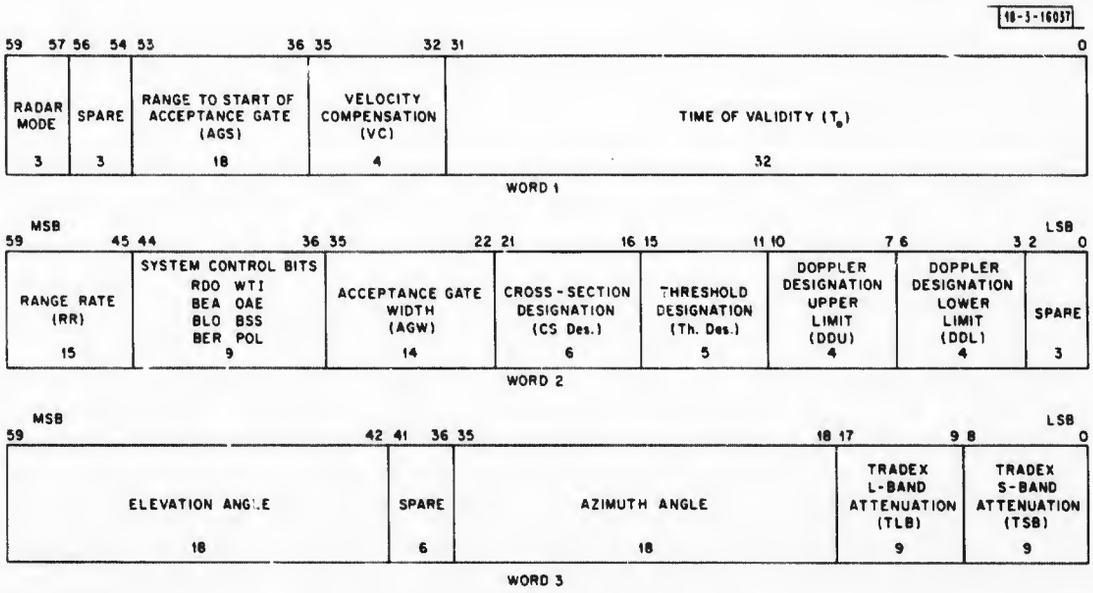


Fig. V-1. BATS input Designation Words.

that ZRT is coincident with T_o. When ZRT and T_o differ, the BSP will extrapolate the AGS Range by $(ZRT - T_o) \times RR$, where RR is the Range Rate specified by the user in Designation Word 2.

R-Mode (57-59)

Radar Mode – (3 bits)

Bit 59	Bit 58	Bit 57	S-Band	L-Band
0	0	0	Chirp	Chirp
0	0	1	Burst and chirp	Chirp
1	0	0	Chirp	LIDAR
1	0	1	Burst and chirp	LIDAR

VC (32-35)

Velocity Compensation – (4 bits) specifies the velocity compensation to the BSP angle error system. The compensation required is specified by the user after knowing which L-band waveform TRADEX is transmitting and the velocity of the target. Offset binary code is used where binary 1000 = 0-nsec delay.

Designation Word 2 (see Fig. V-1)

DDL (3-6)

Doppler Designation, Lower Limit – (4 bits) is used along with DDU to place a velocity window on the 16 velocity outputs of the S-band burst matched filter. The binary number is the filter number.

DDU (7-10)

Doppler Designation, Upper Limit – (4 bits) similar to DDL.

Th. Des. (11-15)

Threshold Designation – (5 bits, LSB = 1 dB) specifies the level above noise to set the detection threshold, thereby establishing a desired probability of detection and probability of false alarm. This level is combined with a sidelobe level, minimum cross section, wake threshold, STC, and noise measurement to form a Detection Threshold.

CS Des. (16-21)

Cross-Section Designation – (6 bits, LSB = 1 dB) specifies the minimum cross section of an acceptable target to the BSP Threshold Subsystem. The value sent to the BSP equals the desired cross-section threshold times the sensitivity of TRADEX-BSP in dB per dBsm at a range of 16,384 TRCs. The BSP will provide the R-fourth correction required for all other ranges up to 638,976 TRCs.

AGW (22-35)

Acceptance Gate Width – (14 bits, LSB = 8 TRCs, maximum value = 131,072 TRCs) specifies the width of the Acceptance Gate.

RDO (36-37)

Range Discriminator Override – (2 bits) specifies either centroid or leading-edge discriminator, or allows the BSP to choose for each target. In the automatic mode, the BSP chooses the centroid discriminator if the slope of the dynamic threshold is negative 200 nsec following the output of the leading-edge range discriminator. The leading-edge discriminator can only be used when the slope is positive:

Bits		
36	37	
1	0	Centroid only
0	1	Leading edge only
0	0	BSP decision
1	1	Not allowed

BER (38)

Burst Enable – (1 bit) Normally, S-band chirp video is supplied to the range discriminator. When this bit is set, the S-band burst video will be sent to the range discriminator.

BEA (39)

Burst Enable Amplitude Report – (1 bit) When this bit is set, the log-amplitude reported in the Target Word is the S-band burst amplitude rather than the S-band chirp amplitude.

BLO (40)

Burst Logic Override – (1 bit) When TRADEX is transmitting the Burst-Chirp Waveform, a coincidence of range marks of the burst and chirp must occur in order for a target to be reported to the target buffer. When this bit is set, the coincidence is no longer required.

OAE (41)

Off-Axis Enable – (1 bit) when enabled, will allow transfer of all target information stored in the BSP target buffer whether or not the targets were in the S-band beam. 0 = enable.

WTI (42)

Wake Threshold Inhibit – (1 bit) When this bit is set, it prevents the wake threshold signal from being combined with other threshold signals. (The signal is always available internally in the BSP for use in measuring an extended target and choosing the range discriminator.)

BSS (43)

Burst Sample Strobe – (1 bit) determines which range strobe, leading edge or centroid, is sent to the burst matched filter to sample the burst waveform:

0 = leading edge
1 = centroid

POL (44)

Polarization – (1 bit) indicates which polarization is connected to the angle error system:

0 = LC
1 = RC

RR (45-59)

Range Rate – (15 bits, LSB = 1 TRC/sec, maximum value = 16,384 TRCs/sec) used by the extrapolation rate control to reposition AGS Range, compensating for target motion between T_o and ZRT.

Designation Word 3 (see Fig. V-1)

TSB Atten. (0-8)

TRADEX S-Band Attenuation – (9 bits, LSB = 0.25 dB, maximum value = 72 dB) indicates the value of the S-band receiver attenuators.

TLB Atten. (9-17)

TRADEX L-Band Attenuation – (9 bits, LSB = 0.25 dB) indicates the value of the L-band receiver attenuators.

Az Angle (18-35)

Azimuth Angle – (18 bits, LSB = 2^{-18} rev or 0.023 mrad) azimuth angle of the TRADEX antenna. Presently not used by the BSP.

El Angle (42-59)

Elevation Angle – (18 bits, LSB = 2^{-18} rev or 0.023 mrad) elevation angle of the TRADEX antenna. Presently not used by the BSP.

Header Word 1 (see Fig. V-2)

TZRT (0-31)

Time of ZRT – (32 bits, LSB = 1 μsec, maximum value = 4295 sec) the value of the BSP Radar Binary Clock when the ZRT is received from TRADEX.

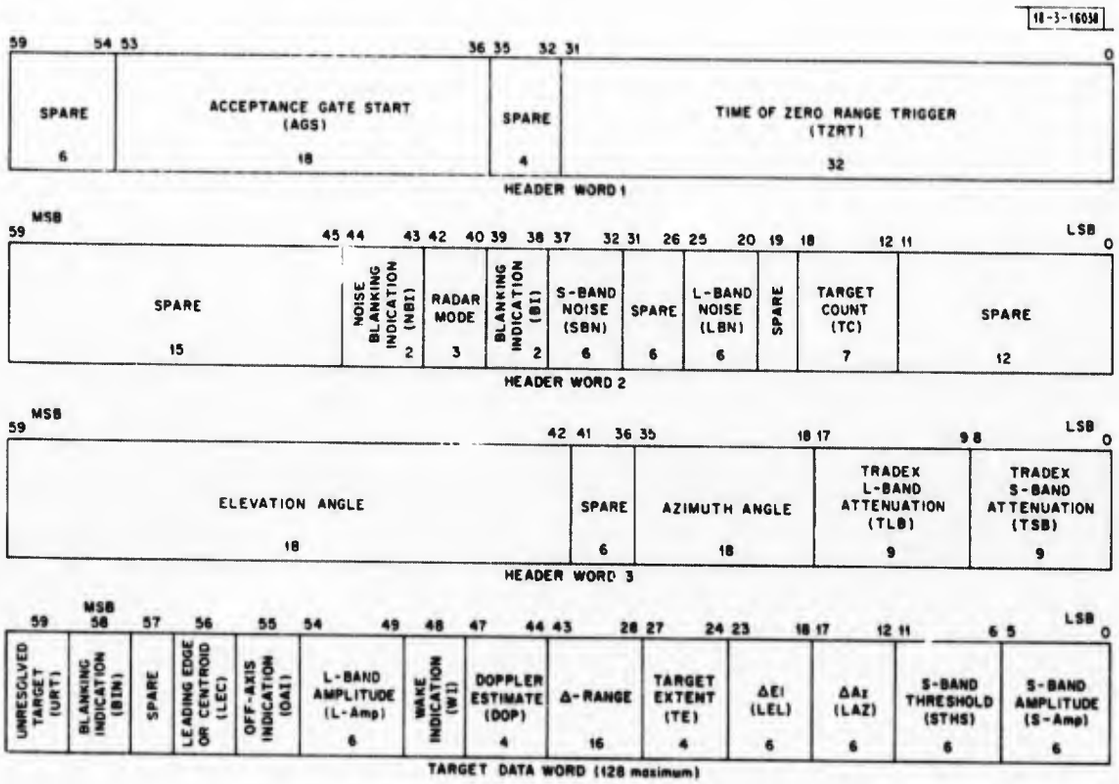


Fig. V-2. BATS data output format.

AGS Range (36-53)

Acceptance Gate Start Range – (18 bits, LSB = 8 TRCs, maximum value = 2,097,146 TRCs) range from ZRT to the opening of the acceptance gate. It will differ from AGS Range given in Designation Word 1 by (ZRT – T_o) × Rate Range.

Header Word 2 (see Fig. V-2)

TC (12-18)

Target Count – (7 bits) a binary number representing the number of Target Words stored in the BSP target buffer.

LBN (20-25)

L-Band Noise – (6 bits, LSB = 1 dB) L-band noise integrated over the noise gate. (It is possible that a TRADEX blanking gate could overlap the noise gate and give an incorrect noise measurement. This condition is indicated by setting of Status Bit 6 and NBI bits.)

SBN (32-37)

S-Band Noise – (6 bits, LSB = 0.5 dB) same as LBN except for S-band.

BI (38-39)

Blanking Indication – (2 bits) indicates if TRADEX blanking gate is overlapping the acceptance gate:

Bits		
38	39	
0	0	No blanking interference
0	1	The blanking gate is up when the acceptance gate opens
1	0	The blanking gate is up when the acceptance gate closes
1	1	The blanking gate is up when the acceptance gate opens and closes

R-Mode (40-42)

Radar Mode – (3 bits) same as in Designation Word 2.

NBI (43-44)

Noise Blanking Indication – (2 bits) same meaning as BI except that the TRADEX blanking gate is overlapping the noise measurement gate preceding the acceptance gate. Status Bit 6 is set if there is any overlap of the noise and blanking gates.

Header Word 3 (see Fig. V-2)

Same as Designation Word 3 and is returned to the CDC 6600 unchanged.

Target Data Word (see Fig. V-2)

S-Amp (0-5)

S-Band Amplitude – (6 bits, LSB = 1.2 dB) S-band amplitude sampled by a range strobe. The amplitude reported is the S-band log-video that is specified in Designation Word 2 with BEA. Normal operation is S-band chirp amplitude. Amplitude is in complemented form (maximum amplitude is all zeros).

STHS (6-11)

S-Band Detection Threshold – (6 bits, LSB = 1 dB) detection threshold sampled by the range strobe at the same moment amplitude is sampled. The dynamic (wake) threshold is not included in the sample.

LAz (12-17)

L-Band Azimuth Error – (6 bits, LSB = 0.2 mrad) range strobe generated by the S-band waveform is corrected and is used to sample the signals in the L-band Angle Error Subsystem. The value reported here is the sampled value of the angle error detector.

LEl (18-23)

L-Band Elevation Error – (6 bits, LSB = 0.2 mrad) same as above except elevation angle.

TE (24-27)

Target Extent – (4 bits, LSB = 32 TRCs) indicates the range interval that the wake threshold remains above the noise and sidelobe thresholds.

Δ-Range (28-43)

Target Range – (16 bits, LSB = 2 TRCs, maximum value = 131,072 TRCs) The range is measured from the AGS given in Header Word 1 to the range mark generated by the range discriminator.

DOP (44-47)

Doppler Estimate – (4 bits) This binary number is the filter number in the velocity window (specified by DDU and DDL) that has the greatest output at the time of the sample pulse.

WI (48)

Wake Indication – (1 bit) If the three low-velocity channels of the burst matched filter have outputs which exceed a threshold shortly (0.3 μsec) after a target is reported from the higher velocity channels, this bit is set.

L-Amp (49-54)

L-Band Amplitude – (6 bits, LSB = 1 dB) L-band target amplitude reported at the time of the corrected S-band sample pulse.

OAI (55)

Off-Axis Indication – (1 bit) indicates that the target reported is outside the S-band beamwidth (6 dB).

LEC (56)

Leading Edge or Centroid – (1 bit) indicates which range discriminator was used to obtain the information contained in a particular Target Word:

0 = Leading edge
1 = Centroid

BIN (58)

Blanking Indication – (1 bit) If this bit is set, the Δ-Range in the corresponding Target Word marks the transition from either state to the other of the TRADEX blanking gate.

URT (59)

Unresolved Target – (1 bit) indicates if the BSP has detected more than one target at S-band that will be unresolved in range by the L-band chirp. L-band data may not be valid when this bit is set.

4. Control Keys

a. RTI Channel 0 Control Keys

Control Key 000	Normal Mission Mode. The three Designation Words are transferred to the BSP using this key.
Control Key 001	Operational Control Word Transfer. The one-word data transfer is loaded into the Operational Control Word register. This key is usually followed by Key 010 for the word transfers.
Control Key 010	Data Word Transfer following Control Key 001. The number of word transfers is established by the Operational Control Word.
Control Key 100	RTI to Minicomputer. Used with Computer Mode G to write data into the minicomputer.
Control Key 110	Transfer ATG Control Words (13) for test or calibration. Used with Computer Mode J.
Control Key 111	BSP Master Clear. No data are transferred.

b. RTI Channel 1 Control Keys

Control Key 000	Normal Mission Mode. The BSP outputs the three Header Words and up to 128 Target Words.
Control Key 001	Read Status Register. (Once read, the Status Register is reset.)
Control Key 011	Loop Test. Used with Computer Mode B for loop test.
Control Key 100	RTI from Minicomputer. Used with Computer Mode H to read data from the minicomputer.

c. Input Control Keys (from Simulator Controller)

Control Key 000	Data transfers from Simulator Controller take place under this control key to the target buffer and header registers.
Control Key 001	A data transfer is made to the Status Register.
Control Key 111	This causes a clearing of the control sequence logic within BATS. No data transfer will accompany a SELECT with this control key.

5. Status Word

A status bit is set in the Status Word when malfunction of the BSP is detected. The bits have the following significance and can be masked in groups (to prevent a RTI Interrupt Request) as specified in the Operational Control Word. The Status Word is read by selecting the BSP on RTI Channel 1 with Control Key 001. Once read, the Status Register is reset.

Group	Bit	
0	0	= Target buffer data incomplete
	1	= Target buffer overflow
	2	
	3	
1	4	= Stale Time of Validity (T_o)
	5	= Data request does not equal TRADEX mode
	6	= Blanking gate overlaps noise gate
	7	
2	8	= Incorrect RTI Channel 0 control key
	9	= Illegal sequence
	10	= EOM not received on RTI Channel 0
	11	= Incorrect RTI Channel 1 control key
3	12	= Illegal minicomputer Begin/End line drop (transmit)
	13	= Incorrect minicomputer read response
	14	= Illegal minicomputer Begin/End line drop (receive)
	15	= Incorrect minicomputer write response
4	16	= L-Band dropped pulse
	17	= S-Band dropped pulse
	18	= L-Band unscheduled dropped pulse
	19	= S-Band unscheduled dropped pulse
5	20	
	21	
	22	
	23	
6	24	
	25	
	26	
	27	
7	28	= ATG Status 1
	29	= ATG Status 2
	30	
	31	

6. Master Clear Function

A Master Clear to BATS resets all control logic, enabling BATS to accept a new request; but a Master Clear does not change the mode of BATS operation nor does it clear BATS memory or reset the BATS Radar Binary Counter. When connected to the RTI, the Master Clear operation for BATS may be initiated in any of three ways. First, the Channel 0 or 1 RTI Master Clear lines may be used. BATS and all other equipment connected to the RTI are affected. Secondly, when BATS is selected on Channel 0 with Control Key 111 the Master Clear for BATS only is initiated. Thirdly, when in Simulation Mode, selection of BATS by the SimController with Control Key 111 will initiate a Master Clear. No BATS Master Clear function is provided via RTI Channel 1.

The Master Clear function halts the execution of any operation that may have been in process at the time of occurrence of the Master Clear signal. It resets all channel select flip-flops, sets the memory control flip-flop to enable the write control logic, and resets the memory address counter to its normal starting position. It also resets the interrupt level to the RTI, and sets the BATS control logic to a condition to accept new data requests or mode selection commands from the RTI or from the BATS control panel, as appropriate.

A Master Clear command should be issued prior to the start of any new D&DE computer program. It may also be commanded at any other time as required by the program, or manually by the operator. A Master Clear push button on the BATS Control Panel enables manual generation of the Master Clear signal when in Local Operation. In addition, the Master Clear signal is generated when BATS prime power is applied, so that BATS comes on in the cleared condition.

7. Miscellaneous RTI Controls

BATS External Device Select Code	011
BATS External Device Status Code	000 (BSP on-line)
	011 (BSP local mode)
BSP RTI Interrupt Request Number	11

D. MINICOMPUTER INTERFACE

Nova Minicomputer-to-BATS Command Word (CW) (see Fig. V-3):– This 16-bit command word sets up BATS DSS to accept control by the minicomputer. The fields in the words are reversed as shown in parentheses, in going from the minicomputer to the BATS DSS.

BOK — Bits 1 (14) through 3 (12) define simulated BATS Output Keys from RTI Channel 1 where:

Bits	Control Key Bit No.
1 (14)	3
2 (13)	2
3 (12)	1

IECS — Bit 7 (8) specifies internal 150/10-MHz clock to be used in the RDSS when equal to a logic 0. A logic 1 specifies using the TRADEX 150/10-MHz clock.

ACI — Bit 8 (7) specifies an inhibit of the control outputs to the analog equipment (except the ATG and High Speed Logic in RDSS) when equal to a logic 1. Logic 0 is no-inhibit.

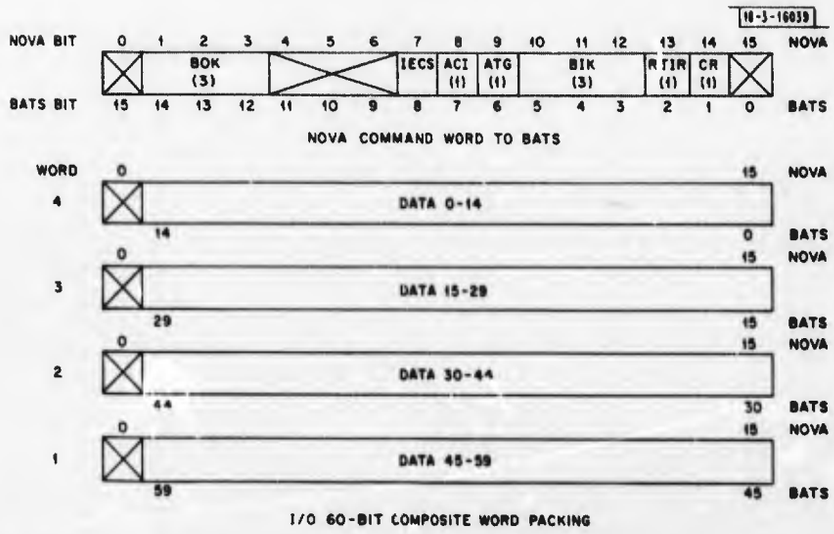


Fig. V-3. Nova minicomputer to BATS command word (CW) format.

ATG — Bit 9 (6) specifies that the data on Channel 25 (input channels) will be directed to the ATG.

BIK — Bits 10 (5) through 12 (3) define simulated BATS Input Keys from the RTI Channel 0 where:

Bits	Control Key Bit No.
10 (5)	3
11 (4)	2
12 (3)	1

RTIR — Bit 13 (2) specifies that a simulated RTI Reset occur.

CR — Bit 14 (1) specifies that a simulated RTI Reset occur at the dropping of the simulated acceptance window under a test condition. No data will be returned to the Nova minicomputer. The continuous-run cycle will cause the BATS to cycle on the same control data until this bit is reset by the Nova computer.

E. ANALOG TEST GENERATOR WORD FORMATS

The formats and definitions of the 13 words sent to the ATG from the minicomputer are summarized in Fig. V-4.

F. SUMMARY OF BATS PHOTORECORDER INTERFACE SIGNALS

1. Analog

All analog outputs are 93-ohm impedance levels and are to be terminated at the BATS cabinet when not in use. They are on individual BNC coax connectors.

1. Log – S: "S-Band Chirp/Photo-Record"
   Threshold Cabinet 4, J911
   +2500-mV peak at cabinet output
2. Log – Burst: None provided

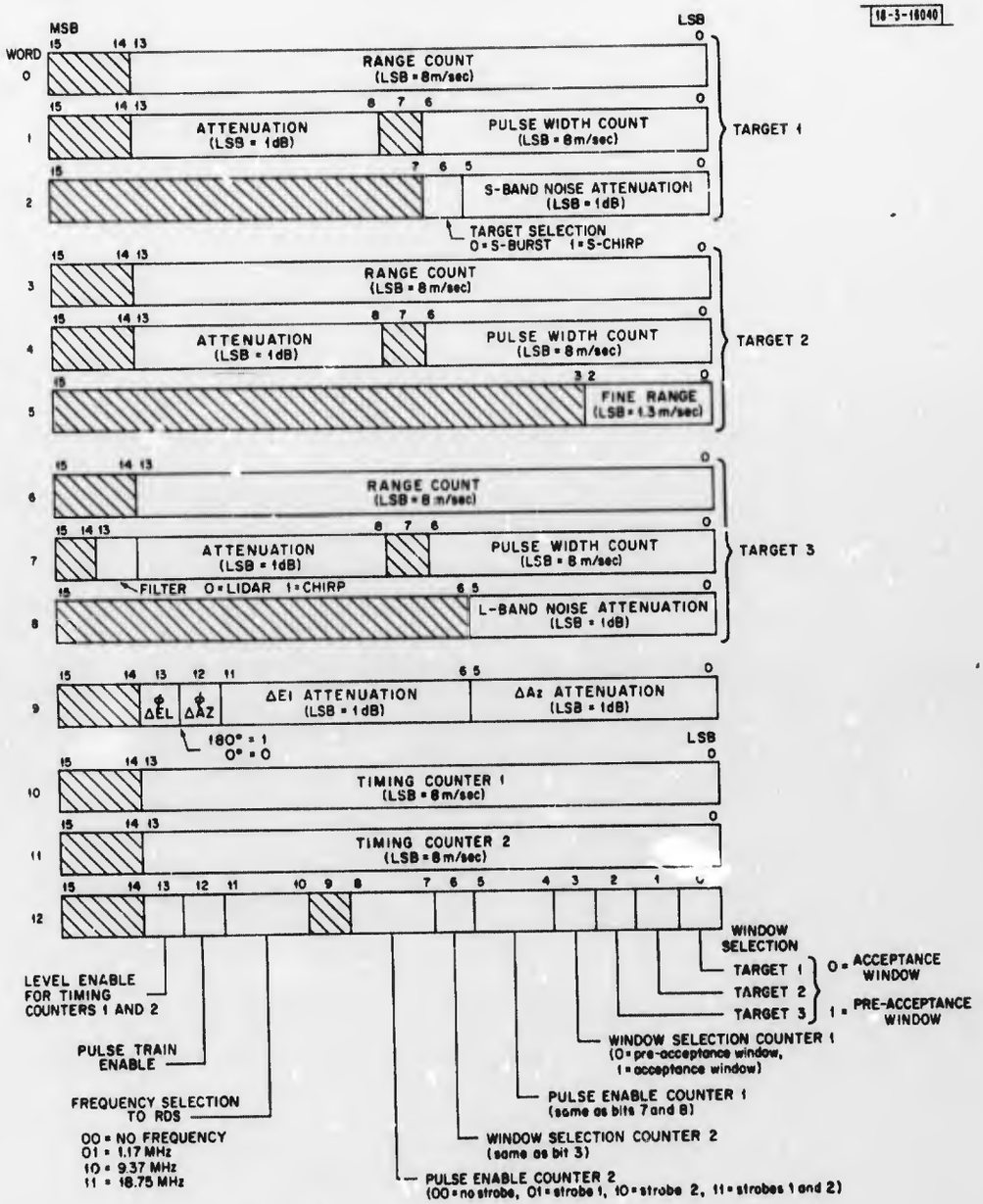


Fig. V-4. ATG word formats.

3. Threshold: "Slow Threshold"
   Threshold Cabinet 4, J909
   +2048-mV peak at cabinet output

4. "Log L Sum"
   Cabinet 1A1, J907
   +2500-mV peak at cabinet output

5. "Δ EL"
   Cabinet 1A2, J907
   ±1200-mV peak at cabinet output

6. "Δ ΛZ"
   Cabinet 1A2, J905
   ±1200-mV peak at cabinet output

7. Threshold: "Composite Threshold"
   Cabinet 4, J907
   +2048-mV peak at cabinet output

2. Digital

All signals appear on an 18-pin connector similar to the one used for TRADEX mode lines: terminating impedance = 100 ohms returned to +4.5 V; and signal level = 3.7 ± 1.0 to 0 + 0.45/−0 V.

Digital Cabinet Outputs (2J30)

1	Acceptance window gate	Pin 1
2	Acceptahce window start strobe	Pin 2
3	ZRT strobe	Pin 3
4	Dump gate start strobe (−49.5 μsec from leading edge of acceptance window gate)	Pin 4