MILLIMETER WAVE PHASE SHIFTER

Gary G. Weidner, et al

RCA Advanced Technology Laboratories
Camden, New Jersey

June 1973

AD

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MILLIMETER WAVE PHASE SHIFTER

FINAL REPORT

By
G. G. Weidner
B. J. Levin

June 1973

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13. ABSTRACT

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Among the tasks requiring study were 1) propagation analysis for the diode-loaded waveguide to determine the relevant parameters, 2) fabricating and evaluating the distributed PIN diodes, and 3) forming a phase shifter using these diodes. Computed and measured data are presented for waveguides loaded with silicon slabs of various conductivities and for distributed PIN diodes.

This work has demonstrated the potential feasibility of the distributed PIN phase shifter.

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For

U. S. ARMY ELECTRONICS COMMAND, FORT MONMOUTH, NEW JERSEY

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FOREWORD

This research was supported by the Advanced Research Projects Agency of the Department of Defense and was monitored by the U. S. Army Electronics Command under contract DAAB07-72-C-0168 (ARPA order 2099). ECOM technical representatives were Dr. H. Jacobs and Mr. M. Chrepta.

In addition to the authors, other significant contributors to the work reported here were J. J. Rudnick, supervision; K. C. Hudson and J. Mitchell, diode fabrication; A. S. Panebianco and H. A. Walter, technicians; L. D. Moore, mechanical fabrication; and C. Riggi, computer programming.

In the work reported here, no research and development effort was expended toward the improvement or creation of electronic components or material other than contracted for.

This final report covers work conducted from 1 April 1972 to 31 December 1972, and was submitted 23 March 1973.

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INTRODUCTION

The primary objective of this program was to develop and demonstrate feasibility of a laboratory model 140-GHz phase shifter. The significance of such a development is that the availability in some practical form of an electronically controllable phase shifter would make possible the construction of a phased array type of antenna, thereby providing rapid electronic scanning of the antenna beam. One of the attractive features of millimeter wavelength radiation is that it can be focused to a quite narrow beamwidth by a relatively small antenna. The high resolution (for a non-optical system) and small size of such an antenna point to applications where portable or airborne equipment is required for meteorology, surveillance, secure communications, high-resolution (by microwave standards) imaging, and tracking or weapon delivery.

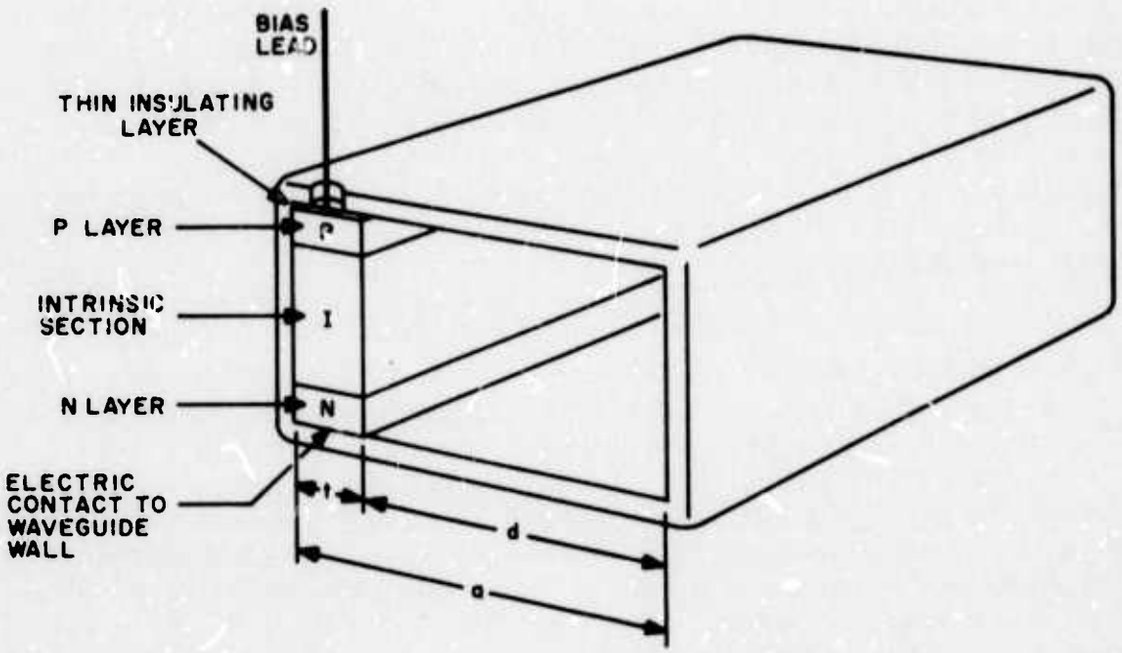
The approach taken here to millimeter wave phase shifting is a technique in which the desired variation in phase shift is produced by electronic modulation of the width of a rectangular waveguide, which results in a change in the phase shift per unit length along the waveguide. The change in effective width of the waveguide is accomplished by means of a PIN diode that is literally distributed along a sidewall of the waveguide as shown in Fig. 1. With no bias applied to the diode, the transmission line is a rectangular waveguide of width a, loaded with a dielectric slab of width t. Application of a suitable bias signal causes injection of free charge carriers into the I region of the diode in sufficient density that its millimeter wave conductivity is raised to a high value, thereby moving the effective waveguide wall to the free surface of the diode and changing the width of the waveguide to d in Fig. 1. The result is a change in the waveguide propagation constant and therefore a change in phase shift per unit length relative to the unbiased condition.

Among the problems requiring study were propagation analysis for the diode-loaded waveguide to determine the relevant parameters, fabrication techniques for use and evaluation of the distributed PIN diodes, and forming of a phase shifter using these diodes.

The program performance goals for the phase shifter were as follows:

Frequency	140 GHz	Power handling capability	1 W, CW
Phase shift	100°/cm	Drive power	10 mW
Insertion loss	0.5 dB/cm	Modulation rate	1 kHz

Although development did not progress to this point, no fundamental problems were found in the proposed phase shifting scheme. Indeed, the technique was shown to be valid, and indications are that the above listed numbers are realistic.



Note: The diode is insulated from the waveguide walls except for its lower terminal.

Fig. 1. Phase shifter geometry.

Section II

DEVICE PROPAGATION CHARACTERISTICS

A. LOADED WAVEGUIDE PROPAGATION ANALYSIS

1. Introduction

In the distributed PIN diode phase shifter, the diode has the effect of a semiconductive slab loaded in a section of rectangular waveguide. In order to obtain a good understanding of the device operation, a theoretical analysis of the propagation in loaded waveguides was undertaken. The initial results of this analysis have been presented in an RCA internal report.[1] In this section we present an extended version of that analysis and remove some of its limitations.

The generalized slab-loaded waveguide considered here is shown in Fig. 2. Each of the regions is assumed to be uniform and homogeneous, with dielectric constant ϵ_i and conductivity σ_i. The previously reported analysis is a special case of the geometry of Fig. 2. There, region 1 was the semiconductor slab and regions 2 and 3 were free space, as shown in Fig. 3. In that analysis the phase shift of the device was found to increase considerably with increases in slab thickness up to a certain critical thickness. Beyond the critical thickness the analysis essentially broke down. For these thick slabs (thickness greater than a quarter wavelength in the slab) it appears that the dominant mode electric field becomes concentrated in the semiconductor portion of the waveguide and decays exponentially in the unloaded section. For slabs under a quarter wavelength thick, the electric field dependence is sinusoidal both in the loaded and unloaded sections of the waveguide. The present analysis yields the propagation constant both for the thinner and thicker slabs. However, there is a definite discontinuity in performance at a thickness greater than a quarter wavelength, with the thinner slabs yielding improved phase shift/insertion loss ratios.

In addition to treating the thicker slab, the present analysis has also yielded results for other slab geometries. This includes a semiconductor slab mounted off the narrow wall, with both an air and dielectric backing. Also treated is the case of two semiconductor slabs symmetrically mounted on the two narrow walls of the waveguide.

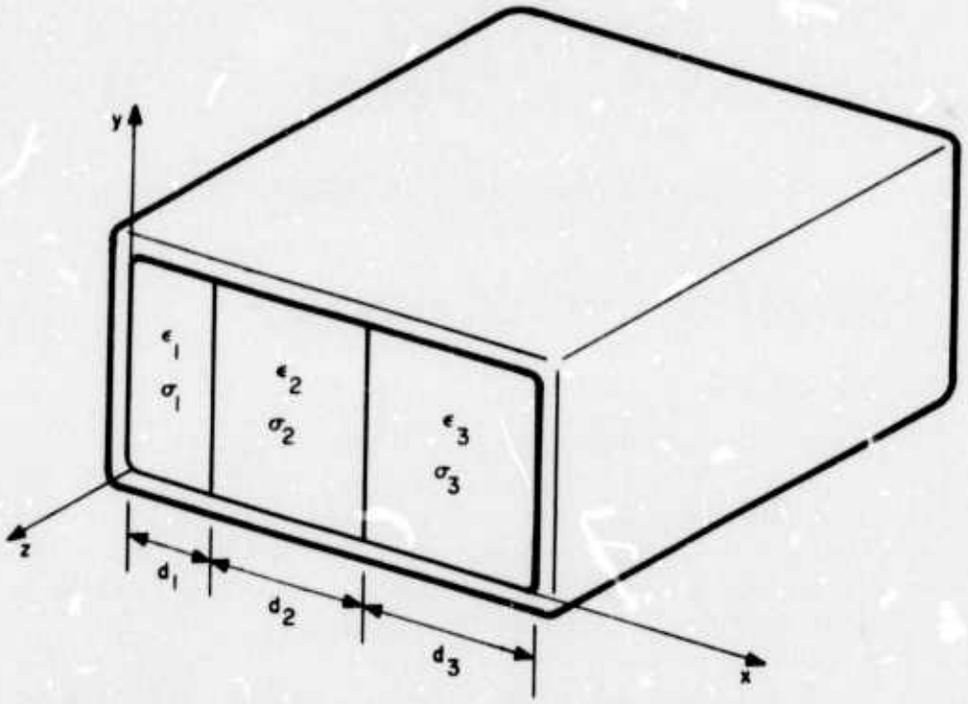


Fig. 2. Multiple slab waveguide geometry.

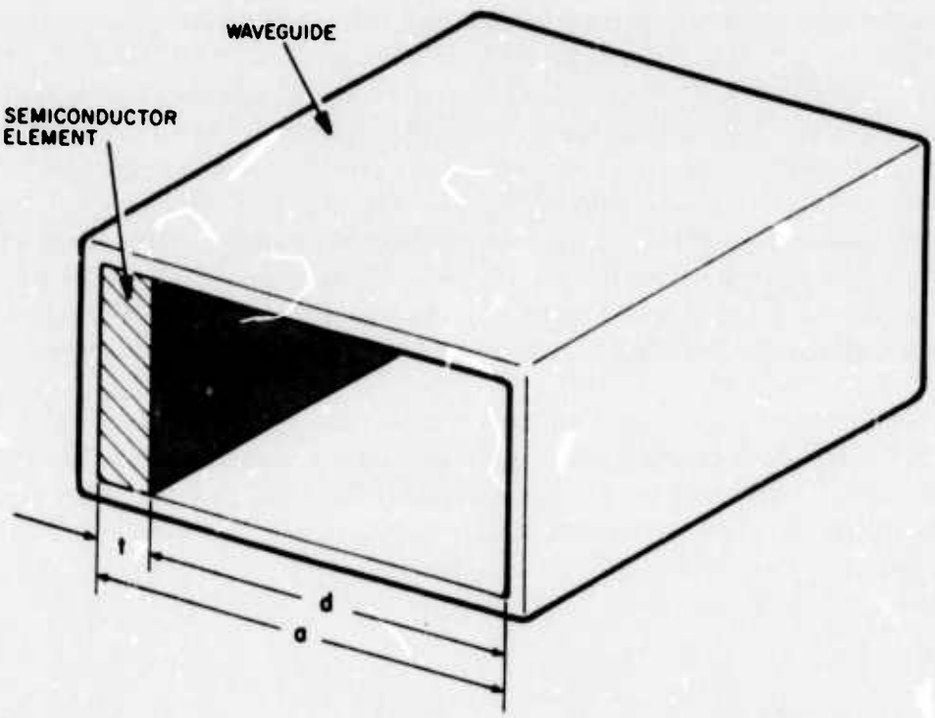


Fig. 3. Single slab on waveguide sidewall.

2. Theoretieal Analysis

In studying wave propagation in hollow eonducting waveguides, it is common to elassify the solutions into two types:

1) Waves that contain eleetric field but no magnetic field in the direetion of propagation. Since the magnetic field lies in the transverse plane, the waves are referred to as transverse magnetic (TM) waves.

2) Waves that contain magnetic field but no electrie field in the direction of propagation. Sinee the electrie field lies in the transverse plane, these waves are referred to as transverse eleetric (TE) waves.

The above is not the only way in whieh the possible wave solutions may be divided, but it is a useful way in that any general field distribution excited in an ideal waveguide may be divided into a number (possibly an infinite number) of the above types with suitable amplitudes and phases. Of eourse, only one of the possibly infinite number may propagate if it alone is excited and if conditions are favorable for its propagation.

The normal modes of propagation for a waveguide loaded with a dielectric slab are not, in general, TE or TM modes, but a combination of a TE and a TM mode. However, the normal modes are either transverse electric or transverse magnetic with respect to the slab boundary planes. This is due to the fact that normal to the slab boundary the "guide" appears uniform, with the narrow walls acting as a short circuit load. The field components are, in this case, derived from a single vector potential which is directed normal to the slab boundary plane. The resultant fields are either transverse electric or transverse magnetic to the interface normal. For the former the electric field lies in the longitudinal interface plane, and the mode is referred to as a longitudinal-seetion electrie (LSE) mode. For the latter the magnetie field lies in the longitudinal interfaee plane, and the mode is referred to as a longitudinal-seetion magnetie (LSM) mode. A speeial case of the LSE mode is the TE_{no} of rectangular waveguide. These modes are the natural modes for the geometry of Figs. 2 and 3, both because of the slab orientation and also because the fields will be launehed by a TE_{10} wave in empty waveguide. The characteristic equation for the propagation eonstant in a uniformly slab-loaded waveguide is transcendental, but ean be solved by numerical techniques.

Propagation equations for the slab-loaded waveguide are developed by Collin[2] for lossless dieleetries. These expressions can be modified for the lossy case by replacing the (real) dielectric eonstant by a complex one that takes the conduetivity of the slab into aeeount. For the LSE mode the fields ean be derived from a magnetic Hertzian potential of the form

$$\hat{\Pi} = \hat{a}_x \Psi (x,y) e^{-\gamma z}$$

where $\hat{a}_x$ is a unit vector normal to the slab-air interface. The electric and magnetic fields are then given by:

$$\hat{E} = j\omega\mu_o \nabla x \hat{\Pi} \tag{1}$$

$$\hat{H} = \nabla x \nabla x \hat{\Pi} \tag{2}$$

Propagation along the guide is given above by the exponential factor $e^{-\gamma z}$ and must be the same in the loaded and unloaded portions of the waveguide if the boundary conditions at the interfaces are to be satisfied for all arbitrary values of z. Here, $\gamma = \alpha + j\beta$ is the complex propagation constant for the composite waveguide structure. Its real part, α, is the attenuation per unit length, while its imaginary part, β, is the phase shift per unit length. These quantities, actually their ratio β/α, are useful in describing the phase shifter performance.

Consider a single semiconductor slab mounted on the narrow waveguide wall as shown in Fig. 3. Applying the boundary conditions that the fields are continuous across the interface and that the tangential component of the electric field vanishes on the perfectly conducting guide walls yields the following:

$$h \tan(\ell t) = -\ell \tan(hd) \tag{3}$$

and

$$\gamma^2 = \ell^2 - k k_o^2 = h^2 - k_o^2 \tag{4}$$

where

$$k_o^2 = \omega^2 \mu_o \epsilon_o$$

and

$$k = \epsilon_r - j(\sigma/\omega\epsilon_o)$$

In Eqs. 3 and 4 h and ℓ are the transverse (in the x direction) wave numbers. They are the two unknowns in these equations.

Combining Eqs. 3 and 4 yields the following transcendental equation in the propagation constant γ:

$$0 = f(\gamma) = \left(\gamma^2 + k_o^2\right)^{1/2} \tan\left[\left(\gamma^2 + k k_o^2\right)^{1/2} t\right] + \left(\gamma^2 + k k_o^2\right)^{1/2} \tan\left[\left(\gamma^2 + k_o^2\right)^{1/2} d\right] \tag{5}$$

Initially, the roots of Eq. 5 were obtained by using a combined Rayleigh-Ritz Newton-Raphson iteration technique.[1,2] This method was found limited in its application and has been superseded by use of a root-search algorithm. The computer programs for the latter approach are given in Appendix A.

In the root-search method of solution we first set $\sigma = 0$ and find all the values of γ (α and β) that make $f(\gamma) = 0$. Program ROOT of the Appendix is used for this initial search. Next σ is increased from zero to a small value, 0.1 $(\text{ohm-m})^{-1}$, and the accurate root for $\sigma = 0$ is used as the "first guess" for the root of Eq. 5 for the new value of σ. The new root is determined to the required accuracy by incrementally searching the α-β plane in the neighborhood of the "first guess" point. This process is continued until σ reaches a high value, 10^5 $(\text{ohm-m})^{-1}$, and then repeated for various slab thicknesses. The search for non-zero values of σ is accomplished by Program WAVE in the Appendix.

The root-search method used in the computer analysis is a modified version of the method of steepest descent. The fact that γ is a complex quantity for non-zero values of slab conductivity leads to a two-dimensional search. The technique used was to step both α and β in both the positive and negative directions and move in the direction that minimized $f(\gamma)$ in Eq. 5. When the current step size did not lead to a smaller value of the function, the step size was decreased by a factor of ten. This was continued for five iterations, the initial step size in α and β being 1.0 and the final step size being 0.0001. In the computer analysis the units of α are nepers/meter while those of β are radians/meter. Thus, in these units, the values of α and β are accurate to the fourth decimal place.

For $\sigma = 0$ the system is lossless and the propagation constant is purely imaginary, $\gamma = j\beta$. The values of β that cause $f(j\beta)$ of Eq. 5 to equal zero are shown in Fig. 4 as a function of relative slab thickness. As stated previously these values of β were generated by Program ROOT. The geometry is that given in Fig. 3, at a frequency of 140 GHz in standard RG-138/U waveguide. The branch in Fig. 4 marked "dominant mode" is an extension of the TE_{10} mode in unloaded waveguide (i.e., t/a=0). The branch marked "$\beta = k_o$" is a trivial root of $f(j\beta)$. However, the point where the dominant mode crosses this horizontal line corresponds to a slab thickness of one-quarter wavelength in the dielectric. It will be shown below that this is a critical thickness in terms of phase shifter performance.

Consider the trivial roots $\beta = k_o$. From Eq. 4 it can be seen that for $\beta < k_o$, both h and ℓ will be real; while for $k_o < \beta < \sqrt{\epsilon_r}\, k_o$ h will be imaginary and ℓ will be real. The wave numbers ℓ and h give the "x" dependence of the fields in the semiconductor slab and air portions of the waveguide, respectively. A real wave number corresponds to a sinusoidal dependence, whereas an imaginary wave number corresponds to a hyperbolic or exponential dependence. Thus below the "$\beta = k_o$" line the dominant mode has sinusoidal field dependence in both regions of the guide; while above this line the sinusoidal dependence is still maintained in the slab; however, the fact that h is imaginary leads

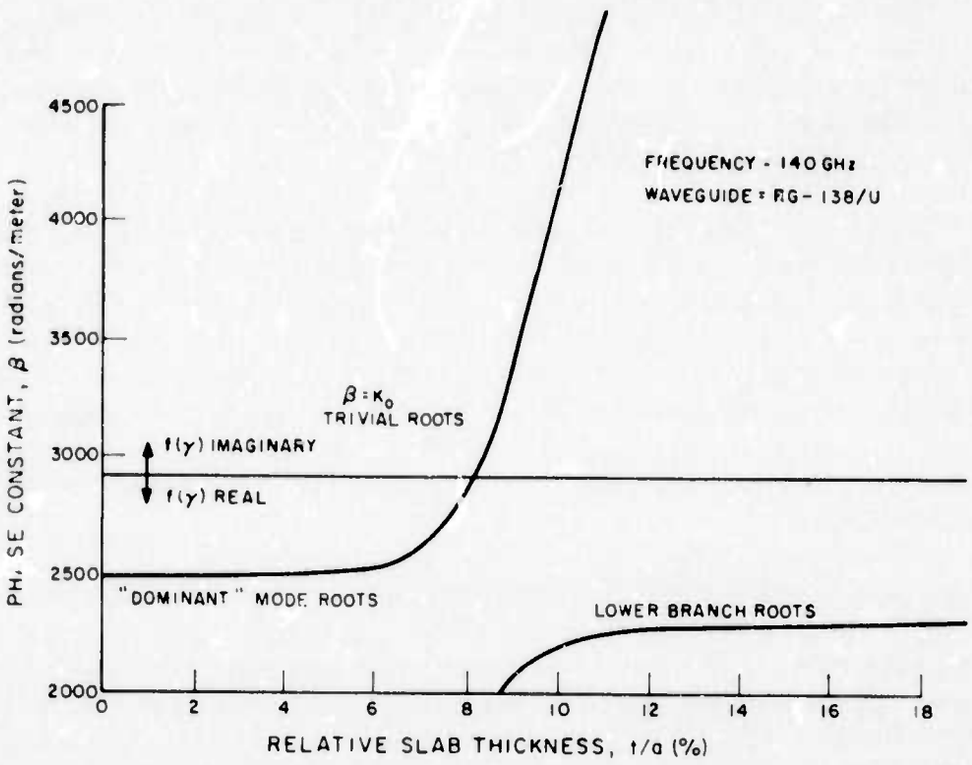


Fig. 4. Phase constant β for $\sigma = o$ in the geometry of Fig. 3, as a function of slab thickness.

to an exponential decay in the air region. This results in a surface type wave encountered in microstrip circuits where the fields are concentrated in the dielectric and decay exponentially away from its surface.[3]

3. Analytical Results

Using the various roots in Fig. 4 as a starting point, Eq. 5 was solved to obtain values of $\gamma = \alpha + j\beta$ for the case of non-zero conductivity. Initially the geometry shown in Fig. 3 was treated. The more general geometry at Fig. 2 will be discussed in Sec. II.A.4.

Typical computer-generated results are shown in Figs. 5 and 6 for a range of slab thicknesses. Here the real (attenuation) and imaginary (phase shift) parts of the propagation constant are plotted as a function of the slab conductivity with slab thickness as a parameter. Initially a relative dielectric of 12 was used; later results are for $\epsilon_r = 11.7$, which is more representative of silicon. (This change does not affect the results significantly.) In these curves the reference for phase shift is taken to be the zero conductivity slab. The insertion phase shift for a section of waveguide

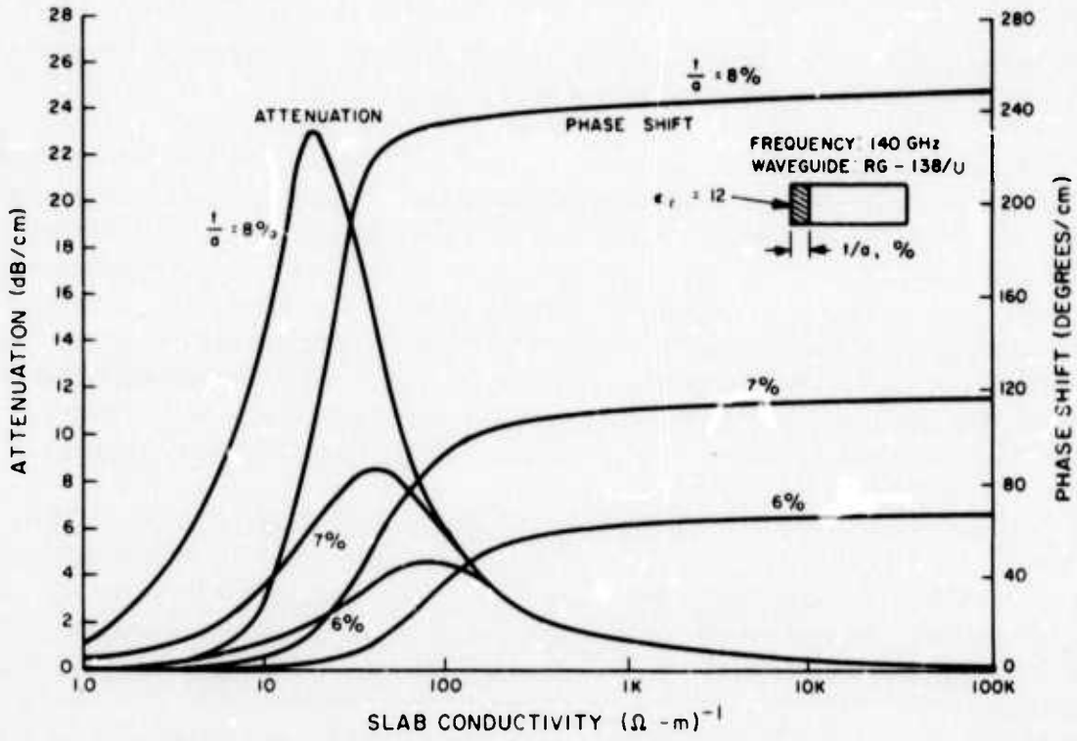


Fig. 5. Phase shift and attenuation for single slab on waveguide sidewall at 140 GHz.

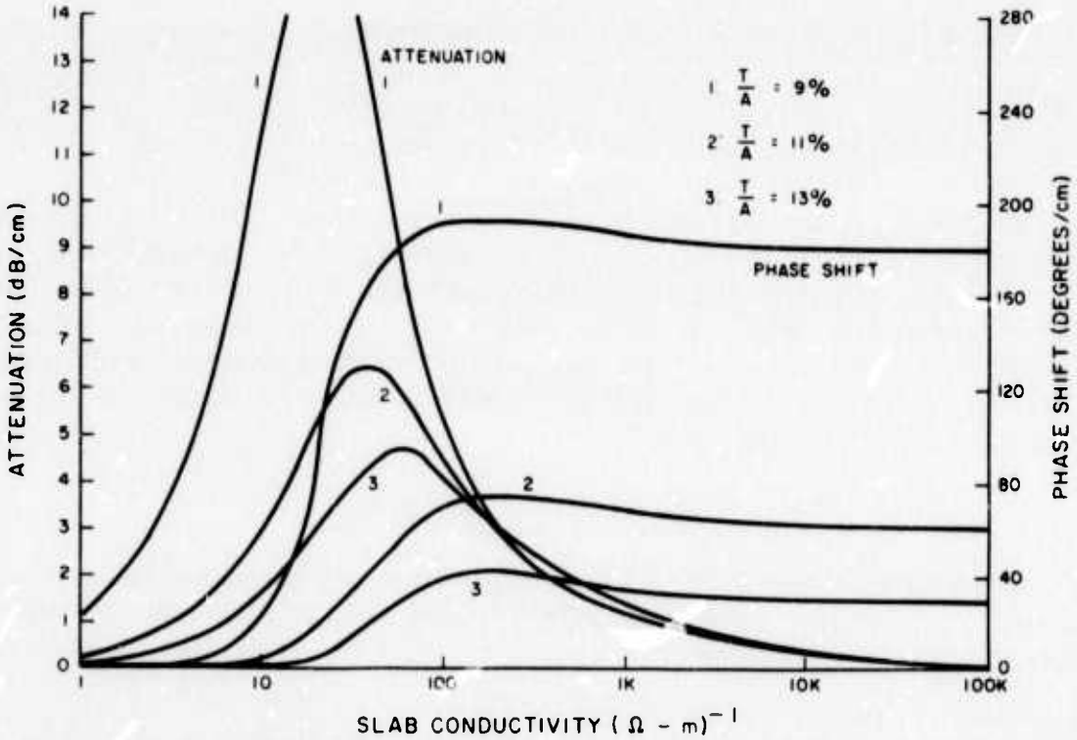


Fig. 6. Phase shift and attenuation for single slab on waveguide sidewall at 140 GHz.

is quite large (360° per guide wavelength, about 0.1 inch). For the zero conductivity slab-loaded waveguide the insertion phase shift is given in Fig. 4.*

Examination of the corresponding curves in Figs. 5 and 6 leads one to suspect that a relationship exists between α and β. The facts that the real part peaks at the point where the imaginary part goes through a point of inflection, and that the general shapes of the curves, are suggestive of the transform relationship that exists between the real and imaginary parts of various physical functions.[4,5] However, on closer examination of the curves, it appears that α and β are not related by the Hilbert transform relationship found in electrical network analysis. This appears to be due to the fact that the slab-loaded waveguide is not a minimum phase shift network. Further effort is needed to determine the relationship, if any, between α and β.

With reference to Fig. 4, the results in both Figs. 5 and 6 correspond to initial values of β less than k_o, the former on the dominant mode braneh and the latter on the lower branch. As indieated in the graphs, the eases where $\beta < k_o$ yields useful phase shift/attenuation characteristics, while for $\beta > k_o$ the attenuation and the phase shift inerease exponentially with slab conductivity. These results agree with the above postulation that the millimeter wave fields are concentrated mainly in the semiconductor slab when $\beta > k_o$, with the fields being highly attenuated as the slab becomes more lossy. The eleétrie and magnetie field distributions in a dielectric (ferrite) slab-loaded waveguide have been presented by Lax and Button.[6] There it is also shown that the fields become concentrated in the slab as its thickness is inereased.

The device performance was evaluated at a number of frequencies in the 90-140 GHz band. Figure 7 shows the dominant mode phase shift and attenuation for $\beta < k_o$ at 90 GHz, whereas Fig. 8 shows the maximum (saturated) value of phase shift over the 90 GHz to 140 GHz band for various slab thicknesses.

All of the analytical results presented above have been for standard 80-mil-wide RG-138/U waveguide. In Fig. 9 the phase shift and attenuation are plotted for a 4.8-mil-thiek slab for two different waveguide widths (70 mils and 90 mils). These should be compared to the t/a = 6 percent data of Fig. 5. In general it ean be seen that the phase shift and attenuation increase with deerease in waveguide width. Thus, over a limited range, the waveguide width provides a convenient parameter for adjusting phase shift and attenuation.

4. Analytical Results for Additional Slab Geometries

The analytical results have been extended to a number of interesting slab geometries. Among them are a semiconductive slab mounted off the narrow wall of the waveguide (with and without a dielectric spaeer between the slab and the wall)

*The conversion from radians/meter to degrees/cm is multiplieation by a factor of 0.573.

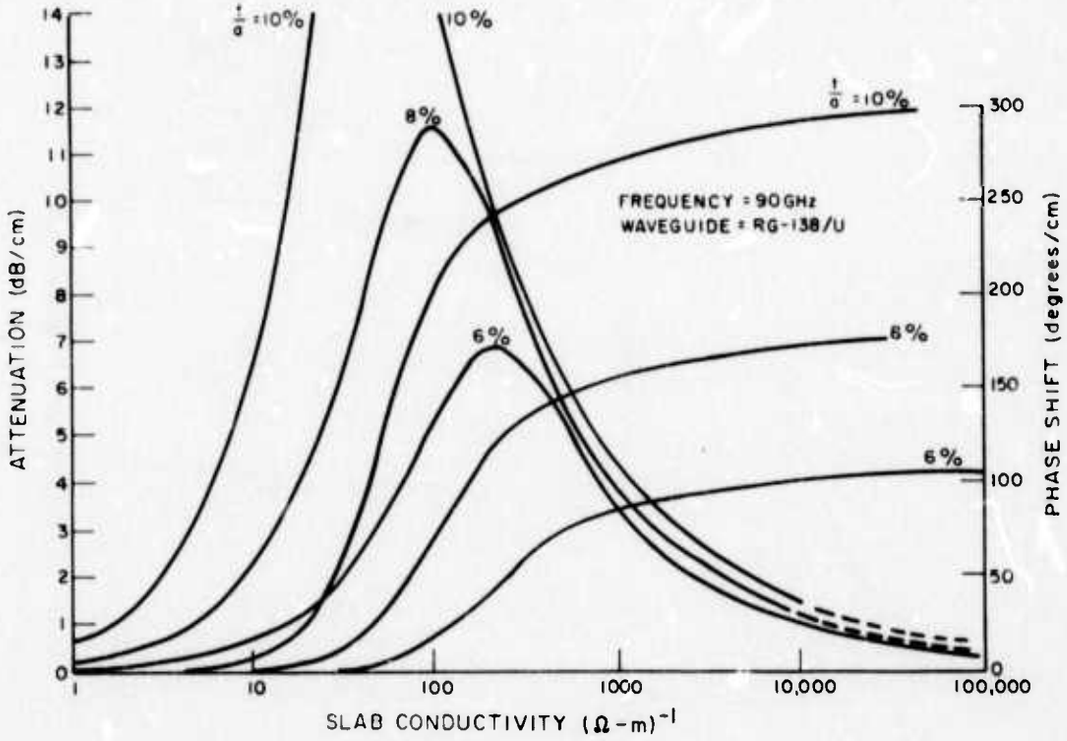


Fig. 7. Phase shift and attenuation for single slab on waveguide sidewall at 90 GHz.

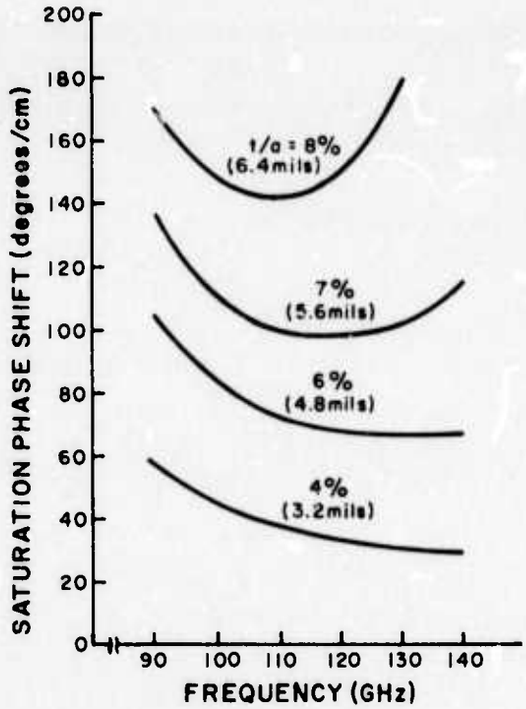


Fig. 8. Saturation phase shift versus frequency for single slab on waveguide sidewall.

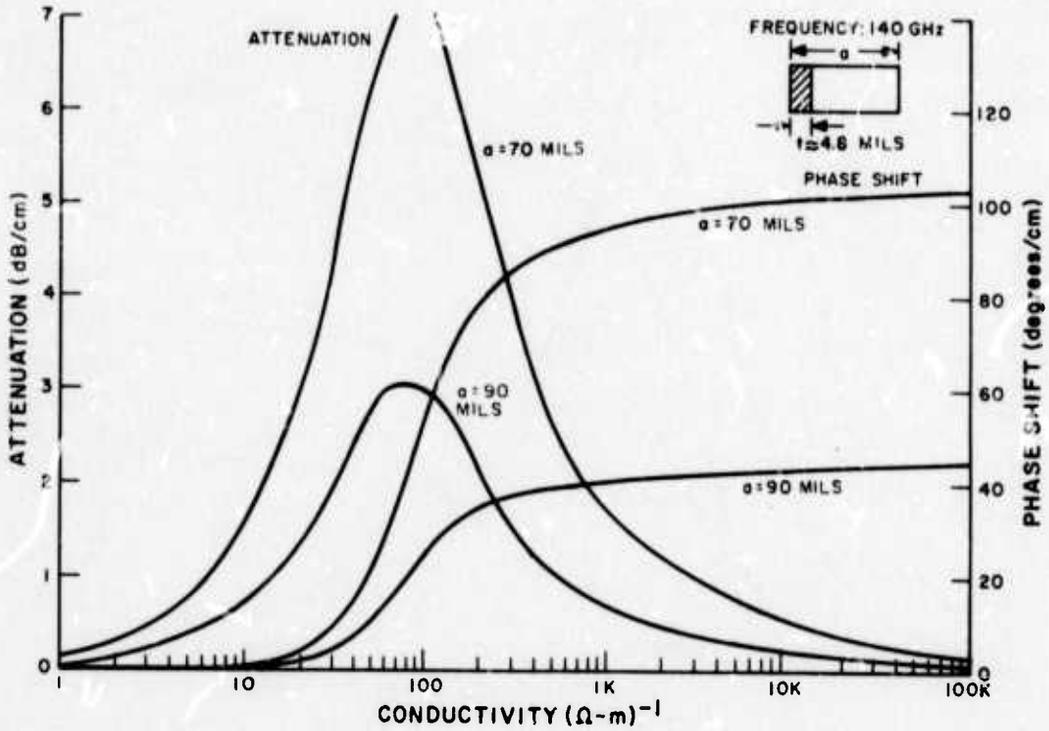


Fig. 9. Phase shift and attenuation for single slab on waveguide sidewall at 140 GHz, 70 and 90 mil wide guide.

and two slabs mounted symmetrically at each of the narrow walls. Both of these cases can be treated as a waveguide containing three homogeneous regions, as shown in Fig. 2. Application of the boundary conditions yields the following transcendental equation:

$$0 = f(\gamma) = h_1 h_3 \tan(h_2 d_2) + h_1 h_2 \tan(h_3 d_3) + h_3 h_2 \tan(h_1 d_1) - h_2^2 \tan(h_1 d_1) \tan(h_3 d_3) \tan(h_2 d_2) \quad (6)$$

where

$$\gamma^2 - h_1^2 - k_1 k_o^2 = h_2^2 - k_2 k_o^2 = h_2^2 - k_3 k^2 \quad (7)$$

and

$$k_i = \epsilon_{r_i} - j(\sigma_i/\omega\epsilon_o) \qquad i = 1, 2, 3 \quad (8)$$

The method of solution of the various cases is similar to that discussed above. The geometries considered here were not too different than that shown in Fig. 2. This similarity allowed the use of the roots in Fig. 4 as a "first guess" in the iterative solution. The search technique was then used to find the values of α and β that cause the right side of Eq. 6 to go to zero. For this case a variation of program WAVE is used in which Eq. 7 is substituted for Eq. 5.

Typical computer-generated results obtained for the various geometries are shown in Figs. 10, 11 and 12. For the curves in Fig. 10 the slab width is maintained constant and the slab is spaced progressively off the narrow wall. These curves are useful for tolerance studies; they show that if the slab is located slightly off the narrow wall the device performance can be significantly affected. The curves in Fig. 11 correspond to a semiconductor mounted on a dielectric slab (whose dielectric constant is the same as that of the semiconductor). In this case the sum of the two slab widths has been maintained constant. These curves indicate that the same amount of phase shift is obtained as we make the semiconductor slab thinner but maintain the total thickness of the semiconductor slab and dielectric constant. There is a limit to how far this can be carried, in that the semiconductor thickness must be at least one skin depth in its high conductivity state. Assuming the semiconductor to be quasi-metallic in the high conductivity state, the skin depth, δ, can be approximated by[7]

$$\delta = \frac{1}{(\pi f \mu \sigma)^{1/2}} \quad \text{(meters)} \tag{9}$$

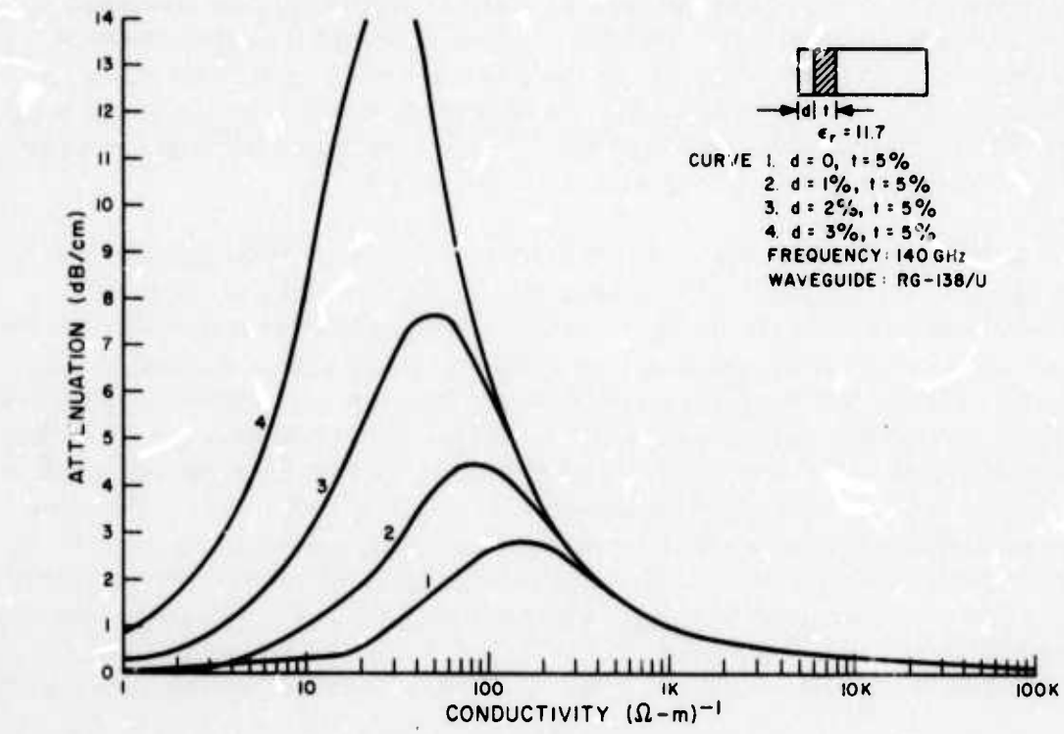
where

f = frequency

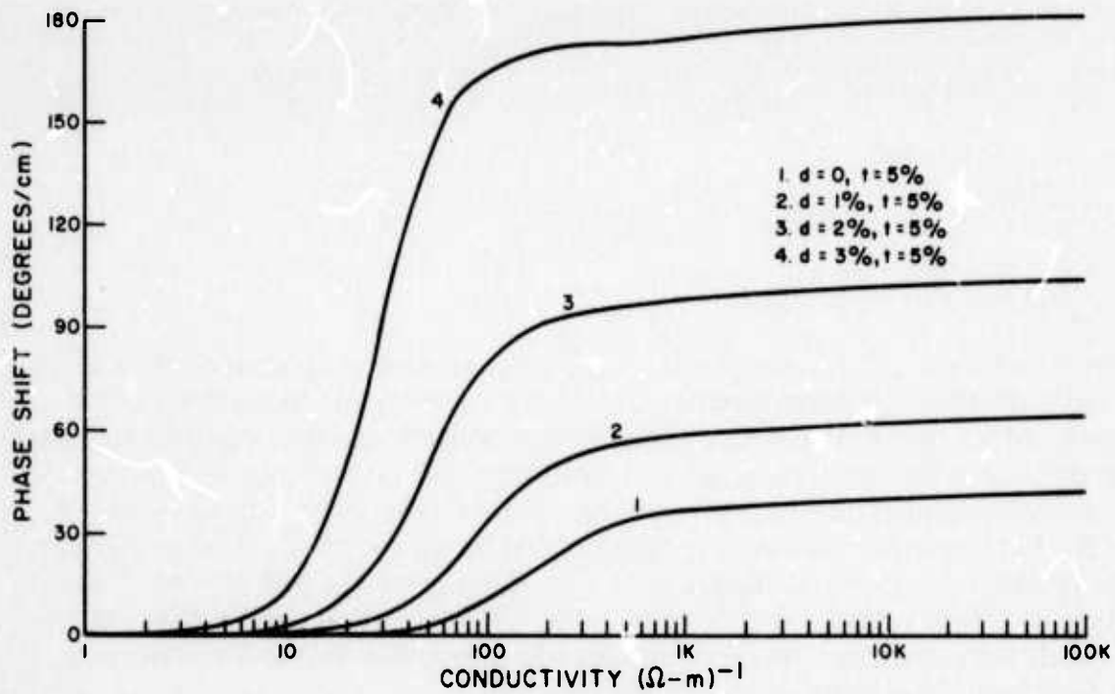
μ = slab permeability

σ = slab conductivity

At 140 GHz with $\sigma = 10^4\ (\Omega\text{-m})^{-1}$ and $\mu = \mu_o$, the corresponding skin depth is about 0.053 mil, or about 1.3 micrometers. This depth corresponds to a relative slab thickness of less than 0.1 percent. Another requirement on the composite structure is that the sum of the semiconductor and dielectric slab thicknesses be kept less than one-quarter wavelength in order to avoid the surface-type waves discussed above, where the field becomes concentrated in the lossy semiconductor. One possibility for obtaining the two layer structure is to epitaxially grow the thin semiconductor structure on a high resistivity substrate. The epitaxial-silicon technology has become highly advanced over the past decade, and appears to be readily applicable to the distributed PIN diode phase shifter elements.

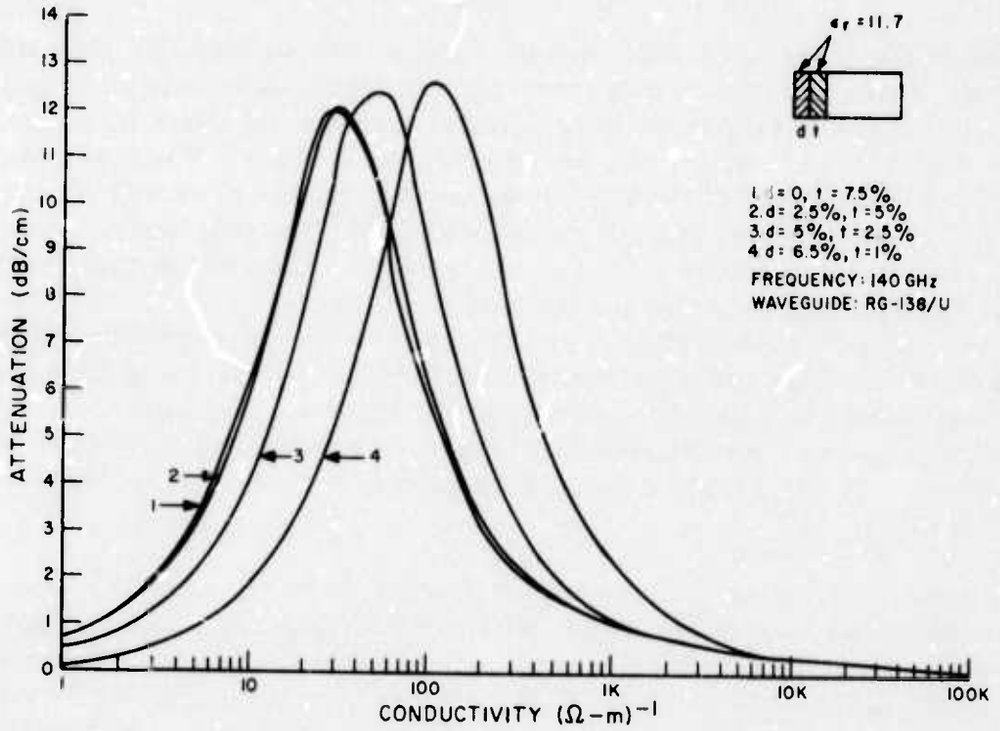


a. Attenuation.



b. Phase shift.

Fig. 10. Phase shift and attenuation for single slab spaced off waveguide sidewall at 140 GHz.



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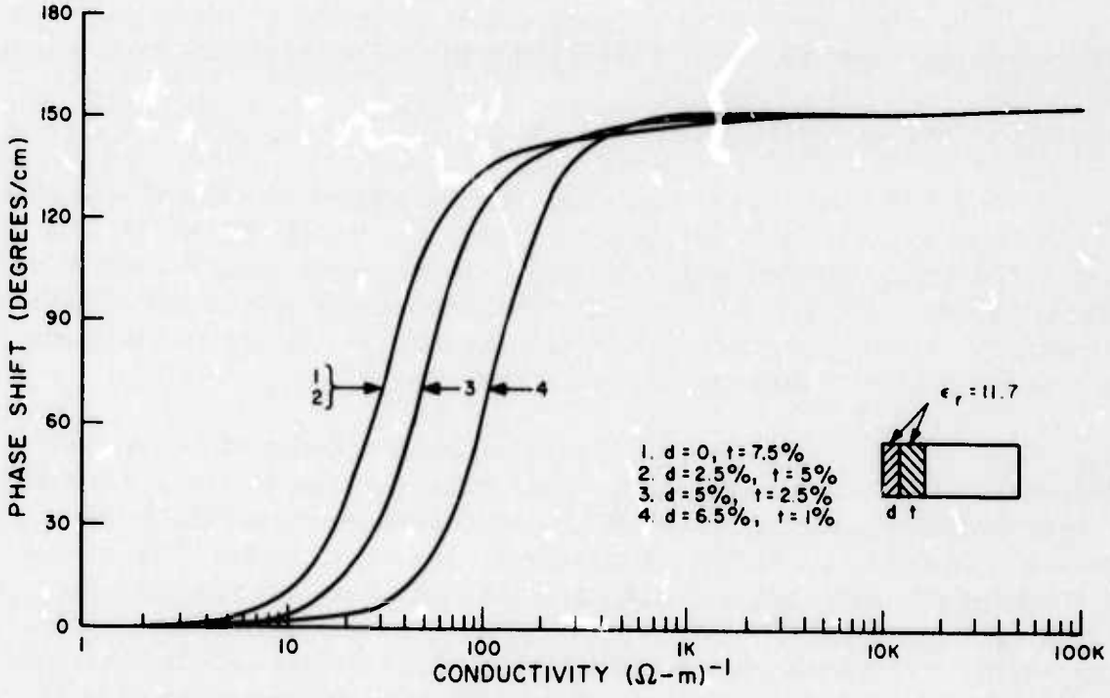


b. Phase shift.

Fig. 11. Phase shift and attenuation for dieleetrie spaeer between single slab and waveguide sidewall at 140 GHz.

The curves in Fig. 12 compare the symmetrically and unsymmetrically slab-loaded waveguides. These curves show that generally splitting the slab in its width and mounting the two slabs symmetrically on opposite narrow walls result in less phase shift as compared to the original slab mounted unsymmetrically. The lower phase shift results from the fact that the thinner slabs are in regions of weaker electric field for the TE_{10} type waves that are being propagated. The symmetrical arrangement may be advantageous when using two semiconductor slabs whose sum is greater than a quarter wavelength and also for the case of two thinned semiconductor slabs mounted on lossless dielectric slabs. For this case a slab whose relative thickness is 2 percent of that of the waveguide width, mounted on 14 percent thick dielectric, would lead to surface waves in the semiconductor. However, making the arrangement symmetrical (i.e., two 1 percent slab on 7 percent dielectrics) might lead to a useful, efficient device. To date, these structures have not been studied, either theoretically or experimentally.

Based on the above results, the optimum geometry (for maximum phase shift and minimum drive power) at 140 GHz in RG-138/U waveguide is a semiconductor slab of 1 percent or less relative thickness mounted or grown on a lossless dielectric whose relative thickness is about 7 percent. This geometry implies a semiconductor slab thickness of less than 0.8 mil and a dielectric thickness of 5.6 mils. This structure would yield phase shift of about 248° /cm and attenuation due to the semiconductor of a few tenths of a dB/cm in both its low and high conductivity states. Decreasing the waveguide width would lead to additional phase shift with increased attenuation as shown in Fig. 9. It appears that two of these composite slabs in a symmetrical arrangement would provide about 500° /cm of phase shift at 140 GHz in standard RG-138/U waveguide.

5. PIN Diode Geometry

Two sets of measurements have been carried out: one on a set of bulk silicon slabs of various conductivities, the other on a set of distributed PIN diodes. The results of the bulk slab measurements are reported in Sec. II.B, while the PIN diode results are given in Sec. III. For the bulk slabs the geometry approximated by the above analysis is quite good, with the measured results for both thin and thick slabs comparing favorably with those predicted theoretically.

However, the test mount used to evaluate the distributed PIN diodes only approximates the structure shown in Fig. II-2, in that the diode height was typically only about half the height of the waveguide. For efficient operation, the height of the diodes is limited by recombination statistics. The excess carrier lifetimes of the distributed PIN diodes has been running about 3 μs. This corresponds to an ambipolar diffusion length of 3 mils. (Diode parameters will be discussed further in Sec. III.B.) For uniform distribution of the injected carriers and minimum loss of carriers by recombination, the width of the diode intrinsic region should be, at most, a few diffusion lengths. This limits the height of the diodes, for the geometry

of Fig. 1, to about 10 mils. To partially compensate for the height difference, the waveguide height was tapered from its 40-mil standard height to 20 mils. Any further taper was found to lead to high test mount insertion loss (> 10 dB) due to the concentrated nature of the fields. The experimental RF results are discussed in Sec. III.C.

The case where the semiconductor slab only partially fills the waveguide height is difficult to analyze in that it leads to mixed boundary conditions. However, based on the experimental PIN diode results, it appears that the propagation in the half-height loaded guide is quite different from that in full height loaded waveguide. Thus, the latter analysis cannot fully explain the experimental results. A possible analytical approach to the half-height loaded guide is to break up the waveguide into a number of uniformly loaded sections.[8] Two such regions are needed for the case under consideration, as indicated in Fig. 13. The solutions for the fields in each region are obtained (by numerical techniques, if necessary) and the continuity of the fields across the boundary of each region yields the complete solution. While this technique is rather complex, it represents a systematic approach to the problem. Due to time limitations, this analysis has not been carried out.

B. BULK SLAB MEASUREMENTS

Two groups of bulk silicon slabs were prepared, all having dimensions 40 mils high and 1 cm long, and conductivities covering the range 1 $(\text{ohm-m})^{-1}$ to 10^4 $(\text{ohm-m})^{-1}$. One set of slabs was 6.2 mils wide (t/a = 7.8 percent) whereas the other set was 13 mils wide (t/a = 16 percent). The thicker set had less of a range in conductivity, thus providing limited results. The slabs were placed, one at a time, along the sidewall of a section of RG-138/U waveguide and their insertion loss and relative phase shift were measured.

The experimental arrangements used to make these measurements are the same as those shown in Fig. 24 for PIN diode measurements, except that the diode bias circuitry is absent; attenuation was measured by the substitution technique while phase shift measurements were obtained by means of a standard bridge technique. Typical results obtained for the two sets of slabs are shown in Figs. 14 and 15.

The insertion loss results in Fig. 14 are in good agreement with the similar data of Fig. 5 for t/a = 8 percent, whereas the measured phase shift is less than predicted by the analytical study. The limited experimental data for the 16 percent slabs in Fig. 15 compare qualitatively with the "lower branch" analytical results.

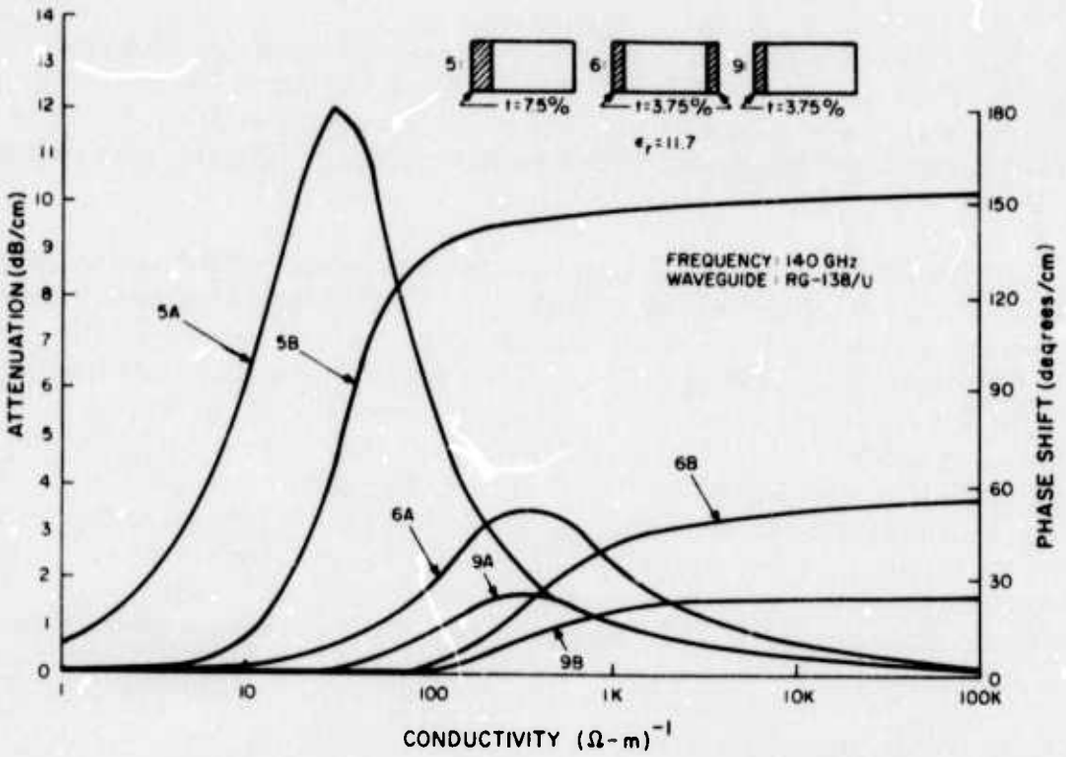


Fig. 12. Phase shift and attenuation for symmetrically and unsymmetrically loaded waveguide at 140 GHz.

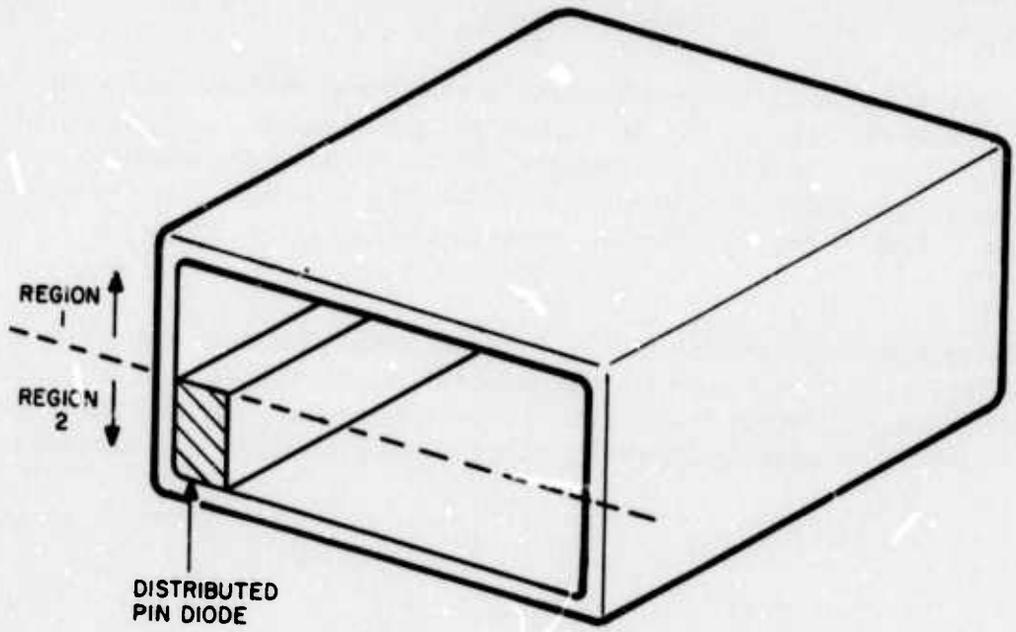


Fig. 13. Geometry for regional analysis of PIN diode loaded waveguide.

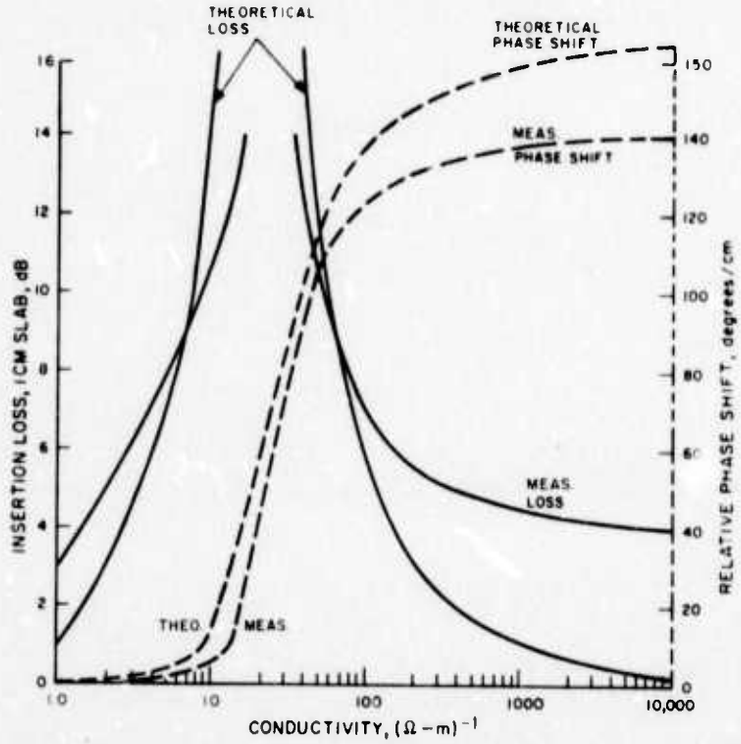


Fig. 14. Measured and theoretical phase shift and insertion loss for a 7.8% wide silicon slab on waveguide sidewall at 140 GHz.

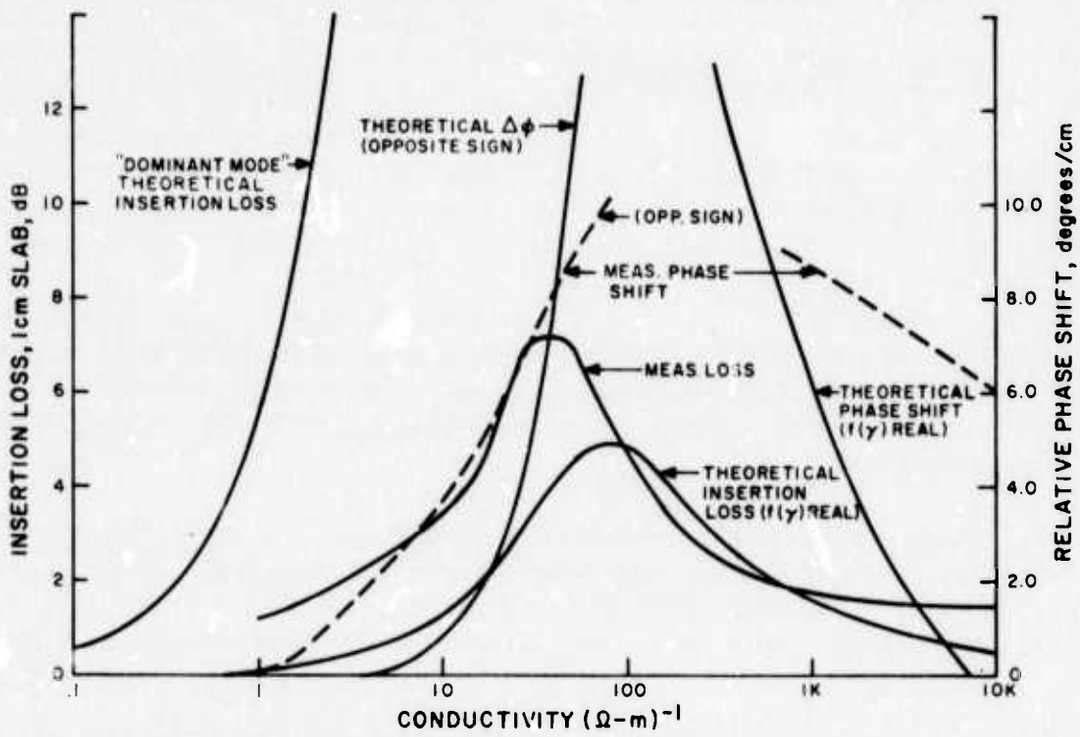


Fig. 15. Measured and theoretical phase shift and insertion loss for a 16% wide silicon slab on waveguide sidewall at 140 GHz.

Section III

THE DISTRIBUTED PIN DIODE

A. FABRICATION

The distributed PIN diode samples used in this investigation were formed by means of conventional diffusion techniques. The major aspects of the fabrication process are outlined in the following paragraphs.

1. Intrinsic Material

The "intrinsic" material from which sample diodes were made was N-type silicon having various resistivities in the range 50 to 2000 ohm-cm. The material was obtained from commercial sources (Monsanto and Wacker) in the form of wafers whose thickness would constitute the height of the diodes from contact to contact. The range of thicknesses was 6 to 13 mils. The silicon was of good quality, exhibiting minority carrier lifetimes in the range 100 to 1000 μs as measured on the original ingots by the photoconductive decay method. (The higher lifetimes correspond to the higher resistivities.)

2. Diffusion of P and N Layers

Typical diffusion cycles were begun with boron-doped and phosphorus-doped silicon dioxide deposited with silane gas at 350°C. Capping with silicon dioxide was performed. Diffusion at 1200°C for 3 to 6 hours yielded diffused layers 10 to 15 μm deep.

An alternate diffusion procedure made use of boron-doped oxide diffused at 1050°C for 30 min. This boron-doped SiO_2 was left on to act as a cap during the phosphorus diffusion. The diffusion source was phosphorus oxychloride, at a temperature of 950°C for 30 min. This procedure yielded P and N layers of about 2 to 3 μm thickness.

Table 1 summarizes the details of the diffusion schedules that have been used. Additional PIN diffused silicon wafers were obtained from U.D.T. Corp., E.G.& G. Corp., and Unitrode Corp. At this point in processing, the P, I, and N layers exist over the whole wafer, but individual diodes have not been defined.

TABLE 1. DIFFUSION SCHEDULES

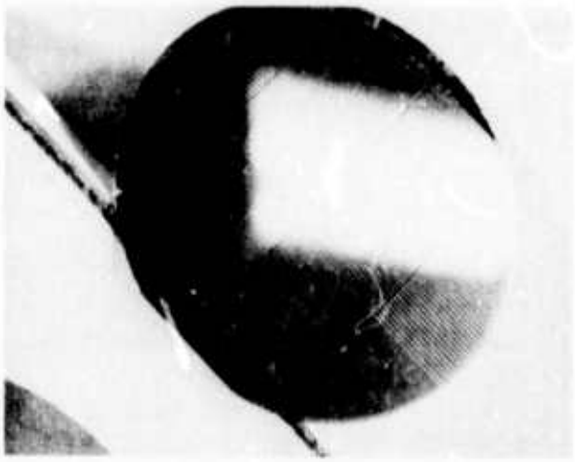
Schedule	Diffusion Conditions
a	1200°C for 6 hours, 15-minute quench in nitrogen.
b	1200°C for 7 hours, cool to 800°C in 4 hours, reheat in program-controlled furnace to 1200° C for 1 hour, cool to 700°C at 1 degree/minute, quench.
c	1200°C for 3 hours, 15-minute quench in nitrogen; half of the wafer batch slow-cooled as in b. above.
d	1050°C for 1/2 hour for boron, 950°C for 1/2 hour for phosphorus.

3. Metallization

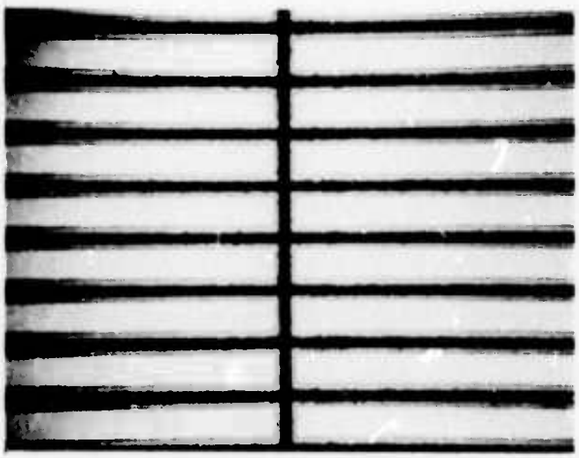
Metal electrodes are required in order to make electrical connection to the diodes. These electrodes were formed by sputtering thin (about 200 Å) layers of titanium and palladium onto both sides of wafers, followed by gold plating to a thickness of about 0.1 mil. The gold provides the bias current-distributing contact, while the titanium/palladium layers provide adhesion and isolate the gold from the silicon wafer. This isolation is necessary because gold has a tendency to diffuse into the silicon and cause a substantial reduction in carrier lifetime. For the same reason, the electrodes must be removed from the silicon in the vicinity of the paths to be followed in cutting the wafer into diodes, lest gold be driven into the silicon along the edges of the diodes. This last step is accomplished by application of photoresist to the wafer in the pattern of the diodes desired, leaving paths several mils wide between diodes. The electrodes are then etched away from these paths, leaving the wafer exposed in the areas where cutting or dicing is to be done. Figure 16a shows a typical wafer having patterns for two sizes of diodes on its face.

4. Dicing

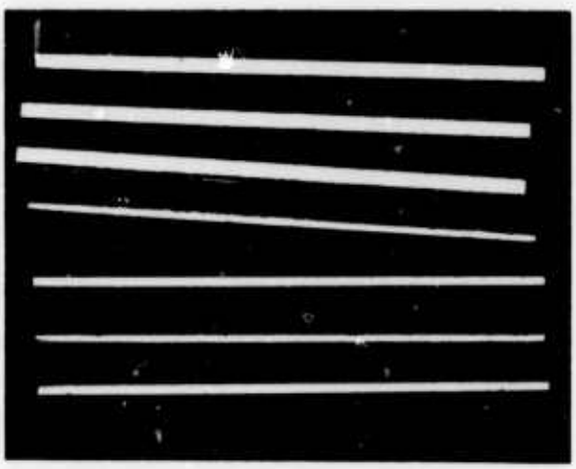
It was found that because of their unusual geometry, typically 0.01 x 0.01 x 0.4 in, the distributed PIN diodes could not be separated from the wafers by conventional scribing techniques. The method used for most samples was to cut around the edges of the diodes, to a depth of about 8 mils, using a Quantronix laser scriber. Figure 16b shows a view of the diode pattern on a wafer face after laser scribing. The dark lines are the laser-cut channels, and the wide light-colored strips are the gold contact strips. Note the small margin of silicon around the contact strips. Since the laser scriber was limited by power and focusing arrangements to a cutting depth of about



(a) Wafer with patterns applied



(b) Wafer face after laser scribing



(c) Finished PIN diodes viewed from top (contact) side; three widths are shown

Fig. 16. PIN diodes before and after dicing.

8 mils, wafers thicker than 8 mils required that the final separation of the diodes be accomplished by breaking the remaining silicon web. When the pattern edges and scribe lines followed cleavage planes, separation was easy; other conditions presented some difficulty leading to lower yields. The final step in processing was a brief acid etch which served to eliminate undesired surface roughness and to remove surface impurities picked up in processing. Figure 16c shows several finished diodes.

An alternate method of dicing that has been tried with very good results is based on the use of a multiple-wire saw. The saw that was tested is made by Geoscience Corp., Mt. Vernon, N.Y. Using a fine abrasive slurry, the wire saw gave straight smooth cuts, eliminating the problem of roughness in the break region of laser scribed wafers.

5. Diode Stacking

Diode stacking refers to a process that laminates two or more diode wafers in series, thus creating a monolithic "stack" of diodes. This technique was of interest in this program because it can produce an overall semiconductor assembly whose height is comparable to the nominal waveguide height. For example, a stack of 5 diodes, each 8 mils thick, will produce an overall diode assembly 40 mils high, thus matching the nominal waveguide dimension. Each diode would operate essentially as described for the individual PIN diodes. Note that a single diode with a very large intrinsic layer will not perform the same as this stacked assembly. Conductivity modulation of the I region is not effective much beyond the diffusion lengths, or 5 to 10 mils in practice.

Diode stacking is a common production technique for high-voltage rectifiers, and the type of diodes being investigated for the phase shifters should be stackable. A single demonstration effort was made by supplying two diffused wafers to the appropriate production group. About 500 Å of platinum were sputtered on the P side of one wafer and the N side of the other to be joined. Then 4000 Å of titanium were sputtered over the platinum. In a vacuum fixture the plated wafer surfaces were then pressed together at about 1000 psi by graphite blocks induction heated to 1200°C for 10 min. Slow cooling at 1°/min was then carried out. The previously described wire sawing technique is especially applicable for dicing these laminated wafers.

B. CHARACTERIZATION

The aim of this section is to characterize the PIN diode from both analytical and experimental viewpoints. The analytical discussion starts with the continuity equations for electrons and holes in the I layer of the diode and develops the current-voltage relationships. The experimental discussion reports on the highlights of the various measurements performed on the phase shifter PIN diodes. The main purpose of these measurements is to characterize diodes that will provide good RF performance.

Although the geometry of the distributed PIN diode is somewhat unique, the conductivity modulation phenomenon operates in the same manner as more conventional PIN diodes. The passage of moderate amounts of forward current through the diode results in injection of holes from the P-region and electrons from the N-region into the central intrinsic region. These injected carriers significantly increase the conductivity of the I-region.

This section presents those aspects of the PIN diode theory that are required to understand the operation of the device and identify the significant parameters and the roles they play. The purpose of the following paragraphs is to analytically determine the diodes current-voltage characteristic, and thereby understand the details of the conductivity modulation phenomenon. Essentially, the procedure is to determine the nature of the charge distribution in the I layer at the various injection levels, apply Poisson's equation to obtain the electric field, and then integrate to obtain the voltage.

1. Charge Distribution in the I Layer

The steady-state equations relating to current flow in a semiconductor are the drift and diffusion current equations and the continuity equations for electrons and holes. If we assume diffusion dominated operation, these equations can be manipulated into the following:[9]

$$\frac{(b+1)}{\mu_n \tau} n = 2\beta \frac{d^2 n}{dx^2} \tag{9}$$

$$J = e\mu_p [(b+1) nE + \beta (b-1) dn/dx] \tag{10}$$

where a one-dimensional model has been assumed without sacrificing the generality of the results, and where

$n = p$ = the equal electron and hole densities

$\beta = \frac{kT}{e}$

k = Boltzmann's constant

T = temperature, K

e = electronic charge

τ = high level lifetime

μ_n (or μ_p) = electron (or hole) mobility

b = μ_n/μ_p

x = distance into I layer; x = o at P-I junction and x = L at N-I junction

J = current density

E = electric field intensity

Equation 9 has the solution

$$n = \frac{n_o \sinh [(L-x)/L_a] + n_L \sinh (x/L_a)}{\sinh (L/L_a)} \tag{11}$$

where

L_a = $[2\beta \mu_n \tau/(b+1)]^{1/2}$ = ambipolar diffusion length

L = length of I layer

n_o = carrier density at P-I junction (x=o)

n_L = carrier density at N-I junction (x=L)

In order to evaluate the two constants n_o and n_L we apply boundary conditions at the two junctions. This is done by equating currents on each side of each of the junctions. For the P-I junction it is convenient to consider the electron current (density) J_n. The low resistivity of the P layer results in only a small electric field, which can be neglected leaving J_n as a purely diffusive current. In the I region, J_n has both diffusion and drift components. Similar statements apply for the hole currents on each side of the N-I junction.

For the P-I junction we obtain

$$\frac{\beta n_o^2}{L_n p_p} = \frac{J}{e\mu_p (b+1)} + \frac{2\beta}{(b+1)} \left.\frac{dn}{dx}\right|_{x=o} \tag{12}$$

For the N-I junction we obtain

$$\frac{\beta n_L^2}{L_p n_n} = \frac{J}{e\mu_p (b+1)} - \frac{2\beta b}{(b+1)} \frac{dn}{dx}\bigg|_{x=L} \tag{13}$$

where

J = total current density

L_n (or L_p) = electron (or hole) diffusion length in the P (or N) layer*

p_p (or n_n) = hole (or electron) density in the P (or N) layer.

The next step might be to substitute the expression for n of Eq. 11 into Eqs. 12 and 13 and solve them simultaneously for n_o and n_L, a difficult task. However, two approximations are applicable, either of which will simplify the solution of these equations. Solutions for n_o and n_L are readily obtained for $L >> L_a$ ("long diode") or $L << L_a$ ("short diode"). The solutions have the same form for either case, but different coefficients. The long diode approximation allows Eq. 11 to be written as

$$n = n_o \exp(-x/L_a) \tag{14}$$

While the short diode approximation gives

$$n = n_o \frac{1}{2}\left(1 - \frac{x}{L}\right) + n_L \frac{x}{2L} \tag{15}$$

Under these conditions Eq. 12 and 13 become, respectively, for the long diode

$$\frac{\beta n_o^2}{L_n p_p} = \frac{J}{e\mu_p (b+1)} - \frac{2\beta n_o}{(b+1) L_a} \tag{16}$$

*If L_n or L_p is much greater than the length of the relevant layer, the length of the layer replaces the diffusion length in Eqs. 12 and 13.

$$\frac{\beta n_L^2}{L_p n_n} = \frac{J}{e\mu_p(b+1)} - \frac{2\beta b n_L}{(b+1) L_a} \tag{17}$$

and for the short diode

$$\frac{\beta n_o^2}{L_n p_p} = \frac{J}{e\mu_p(b+1)} - \frac{\beta (n_o - n_L)}{(b+1) L} \tag{18}$$

$$\frac{\beta n_L^2}{L_p n_n} = \frac{J}{e\mu_p (b+1)} - \frac{\beta b (n_L - n_o)}{(b+1) L} \tag{19}$$

If we now consider asymptotic solutions of the above four equations, we find two solutions for each equation, corresponding to two distinct injection levels. For example, in Eq. 16 we can consider

$$n_o << \frac{2 L_n p_p}{(b+1) L_a} \qquad \text{("low injection level")}$$

or

$$n_o >> \frac{2 L_n p_p}{(b+1) L_a} \qquad \text{("high injection level")}$$

Similar relations apply for Eqs. 17, 18 and 19. Solving the four equations (16, 17, 18, 19) under these approximations, we find for both the long and short diodes that the low injection levels result in n_o and n_L proportional to J while the high injection levels result in n_o and n_L proportional to $J^{1/2}$. If these results for n_o and n_L are substituted into Eq. 11 we obtain the I layer charge distribution for low and high injection levels in long and short diodes.

2. I-V Characteristic

The electric field in the I layer is found for the various cases by substituting the expressions for the charge distribution, n, into Eq. 10. For long and short diodes at low injection levels this step eliminates J from Eq. 10 indicating E is independent of J. The voltage drop across the I (bulk) layer is found by integrating E. For both diodes the voltage is constant, given by

$$V_B = \frac{\beta b^{1/2} \pi}{(b+1)} \exp(L/2L_a) \text{ where } L >> L_a \quad (20)$$

$$V_B = \frac{2\beta b}{(b+1)^2} (L/L_a)^2 \text{ where } L << L_a \quad (21)$$

Since the injected carrier density was found to be linearly proportional to the total current during low injection, the conductivity must be inversely proportional to the current and the I layer voltage drop should, indeed, be a constant.

For high injection levels the injected carrier density was found to be proportional to $J^{1/2}$. Inserting the specific relations into Eq. 10 we find that E is no longer independent of J. Integrating E to obtain the I layer voltage we find, for both the long and short diodes,

$$J = A V_B^2 \quad (22)$$

where the constant A has appropriate values for the long and short diodes.

Figure 17 shows the two injection regimes discussed here. In addition, at very low drive levels where the injected carrier density is less than the intrinsic concentration, the I layer is ohmic in behavior, presenting a third regime.

This analysis deals with V_B, the voltage drop across the I layer. To accurately predict the total diode voltage drop we must add to V_B the voltage drops across the contacts, the doped layers, and the junctions. While the analysis given here is adequate for our purposes, its approximate nature must be kept in mind.

3. Experimental Measurements

When diodes have been constructed there are three measurements which can be made with reasonable ease to help determine whether the diodes will function properly. They are spreading resistance, I-V characteristics, and carrier lifetime measurements. The fabrication details referred to are described in part A of this section.

a. Spreading Resistance

Spreading resistance measurements were performed on the various diffused silicon PIN diode wafers by using a four-point probe assembly. After the wafers are lapped down to a five-to-one taper, the local resistivity is measured by using the probe assembly. These results are summarized in Table 2. Group 3 diodes

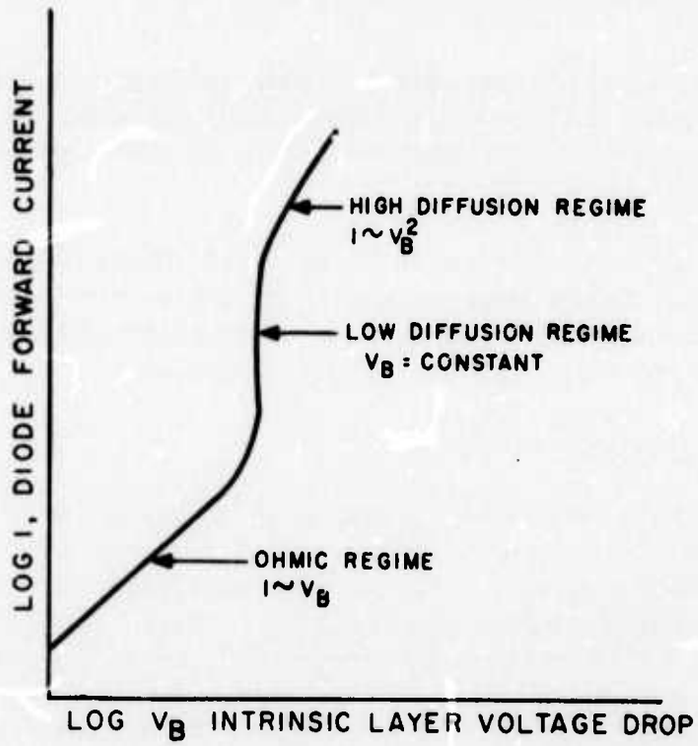


Fig. 17. Theoretical I-V_B characteristic for PIN diode.

TABLE 2. SPREADING RESISTANCE MEASUREMENTS

Group	Diffusion Schedule	L_n, L_p (μm)	p_p, n_n (cm^{-3})	L (μm)	ρ (Ω-cm)
3	a	13.5	4×10^{19}	212	50
4	b	15.6	5×10^{19}	208	650
9	d	2.5	10^{18}	236	1600

NOTES

L_n, L_p are the lengths of the doped layers.

p_p, n_n are the carrier densities of these layers.

L is the length of the intrinsic layer.

ρ is the resistivity of the intrinsic layer.

were processed from 50 ohm-cm silicon wafers, while groups 4 and 9 wafers had initial resistivities of 750 ohm-cm and near 2000 ohm-cm, respectively. Groups 3 and 4 are seen to have fairly similar doped layers, while group 9 diodes have a more shallow diffusion.

The spreading resistance data has been useful in evaluating the post-diffusion wafers, by providing the carrier populations and lengths of the various regions of the PIN diode phase shifting elements. It has confirmed that the manufacturing processes are providing diffusions of the type desired.

b. I-V Characteristics

The different diode groups exhibited a large range of I-V characteristics. Figure 18 is a multiple exposure photograph of the I-V characteristics of a number of diodes from various groups. Diodes from groups 3 and 9 are seen to have a sharp break in their characteristic while the group 4 diode is seen to have a gradual break and a corresponding large forward voltage drop. Generally diodes with a sharp, nearly vertical break at about 0.6 V gave satisfactory insertion loss and phase shift performance, while diodes with a large forward voltage drop exhibited high insertion loss.

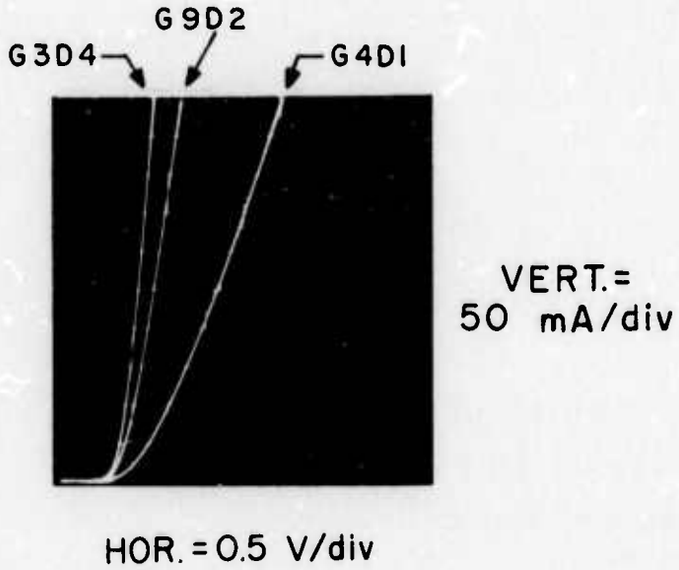


Fig. 18. Multiple exposure photograph of the I-V characteristic of various distributed PIN diodes.

A typical plot of the I-V characteristic of a group 9 diode on a log I-log V format is shown in Fig. 19. This curve (which plots the total voltage across the diode) is to be compared with the theoretical curve shown in Fig. 17 (which plots only the voltage across the intrinsic layer). To get the intrinsic layer voltage from the total voltage, we would have to subtract the junction, contact and series resistance voltage drops. However, it is possible to evaluate the experimental data without actually doing this. In Figs. 17 and 19 there are a number of essential similarities. For instance at low values of current and voltage, the curve in Fig. 19 exhibits a linear region (slope ≈ 1) corresponding to the ohmic regime of Fig. 17. This region is followed by a steeply rising portion corresponding to the vertical low diffusion regime of the theoretical curve. The falloff of the steep portion in Fig. 19 at high values of diode current corresponds to the high diffusion regime. The break between these two regimes is seen to occur at a few hundred milliamperes of forward current.

Additional insight can be gained by plotting the data of Fig. 19 on a log I-V (i.e., semilog) format, as shown in Fig. 20. This curve shows a straight line exponential regime where $I \sim \exp\left(\frac{eV}{nKT}\right)$, where $n = 2.5$ for this particular diode. The theoretical value of n for a PIN diode in the double-injection regime is two.[10] The falloff of the curve at high currents characterizes the effects of series resistance. In this region, the current departs significantly from exponential behavior and becomes limited by the series and contact resistances of the diode.

It is possible to use the curve in Fig. 20 to get a measure of the degree of conductivity modulation under bias conditions. The diode series resistance can be effectively subtracted by extending the straight line section of the curve. The ac conductance of the intrinsic layer is then given by the slope of the I-V curve at the bias current of interest. Figure 21 shows the conductivity modulation as a function of bias current. The initial conductivity of the I region for this diode was about 0.06 $(\Omega\text{-m})^{-1}$. Thus we have effected about a four-order-of-magnitude modulation.

e. Excess Carrier Lifetime

An important parameter in characterizing a PIN diode is the lifetime τ or the ambipolar diffusion length L_a of the excess carriers injected into the I region. These two parameters are related by

$$L_a = [2\beta\mu_n \tau/(b+1)]^{1/2} \tag{23}$$

For intrinsic silicon this becomes

$$L_a \text{ (mils)} = 1.7\,[\tau\ (\mu s)]^{1/2} \tag{24}$$

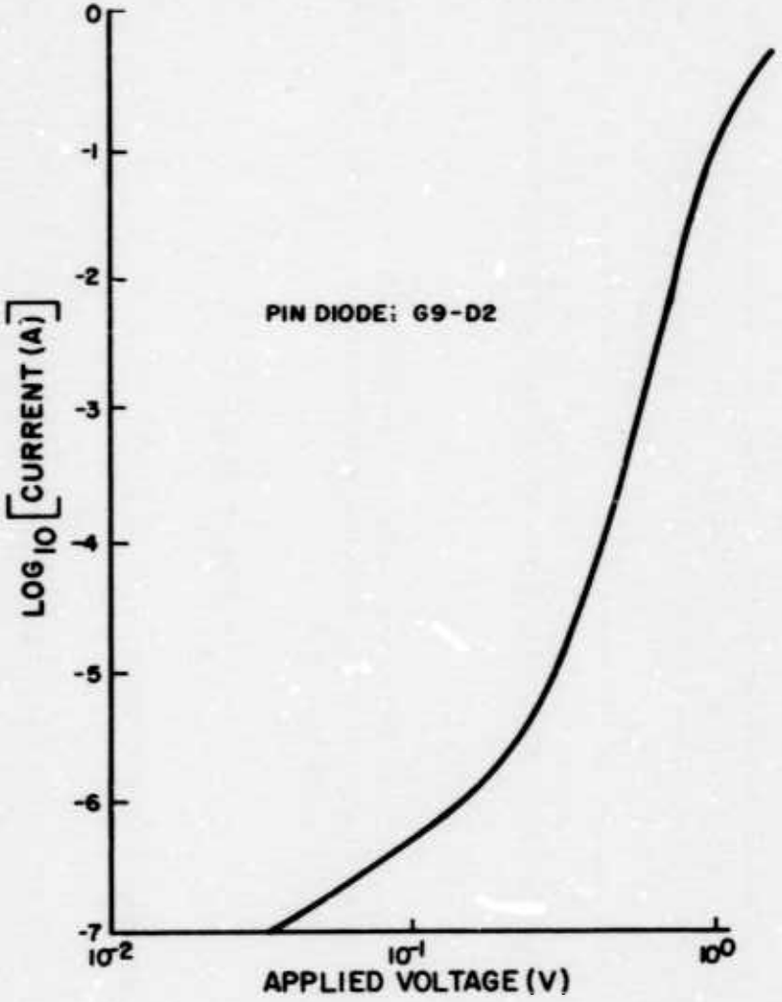


Fig. 19. Forward current versus applied voltage for diode G9-D2 plotted on a log-log format.

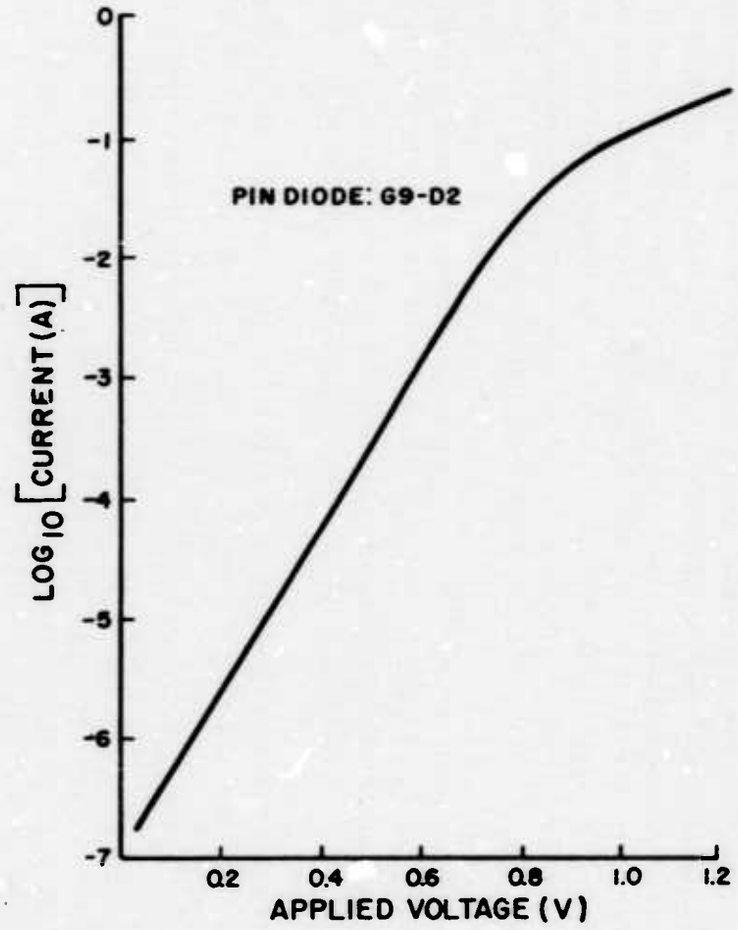


Fig. 20. Forward current versus applied voltage for diode G9-D2 plotted on a semilog format.

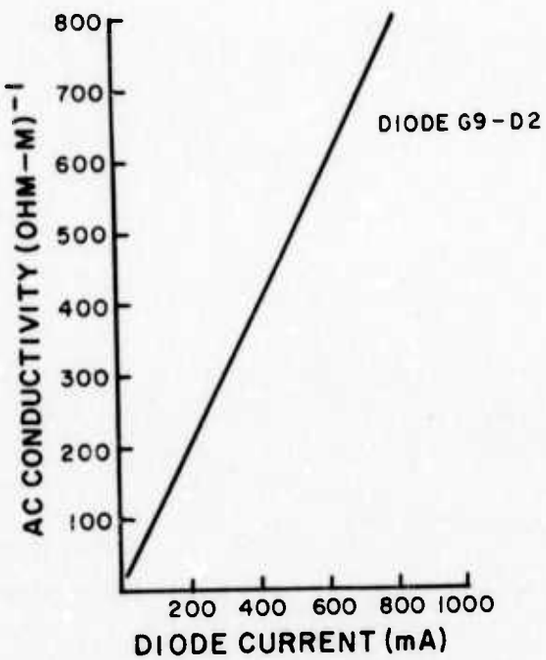


Fig. 21. Conductivity of intrinsie region of a PIN diode as a funetion of forward eurrent.

A plot of Eq. 24 is given in Fig. 22. From Eq. 11 it ean be seen that L_a is the characteristie length for PIN diodes. For a long diode ($L >> L_a$) the exeess carriers decay as exp ($-x/L_a$) from the injeeting eontaet.

The eireuit used for lifetime measurements of the PIN diode phase shifter elements is shown in Fig. 23. The teehnique used is to fill the intrinsie layer of the diode with exeess holes and eleetrons by pulsing the diode under test (DUT) with a forward voltage, and then observe the open-eireuit voltage transient aeross the diode. Under eonditions of high-level injeetion (i.e., injeeted carrier density greater than the doping density of the I region), the lifetime is related to the voltage deeay as follows:[11]

$$\tau = \frac{2KT}{e} \left(\frac{dV}{dt}\right)^{-1}$$

Table 3 summarizes the lifetime measurements for the various groups of PIN diodes. Sinee the lifetime is a funetion of the injeetion level, it is important that it is measured at the level of interest. The values reported in the table were measured at a forward current of 300 mA, and range from about 2.5 μs to 4.0 μs. From Fig. 22 these values correspond to a range of ambipolar diffusion lengths between 2.6 mils

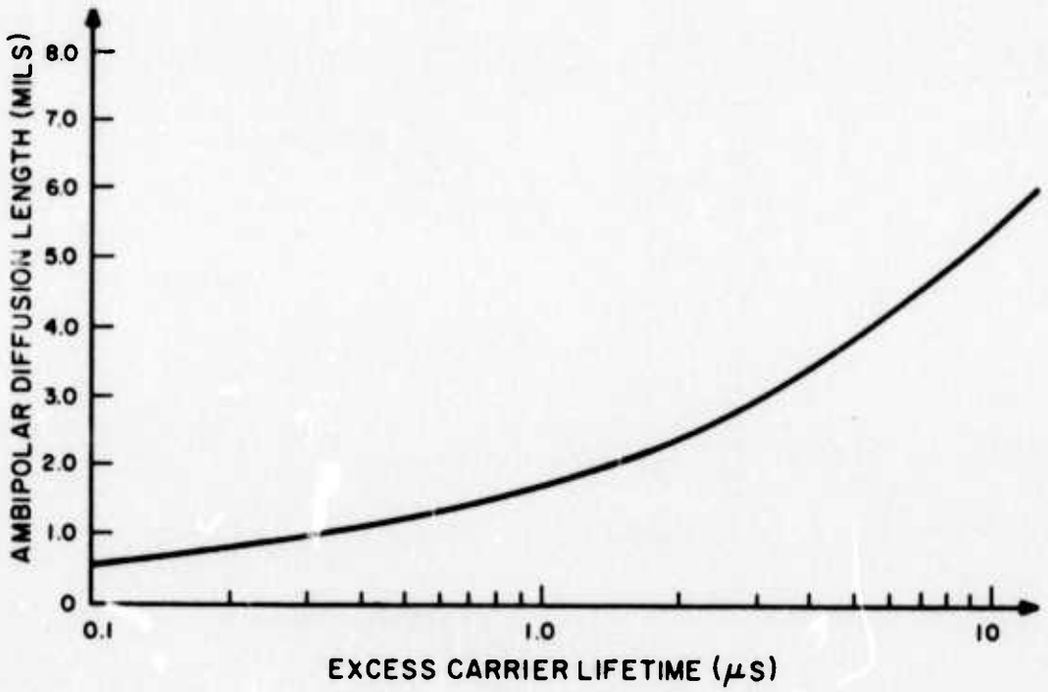
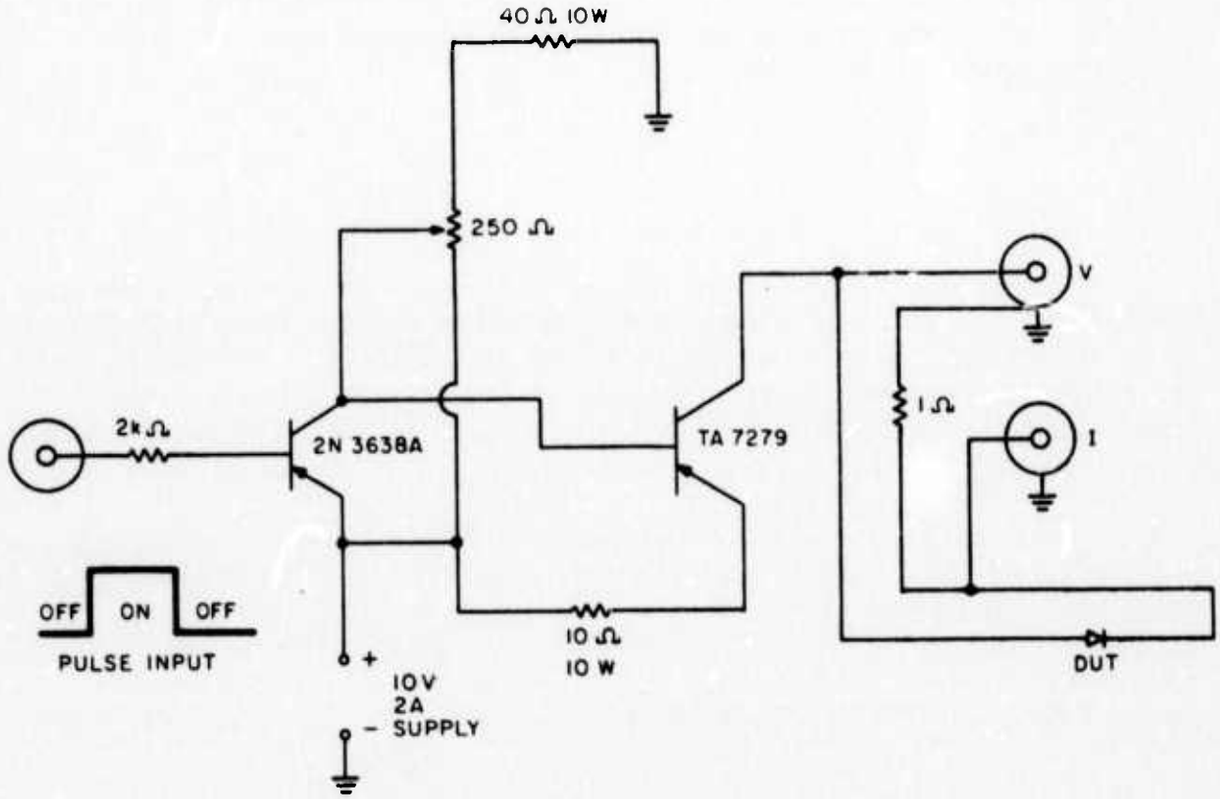


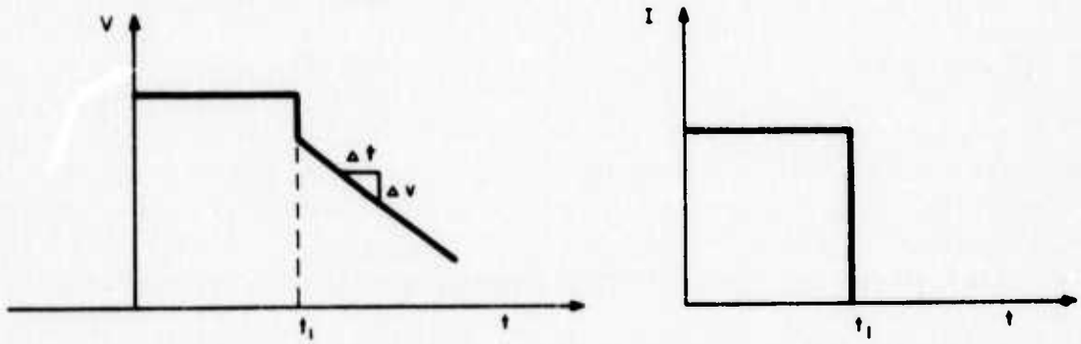
Fig. 22. Ambipolar diffusion length versus excess carrier lifetime for intrinsic silicon.

TABLE 3. CARRIER LIFETIME MEASUREMENTS

Diode Group	τ (μs)
3	3.3
3	2.5
6	2.8
9	2.6
9	4.0



a. LIFETIME MEASUREMENT CIRCUIT



b. OUTPUT WAVEFORMS

Fig. 23. Circuit used for lifetime measurements, showing the input and output waveforms.

and 3.4 mils. Most PIN diodes evaluated have approximately a 10-mil intrinsic layer width, which corresponds to about three to four diffusion lengths.

An increase in τ by about one order of magnitude would lead to a 9-mil diffusion length, which would increase the injection efficiency and would lead to lower drive power requirements.

C. RF MEASUREMENTS

1. Test Setup

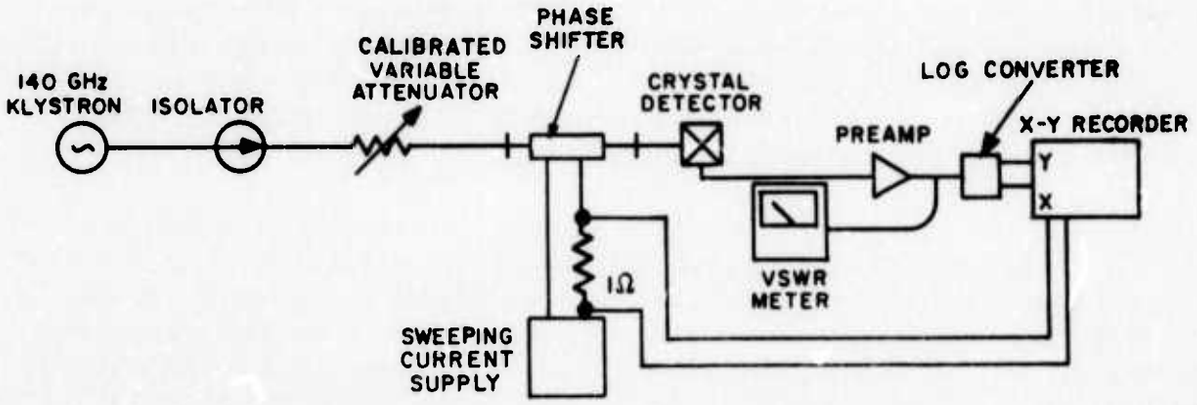
The experimental arrangements used to measure attenuation and phase shift are shown in Fig. 24. Insertion loss was measured by the substitution method by using the calibrated variable attenuator. Plots of loss versus bias current were obtained by means of the sweeping current supply and the X-Y recorder. Use of the log converter allowed calibration of the recorder charts in dB/in on the Y axis, while the X axis units were mA/in.

Phase shift measurements were done by means of a standard bridge technique, Fig. 24b. Here the signal from the klystron source is split between two paths. One path provides the phase reference signal, while the other includes the phase shifter producing unknown phase shift. The probe of the slotted waveguide section is moved along the guide until a null is encountered in the standing wave produced by the signals from the two bridge arms. (The variable attenuators may be adjusted for a deep null.) Next the phase shifter bias current is increased from 0 to 500 mA in convenient increments while the location of the null is tracked with the slotted line. Provided the reference arm has not been disturbed, the difference in phase shift between any two bias current levels can be obtained in degrees by dividing the linear null shift by the guide wavelength and multiplying by 360. In addition to the bridge configuration shown in Fig. 24b, occasional tests were done by using an isolator in each arm of the bridge to check for the absence of reflection effects.

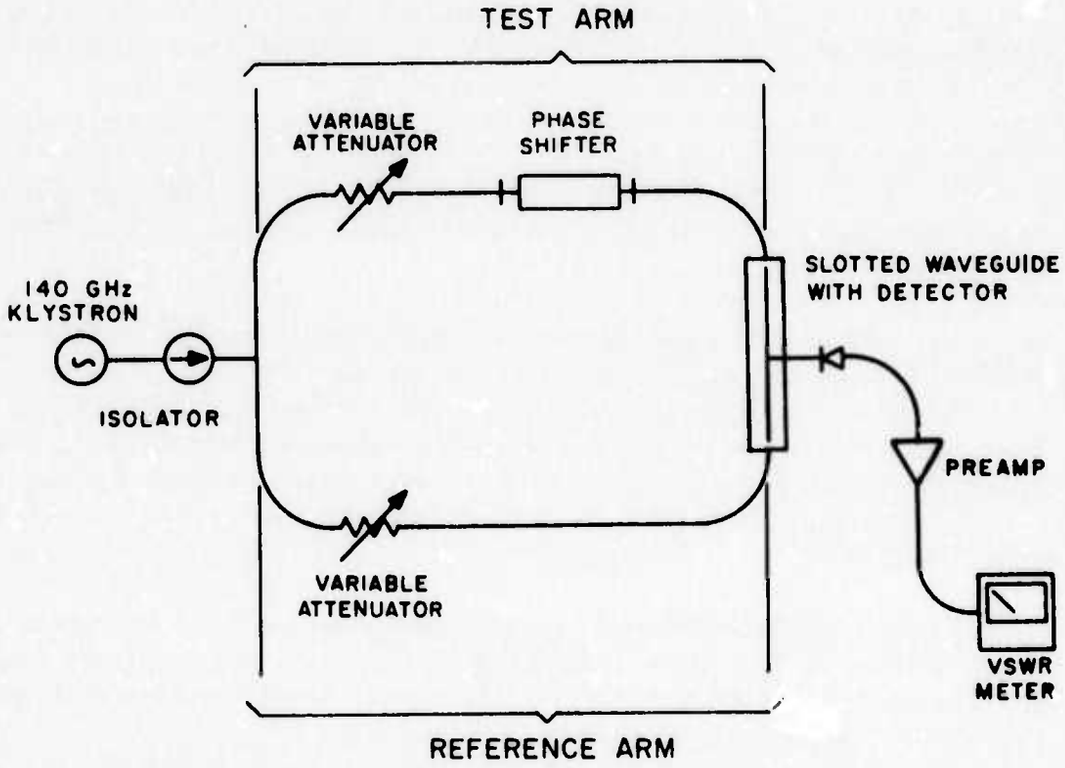
2. Diode Mount

Because of the distributed parameter nature of the PIN diodes used here, the experimental diode mounts were essentially nothing more than appropriate sections of transmission line. Of course, the practical matters of matching to standard waveguide, mounting the diode, providing a bias current path, and allowing for easy installation and removal of the various diodes required the addition of appropriate features.

The test equipment and components available for immediate use were mostly in RG138/U waveguide, which has an interior width of 80 mils and a height of 40 mils. Because of diodes were limited to heights in the 5 to 15 mil range by the nature of the conductivity modulation mechanism, the height of the waveguide was reduced in



a. Setup for insertion loss measurements.



b. Setup for phase shift measurements.

Fig. 24. Experimental arrangements for insertion loss and phase shift measurements.

the diode mount to 20 mils or less while retaining the 80 mil width for convenience. The diodes were held in place in the mount by low density plyfoam spacers or wedges of Rexolite 1422 inserted in the waveguide. The dc bias circuit was established by allowing one contact strip of the diode to rest against the bottom of the waveguide while a fine insulated wire was inserted through a small hole in the top of the waveguide to make contact with the other diode contact strip. Figure 25 shows a cross-section view of the diode mount, looking through the narrow wall of the waveguide, while Fig. 25a is a photograph of the same mount.

Several mounts were made and tested for transmission loss without diodes at 140 GHz. The 2 to 3 dB typical measured loss is not considered high since the mount is in the form of a split waveguide embedded in a brass block, and has an overall length of 4 in, including the region where the diode is located, the input and output tapers, and input and output waveguide extensions for working convenience. While the 2 to 3 dB mount loss would be unacceptable in a phase shifter for actual antenna use, it is not a cause for concern when evaluating the PIN diodes.

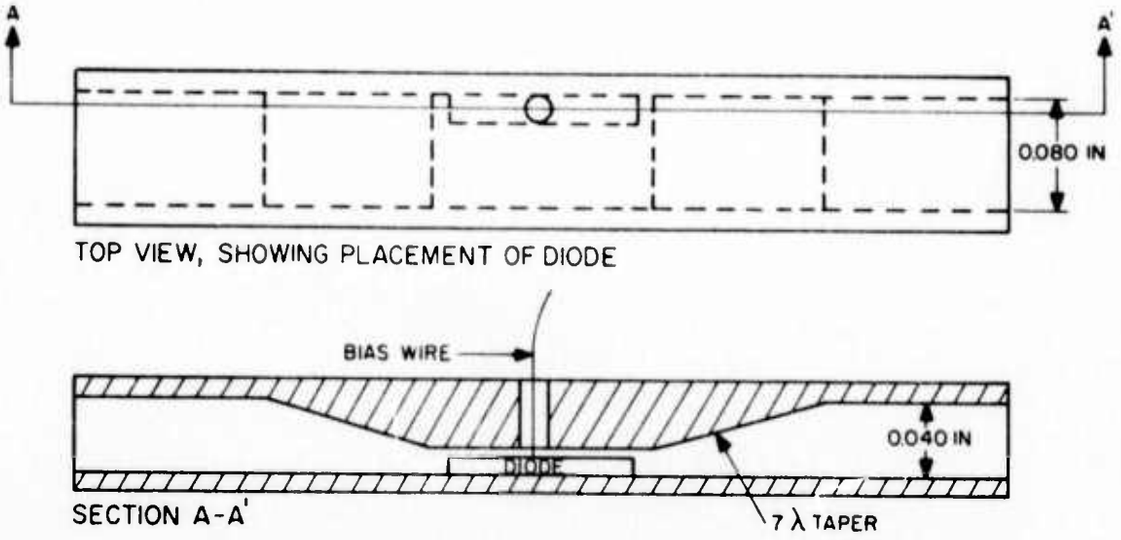
3. Test Data

Various distributed PIN diode samples prepared as described in Sec. III.A were tested for attenuation and phase shift at 140 GHz. All diodes were 1 cm long and were tested for forward bias currents in the 0 to 500 mA range.

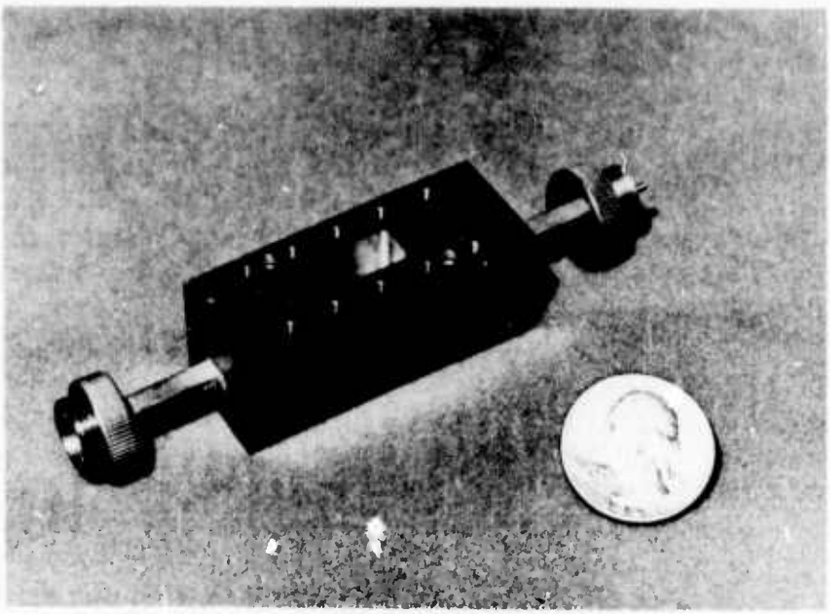
It is important to note that almost every diode tested differed in some significant way from the model used for theoretical studies. These differences were the result of expediencies of the moment; a practical approximation to the analytically studied configuration does appear to be attainable.

The test results were quite sensitive to the position of the diode within the mount. For any given diode, the strongest effects were due to the proximity of the diode to the waveguide sidewall. Figure 26 shows how the loss characteristic of diode G19-D2 varied for 1-mil changes in the diode position with respect to the sidewall. The indicated spacings were obtained by means of Mylar shims placed between the diode and the waveguide wall. Figure 27 shows similar data for seven different positions of diode G19-1F.

The relative heights of the diode and the waveguide also had a bearing on the experimental results. Figure 28 shows the effect of three different waveguide heights on the loss characteristic of diode G19-2F. Note that the "static" or zero bias insertion loss is also affected by mount geometry and diode position.



(a) Top and cross-section view (simplified)



(b) Photograph

Fig. 25. Experimental diode mount.

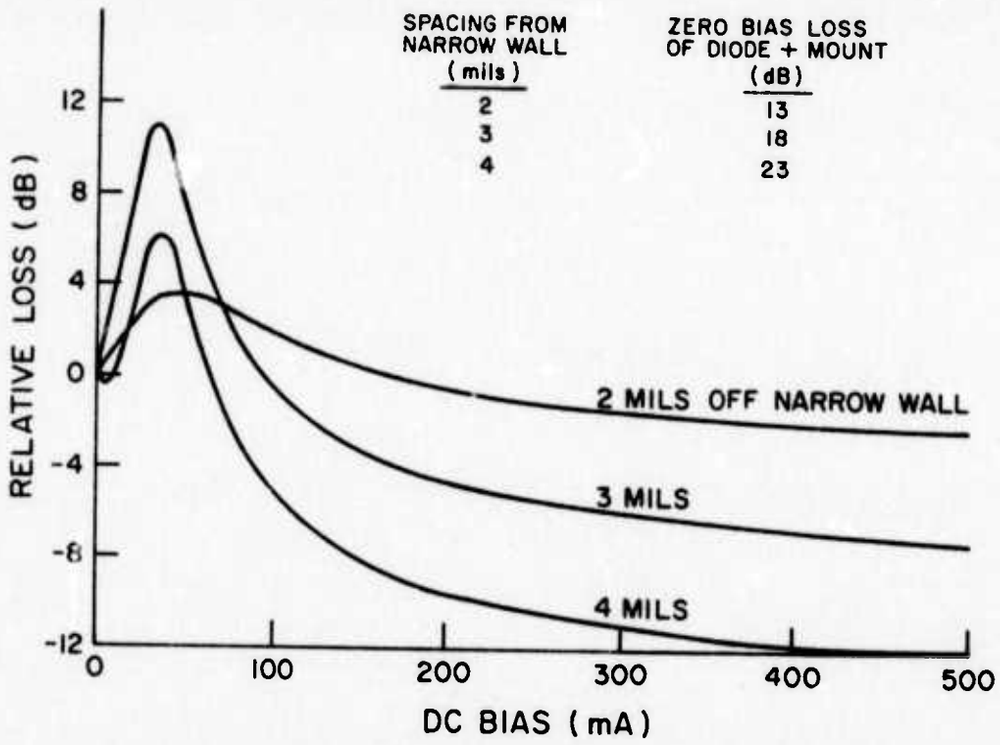


Fig. 26. Loss characteristic of diode G19-D2 for various mounting positions.

In the preceding discussion, phase shift was not mentioned because the nature of the loss characteristic provides an indication of the phase characteristic, and the loss data are easier to obtain in the laboratory.

Diodes of the type yielding the data of Fig. 29a were the first to provide a significant amount of controlled phase shift at 140 GHz. These diodes were processed from 50 ohm-cm silicon by using a high temperature diffusion. They have a nominal width of 12 mils. While the phase shift performance is attractive, the loss is very high even if the 2-1/2 dB of "breadboard" diode mount loss is taken into account.

The diode of Fig. 29b has the same geometry as that shown in Fig. 29a but displays a substantially reduced loss characteristic. Allowing for the breadboard mount loss, the diode loss is seen to be less than 1 dB in the "off" state (0 mA) and less than 2 dB in the "on" state (500 mA). This group of diodes was processed from 1600 ohm-cm silicon, a much higher resistivity than in the diode described above. The high resistivity is necessary in order that the diode I layer appear as a low-loss dielectric to the millimeter waves when the diode is not biased. Only a few samples of the low-loss type of diode depicted in Fig. 29b were obtained. Further samples could not be obtained because of excessive time lag in material procurement.

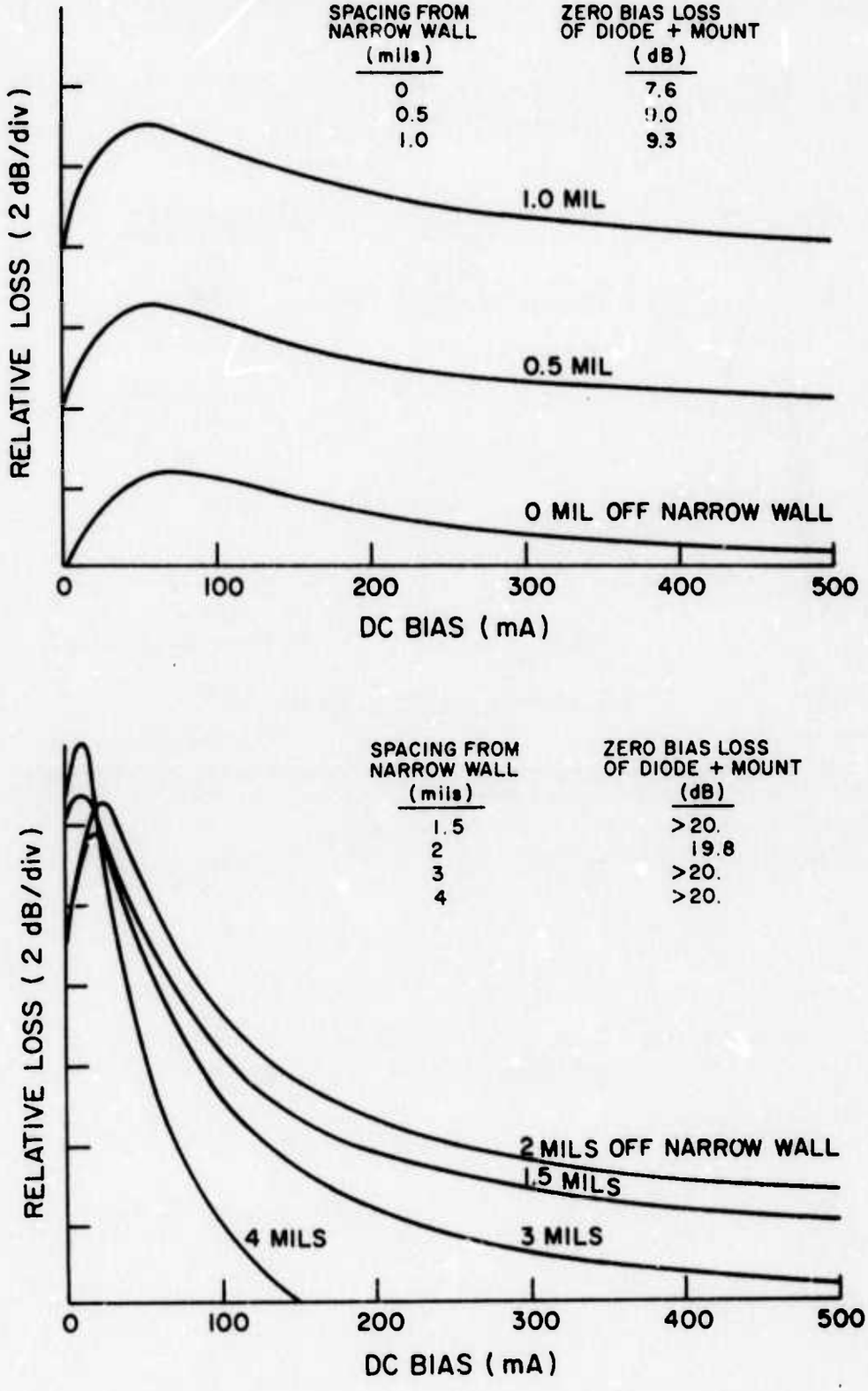


Fig. 27. Loss characteristic of diode G19-1F for various mounting positions.

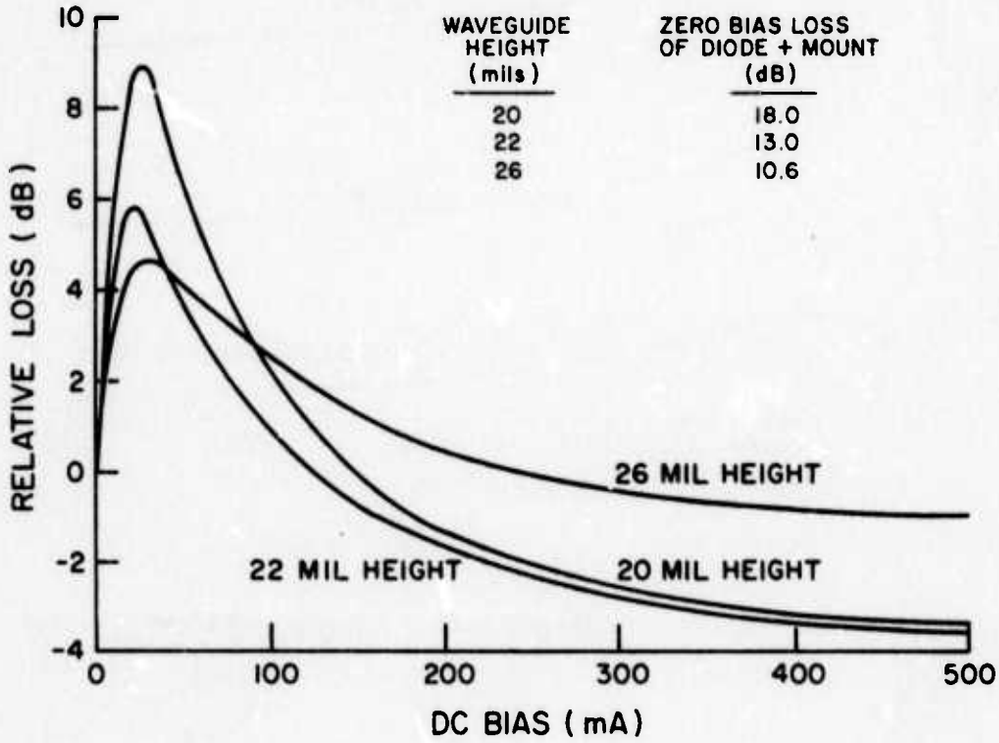


Fig. 28. Loss characteristic of diode G19-2F for various waveguide heights.

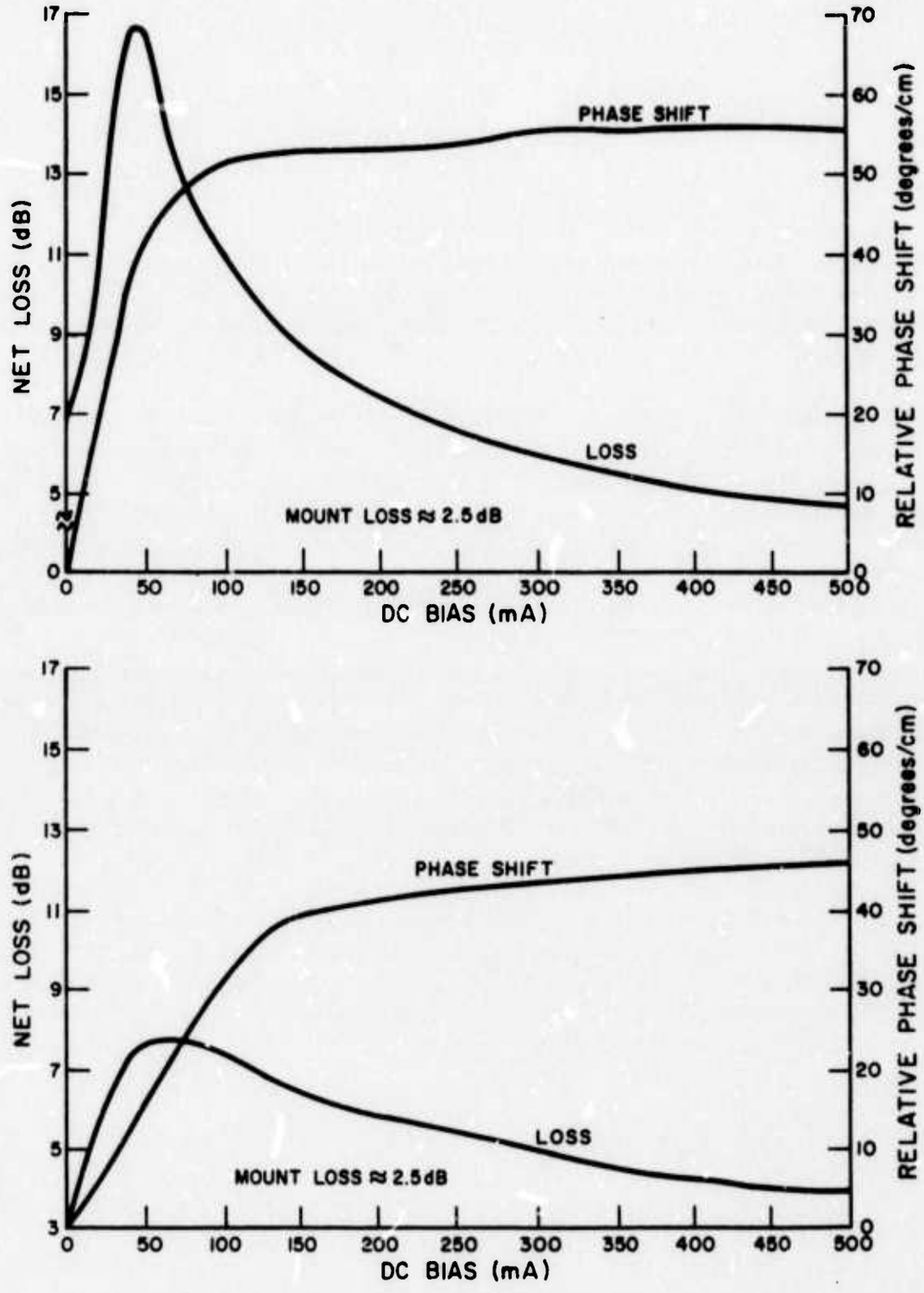


Fig. 29. Measured phase shift and insertion loss for two different PIN diodes at 140 GHz.

Section IV

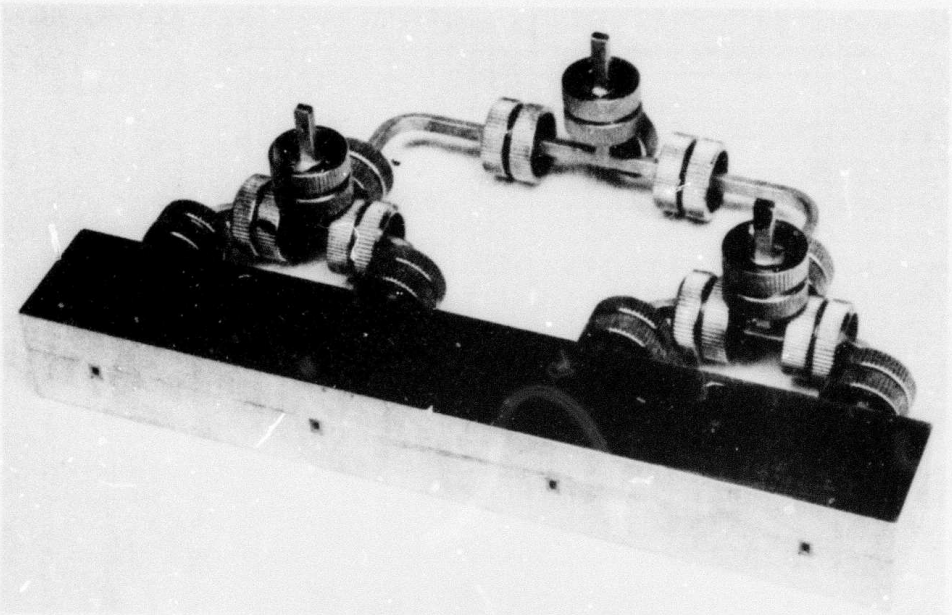
FOUR-ELEMENT ARRAY

In order to clearly demonstrate the distributed PIN diode phase shifter in operation, a four-element linear-array antenna and four 4-bit diode mounts were designed and constructed. Assembly of multibit phase shifters and antenna testing were, however, precluded by the substantial insertion loss of the diodes available for use in the array.

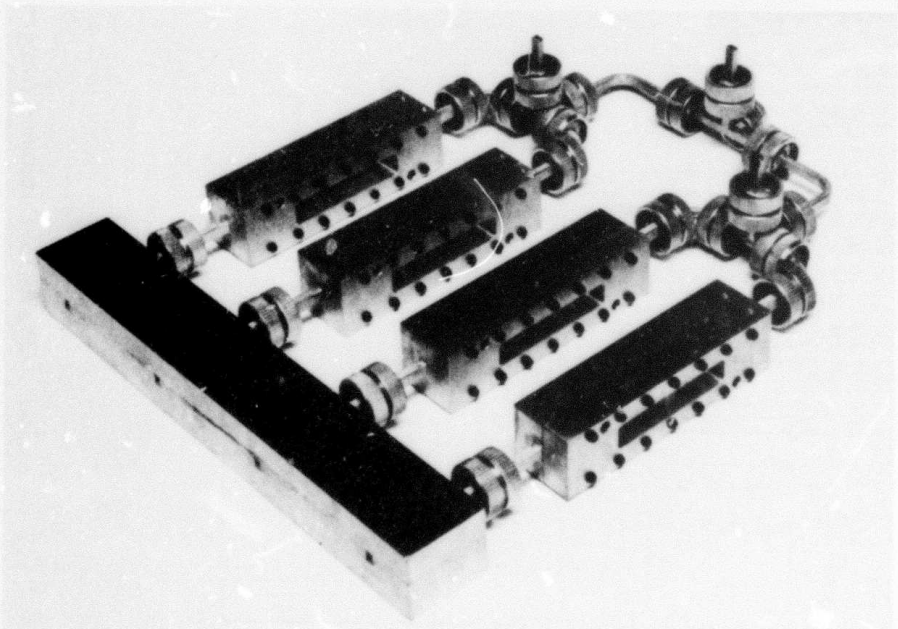
Selection of a four-element array was based on the need to limit cost and complexity. A straightforward corporate (waveguide) feed arrangement of more than four elements in RG138/U waveguide would be difficult to make to a reasonable size, and would be too lossy and too expensive. Figure 30 shows the four-element array with and without phase shifters installed. The waveguide openings on the front face are 0.04 by 0.08 in and are spaced 1.84 in apart on centers. This geometry will yield a multilobe radiation pattern with each lobe having a half-power beamwidth of about 0.6°.

Figure 31 shows the complete pattern of the array and an expanded display of the region about the central lobe, as computed by standard methods. Although 1.84 in is a rather substantial element spacing, it is the smallest spacing that could be obtained without inordinate effort in the fabrication of the feed. The commercial hybrid tees that were used were shortened as much as feasible, and special short radius bends were made.

The phase shifters are removable from the array in order to evaluate them properly. The broadside radiation pattern of the array would be measured without phase shifters in the feed section, as in Fig. 30a. Then the phase shifters would be installed and pattern measurements made at broadside and at various steering angles.

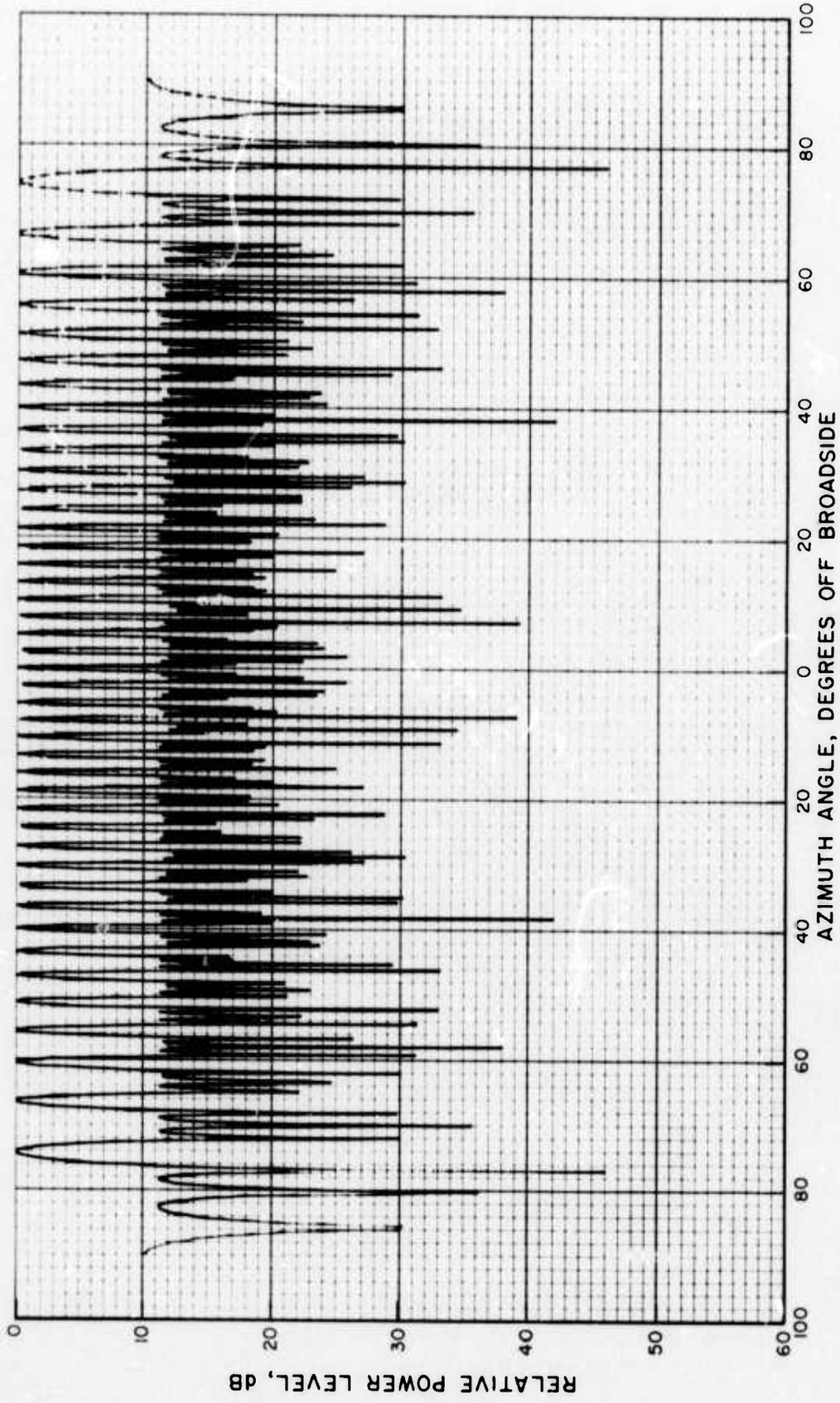


(a) Without phase shifters.



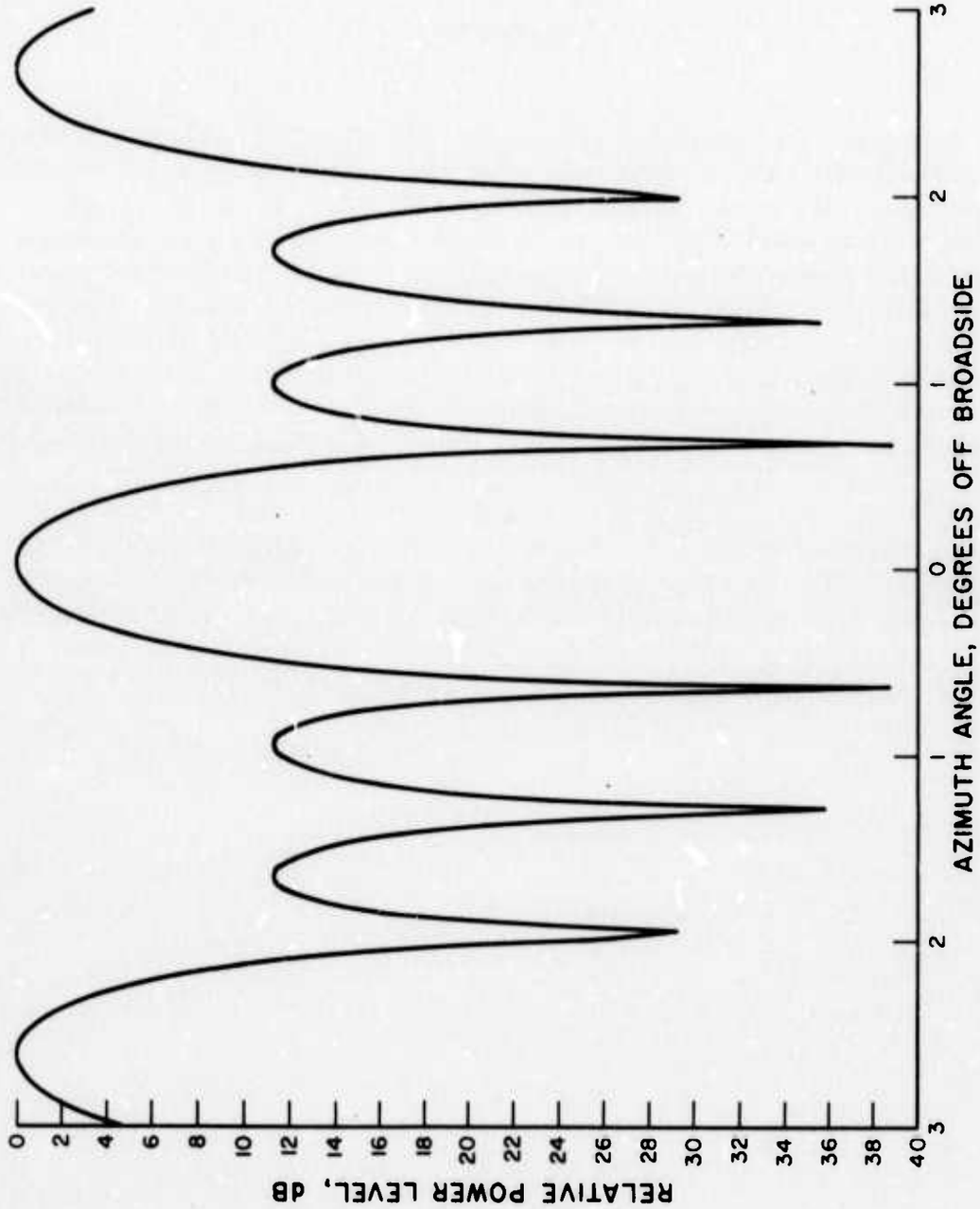
(b) With phase shifters.

Fig. 30. Four-element array.



a. Full pattern.

Fig. 31. Computed pattern of four-element array. (sheet 1 of 2)



b. Expanded portion of pattern.

Fig. 31. Computed pattern of four-element array. (sheet 2 of 2)

Section V

CONCLUSIONS

The computed RF characteristics of a silicon slab of varying conductivity, shown in Fig. 5, indicate that a phase shifter with attractive performance (i.e., 100°/dB or better) is possible. The measured data on bulk silicon slabs, shown in Fig. 14, tend to confirm the theoretical predictions and indicate that there are no fundamental reasons why a conductivity modulation phase shifter can not be built that will offer attractive performance at 140 GHz or other millimeter wave frequencies. The measured data for PIN diodes has the same form as the theoretical data. However, the similarity is only qualitative, primarily because the PIN diodes tested did not fill the entire height of the waveguide, and the conductivity modulation effect was incomplete in that it did not extend through the entire I layer due to limited excess carrier lifetime.

The work described in this report has demonstrated the potential feasibility of the distributed PIN phase shifter. In view of the promise shown by the device, it is recommended that further development of construction techniques (including stacking of diodes) be carried out in order to build phase shifters having attractive phase-shift/loss ratios.

Appendix A

COMPUTER PROGRAMS FOR

PROPAGATION ANALYSIS

PROGRAM ROOT

```
      PROGRAM ROOT
      INTEGER*2 FSTSWT
      COMPLEX GAMMA,ARG1,ARG2,WFG
      EZMUZ/8.854E-12*12.5663706*1.0E-07
      READ(5,100) A,F,ER
100   FORMAT(3(F6.4,1X))
      OMEGA=6.2831853*F*1.0E+09
      AKZSQ=OMEGA*OMEGA*EZMUZ
      A=A*0.0254
      DO 1 IT=1,25
      T=IT*A/100.0
      D=A-T
      FSTSWT=0
      WRITE(6,101) IT
101   FORMAT('1',20X,I2,' PERCENT')
      DO 1 I=0001,2001
      BETA=0.0+(I-1)*1.0
      GAMMA=CMPLX(0.0,BETA)
      ARG1=CSQRT(GAMMA*GAMMA+AKZSQ)
      ARG2=CSQRT(GAMMA*GAMMA+ER*AKZSQ)
      WFG=ARG1*CSIN(ARG2*T)/CCOS(ARG2*T)
     1   +ARG2*CSIN(ARG1*D)/CCOS(ARG1*D)
      FIMAG=AIMAG(WFG)
      FREAL=REAL(WFG)
      ASGN=SIGN(1.0,FIMAG)
      BSGN=SIGN(1.0,FREAL)
      IF(FSTSWT.EQ.0) GO TO 5
      IF(ASGN.NE.SVSGN) GO TO 2
      IF(BSGN.NE.SVSGNB) GO TO 3
      GO TO 1
2     WRITE(6,102) BETA,FIMAG,ASGN,SVSGN
102   FORMAT(21X,F5.1,5X,E11.4,2(5X,F4.1))
      GO TO 5
3     WRITE(6,102) BETA,FREAL,BSGN,SVSGNB
5     SVSGN=ASGN
      SVSGNB=BSGN
      FSTSWT=1
1     CONTINUE
      STOP
      END
```

PROGRAM WAVE

```
      PROGRAM WAVE
      EXTERNAL HEXDMP
      COMPLEX    CJ,RJ,AKZ,GAMMA,H(4),WFG
      COMPLEX    CZ
      IMPLICIT REAL   (A-H,O-Z)
      REAL   PI(4),Q(4)
      INTEGER*2 FSTSWT,IFREQ,NI,NIT
      COMMON/CMPX/AKZ,CJ,RJ
      COMMON/REL/PI,AKZSQ,T,A,D
C
C     FORMAT STATEMENTS
C
100   FORMAT(F6.4,1X,3(F5.1,1X),4(I3,1X))
101   FORMAT('1',36X,'FREQUENCY=',I3,' GHZ')
102   FORMAT('0',60X,'T/A=',F5.3)
103   FORMAT('0',30X,'SIGMA',14X,'ALPHA',10X,'BETA',16X,'R(F)',11X,'I(F)')
104   FORMAT(' ',27X,F8.1,10X,2(F9.2,5X),2(5X,E10.3))
105   FORMAT('+',13X,'REFERENCE'//)
106   FORMAT('1')
C
C     READ PARAMETERS AND INITIALIZE
C
1     READ(5,100,END=21) A,F,ER,HR,NIT
      A=A*0.0254
      CJ=(0.0,1.0)
      RJ=(1.0,0.0)
      CZ=(0.0,0.0)
      PI(1)=3.1415927
      PI(2)=6.2831853
      PI(3)=9.4247780
      PI(4)=12.5663706
      OMEGA=PI(2)*F*1.0E+09
      EZMUZ=8.854E-12*PI(4)*1.0E-07
      AKZSQ=OMEGA*OMEGA*EZMUZ
C
C     START SIGMA LOOP
C
25    SIGMA=0.0
      SINC=0.1
      FSTSWT=0
C
C     COMPUTE W FOR SIGMA=0
C
      AKZ=ER
      CALL RARITZ(TI,GAMMA,NDIT)
      IF(NDIT.EQ.1) GO TO 1
      T=TI*A/100.
      D=A-T
      CALL WF(GAMMA,CZ,QLOW,WFG)
C
```

PROGRAM WAVE (cont.)

```
C       COMPUTE Q(+H),Q(+IH),Q(-H),Q(-IH)
C
4       J=0
        QLIM=0.01
        H(1)=RJ*HR
        H(2)=CJ*HR
        H(3)=-RJ*HR
        H(4)=-CJ*HR
6       J=J+1
8       NI=0
        DO 5 I=1,4
        CALL WF(GAMMA,H(I),Q(I),WFG)
        IF(Q(I).LT.QLOW) GO TO 3
        GO TO 5
3       QLOW=Q(I)
        NI=I
5       CONTINUE
        IF(NI.EQ.0) GO TO 7
        IF(QLOW.LT.QLIM) QLIM=QLOW
        GAMMA=GAMMA+H(NI)
        GO TO 8
7       IF(J.EQ.NIT) GO TO 10
        DO 9 I=1,4
9       H(I)=H(I)/10.0
        GO TO 6
10      IF(FSTSWT.NE.0) GO TO 15
        FSTSWT=1
C
C       WRITE HEADERS AND REFFRENCE VALUES
C
        IFREQ=F
        WRITE(6,101) IFREQ
        TR=T/A
        WRITE(6,102) TR
        WRITE(6,103)
        ALPHRF= REAL(GAMMA)*0.08683
        BETARF=AIMAG(GAMMA)*0.573
        CALL WF(GAMMA,CZ,W,WFG)
        FREAL= REAL(WFG)
        FCMPX=AIMAG(WFG)
        WRITE(6,104) SIGMA,ALPHRF,BETARF,FREAL,FCMPX
        WRITE(6,105)
        LCNT=10
C
C       WRITE COMPUTED VALUES
C
15      ALPHA= REAL(GAMMA)*0.08683-ALPHRF
        BETA=AIMAG(GAMMA)*0.573-BETARF
        CALL WF(GAMMA,CZ,W,WFG)
        FREAL= REAL(WFG)
```

PROGRAM WAVE (cont.)

```
      FCMPX=AIMAG(WFG)
      WRITE(6,104) SIGMA,ALPHA,BETA,FREAL,FCMPX
      LCNT=LCNT+1
      IF(LCNT.EQ.55) WRITE(6,106)
C
C     INCREMENT SIGMA
C
      IF( ABS(SIGMA-1.).LT.0.01) SINC=1.
      IF( ABS(SIGMA-10.).LT.0.1) SINC=10.
      IF( ABS(SIGMA-100.).LT.1.) SINC=100.
      IF( ABS(SIGMA-1000.).LT.10.) SINC=1000.
      IF( ABS(SIGMA-10000.).LT.100.) SINC=10000.
      IF( ABS(SIGMA-100000.).LT.1000.) GO TO 25
      SIGMA=SIGMA+SINC
      AKZ=ER-CJ*SIGMA/(8.854E-12*OMEGA)
      CALL WF(GAMMA,CZ,QLOW,WFG)
      GO TO 4
21    STOP
      END
```

PROGRAM WAVE, SUBROUTINE RARITZ

```
      SUBROUTINE RARITZ(TI,GAMMA,NDIT)
      COMPLEX GAMMA
      NDIT=0
      READ(5,100,END=99) TI,BETA
100   FORMAT(F4.1,1X,F7.1)
      GAMMA=CMPLX(0.0,BETA)
      RETURN
99    NDIT=1
      RETURN
      END
```

PROGRAM WAVE, SUBROUTINE WF

```
      SUBROUTINE WF(GAMMA,H,W,WFG)
C
C     WF COMPUTES |F(GAMMA)|**2
C
      COMMON/CMPX/AKZ,CJ,RJ
      COMMON/REL/PI,AKZSQ,T,A,D
      COMPLEX    ARG1,ARG2,GAMMA,H,AKZ,WFG,CJ,RJ
      REAL   PI(4),AKZSQ,T,A,D,W
      ARG1=CSQRT ((GAMMA+H)*(GAMMA+H)+AKZSQ)
      ARG2=CSQRT ((GAMMA+H)*(GAMMA+H)+AKZ*AKZSQ)
      WFG=ARG1*CSIN (ARG2*T)/CCOS (ARG2*T)
     1   +ARG2*CSIN (ARG1*D)/CCOS (ARG1*D)
      W= REAL(WFG)* REAL(WFG)+AIMAG(WFG)*AIMAG(WFG)
      RETURN
      END
```

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