PULSED-POWER BURNOUT OF INTEGRATED CIRCUITS

R. H. Vandre

Aerospace Corporation

Prepared for:

Air Force Systems Command

15 August 1972

AIR FORCE REPORT NO.
SAMSO-TR-72-226

AEROSPACE REPORT NO.
TR-0073(3124)-1

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Prepared by R. H. VANDRE
Plasma Research Laboratory
Laboratory Operations

72 AUG 15

Technology Division
THE AEROSPACE CORPORATION

Prepared for SPACE AND MISSILE SYSTEMS ORGANIZATION
AIR FORCE SYSTEMS COMMAND
LOS ANGELES AIR FORCE STATION
Los Angeles, California

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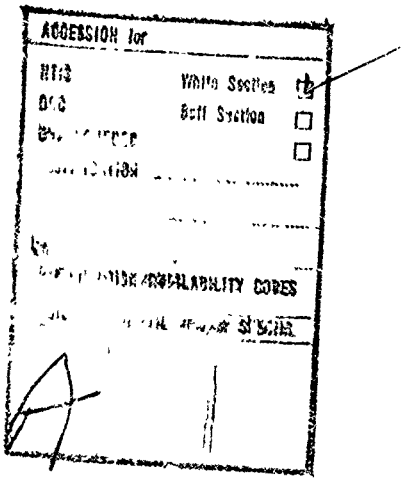

UNCLASSIFIED
Security Classification

DOCUMENT CONTROL DATA - R & D
(Security classification of title, body of abstract and indexing annotation must be entered when the overall report is classified)

1. ORIGINATING ACTIVITY (Corporate author) The Aerospace Corporation El Segundo, California	2a REPORT SECURITY CLASSIFICATION Unclassified 2b GROUP

3. REPORT TITLE
Pulsed-Power Burnout of Integrated Circuits

4 DESCRIPTIVE NOTES (Type of report and inclusive dates)

5 AUTHOR(S) (First name, middle initial, last name)
Robert H. Vandre

6 REPORT DATE	7a TOTAL NO. OF PAGES	7b NO. OF REFS
72 AUG 15	38 42	1

8a CONTRACT OR GRANT NO.	9a ORIGINATOR'S REPORT NUMBER(S)
F04701-72-C-0073 b PROJECT NO.	TR-0073(3124)-1
c	9b OTHER REPORT NO(S) (Any other numbers that may be assigned this report)
d	SAMSO-TR-72-226

10. DISTRIBUTION STATEMENT
Approved for public release; distribution unlimited.

11. SUPPLEMENTARY NOTES	12. SPONSORING MILITARY ACTIVITY
	Space and Missile Systems Organization Air Force Systems Command Los Angeles Air Force Station

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DD FORM 1473 (FACSIMILE)

UNCLASSIFIED
Security Classification

14 KEY WORDS

EMP
Integrated circuit pulse burnout
Junction burnout
Wunsch-Bell theory

Distribution Statement (Continued)

Abstract (Continued)

Air Force Report No.
SAMSC-TR-72-226

Aerospace Report No.
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FOREWORD

This report is published by The Aerospace Corporation, El Segundo, California, under Air Force Contract No. F04701-72-C-0073.

This report, which documents research carried out from September 1971 through March 1972, was submitted on 15 August 1972 to Major James H. Heilman, DYX, for review and approval.

The author is grateful to Dr. V. Josephson for his encouragement and support during the course of this work and to R. Marshall for his technical support.

Approved

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Technology Division

Publication of this report does not constitute Air Force approval of the report's findings or conclusions. It is published only for the exchange and stimulation of ideas.

James H. Heilman, Major, USAF
Survivability Directorate

ABSTRACT

Results of pulsed-power burnout testing of the Fairchild 9046 quad dual-input nand gate and the Amelco 6041 dual three-input nand gate showed the circuits to be vulnerable to junction burnout for pulses of less than 100 V and pulse widths on the order of 100 nsec. Calculations based on Wunsch-Bell junction burnout theory showed good agreement with the experimental results. Sample calculations applying Wunsch-Bell theory to integrated circuits are given.

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FIGURES

FIGURES (Concluded)

I. INTRODUCTION

An important long-range mechanism by which satellite electronics can be adversely affected is the electromagnetic pulse (EMP) associated with nuclear detonations occurring above the atmosphere. This pulse can couple directly into the satellite antennas proper or, through slots in the satellite structure, into unshielded wires leading directly to electronics boxes. The magnitude of the voltage transients generated in the electronics and the hardness of the electronics determine the vulnerability of the electronics to burnout. The theoretical model used in prediction of semiconductor junction burnout voltages is that developed by Wunsch and Bell.[1] This theory predicts the power level per unit area for a given pulse width necessary to heat a semiconductor junction to the melting point of silicon. Extensive tests were conducted by Wunsch and Bell on discrete transistors and diodes, and agreement was obtained with the theory. A major conclusion of their work was that burnout comes at a power level between that predicted by theory and a level one tenth as high. This result is explained by photomicrographs of the semiconductor junctions, which showed that melting of the junction usually occurred at isolated spots that covered only a fraction of the junction area.

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[1] D. L. Wunsch and R. R. Bell, "Determination of Threshold Failure Levels of Semiconductor Diodes and Transistors Due to Pulsed Voltages," IEEE Trans. Nucl. Sci. NS-15, 244 (1968).

Wunsch-Bell theory is used extensively to predict the burnout levels of discrete components but is seldom used on integrated circuits because of the difficulty involved in determination of device parameters, such as junction area and doping levels. This report is an account of measurements of EMP burnout levels for two integrated circuits, the Fairchild 9046 quad dual-input nand gate and the Amelco 6041 dual three-input nand gate. These circuits utilize standard low-power Transistor-Transistor Logic (TTL) design techniques and are used extensively in spacecraft because of their low power consumption ($\sim$1 mW). Because of their function, these circuits are used in positions in spacecraft where they are subjected to the EMP environment. This report presents experimental data and Wunsch-Bell predictions of the burnout levels for comparison purposes. Sample calculations and a comparison between the Wunsch-Bell theory and experimental values are included.

II. WUNSCH-BELL THEORY

Wunsch-Bell theory can be a useful tool for prediction of burnout of integrated circuits. To use it effectively, one must make an accurate estimate of the power dissipated in the vicinity of the semiconductor junction under consideration.

The Wunsch-Bell burnout model predicts the pulsed power level per unit area necessary to raise a semiconductor junction to the melting temperature. It is assumed that when the junction reaches this temperature it will fail. The model uses linear heat-flow theory to derive the following junction failure relation[2]

$$\frac{P}{A} = \sqrt{\pi k \rho c_p}\left[T_m - T_i\right] t^{-1/2}$$

where P is the power, A the junction area, k the thermal conductivity, ρ the density, c_p the specific heat, T_m the failure temperature, T_i the initial temperature, and t the time. Figure 1 is a graph of P vs A for silicon at room temperature.

The value of P to be used in the above equation must be determined with care. Only power dissipated in the immediate vicinity of the junction will contribute toward raising its temperature to the melting point. Power is dissipated in a semiconductor device either (1) across the junction itself

$$P = IV$$

where V is either the forward voltage drop or the reverse breakdown voltage, depending on the polarity of the pulse; or (2) in the bulk resistance R_{BULK}

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[2] See Footnote 1.

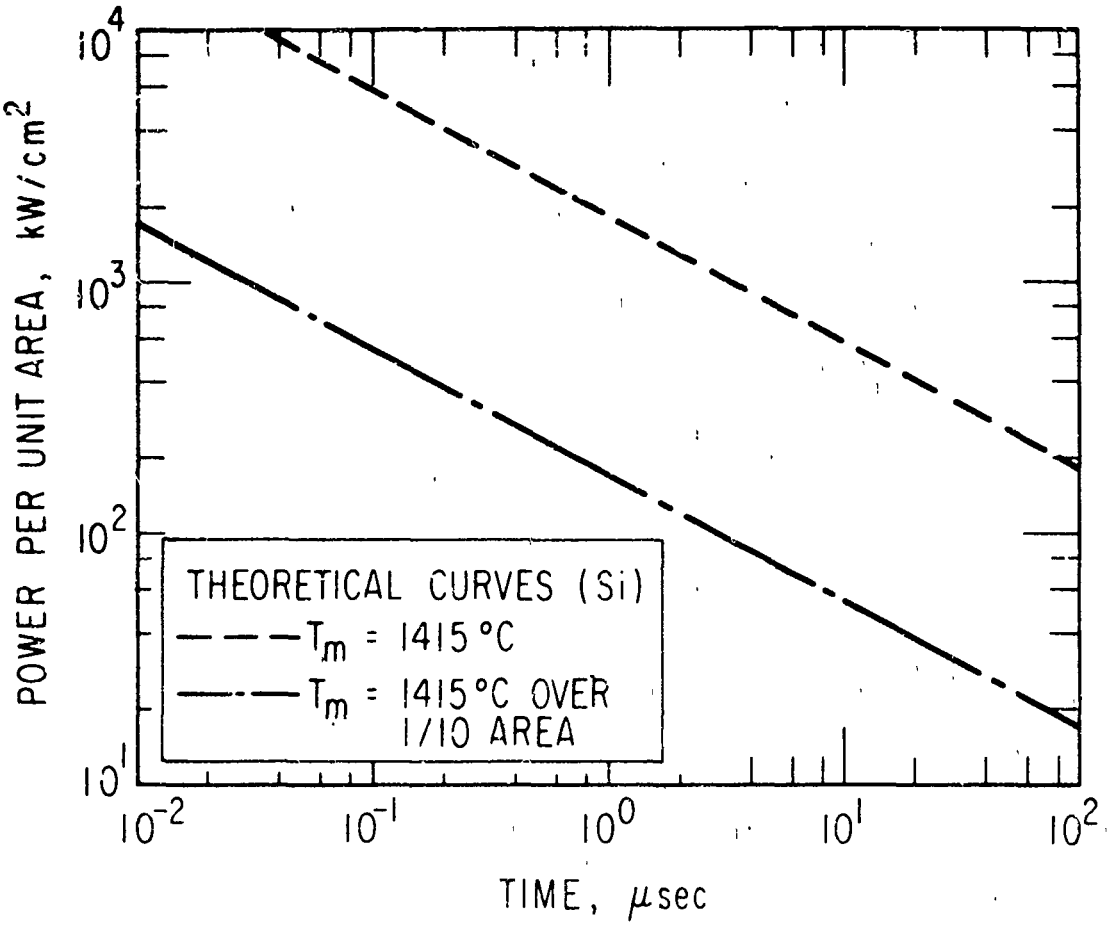


Figure 1. Wunsch-Bell Burnout Limits for Silicon

of the device

$$P = I^2 R_{BULK}$$

Power dissipated across the junction should clearly be included in calculation of burnout by the Wunsch-Bell theory. The situation is not so clear with regard to power dissipated in the bulk resistance. For current flowing from emitter to collector, most of the bulk resistance is in the collector and, therefore, far away from the junction. In this situation one would not include the $P = I^2 R_{BULK}$ term. Conversely, if one were considering a current path from base to emitter or base to collector, the $P = I^2 R_{BULK}$ term (R_{BULK} is the bulk resistance of the base) should usually be included. For a more complete explanation of the application of Wunsch-Bell theory to circuits, see Appendix A.

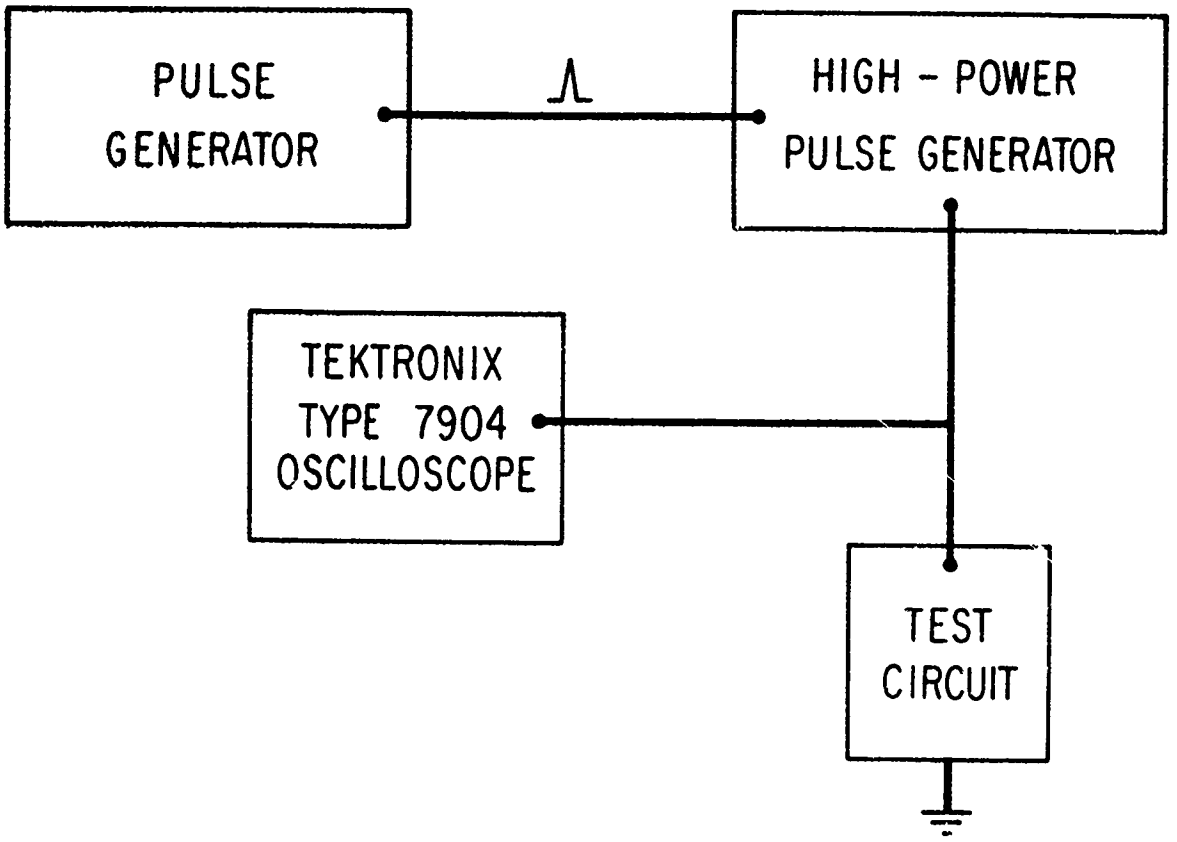


Figure 2. Experimental Setup

III. EXPERIMENTAL APPARATUS

A. TEST SETUP

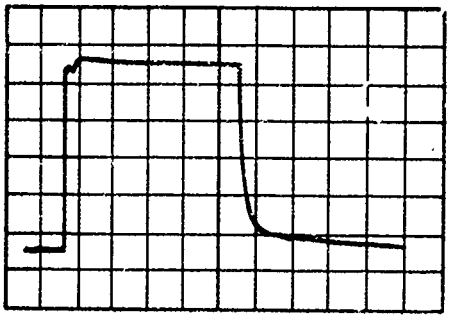
The basic electrical test setup is shown in Figure 2. A single-pulse generator was used to trigger the high-power pulser. The pulse from the high-power pulser was then fed into the test circuit and measured by a Tektronix 7904 oscilloscope (the risetime of the scope and amplifier is 0.8 nsec).

The high-power pulser used five MPSU 04 transistors avalanched in series to obtain square pulses of from 100 to 450 V across 50 Ω with a risetime of approximately 1 nsec. For longer pulses of lower voltage, an emitter follower circuit with a TIP 33A power transistor was used to amplify an input square pulse. Pulses with amplitudes ranging from 1 to 60 V (across as little as 10 Ω) and with risetimes of approximately 80 nsec were obtained.

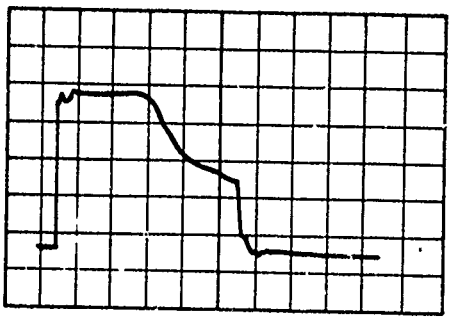
B. EXPERIMENTAL PROCEDURE

Each device was thoroughly checked for performance before burnout testing was initiated. After each high-power pulse, the device was tested for failure, which consisted of either a change in risetime or a change in logic voltage. The pulses started at low voltage and increased until failure occurred. After a failure had occurred, the cover was taken off the chip and a photomicrograph was made to determine the type of damage mechanism.

A typical pulse without a load can be seen in Figure 3a. Figure 3b shows the same pulse across an integrated circuit under test. Note that the maximum amplitude of the pulse across the test circuit is lower than the amplitude of the unloaded pulse. This happens because the circuit under



a. Unloaded Pulse



b. Pulse Across Integrated Circuit

Figure 3. Pulses from High-Power Pulser

test tends to load down the pulser. Figure 3b shows that, after ~40 nsec, the integrated circuit breaks down and loads the pulser even more.

In the calculations on the basis of the Wunsch-Bell model a constant voltage across the device for the duration of the pulse was assumed. Accordingly, the voltage reported for burnout is the average voltage across the junction during the high-power pulse. In most cases the peak voltage was ~40 to 50 percent higher.

Table 1. Burnout Voltages

Fairchild 9046 Quad Dual-Input Nand Gate				
Pulse On	Pulse Width, nsec	Average Pulse, V	Wunsch-Bell Total Junction Predicted Melt, V	Failure Mode
Power supply	100	+400	700	Metallization burnout
Input (with other input at ground)	60	+105	150	Input diode burnout
	110	+95	125	Input diode burnout
	125	+100	120	Input diode burnout
Input (with other input floating)	25	-120	250	Inner transistor burnout
	100	-100	150	Inner transistor burnout
	640	-65	85	Inner transistor and input diode burnout
Output	25	+115	200	Output transistor burnout
	60	+58	140	Output transistor burnout
	100	+48	110	Output transistor burnout
	640	+34	50	Output transistor burnout
Amelco 6041 Dual Three-Input Nand Gate				
Pulse On	Pulse Width, nsec	Average Pulse, V	Wunsch-Bell Total Junction Predicted Melt, V	Failure Mode
Input (with other input floating)	25	115	350	Inner transistor and input diode burnout
	100	+72	210	Inner transistor and input diode burnout
Output	25	+72	430	Metallization burnout
	100	+30	230	Output transistor burnout
	1500	+35	77	Output transistor burnout
	11,000	+25	34	Output transistor burnout

IV. RESULTS AND CONCLUSIONS

The results of pulsed voltage testing of the Fairchild 9046 quad dual-input nand gate and the Amelco 6041 dual three-input nand gate showed good agreement with Wunsch-Bell theory. In almost all cases, the voltage required for junction burnout lay between the 1/10 junction melt and total junction melt curves. Photomicrographs of the burned-out circuits showed that, in all but two instances, junction burnout occurred In the two isolated instances, metallization burnout was the cause of failure.

A list of the devices tested and their burnout voltages is given in Table 1. In addition, Wunsch-Bell calculations for the different test configurations were performed. The results of these calculations can be seen in Figures 4-8.

Comparisons of experimental data and Wunsch-Bell theory show good agreement when the theory is extended to integrated circuits. The results also show that burnout almost always occurs at a level greater than the 1/10 junction melt level. Therefore, one could use Wunsch-Bell calculations in actual practice to see which circuits of a system under study might be stressed to the 1/10 junction melt level, and the exact burnout levels of these circuits could be determined by bench testing.

The difficulty of using Wunsch-Bell theory for integrated circuits is in the determination of necessary parameters for calculation: the resistivity of the collector, the base sheet resistance, the buried layer sheet resistance, the depth of the buried layer, the depth of the emitter,

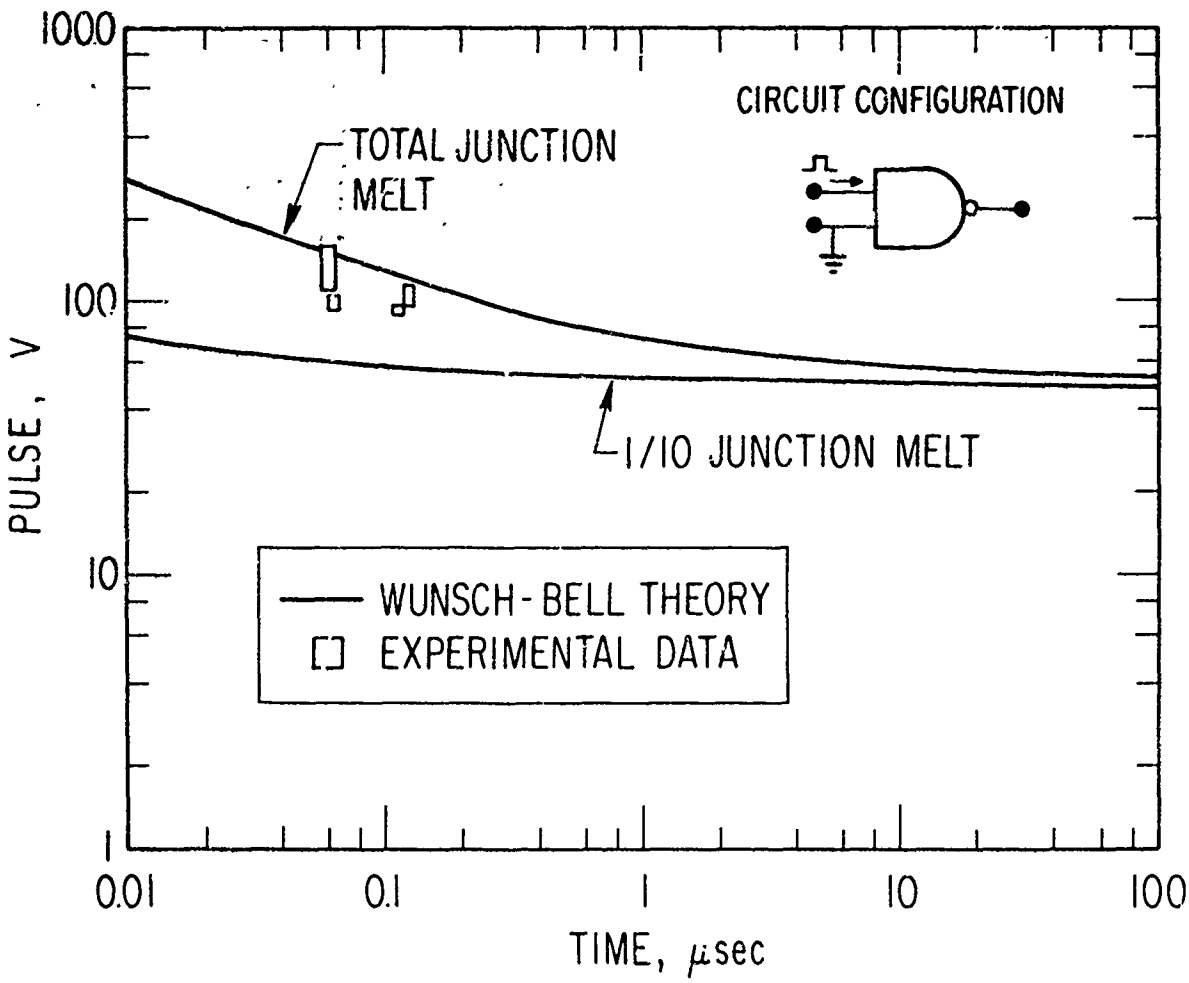


Figure 4. Comparison of Wunsch-Bell Theory and Experiment for Fairchild 9046 Nand Gate with Positive Pulse on Input with Other Input at Ground

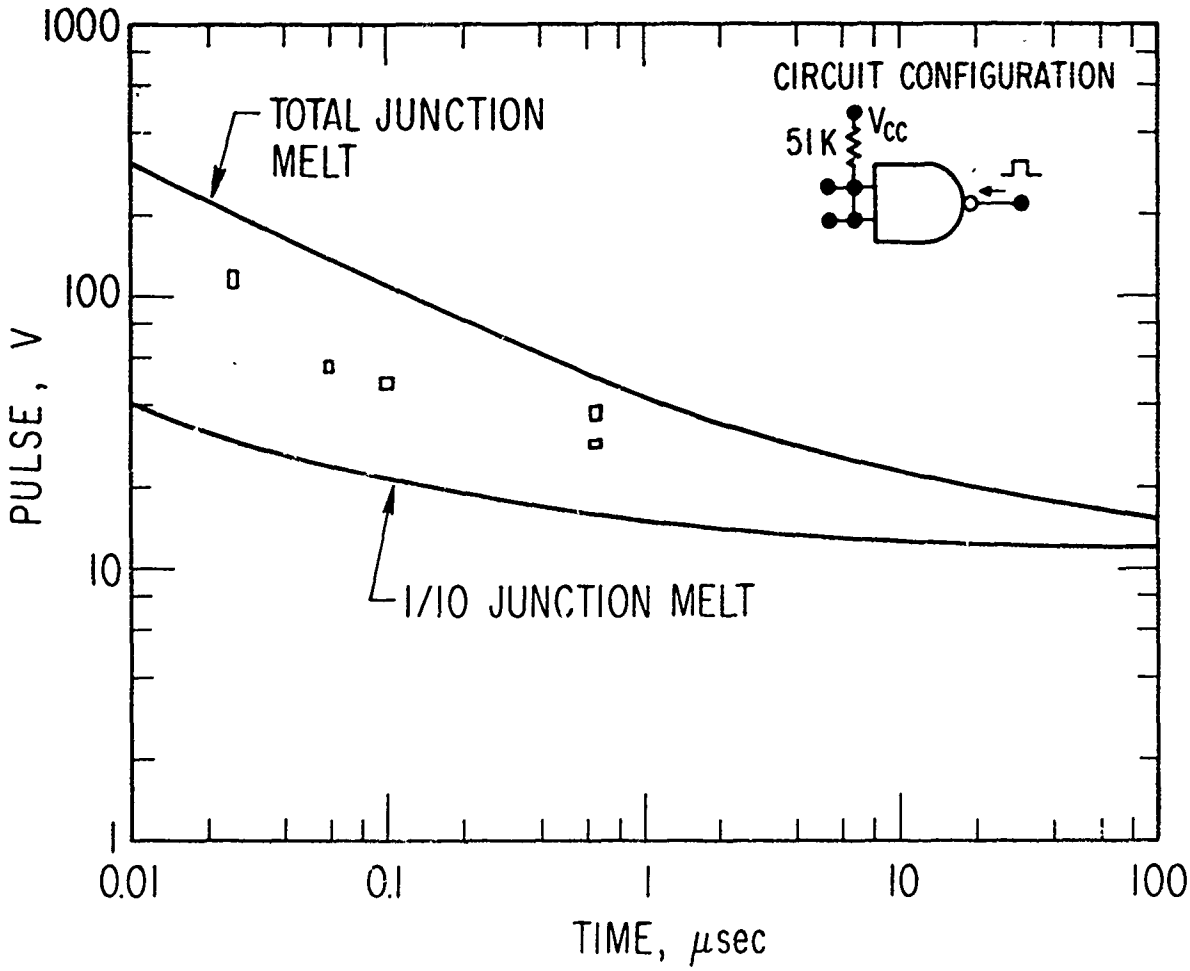


Figure 5. Comparison of Wunsch-Bell Theory and Experiment for Fairchild 9046 Nand Gate with Positive Pulse on Output

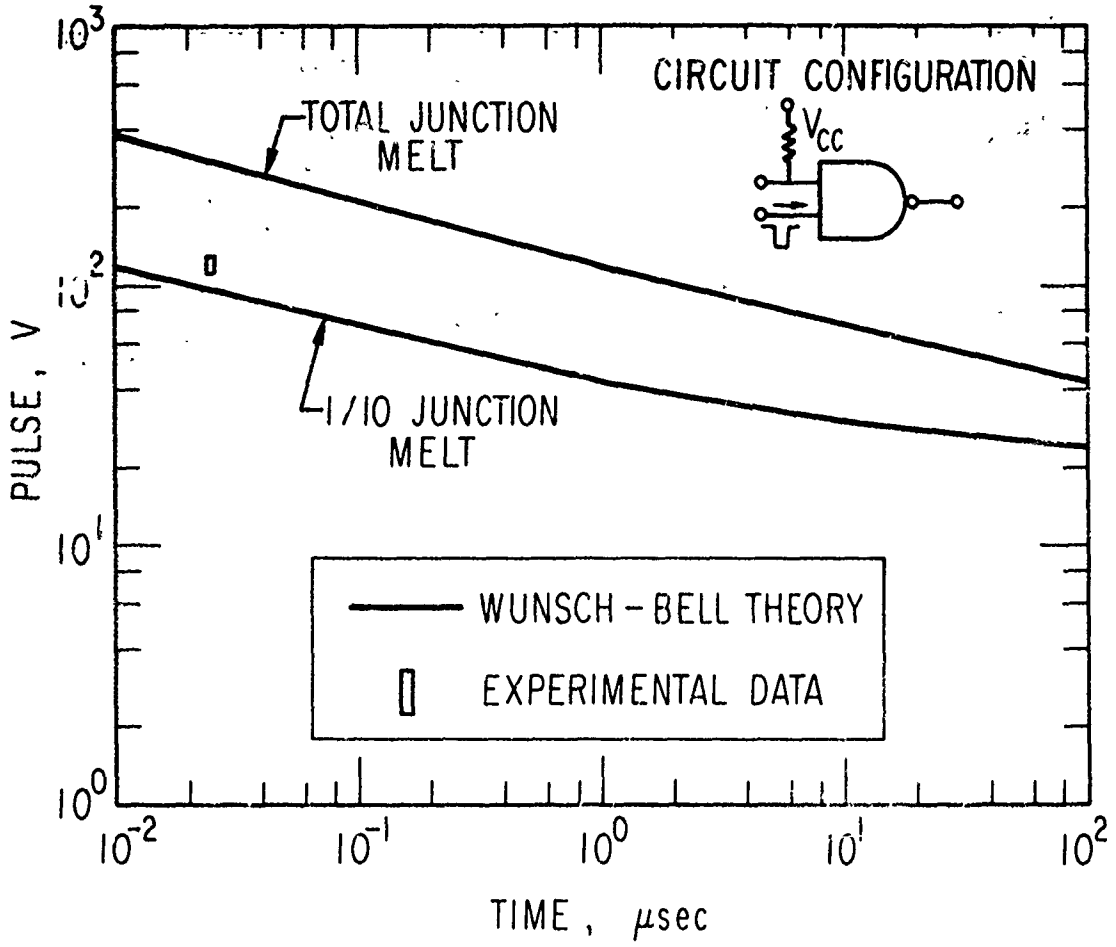


Figure 6. Comparison of Wunsch-Bell Theory and Experiment for Amelco 6041 Nand Gate with Negative Pulse on Input

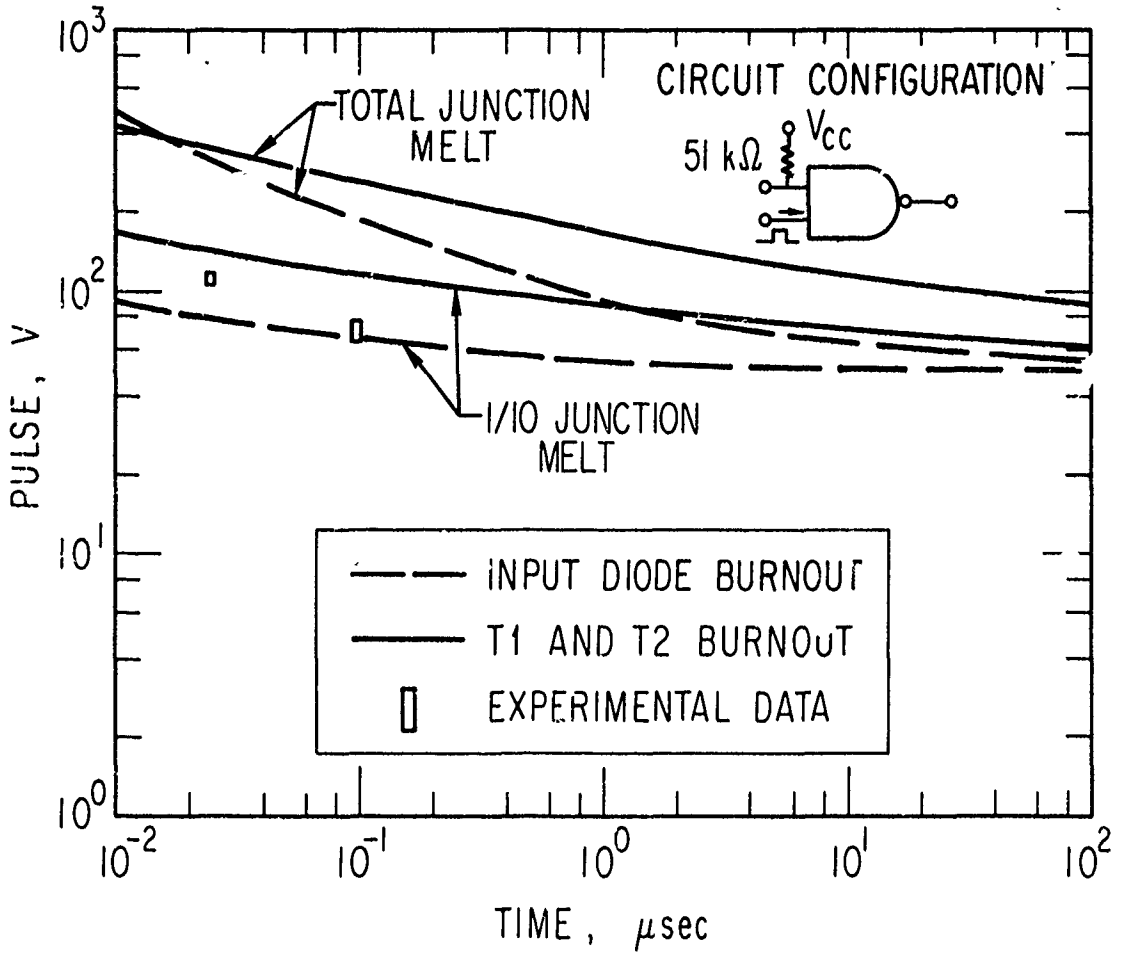


Figure 7. Comparison of Wunsch-Bell Theory and Experiment for Amelco 6041 Nand Gate with Positive Pulse on Input

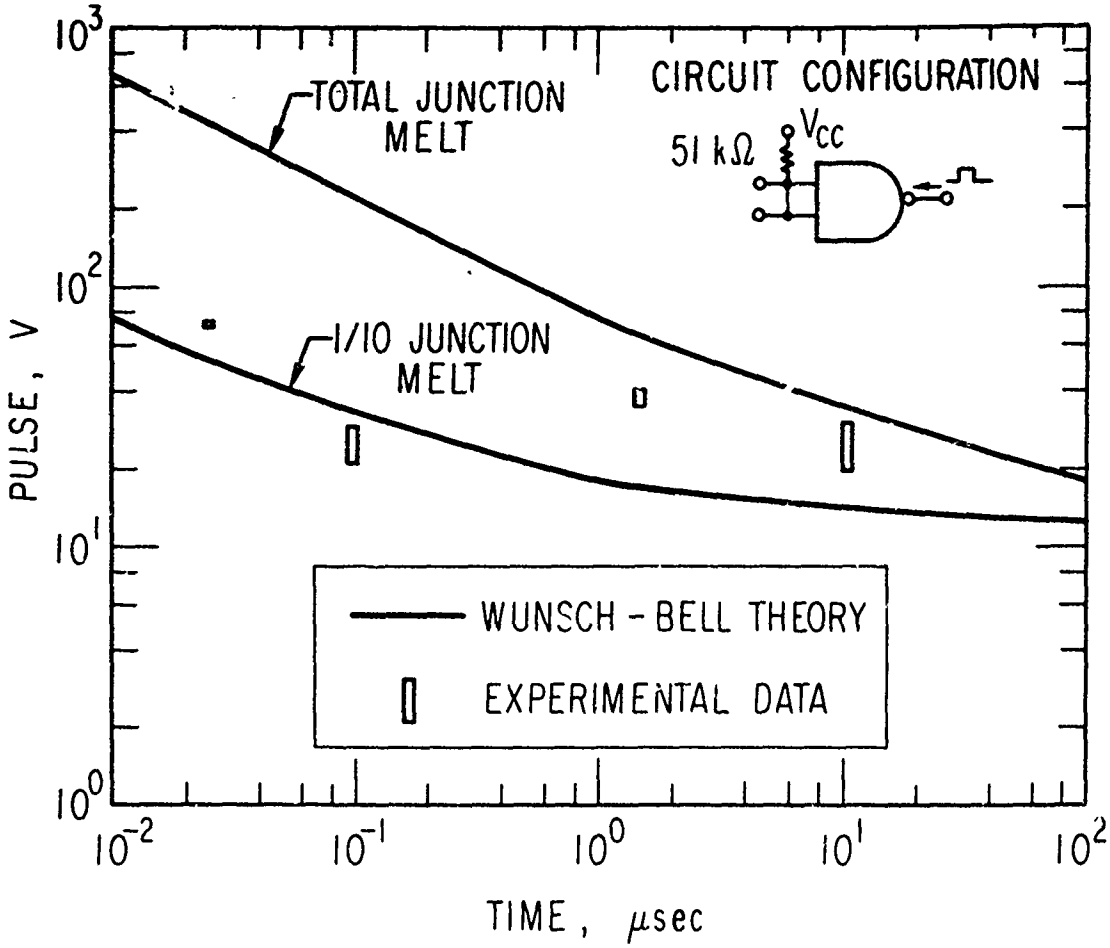
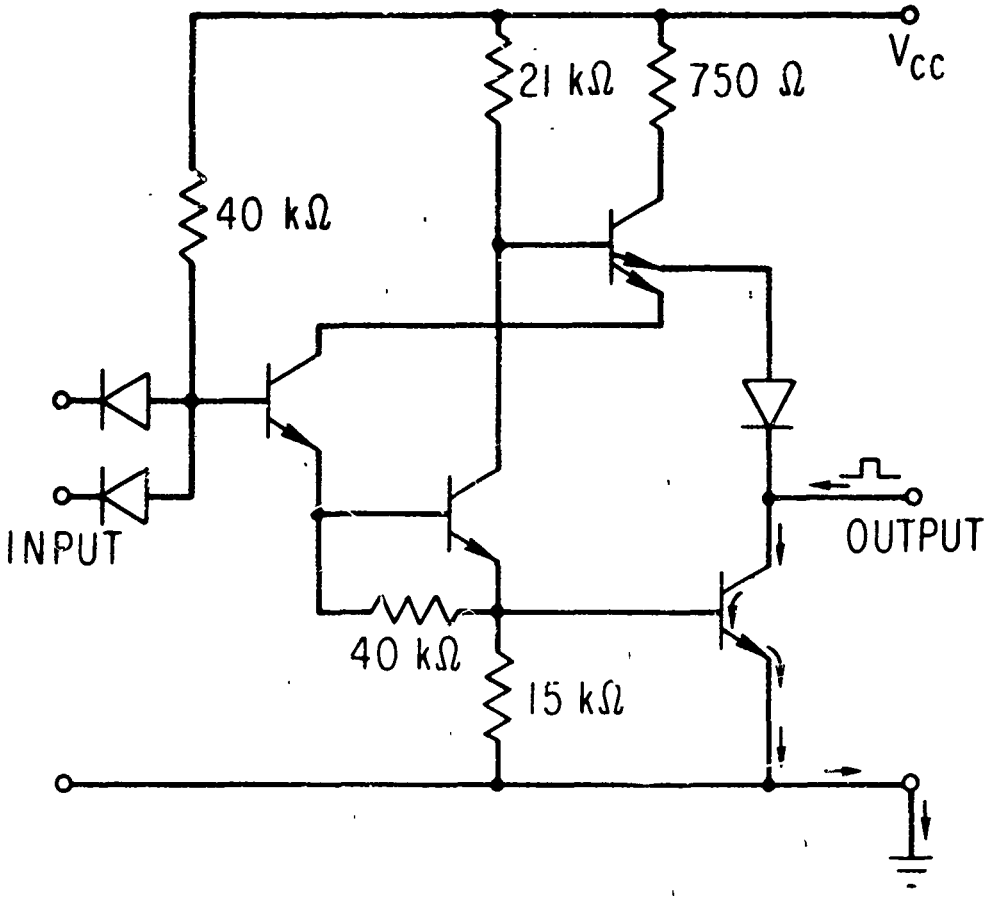


Figure 8. Comparison of Wunsch-Bell Theory and Experiment for Amelco 6041 Nand Gate with Positive and Negative Pulses on Output

the depth of the base, and the junction areas. Once these parameters are determined, the calculations are straightforward. Sample Wunsch-Bell calculations are given in Appendix A.



CIRCUIT CHARACTERISTICS		
BV_{CEO} =	8 V MIN.;	12-15 V TYPICAL
BV_{EBO} =	6 V MIN.;	7-8 V TYPICAL
BV_{CBO} =	40 V MIN.;	50 V TYPICAL
ρ_c =	0.2 Ω - cm	
$R_{BURIED\ LAYER}$ =	3 Ω / SQUARE	

Figure 9. Circuit Diagram for One Channel of the Fairchild 9046 Quad Dual-Input Nand Gate

APPENDIX A. WUNSCH-BELL CALCULATIONS FOR A PULSE APPLIED TO THE OUTPUT OF THE FAIRCHILD 9046 NAND GATE

The circuit diagram is shown in Figure 9. Because of the resistors going up to the power supply, the main current path is through the output transistor. The geometry of the output transistor is shown in Figure 10. Calculations of burnout of a specific active element depend on the ability of the power dissipated in the bulk resistance to add to heating effects at the junction. In the case of the output transistor, most of the bulk resistance is located in the collector. Therefore, most of the power dissipated in the bulk resistance of the device is too far removed from the junction to cause significant heating of the junction during a short pulse. The power dissipated at the junction is therefore

$$P = IV \tag{A. 1}$$

where V is the voltage drop across the transistor. It is obvious that this V term will be largest when the junction is broken down in the reverse direction. In this case, large currents can be drawn that are limited only by the sum of the bulk resistance and metallization resistance of the device.

Figure 9 shows that, for a current path going through the output transistor, where the transistor is broken down in the reverse direction, the current is

$$I = (V - BV_{CEO})/R_T \tag{A.2}$$

The difficulty in application of Wunsch-Bell theory is the determination of the value for the bulk resistance. Because it is usually impossible

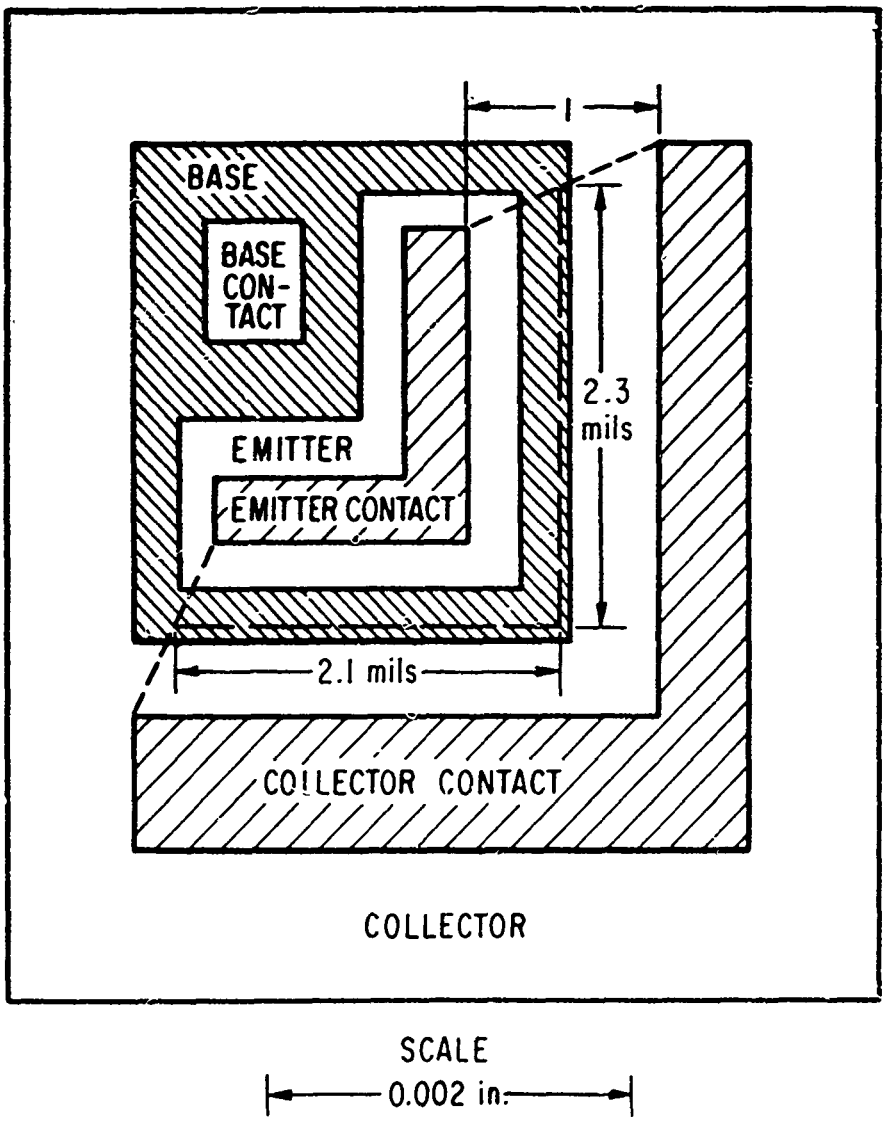


Figure 10. Output Transistor Geometry of Fairchild 9046 Quad Dual-Input Nand Gate

to measure bulk resistance in integrated circuits, and because the manufacturers usually don't supply information on such parameters, it is necessary to calculate these resistances. The resistance of the device is broken down into three components, which are shown in Figure 11.

The up-down resistance (R_{UD}) and the down-up resistance (R_{DU}) are calculated from the equation

$$R = \frac{\rho_c \ell}{A}$$

where R is resistance in ohms, ρ_c is collector resistivity, ℓ is length of current path, and A is the cross-sectional area. Figure 11 shows that A for R_{UD} is just the area of the collector contact. Therefore

$$A = (3.4)(0.7) + (0.5)(3.6) = 4.2 \text{ mil}^2 = 2.7 \times 10^{-5} \text{ cm}^2$$

From Figure 11, we find $\ell = 5$ μm and $\rho_c = 0.2$ Ω-cm. Therefore, the resistance is

$$R_{UD} = \frac{(0.2)(5 \times 10^{-4})}{2.7 \times 10^{-5}} \approx 4 \Omega$$

Similarly, in the calculation of R_{DU} A is the area of the emitter and $\ell = 5 \times 10^{-4}$ cm. Therefore the down-up resistance

$$R_{DU} = \frac{(0.2)(5 \times 10^{-4})}{1.8 \times 10^{-5}} \approx 4.4 \Omega$$

The resistance through the buried layer (R_{across}) is a function of the sheet resistivity of the layer measured in ohms/square. The number of squares involved is the length of the current path divided by the width. For example, in Figure 12 the number of squares is three.

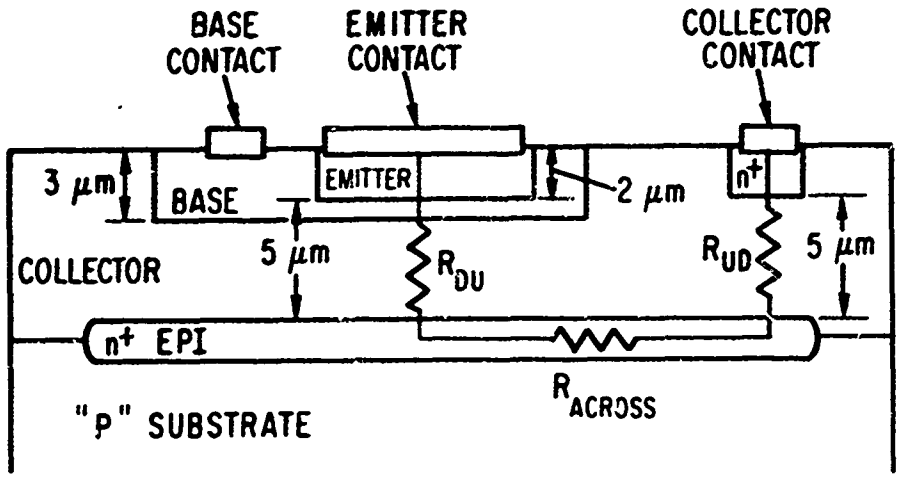


Figure 11. The Three Contributions to the Bulk Resistance of a Transistor

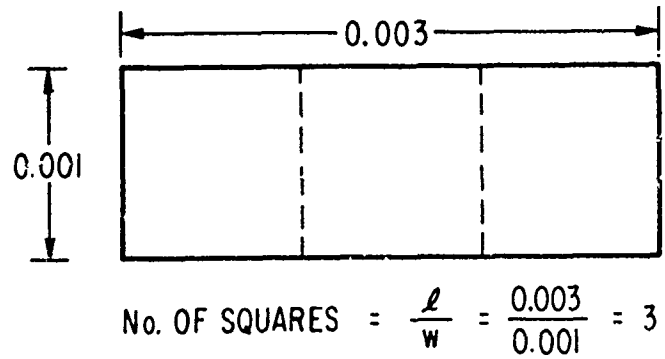


Figure 12. Sample Calculation of Number of "Squares"

For our circuit, the width of the current path varies. The width chosen is the average value of the width, as seen in Figure 10. The length can also be determined from Figure 10. Therefore, the resistance is

$$R_{across} = 3(\Omega/\text{square}) \times \frac{(1\ \text{mil})(\text{square})}{(2.3 + 2.1)\ \text{mil}} = \frac{3}{4.4} \approx 1\ \Omega$$

The total resistance of the transistor is therefore

$$R_{BULK} = R_{UD} + R_{across} + R_{DU} = 4 + 1 + 4.4 = 9.4\ \Omega$$

The resistance of the aluminum metallization leading from the output transistor to ground is

$$R_{MET} = \frac{\rho \ell}{A} = \frac{(2.82 \times 10^{-6}\ \Omega\text{-cm})(0.1\ \text{cm})}{(1\ \mu\text{m})(10\ \mu\text{m})} = 1.4\ \Omega$$

$$\therefore R_{Total} = R_{BULK} + R_{MET} = 9.4 + 1.4 \approx 11\ \Omega$$

Having computed the limiting resistance of the current path, we can determine the power dissipated in the junction from Eqs. (A. 1) and (A. 2). The power dissipated in the device is shown in Figure 13. The power per unit area necessary to burn out a junction in a given time can be obtained from Figure 1. With the area of the emitter junction, 1.8×10^{-5} cm^2, known, one can compute the power necessary to burn out the junction for a specific pulse width and from Figure 13 can then find the voltage necessary to cause this burnout. This result is shown in Figure 5. The actual effect of the pulse can be seen with the aid of a microscope. In the case just treated, the pulse burned a path from the emitter to the collector of the output transistor (see Figure 14).

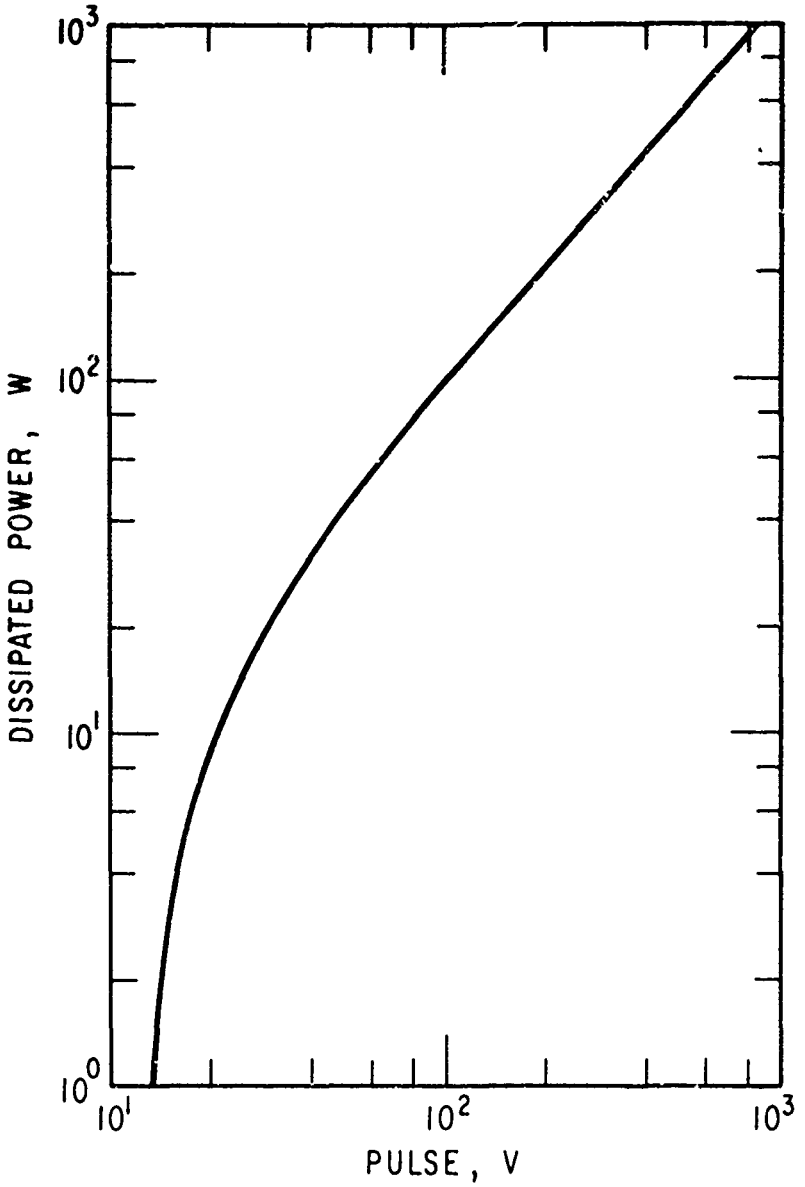


Figure 13. Power Dissipated Across Junction of Output Transistor of Amelco 6041 Dual Three-Input Nand Gate with High-Power Pulser on Output Connection

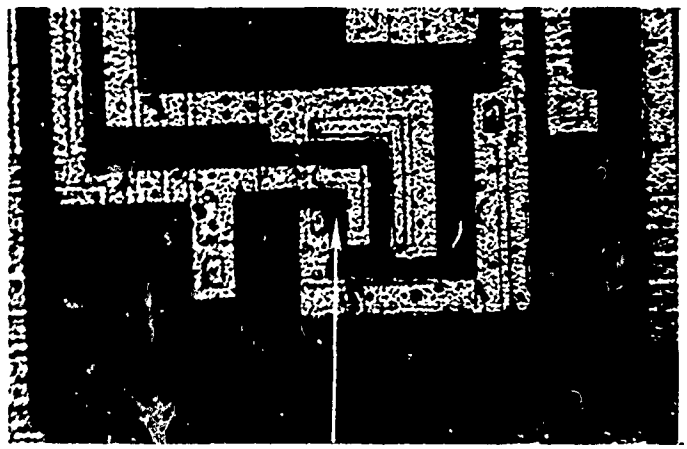


Figure 14. Photomicrograph of Burned-Out
Fairchild 9046 Output Transistor
Caused by Pulses Applied
to Output

APPENDIX B. WUNSCH CELL CALCULATIONS FOR A PULSE ON THE INPUT OF AN AMELCO 6041 NAND GATE

The circuit diagram and a photomicrograph of the 6041 are shown in Figures 15 and 16. The areas of the junctions and metallization can be measured from the photomicrograph. For a pulse on the input, the current will flow through input diode D1 and transistors T1, T2, and T3 to ground. The other possible paths all have limiting resistors and thus can be excluded. It is necessary, therefore, to compute the bulk resistances of D1, T1, T2, and T3.

The resistance of the input diode is

$$R_{UD} = \frac{\rho \ell}{A} = 100\ \Omega$$

where A is the area of the collector contact

$$R_{across} = \text{sheet resistance} \times \text{number of squares} = 8\ \Omega$$

$$R_{DU} = \frac{\rho \ell}{A} = 45\ \Omega$$

where A is the area of the base contact

$$R_{D1} = R_{UD} + R_{across} + R_{DU} = 153\ \Omega$$

The resistance of T1 and T2 is

$$R_{T1} = \text{sheet resistance} \times \text{number of squares} = 47\ \Omega$$

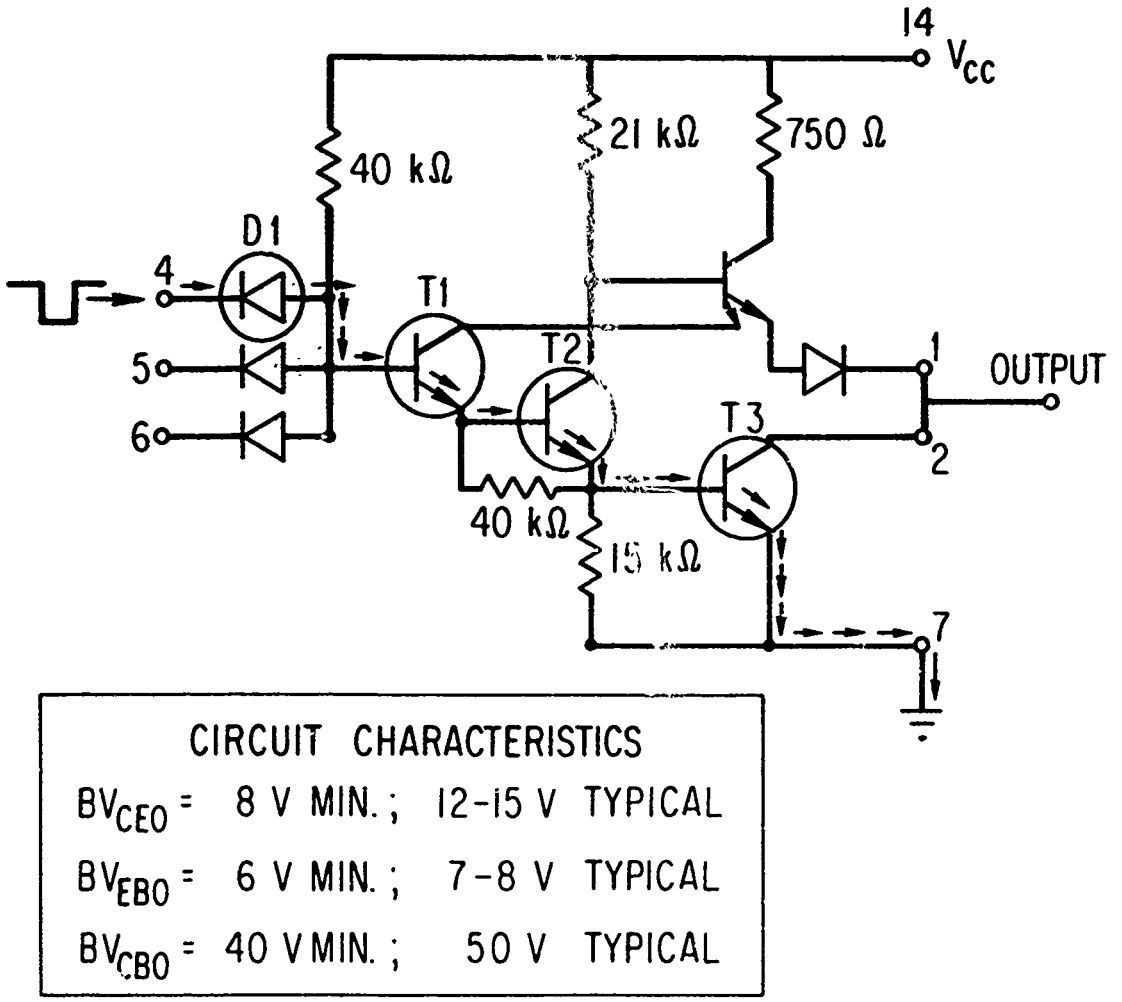
$$R_{T1} = R_{T2} = 47\ \Omega$$

The resistance of T3 is

$$R_{T3} = \text{sheet resistance} \times \text{number of squares} = 50\ \Omega$$

The resistance of the aluminum metallization is R = 1 Ω. The total resistance is

$$R_T = R_{D1} + R_{T1} + R_{T2} + R_{T3} + R_{A1} = 297\ \Omega$$



CIRCUIT CHARACTERISTICS		
BV_{CEO} =	8 V MIN.;	12-15 V TYPICAL
BV_{EBO} =	6 V MIN.;	7-8 V TYPICAL
BV_{CBO} =	40 V MIN.;	50 V TYPICAL

Figure 15. Circuit Diagram for One Channel of Amelco 6041 Dual Three-Input Nand Gate

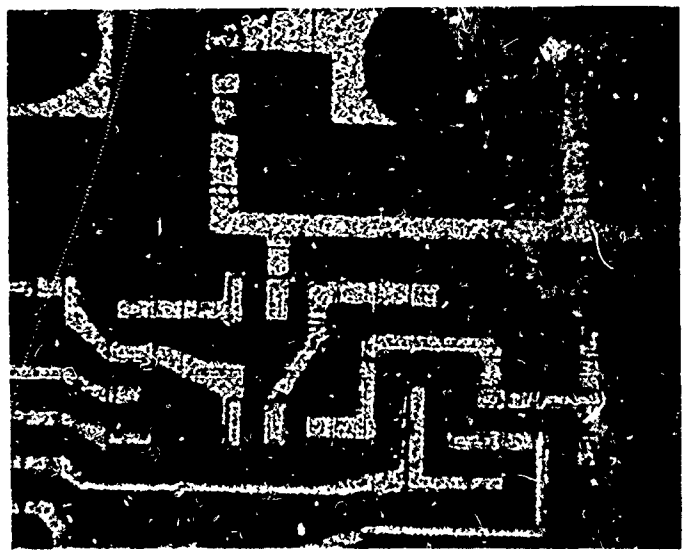


Figure 16. Photomicrograph of Amelco 6041 Nand Gate Geometry

Burnout of the various active elements depends upon the polarity of the pulse delivered to the input. For positive pulses, most of the power is dissipated across the input diode, and it will be most likely to burn out. For negative pulses, the input diode is forward biased and does not dissipate much power. Therefore, most of the power will be dissipated in the transistors T1, T2, and T3. Since T1 and T2 have smaller areas than does T3, transistors T1 and T2 are most likely to burn out. For a negative pulse, the current is

$$I = \frac{V}{R} = \frac{V - 3BV_{transistor}}{297} \qquad (B.1)$$

The power dissipated in the junction of T1 and T2 is

$$P = IV + I^2 R_{BULK}$$

Here the power dissipated in the bulk resistance is included because the base is so near the emitter junction. The power is shown in Figure 17. From Figure 16, we can measure the area of the emitter for transistors T1 and T2 (4.3×10^{-6} cm^2). With this value known, we can apply the Wunsch-Bell theoretical values from Figure 1 to obtain a graph of breakdown voltage vs pulse width, Figure 6. The damage mechanism is junction burnout of transistors T1 and T2, which can be clearly seen in Figure 18. If the pulse is sufficiently large, D1, T1, T2, and T3 will all burn out, as is shown in Figure 19.

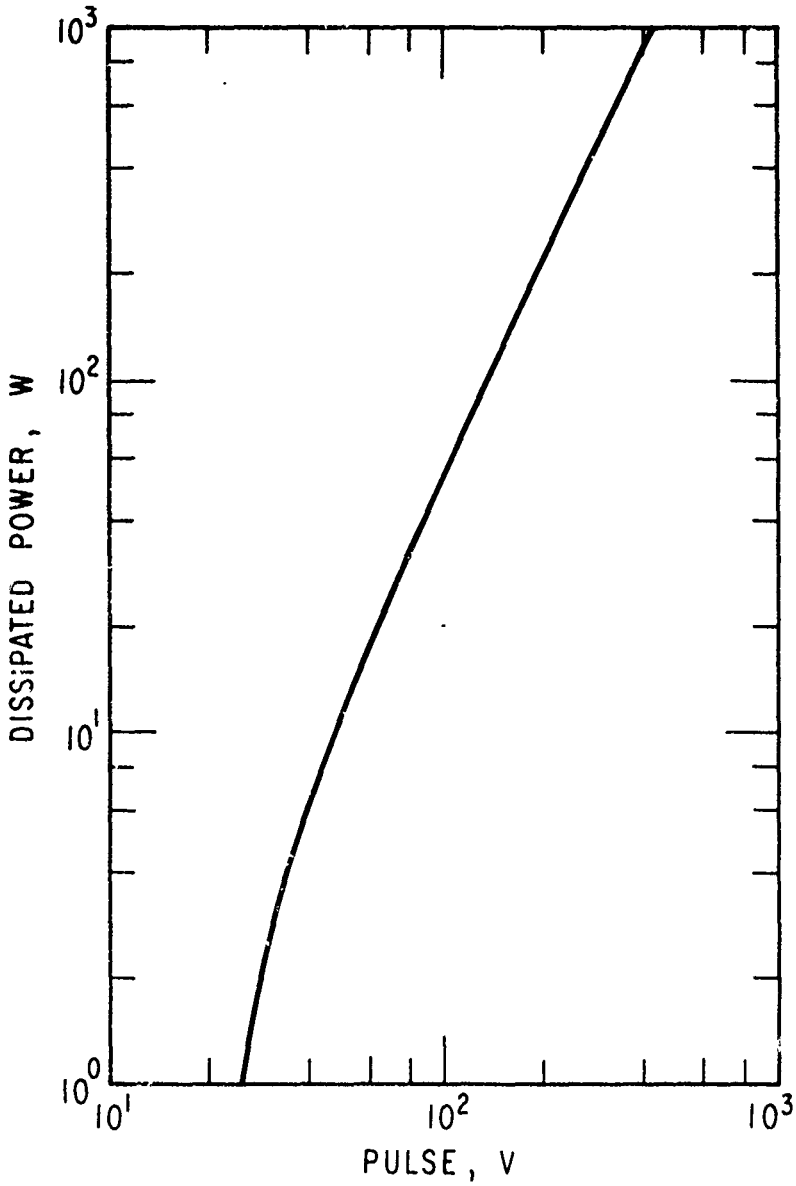


Figure 17. Power Dissipated at Emitter Junction of Transistor T1 or T2 of Amelco 6041 Nand Gate with Negative High-Power Pulses on Input

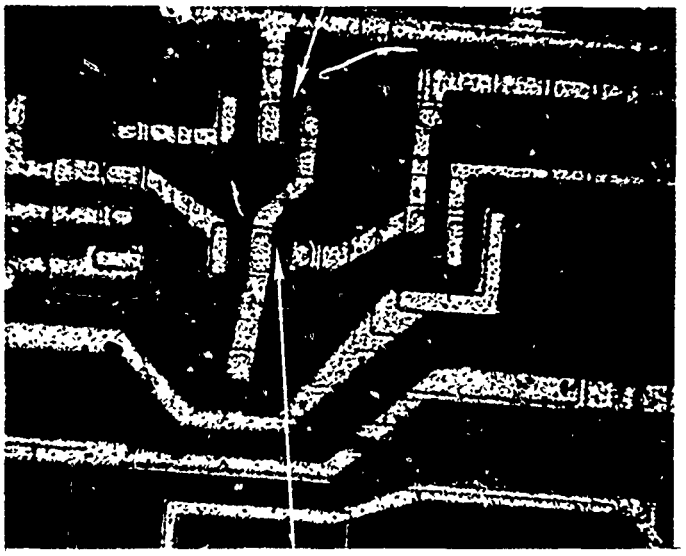


Figure 18. Photomicrograph of Amelco 6041 Nand Gate After Application of High-Power Negative Pulse to Input, Showing Failure of Transistors T1 and T2

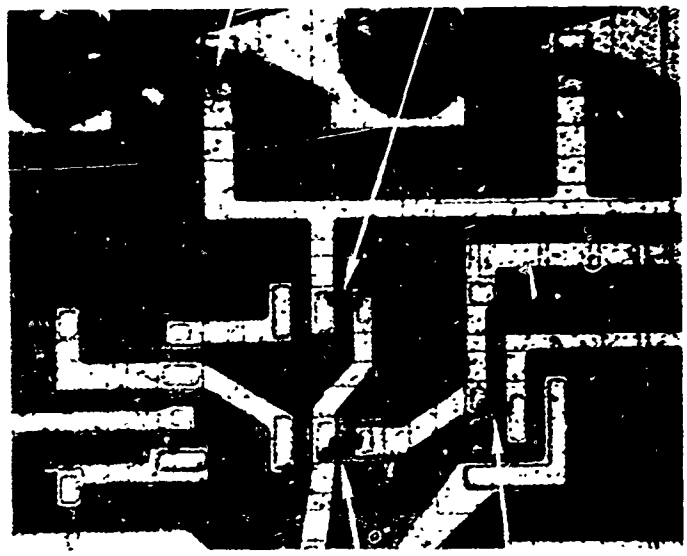


Figure 19. Photomicrograph of Amelco 6041 Nand Gate After Application of High-Power Negative Pulse to Input, Showing Failure of Diode D1 and Transistors T1, T2, and T3