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ELECTRICAL CHARACTERIZATION OF COMPLEX MICROCIRCUITS

General Electric Ordnance Systems

Rome Air Development Center
Air Force Systems Command
Griffiss Air Force Base, New York

ELECTRICAL CHARACTERIZATION OF COMPLEX MICROCIRCUITS

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FOREWORD

This Final Report was prepared by General Electric Ordnance Systems, 100 Plastics Avenue, Pittsfield, Massachusetts, for Rome Air Development Center, Griffiss Air Force Base, New York, under contract F30602-72-C-0188, Job Order No. 55190000. It covers the period March 1971 to March 1972. Mr. Regis C. Hilow, RCRM, was the RADC Project Engineer.

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13 ABSTRACT

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Section 3000 of MIL-STD-883 was reviewed and rewritten. New or modified slash sheets to MIL-M-38510 were prepared for DTL and T^{2}L-SSI logic circuits, 741 Operational Amplifier, 710/711/LM106 Differential Comparator, and the 723 Regulator. The results of the vendor comparison, test circuits, and proposed slash sheets are included in this report.

Test profiles were prepared for a broad range of bipolar and MOS semiconductor memories. ROM's, PROM's, and static and dynamic RAM's were considered. The test profiles cover static and dynamic functional test requirements.

MSI/LSI test considerations were based upon the development of a minimum set of logic tests, based upon a stuck-at-one, stuck-at-zero philosophy in order to provide a rapid and accurate functional test of complex devices. This testing criteria termed "Logic Integrity Tests" is described and is aproposed for inclusion in MIL-STD-883. Test Vectors based upon the Logic Integrity Test for the 2 and 4 bit full adders, 4 x 2 multiplier and the 9341/54181 Arithmetic Logic Unit are included in this report.

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EVALUATION

1. The prime objective of this study was to electrically characterize state-of-the-art microcircuits to provide guidance for the preparation of MIL-M-38510 (General Military Specification, Microcircuits) detail specifications for generic classes of devices. A detailed review of the test methods contained in the 3000 and 4000 series of MIL-STD-883 (Test Methods and Procedures for Microelectronics) was to be conducted and recommendations for changes, additions and/or deletions made. Optimum and complete test methods and procedures to electrically characterize complex microelectronic devices such as multipliers, arithmetic units, RAM's, ROM's, etc., were also to be developed.

2. This study was considered to be highly successful and productive with all objectives achieved. More specifically, all the 3000 series test methods of MIL-STD-883 were reviewed and revised to reflect state-of-the-art testing. Additional test methods were developed to cover bistable and special MOS devices. These revised and new test methods are presently being reviewed by EIA, AIA and the DOD agencies to effect their coordination as military standards. Test method revisions to the 4000 series of MIL-STD-883 were developed jointly by GE and RADC. This resulted in MIL-M-38510/101, the military specification that will be used to procure 741's, 747's and LM101's (commercial operational amplifiers). New test methods were added to the 4000 series and others were changed. EIA and AIA committees are presently reviewing the methods for possible inclusion into the 4000 series of MIL-STD-883. GE reviewed and provided test data when needed to verify the electrical parameters specified in the first group of military digital specifications (MIL-M-38510/1 through 23) covering 89 TTL device types. They also prepared in the MIL-M-38510 format, detail specifications covering the 900 series of DTL logic. In the linear circuit area, in addition to the 741, 747 and 101, they prepared, based on contract test results, MIL-M-38510/102 and 103 covering the 723 voltage regulator and the 710, 711 and 106 comparators, respectively. The details and test conditions over the operating temperature range are presented in sufficient detail to cover all vendors' devices.

3. In the area of MSI/LSI testing, some significant results were achieved. For example, in testing and studying the 54181 and 9341 arithmetic units, it was determined that vendors only te[illegible] 83% of the circuit. Logic integrity tests (basically a series of functional tests) to complete the testing were developed and were added to the military specification (MIL-M-38510/11) that will be used to procure this part. It was also determined that a different logic integrity test must be conducted on the 54181 than on the 9341 even though they perform identical functions. Also included in this report is a general guideline document for testing read-only memories. This information will be used to prepare future military specifications.

4. It should also be pointed out that a significant portion of the work resulting from this effort will be used in procuring microcircuits for the F-15, AX, AWACS, B-1, Minuteman III and Poseidon programs.

Regis C. Hilow

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Section I

SUMMARY

The characterization of complex microcircuits study covered a broad range of microcircuits of varying complexity including analog and digital circuitry. Either detailed electrical tests were performed or guidelines for testing the various microcircuits were developed. Interchangeability tests were performed where equivalent parts were available from several vendors.

In nearly all areas, the tested parts met the vendor's published data sheets. However, significant differences between test results and vendor specifications were found. At times these differences could be attributed to varying methods of writing specifications for these devices. This was particularly true of the more mature parts as exemplified by the dynamic test conditions for SSI-T^2L circuits. For the newer parts, major differences can be correlated to the time a vendor decided to become a second source for a particular device type. His entry into the marketplace would be based of the latest design and processing capability available to him at that time. New devices were considered, i.e. device types that take advantage of a new [illegible] technique and/or circuit design breakthrough, a parallel but situation is found. In the rush to market these devices, the bugs in the design, processing, specification, and test techniques have not been worked out. The device will undergo a rapid redesign cycle to improve performance or alleviate manufacturing problems and the associated specification sheet will vary accordingly. Particular care is also required to properly assess the test requirements in this case since the problem is not "has the vendor met his data sheet?" but "is he testing the correct parameters?".

It should be noted that this problem is not necessarily confined to the new devices because it appears to a lesser degree even in mature devices. For example, tests to check if a flip flop performs its intended function, i.e., is it working as a memory element, strobe line gating function in comparators, noise tests for operational amplifiers, function testing of digital logic networks, etc. The general problem is that specifications generated by the vendor are supplier-oriented and not user-oriented.

The development of complex MSI and LSI digital functions has significantly complicated the component test problem. This added complexity has transferred the 1960 subsystem test considerations to the component level in the 1970's. The greater complexity of the devices results in more possible failure modes. Consequently, the complexity of the test procedures necessary to guarantee the integrity of the component will be radically increased. Furthermore, large portions of the device's circuitry will be "buried" within its package without direct access terminals, raising fundamental questions about the very existence of a means of testing it.

Multiple sources supplying identical functions of differing design further complicate the situation. For any given state table or Boolean equation there are a large number of possible circuit realizations which are functionally equivalent. The user is faced with the dilemma of either performing exhaustive testing of all possible logic states or the utilization of computer techniques which may be prohibitively expensive. This is often resolved by performing a heuristically determined set of tests that he feels comfortable with or attempts to extract a guarantee from the vendor or vendors concerning the performance of the device.

For these reasons, it is recommended that for MSI/LSI devices a logic flow diagram depicting the exact realization of the internal circuitry be made part of the device specification. Associated with this logic diagram, a minimum set of test vectors should be included that will exercise each gate of the given logic mechanization. When multiple sources supply equivalent mechanizations, each logic diagram should be included in the specification and a cover set of test vectors that exercise all the logic mechanizations should also be supplied.

The rapidly growing field of semiconductor memories that include ROM's, PROM's, static and dynamic memory devices have raised an entirely new set of test considerations. The magnetic memory test techniques are not directly applicable, it is difficult to specify a single set of "worst case patterns" when the memory cell, decoders, and sense amplifiers are contained in a single monolithic structure that can have completely different circuit designs and topology from several vendors supplying equivalent devices. The entire area of pattern testing is not included in vendor specifications and no industry standards exist. Exhaustive testing of a 1000-bit memory for all possible patterns is impossible.

A set of test patterns is recommended in this report. Each memory type, ROM, PROM etc., is considered separately. It is hoped that this will form the basis for a set of industry standards.

Section II

INTRODUCTION

2.0 Objective

The objective of this study and investigation was to develop guidelines for the electrical characterization and testing of microcircuits of varying degrees of complexity and to aid in assuring conformance to their detailed specification. For digital circuitry, this included a detailed static, dynamic, and functional analysis of the various logic arrangement within and between the various logic configurations. For linear circuits, all parameters as specified in the 4000 series of MIL-STD-883 were reviewed and worst case conditions defined. The features, limitations, and interchangeability criteria were determined and compared according to established tradeoffs such as power-speed, temperature-frequency, etc. In addition, test methods for characterizing MOS microcircuits as well as changes to the present test method were developed and reported in a format.

This effort developed general knowledge regarding the optimum electrical test conditions for microcircuits, and provided criteria for selecting and evaluating interim critical and end-point electrical parameters for use in Government or contractor prepared detail specifications.

2.1 Background

Microcircuits of varying degrees of complexity are presently being designed into military equipments in increasingly large numbers. There are many different processes, configurations, and methods involved in fabricating these devices, all of which could possibly introduce reliability problems. To aid in eliminating certain failure modes and to remove gross defects in a given population, reliability screening and qualification methods per MIL-STD-883 and MIL-M-38510 were developed and are presently being utilized in military equipment procurements. Concurrent with the development of these standards, MIL-STD-1331 was initiated to account for, and require the specification of, a minimum number and type of electrical parameters for linear or digital microcircuits. This standard references the 3000 and 4000 series of MIL-STD-883 for test procedures for the various electrical tests. However, many specific details are missing in these two standards or, again, parameters need to be further quantified with respect to a given test method. For example, worst case situation per a test method and a circuit type need to be established and introduced into MIL-STD-883 and eventually MIL-STD-1331. This study provided this information, thus enhancing microcircuit procurement specifications.

Complex microcircuits in the MSI and LSI categories need to be electrically characterized on a circuit basis and/or functional basis according to established guidelines. It was the intent of this effort to provide these guidelines for both complex bipolar and MOS microcircuits.

In general, this effort eliminated, or acccunted for the variations in electrical test methods and parameters for a given circuit type purchased from more than one vendor and defined the optimum or minimum number of electrical parameters that must be specified and/or tested for special devices. In addition, the conditions of test were defined with respect to the requirements of MIL-M-38510, MIL-STD-883, and MIL-STD-1331.

2.2 Approach

Studies and investigations to develop guidelines for the electrical characterization of microcircuits, both bipolar and MOS, of varying degrees of complexity were performed. These included factors affecting design, fabrication processes, vendor detail specifications, computer-aided-tests, and review of pertinent microcircuit standards. The program included study and evaluation of the following work elements:

- State-of-the-Art Survey: A complete review and analysis of prior work directed toward standardizing electrical parameters for linear and digital microcircuits was conducted.

- Review of MIL-STD-883, MIL-STD-1331, and MIL-M-38510.

- Major vendor/user recommended specifications. Initial work under this element was limited to TTL, DTL, and ECL for digital circuits and to an operational amplifier, a differential amplifier, a general purpose amplifier for a linear circuit, and a MOS device.

- Device Characterization: Those devices mentioned immediately above except for ECL were electrically characterized according to their a-c, d-c, and functional parameters. Variations of these parameters over the vendor-rated temperature extremes were also considered. Where possible, the specific MIL-STD-883 electrical test methods were aligned with these selected parameters.

- Interchangeability: Sufficient effort was expended to determine the variations in circuit design, testing, and specified electrical parameters for families of devices manufactured by different vendors. Initial emphasis was placed on the 930 DTL series, 54 TTL series, the standard ECL series, and on the 741 operational amplifier and the 106 differential comparator in the linear category.

- Complex Microcircuits: This task was directed at determining the optimum or minimum number of electrical parameters that must be measured to adequately characterize electronically a complex device in the MSI and LSI categories. To accomplish this task, complex devices presently being marketed by multiple sources was considered for study. A 2-bit and 4-bit adder, arithmetic logic unit and a 4x2 multiplier were tested.

- **Standardization of Tests:** A review of the electrical parameter tests required in Groups A, B, and C tests of the 5004 and 5005 tests of MIL-STD-883 was conducted to determine if additional tests need to be specified, present tests need to be deleted, or present tests need to be modified. In addition, the 3000 and 4000 series test procedures of MIL-STD-883 were reviewed to effect changes, additions, and deletions. Results of this task were presented in a format compatible with the appropriate test method or procedure of the applicable military standard.

Section III

EVALUATION OF DTL-SSI LOGIC CIRCUITS

3.0 Introduction

Many years of experience with DTL on the Poseidon and Naval Electronic Standard Hardware Program (SHP) has led to a thorough familiarization of the characteristics and problems encountered with the particular family of Logic. Considerable data has been accumulated regarding static and dynamic electrical parameters measured over the temperature range. A summary of the d.c. results at room temperature is shown in Figures 3.1 through 3.4 for a DTL 930, DTL 932, DTL 946 and DTL 962.

3.1 DTL Specifications

Based on the above data and experience, a proposed set of specifications in the MIL-M-38510 format was made up. These specifications consisted of a complete Table I for electrical performance characteristics and a complete Table III for Group A inspection for each of three types of devices, i.e., a gate, a flip flop, and a buffer gate. Many of the limits used in these specifications are tighter than those advertised as standard by the manufacturers but have been easily procured to in the Poseidon Program from more than one manufacturer. The specifications can be found in the Appendix of this document.

3.2 Changes to MIL-STD-883, Method 3000's

Experience gained in testing DTL devices relating to test fixtures and test procedures was used in the preparation of the proposed changes to MIL-STD-883 Method 3000. Over the years many problems in testing have been encountered and successfully resolved, especially with dynamic electrical parameters and J-K flip flop operation. Information such as reasonable limits on forcing functions and functional testing of flip flops was included in the proposed changes. In fact three completely new method 3000's were added to cover some of the aforementioned problems. Experience also dictated a complete change to the methods for measuring noise margins, Method 3013.

3.3 Vendor Comments

The proposed DTL specifications were sent to all the major manufacturers for comments. Since these specifications closely follow the requirements of the T^2L specifications which are already in existence, there were no adverse comments on the test methods nor on the electrical requirements. Some vendors feel that the usage of DTL devices is falling off and that the projected future requirements do not warrant

the expense of preparing new specifications nor qualifying to them. The projected dollar value for 1972 is thirty-two million dollars based on a volume of sixteen million units. This corresponds to a T^2L value of fourteen million dollars based on twenty million devices. Furthermore the T^2L usage is growing while the DTL usage is declining. On the other hand DTL has been designed into military equipment which will continue to need replacement parts for at least 10 years. It would certainly be advantageous to military users to be able to procure DTL devices to MIL-M-38510 processing and reliability.

Vendor	V_{OH} (V)	V_{OL} (MV)	O_{SC} (ma)	I_{CL} (ma)	I_{CH} (ma)	P_{DH} (MW)	P_{DL} (MW)
F	4.184 0.0556	256 44.5	1.114 0.1049	1.629 0.533	0.0493	14.85 2.59	31.50 3.50
B	4.121 0.0663	304 53.2	0.8955 0.1189	1.159 0.1529	0.1093	12.59 2.33	26.04 3.82
E	4.127 0.0457	307 41.5	0.8750 0.0830	1.196 0.1183	0.0161	12.94 2.84	25.91 3.00
Limits	3.8V min	400mV max	.765/1.12 ma	1.6ma max	2ua max	30mw max	40mw max

1st number: mean
2nd number: sigma

T_A = +25°C

Figure 3.1. Parameter Distribution of DTL930

Vendor	V_{OH} (V)	V_{OL} (MV)	O_{SC} (ma)	I_{CL} (ma)	I_{CH} (ma)	P_{DH} (MW)	P_{DL} (MW)
F	4.030	208	20.99	1.162	0.4137	13.73	114.19
	0.1066	28.3	5.44	0.213		2.33	19.19
B	4.016	223	20.37	1.046	0.5021	13.65	111.28
	0.1308	42.6	4.61	0.284		1.91	14.31
E	4.066	280	20.14	1.333	0.0574	15.19	117.94
	0.0581	36.7	4.62	0.095		1.31	13.27
Limits	3.8V min	400mV max	18/46ma	1.6ma max	2ua max	80mw max	180mw max

1st number: mean
2nd number: sigma

T_A = +25°C

Figure 3.2. Parameter Distribution of DTL932

Vendor	V_{OH} (V)	V_{OL} (MV)	I_{SC} (ma)	I_{CL} (ma)	I_{CH} (ma)	P_{DH} (MW)	P_{DL} (MW)
F	4.065 0.0700	285 86.7	0.373 0.0987	1.174 0.1485	0.4412	24.14 3.58	51.61 6.42
B	4.066 0.0695	292 97.7	0.366 0.0988	1.172 0.1271	0.2832	23.33 3.66	51.46 5.59
E	4.056 0.0578	317 84.4	0.857 0.0561	1.179 0.0930	0.0932	25.40 2.08	51.22 4.05
Limits	3.8V min	400mV max	0.765/1.12 ma	1.6ma max	2ua max	60mw max	80mw max

1st number: mean
2nd number: sigma

T_A = +25°C

Figure 3.3. Parameter Distribution of DTL946

Vendor	V_{OH} (V)	V_{OL} (MV)	O_{SC} (ma)	I_{CL} (ma)	I_{CH} (ma)	P_{DH} (MW)	P_{DL} (MW)
F	4.123 0.0395	237 35.6	0.863 0.0796	1.087 0.1406	.0061	17.49 1.66	35.89 3.20
B	4.131 0.0632	269 39.4	0.912 0.1068	1.240 0.1430	0.1000	19.92 2.67	40.10 4.60
E	4.136 0.0427	307 33.9	0.902 0.0810	1.253 0.1048	0.0068	19.33 1.71	41.41 3.31
Limits	3.8V min	400mV max	0.765/1.12 ma	1.6ma max	2ua max	45mw max	60mw max

1st number: mean
2nd number: sigma

T_A = +25°C

Figure 3.4. Parameter Distribution of DTL962

ITT SEMICONDUCTORS
ELECTRONICS WAY, WEST PALM BEACH, FLORIDA
A DIVISION OF INTERNATIONAL TELEPHONE AND TELEGRAPH CORPORATION

Ref. No.: G/694

13 December 1971

Mr. Herb Labb
General Electric
P. O. Box 606
Pittsfield, Mass.

Dear Herb:

I would like to make some formal comments on the proposed MIL-M-38510 DTL specs which you sent. These comments will be in line with our telephone conversation, and based on the 930, 932, and 945 specs which I have received.

I would recommend that the ten lead TO-99 package be deleted as an approved package. ITT has seen very little demand for this package, and the use of only ten leads severely restricts the logic available.

The static parametric (DC) tests you show on the specs I received seem well in line with device capabilities. Although they are somewhat tighter than our present standard, I feel that we could meet them with little problem and that the limits are more realistic for high reliability users' designs.

I am concerned, however, about the extensive dynamic (AC) testing you propose, especially over the full temperature range. Good, repeatable results can be obtained with room temperature testing, but the added equipment (ovens, special sockets and fixtures) required for full-range testing make repeatability and correlation between vendors very difficult. AC temperature testing at best is slow, unwieldy, and expensive.

As an alternative, I would recommend that a comprehensive design qualification and characterization be required on a one-time basis, and only lot sampling be used on a continuing basis to insure that no device changes have occurred. ITT has supplied DTL devices to NAD Crane, Indiana, using a scheme similar to this with very good results.

The 945 flip-flop spec presents a good example of what I consider to be unnecessary testing. You have proposed testing clock to output propagation

TELEPHONE 305 842-2411 TWX 510-952 6007

delay time high to low and low to high, setup time, release time, direct input to output propagation delay time high to low and low to high, clock high level and clock low level thresholds, and maximum operating frequency, all over the full temperature range. While I agree that typical and limiting values of all these parameters must be known, I feel that after a full characterization, device operation can be guaranteed with room temperature testing of clocked operation only.

I would recommend the following limits for AC parameters as follows. These limits are based on our experience with NAD Crane and can be guaranteed by room temperature tests.

		Tpd+	Tpd-
930, 962, 946	25°C	25 - 80 ns	10 - 30 ns
	125°C	25 - 110 ns	7 - 35 ns
	-55°C	25 - 80 ns	10 - 40 ns
944	25°C	15 - 50 ns	10 - 35 ns
	125°C	15 - 100 ns	10 - 35 ns
	-55°C	10 - 45 ns	10 - 30 ns
945	25°C	35 - 75 ns	30 - 75 ns
	125°C	35 - 110 ns	30 - 90 ns
	-55°C	20 - 90 ns	25 - 65 ns
932	25°C	25 - 80 ns	15 - 40 ns
	125°C	25 - 140 ns	15 - 45 ns
	-55°C	20 - 80 ns	15 - 40 ns

If you have any questions or comments, please give me a call.

Respectfully,

ITT SEMICONDUCTORS

Michael I. Wier

Michael I. Wier
Product Engineer

MIW/bp

Copies to:
F. DiGesualdo
R. Morey
J. Paschal

National Semiconductor Corporation

December 16, 1971

Mr. Herbert C. Labb
General Electric Ordance Systems
Advanced Components Engineering
Room 2072T, 100 Plastics Ave.
Pittsfield, Mass. 01201

REF: 5070-381

Dear Mr. Labb:

I just received a preliminary characterization of the 930 DTL family for inclusion in MIL-M-38510 slash sheets. I must say I was surprised if not shocked to see this.

The MIL-M-38510 slash sheets originally were, and I believe still are, to be prepared for widely used integrated circuits. The 930 DTL family is certainly not a popular family of devices. The 930 DTL useage reached its peak approximately 2 years ago. Since then it is been replaced by the faster and more versatile 54 series, TTL integrated circuits, as the industry standard bipolar digital logic family. The 930 family is used only in old designs and the majority useage here being for the commercial version in the dual-in-line package (DIP). All new designs utilize the 54 series TTL IC's. Additionally, 930 DTL is available in only basic functions. MSI (medium scale integration) circuits are not available in the 930 series. The attached curves depict the rapid demise of 930 DTL series total factory sales in both dollars and units.

MIL-M-38510 slash sheets have been prepared for the popular 54 series TTL devices with more on the way. It appears to be an unwise move to prepare specifications, at a substantial cost, that would not find any useage. I sincerely hope you will seriously consider the industry trends for the 930 DTL integrated circuits before deciding to incur the cost of preparing and releasing MIL-M-38510 slash sheets.

Very truly yours,

NATIONAL SEMICONDUCTOR CORP.

Eugene R. Hnatek

EUGENE R. HNATEK
MILITARY/AEROSPACE PRODUCT
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Section IV

EVALUATION OF T^2L - SSI LOGIC CIRCUITS

4.0 Introduction

Data was taken on radiation hardened and normal low power T^2L devices and normal standard T^2L devices. All devices tested were Vendor E's two-input nand gates. For comparison purposes certain tests were performed on similar devices manufactured by other vendors.

The integrated circuits were tested to MIL-M-35810/1 (USAF) dated 1 February 1971. Since this specification was written for standard devices, deviations were made in order to supply appropriate static and dynamic loads for the low-power devices. Static and dynamic tests were performed at three temperatures: -55°C, +25°C, and +125°C. In addition to the specification, pictures were taken of transfer characteristics at the above three temperatures. Some limited testing was done on four input high speed T^2L nand gates in order to provide a three-way comparison on input loading characteristics and transfer characteristics.

The test limits and loading for the normal low-power and radiation-hardened low-power devices were extracted from the "Integrated Circuits Catalog for Design Engineers" written by Vendor E (1971); Catalog No. CC401. Test results were analyzed and compared with the manufacturers specifications and to MIL-M-38510/1 requirements. Comments on test results are given and problem areas outlined with respect to specifying and testing these devices.

Although testing was done only on two input nand gates, the characterizations (in this report) can be extended to other devices in the same product line family.

4.1 Summary

4.1.1 Low Power Devices

4.1.1.1 Radiation Hardened

Radiation hardened (RH) and normal (N) low-power devices have output saturation voltages (V_{OL}) that are 0.1 volts lower than standard or high-speed devices. The logic "0" input threshold for RH low-power devices however is 0.1 volts higher than it is for N low-power devices. The results is that the RH logic "0" noise margin is 0.1 volts greater than it is for the N low-power devices.

The high logic "0" threshold of the RH devices is a design feature requested by the Air Force.

The RH device input leakage is an order of magnitude greater than it is for N devices; yet the maximum limits are the same. Leakage on N standard devices is similar to that for RH low-power devices; however, the standard device leakage limit is four times greater. The maximum limit can be held by the RH devices because the leakage is largely a function of geometry. The N standard device leakage is a function primarily of process control and thereby not as predictable; therefore; wider limits are required.

Forward current gains of transistors drop after irradiation. Input leakage is a function of the inverse gain of the input transistor, and, if that gain should drop after irradiation, the maximum limit would be comparable to the N low-power device limit. The specification limit may therefore be user oriented; that is, limits are based upon post irradiation performance.

Vendor E's output short circuit limits for RH devices are broader than they are for N devices. Data indicated that the short circuit currents are the same. It was explained by Vendor E that the limits reflect post irradiation performance of the device and not initial performance.

Care must be taken when screening RH devices initially to post irradiation limits. The third and fourth paragraph above illustrate both dilemmas of the problem:

a) Third paragraph - screening initially to a limit that is too tight. This could reduce yield though not specifically in this case.

b) Fourth paragraph - screening initially to broad post irradiation limits can allow devices which could be out of specification after irradiation.

A suggestion would be to screen initially to pre-irradiation requirements and then sample the lot; irradiate; and then test the samples to new limits.

RH device turn-on (t_{PHL}) and turn-off (t_{PLH}) delays were considerably longer (10-20ns) than N low-power device delays at -55°C. At elevated temperatures the delays were similar.

An interaction between gate inputs was observed. See Figure 4.8. The nature of the interaction is not known; however, it was not transistor action. In most cases, when this interaction occurs, the input leakage currents can become excessive with respect to typical readings; however, the maximum leakage current limit is so high that the gate inputs will pass requirements. Although the number of times this interaction was observed was small, its stability with time and temperature cannot be verified. It does not appear necessary to provide test restraints; however, a satisfactory explanation from the vendor should be obtained.

No major differences were observed between the two lots of RH low-power devices supplied by Rome Air Development Center (RADC).

Based upon test results, it is concluded that the RH low-power devices supplied by RADC were not irradiated.

Device characteristics that will change with irradiation should be defined. Irradiated devices should be tested and compared to non-irradiated devices. Where characteristics change considerably, 100 percent initial screening requirements should not be mixed with post irradiation device performance on procurement specifications. Separate tests could be run on a sampled basis on units that have been irradiated to verify the magnitude and direction of change.

4.1.1.2 Normal Low Power

(N) low-power device input logic "0" thresholds and logic "0" output voltages are 0.1 volts lower than they are for standard or high speed devices.

Mixing normal low-power devices and standard or high-speed circuits has some short comings. First of all, the logic "0" noise margin for the low-power device is decreased by 0.1 volts (the opposite is true for the high-speed and standard devices).

Secondly with standard device logic "0" input voltages 0.1 volts higher, the low-power device will be operating on one of the negative sloped portions of the segmented transfer characteristic (+125°C characteristic). This will cause low-power logic "1" output voltages to be lower. This in turn causes logic "1" noise margins to decrease. Refer to Figure 4.5, Part B.

An interaction was observed between gate inputs. The interaction was similar to that described in the summary for RH low-power devices.

The dynamic load for normal low-power devices should be simplified. See Figure 4.12.

(N) low-power device propagation delays were considerably greater than the manufacturers typical numbers.

Data also indicates that propagation delay limit increases of approximately 7ns over a 25°C limit would have to be made for delay measurements at the temperature extremes.

The manufacturers test limits are realistic with respect to device performance in all areas except propagation delay.

Propagation delay data were close to the manufacturers maximum limits. In some cases there were failures. More testing should be done with other lots to determine how delays vary between lots.

4.1.2 Standard Devices (Normal)

Several logic "1" level failures occurred at both temperature extremes. The failures were all "marginal", except that those at +125°C occurred on the very low impedance portion of the transfer characteristic. Slight variations in threshold here produce very large changes in the logic "1" level. The low impedance breaks on the transfer characteristics for low temperatures are at high thresholds and do not produce this effect. Therefore, V_{OH} measurements at +125°C are important; setting of the initial conditions of the Gate Under Test (GUT) input thresholds is critical to the measurement.

An interaction was observed between gate inputs. The interaction was similar to that described in the summary for RH low-power devices.

All data fell within MIL-M-38510/1 limits; exceptions noted. Generally the test limits were neither severe nor lenient. The maximum limit for high-level input current (I_{IH2}) reflects circuit breakdown and not normal leakage current. At a glance, the limits would appear to be too high, but in fact are not.

The MIL-M-38510/1 turn-off delay maximum limit (t_{PLH}) at 25°C is satisfactory. The limit extension for the temperature extremes (Δ of 2ns) is adequate, however, data shows that in order to be on equal terms with the 25°C limits, the limit increase for the temperature extremes should be 5 ns.

4.1.3 Parameter Trend Summary

The following figures, Figures 4.1 and 4.2 summarize the parameter trends of the T^2L integrated circuits under consideration.

4.2 Input Clamping Characteristics - Summary

Devices which do not specifically have input clamping diodes as a design feature may still exhibit some clamping action.

Basically, two lots of standard Vendor E devices were tested. One lot was known to have clamp diodes and passed V.I.C. test requirements easily. Another lot procured off the shelf (7013A) failed on all but one input tested. The average reading for this lot was -8.04ma at -1.5 volts. It was decided that this second lot did not have clamping diodes. It may be possible for standard devices without clamp diodes to pass V.I.C. requirements; if a lot did pass, the integrity of the clamp characteristic with time, temperature, and load conditions may be questionable. Available data indicate that standard devices with clamp diodes will meet -12ma at less than -1.0 volts. A change in the V.I.C. test voltage from 1.5 to 1.3 volts would further discriminate against gates without clamp diodes. It would also tend to eliminate gates with clamp diodes with low voltage secondary breaks.

Parameter		Parameter Trend, Min/Max versus: Temperature		
		-55°C	+25°C	+125°C
V_{OL} - Low Level Output Voltage		Min	--	Max
V_{OH} - High Level Output Voltage		Min	--	Min*
I_{OS} - Output Short Circuit Current		Min	--	--
I_{IH1} - High Level Input Current		Min	--	Max
I_{IH2} - High Level Input Current		Min	--	Max
I_{IL} - Low Level Input Current	(RH)	--	Min	--
	(N)	Max	--	Min
I_{CCH} - High Level Supply Current Drain		--	Min	--
I_{CCL} - Low Level Supply Current Drain	(RH)	--	Min	--
	(N)	Max	--	--
t_{PHL} - Propagation Delay Time, High to Low Level Output		Max	--	Min
t_{PLH} - Propagation Delay Time, Low to High Level Output	(RH)	--	Min	--
	(N)	--	Min	--

*If device thresholds are low, a minimum reading will also occur at this temperature.

Figure 4.1. Summary - Parameter Trend

Low Power (N) and (RH - Pre-irradiation) Devices

Parameter	Parameter Trend, Min/Max versus: Temperature		
	-55°C	+25°C	+125°C
V_{OL} - Low Level Output Voltage	Min	--	Max
V_{OH} - High Level Output Voltage	Min	--	Min*
I_{OS} - Output Short Circuit Current	Max	--	Min
I_{IH1} - High Level Input Current	Min	--	Max
I_{IH2} - High Level Input Current	Min	--	Max
I_{IL} - Low Level Input Current	--	--	Min
I_{CCH} - High Level Supply Current Drain	--	Max	--
I_{CCL} - Low Level Supply Current Drain	--	Max	--
t_{PHL} - Propagation Delay Time, High to Low Level Output	Max	--	Min
t_{PLH} - Propagation Delay Time, Low to High Level Output	Min	--	Max

*If device thresholds are low, a minimum reading will also occur at this temperature.

Figure 4.2. Summary - Parameter Trend

Normal - Standard Devices

Vendor E indicated that, eventually, all standard T^2L devices will have clamp diodes with the exception of SN54/74-83. Old designs will be recycled; however, the schematics will not be changed to illustrate this.

Vendor E also indicated that all radiation-hardened, low-power devices have clamping diodes. The suggested test limits (-1.0ma @ V_{in} - 1.2V to -1.6V) however do not appear to be compatible with these devices. Secondary high impedance diode breaks were observed at relatively low current levels, thus precluding those devices from meeting the above criteria. If, in fact, all low-power, radiation-hardened devices have clamp diodes, it was not apparent for the two lots tested. A more in-depth investigation would be required at this point in order to establish test limits. Test limits established for standard devices definitely cannot be applied.

No outstanding differences were noted between the two lots of radiation hardened low power devices.

Some of the newer Vendor E normal low-power devices may have clamping diodes. As a rule though, the normal low-power devices will not have clamping diodes. The old designs will not be recycled.

Since the normal low-power devices tested were of an old design, they should not have had clamp diodes. The clamp characeristics were similar to those for the radiation-hardened, low-power devices. One noticable difference was that the knee of the initial break was softer for the normal devices. Other than that, no other differences were noted.

Secondary breaks in input clamping characteristics show up more frequently in devices without clamping diodes because they occur at low voltages. Secondary breaks, in devices with clamp diodes, occur at high voltages (-3.0V) and at very high currents (-150ma) and are beyond the scope of normal consideration. In several cases, secondary breaks could not be observed, even at several hundred ma of current.

4.3 Reduced Data and Comments

The following data is representative of four integrated circuits of each lot. Each device contains four, two-input nand gates. The test loads are shown in Figure 4.3.

Measurement	Low Power Devices (R.H.) and (N)	Standard Devices
V_{OL} Output voltage low	(to I.C. V_{CC}) 2.1K ±1% to I.C. Output	(to I.C. V_{CC}) 259 Ω ±1% to I.C. Output
V_{OH} Output voltage high	to I.C. Output 23.7K ±1%	to I.C. Output 6.19K ±1%
t_{PHL} Propagation delay time high to low level output t_{PLH} Propagation delay time low to high level output	(to I.C. V_{CC}) 4K ±1% * 50pf 30pf Diodes -1N4148	(to I.C. V_{CC}) 383 Ω ±1% * 50 pf Diodes - 1N4148

*Including scope probe, wiring, and strap capacitance without package in test fixture.

Figure 4.3. Integrated Circuit Test Loads

Device Tested and Lot Identification	Test Limit -55C to +125°C	Reduced Data				High and Low Data Points
		-55°C	+25°C	+125°C	-55°C to +125°C	
RSN54L00 (7026)	0.3v max	0.149v	0.172v	0.215v	0.239v 0.138v	High Low
RSN54L00 (7051)	0.3v max	0.141v	0.165v	0.202v	0.228v 0.124v	High Low
SN54L00T (7033A)	0.3v max	0.140v	0.161v	0.191v	0.221v 0.121v	High Low
SN5400F (7013A)	0.4 max	0.241	0.248v	0.294v	0.362v 0.176v	High Low

*Reduced data is an average of 16 data points.

Comments

1.) There are now apparent differences between the radiation hardened and the normal low-power devices.

2.) The standard device saturation voltage is approximately 0.1 volts higher than the low-power device saturation voltage (at all temperatures). This is in agreement with the manufacturer's claims.

3.) Worse-case, high-saturation voltage occurs at elevated temperatures.

4.) No failures were encountered on any of the devices.

Figure 4.4. V_{OL} - Low Level Output Voltage

MIL-M-38510/1 Test Conditions 1-4

Device Tested and Lot Identification	Test Limit -55°C to +125°C	Reduced Data*				High and Low Data Points for Data within Limits
		-55°C	+25°C	+125°C	-55°C to +125°C	
RSN54L00 (7026)	2.4v min	2.56v	2.67v	2.67v	2.71v	High
					2.46v	Low
RSN54L00 (7051)	2.4v min	2.57v	2.68v	2.62v	2.73v	High
					2.46v	Low
SN54L00T (7033A)	2.4v min	2.50v	2.58v	2.47v	2.62v	High
					2.400v	Low
SN5400F (7013A)	2.4v min	2.56v	2.67v	2.62v	2.76v	High
					2.45v	Low

Figure 4.5. V_{OH} - High-Level Output Voltage

PART A

MIL-M-38510/1 Test Conditions 5-12

Device Tested and Lot Identification	Number of Failures		
	-55°C	+25°C	+125°C
RSN54L00 (7026)	0	0	0
RSN54L00 (7051)	0	0	0
SN54L00T (7033A)	1**	0	14**
SN5400F (7013A)	6	1	13

PART B

*Reduced data is an average of 32 data points less any failures. Failures were not factored into reduced data.

**See comment #1.

Comments

1.) All V_{OH} measurements were run with 0.8 volts for the maximum logic "0" level. Normal low-power devices specify 0.7 volts (radiation hardened low-power devices are specified at 0.8v). There were a large number of failures for the SN54L00T's at +125°C. Referring tothe +125°C transfer characteristic, Figure 4.39 shows that the gate thresholds are a worst case low at elevated temperatures. The break in the transfer characteristic which defines the beginning of a low output impedance region occurs at approximately 3.0 volts. Therefore, the minimum acceptable V_{OH} of 2.4 volts is on a very steep vertical slope and a small change in input threshold for a border-line case would cause a failure. A review of the raw data indicates that all the failures documented in Figure 4.5, Part B for SN54L00T's would never have occurred with an input voltage of 0.7 volts. This confirms the manufacturer's claims on threshold differences between radiation-hardened and normal low-power devices.

Note that for the standard power device failures, the V_{OH} readings were exceptionally low (1.4 volts - see raw data) at +125°C.

2.) The tabularized average V_{OH} readings for the SN54L00T's are lower than they normally would be because an input voltage of 0.8 volts was used instead of 0.7 volts. However this does afford a good comparison between normal and radiation-hardened units.

3.) The failures that occurred at -55°C for the SN5400F were marginal type failures. This is borne out by the transfer characteristics. The low impedance break at -55°C occurs at a V_{OH} of approximately 2.0 volts and an input voltage of 1.40 volts.

Device Tested and Lot Identification	Test Limit -55°C to -125°C	Reduced Data*				High and Low Data Points
		-55°C	+25°C	+125°C	-55°C to +125°C	
RSN54L00 (7026)	-5.36ma -15ma	-5.36ma	-7.79ma	-7.59ma	3.6ma 4.5ma	High Low
RSN54L00 (7051)	-1 to -15ma	-5.85ma	-7.21ma	-7.38ma	7.6ma 4.1ma	High Low
SN54L00T (7033A)	-3 to -15ma	-5.52ma	-7.38ma	-6.40ma	7.8ma 3.7ma	High Low
SN5400F (7013A)	-20 to -55ma	-34.2ma	-33.8ma	-29.6ma	38.5ma 25.2ma	High Low

Figure 4.6. I_{OS} – Output Short Current
MIL-M-38510/1 Test Conditions 13-16

· omments

. . Output short circuit current for low-power devices (normal and radiation-hardened) appears to peak up between +25°C and +125°C. This is an indicator of the resistivity change of the output collector resistor with temperature and also of the type of silicon doping used to form that resistor. The manufacturer's schematic shows a diode and a saturated collector-emitter junction in series with the collector resistor. Calculations show that changes in current due to changes in junction voltage with temperature will cause the current at -55°C to decrease approximately 0.5ma and to increase approximately 0.5ma at +125°C. This tends to mask the resistivity changes of the collector resistor.

... The data does not show any justification for the manufacturer's lowering the lower limit for radiation-hardened devices from -3ma to -1ma. Vendor E explained that the limits reflect user application. That is, after exposure to radiation, the output short circuit current can be expected to drop. This means that the logic "1" fanout can be expected to decrease. There are two inconsistencies: 1) The first is that both the normal and radiation-hardened device outputs are rated at V_{OH}'s of +2.4 volts at -110μa (a fanout of 10). It seems appropriate that a change in fanout is due for one of the two devices. Also, the range of the limits appears to be excessive, even when considering data variation with temperature and lot. 2) The second inconsistency is that 100 percent screening should be done to the pre-radiation limits which are tighter. There should also be user design limits which reflect post radiation circuit changes.

3.) The resistivity of the collector resistor for intermediate power devices appears to increase at +125°C. A bottoming out may occur between -55°C and +125°C. This resistivity characteristic is different from the low-power characteristic

. All low and intermediate power devices met their respective requirements. [illegible] readings varied between mid range and the low end of the specified limits. There were no major differences between the two lots of low-power, radiation-hardened devices or between these devices and the normal low-power devices

4.3.4 I_{IH1} - High Level Input Current

Device Tested and Lot Identification	Test Limit -55°C to +125°C	Reduced Data	
		+25°C	+125°C
RSN54L00 (7026)	10μa max	2.84μa	3.98μa
RSN54L00 (7051)	10μa max	2.59μa	4.37μa
SN54L00T (7033A)	10μa max	.25μa	.49μa
SN5400F (7013A)	40μa max	2.74μa	5.99μa

Figure 4.7. I_{IH1} - High Level Input Current

MIL-M-38510/1 Test Conditions 17-24

Comments

1.) The raw data taken at -55°C was not reduced. It was felt that the range of the readings (low versus high) and inconsistency was too great for the readings to have any credibility. Problems were encountered with water condensation on the inside of the test chamber. The moisture adversely affected current readings.

A data trend was established: The trend being that the maximum input leakage current occurs at elevated temperatures. To further back up the data trend, leakage current readings were taken at 0°C with input voltages of 5.5 volts. Water condensation was not a problem at 0°C.

2.) The leakage current levels for the low-power, radiation-hardened devices were similar to those for the standard devices and approximately an order of magnitude higher than the normal low power devices. Although RH, low-power data were similar to the standard device data, the manufacturer's maximum limits for the two are different: (10μa versus 40μa). 10μa is also the maximum limit for normal low power devices. It was explained by Vendor E that the 40μa limit reflects process variables. The 10μa limit can be held by the RH devices because it is more of a geometric variable which is more controllable than a process variable. The reason why the leakage is actually higher for RH devices is because the inverse gain of the input transistor was made higher to increase

the threshold of the device from 0.7v, for normal low power, to 0.8v. This was done per Air Force request. The inverse currents become greater with high inverse gains.

3.) No outstanding differences were noted between the two lots of RH devices.

4.3.5 I_{IH2} - High Level Input Current

Device Tested and Lot Identification	Test Limit -55°C to +125°C	Reduced Data			
		0°C* Retake	+25°C Retake	+25°C Original	125°C
RSN54L00 (7026)	100μa max	2.58μa	3.36μa	4.59μa	6.87μa
RSN54L00 (7051)	100μa max	2.80μa	3.57μa	3.84μa	7.07μa
SN54L00T (7033A)	100μa max	.16μa	.22μa	.34μa	.69μa
SN5400F (7013A)	1ma max	4.42μa	5.53μa	5.41μa	10.15μa
SN54H20S (7119A & 7105A)	1ma max	---	---	4.59μa**	9.65μa**

*This data is an average taken on two samples in order to supply a third data point (at 0°C). It is intended to show that maximum current readings will occur at elevated temperatures. Moisture problems were encountered in the test chamber at temperatures below 0°C.

**See comment #4.

Figure 4.8. I_{IH2} - High Level Input Current
MIL-M-38510/1 Test Conditions 25-32

Comments

1.) The leakage current levels for the low-power, radiation-hardened devices were similar to those for the standard devices and approximately an order of magnitude higher than the normal low-power devices.

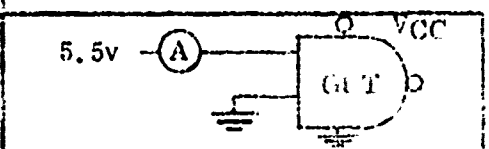
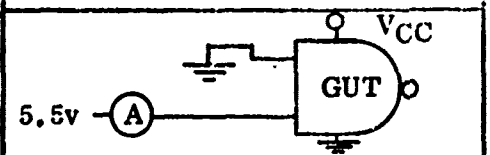
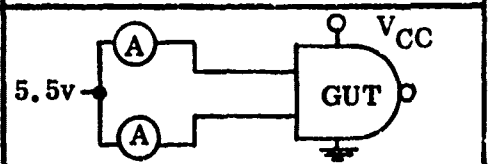
2.) No outstanding differences were noted between the two lots of radiation-hardened devices.

3.) Some of the gate input pairs for the low-power and standard devices (all two input nands) reacted strangely. The data for one gate input pair for sample #5, lot 7026 (RSN54L00), has been retabulated below.

Test*** Cond.	I_{IH1}		I_{IH2}		Test*** Cond.
	25°C	125°C	25°C	125°C	
21	3.3μa	1.1μa	5.4μa	1.75μa	29
22	3.2μa	11.4μa	5.3μa	58.5μa	30

***Note - test conditions 21 and 22 (IIH 1) correspond to test conditions 29 and 30 for test IIH 2.

At elevated temperature the current in one input of an input pair decreases from what it was at a lower temperature and the current in the other gate input increases by an order of magnitude. Further tests were run in order to determine the mechanics of the problem. The following tabulation outlines these tests.

Test Cond.	I_{IH2} (Temp = +125°C)		
	V_{cc} = 4.5v	V_{cc} = 0v	
29	2.1μa	3.1μa	
30	51.0μa	51.0μa	
29	6.2μa	0.8μa	
30	26.5μa	51.0μa	

In order to sustain transistor action on input diodes, power must be applied to the integrated circuit. Also transistor action is bi-directional for a given gate input pair. The preceding data tabulation shows that transistor action is not occurring. When this problem was explained to Vendor E engineers, they ran similar tests and concurred with the results. They explained that there is definitely an interaction between inputs, although it is not transistor action. This interaction will not be seen on all gates, because the geometry difference each emitter inputs to its respective collector is slightly different, hence the inverse gain is different. Although specification limits were met by maverick gates, data for "normal" gates were far below the specification limits. Therefore, in order to prevent skewing of "normal" gate data, they were excluded from the data breakdown.

Data were normally far below specification limits. When leakage current readings are made with high input voltages (I_{IH2}), input gate breakdown may occur. These limits therefore reflect current levels incurred during input breakdown.

4.) Because transistor action was not found on two input gates, it was decided that some four input gates would be tested (SN54H20S). These gates did not exhibit transistor action nor were there any "maverick" gates. This data was broken down and tabulated for comparison.

5.) Measurements made for test requirements I_{IH1} showed similar "maverick" gate problems; however, the results were more dramatic for I_{IH2}.

Device Tested and Lot Identification	Test Limit -55°C to +125°C	Reduced Data				High and Low Data Points for Data within Limits
		-55°C	+25°C	+125°C	-55°C to +125°C	
RSN54L00 (7026)	-.18ma max	.119ma	.110ma	.121ma	.155ma .096ma	High Low
RSN54L00 (7051)	-.18ma max	.115ma	.112ma	.140ma	.170ma .104ma	High Low
SN54L00T (7033A)	-.18ma max	.114ma	.107ma	.091ma	.125ma .072ma	High Low
SN5400F (7013A)	-1.6ma max	1.17ma	1.19ma	1.09ma	1.45ma 0.93ma	High Low

Figure 4.9. I_{IL} - Low Level Input Current

MIL-M-38510/1 Test Conditions 33-40

Comments

1.) The Logic "0" input current for the low-power, radiation-hardened devices seemed to peak up slightly at the temperature extremes. A substantiating factor that this is happening is the fact that two failures occured for lot 7026 (radiation-hardened) at each of the temperature extremes. Only one failure was common at both of the extremes. The units passed requirements at 25°C. Some of that data is shown below:

	Unit #1	Test Step	-55°C	+25°C	+125°C
RSN54L00 (7026)	51	35	.185v	.107v	.109v
		36	0.32v	.107v	.90v
	56	37	.155v	.128v	.265v

2.) The normal low-power devices and the standard devices appeared to perform differently from the radiation-hardened devices. The logic "0" level input currents were highest at the lower temperature only.

4.3.7 I_{CCH} - High Level Supply Current Drain

Device Tested and Lot Identification	Test Limits -55°C to +125°C	Temperature		
		-55°C	+25°C	+125°C
RSN54L00 (7026)	0.8ma max	.540ma	.455ma	.494ma
RSN54L00 (7051)	0.8ma max	.542ma	.496ma	.534ma
SN54L00T (7033A)	0.8ma max	.495ma	.478ma	.495ma
SN5400F (7013A)	8ma max	5.08ma	5.26ma	5.11ma

Figure 4.10. I_{CCH} - High Level Supply Current Drain

MIL-M-38510/1 Test Condition 41

Comments

1.) Power supply current measurements (high and low level) were all well within limits. Readings for the low-power, radiation-hardened devices were a maximum at the temperature extremes while the current peaked up at room temperature for the normal standard devices. The normal low-power devices did not have a definable trend.

4.3.8 I_{CCL} - Low Level Supply Current Drain

Device Tested and Lot Identification	Test Limit -55°C to +125°C	Temperature		
		-55°C	+25°C	+125°C
RSN54L00 (7026)	2.04ma max	1.26ma	.986ma	1.30ma
RSN54L00 (7051)	2.04ma max	1.28ma	1.01ma	1.43ma
SN54L00T (7033A)	2.04ma max	1.32ma	1.28ma	1.20ma
SN5400F (7013A)	27ma max	15.9ma	16.3ma	15.4ma

Figure 4.11. I_{CCL} - Low Level Supply Current Drain

MIL-M-38510/1 Test Condition 42

Device Tested and Lot Identification	Test Limit	Reduced Data*				High and Low Data Points
		-55°C	+25°C	+125°C	-55°C to +125°C	
RSN54L00 RSNL00 (7026)	25°C (1,2) (X) ns min 60ns max		55.2ns		63.4ns	High
					35ns	Low
	-55°C; +125°C (X)ns min (X)ns max	77.3ns		44.8ns	91.8ns	High
					36.8ns	Low
RSN54L00 (7051)	25°C (1,2) (X) ns min 60ns max		54.7ns		64.6ns	High
					47.0ns	Low
	-55°C; +125°C (X)ns min (X)ns max	79.5ns		41.2ns	94.6ns	High
					34.4ns	Low
SN54L00T (7033A)	25°C (1,2) (X)ns min 60ns max		51.0ns		68.8ns	High
					39.8ns	Low
	-55°C; +125°C (X)ns min (X)ns max	58.5ns		43.3ns	77.4ns	High
					32.4ns	Low
SN5400F (7013A)	25°C 3ns min 20ns max		7.8ns		8.2ns	High
					6.8ns	Low
	-55°C; +125°C 3ns min 24ns max	11.4ns		6.3ns	12.4ns	High
					5.0ns	Los

*Reduced data is an average of 16 data points

Figure 4.12. t_{PHL} - Propagation Delay Time, High to Low Level Output

MIL-M-38510/1 Test Conditions 51-54, 59-62

Comments

1.) The loads specified in the manufacturer's catalog for normal low-power and radiation-hardened, low-power devices are different for the propagation delay measurements. For comparison purposes the load specified for the normal low-power devices was used for both types. The radiation-hardened device load did not have the 30pf capacitor shown in the Test Load Figure 4.1. A comparison of the two loads was made. The 30pf capacitor on the average adds 0.3ns to t_{PHL} measurements and 2.75ns to t_{PLH} measurements. This data is tabulated in the section for RSN54L00 (7026). See the Appendix.

Vendor E indicated that the addition of the 30pf capacitor helps to best simulate the input capacitive loading of normal low-power devices, but that they could not see why the loads should be different. The electrical difference noted between these loads, however, does not appear to be substantial enough to warrant specifying different loads for normal and radiation-hardened devices. The 30pf capacitor could be deleted from the normal low power load.

2.) Wherever the manufacturer has not supplied test limits, an X has been entered in the figure.

3.) For the standard devices, the delays were measured from the 1.5 volt level on the input waveforms to the 1.5 volt level on the output waveform as per the specification requirements. The delays for the low-power devices were measured from the 1.3 volt levels on the input waveform to the 1.3 volt level on the output waveform. The input waveforms were the same for all devices; they were adjusted per MIL-M-38510/1.

4.) The standard devices were comfortably within specification requirements. The increase in the turn on delays at -55°C from the +25°C delay (+3.6ns) was similar to the maximum limit extension of 4ns specified in MIL-M-38510/1. The recorded data match very closely the manufacturer's typical numbers. The temperature dependency of these devices was also verified.

5.) Curves in the manufacturer's catalog showing the temperature dependency of this measurement were not verified for (N) low-power devices. That is, the turn-on delay (t_{PHL}) is a minimum at 25°C and increases at the temperature extremes. Instead the minimum occurred at +125°C and the maximum at -55°C. The averaged data in Figure 4.12 also shows much higher "typical" numbers for normal devices; no typical numbers were given for RH devices. Also, the change in delay with temperature was observed to be much greater than that claimed by the manufacturer.

6.) The delays for the radiation-hardened, low-power devices at -55°C were significantly longer than those for the normal low-power devices. Vendor E indicated

that the delays should be similar. They were in fact similar at +25°C and at +125°C, however the data diverged at the low temperature extreme. Vendor E does not specify propagation delays at the temperature extremes, nor do they provide temperature dependency curves for the RH low power devices.

Device Tested and Lot Identification	Test Limit	Reduced Data*				High and Low Data Points
		-55°C	+25°C	+125°C	-55°C to +125°C	
RSN54L00 (7026)	25°C (1) (X)ns min 60 ns max		43.8ns		48.2ns	High
					36.0ns	Low
	-55°C; +125°C (X)ns min (X)ns max	50.3ns		45.6ns	56.0ns	High
					38.2ns	Low
RSN54L00 (7051)	25°C (1) (X)ns min 60ns max		44.4ns		47.0ns	High
					39.8ns	Low
	-55°C; +125°C (X)ns min (X)ns max	53.2ns		44.1ns	58.4ns	High
					41.2ns	Low
SN54L00T (7033A)	25°C (1) (X)ns min 60ns max		41.5ns		48.4ns	High
					36.0ns	Low
	-55°C; +125°C (X)ns min (X)ns max	43.9ns		47.2ns	55.2ns	High
					37.6ns	Low
SN5400F (7013A)	25°C 3ns min 25ns max		10.5ns		12.2ns	High
					9.2ns	Low
	-55°C; +125°C 3ns min 27ns max	8.8ns		15ns	19.0ns	High
					7.2ns	Low

*Reduced data is an average of 16 data points

Figure 4.13. t_{pLH} - Propagation Delay Time, Low to High Level Output
MIL-M-38510/1 Test Conditions 55-58, 63-66

Comments

1.) Wherever the manufacturer has not supplied test limits, an X has been entered in the figure.

2.) Curves in the manufacturer's catalog showing the temperature dependency of this measurement were satisfactorily verified for normal low-power devices. That is, the turn-on delay is a minimum at approximately +25°C and increases at the temperature extremes. These curves were also approximated by the RH devices. The manufacturer does not supply curves for the RH low-power devices.

3.) The 25°C readings were similar to the typical advertised numbers. No typical numbers are given for the RH, low-power devices. The delays for the RH devices were significantly longer than for the normal devices at -55°C; this was also true for turn on delay (t_{PHL}).

4.) The data for the standard devices varied considerably more with temperature than shown in the manufacturer's curves.

The maximum (t_{PLH}) specification limit was increased by 2ns for -55°C and +125°C delays from the 25°C limit for standard devices in MIL-M-38510/1. The difference between the 25°C data and the +125°C data in Figure 4.13 was 4.5ns. This verifies that the MIL-M-38510/1 limits should increase for temperature testing. The amount of the increase is questionable.

4.4 Input Clamping Characteristics

4.4.1 Introduction

The Static Electrical test, Voltage Input Clamping (V.I.C., as outlined in procurement specifications MIL-M-38510/1,2,3, attempts to screen for a short gate input clamping diode characteristic by making one current and voltage measurement. Heretofore, clamping diodes were generally design features of high-speed devices; however, some low-power and standard devices are now being manufactured with similar input characteristics.

Devices from three different manufacturers (Figure 4.14) were checked for input clamping diode action.

Enclosed are some pictures, with supporting data, which illustrate several different types of clamping characteristics.

4.4.2 Results

All low-power integrated circuits tested did not exhibit "simple" input diode clamping characteristics, nor did they meet the V.I.C. test criteria of -12ma at V_{in} = 1.5 volts. Some intermediate power devices met the V.I.C. test requirements; whereas all high-power samples met them.

The low-power devices had three modes of failure:

- No diode characteristic - high impedance curve (Figure 4.25)
- A diode characteristic breaking initially at approximately 0.7 volts followed by a low impedance region and then a secondary break followed by a high impedance region (Figures 4.23, 4.24, 4.25 and 4.26).
- A diode characteristic breaking initially at approximately 0.7 volts followed by a comparatively high impedance region. Secondary breaks were found at voltages less than -1.5 volts.

The double breaking input characteristic curve is not representative of simple diode action. Although the initial break is representative of a P-N junction, it is compounded by an additional break through some internal path which may be dependent upon the internal geometry of the device. In a review of the data, no correlation was apparent between any of the three types of input characteristics and their repeating at the same gate input pins. Several of the low-power samples were further tested to determine what input voltages were required in order to draw -12ma of current. It was found that input voltages of -2.5 to -7.1 volts were required.

Standard Vendor E devices (two-input nand gates) procured for evaluation purposes (date coded 7013A - see Figure 4.14) had input characteristics similar to the third characteristic described above. The secondary breakthrough occurred at higher currents than it did for the low-power devices (see Figure 4.28). One input of all

Vendor E RSN54L09	(Lot 7051)	Supplied by RADC (Figures 4.22 and 4.23)		
Vendor E RSN54L00	(Lot 7026)	Supplied by RADC (Figure 4.24)		
Vendor E SN54L00T	(Lot 7033A)	Procured off-the-shelf (Figures 4.25 and 4.26)		
Vendor E SN5400F	(Lot 7013A)	Procured off-the-shelf (Figures 4.27 and 4.28)		
Vendor E SN7476N	(Lot 7025A)	Procured off-the-shelf	Borrowed from in-house stock	(Figure 4.30)
Vendor E SN7400N	(Lot 7027A)	Procured off-the-shelf		(Figure 4.30)
Vendor G US74H40A	(Lot 6948)	Procured off-the-shelf		(Figure 4.31)
Vendor H N74N04A	(Lot 6933)	Procured off-the-shelf		(Figure 4.31)
Vendor H N7410A	(Lot 6907)	Procured off-the-shelf		(Figure 4.32)
Vendor E SN54H20S	(Lot 7118A)	Procured off-the-shelf		(Figures 4.33 and 4.34)
Vendor E SN5400J	(Lot 7119A)	Supplied as samples from Vendor E (Figures 4.35, 4.36, and 4.37)		

those sampled met the V.I.C. requirements. Several of these samples were also evaluated to determine what input voltages were required in order to draw -12ma of input current. In this case, -1.76 volts to -2.0 volts was required (see Figure 4.1[illegible]. One Vendor E sample (Figure 4.30 - dual J-K flip flop - date code 7025A) is illustrated in Vendor E's 1969-1970 catalog as not having input clamping diodes; however, it did meet the V.I.C. specification requirements and did exhibit a simple diode characteristic up to currents of -100ma on all inputs, including the clock inputs. No secondary break was observed. The knee of the curve however was noticeably not as sharp as it was on the Vendor G and Vendor H high-power devices (Figures 4.31 and 4.32).

The curves shown in Figures 4.31 and 4.32 are good examples of low-impedance [illegible] characteristics. The knees of the curves are very sharp, and all curves reach [illegible] at approximately 0.9 volts. The Vendor E J-K flip flop (Figure 4.30) met the [illegible].C. criteria at a higher input voltage of -1.2 volts. Note that the current offset [illegible] volts input voltage is primarily a function of the device low level (logic "0") input [illegible]rent and is dependent upon the power supply voltage of the device.

In conversations with Vendor E representatives, concerning input clamping [illegible]odes, the following details were discussed:

[illegible]. Standard digital T^2L devices

All standard devices with the exception of the SN54/74 - 80, 82, 91, 94 and 96 will have input clamping diodes. All new devices will have clamping diodes; schematics will reflect this. Old designs will have clamping diodes put in. The SN54/74 - [illegible]3 will be the last of the recycled designs and will be completed by the fourth quarter [illegible] this year (1971). Because recycling old schematics is an "unnecessary" cost, they will not be recycled for the sake of illustrating clamping diodes.

[illegible]ormal low-power devices

New devices will probably have clamping diodes. Old designs and schematics [illegible]ot be recycled.

[illegible] Radiation-hardened, low-power devices

All radiation-hardened, low-power devices have clamping diodes. There will be only one clamp diode per gate, independent of the number of gate inputs. The diode will be located between the collector of the multi-emitter input transistor and ground. The dielectrically isolated inputs on the radiation-hardened devices makes placement of the clamp diodes in the conventional location (from each input to ground) impractical.

Test criteria for the verification of clamp diodes was discussed. The voltage check point would probably be -1.2 to -1.6 volts. The current should be significantly

greater than I_{IL}* (0.18ma max). Minus one milliamp was suggested by Vendor E for V.I.C. Figure 4.24 shows that a secondary break in the clamping characteristic occurs at approximately 300μa. With secondary breaks occurring at such low currents, -1ma is not a realistic check point; however, 300μa does not sufficiently define the diode clamp. Vendor E indicated that a secondary break in the clamp characteristic can be expected and that for low-power devices it will occur at a lower voltage than for the standard devices.

Figure 4.15 and 4.16 are summaries of the test data. The raw data is pictured in Figures 4.17 through 4.21.

	Average Reading	Minimum Reading	Maximum Reading	No. of Data Samples Averaged
	E=-1.5v	E=-1.5v	E=-1.5v	
RSN54L00 (7026)	-4.67ma	-3.50ma	-5.40ma	71
RSN54L00 (7051)	-4.35ma	-1.1ma	-5.8ma	97
SN54L00T (7033A)	-3.35ma	-0.88ma	-5.7ma	60
SN5400F (7013A)	-8.04ma	-4.80ma	-12.0ma	72
SN5400J[1] (7119A)	---	---	---	--

[1]See Figure 4.21 this section

Figure 4.15. Data Breakdown-V.I.C. Input Current with Input Voltage Set at -1.5 volts

*Note that for standard devices the difference between I_{IL} and the V.I.C. current check point is approximately 1 to 10 (1.6ma vs. 12ma).

	Average Reading	Minimum Reading	Maximum Reading	No. of Data Samples Averaged
	I=-12ma	I=-12ma	I=-12ma	
RSN54L00 (7027)	-4.02v	-3.64v	-5.01v	8
RSN54L00 (7051)	-3.56v	-2.47v	-4.87v	16
SN54L00T (7033A)	-4.05v	-1.99v	-7.11v	8
SN5400F (7013A)	-1.86v	-1.76v	-2.0v	8
SN5400J (7119A)	-.874v	-.828v	-.959v	8

*Readings which deviated erratically from the norm were excluded from the data breakdown.

Figure 4.16. Data Breakdown - V.I.C. Input Voltage with Input Current Set at -12.0ma

Figure 4.17. Raw Data Vendor E RSN54L00 - Date Code 7026

SYMBOL	*** TEST NO.	SAMPLE NUMBER * 50 I=-12mA	* 51 E=-1.5v	* 52 E=-1.5v	* 53 E=-1.5v	* 54 E=-1.5v	* 55 E=-1.5v	* 56 E=-1.5v	* 57 E=-1.5v	* 58 E=-1.5v	* 59 E=-1.5v
V.I.C.	43	-3.64v	-4.6mA	-5.2mA	-4.3mA	-3.5mA	-.37mA[1]	-4.6mA	-4.5mA	-4.7mA	-5.1mA
V.I.C.	44	-3.64v	-4.5mA	-5.1mA	-4.3mA	-3.9mA	-5.2mA	-4.6mA	-4.5mA	-4.8mA	-5.0mA
V.I.C.	45	-4.44v	-4.8mA	-5.3mA	-4.3mA	-4.1mA	-4.9mA	-4.5mA	-4.1mA	-4.8mA	-5.0mA
V.I.C.	46	-5.01v	-4.8mA	-5.2mA	-4.3mA	-4.2mA	-5.4mA	-4.5mA	-4.1mA	-4.9mA	-5.2mA
V.I.C.	47	-3.86v	-4.7mA	-5.2mA	-4.3mA	-4.3mA	-5.3mA	-4.5mA	-4.1mA	-4.9mA	-5.2mA
V.I.C.	48	-3.86v	-4.6mA	-5.1mA	-4.2mA	-4.2mA	-5.2mA	-4.4mA	-4.4mA	-4.8mA	-5.1mA
V.I.C.	49	-3.86v	-4.5mA	-5.0mA	-4.3mA	-4.1mA	-5.2mA	-4.4mA	-4.4mA	-4.8mA	-4.9mA
V.I.C.	50	-3.86v	-4.6mA	-5.2mA	-4.4mA	-4.2mA	-5.4mA	-4.6mA	-4.6mA	-4.9mA	-5.1mA

[1] See Figure 4.24

NOTE: For definition of asterisk (*) see Figure 4.20

Figure 4.18. Raw Data Vendor E RSN54L00 - Date Code 7051

SYMBOL	*** TEST NO.	SAMPLE NUMBER								
		** 0	* 1	* 2	* 3	* 4	* 5	* 6	* 7	* 8
		I=-12mA	I=-12mA	E=-1.5v	E=-1.5v	E=-1.5v	E=-1.5v	E=-1.5v	E=-1.5v	E=-1.5v
V.I.C.	43	-2.58v	-4.55v	-4.3mA	-4.5mA	-4.5mA	-4.6mA	-5.0mA	-4.4mA	-4.5mA
V.I.C.	44	-2.57v	-4.15v	-4.4mA	-4.5mA	-4.5mA	-4.6mA	-4.9mA	-4.5mA	-4.4mA
V.I.C.	45	-2.56v	-4.57v	- .7mA	-5.0mA	-4.9mA	-4.5mA	-4.8mA	-4.6mA	-4.5mA
V.I.C.	46	-2.61v	-4.72v	-4.7mA	-5.8mA	-4.8mA	-4.4mA	-.45mA	-4.8mA	-4.8mA
V.I.C.	47	-2.47v	-4.72v	-4.6mA	-4.8mA	-4.3mA	-4.5mA	-4.8mA	-4.5mA	-4.6mA
V.I.C.	48	-2.53v	-4.41v	-4.5mA	-4.8mA	-4.2mA	-4.3mA	-4.7mA	-4.4mA	-4.5mA
V.I.C.	49	-2.54v	-4.87v	-4.5mA	-4.9mA	-4.5mA	-4.3mA	-4.7mA	-4.4mA	-4.5mA
V.I.C.	50	-2.50v	-4.55v	-4.7mA	-5.1mA	-4.7mA	-4.0mA	-.65mA	-4.5mA	-4.5mA

SYMBOL	TEST NO.	* 9	* 10	* 11	* 12	* 13	* 14
		E=-1.5v	E=-1.5v	E=-1.5v	E=-1.5v	E=-1.5v	E=-1.5v
V.I.C.	43	-4.3mA	-4.4mA	-4.6mA	-1.3mA	-5.3mA	- .2mA
V.I.C.	44	-4.2mA	-4.3mA	-4.6mA	-1.3mA	-5.3mA	- .2mA
V.I.C.	45	-3.9mA	-4.5mA	-4.7mA	-.66mA	-4.7mA	-4.6mA
V.I.C.	46	-4.1mA	-4.5mA	-4.7mA	-.66mA	-4.7mA	-4.5mA
V.I.C.	47	-3.8mA	-4.6mA	-4.5mA	-1.2mA	-4.7mA	-4.5mA
V.I.C.	48	-3.7mA	-4.5mA	-4.4mA	-1.1mA	-4.6mA	-4.4mA
V.I.C.	49	-3.8mA	-4.5mA	-4.2mA	-1.4mA	-5.0mA	-4.5mA
V.I.C.	50	-3.8mA	-4.5mA	-4.5mA	-1.4mA	-5.2mA	-4.6mA

NOTE: For definition of asterisk (*) see Figure 4.20

Figure 4.19. Raw Data Vendor E SN54L00T - Date Code 7033A

SYMBOL	*** TEST NO.	SAMPLE NUMBER									
		** 2	* 1	* 3	* 4[2]	* 5	* 6	* 7	* 8	* 9	* 10
		I=-12mA	E=-1.5v	E=-1.5v	E=-1.5v	E=-1.5v	E=-1.5v	E=-1.5v	E=-1.5v	E=-1.5v	E=-1.5v
V.I.C.	43	-5.23v	-.88mA	-1.6mA	X	-1.2mA	-.14mA	-3.2mA	-3.9mA	-3.5mA	-3.9mA
V.I.C.	44	-3.42v	-1.0mA	-1.6mA	X	-4.4mA	-3.5mA	-3.5mA	-3.2mA	-4.2mA	-.14mA
V.I.C.	45	-3.21v	-2.9mA	-1.5mA	X	-4.2mA	-3.5mA	-3.9mA	-5.7mA	-4.6mA	-4.7mA
V.I.C.	46	-2.18v	-2.9mA	-1.4mA	X	-1.1mA	-3.5mA	-3.2mA	-5.3mA	-4.6mA	-4.7mA
V.I.C.	47	-5.41v	-2.1mA	-.14mA	X	-4.5mA	-1.5mA	-3.8mA	-5.6mA	-4.6mA	-4.9mA
V.I.C.	48	-7.11v	-1.2mA	-1.5mA	X	-.12mA	-.68mA	-1.9mA	-5.3mA	-2.7mA	-4.6mA
V.I.C.	49	-3.86v	-3.1mA	-1.6mA	X	-4.5mA	-3.7mA	-3.6mA	-5.2mA	-4.8mA	-4.2mA
V.I.C.	50	-1.99v	-3.0mA	-1.7mA	X	-3.7mA	-3.7mA	-3.7mA	-4.5mA	-4.8mA	-4.8mA

[2] **This sample was inadvertently destroyed in test.**

NOTE: For definition of asterisk (*) see Figure 4.20

Figure 4.20. Raw Data Vendor E SN5400F - Date Code 7013A

SYMBOL	*** TEST NO.	SAMPLE NUMBER									
		** 1	* 2	* 3	* 4	* 5	* 6	* 7	* 8	* 9	* 10
		I=-12mA	E=-1.5v	E=-1.5v	E=-1.5v	E=-1.5v	E=-1.5v	E=-1.5v	E=-1.5v	E=-1.5v	E=-1.5v
V.I.C.	43	-1.88v	-4.8mA	- 9.9mA	-11.0mA	-7.3mA	-6.9mA	-6.0mA	-8.9mA	-8.0mA	- 9.1mA
V.I.C.	44	-1 85v	-5.6mA	-10.1mA	-10.1mA	-7.4mA	-6.1mA	-6.1mA	-9.1mA	-8.0mA	-10.7mA
V.I.C.	45	-1.76v	-7.6mA	-10.1mA	-11.4mA	-7.2mA	-6.7mA	-5.9mA	-9.0mA	-8.9mA	-10.5mA
V.I.C.	46	-1.78v	-7.6mA	-10.0mA	- 7.7mA	-7.8mA	-6.6mA	-5.9mA	-8.4mA	-8.2mA	-10.5mA
V.I.C.	47	-1.80v	-6.8mA	-10.0mA	- 9.3mA	-7.7mA	-6.3mA	-6.7mA	-8.9mA	-8.1mA	-10.7mA
V.I.C.	48	-1.85v	-6.5mA	- 9.7mA	-11.0mA	-7.5mA	-6.2mA	-5.5mA	-8.8mA	-7.9mA	-10.0mA
V.I.C.	49	-2.00v	-5.7mA	- 9.3mA	-10.0mA	-6.8mA	-5.5mA	-6.2mA	-8.4mA	-7.2mA	- 6.8mA
V.I.C.	50	-1.92v	-6.1mA	- 9.7mA	-10.0mA	-6.9mA	-5.4mA	-6.2mA	-8.4mA	-7.2mA	-12.0mA

* Input voltage was set to -1.5volts and the input current was recorded.

** The input voltage was varied until the input current reached -12mA. The voltage was then recorded.

*** Tests were performed per specification MIL-M-38510/1 (device type 04 - case A&B). Test step numbers refer to table designations per the specification.

Figure 4.21. Raw Data Vendor E SN5400J - Date Code 7119A

		Sample Number					
Symbol	*** Test No.	#1** Ein	#1** I_{in}	#2** Ein	#2** I_{in}	#1* I_{in}=-12mA	#2* I_{in}=-12mA
V.I.C.	43	-1.5 v	45mA	-1.5 v	47mA	-.948v	-.959v
V.I.C.	45	-1.5 v	70mA	-1.09v	50mA	-.848v	-.830v
V.I.C.	47	-1.11v	55mA	-1.05v	50mA	-.838v	-.828v
V.I.C.	49	-1.27v	50mA	-1.2 v	50mA	-.878v	-.865v

* Input voltage was recorded with gate input current of -12mA

** Input current was recorded with the input voltage set at -1.5v. In many cases -1.5 volts was not reached since currents became excessive and the test was stopped to prevent device damage.

*** Tests were performed per specification MIL-M-38510/1 (device type 04 case D) test step numbers refer to table designations per the specification.

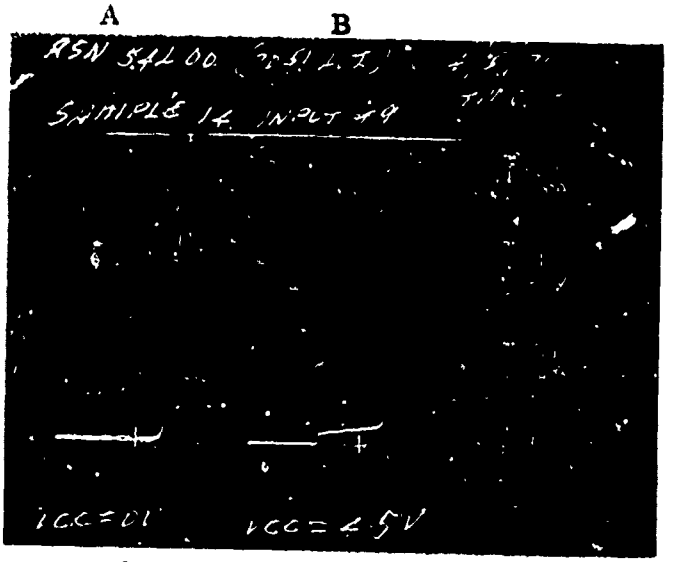


Figure 4.22 Photo 1
Vendor E 5400 radiation-hardened, low-power integrated circuit - although it is not shown in the picture, this sample failed the clamping specification of -12ma @ V_{in} $\leq$ -1.5v for standard devices. Not shown on curve B is a secondary break similar to that on curve 2B. The break occurred at -12ma and -2.7 volts. All radiation-hardened, low-power devices are manufactured with clamp diodes. Test criteria should be different from standard device test limits.

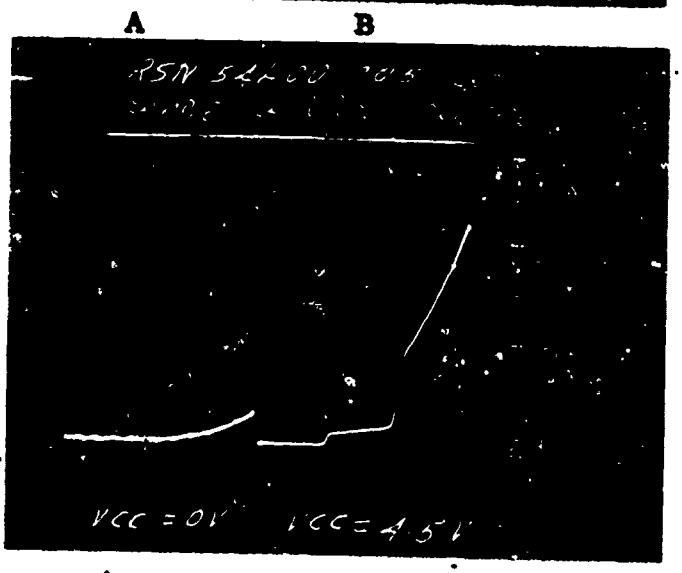


Figure 4.23 Photo 2

Vendor E 5400 radiation-hardened, low-power integrated circuit - This characteristic exhibits two distinct breaks followed by a low and then a high impedance region.

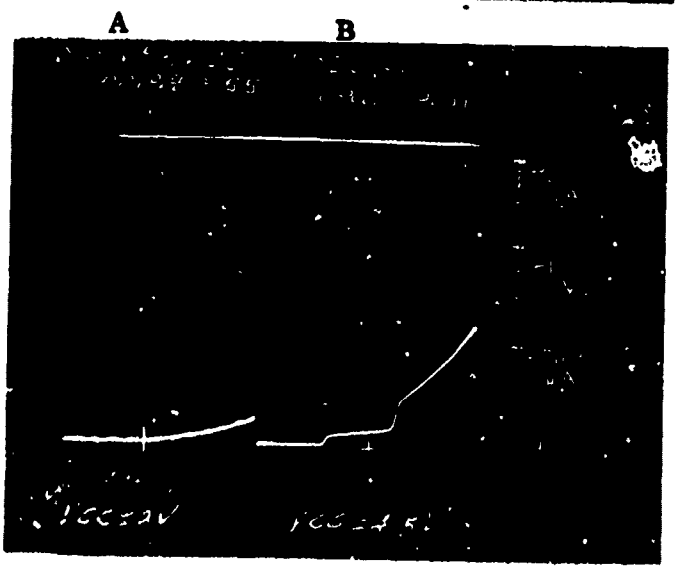


Figure 4.24 Photo 3

Vendor E 5400 radiation-hardened, low-power integrated circuit - The secondary break for this clamp characteristic occurs at a low current level, approximately -300μa. Because the secondary breaks seem to occur at low current levels for the RH, low-power devices, not much latitude is left for specifying reasonable test limits.

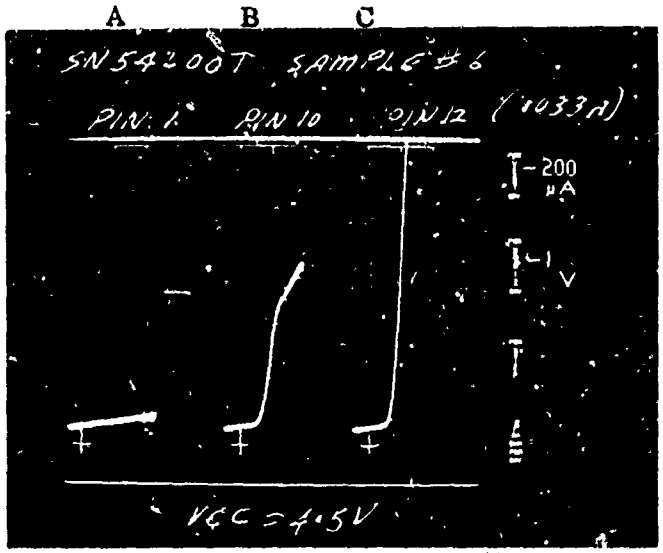


Figure 4.25 Photo 4
Vendor E 5400 low-power integrated circuit - Three different input characteristics, all of which were exhibited on one integrated circuit. Characteristic waveform (A) was not typical. It occurred approximately nine times out of 352 inputs tested.
Not shown on curve "C" was a secondary break similar to that on waveform B. The break occurred at -5ma and -1.7 volts. Refer to Figure 4.17, test no. 43, (for this sample) for backup data for waveform "A".

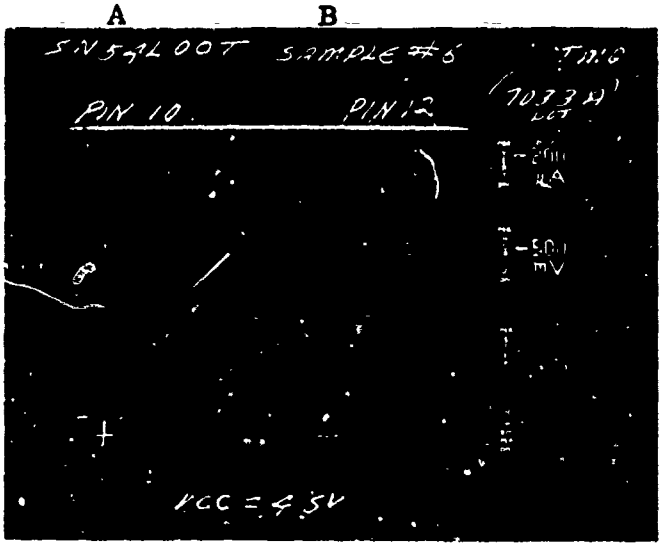


Figure 4.26 Photo 5

Vendor E 5400 low-level integrated circuit.

Normal low-power devices, as a rule, will not have clamp diodes. These curves are not much different from the RH low-power characteristics (which have clamp diodes). Also low-power devices should not be expected to meet clamp test criteria established for standard devices.

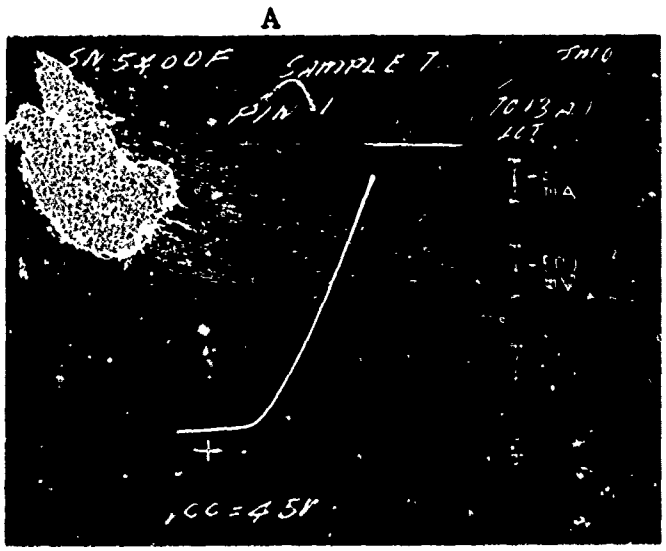


Figure 4.27 Photo 6

Vendor E 5400 standard integrated circuit. The characteristic shown was typical for standard device gates. The characteristic has a soft break followed by a relatively high impedance region. Some of these gate inputs nearly met the V.I.C. test criteria.

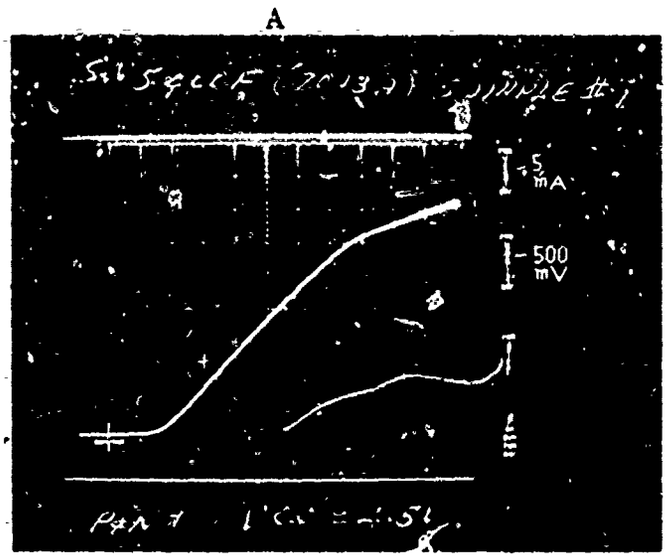


Figure 4.28 Photo 7

Vendor E 5400 standard integrated circuit. This lot of devices did not meet test criteria - Note the secondary break.

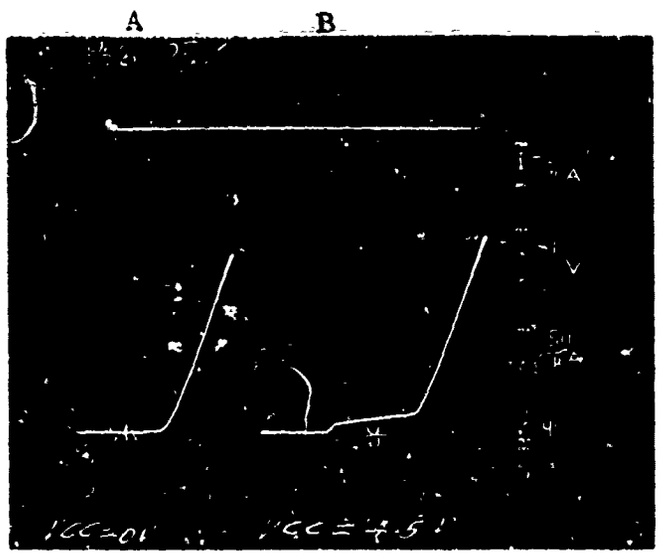


Figure 4.29 Photo 8

Vendor B Diode - transistor 900 series integrated circuit.

This picture affords a comparison for T^2L circuitry. Note that the characteristic breaks at approximately -1.2 volts.

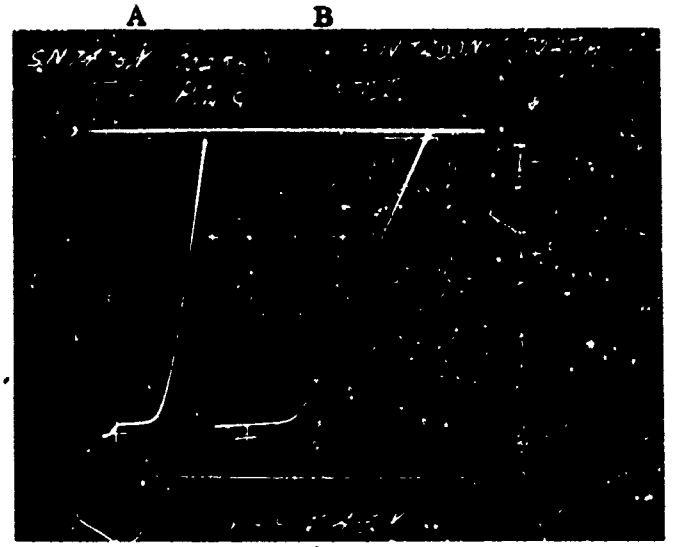


Figure 4.30 Photo 9

Vendor E 7400 series standard integrated circuits.

Waveform A - low forward impedance characteristic (All inputs including clocks - no sec. breaks)
Waveform B - high forward impedance characteristic

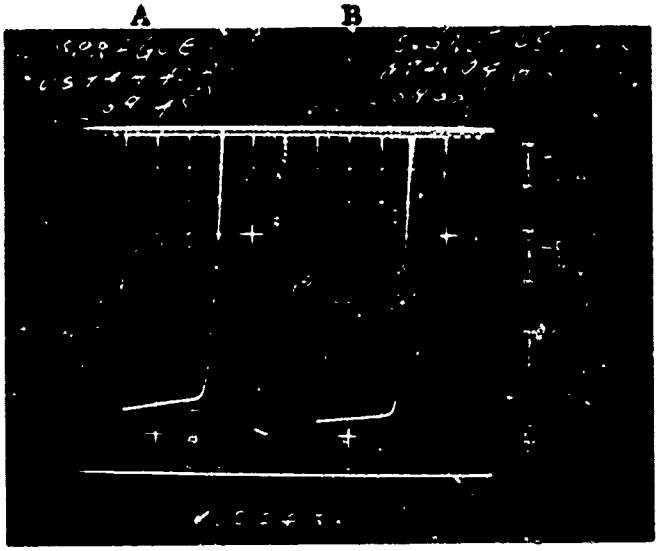


Figure 4.31 Photo 10

Vendor G and Vendor H 7400 series high power integrated circuits.

Secondary breaks were not found in these samples, even at several hundred ma of current.

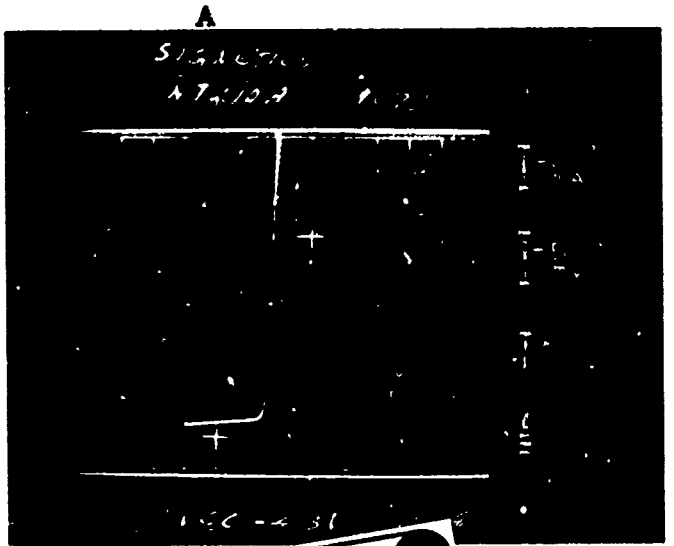


Figure 4.32 Photo 11

Vendor H 7400 series standard integrated circuit.

This device probably has clamp diodes.

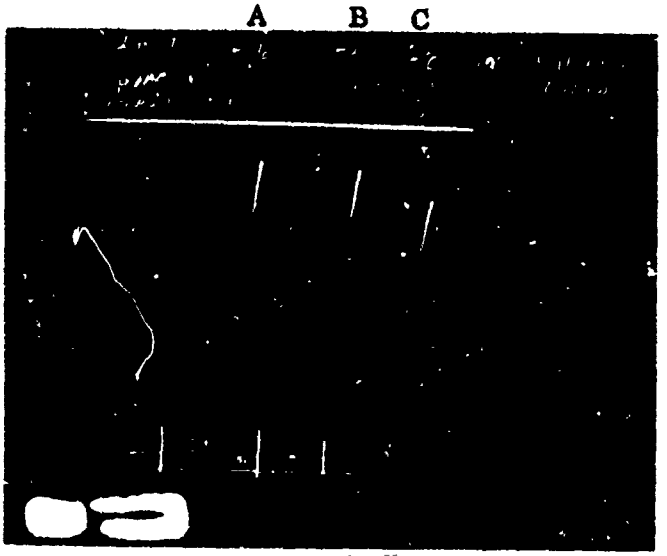


Figure 4.33 Photo 12

Vendor E 5400 high speed integrated circuits.

These devices are illustrated and sold as having clamp diodes. The test criteria established in MIL-M-38510/1 for clamp diodes for standard devices is easily met.

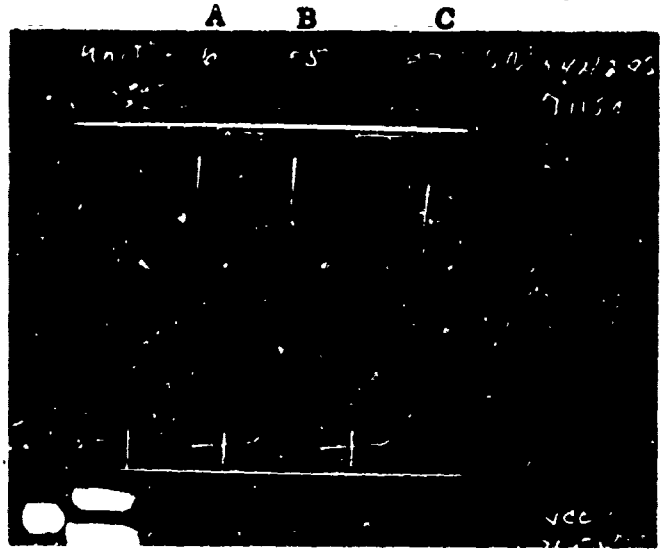


Figure 4.34 Photo 13

Vendor E 5400 high-speed integrated circuits.

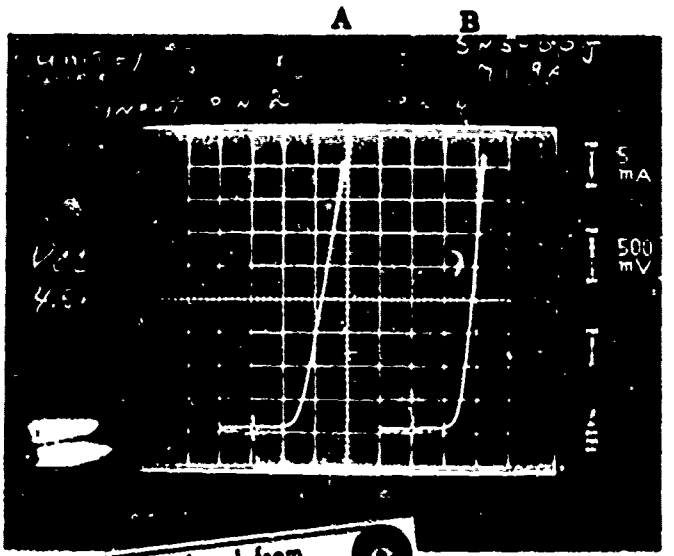


Figure 4.35 Photo 14

Vendor E standard 5400 integrated circuits. These units were sent as samples having input clamp diodes.

These curves and further test results verify this (see Figures 4.15 and 4.16 this section). Refer to pictures #15 and #16.

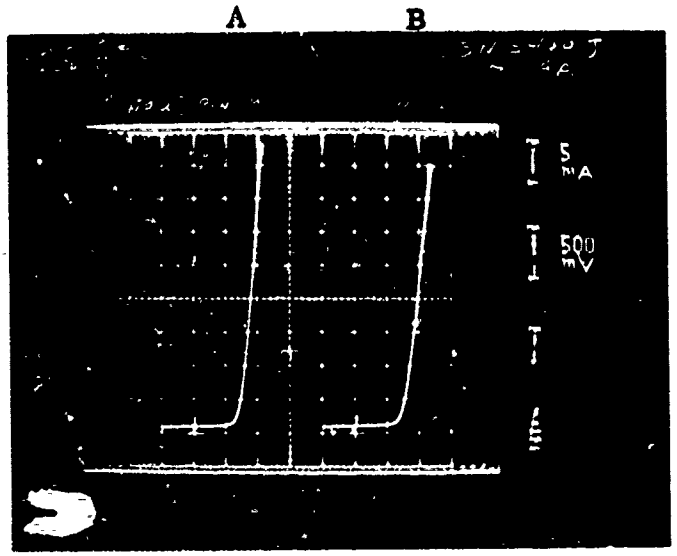


Figure 4.36 Photo 15

Vendor E standard 5400 integrated circuits.

These units were sent as samples having input clamp diodes.

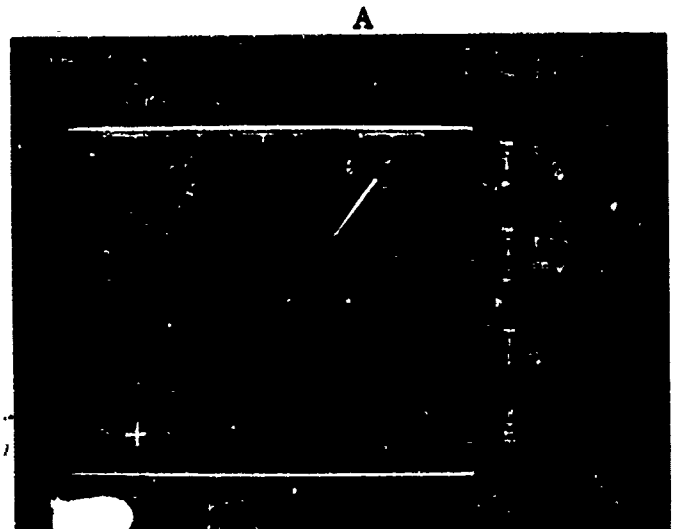


Figure 4.37 Photo 16

Vendor E standard 5400 integrated circuit. This unit was sent as a sample, having input clamp diodes. Note that it passes V.I.C. test criteria (-12ma at V_{in} -1.5v) and has no secondary break at a current of -350ma and a voltage of -3.5 volts. Test results verify the clamp diode (see Figures 4.15 and 4.16 this section).

4.5 Transfer Characteristics

The following curves display typical transfer characteristics of low-power, standard, and high-speed Vendor E T^2L general-purpose nand gates. Each picture is a triple exposure illustrating a gate's performance at each of the following temperatures: -55°C, +25°C, and +125°C.

General characteristics of each device class may be compared; however, if data is extracted from the curves, it must be done judiciously because of oscilloscope inaccuracies.

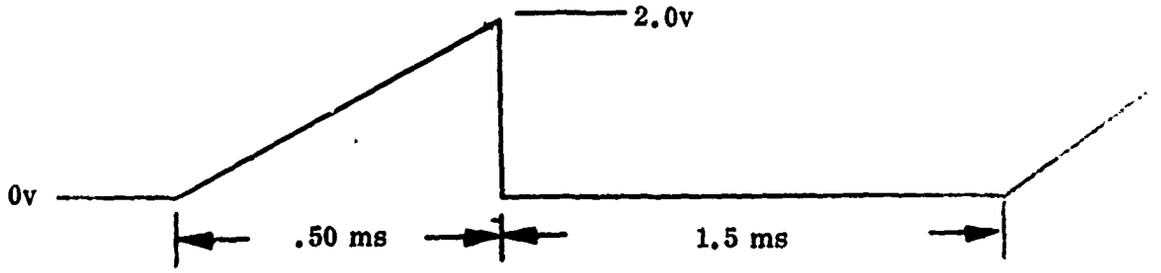
In particular, some differences were noted in gate thresholds. The high-speed devices had the highest thresholds, while the standard and radiation-hardened, low-power devices were lower. The normal low-power devices had the lowest thresholds. Vendor E's Integrated Circuits Catalog for Design Engineers (1971 edition) shows the following:

	Normal Low Power Devices	Radiation-Hardened, Low-Power Devices	Normal Standard Devices	Normal High-Speed Devices
Max low level Output Voltage (V_{OL})	0.3v	0.3v	0.4v	0.4v
Max low level Input Voltage (V_{IL})	0.7v	0.8v	0.8v	0.8v

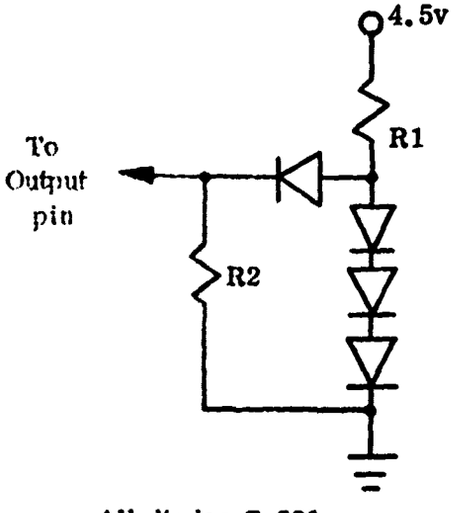
The data breakdown of V_{OL} measurements (Figure 4.14) did show that the low power devices had V_{OL}'s 0.1 volts lower than the standard devices (V_{OL} data for high speed devices was not taken). Figure 4.14 data and the following transfer characteristics tend to backup the manufacturer's claims on thresholds and V_{OL} voltages. One result of all this is that the low-level noise margin is 0.1 volts greater for the low-power, radiation-hardened devices.

The logic "1" noise margin suffers as a result of the shape of the transfer characteristics for all devices. At an input voltage of approximately 0.3 volts, the output voltage starts dropping. The resulting minimum V_{OH} is a specified low of 2.4 volts. This allows only 0.4 volts of noise margin since the guaranteed minimum logic "1" voltage is 2.0 volts.

GATE INPUT WAVEFORM



OUTPUT LOAD



All diodes G-321

Device Power Rating	R1	R2
Low power	2.1K	24K
Intermediate power	256Ω	6.19K
High power	205Ω	4.1°K

Figure 4.38. Transfer Characteristics for Vendor E's Low-Power, Standard, and High-Speed 5400 Series T^2L Integrated Circuits

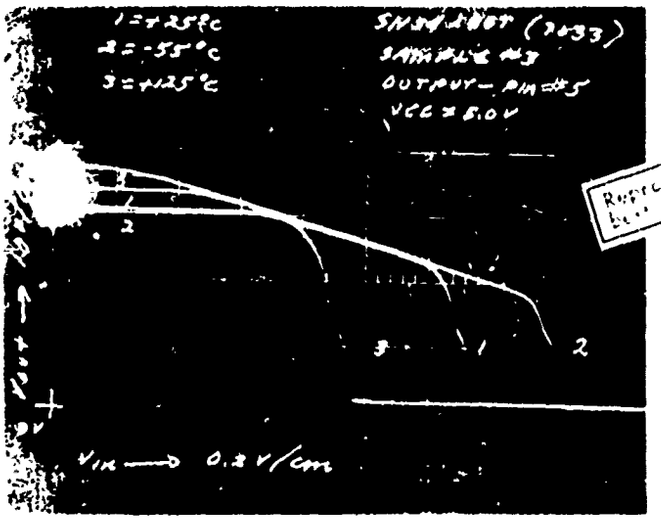


Figure 4.39 Photo 17

SN54L00T

Lot 7033

Sample #3

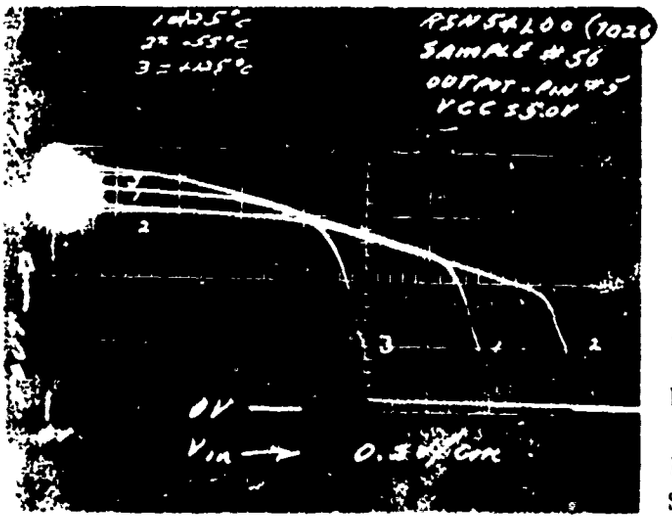


Figure 4.40 Photo 1

RSN54L00

Lot 7026

Sample #56

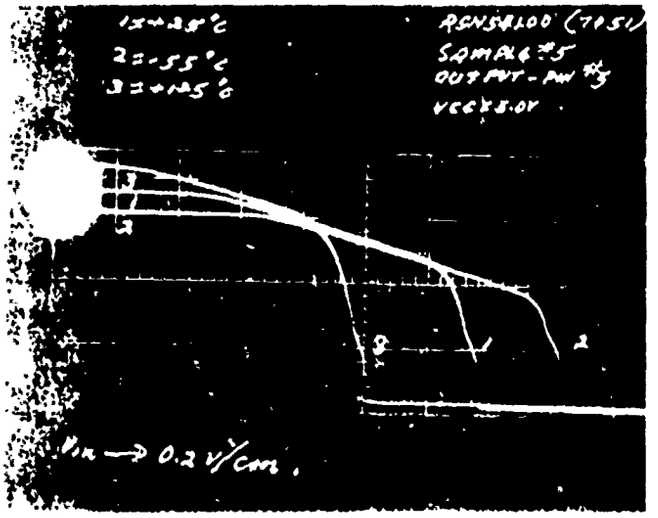


Figure 4.41 Photo 1

RSN54L00

Lot 7051

Sample #5

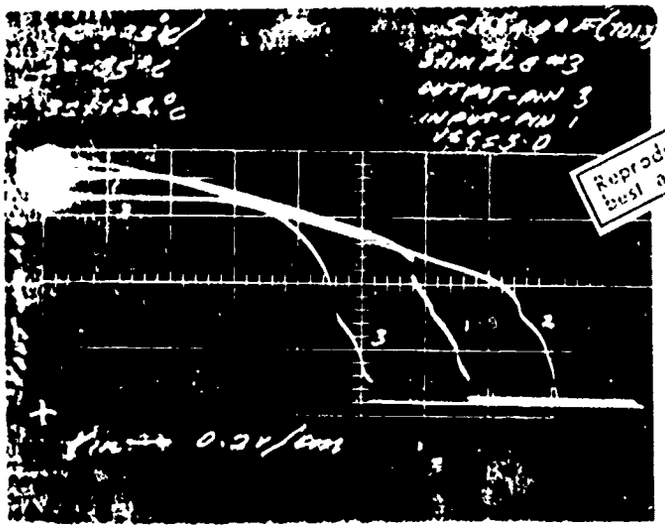


Figure 4.42 Photo

SN5400F

Lot 7013
Sample #4

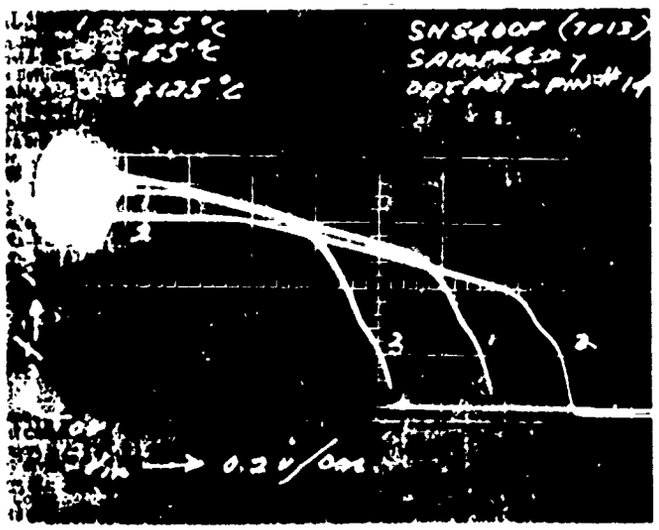


Figure 4.43 Photo

SN5400F

Lot 7013
Sample #7

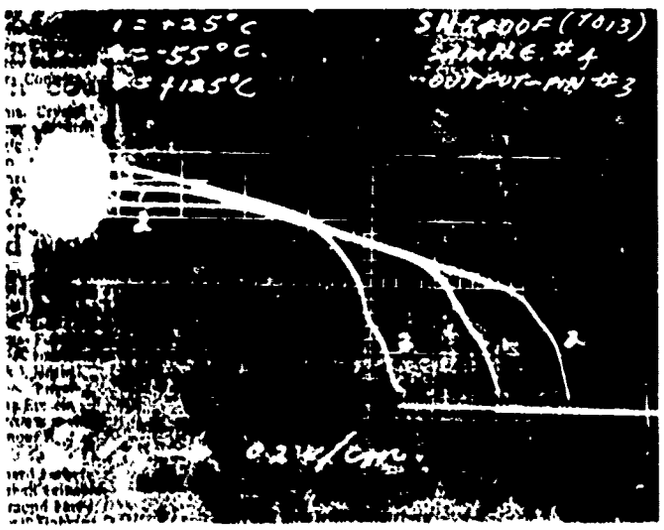


Figure 4.44

SN5400

Lot 70
Sam

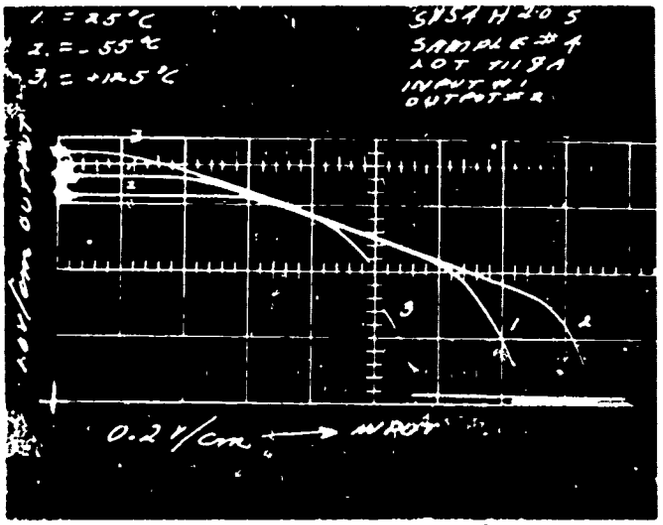


Figure 4.4 - Photo [illegible]

SN54H20S

Lot 711SA
Sample #4

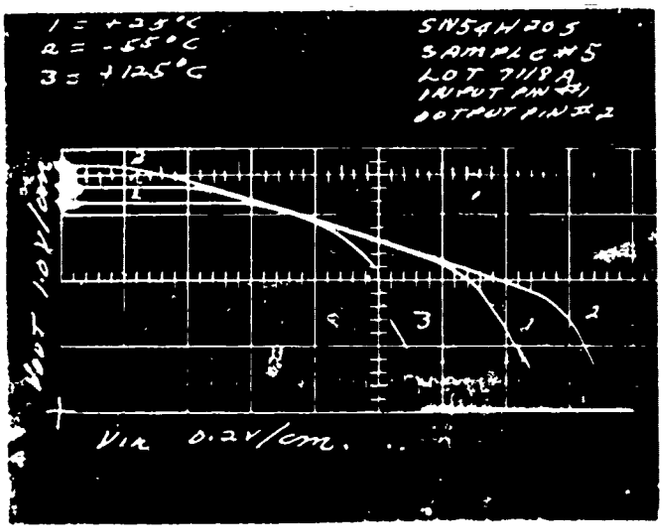


Figure 4.5 Photo [illegible]

SN54H20S

Lot 711SA
Sample #5

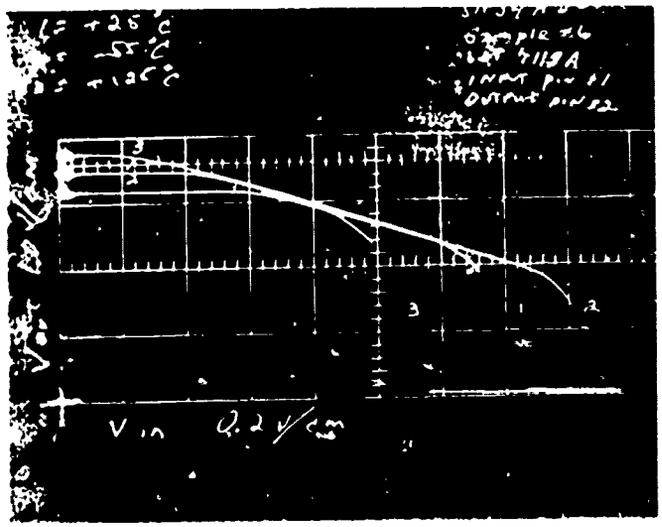


Figure 4.[illegible] Photo [illegible]

SN54H20S

Lot 711SA
Sample #6

4.6 Vendor Survey

Four vendor's lines of standard T^2L nand gates were compared. Standard nand gates were compared for similarity of test and specification and ultimately for compatibility. The vendors were:

1. Vendor E
2. Vendor D
3. Vendor C
4. Vendor F

Since the compared gates are representative of product line families, the comparison should still be valid for other devices in those families.

Vendor D stresses low temperature range devices. Therefore, many of their products are specified with min/max power supply voltages of ±5 percent over a 0°C to 70°C temperature range. The same test limits, however, apply to full temperature range units (-55°C to +125°C) with ±10 percent power supply tolerances.

All of the above vendors tested all specified parameters identically and to the same limits, except for power supply current drain and propagation delay.

Shown below in tabular form are the individual vendor specifications for power supply current drain. The test configurations are the same.

Logic (0) (I_{CCL})
Logic (1) (I_{CCH})

	Vendor E	Vendor C	Vendor F	Vendor D
	-55°C to +125°C V_{CC} = 5.5V	-55°C to +125°C V_{CC} = 5.0V	25°C V_{CC} = 5.0V	-55°C to +125° V_{CC} = 5.5V
I_{CCL}	22ma max	20.4ma max	12ma	20.4ma max
I_{CCH}	8ma max	7.2ma max	4ma	7.2ma max

Figure 4.48. SN5400 - Power Supply Current Drain

Given the same voltage and environmental conditions the power supply current drain limits would probably all be the same. The circuit designs are the same, but circuit resistor values do vary slightly.

Shown below, Figures 4.49 through 4.51, are the propagation delay time test configurations for each of the four vendors.

Propagation Delay Time

t_{PHL} t_{PLH}

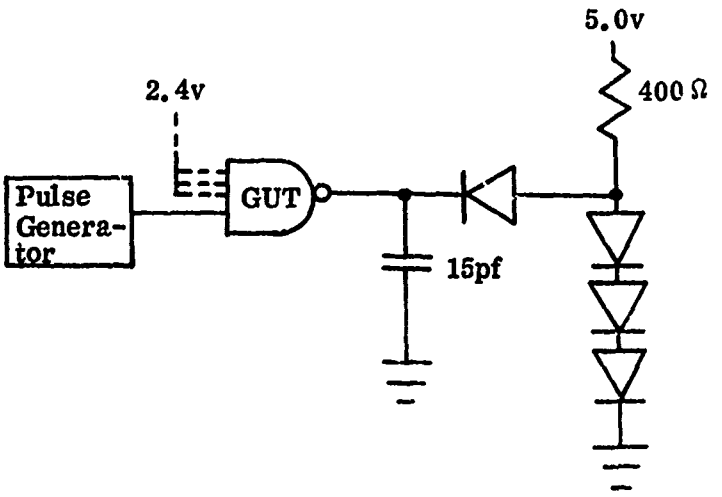


Figure 4.49. Vendor E - Test Circuit

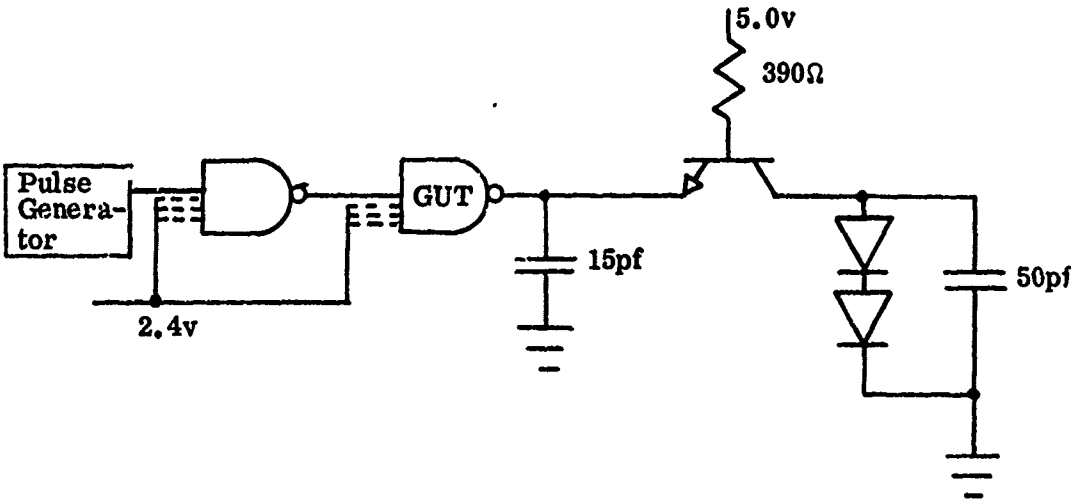


Figure 4.50. Vendors C and F-Test Circuit

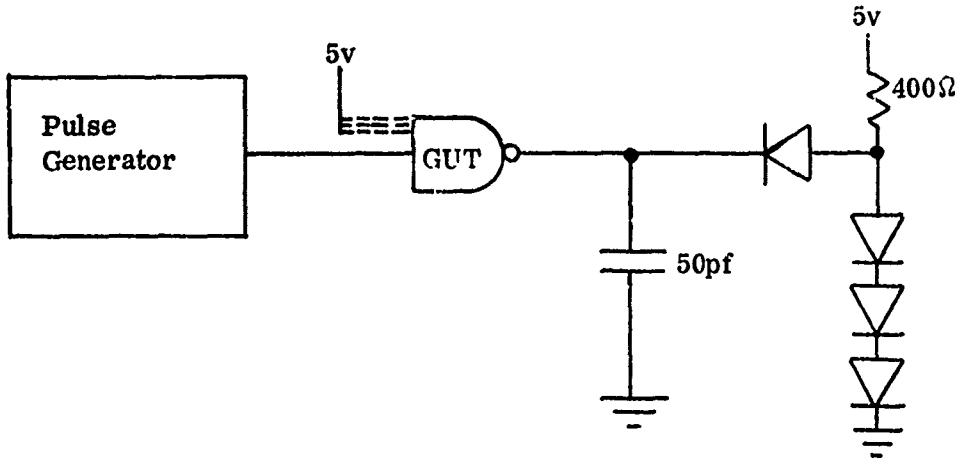


Figure 4.51. Vendor D - Test Circuit

	Propagation Delays V_{CC} = 5.0V Temperature = +125°C			
	Vendor E	Vendor C	Vendor F	Vendor D
t_{PHL}	15ns max	15ns max	15ns max	15ns max
t_{PLH}	22ns max	29ns max	29ns max	25ns[2] max

Figure 4.52 Comparison of Vendor Propagation Delay Limits

Note 1: All delays are measured from the 1.5 volt level on the input pulse to the 1.5 volt level on the output pulse (measured from ground).

Note 2: Delay reflects a 50pf capacitive load.

Vendor C's and Vendor F's propagation delay test circuits are exactly the same, but they are configured differently from the other vendor loads. The main difference with the load is the addition of a 50pf capacitor from circuit ground to the collector of the load input transistor. This capacitor will make transitions to a logic 1 longer. The exact increase in time has not been determined; however, previous experience (see comments, Figure 4.12) has shown that it should be small relative to the actual delay. The maximum t_{PLH} limit with this load is several nanoseconds longer than it is for the same device tested with loads not having the additional capacitor.

Vendor C's and Vendor F's propagation delay test circuits are exactly the same, but they are configured differently from the other vendor loads. The main difference with the load is the addition of a 50pf capacitor from circuit ground to the collector of the load input transistor. This capacitor will make transitions to a logic 1 longer. The exact increase in time has not been determined; however, previous experience (see comments, Figure 4.12) has shown that it should be small relative to the actual delay. The maximum t_{PLH} limit with this load is several nanoseconds longer than it is for the same device tested with loads not having the additional capacitor.

Vendor E's and Vendor D's test circuits show the GUT being driven directly by pulse generators. Vendor C's and Vendor F's drive the GUT with another gate.

Vendor's F and D were the only vendors that specified voltage/current criteria for the input clamping diodes. They each used different device power supply voltages for the same limits (less than -12ma at -1.5 volts min. input voltage). The limits specified are used in MIL-M-38510/1 (V.I.C. tests). Since device power supply voltage is not an important constraint for this measurement, the input clamp characteristics for the Vendor F and Vendor D devices are specified to the same clamping criteria.

Vendor's D and E are the only vendors that displayed typical performance curves in their catalogs. The propagation delay characteristics for these two vendors are shaped differently over the temperature range of the devices. The Vendor D characteristics are somewhat cup shaped while the Vendor E delay characteristics are more linear. The 50pf load delay characteristic (propagation delay to logic "0") for both vendors are similar and in fact have similar delays. However, the Vendor E propagation delay curve (to a logic "1" level) for a 15pf load compares to the Vendor D curve for a 50pf load. Note that propagation delay tests performed to MIL-M-38510/1 specify 50pf capacitive loads and a 25ns (t_{PLH}) maximum limit. This is the same limit that Vendor D specifies. Tests performed in earlier sections of this report show that Vendor E devices will meet these delay requirements.

The conclusion is that the Vendor E device propagation delay low-to-high level output is conservatively specified in the catalog; also, Vendor D may be willing to exercise some control on their devices to guarantee meeting the maximum propagation delay limit with a 50pf load capacitor. All vendors could probably pass the MIL-M-38510/1 t_{PLH} delay requirements.

5400 series T^2L devices from the above vendors are compatible with each other and are, in fact, specified in similar manners to similar limits.

Section V

VENDOR ANALYSIS OF 741 OPERATIONAL AMPLIFIER

5.0 General

Forty 741A operational amplifiers were purchased "off-the-shelf" from four different vendors. These vendors were not informed of the proposed use of their devices, nor were samples selected. All units were in standard eight-pin metal can. The date codes for each vendor's part was as follows: A(7117), B(7111), C(7021), and D(7106). From the forty devices, twenty-eight units (seven per vendor) were randomly selected and tested at 25°C and in accordance with the test conditions, procedures, and limits of MIL-M-38510/101. Eight units (two per vendor) of the twenty-eight were also tested at -55°C and +125°C.

Paragraphs 5.1 and 5.2 will include the test circuit and test equipment used and the conditions under which each test was performed; in addition these paragraphs will outline some of the troublesome areas in testing and in calculating test results.

Paragraph 5.3 will include, parameter by parameter, results of testing the various samples. The vendors are listed in alphabetical order for each condition, not in order of results. It should be noted that in the conditions applicable, absolute numbers were used in order to give a meaningful analysis of the data. The test data is presented as follows:

> a) Number of samples tested, b) number of samples allowed (this was done to weed out the obvious errors in testing; for example, if all readings for input impedance were around 10 Megohms and one reading was 2000 Megohms, then it would be disallowed, c) min and max readings over the samples taken, d) average Δ from 25° (this would be a measure of change of the two units which were checked at the temperature extremes as well as 25°C), e) maximum Δ from 25°C.

Paragraph 5.4 summarizes the results obtained on all tests and establishes a figure of merit for each of the four vendors investigated.

Finally, paragraph 5.5 will show the results of noise measurements taken for all vendors. General Electric Ordnance Systems (GEOS) feels it is of extreme importance in sensitive analog applications and should be controlled because it puts a definite limit on usefulness of amplifiers in high-gain and high-impedance circuits.

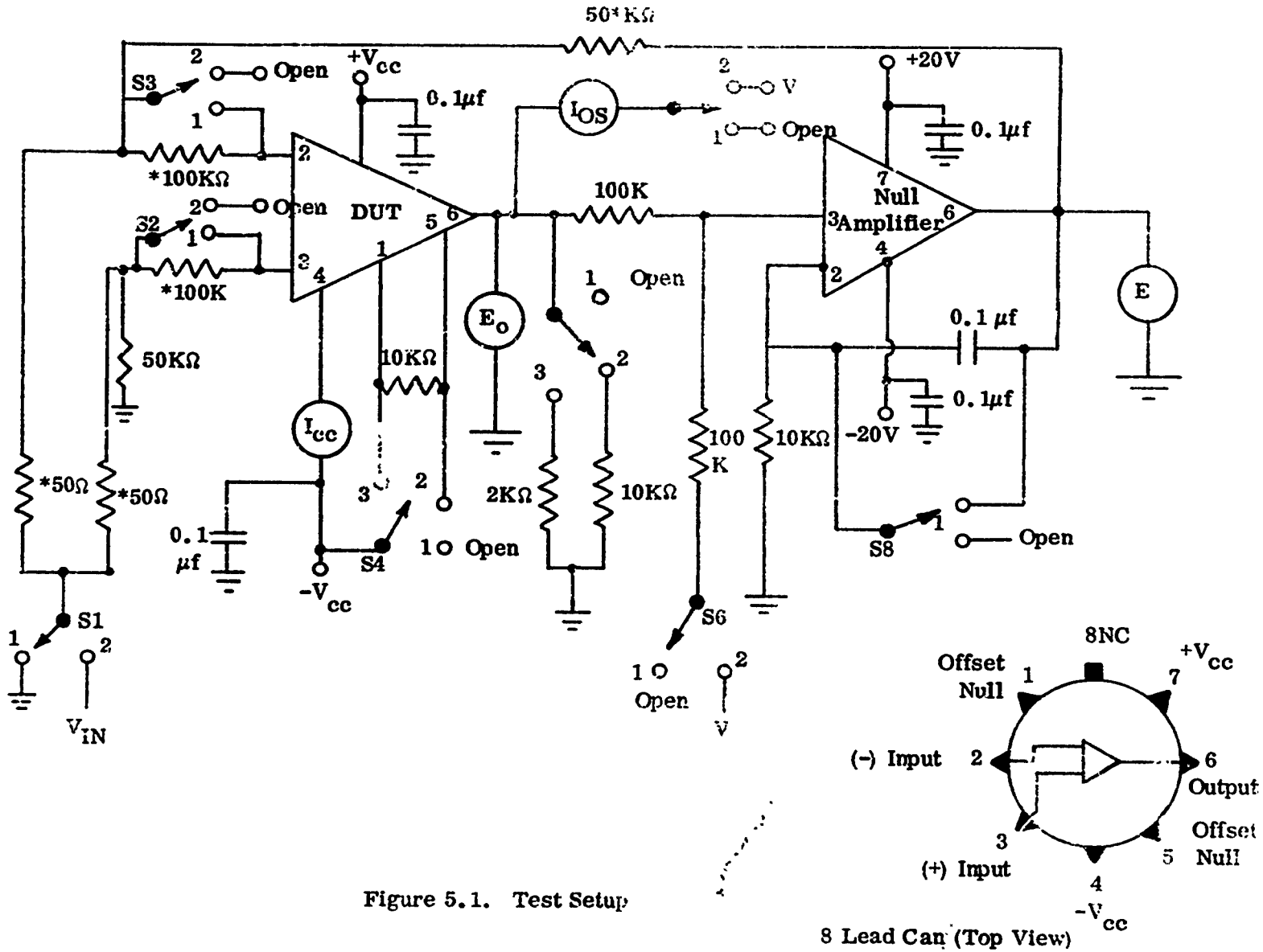


Figure 5.1. Test Setup

8 Lead Can (Top View)

Parameter	Sect.	Apply (in volts) +Vcc	-Vcc	V_{IN}	V	Switch positions S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	Measure Value	Units	Measured parameter Equation	Units
V_{IO}	5.3.1	20	-20	---	---	1	1	1	1	1	1	1	1	E_1	mV	$V_{IO} = \frac{E_1}{1000}$	mV
I_{IO}	5.3.2	20	-20	---	---	1	2	2	1	1	1	1	1	E_2	mV	$I_{IO} = \frac{E_1 - E_2}{100}$	nA
$+I_{IB}$	5.3.5	20	-20	---	---	1	2	1	1	1	1	1	1	E_3	mV	$+I_{IB} = \frac{E_1 - E_3}{100}$	nA
$-I_{IB}$	5.3.5	20	-20	---	---	1	1	2	1	1	1	1	1	E_4	mV	$-I_{IB} = \frac{E_1 - E_4}{100}$	nA
I_{IB}	5.3.5	Calculation														$I_{IB} = \frac{E_4 - E_3}{200}$	nA
+PSRR	5.3.6	5	-20	---	---	1	2	2	1	1	1	1	1	E_5	mV	$+PSRR = 20 \log \left[\frac{15 \times 10^6}{E_1 - E_5}\right]$	dB
-PSRR	5.3.7	20	-5	---	---	1	2	2	1	1	1	1	1	E_6	mV	$-PSRR = 20 \log \left[\frac{15 \times 10^6}{E_1 - E_6}\right]$	dB
CMRR	5.3.8	20	-20	+15	---	2	1	1	1	1	1	1	1	E_7	mV	$CMRR = 20 \log \left[\frac{30 \times 10^6}{E_7 - E_8}\right]$	dB
		20	-20	-15	---	2	1	1	1	1	1	1	1	E_8	mV		
V_{IO} ADJ. (+)	5.3.9	20	-20	---	---	1	1	1	2	1	1	1	1	E_9	mV	$V_{IO\ ADJ.(+)} = \frac{(E_1 - E_9)}{1000}$	mV
V_{IO} ADJ. (-)	5.3.10	20	-20	---	---	1	1	1	3	1	1	1	1	E_{10}	mV	$V_{IO\ ADJ.(-)} = \frac{(E_1 - E_{10})}{1000}$	mV
I_{OS}	5.3.11	15	-15	---	-15	1	1	1	1	1	2	2	1	I_{OS_1}	mA	$I_{OS(+)} = I_{OS_1}$	mA
I_{OS}	5.3.12	15	-15	---	+15	1	1	1	1	1	2	2	1	I_{OS_2}	mA	$I_{OS(-)} = I_{OS_2}$	mA
P_D	5.3.13	20	-20	---	---	1	1	1	1	1	1	1	1	I_{CC}	mA	$P_D = 40 \times I_{CC}$	mW
N_I	5.5	20	-20	---	---	1	2	2	1	1	1	1	2	E_{19}	mv	$N_I = E_{19}/1000$	μV

Figure 5.2 - Test Condition Used With 741 Tester (continued)

Ammeter	Sect.	Apply (in volts) +VCC	-VCC	V_{IN}	V	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	Measure Value	Units	Measured parameter Equation	Units
V_{IOZ}	-	20	-20	---	+10	1	1	1	1	1	2	1	1	E_{11}	mV		
$Z_{is(+)}$	5.3.14	20	-20	---	+10	1	2	1	1	1	2	1	1	E_{12}	mV	$Z_{is} = \frac{\lvert E_{11} - E_1 \rvert \times 100}{\lvert (E_1 - E_3) - (E_{11} - E_{12}) \rvert}$	Meg ohm
$Z_{is(-)}$	5.3.15	20	-20	---	+10	1	1	2	1	1	2	1	1	E_{13}	mV	$Z_{is} = \frac{\lvert E_{11} - E_1 \rvert \times 100}{\lvert (E_4 - E_1) - (E_{13} - E_{11}) \rvert}$	Meg ohm
$+V_{OPP}$ $R_L = 10K\Omega$	5.3.16	20	-20	---	-20	1	1	1	1	2	2	1	1	E_{01}	V	$V_{OPP} = \lvert E_{01} - E_{02} \rvert$	V
$-V_{OPP}$ $R_L = 10K\Omega$	5.3.16	20	-20	---	+20	1	1	1	1	2	2	1	1	E_{02}	V		V
$+V_{OPP}$ $R_L = 2K\Omega$	5.3.17	20	-20	---	-20	1	1	1	1	3	2	1	1	E_{03}	V		V
$-V_{OPP}$ $R_L = 2K\Omega$	5.3.17	20	-20	---	+20	1	1	1	1	3	2	1	1	E_{04}	V	$V_{OPP} = \lvert E_{03} - E_{04} \rvert$	V
+Avs $R_L = 2K\Omega$	5.3.18	20	-20	---	-15	1	1	1	1	3	2	1	1	E_{14}	mV	$+A_{vs} = \left\lvert \frac{15}{(E_1 - E_{14})} \right\rvert$	V/mv
-Avs $R_L = 2K\Omega$	5.3.18	20	-20	---	+15	1	1	1	1	3	2	1	1	E_{15}	mV	$-Avs = \left\lvert \frac{15}{(E_1 - E_{15})} \right\rvert$	V/mv
V_{IOA}	-	5	-5	---	---	1	1	1	1	1	1	1	1	E_{16}	mV		
+Avs $R_L = 2K\Omega$	5.3.19	5	-5	---	-2	1	1	1	1	3	2	1	1	E_{17}	mV	$+Avs = \left\lvert \frac{2}{(E_{16} - E_{17})} \right\rvert$	V/mv
-Avs $R_L = 2K\Omega$	5.3.19	5	-5	---	+2	1	1	1	1	3	2	1	1	E_{18}	mV	$-A = \left\lvert \frac{2}{(E_{16} - E_{18})} \right\rvert$	V/mv

Figure 5.2 – Test Condition Used With 741 Tester (concluded)

5.1 Test Setup

The test setup of Figure 5.1 was used in conjunction with the switch positions and voltages shown in Figure 5.2. A computer program was developed to change data in raw form (E1, E2, etc.) to spec requirements.

The following test equipment was used for all tests:

- d.c. supplies - Harrison 6200B
- DV voltmeter - Fairchild 7000A
- DV ammeter - HP 428B
- Temperature chamber, Statham

The oven temperature was allowed to stabilize for three hours with bias power applied to the units before readings were taken. Ambient temperatures were held to within ±3°C.

5.2 Analysis of Test Circuit

5.2.1 Measurement Accuracy Determination

All measurements except Power Supply Rejection Ratio (PSRR), Common Mode Rejection Ratio (CMRR), and Input Impedance (Zis) require simple formula conversions to yield the calculated parameter. For two-place accuracy on the parameter, three places are required on the measurement. The required number of places on the measurements of PSRR, CMRR, and Zis is determined below.

Power Supply Rejection Ratio (PSRR) - Given that

$$PSRR = 20 \log \left\{ \frac{15 \times 10^6}{|E_1 - E_5|} \right\}$$ our problem is to determine the equipment accuracy required to measure E_1 and E_5 to insure two-place accuracy of PSRR. (i.e., d(PSRR) = ±.1 when PSRR = 86)

$$PSRR = 20 \log \left\{ \frac{15 \times 10^6}{|E_1 - E_5|} \right\} = 143.5 - 20 \log \left\{ |E_1 - E_5| \right\}$$ and $|E_1 - E_5| = .752$ when PSRR = 86. Taking the derivative of the above equation

$$d(PSRR) = (-20 \log e) \frac{d(|E_1 - E_5|)}{|E_1 - E_5|}$$

$$\frac{d(|E_1 - E_5|)}{|E_1 - E_5|} = -.1152\, d(PSRR)$$

For $|E_1 - E_5| = .752$ mv; d(PSRR) = ±.1db

$d(|E_1 - E_5|) = \pm 8.67$ mv

Therefore, E_1 and E_5 will each require accuracy to ±.0043V. Since typically E_1 and E_5 are measured in volts, the instrument readout must contain four places. The equipment accuracy should be good to ±1 mv.

Similarly, the measurement for CMRR will require four-place readout. The measurements requiring four-place readout with ±1 mv accuracy are E_1, E_5, E_6, E_7, and E_8.

Input Impedance

$$Zis = \frac{|E_{11} - E_1| \times 100}{|(E_1 - E_3) - (E_{11} - E_{12})|}$$

$$= \frac{|E_{11} - E_1| \times 100}{|I_{IBO} - I_{IBV}|}$$

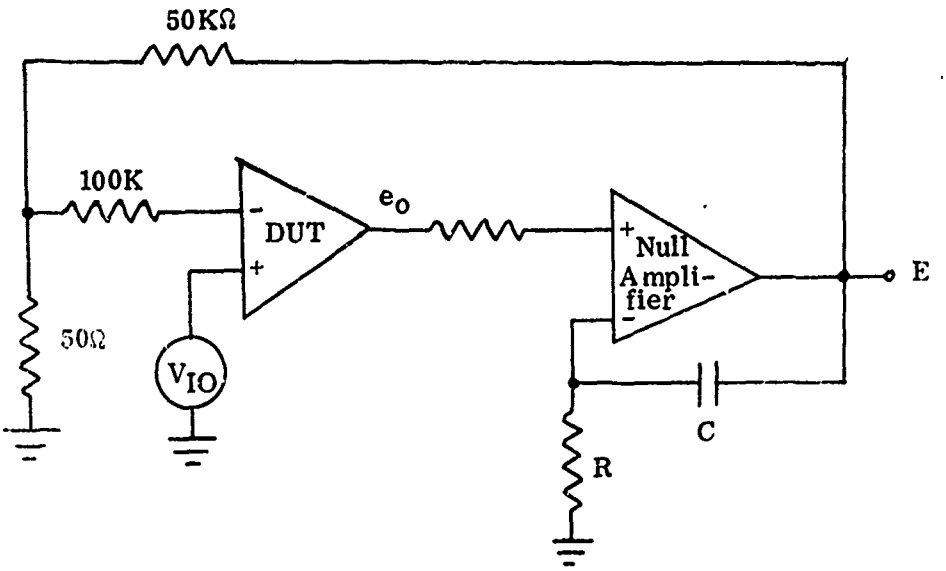
$$d\,Zis = \frac{(I_{IBO} - I_{IBV})\,0 - |E_{11} - E_1| \times 100}{|I_{IBO} - I_{IBV}|^2} d\,I_{IBO}$$

$$= - Zis \frac{dI_{IBO}}{I_{IBO} - I_{IBV}}$$

$$\frac{d\,Zis}{Zis} = - \frac{dI_{IBO}}{I_{IBO} - I_{IBV}}$$

Scaling accuracy for Zis and I_{IBO} is the same. Observation shows that the scaling accuracies for Zis and I_{IBV} are also the same. Three-place accuracy will be sufficient for measurements of E_3, E_{11}, E_{12} and E_{13}.

5.2.2 Analysis of Circuit to Measure E_1 and E_4



$$E = e_o\left(\frac{1}{RC}\right)\left(\frac{1+RCS}{S}\right)$$

$$V_f = \frac{E}{1001}$$

$$e_o = G\,V_{IO} - G\,(V_f - I_{b-}\ (10^5))$$

$$E = \left\{G\,V_{IO} - G\,(V_f - I_{b-}\ (10^5))\right\}\left\{\left(\frac{1}{RC}\right)\left(\frac{1+RCS}{S}\right)\right\}$$

$$= \frac{G}{RC}\left\{V_{IO} - \frac{E}{1001} + I_{b-}\ (10^5)\right\}\left\{\frac{1+RCS}{S}\right\}$$

$$E\left\{1 + \frac{G}{RC}\left(\frac{1}{1001}\right)\left(\frac{1+RCS}{S}\right)\right\} = \frac{G}{RC}\left\{V_{IO} + I_{b-}\ (10^5)\right\}\left(\frac{1+RCS}{S}\right)$$

$$\frac{E}{1001} \approx V_{IO} + I_{b-}\ (10^5)$$

If the 100KΩ resistor is shorted,

$$I_b\,(0) = 0$$

$$\frac{E_1}{1001} = V_{IO}$$

If the 100KΩ resistor is <u>not</u> shorted,

$$\frac{E4}{1001} = V_{IO} + I_b\,(10^5)$$

$$\frac{E4}{1001} = \frac{E1}{1001} + I_b\,(10^5)$$

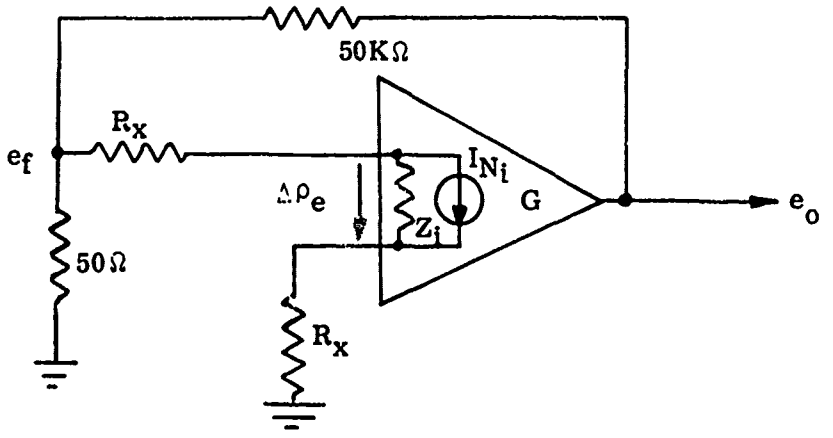
$$I_b = \frac{E4 - E1}{10^8}$$

If E_1 and E_4 are in millivolts,

$$I_b = \frac{E4 - E1}{100} \text{ na.}$$

5.2.3 <u>Noise Circuit Analysis</u>

It has been shown that noise is mostly current generated; therefore, the following circuit will be used for analysis:



$$e_o = G\,(\Delta\,\rho_e)$$

If $R_x >> 50\Omega$

Then $$\Delta\,\rho_e = I_{Ni}\left\{\frac{R_x Z_i/2}{R_x/2 + Z_i}\right\} - e_f\left\{\frac{Z_i}{2\,R_x + Z_i}\right\}$$

$R_{in} >> 2\,R_x$

$$e_o = G\left\{ I_{Ni}\ \frac{R_x}{2} - e_f \right\}$$

also $e_f = \frac{e_o}{1001}$

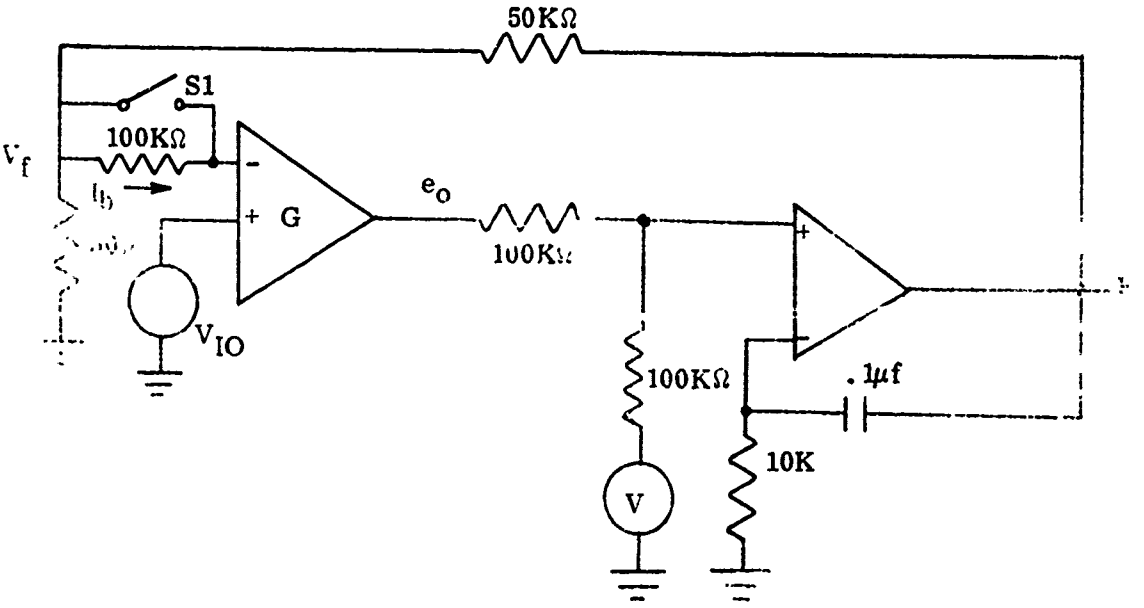
$$e_o\left\{ 1 + \frac{G}{1001} \right\} = G\, I_{Ni}\ \frac{R_x}{2}$$

$$\frac{e_o}{I_{Ni}\ \frac{R_x}{2}} = \frac{1}{1001}\left\{ \frac{G/1001}{1 + G/1001} \right\}$$

Let $V_{Ni} = I_{Ni}\ \frac{R_x}{2}$

Therefore, $\frac{e_o}{V_{Ni}} \simeq \frac{1}{1000}$

Analysis of Circuit to Measure Voltage for Calculation of Zis(-)



S1 open

$$e_o = -G(V_f - I_b(10^5)) + G V_{IO}$$

$$= G\left\{ V_{IO} + I_b(10^5) - V_f \right\}$$

$$E \quad \frac{V + e_o}{2}\left(\frac{1}{RC}\right)$$

$$V_f = \frac{E}{1001} = \left\{\frac{V + e_o}{2}\right\}\left(\frac{1}{RC}\right)\left(\frac{1}{1001}\right)$$

$$E = \frac{V + G\left\{V_{IO} + I_b(10^5) - E/1001\right\}}{2}\frac{1}{RC}$$

$$\left[\frac{V}{2} + \left\{\frac{G V_{IO}}{2} + \frac{G I_b(10^5)}{2} - \frac{GE}{2002}\right\}\right]\left(\frac{1}{RC}\right)$$

$$E\left\{1 - \frac{G}{2}\left(\frac{1}{RC}\right)\left(\frac{1}{1001}\right)\right\} = \left[\frac{V}{2} + \frac{G}{2}\left\{V_{IO} + I_b 10^5\right\}\right]\left(\frac{1}{RC}\right)$$

$$E = \frac{V/2\left(\frac{1}{RC}\right)}{1+\frac{G}{2}\left(\frac{1}{RC}\right)\left(\frac{1}{1001}\right)} + V_{IO}\left\{\frac{\left(\frac{G}{2}\right)\left(\frac{1}{RC}\right)}{1+\left(\frac{G}{2}\right)\left(\frac{1}{RC}\right)\left(\frac{1}{1001}\right)}\right\}$$

$$+ I_b\,(10^5)\left\{\frac{\left(\frac{G}{2}\right)\left(\frac{1}{RC}\right)}{1+\left(\frac{G}{2}\right)\left(\frac{1}{RC}\right)\left(\frac{1}{1001}\right)}\right\}$$

$$= \frac{V/2\left(\frac{1}{RC}\right)}{1+\left(\frac{G}{2}\right)\left(\frac{1}{RC}\right)\left(\frac{1}{1001}\right)} + 1001\,V_{IO} \quad 1001\,I_b\,(10^5)$$

$$\frac{E}{1001} - \frac{(V/2)\left(\frac{1}{RC}\right)\left(\frac{1}{1001}\right)}{1+\left(\frac{G}{2}\right)\left(\frac{1}{RC}\right)\left(\frac{1}{1001}\right)} + V_{IO} \cdot I_b\,(10^5)$$

With S1 short $E = E_{11}$; $V_{IO} = \frac{E_1}{1001}$

$$\frac{E_{11}}{1001} = \frac{(V/2)\left(\frac{1}{RC}\right)\left(\frac{1}{1001}\right)}{1+\left(\frac{G}{2}\right)\left(\frac{1}{RC}\right)\left(\frac{1}{1001}\right)} + \frac{E_1}{1001}$$

$$\frac{E_{11}-E_1}{1001} = \frac{(V/2)\left(\frac{1}{RC}\right)\left(\frac{1}{1001}\right)}{1+\left(\frac{G}{2}\right)\left(\frac{1}{RC}\right)\left(\frac{1}{1001}\right)} = \frac{V}{G}$$

With S1 open $E = E_{13}$; $\frac{V}{G} = \frac{E_{11}-E_1}{1001}$; $V_{IO} = \frac{E_1}{1001}$

$$\frac{E_{13}}{1001} = \frac{E_{11}-E_1}{1001} + \frac{E_1}{1001} + I_b\,(10^5)$$

$$= \frac{E_{11}}{1001} + I_b\,(10^5)$$

$$I_b\ (10^5) = \frac{E_{13} - E_{11}}{1000}$$

$$Zis = \left|\frac{e_i}{i_i}\right|$$

With S1 short $e_i = \frac{|E_{11} - E_1|}{1000}$

$$i_i = I_{bv} - I_{bo}$$

$$= \left\{\frac{E_{13} - E_{11}}{1000} - \frac{E_4 - E_1}{1000}\right\} \frac{1}{10^5}$$

$$Zis = \left\{\frac{|E_{11} - E_1|}{|(E_{13} - E_{11}) - (E_4 - E_1)|}\right\} 10^5$$

If En is expressed in millivolts

$$Zis = \frac{|E_{11} - E_1| \times 100}{|(E_{13} - E_{11}) - (E_4 - E_1)|} \quad \text{Meg ohms}$$

5.2.5 Settling Time of Voltage Readings

The test circuit of paragraph 5.1 was rebuilt in a very tight arrangement, especially with regard to the input circuit to the DUT. Tests E_1 through E_4 were performed in accordance with para. 5.2 on one device from each of the four vendors. This was done to determine the time required for the reading in question to stabilize. The switch positions were set and power (± VCC) was applied simultaneously (manually) and results were plotted using a Visacorder. All units were tested at 25°C. The

results are shown in accompanying figures 5.5 through 5.6. For each test, a percentage was calculated based on the drift from time 0 with respect to the stabilized value (percent change). For example, E_2 from Vendor C changed from 2450 mv at time 0 to 2300 mv at time .5 minutes and finally settled out at 2100 mv after three minutes.

$$\text{percent change (at .5 min)} = \frac{2450 - 2300 \times 100}{2100} = 9.5\%$$

Also, the Δ percent between each increment of time was also calculated (Δ percent change).

NOTE The first .05 min was disregarded due to switching transients, this is considered time zero.

The results of these tests indicate that the parameters which take the longest are E_1 and E_2 and especially the Vendor C and Vendor B parts. It was further noted that the drift was not drastically changed by allowing the units to cool (no power applied) for one hour before applying power.

From analyzing the data, it seems that a wait of at least 30 seconds will allow most of the units to achieve 75 percent to 80 percent of their total drift. After three minutes, no appreciable drift is discernable.

5.3 Test Results

5.3.1 Input Offset Voltage

MIL-M-38510/101; Ref: Table III, tests 1, 14, and 24
Specification: ±3 mv at 25°C, ±4 mv at -55° and +125°
Results:

Vendor	T_A °C	Samp Tested	Samp Allowed	Max	Min	Avg "X"	Avg "Y"	Avg Δ from 25°C	Max Δ from 25°C
A	25	7	7	1.67	.020	.667	.617	NA	NA
	-55	2	2	.837	.054	.445	NA	-.172	-.194
	+125	2	2	.352	.13	.240	NA	-.377	-.391
B	25	7	7	2.94	.09	1.35	1.27	NA	NA
	-55	2	2	.56	.02	.29	NA	-.88	-2.0
	+125	2	2	2.3	.66	1.45	NA	+.18	+.50
C	25	7	7	8.25	.02	2.72	2.0	NA	NA
	-55	2	1	---	---	7.60*	NA	+5.6	---
	+125	2	1	---	---	4.70*	NA	+2.7	---
D	25	7	7	1.5	.18	.55	.44	NA	NA
	-55	2	2	.63	.05	.34	NA	-.10	-.11
	+125	2	2	1.0	.7	.85	NA	+.41	+.54

NOTES:

a) Avg "X" is the average (absolute) for total samples allowed. Avg "Y" is the average (absolute) for two samples used in temperature tests. Δ's for -55° and +125° were calculated by comparing Avg "Y" at 25°C with Avg "X" at -55° and +125°.

b) *indicate out of spec conditions.

c) Signs in Δ columns indicate direction from 25°C.

d) Only one sample on Vendor C was allowed because of burn out of one device at +125° after -55°C and almost all of 125° data taken. Data was not repeatable (this note applies to paragraphs 5 3.1 through 5.3.19.

e) It was noted that if the VCC for the Vendor C units was reduced from ±20v to ±15v, all offset readings dropped well within spec.

	E1		E2		E3		E4	
Time Minutes	% Change	Δ% Change	% Change	Δ % Change	% Change	Δ % Change	% Change	Δ % Change
0	0							
.5	+7.1	7.1	-1.9	1.9	1	0	-1.5	1.5
1.0	+2.3	4.8	-3.8	1.9	1	0	-4.6	3.1
2.0	-1.16	3.46	-5.7	1.9	1	0	-7.8	3.3
3.0	-2.3	.14	-4.7	1.0	1	0	-8.7	.9
4.0	-2.3	0	-3.8	.9	1	0		

Figure 5.3. Vendor A - Test Results

	E1		E2		E3		E4	
Time Minutes	% Change	Δ % Change	% Change	Δ % Change	% Change	Δ % Change	% Change	Δ % Change
0	0		0		0		0	
.5	+30	30	+28	28	-20	20	-8.3	8.3
1.0	+45	15	+35	7	-25	5	-12.5	4.2
2.0	+47	2	+40	5	-25	5	-12.5	0
3.0	+47	0	+42	2	-30	0	-12.5	0
4.0	+47	0	+43	1	-30	0		

Figure 5.4. Vendor B - Test Results

Time Minutes	E1 % Change	Δ % Change	E2 % Change	Δ % Change	E3 % Change	Δ % Change	E4 % Change	Δ % Change
0	0		0		0		0	
.5	-5.6	5.6	-6.5	6.5	1	0	1	0
1.0	-11.5	5.9	-11.0	4.5	1	0	1	0
2.0	-19	7.5	-15	4.0	1	0	1	0
3.0	-23	0	-17.2	2.2	1	0	1	0
4.0	-23	0	-17.2	0	1	0	1	0

Figure 5.5. Vendor C - Test Results

Time Minutes	E1 % Change	Δ % Change	E2 % Change	Δ % Change	E3 % Change	Δ % Change	E4 % Change	Δ % Change
0	0		0		0		0	
.5	+20	20	+10	10	-7.3	7.3	-2	2
1.0	+10	10	0	10	-9.4	2.1	-4	2
2.0	+5	5	0	0	-9.4	0	-4	0
3.0	0	5	0	0	-9.4	0	-6	2
4.0							-6	0

Figure 5.6. Vendor D - Test Results

5.3.2 Input Offset Voltage Temperature Sensitivity

MIL-M-38510/101 Ref: Table III, tests 15 and 25
Specification: ±15uv/°C max
Results:

Vendor	Results
A	+ 2.3
B	-12.9
C	+16.1*
D	- 3.60

NOTES:

a) The total spread of each of the two modules tested at -55° and +125° was divided by 180°. Results are for worst of the two modules (not average).

b) Sign of results were determined as follows.

- + if reading at +125° was more positive than reading at -55°
- - if reading at -55° was more positive than reading at +125°

c) * indicates out of spec condition

5.3.3 Input Offset Current

MIL-M-38510/101 Ref: Table III, tests 2, 16, and 26
Specification: 30 na max at 25°C; 75 na max at -55° and +125°
Results:

Vendor	T_A °C	Samp Tested	Samp Allowed	Max	Min	Avg "X"	Avg "Y"	Avg Δ from 25°C	Max Δ from 25°C
A	25	7	7	4.4	.173	2.49	2.8	NA	NA
	-55	2	2	47.5	39.6	45.0	NA	+42.2	+47.0
	+125	2	2	13.5	2.1	8.3	NA	+5.5	+9.0
B	25	7	7	35.6	4.5	16.04	17.0	NA	NA
	-55	2	2	15.1	2.8	7.7	NA	-9.3	-10.1
	+125	2	2	10.4	1.3	5.8	NA	-11.2	-15.0
C	25	7	7	8.8	3.24	6.4	9.0	NA	NA
	-55	2	1	--	--	244*	NA	+235	--
	+125	2	1	--	--	2.15	NA	-6.85	--
D	25	7	7	2.3	.2	1.7	1.45	NA	NA
	-55	2	2	2.4	.8	1.6	NA	+.15	+.33
	+125	2	2	.5	.3	.4	NA	-1.05	-1.7

NOTES:

a) Avg "X" is the average (absolute) for total samples allowed. Avg "Y" is the average (absolute) for two samples used in temperature tests. Δ's for -55° and +125° were calculated by comparing Avg "Y" at 25°C with Avg "X" at -55° and +125°.

b) * indicate out of spec condition.

c) Signs in Δ columns indicate direction from 25°C.

5.3.4 Input Offset Current Temperature Sensitivity

MIL-M-38510/101 Ref: Table III, tests 18 and 28
Specification: ±.5na/°C from -55° to +125°
±.5na/°C from 25° to +125°

Results:

Vendor	-55° to +25°	+25° to +125°
A	+ .596*	-.047
B	+ .125	-.15
C	+3.15*	+.09
D	+ .0125	-.024

NOTES:

a) The total spread of each of the two modules tested at (-55° to +25°) and (+25° to +125°) was divided by 80° and 100°, respectively. Results are for worst of two modules (not average).

b) Sign of results were determined as follows:

+ if reading was more positive at 25° than at -55°
- if reading was more positive at -55° than at 25°
+ if reading was more positive at 125° than at 25°
- if reading was more positive at 25° than at 125°

c) * denotes out of spec condition.

5.3.5 Input Bias Current

MIL-M-38510/101 Ref: Table III, tests 3, 18, and 28
Specification: 80na max at 25°; 210na max at -55° and +125°
Results:

Vendor	T_A °C	Samp Tested	Samp Allowed	Max	Min	Avg "X"	Avg "Y"	Avg Δ from 25°C	Max Δ from 25°C
A	25	7	7	58.6	15.7	29.3	24.7	NA	NA
	-55	2	2	29.5	28.2	28.8	NA	+4.1	+12.5
	+125	2	2	17.2	9.5	13.4	NA	-11.3	-16.4
B	25	7	7	72.8	28.5	49.25	50.5	NA	NA
	-55	2	2	178	177	177.5	NA	+127	+51
	+125	2	2	30	13	21	NA	-29.5	-42
C	25	7	7	149*	52.6	93.2*	65.7	NA	NA
	-55	2	1	---	---	43	NA	-22.7	--
	+125	2	1	---	---	66.5	NA	+.8	--
D	25	7	7	95*	17.5	47.7	35	NA	NA
	-55	2	2	34.5	13.5	24	NA	-11	-18
	+125	2	2	20.7	11.25	15.9	NA	-19.1	-32

NOTES:

a) Avg "X" is the average (absolute) for total samples allowed. Avg "Y" is the average (absolute) for two samples used in temperature tests. Δ's for -55° and +125° were calculated by comparing Avg "Y" at 25°C with Avg "X" at -55° and +125°.

b) * indicate out of spec condition.

c) Signs in Δ columns indicate direction from 25°C.

5.3.6 Power Supply Rejection Ratio (+)

MIL-M-38510/101 Ref: Table III, test 4
Specification: 86db min at 25°
Results:

Vendor	T_A °C	Samp Tested	Samp Allowed	Max	Min	Avg "X"	Avg "Y"	Avg Δ from 25°C	Max Δ from 25°C
A	25	7	7	105	79.2*	90.8	90.9	NA	NA
	-55	2	2	106	96.7	101.3	NA	+10.4	+24.5
	+125	2	2	118	93.2	105.6	NA	+15.1	+36
B	25	7	7	96.2	89.7	91.7	90.2	NA	NA
	-55	2	2	98.9	91.7	95.3	NA	+ 5.1	+ 8.1
	+125	2	2	91.7	91.2	91.4	NA	+ 1.2	+ 1.2
C	25	7	7	111.5	63.6*	83.1*	76.5*	NA	NA
	-55	2	1	--	--	67.4	NA	- 9.1	--
	+125	2	1	--	--	69.9	NA	- 6.6	--
D	25	7	7	106	79.7*	95.7	99.0	NA	NA
	-55	2	2	101.2	97.8	99.5	NA	- .5	- 6.0
	+125	2	2	109.5	80.6	103.1	NA	+ 4.1	+ 4.5

NOTES:

a) Avg "X" is the average (absolute) for total samples allowed. Avg "Y" is the average (absolute) for two samples used in temperature tests. Δ's for -55° and +125° were calculated by comparing Avg "Y" at 25°C with Avg "X" at -55° and +125.

b) * indicate out of spec condition.

c) Signs in Δ columns indicate direction from 25°C.

d) Although not called out, temperature data taken on units.

5.3.7 Power Supply Rejection Ratio (-)

MIL-M-38510/101 Ref: Table III, test 5
Specification: 86db min at 25°C
Results:

Vendor	T_A °C	Samp Tested	Samp Allowed	Max	Min	Avg "X"	Avg "Y"	Avg Δ from 25°C	Max Δ from 25°C
A	25	7	7	92.15	81.5*	89.1	89.7	NA	NA
	-55	2	2	100.4	92.1	96	NA	+ 6.3	+11.3
	+125	2	2	90.4	89.5	89.9	NA	+ .2	+ .81
B	25	7	7	101	81.24*	87.4	84.5	NA	NA
	-55	2	2	95.9	76	85.5	NA	+ 1	+ 7.2
	+125	2	2	87.0	80	83	NA	- 1.5	- 1.5
C	25	7	7	92	62.7*	82.2*	84.8*	NA	NA
	-55	2	1	--	--	69.6	NA	-15.2	--
	+125	2	1	--	--	72.1	NA	-12.7	--
D	25	7	7	100.7	80.6	93.7	99.0	NA	NA
	-55	2	2	99.4	96.3	97.8	NA	- 1.2	- 1.7
	+125	2	2	105	99	102	NA	+ 3	+ 7.0

NOTES:

a) Avg "X" is the average (absolute) for total samples allowed. Avg "Y" is the average (absolute) for two samples used in temperature tests. Δ's for -55° and +125° were calculated by comparing Avg "Y" at 25°C with Avg "X" at -55° and +125°.

b) * indicate out of spec condition.

c) Signs in Δ columns indicate direction from 25°C.

d) Although not called out, temperature data taken on units.

5.3.8 Input Voltage Common Mode Rejection Ratio

MIL-M-38510/101 Ref: Table III, test 6
Specification: 80db min at 25°; -55° and +125°
Results:

Vendor	T_A °C	Samp Tested	Samp Allowed	Max	Min	Avg "X"	Avg "Y"	Avg Δ from 25°C	Max Δ from 25°C
A	25	7	7	112.6	90.23	96.5	94.2	NA	NA
	-55	2	2	95.6	95.2	95.4	NA	+ 1.2	- 1.4
	+125	2	2	94.97	93.1	94.0	NA	- .2	- .4
B	25	7	7	104.4	81.51	90.17	92.0	NA	NA
	-55	2	2	98.1	91.0	94.5	NA	+ 2.5	+16.7
	+125	2	2	89.3	79.6	84.0	NA	- 8	- 8.5
C	25	7	7	94.6	63.9*	82.2	78*	NA	NA
	-55	2	1	--	--	75.0*	NA	- 3	--
	+125	2	1	--	--	80.0	NA	+ 2	--
D	25	7	7	59.5*	58.8*	58.95*	59*	NA	NA
	-55	2	2	99.4	58.9*	78*	NA	+19	+40
	+125	2	2	58.9*	58.5*	58.7*	NA	- .3	- .4

NOTES:

a) Avg "X" is the average (absolute) for total samples allowed. Avg "Y" is the average (absolute) for two samples used in temperature tests. Δ's for -55° and +125° were calculated by comparing Avg "Y" at 25°C with Avg "X" at -55° and +125°.

b) * indicate out of spec condition.

c) Signs in Δ columns indicate direction from 25°C.

5.3.9 Adjustment for Input Offset Voltage b)

MIL-M-38510/101 Ref: Table III, test 7
Specification: 10mv min at 25°C; -55° and +125°
Results:

Vendor	T_A °C	Samp Tested	Samp Allowed	Max	Min	Avg "X"	Avg "Y"	Avg Δ from 25°C	Max Δ from 25°C
A	25	7	7	18.6	16.8	17.6	17.19	NA	NA
	-55	2	2	12.85	11.73	12.29	NA	-4.9	-5.8
	+125	2	2	19.33	18.8	19.01	NA	+1.82	+2.5
B	25	7	7	16.36	12.5	15.12	14.7	NA	NA
	-55	2	2	10.1	7.4*	8.7*	NA	-6.0	-6.8
	+125	2	2	21.2	17.0	19.1	NA	+4.1	+5.8
C	25	7	7	27.1	15.9	18.87	16.8	NA	NA
	-55	2	1	--	--	11.1	NA	-5.7	--
	+125	2	1	--	--	15.0	NA	-1.8	-
D	25	7	7	19.3	16.2	17.4	16.7	NA	NA
	-55	2	2	15.6	14.7	15.15	NA	-1.55	-2.0
	+125	2	2	16.3	14.3	15.3	NA	-1.4	-1.9

NOTES:

a) Avg "X" is the average (absolute) for total samples allowed. Avg "Y" is the average (absolute) for two samples used in temperature tests. Δ's for -55° and +125° were calculated by comparing Avg "Y" at 25°C with Avg "X" at -55° and +125°.

b) * indicate out of spec condition.

c) Signs in Δ columns indicate direction from 25°C.

5.3.10 Adjustment for Input Offset Voltage (-)

MIL-M-38510/101 Ref: Table III, test 8
Specification: 10mv min at 25°C; -55° and +125°
Results:

Vendor	T_A °C	Samp Tested	Samp Allowed	Max	Min	Avg "X"	Avg "Y"	Avg Δ from 25°C	Max Δ from 25°C
A	25	7	7	17.39	16.18	16.21	16.7	NA	NA
	-55	2	2	12.54	12.06	12.30	NA	-4.1	-4.6
	+125	2	2	17.2	16.9	17.05	NA	+ .35	+ .69
B	25	7	7	15.78	12.29	14.61	13.2	NA	NA
	-55	2	2	10.3	17.4*	8.84*	NA	-4.4	-4.9
	+125	2	2	17.1	14.5	15.8	NA	+2.6	+4.6
C	25	7	7	20.5	15.0	16.49	16.4	NA	NA
	-55	2	1	--	--	12.3	NA	-4.1	--
	+125	2	1	--	--	21.8	NA	+5.4	--
D	25	7	7	17.7	15.8	16.38	16.9	NA	NA
	-55	2	2	12.75	12.27	12.5	NA	-4.4	-4.65
	+125	2	2	17.6	15.8	16.7	NA	- .2	- .6

NOTES:

a) Avg "X" is the average (absolute) for total samples allowed. Avg "Y" is the average (absolute) for two samples used in temperature tests. Δ's for -55° and +125° were calculated by comparing Avg "Y" at 25°C with Avg "X" at -55° and +125°.

b) * indicate out of spec condition.

c) Signs in Δ columns indicate direction from 25°C.

5.3.11 Output Short Circuit Current (+)

MIL-M-38510/101 Ref: Table III, tests 9, 19, and 29
Specification: 15-30ma at 25°C; 15 -35ma at -55° and +125°
Results:

Vendor	T_A °C	Samp Tested	Samp Allowed	Max	Min	Avg "X"	Avg "Y"	Avg Δ from 25°C	Max Δ from 25°C
A	25	7	7	20	17	18.4	17.8	NA	NA
	-55	2	2	30	24	27	NA	+9.2	+11.8
	+125	2	2	13.2*	12.5*	12.8*	NA	-5.0	- 5.7
B	25	7	7	20.5	14.5*	17.02	18.2	NA	NA
	-55	2	2	22	14	18	NA	- .2	- 2.0
	+125	2	2	11*	9*	10*	NA	-8.2	- 8.5
C	25	See note (d) below							
	-55								
	+125								
D	25	See note (d) below							
	-55								
	+125								

NOTES:

a) Avg "X" is the average (absolute) for total samples allowed. Avg "Y" is the average (absolute) for two samples used in temperature tests. Δ's for -55° and +125° were calculated by comparing Avg "Y" at 25°C with Avg "X" at -55° and +125°.

b) * indicate out of spec conditions.

c) Signs in Δ column indicate direction from 25°C.

d) Vendor D's units blew when performing this test at 25°C (two units). Vendor C's units blew at +125° (two units).

5.3.12 Output Short Circuit Current (-)

MIL-M-38510/101 Ref: Table III, tests 10, 20, and 30
Specification: 15-30ma at 25°C; 15-35ma at -55° and +125°
Results:

Vendor	T_A °C	Samp Tested	Samp Allowed	Max	Min	Avg "X"	Avg "Y"	Avg Δ from 25°C	Max Δ from 25°C
A	25	7	7	18	16	16.6	16.3	NA	NA
	-55	2	2	30	27	28.5	NA	+12.2	+14.0
	+125	2	2	14*	10.5*	12.2*	NA	- 4.1	- 4.5
B	25	7	7	20.5	14.0	16.91	17.2	NA	NA
	-55	2	2	22.5	16.3	19.4	NA	+ 2.2	+ 5.2
	+125	2	2	12*	7.0*	10*	NA	- 7.2	- 9.1
C	25	See note (d) below							
	-55								
	+125								
D	25	See note (d) below							
	-55								
	+125								

NOTES:

a) Avg "X" is the average (absolute) for total samples allowed. Avg "Y" is the average (absolute) for two samples used in temperature tests. Δ's for -55° and +125° were calculated by comparing Avg "Y" at 25°C with Avg "X" at -55° and +125°.

b) * indicate out of spec condition.

c) Signs in Δ columns indicate direction from 25°C.

d) Vendor D's units blew when performing this test at 25°C (two units). Vendor C's units blew at +125°C (two units).

5.3.13 d.c. Power Dissipation

MIL-M-38510/101 Ref: Table III, tests 11, 21, and 31
Specification: 150 mw max at 25°C, 165 mw max at -55°C
135mw max at +125°C

Results:

Vendor	T_A °C	Samp Tested	Samp Allowed	Max	Min	Avg "X"	Avg "Y"	Avg Δ from 25°C	Max Δ from 25°C
A	25	7	7	112	88	100	110	NA	NA
	-55	2	2	120	112	116	NA	+ 6	+ 8
	+125	2	2	88	80	84	NA	-26	-28
B	25	7	7	116	88	102.1	111	NA	NA
	-55	2	2	136	132	134	NA	+23	+27
	+125	2	2	90	88	89	NA	-29	-29
C	25	7	7	120	69	83.6	70	NA	NA
	-55	2	1	--	--	74.0	NA	+ 4	-
	+125	2	1	--	--	64.4	NA	- 5.6	--
D	25	7	7	96	80	87.2	91.5	NA	NA
	-55	2	2	104	99	101.5	NA	+10	+12
	+125	2	2	80	68	74	NA	-17.5	-18

NOTES:

a) Avg "X" is the average (absolute) for total samples allowed. Avg "Y" is the average (absolute) for two samples used in temperature tests. Δ's for -55° and +125° were calculated by comparing Avg "Y" at 25°C with Avg "X" at -55° and +125°.

b) * indicate out of spec condition.

c) Signs in Δ columns indicate direction from 25°C.

5.3.14 Single Ended Input Impedance (÷)

MIL-M-38510/101 Ref: Table III, tests 12, 22, and 32
Specification: 1 Meg ohm min at 25°, .5 Meg ohm min at -55° and +125°
Results:

Vendor	T_A °C	Samp Tested	Samp Allowed	Max	Min	Avg "X"	Avg "Y"	Avg Δ from 25°C	Max Δ from 25°C
A	25	7	6	360	39	192	180	NA	NA
	-55	2	2	4	1.09	2.5	NA	-1 [illegible]	-329
	+125	2	2	91	9.0	50	NA	-130	-341
B	25	7	6	19.3	.313*	8.45	7.8	NA	NA
	-55	2	2	10.0	10.0	10.0	NA	+ 2.2	+ 9.3
	+125	2	2	100	86.3	93	NA	+ 85.2	+ 96
C	25	7	6	82.7	1.26	32.1	1.26	NA	NA
	-55	2	1	--	--	1.96	NA	+ .7	--
	+125	2	1	--	--	20.3	NA	+ 19.04	--
D	25	7	6	100	[illegible]	42.9	77.6	NA	[illegible]
	-55	2	2	8.1	5.2	6.6	NA	- 71	[illegible]
	+125	2	2	20.1	6.5	13.7	NA	- 63.9	- 94

NOTES:

a) Avg "X" is the average (absolute) for total samples allowed. Avg "Y" is the average (absolute) for two samples used in temperature tests. Δ's for -55° and +125° were calculated by comparing Avg "Y" at 25°C with Avg "X" at -55° and +125°.

b) * indicate out of spec condition.

c) Signs in Δ columns indicate direction from 25°C.

5.3.15 **Single Input Impedance (-)**

MIL-M-38510/101 Ref: Table III, tests 13, 23, and 33
Specification: 1 Meg ohm min at 25°C, .5 Meg ohm min at -55° and +125°
Results:

Vendor	T_A °C	Samp Tested	Samp Allowed	Max	Min	Avg "X"	Avg "Y"	Avg Δ from 25°C	Max Δ from 25°C
A	25	7	7	850	2.7	233	152	NA	NA
	-55	2	2	110	4	57	NA	- 95	-305
	+125	2	2	59	55	57	NA	- 95	-301
B	25	7	7	15.5	1.2	8.5	7.5	NA	NA
	-55	2	2	10	10	10	NA	+ 2.5	+ 5.1
	+125	2	2	70	63.3	67	NA	+ 59.5	+ 60.7
C	25	7	6	109	3.4	46.8	3.4	NA	NA
	-55	2	1	--	--	16.6	NA	+ 13.2	--
	+125	2	1	--	--	13.7	NA	+ 10.3	--
D	25	7	6	100	15	60.2	26.3	NA	NA
	-55	2	2	15.7	10.9	13.3	NA	- 13	--
	+125	2	2	300	13.8	157	NA	+130.7	+247

NOTES:

a) Avg "X" is the average (absolute) for total samples allowed. Avg "Y" is the average (absolute) for two samples used in temperature tests. Δ's for -55° and +125° were calculated by comparing Avg "Y" at 25°C with Avg "Y" at -55° and +125°.

b) * indicate out of spec condition.

c) Signs in Δ columns indicate direction from 25°C.

5.3.16 Output Voltage Swing (R_L = 10K)

MIL-M-38510/101 Ref: Table III, tests 34, 38, and 42
Specification: 32v P to P at 25°C; -55° and +125°
Results:

Vendor	T_A °C	Samp Tested	Samp Allowed	Max	Min	Avg "X"	Avg "Y"	Avg Δ from 25°C	Max Δ from 25°C
A	25	7	7	37.01	36.36	36.73	36.71	NA	NA
	-55	2	2	36.24	36.19	36.21	NA	-.5	-.52
	+125	2	2	37.63	37.63	37.65	NA	-.06	-.08
B	25	7	7	37.06	36.38	36.84	36.80	NA	NA
	-55	2	2	36.46	36.42	36.44	NA	-.46	-.52
	+125	2	2	37.14	36.95	37.04	NA	+.24	+.60
C	25	7	7	37.8	37.0	37.44	37.2	NA	NA
	-55	2	1	--		37.0	NA	-.2	--
	+125	2	1	--	--	36.3	NA	-.9	--
D	25	7	7	38.0	37.2	37.55	37.50	NA	NA
	-55	2	2	37.5	37.0	37.25	NA	-.25	.50
	+125	2	2	38.3	38.1	38.2	NA	+.7	+.8

NOTES:

a) Avg "X" is the average (absolute) for total samples allowed. Avg "Y" is the average (absolute) for two samples used in temperature tests. Δ's for -55° and +125° were calculated by comparing Avg "Y" at 25°C with Avg "X" at -55° and +125°.

b) * indicate out of spec condition.

c) Signs in Δ columns indicate direction from 25°C.

5.3.17 Output Voltage Swing (R_L = 2K)

MIL-M-38510/101 Ref: Table III, tests 35, 39, and 43
Specification: 30v P to P at 25°C; -55° and +125°
Results:

Vendor	T_A °C	Samp Tested	Samp Allowed	Max	Min	Avg "X"	Avg "Y"	Avg Δ from 25°C	Max Δ from 25°C
A	25	7	7	36.37	35.77	36.12	36.16	NA	NA
	-55	2	2	35.78	35.71	35.74	NA	-.42	-.48
	+125	2	2	36.6	36.32	36.46	NA	+.30	+.5
B	25	7	7	36.41	35.93	36.26	36.25	NA	NA
	-55	2	2	36.93	35.88	35.9	NA	-.35	-.37
	+125	2	2	36.6	35.71	36.15	NA	-.10	-1.5
C	25	7	7	36.8	36.3	36.52	36.3	NA	NA
	-55	2	1	--	--	36.3	NA	0	--
	+125	2	1	--	--	36.2	NA	-.1	--
D	25	7	7	36.3	36.2	36.6	36.55	NA	NA
	-55	2	2	36.5	36.1	36.3	NA	-.25	-.6
	+125	2	2	37.5	37.4	37.45	NA	+.9	+.9

NOTES:

a) Avg "X" is the average (absolute) for total samples allowed. Avg "Y" is the average (absolute) for two samples used in temperature tests. Δ's for -55° and +125° were calculated by comparing of Avg "Y" at 25°C with Avg "X" at -55° and +125°.

b) * indicate out of spec condition.

c) Signs in Δ columns indicate direction from 25°C.

7.3.8 Open Loop Voltage Gain (V_{IN} = 15v)

MIL-M-38510/101 Ref: Table III, tests 36, 40, and 44
Specification: 31.6v/mv min (90db) at 25°C, -55°, and +125°
Results:

Vendor	T_A °C	Samp Tested	Samp Allowed	Max	Min	Avg "X"	Avg "Y"	Avg Δ from 25°C	Max Δ from 25°C
A	25	7	7	242	81	113	95	NA	NA
	-55	2	2	202	119	167	NA	+ 72	+102
	+125	2	2	123	83	105	NA	+ 10	+ 30
B	25	7	7	365	62	127	108	NA	NA
	-55	2	2	375	75	150	NA	+ 42	+300
	+125	2	2	100	60	91	NA	- 17	- 40
C	25	7	6	57.7	2.42*	19.32*	15.6*	NA	NA
	-55	2	1	--	--	4.5*	NA	- 11.1	--
	-125	2	1	--	--	4.5*	NA	- 11.1	--
D	25	7	7	258	8.5*	145.9	175	NA	NA
	-55	2	2	75	51	63	NA	-112	165
	-125	2	2	166	68.2	117	NA	- 28	-135

NOTES:

a) Avg "X" is the average (absolute) for total samples allowed. Avg "Y" is the average (absolute) for two samples used in temperature tests. Δ's for -55° and +125° were calculated by comparing Avg "Y" at 25°C with Avg "X" at -55° and +125°.

b) * indicate out of spec condition.

c) Signs in Δ columns indicate direction from 25°C.

d) The gain tests were taken on both inverting and non-inverting inputs and then averaged.

5.3.19 Open Loop Voltage Gain (V_{IN} = 2v)

MIL-M-38510/101 Ref: Table III, tests 37, 41, and 45
Specification: 10v/mv min (80db) at 25°C, -55° and +125°
Results:

Vendor	T_A °C	Samp Tested	Samp Allowed	Max	Min	Avg "X"	Avg "Y"	Avg Δ from 25°C	Max Δ from 25°C
A	25	7	6	400	95	183	255	NA	NA
	-55	2	2	176	29	105	NA	-150	-175
	+125	2	2	119	28	75	NA	-180	-250
B	25	7	7	500	18	125.4	100	NA	NA
	-55	2	2	25	8.3	18.0	NA	- 82	-125
	+125	2	2	200	30	122	NA	+ 22	+150
C	25	7	6	200	20	57.4	133	NA	NA
		2	1	--	--	25	NA	-107	--
		2	1	--	--	41	NA	- 92	--
D	25	7	6	250	26	110	55	NA	NA
	-55	2	2	100	16	58	NA	+ 3	+ 44
	+125	2	2	200	19	109	NA	+ 54	+219

NOTES:

a) Avg "X" is the average (absolute) for total samples allowed. Avg "Y" is the average (absolute) for two samples used in temperature tests. Δ's for -55° and +125° were calculated by comparing Avg "Y" at 25°C with Avg "X" at -55° and +125°.

b) * indicate out of spec condition.

c) Signs in Δ columns indicate direction from 25°C.

d) The gain tests were taken on both inverting and non-inverting input, and then averaged.

5.3.20 Slew Rate

MIL-M-38510/101 Ref: Figure 13
Specification: 0.4v/usec min at V_{IN} = ±15v @ 25°C
Results:

Vendor	Samples Tested	Samples Allowed	Max	Min	Avg
A	-	-	.515	.445	.486
B	4	4	.57	.50	.542
C	4	4	1.82	1.22	1.43
D	4	4	.80	.635	.716

5.4 Analysis of Test Results

No vendor met all the test specifications of MIL-M-38510/101. Vendor A's devices came closest; his failed only three tests.

A complete rundown, vendor by vendor is shown in the following table.

Vendor	Total No. Tests	Tests Passed			Tests Failed		
		Easily	Normal	Margin	Badly	Normal	Marginal
A	51	27	18	3	0	0	3
B	51	21	23	3	1	2	1
C	51	19	11	3	11	4	3
D	51	29	12	1	6	2	1

Figure 5.7. Vendor Comparison Chart

a. Total tests include all temperatures, i.e. offset would include three tests 25°, -55°, and +125°.

b. An easily passed test would be one in which less than 50 percent of the spec used.

c. A marginally passed test would be one in which more than 90 percent of the spec is used.

d. A badly failed or catastrophic test would be one in which reading was 50 percent or greater over the limits.

e. A marginally failed test would be one in which reading was 10 percent or less over the limit.

To establish some vehicle for comparison, the following method was devised. An adder or subtractor was assigned to each of the categories of Figure 5.7. The method can be described graphically as follows:

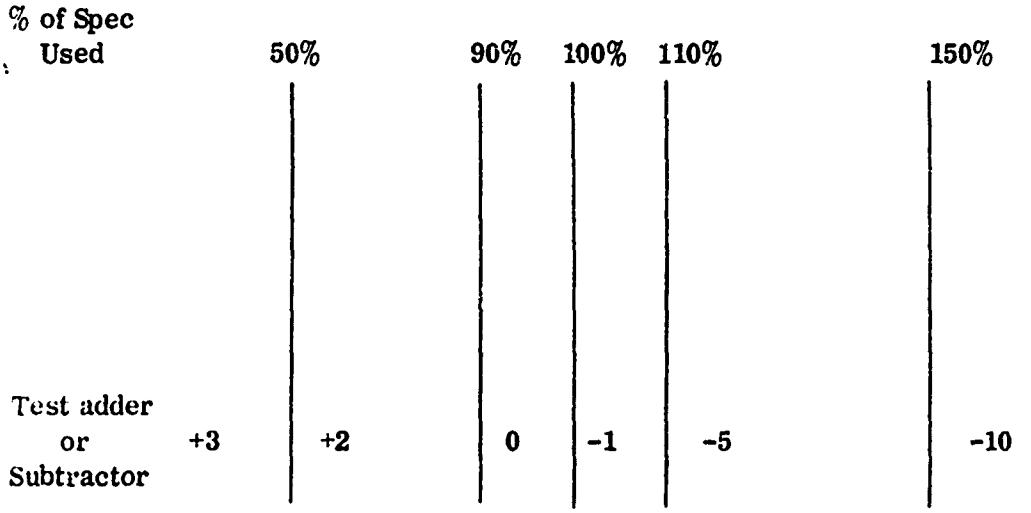


Figure 5.8. Vendor Comparison Clarification

The above method of point establishment is arbitrary and can be adjusted depending upon the area of concern for the user. Also, if -55°C was an important operating temperature to a particular user, and +125° and 25° were not, then the weight of the -55°C test could be more than the other tests.

The results of applying the format of Figure 5.8 to the test results of Figure 5.7 is as follows:

A	114
B	89
C	-54
D	40

NOTE: A perfect score is all parameters (using less than 50 percent of the spec) would be 303.

5.5 Noise Investigation

Integrated circuit operational amplifiers such as the 709 and 741 exhibit two distinct kinds of noise. White or normal noise can be readily measured with a noise analyzer and broken down into a voltage and current component. This noise occurs over a wide frequency range.

The other type of noise, commonly called "popcorn", is characterized by erratic bursts or shifts in the d.c. output level. It occurs at a low frequency and the bursts last for 100 μseconds or more. The shifts can be either positive, negative or both for a particular device. Popcorn noise gets worst at high input impedances and at low temperatures.

When popcorn noise was first noticed, it was feared by many users that it indicated either a cracked or contaminated chip and would adversely affect reliability. GEOS on the Poseidon Program performed many life tests on 709's being careful to separate units exhibiting popcorn noise from those that had only white noise. No difference in either failure rate or drift of parameters were noted. These tests have since been repeated by the Naval Ammunition Depot, Crane, Indiana with the same results. It is now commonly believed that popcorn noise is caused by flaws in either the crystal or oxide passivation near the surface occurring in the area of the input transistors, an NAD Crane report is available on the subject.

Noise must be specified and controlled because it puts a definite limit on the usefulness of these amplifiers in high gain or high input impedance circuits.

On the Poseidon Program, noise for 709's was specified with a 10 K Ω source impedance. It was found that white noise was always below 15 μ v peak referred to the input and popcorn noise almost always above 50 μ v peak and sometimes going to several hundred μ v's. Consequently, the specification was set at 20 μ v peak and over 10,000 devices have been purchased to this requirement. This parameter is 100 percent tested for. Many vendors had no yield to this requirement but some only lost 10 percent of their product because of it. The price per part increased approximately 20 percent. The requirement has become less of a handicap now than it was a few years ago since less than 1 percent of the most recent devices have exhibited popcorn noise bursts between 15 and 20 μ v.

The data for the 741 devices, Figure 5.9, shows that white noise is similar to 709's in that it is always below 15 μ v's. Popcorn noise at a source impedance of 100 K Ω appears in almost all devices and ranges from 12 μ v to 44 μ v peak. This is lower than 709's because the 30 pf internal capacitor limits the bandwidth below that of a 709. Two vendors have devices which would meet 25 μ v peak with a 100 percent yield for the devices tested. The other two vendors would have almost no yield to this requirement. Other not tested vendors guarantee no popcorn above 25 μ v peak.

It is our recommendation that a noise requirement of 25 μ v peak be added to M38510/101. That this parameter be tested for using a shielded circuit with a closed loop gain of 1000 and a memory voltmeter or storage oscilloscope. Because of the erratic nature of the noise and its low frequency, it is not known whether or not this parameter could be measured on automatic test equipment. The time required to perform the test (i.e. 30 seconds) would make automatic test equipment impractical for this parameter.

Noise Data: 741 Operational Amplifier

Data is expressed in μ v peak.

Vendor A

Unit No.	@ 10 KΩ	@ 100 KΩ
20	15 popcorn	20 popcorn
21	15 popcorn	18 popcorn
23	15 popcorn	20 popcorn
24	16 popcorn	17 popcorn
25	15 popcorn	16 popcorn
26	15 popcorn	16 popcorn
Vendor B		
27	15 popcorn	40 popcorn
28	6 white	16 white
29	15 popcorn	40 popcorn
30	10 popcorn	34 popcorn
32	24 popcorn	36 popcorn
Vendor C		
40	24 popcorn	30 popcorn
41	35 popcorn	40 popcorn
43	36 popcorn	44 popcorn
45	15 popcorn	40 popcorn

Figure 5.9. Noise Data for 741 (Continued)

Vendor D

Unit No.	@ 10 K Ω	@ 100 K Ω
15	20 popcorn	25 popcorn
16	17 popcorn	20 popcorn
18	10 white	10 white
19	18 popcorn	20 popcorn
1		11 white
2		10 white
3		18 popcorn
4		12 popcorn
5		13 popcorn
6		22 popcorn
7		13 popcorn
8		10 white
9		21 popcorn
10		18 popcorn

Figure 5.9. Noise Data for 741 (Concluded)

Section VI

ECL REVIEW

6.0 Introduction

Information presented in this report was obtained from a variety of sources, vendor catalogs, application notes, discussion with manufacturers, and visit to a military user of these devices.

Emitter-coupled logic is a non-saturating form of logic circuit which is generally characterized by extremely fast rise and fall times of four nsec or less and a d... between output high and low levels of less than one volt. In contrast to sat... logic such as DTL and T^2L, ECL is extremely susceptible to noise and p... stem is strongly dependent upon interconnection methods.

6.1 Thermal Considerations

Non-saturating logic, output levels and input thresholds are dependent on t... perature. This becomes a serious problem for example when devices running at ... temperature interface with devices at another temperature. In these cases the nois... margins can be greatly reduced and render the circuit inoperable. This problem is compounded by the fact that ECL circuits dissipate considerably more power per gate than non-saturating types. Devices with high dissipation are packaged in a flat pack with a thermal stud. If the thermal studs are all connected to a common heat sink, the junctions can be maintained within reasonable limits to each other.

6.2 Interconnections

Because of the high speed and susceptibility to noise, interconnections are ... made through terminated transmission lines. One advantage of ECL circuits ... ated logic is the capability of driving matched - impedance transmission ... of transmission lines retains signal integrity over long distances. ... circuit boards, transmission lines are formed in two ways - either microstrip or stripline techniques. The microstrip is formed by a constant width conductor on ... of a circuit board, with a ground plane on the other side. Stripline is used ... multilayer circuit boards; the stripline consists of a constant width conductor ... between two ground planes. Interconnection between boards are made by the complementary outputs of the ECL circuit driving a twisted pair line with a line receiver ... end.

6.3 Clock Distribution

Clock Distribution for any high-speed logic is often a major system problem. Either coaxial cable or twisted pair line can be used to distribute clock signals

throughout an ECL system. Clock line lengths should be controlled and matched when timing is critical. Once the clocking signals arrive on card, a tree distribution should be used for large fan outs at high frequency.

6.4 New Types of ECL

In order to alleviate some of the aforementioned problems, new families of ECL have recently been introduced. These new families offer some of the following advantages. They have temperature compensation; the logic levels remain constant across the temperature range which maintains maximum system noise immunity and eliminates saturation problems. They have internal pull down resistors which permits point-to-point wiring of up to eight inches on single-sided boards. The resistors also eliminate oscillation problems and allow unused inputs to be left open. On these newer devices, power dissipation remains relatively constant over the frequency range. On some of the most recent devices, supply voltage compensation allows variation in the supply voltage without change of the output or threshold levels.

6.5 Future of ECL

Even though some of the higher speed saturated logic types such as Schottky clamped T^2L has reached into the ECL speed range, at the very highest speeds of one nsec rise and fall times, ECL remains the dominant type and probably will remain so for the near future. With the advent of the new families which are multi-sourced as well as offering performance advantages, the use of ECL should grow rapidly in the next few years.

Section VII

VENDOR ANALYSIS OF LM 106 DIFFERENTIAL COMPARATOR

7.0 Introduction

Twenty LM 106 differential comparators were purchased "off the shelf" equally from two different vendors. These vendors were not informed of the proposed use of their devices nor were samples selected. All units were in standard eight pin metal can. The date codes for each vendors part was as follows: A(7130), D(7026). All units were tested in accordance with the test conditions, procedures, and limits of proposed MIL-M-38510/10303 at 25°C, -55°C, and +125°C.

Paragraphs 7.1 and 7.2 will include the test circuit and test equipment used and the conditions under which each test was performed; in addition, these paragraphs will outline some of the troublesome areas in testing and in calculating test results.

Paragraph 7.3 will include, parameter by parameter, results of testing the various samples. The vendors are listed in alphabetical order for each condition and not in order of results. The test data is presented as follows:

a) Vendor, b) Ambient Temperature, c) Number of samples tested, d) max. reading, e) min. reading and f) average of readings.

Section 7.4 summarizes the results obtained on all tests.

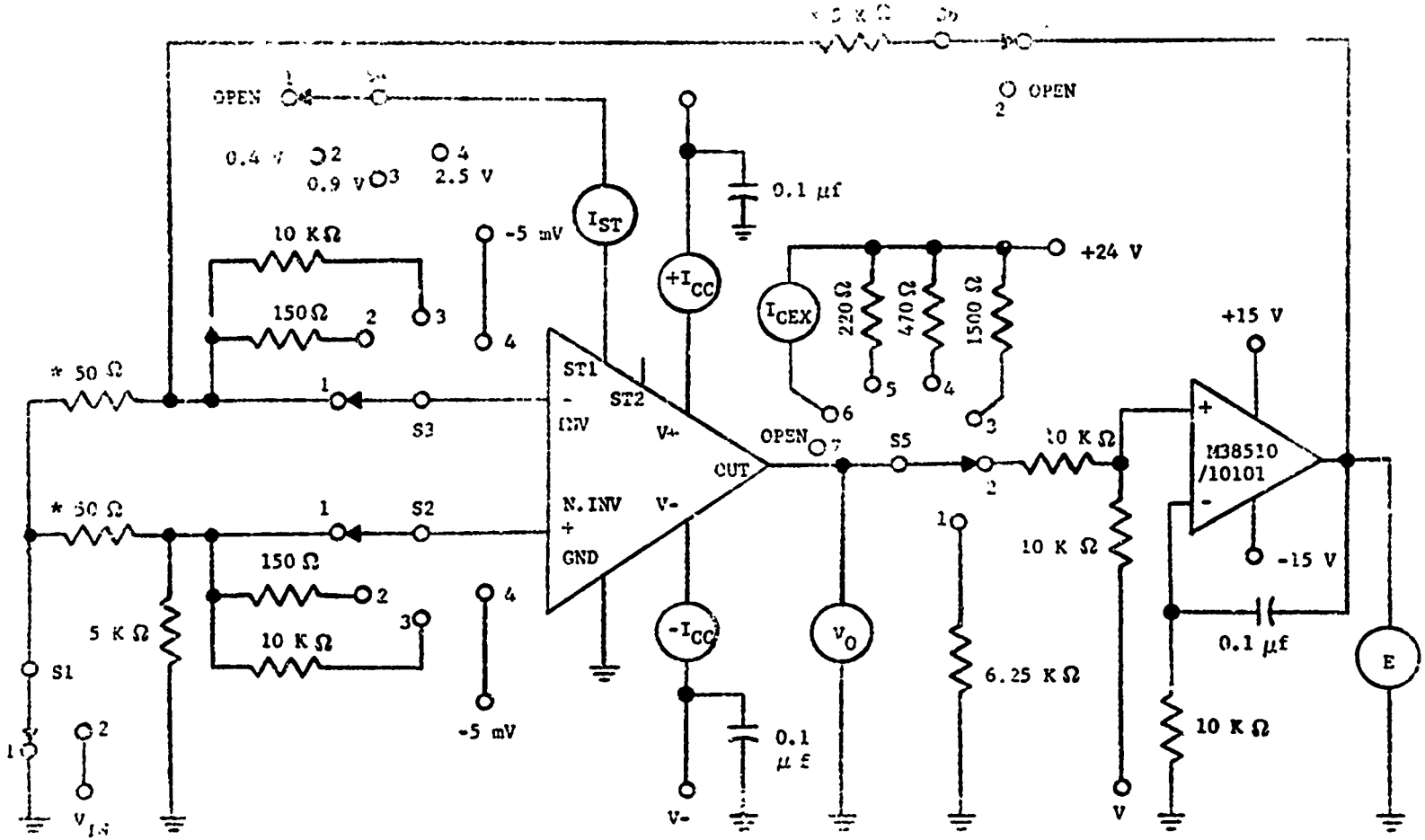
7.1 Test Setup

The test setup of Figure 7.1 was used in conjunction with the switch positions and voltages shown in Figure 7.1 for all the d.c. tests.

The test setup of Figure 7.2 was used for the response time.

a) d.c. supplies - Harrison, various
b) d.c. Voltmeter - Dana 5400
c) d.c. Voltmeter - Fluke 887A
d) d.c. Ammeter - Hewlett Packard 425A
e) Temperature Chamber - Wyle
f) Oscilloscope - Tektronix 585

The oven temperature was allowed to stabilize for one hour with power applied to the unit before readings were taken. Ambient temperatures were held to within ±3°C.

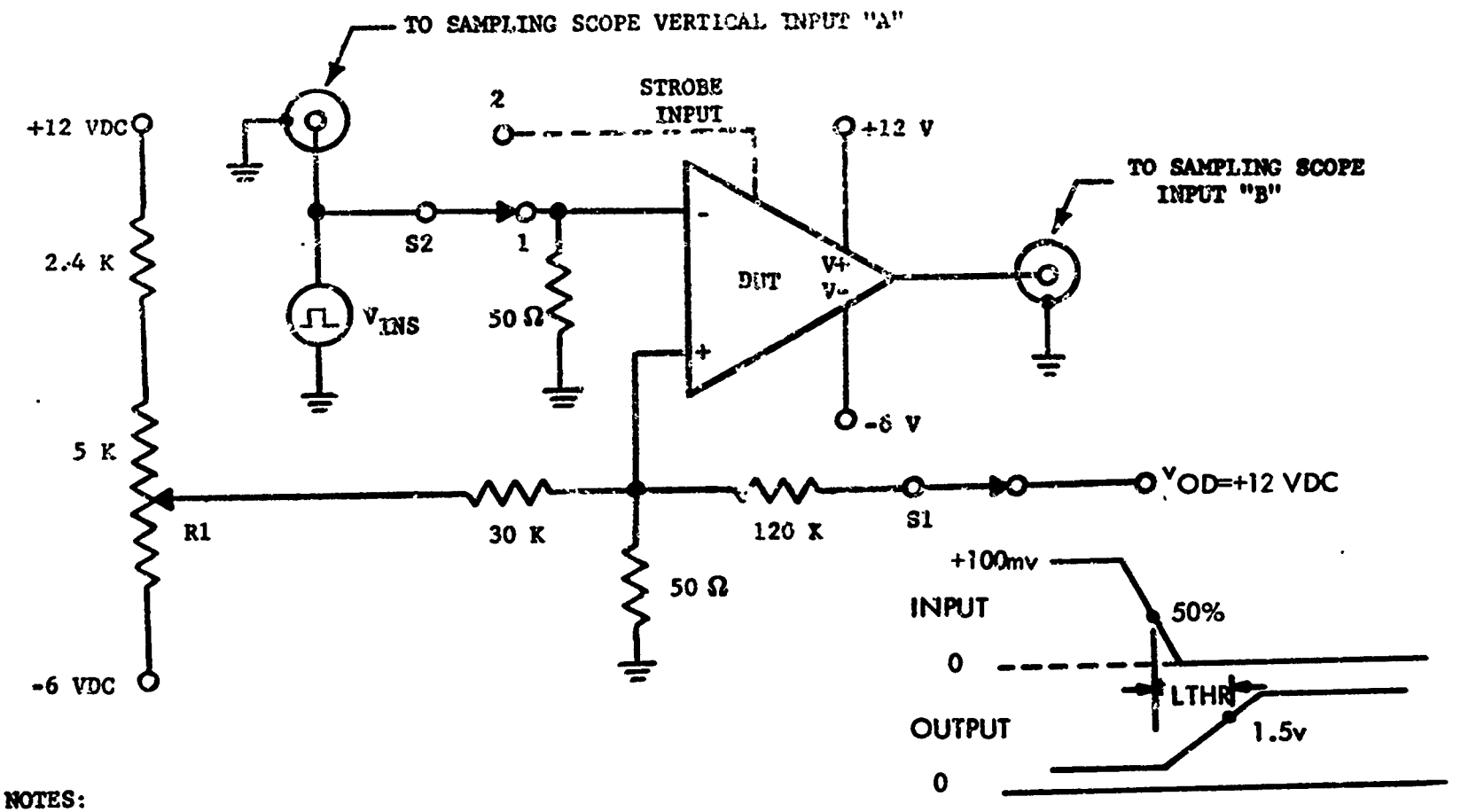


* These two 50 Ω resistors matched to 0.01%. All other resistors are 1%, capacitor tolerance is 10%. Precautions must be taken to prevent damage to the device during insertion into socket and change of switch positions

Figure 1. Test Circuit for Static and Dynamic Tests

PARAMETER	APPLY (IN VOLTS) $+V_{CC}$	$-V_{CC}$	V_{IN}	V	SWITCH POSITION S1	S2	S3	S4	S5	S6	MEASURE VALUE	UNITS	MEASURED PARAMETERS EQUATION	UNITS
V_{IO}(50Ω)	12	-6	--	-1.5	1	1	3	1	2	1	E_1	mV	$V_{IO} = \frac{E1}{100}$	mV
V_{IO}(200Ω)	12	-6	--	-1.5	1	2	2	1	2	1	E_2	mV	$V_{IO} = \frac{E2}{100}$	mV
I_{IO}	12	-6	--	-1.5	1	3	3	1	2	1	E_3	mV	$I_{IO} = \frac{E_1 - E_3}{1000}$	μA
$+I_{IB}$	12	-6	--	-1.5	1	3	1	1	2	1	E_4	mV	$+I_{IB} = \frac{E_1 - E_4}{1000}$	μA
$-I_{IB}$	12	-6	--	-1.5	1	1	3	1	2	1	E_5	mV	$-I_{IB} = \frac{E_5 - E_1}{1000}$	μA
I_{IB}	CALCULATION												$I_{IB} = \frac{E_5 - E_4}{2000}$	μA
CMRR	12	-7	+5	-1.5	2	2	2	1	2	1	E_6	mV	$CMRR = 20 \log \frac{10 \times 10^5}{E_6 - E_7}$	dB
	12	-7	-5	-1.5	2	2	2	1	2	1	E_7	mV		
$+I_{CC}$	12	-6	--	--	1	4	1	1	2	2	$+I_{CC}$	mA		
$-I_{CC}$	12	-6	--	--	1	4	1	1	2	2	$-I_{CC}$	mA		
V_{OH}	12	-6	--	--	1	1	4	1	1	2	V_O	V	$V_{OH} = V_O$	V
V_{OL}(100mA)	12	-6	--	--	1	4	1	1	5	2	V_O	V	$V_{OL} = V_O$	V
V_{OL}(50mA)	12	-6	--	--	1	4	1	1	4	2	V_O	V	$V_{OL} = V_O$	V
V_{OL}(16mA)	12	-6	--	--	1	4	1	1	3	2	V_O	V	$V_{OL} = V_O$	V
V_O STROBE LOW	12	-6	--	--	1	4	1	3	7	2	V_O	V		V
V_O STROBE HIGH	12	-6	--	--	1	4	1	4	3	2	V_O	V		V
I_{STROBE}	12	-6	--	--	1	4	1	2	7	2	V_O	V	$I_{ST} = I_{STROBE}$	mA
I_{CEX}	12	-6	--	--	1	1	4	1	6	1	I_{CEX}	μA		

Figure 7.1. Test Circuit for Static and Dynamic Tests (concluded)



NOTES:

1. V_{INS} = 100 ns pulse width, 100 kHz repetition rate, t_r and $t_f \leq 5$ ns.
2. Set up procedure : with S1 open and V_{INS} = 0 adjust R1 for V_{OUT} = 1.5 V. Apply V_{OD} and close S1. Apply V_{INS}.

Figure 7.2. Response Time Test Circuit and Wave Forms

7.2 Analysis of Test Circuit

7.2.1 Measurement Accuracy Determination

All measurements except Common Mode Rejection Ratio (CMRR) require simple formula conversions to yield the calculated parameter. For two-place accuracy on the parameter, three places are required on the measurement.

Since $CMRR = 20 \log \frac{10 \times 10^5}{E_6 - E_7}$,

E_6 and E_7 must be measured to four place accuracy to insure two place accuracy to CMRR.

7.2.2 Self-heating

The specification for V_{OL} at 100 ma is 1.5V maximum and at 50 ma is 1.0V maximum. Both of these readings must be taken quickly since the added power of 150 mw and 50 mw respectively heats the unit enough to alter the reading.

7.2.3 Strobe Test

Test Figure 7.1 tests the strobe on a go-no go basis. It insures that at 0.9 volts the strobe is on and at 2.5V the strobe is off. For vendor comparison purposes the actual voltages that turn the strobe on and off were measured instead.

7.3 Test Results

7.3.1 Input Offset Voltage (V_{IO})

Specification: ±2 mV at 25°C, ±3 mV at -55°C and +125°C
Conditions: $R_S = 50\,\Omega$, $V_{OUT} = 1.5V$
Results:

Vendor	T_A °C	Samples Tested	Max	Min	Avg
A	+25	10	1.16	0.12	0.55
	-55	10	1.43	0.02	0.63
	+125	10	1.43	0.03	0.64
D	+25	10	1.55	0.08	0.70
	-55	10	1.50	0.21	0.66
	+125	10	1.77	0.16	0.94

7.3.2 Input Offset Voltage Temperature Sensitivity ($\Delta V_{OUT}/\Delta T$)

Specification: 10 μV/°C maximum from +25°C to -55°C and +25°C to +125°C
Conditions: R_S = 50 Ω, V_{OUT} = 1.5 V
Results:

Vendor	T_A(°C)	Samples Tested	Max	Min	Avg
A	+25 to +125	10	7.3	0.2	3.2
	+25 to -55	10	4.2	1.2	2.8
D	+25 to +125	10	8.0	0.8	5.0
	+25 to -55	10	9.4	0.4	3.1

7.3.3 Input Offset Current (I_{IO})

Specification: 3.0 μA maximum at +25°C, 7.0 μA maximum at -55°C,
3.0 μA maximum at +125°C
Results:

Vendor	T_A(°C)	Samples Tested	Max	Min	Avg
A	+25	10	.142	.005	.053
	-55	10	.163	.009	.072
	+125	10	.120	.000	.057
D	+25	10	.224	.016	.081
	-55	10	.276	.012	.138
	+125	10	.154	.020	.086

7.3.4 Input Offset Current Temperature Sensitivity ($\Delta I_{IO}/\Delta T$)

Specification: 25 nA/°C at +25°C to +125°C and 75 nA/°C at +25°C to -55°C
Results:

Vendor	T_A(°C)	Samples Tested	Max	Min	Avg
A	+25 to +125	10	1.56	0.05	0.69
	+25 to -55	10	1.16	0.01	0.43
D	+25 to +125	10	1.60	0.13	0.82
	+25 to -55	10	1.02	0.05	0.63

7.3.5 Input Bias Current (I_{IB})

Specification: 20 μA maximum at +25°C and 45 μA maximum at -55°C and +125°C

Results:

Vendor	T_A(°C)	Samples Tested	Max	Min	Avg
A	+25	10	7.2	2.4	4.8
	-55	10	15.3	5.1	10.1
	+125	10	2.1	0.6	1.4
D	+25	10	10.1	2.9	7.3
	-55	10	18.1	6.4	13.6
	+125	10	4.3	1.0	2.9

7.3.6 Strobe Current (I_{STROBE})

Specification: 3.3 mA maximum at +25°C, -55°C and +125°C
Conditions: V_{STROBE} = 0.4 V, V_{ID} = -5 mV
Results:

Vendor	T_A(°C)	Samples Tested	Max	Min	Avg
A	+25	10	2.65	2.25	2.45
	-55	10	2.20	1.85	1.99
	+125	10	2.10	1.65	1.81
D	+25	10	2.40	1.35	2.11
	-55	10	2.05	1.60	1.84
	+125	10	1.85	1.35	1.57

7.3.7 Common Mode Rejection Ratio (CMRR)

Specification: 80 db minimum at +25°C, -55°C and +125°C
Conditions: V_{OUT} = 1.5 V, V_{IN} (common) = ±5 V
Results:

Vendor	T_A(°C)	Samples Tested	Max	Min	Avg
A	+25	10	100	88	96
	-55	10	108	87	95
	+125	10	100	91	95
D	+25	10	120	88	101
	-55	10	114	81	96
	+125	10	120	86	104

7.3.8 High Output Level (V_{OH})

Specification: 2.5 V minimum to 5.5 V maximum at +25°C, -55°C and +125°C
Conditions: V_{ID} = +5 mV, I_{OH} = 400 μA
Results:

Vendor	T_A(°C)	Samples Tested	Max	Min	Avg
A	+25	10	3.93	3.67	3.83
	-55	10	3.62	3.37	3.54
	+125	10	4.23	3.95	4.11
D	+25	10	4.27	3.73	4.00
	-55	10	3.95	3.43	3.71
	+125	10	4.58	3.95	4.30

7.3.9 Low Output Level (V_{OL})

Specification: 1.0 V maximum at +25°C, -55°C and +125°C
Conditions: V_{ID} = -5 mV, I_{OL} = 50 mA
Results:

Vendor	T_A(°C)	Samples Tested	Max	Min	Avg
A	+25	10	.541	.458	.504
	-55	10	.534	.426	.487
	+125	10	.643	.551	.600
D	+25	10	.579	.453	.516
	-55	10	.629	.474	.549
	+125	10	.726	.551	.635

Specification: 0.4 V maximum at +25°C, -55°C and +125°C
Conditions: V_{ID} = -5 mV, I_{OL} = 16 mA
Results:

Vendor	T_A(°C)	Samples Tested	Max	Min	Avg
A	+25	10	.282	.232	.259
	-55	10	.268	.212	.242
	+125	10	.327	.274	.299
D	+25	10	.295	.247	.274
	-55	10	.307	.241	.268
	+125	10	.351	.275	.312

7.3.10 Strobe ON Voltage

Specification: 0.9 V minimum at +25°C, -55°C and +125°C
Results:

Vendor	T_A(°C)	Samples Tested	Max	Min	Avg
A	+25	20	1.35	1.25	1.30
	-55	19	2.14	1.62	1.70
	+125	20	.985	.900	.931
D	+25	20	1.46	1.37	1.41
	-55	20	1.78	1.64	1.71
	+125	20	1.04	.911	.984

NOTE: Each device has two strobes; one strobe from Vendor A did not operate at -55°C.

7.3.11 Strobe OFF Voltage

Specification: 2.5 V maximum at +25°C, -55°C and +125°C
Conditions: I_{OL} = 16 mA
Results:

Vendor	T_A(°C)	Samples Tested	Max	Min	Avg
A	+25	20	1.67	1.60	1.62
	-55	19	2.39	1.82	1.92
	+125	20	1.33	1.21	1.25
D	+25	20	1.73	1.62	1.66
	-55	20	2.02	1.81	1.93
	+125	20	1.38	1.21	1.30

NOTE: Each device has two strobes.

7.3.12 Output Leakage Current(I_{CEX})

Specification: 1.0 μA maximum at +25°C, 100 μA maximum at -55°C and +125°C
Conditions: V_{ID} = +5 mV, V_{OUT} = +24 V
Results:

Vendor	T_A(°C)	Samples Tested	Max	Min	Avg
A	+25	10	0.180	0.042	0.086
	-55	10	0.250	0.115	0.199
	+125	10	93.0	29.5	62.8
D	+25	10	0.110	0.048	0.062
	-55	10	0.250	0.020	0.114
	+125	10	28.0	20.0	24.0

7.3.13 Positive Supply Current (+I_{CC})

Specification: 10 mA maximum at +25°C, -55°C and +125°C
Conditions: V_{ID} = -5 mV
Results:

Vendor	T_A(°C)	Samples Tested	Max	Min	Avg
A	+25	10	6.0	5.4	5.7
	-55	10	6.2	5.4	5.8
	+125	10	4.8	4.3	4.6
D	+25	10	5.6	4.6	5.3
	-55	10	5.9	5.0	5.6
	+125	10	4.6	3.9	4.4

7.3.14 Negative Supply Current ($-I_{CC}$)

Specification: 3.6 mA maximum at +25°C, -55°C, and +125°C
Conditions: V_{ID} = -5 mV
Results:

Vendor	T_A(°C)	Samples Tested	Max	Min	Avg
A	+25	10	1.5	1.2	1.4
	-55	10	1.6	1.3	1.5
	+125	10	1.0	0.8	0.9
D	+25	10	1.4	1.1	1.2
	-55	10	1.6	1.3	1.4
	+125	10	0.9	0.8	0.87

7.3.15 Response Time - Output Saturated High Level to Threshold Level (t_{HTHR})

Specification: 60 nsec maximum at +25°C
Conditions: 100 mV step, 5 mV overdrive
Results:

Vendor	T_A(°C)	Samples Tested	Max	Min	Avg
A	+25	10	35.0	29.0	32.3
	-55	3	27.0	25.0	26.0
	+125	10	47.0	40.0	43.8
D	+25	10	35.0	30.0	32.6
	-55	3	28.0	28.0	28.0
	+125	10	44.0	40.0	42.6

7.4 Analysis of Test Results

Vendor A - All devices except one met all the specifications; one strobe did not operate at -55°C. On two parameters, the results were marginal. For Strobe ON Voltage at +125°C, the requirements is .90 volts min. and the device read .90 volts. For output Leakage Current at +125°C, the requirement is 100 ua max., and one device read 93 ua.

Vendor D - All devices met all the specifications. On three parameters, the results were marginal. For Offset Voltage Temperature Sensitivity, the requirement from +25°C to -55°C is 10 uv/°C; one device read 9.4 uv/°C. For Common Mode Rejection Ratio at -55°C, the requirement is 80 db min.; one device read 81 db. For Strobe ON Voltage at +125°C the requirement is .90 V min.; one device read .91 V.

Section VIII

723 REGULATOR EFFORT

The rough draft of MIL-M-38510/102 received from RADC was reworked into a final format. All the tables were redone to the format of MIL-M-38510/101 and the figures were redrawn. Major effort went into preparation of the test circuits for d.c. electrical testing. This includes a test schematic and a complete test table. A.c. parameters and test procedures were added for voltage and current transient response. The specification can be found in the Appendix of this document.

Section IX

MEMORY CONSIDERATIONS

9.0 Introduction

The test problems associated with semiconductor memories are the same as those of LSI devices in general. The major problems are high circuit density with few access points and the exact realization of the internal logic circuits that are unknown or known at one point in time but changes as technology advances. Fortunately, the memory is an extremely orderly function, and functional testing of the devices should provide a high Testing Confidence Level (TCL). Functional testing can be defined as static or at a repetition rate (dynamic) commensurate with the memory access or cycle time. Unique tests would be required that depend on the technology used to construct a particular device, topology, or the organization.

The functional test does imply however that hundreds and thousands of tests are required and, in some instances, at high repetition rates. This also indicates the need for automated test equipment if the devices are to be evaluated properly.

The approach used to analyze the functional test problem is to consider the memory as a "black box" with smaller internal black boxes, i.e., memory cells, decoders, sense amplifiers, etc. The integrity of the basic memory function of data storage and data recovery must be verified under various conditions of supply voltages, temperature, etc. Several levels of functional testing and a variety of test patterns to analyze the memory as a "black box" will be discussed:

Pattern Sensitivity Testing
Memory Pattern Testing
Walking-One-Walking-Zero Pattern Testing
Galloping-One-Galloping-Zero Pattern Testing
Write Recovery Pattern Testing
Data Retention Pattern Testing

The effectiveness of each test pattern relative to detecting potential faults and the number of tests required to perform these patterns are also given.

9. [illegible] Considerations

9. [illegible] Static Memory

9. [illegible] Static Functional Tests

A typical [illegible] configuration has five sets of terminals [illegible] power [illegible]

1. Data Input Terminal

   Number of data input lines is equal to the word length (bits per word).

2. Data Output Terminal

   Number of data output lines is equal to the word length (bits per word).

3. Address Input Terminal

   Number of address lines is equal to N, where 2^N equals the number of words.

4. Read/Write Terminal

   Assume Read/Write terminal requires one control line.

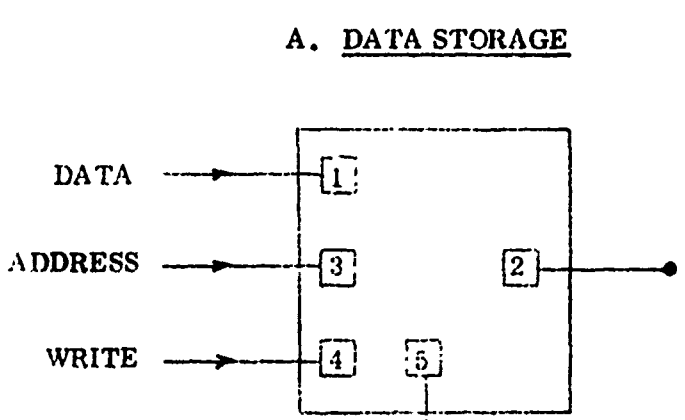
5. Chip Select Terminal

   Assume Chip Select Terminal requires one control line.

The RAM performs two basic functions:

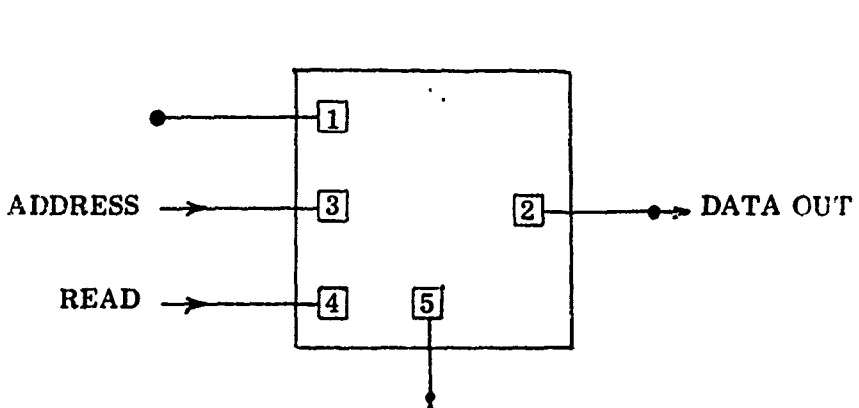
A. Data Storage
B. Data Recovery

A. DATA STORAGE



In the storage mode, the data to be stored is loaded on the data input lines (1). The address lines (3) are loaded with the storage location data. The chip select input (5) is in the required state that enables the device. When all the above conditions are met the data can be written into its required location by the application of a write signal to the Read/Write input.

B. DATA RECOVERY



To recover a word from memory, the chip select input is set to the required state that enables the chip; the read/write input is set in the read mode and the location of the desired word is loaded on the address lines. The desired word is then accessible from the data output lines (2).

NOTE: If the chip select input is at the level that disables the chip, it is impossible to write in or read out data and the data output lines will be at the same logic level (assume a Logic 1).

If the exact configuration, relative placement on substrate, and the most probable failure patterns of a RAM were known, it would be relatively easy to develop a test that would have a high confidence level with a minimum amount of test vectors.

Under normal circumstances, the above information is not available. Even if this information were known for a particular RAM, at some time, a change by the manufacturer in his processes, layout, or circuit design (Variable factors of production) would reduce the confidence level previously obtained. If it is assumed that the devices used are to be functionally specified, it is more than likely that the same manufacturer, at different times, and different manufacturers will have different variable factors of production. It is impossible, under the above conditions, to obtain an optimized set of test vectors based on the factors of one configuration that will guarantee a high confidence level on all other configurations.

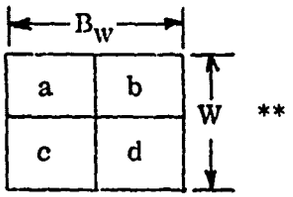
Based on the above, various approaches to testing might be considered, the most stringent being pattern sensitivity testing.

+ Pattern sensitivity, a relatively new term to semiconductor people, is not necessarily related to memories but to LSI, and memories happen to be of the first LSI forms available. Pattern sensitivity is the sensitivity to data or address patterns that cause device malfunction. Pattern sensitivity is caused by unique circumstances or combinations of events that cause parameter(s) to shift to extreme values. These results of the circumstances could yield electric fields, hot spots due to power dissipation, or cumulative charge on a line due to a long sequence of ones or zeroes. Each memory design will exhibit unique pattern sensitivities and the same design using two different processes could yield different pattern sensitivities. Also, the same supplier can cause many variations of sensitivities due to normal processing tolerances.

To perform this type of testing on a functionally specified memory, an indeterminate number (∞) of test vectors would be required.

Another level of testing would be memory pattern testing. The objective of this type of testing is to check that all possible bit patterns are obtainable and would show complete static independence of each bit.

In order to derive an equation for the number of test vectors* required for testing a W x Bw (Number of Words X Number of Bits per Word) RAM using memory pattern testing, a 2 X 2 RAM will be evaluated.



**

* A Vector is a pattern of 1's and 0's that contains the required information to either Write in a Data Word or Read out a Data Word.

** These diagrams are pictorial descriptions of the contents of the memory and are not an attempt to describe organization.

+ Lauffer, Don and Lim, Peng: "A User's Look at MOS-RAMS for Main Frame Memory" IEEE 71 International Convention Digest, March 1971.

The number of bit patterns possible is $2^{W \times Bw}$ which for a 2 X 2 RAM equals $2^{2 \times 2} = 2^4 = 16$

a	b	c	d
0	0	0	0
1	0	0	0
0	1	0	0
1	1	0	0
0	0	1	0
1	0	1	0
0	1	1	0
1	1	1	0
0	0	0	1
1	0	0	1
0	1	0	1
1	1	0	1
0	0	1	1
1	0	1	1
0	1	1	1
1	1	1	1

The number of test vectors required to write in data for the entire test is:

$$\sum_{Z=0}^{Z=(W-1)} \frac{2^{W \times B_W}}{(2^{Bw})^Z} = \sum_{Z=0}^{Z=(W-1)} 2^{B_W (W-Z)}$$

The number of test vectors required to read out data for the entire test is:

$$2^{W \times Bw} \times W$$

Therefore, the total number of test vectors (V_t) required to test a device (including the vectors required to check out the Chip Select Terminal) is:

$$V_t = 2^{W \times B_W} \times W + \sum_{Z=0}^{Z=(W-1)} \frac{2^{W \times B_W}}{(2^{B_W})^Z}$$

To emphasize the impracticability of this type of testing, a 32 word x 4 bit array would require a

$$V_t = (2^{128} \times 32) + \sum_{Z=0}^{Z=31} \frac{(2^{128})}{(2^4)^Z} = 1.124 \times 10^{40}$$

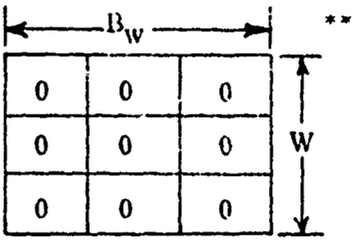
If the tests were run at 1M Hz, it would take approximately 3.562×10^{26} years to complete the tests.

Since the above approaches are impractical, the Walking-One-Walking-Zero method of testing will be used as a baseline for further study.

The objective of Walking-One-Walking-Zero Pattern testing (Writing a One in a field of Zeroes and a Zero in a field of Ones) is to show the independence of each bit in both the zero and one state with respect to all other bits which are in the complement state.

In order to derive an equation for the number of test vectors required for testing a W x B (Number of Words x Number of Bits per Word) RAM, a 3 x 3 RAM will be evaluated.

I. Determine that the entire memory can be loaded with all "0"'s.



A. 3 Vectors required to write in data
B. 3 Vectors are required to read out data

W	+	W
(Write In) Data		(Read Out) Data

II. Determine that a single location in memory can be uniquely loaded with a "1".

1	0	0
0	0	0
0	0	0

A. 1 Vector is required to write in data.
B. 3 Vectors are required to read out data.

III. Determine that the next location can be uniquely loaded with a "1"

0	1	0
0	0	0
0	0	0

A. 1 Vector required to write in data
B. 3 Vectors required to read out data

IV. Determine that the next location can be uniquely loaded with a "1"

0	0	1
0	0	0
0	0	0

A. 1 Vector required to write in data
B. 3 Vectors required to read out data

V. Determine that the next location can be uniquely loaded with a "1"

0	0	0
1	0	0
0	0	0

A. 2 Vectors required to write in data
B. 3 vectors required to read out data

VI thru X. Continue above procedure until a "1" has been walked through the entire memory.

The total number of vectors required for steps I thru X is:

$$2W + WB_W (W + 1) + W - 1$$

$$3W + WB_W (W + 1) - 1$$

For steps XI thru XX the same procedure as steps I thru X except a "0" is walked thru a field of ones.

The total number of vectors (V) required for steps I thru XX is:

$$V = 2 \left[3W + WB_W (W + 1) - 1\right]$$

$$V = 6W + 2WB_W (W + 1) - 2$$

Since $W \times B_W$ = total number of bits (B_t)

$$V = 2B_t (W + 1) + 6W - 2$$

XI. Determine that chip select is operable

0	0	0
0	0	0
0	0	0

A. 3 Vectors required to write in data
B. With chip disabled and in the read mode, 3 vectors are required to read a logic 1 on each data output line for each address.
C. With Chip disabled, in the Write mode and data input lines at a Logic 1 it requires 3 Vectors to attempt to Write in a Logic 1 in each memory location.
D. With Chip enabled and in the Read mode, it requires 3 Vectors to ensure that a Logic 0 is in every memory location.

$$W + W + W + W = 4W$$

(Write In) Data (Read Out) Data

The total number of Test Vectors (V_t) required with this test approach is:

$$V_t = 2 B_t (W + 1) + 10 W - 2$$

Using the same 32 x 4 bit RAM as an example, 8,254 test vectors are required. Testing at a 1 M Hz rate, it would take 8.25 milliseconds of test time.

9.1.1.2 Dynamic Functional Tests

A Walking-one-Walking-zero method of testing was developed and has been discussed. The objective was to show the independence of each bit in both the zero and one state with respect to all other bits which are in the complement state. Dynamic Functional tests considerations were not previously discussed.

One of the most important test considerations for a RAM is its access time. Access time is the time required in a read cycle to guarantee valid output data after its respective address is stabilized. The access time in one cycle is affected by the previous cycle and the data pattern stored in the memory. A different effect will be obtained depending on whether the previous cycle was a read or write.

In order to test access time adequately, it is necessary to check all possible address transitions (addressing) from a read cycle to a read cycle, and all possible address transitions from a write cycle to a read cycle.

A program that fulfills the first requirement above would be as follows:

1. Write a pattern of all zeroes into all memory locations.
2. Write a pattern of all ones into word location one.
3. Read word two
4. Read word one
5. Read word three
6. Read word one.

After every pair of transistions is checked:

1. Write a pattern of all zeroes into word location one.
2. Write a pattern of all ones into word location two.
3. The previous sequence is repeated by checking all transitions with the second word.

The above procedure would be repeated for the entire memory. The patterns would then be reversed and the entire procedure is repeated. Macrodata Company has developed a program that implements the above and has named it Galloping Ones and Zeroes.

In order to fulfill the second requirement for testing access time, a program such as the following is used.

1. Write a pattern of all zeroes into the entire memory.
2. Write a pattern of all ones into the second word location.
3. Read the first word.
4. Write a pattern of all zeroes into the second word location.
5. Read the first word.
6. Write a pattern of all ones into the third word location.
7. Read the first word.

Repeat this procedure until the entire memory is checked. The entire procedure is then repeated with the patterns reversed. This program tests for write recovery.

By performing a walking-one-walking-zero pattern, galloping-one-galloping-zero pattern, and a write recovery pattern, a comprehensive functional check of a static RAM is attained. This combination of test patterns performs an excellent check for bit independence, access time, write recovery, and addressing.

The number of test vectors required for each of the above patterns is as follows:

Walking-one-Walking-Zero	$2 B_T (W + 1) + 10W - 2$
Galloping-one-Galloping-Zero	$4W^2 + 4W + 3$
Write Recovery	$6W^2 + 4W + 4$

9.1.2 Dynamic Memory

The test considerations discussed previously apply to dynamic memories as well. Additional test considerations must be made since dynamic memories use capacitor storage. This technique of storage has a time constant associated with it in which the stored data (charge) decays. Therefore, the data must be updated or refreshed at a rate commensurate with the associated time constant or the data would be lost.

As an example, the 1103 memory cells are dynamic and require periodic data refreshing. This is accomplished by cycling through (Read Cycle) the 32 addresses of the A_0 through A_4 inputs at least every 2 milliseconds. Only 32 addresses are required because the 1024 bit memory is arranged in a 32 x 32 bit matrix and a complete row is refreshed at one time. The 1103 memory is organized as a 1024X1 for normal operation and as a 32 x 32 for refresh.

A test for verifying the circuit time constants or data retention could be implemented in the following manner. Write a test pattern, (this pattern is chosen to minimize the data output signal), wait maximum delay time (refresh time), read to verify data pattern, write test pattern complement, wait refresh time, read to verify test pattern complement, etc.

In general, a set of test patterns that will provide a comprehensive functional test for a dynamic memory are:

1. Walking-one-Walking-zero Pattern
2. Galloping-one-Galloping-zero Pattern
3. Write Recovery Pattern
4. Data Retention Pattern

9.2 ROM Test Considerations

9.2.1 Masked Generated

Remove the write capability from a RAM and you create a ROM. However, it is still a random access device, because the access time is independent of data location.

There are two functional test requirements for a custom-masked ROM. One is obvious and that is to verify the proper stored data at the respective address (location). The second is a test for Access Time. This test is essentially the same as indicated for the RAM and would be implemented as follows:

Read location 2
" " 1
" " 3
" " 1
" " 4

Read location 1 etc.

then

Read location 1
" " 2
" " 3
" " 2
" " 4

Read location 2 etc.

Continue the above sequence of testing throughout the entire memory. The number of test vectors required for the above pattern is $2W^2$.

9.2.2 Field Generated PROM

Electrically alterable or field-programmable ROM's commonly called Programmable Read Only Memories (PROM's) once programmed have the same functional test

requirements as the factory masked generated ROM, i.e., pattern integrity and access time.

However, PROM's have a unique testing problem in that when they are unprogrammed, all outputs are in one state regardless of address. Therefore, testing does not detect many faults in the internal circuitry such as decoders, memory array, and sense amplifiers.

It is recommended that adding an extra bit to each word for testing purposes, is an excellent way to provide for functional and dynamic testing. A 64 word, 8 bit memory would be expanded to 64 words by 9 bits. This extra bit used properly would provide a high confidence that the internal circuitry is functioning and a sampling that the links can be blown.

A recommended comprehensive test utilizing the extra bit would be as follows:

- Read all word locations
- Program extra bit in LOCATION 1
- Read location 1
- Read location 2
- Read location 1
- Read location 3
- Read location 1

etc. throughout the memory

- Program extra bit in LOCATION 2
- Read location 2
- Read location 1
- Read location 2
- Read location 3
- Read location 2
- Read location 4
- Read location 2

etc. throughout the memory

- Program extra bit in LOCATION 3

etc. throughout the memory

The entire above sequence would require

$2 (W^2 + W)$ test steps

Reading the entire memory will show that all outputs are zero. Addressing the first location, programming the extra bit, and then verifying it (Read location 1) will show that a location was programmed. Reading the remainder of the memory in the

above sequence at a specific repetition rate will check the addressing and access time relative to location 1 and that no other bit was programmed.

Addressing the second location, Programming the extra bit and verifying it (Read location 2) will show that a second location (in sequence) was Programmed. Reading the remainder of the memory will verify again access time, addressing and that no other bit was programmed.

When the entire memory has been gone through in this fashion, all the previous tests become meaningful in that it proves the correct number of unique locations exist.

A second alternative, which would not be as complete a test, would be to have the vendor program a specific pattern utilizing the extra bits. The object of the pattern would be to detect a fault at any of the address lines, and again a sampling that the links can be blown.

Obviously, variations of the above tests will provide for different confidence levels.

To determine that chip select is operable, the chip would be disabled and the entire memory would be read ensuring that the output lines were in the proper state.

Section X

MSI/LSI TEST CONSIDERATIONS

10.0 Introduction

MSI/LSI devices will require tests similar to those performed on the present SSI devices: input leakage current, input threshold levels, output voltage levels, and propagation delay. However, these new devices with their increased complexity, number of gates, and memory elements present test problems of a different nature.

The functional level at which component procurement testing must be done will be much higher than the present. The greater complexity of the devices result in more possible failure modes. Consequently, the complexity of the test procedures necessary to guarantee the integrity of the component will be radically increased. Furthermore the fact that large portions of the circuitry of each device will be "buried" within its package without direct access terminals raises fundamental questions about the very existence of a means of testing it.

What complicates the problem further is that multiple sources supply identical functions of different designs. For any given state table or Boolean equation there is a large number of possible circuit realizations which are functionally equivalent, some of them differing quite markedly from one another in types, numbers and interconnections of logic circuit elements.

Based on the above indicated problems it is recommended that for an MSI/LSI device a logic flow diagram depicting the exact realization of the internal circuitry be part of the device specification.

With a logic flow diagram(s) for a specific function an economical approach to functional testing can be established. The method of functional testing which has gained widest acceptance in the IC industry is vector testing. A "Vector" is a pattern of ones and zeroes that contains input and output information for the device under test. The input portion of the Vector is applied to the device and the output portion is compared with the outputs of the device. There are many available Vector Testers with various options available such that implementation of such a test technique is no longer a problem.

Another vector test method advertised is presenting all combination of inputs (2^N) and comparing the outputs of the device under test (DUT) with a known good device. There are many fallacies with this method, the two most obvious is 2^N can become too large, and the method falls apart when testing sequential circuits. This test technique has application for combinational circuits with a relatively small number of inputs.

The problem has now been reduced to the determination of the test vector or set for a specific logic network. Before this can be accomplished, some rationale as to the potential failure modes and how they may be detected must be realized.

Analyzing the problem from a circuit stand point, one question to be answered is, "How in an MSI/LSI device does a buried standard electrical fault (high leakage, high saturation voltage, voltage breakdown, etc.) manifest itself?"

Generally, no topology information is available, i.e., how a gate is actually designed, the exact metalization runs, or placement of the gates (circuits) on the substrate. Usually a gate level mechanization (logic flow diagram) is published for an MSI/LSI device. Since this is the case, the question now becomes, "How do the standard electrical faults manifest themselves as faults at the gate level?" For any particular logic network under known conditions, one can assign a logic 1 or 0 state to every node within the network for every set of input conditions. If a specific node should be a 1 and the remainder of the network responds accordingly, then it is a 1. If the remainder of the network responds as if it were a 0 then a fault exists somewhere. In this manner detection of a fault is accomplished. Since all nodes are not accessible, all faults must be detected via the accessible nodes or pins of a device. It appears then that if a fault occurs it will manifest itself as a logic "state" error.

The next step is to analyze the device at the gate level under known input/output conditions. Determine what potential faults would cause the wrong logic state at any specific node. The potential faults are:

1. Open nodes
2. Nodes shorted to a voltage that is interpreted as a logic 0.
3. Nodes shorted to a voltage that is interpreted as a logic 1.
4. Node to Node shorts.

The above faults, with the exception of the Node to Node fault always manifests itself as being stuck at a 1 or a 0. The node to node short may look like a "stuck at" fault, but in order to test for all Node to Node shorts 2^N (where N equals the number of inputs to a network) number of test vectors would be required for combinational networks and an even larger number of vectors for sequential networks.

If the majority of the potential node to node faults manifest themselves as a "stuck at" fault then there exists a high probability that these faults will be detected with a "stuck at" test.

It is implied that if a test can be implemented that will check each node in the network for a "stuck at" condition then a high testing confidence level can be attained. This approach to testing has gained wide acceptance in industry as being effective and economically feasible. Basically, the objective of developing a "stuck at" test for a particular node is as follows:

1. Select a node.
2. Sensitize a path from the input pins of the network to the output pins of the network. In other words determine a set of input conditions such that at least one output is dependent upon the logic state of the node selected.
3. Specify whether checking for stuck at a 1 or 0 (assume stuck at 0).
4. Set input conditions for a logic 1 at selected node.
5. Check output to see if the selected node is stuck at a 0.
6. Repeat above to check for a stuck at 1 condition.

The entire network would be gone through in the above fashion in order to design a complete "Stuck at 1", "Stuck at 0" test.

The problem now is how to generate the above sequence of tests for MSI/LSI logic networks.

10.1 Automatic Test Generation

Currently there are three options available for designing a test procedure for logic networks. They are:

1) Manual design and verification of the Test Vector Set
2) Manual design of Test Vector Set with computer aided verification, via a fault simulation program
3) Automatic Test Vector Generation by computer program.

The first option rapidly becomes economically impractical and unreliable due to human error. Therefore computer aids such as those mentioned in options 2 and 3 are becoming a must.

The computer program used at GEOS to generate the "stuck at" tests is the Automatic Test Vector Generation (ATVG) program. The program was used to evaluate the 934-X (4 by 2 multiplier), 9341-54181 Arithmetic Logic Unit (ALU) and the 2 bit and 4 bit Full Adders under this contract. The detailed evaluation of these devices will be discussed later and a brief discussion of the program follows.

The ATVG Program is a combination of Options 2 and 3 in that is generates test vectors and has a fault simulation option. The test vector set is generated to test for a failure condition of "stuck at 1" or "stuck at 0" of every possible lead of the network. It is assumed that only a single failure is present at any one time.

For test vector generation, the following inputs are required:

1) Module description file - description of the logic elements in the network

2) Module location file - location of the elements in the network
3) Interconnection file - interconnection of the elements in the network.

For the fault simulation option, an additional input of a vector set would be required.

The typical way the program was used is best described by the evaluation of two alternate mechanizations (Vendors E and D) of the 4 bit full adder.

1) Generate the card decks for both network mechanizations of the adder.
2) Input the ATVG with one mechanization (Vendor E) for vector generation. Obtain test vector set.
3) Using the fault simulation and vector generation option, the program is inputted to evaluate the effectiveness of the Vendor E vector set on the Vendor D mechanization and to generate vectors for any tests not accomplished.

At this point a set of test vectors has been generated that provides for a 100 percent Testing Confidence Level (TCL*) for both mechanizations of the adder.

It is not intended to imply that programs like the ATVG program is a cure-all and can be used blindly. It is an excellent engineering tool and with it, effective economical function tests can be generated.

10.2 Functional Testing of the 4 X 2 Multiplier

The 934 X chip, Figure 10.1, is an LSI array of 93 gates designed by Vendor A using their Bipolar Micromosaic TM concept. The basic chip is defined as:

- It multiplies a 4 bit number X by a 2 bit number Y and adds a 4 bit number K and also a 2 bit number M to the product to form a 6 bit result S.

$$S = (X)(Y) + M + K$$

- X and K have a range of 0 to 15
- Y and M have a range of 0 to 3

- Worst case this generates (15)(3) + 15 + 3 = 63
- Therefore requires a 6 bit output

- Therefore requires 12 inputs and 6 outputs

- [illegible]

*The [illegible] program [illegible] tests needed [illegible] total number of gate pins [illegible]

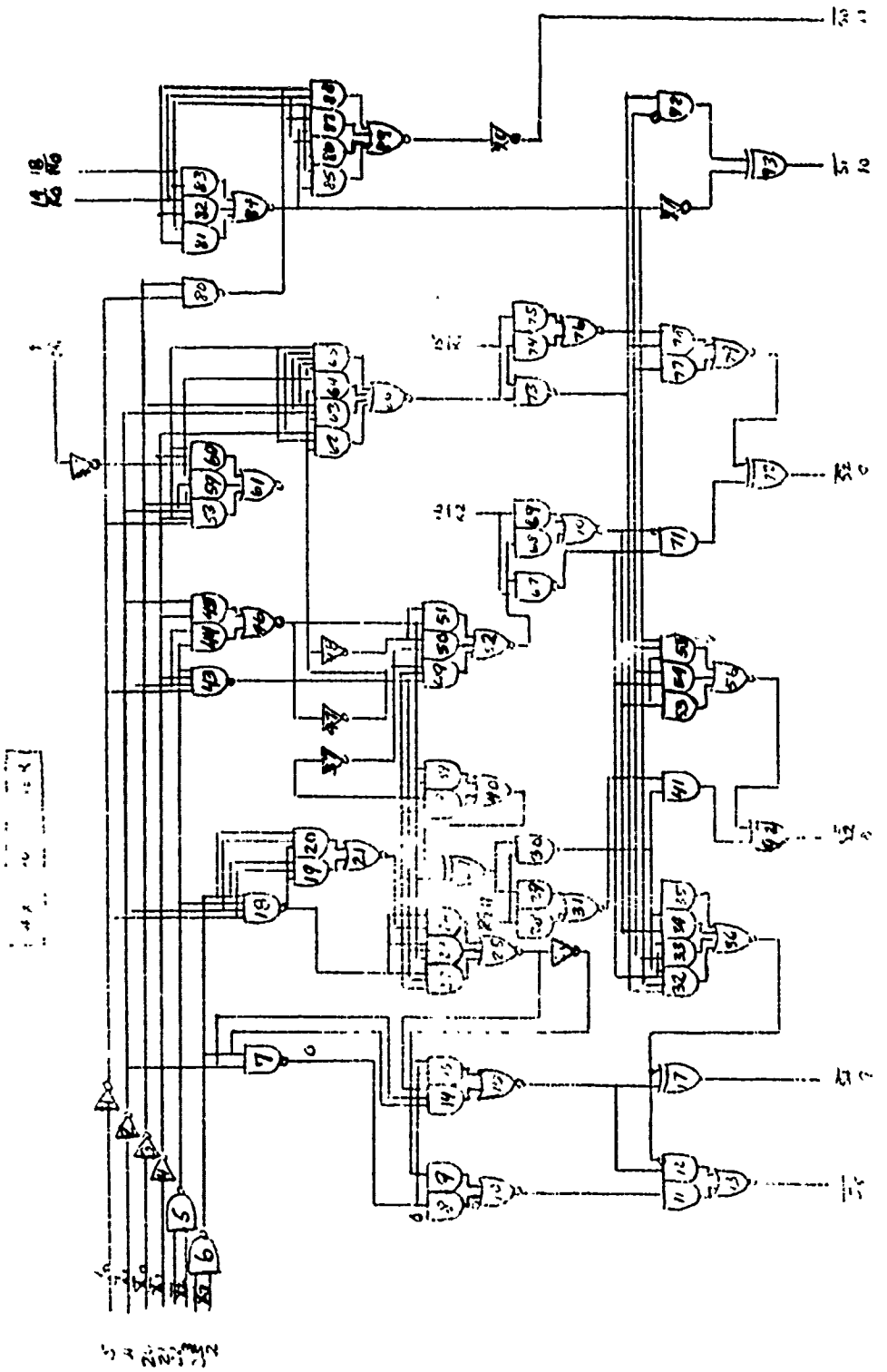


Figure 10.1. 8X8X Chip

Two sets of test vectors were generated, one manually and one using the Automatic Test Vector Generation (ATVG) program.

The criteria used to generate the tests manually was to put at least one "0" and "1" on all inputs and outputs based on the function. In addition, multiplication by zero and the maximum product was checked. The total number of test vectors required to perform the above was 21. Five chips were tested successfully using these vectors.

The second set of test vectors was generated by the ATVG program. The set consisted of twenty-six vectors. The five chips were retested successfully.

Three tests were listed in the "Test Not Accomplished List" of the ATVG output. The three not possible were three inputs to two AND gates (gates 23 and 39). In order to test these inputs, a logic 0 has to be present on the input under test while all other inputs of that respective gate are held at Logic 1. It was noted that if any of the untested inputs were at a Logic "0", another input of its respective gate was also at a Logic "0". See Note 1.

Therefore these inputs can not be tested as separate entities. In other words, if an "open" occurs at these inputs, no malfunction occurs. However, if a "short" occurs, a fault will be detected at the output.

Based on the ATVG testing criteria, there are 341 tests that should be performed to check the 93 gates in the device. Since the three tests not accomplished are irrelevant to the function of the device, the Testing Confidence Level (TCL) will be based on 338 tests required.

$$TCL = \frac{\text{Tests Accomplished}}{\text{Tests Required}} \times 100 \text{ percent}$$

The following is a summary of TCL's and approximate costs in comparing the two sets of test vectors generated.

	TCL	Man hours	Computer Time
Manual Set	75 percent*	8	
ATVG Set	100 percent*	12	$215

*The Fault "Simulation Option" (See Note 2) of the ATVG program was used to determine the effectiveness of the manually generated test vectors. It must be noted that the TCL was unknown until this was done and the cost to determine the TCL is not included in the eight hours.

If an attempt were made to generate the test vectors, fault dictionary and documentation equivalent to that provided by the ATVG program, it is estimated that one (1) man-month of engineering effort would be required.

NOTE 1: The Boolean equation for the untested inputs are:

Inputs 1 and 2 = $\overline{Y_0} + \overline{Y_1} + \overline{X_1} + (\overline{X_2 A})(\overline{X_2 B})$

Input 3 = $\overline{Y_0} + \overline{Y_1} + (\overline{X_2 A})(\overline{X_2 B}) + (\overline{X_3 A})(\overline{X_3 B})$

Another input that is common to the two AND gates has a Boolean equation as follows:

Input 4 = $(\overline{Y_1} + \overline{X_1})\ \overline{Y_0} + (\overline{X_2 A})(\overline{X_2 B})$

In order to test inputs 1 and 2, it is necessary to hold the input under test at a logic "0" and all other inputs, of that respective gate, at a Logic 1.

For inputs 1 and 2 to be a Logic 0, the following conditions must exist:

$Y_0 = 1$

$Y_1 = 1$

$X_1 = 1$

X_2A or $X_2B = 1$

When Y_1 and X_1 are at a Logic "1", input 4 is at a Logic 0. Therefore, inputs 1 and 2 cannot be tested.

Whenever input 3 is at a Logic 0 the following conditions must exist:

$Y_0 = 1$

$Y_1 = 1$

X_2A or $X_2B = 1$

X_3A or $X_3B = 1$

When Y_0 and X_2A or X_2B are at a Logic "1" input 4 is at a Logic 0. Therefore, input 3 cannot be tested.

10.2 FAULT SIMULATION OPTION

Using this option, the Vector Generation phase of the ATVG Program is inhibited. The manually generated input vectors are inputted in a specific format and a fault simulation of the vector takes place. When the end of the file is reached, a dictionary is printed. This option is used to determine the integrity of the manually generated vectors.

10.3 Functional Testing of the 9341-54181 Arithmetic Logic Unit

The Vendor B μA 9341, Figure 10.2, and Vendor E SN 54181 are four bit, high speed, Arithmetic Logic Units (ALU). These Chips perform all 16 logic operations [illegible] variables plus a variety of arithmetic operations, the most important being add and subtract.

Four mode select lines and an active low carry enable line control operation. In internal carries enabled arithmetic operations are performed, while logic operations are performed. The arithmetic operations are performed on a bit basis, whereas logic operations are on a bit basis.

A signal is provided from the ALU which indicates logic equivalence between bits when the unit is in the subtract mode. This signal can be used together with the carry out signal to indicate A > B or A = B.

Vendor B and E's ALU's, although identical in function, have slightly different logic flow diagrams. Therefore, two sets of test vectors were generated.

The first set of vectors generated was for the Vendor E ALU. Based on the testing criteria* of the ATVG Program, there are 282 tests that should be performed to test all gates completely. Due to module configuration, eight of the 282 tests are impossible to perform. Since the eight tests not possible are irrelevant to the function, only 274 tests are required. The ATVG Program generated 31 vectors which accomplished 268 tests (six tests not accomplished). This represents a Testing Coverage Level** (TCL) of 97.8 percent. The remaining six tests were then accomplished with relative ease, resulting in a TCL of 100.0 percent.

Another set of Vectors was generated for the Vendor B ALU. Based on the testing criteria of the ATVG Program, 265 tests are required (all tests possible). The ATVG Program generated 26 vectors which accomplished 251 tests (14 not accomplished). This represents a TCL of 94.7 percent.

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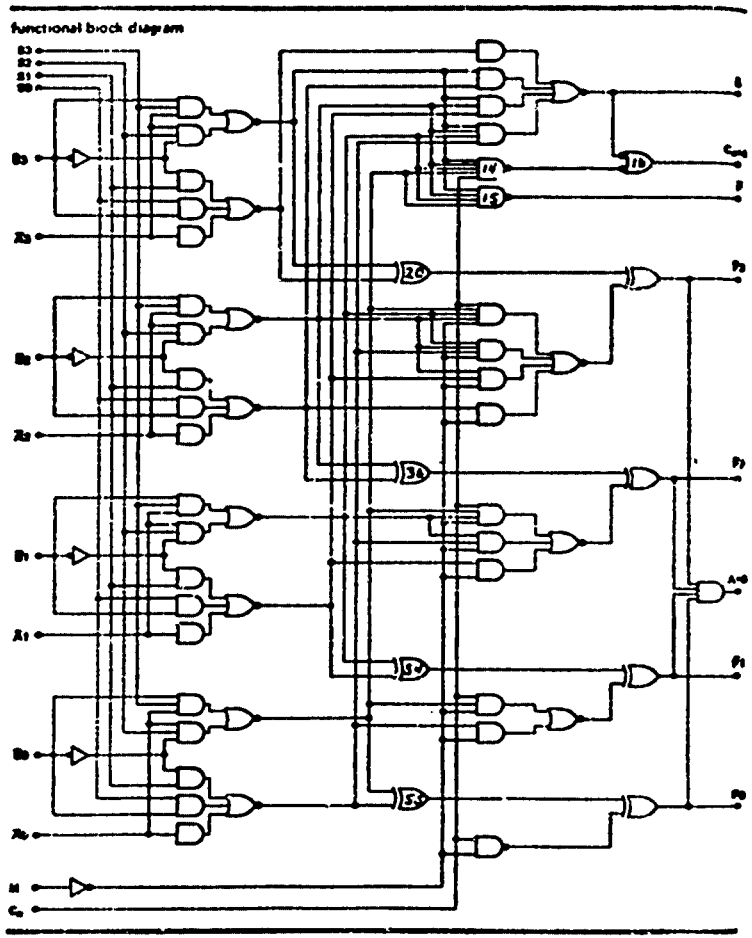
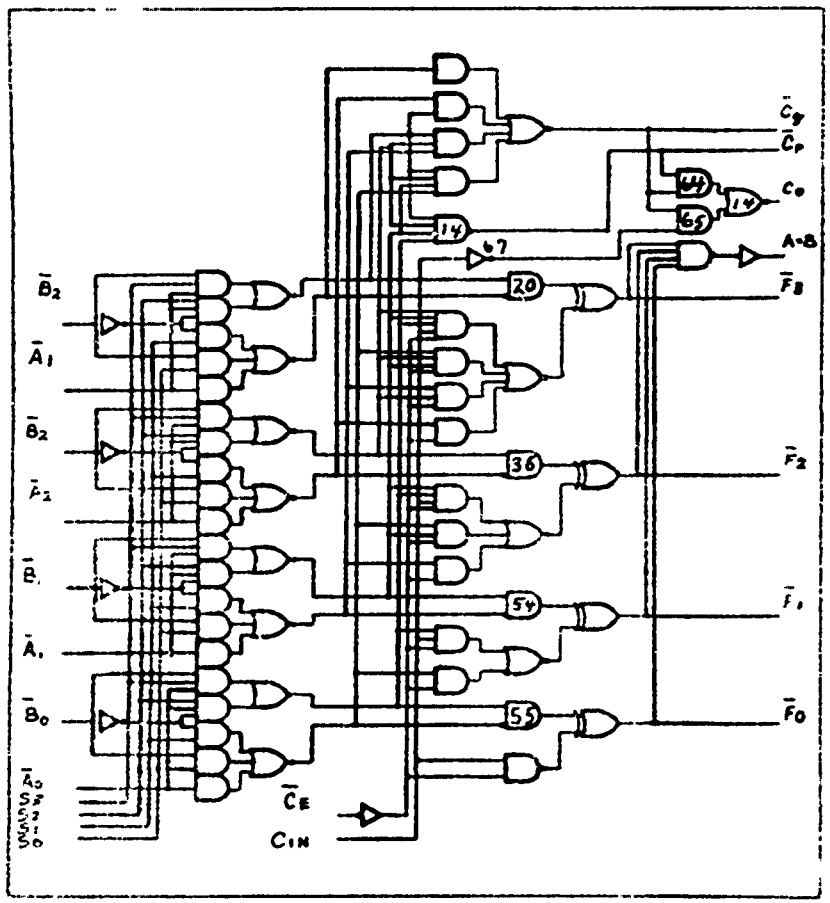
* For purposes of the ATVG Program, the number of tests needed to check a device totally is equal to the total number of gate pins plus connector pins.

** TCL = $\frac{\text{Tests Accomplished}}{\text{Tests Required}}$ X 100 percent



Vendor E SN 54181



Vendor B A9341

Figure 16. 2.

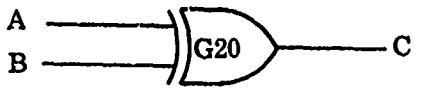
To determine the TCL that could be obtained by testing one device with the test vectors generated for the other and vice versa, two additional runs were made using the Fault Simulation Option of the ATVG Program. First the vectors generated, by ATVG, for the Vendor E ALU were run using the Vendor B ALU logic flow diagram. A total of 260 of the 265 tests required were accomplished resulting in a TCL of 98.1 percent. When the Vendor B ALU generated Vectors were run using the Vendor B ALU logic flow diagram 256 of the 268 required tests were accomplished resulting in a TCL of 95.5 percent. It should be noted that the Vendor E ALU has a five input gate where the Vendor B ALU has a four input gate. Therefore, the Vendor B ALU vectors did not test the extra input of the Vendor E ALU. The vector set generated for the Vendor E unit provided for a 100 percent TCL for both logic mechanizations. Table I is a tabulated summary of the above discussion.

	Vendor E	Vendor B	B Tested with E Vectors	E Tested with B Vectors
Tests Necessary	282	265	---	---
Tests Relevent to the Function	274	265	---	---
Tests Accomplished by ATVG	268	251	260	256
Tests Accomplished Manually	6	*14	---	---
Number of Vectors Generated by ATVG	31	27	---	---
Number of Vectors Generated Manually	4	*10	---	---
ATVG TCL	97.8%	94.7%	98.1%	95.5%
ATVG + Manual TCL	100%	100%	100%	99.6%

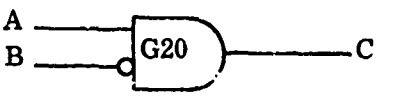
*Those specified as manual were determined both by hand and sorting the tests accomplished by cross checking the Vendor B and E test vectors.

Table 10.1. Tabulated Summary

NOTE 1: The purpose of the following discussion is to explain the differences between the Vendor E and Vendor B ALU's.



Vendor E



Vendor B

The truth tables for both G20's are as follows:

Vendor E

	A	B	C
1	0	0	0
2	1	1	0
3	1	0	1
4	0	1	1

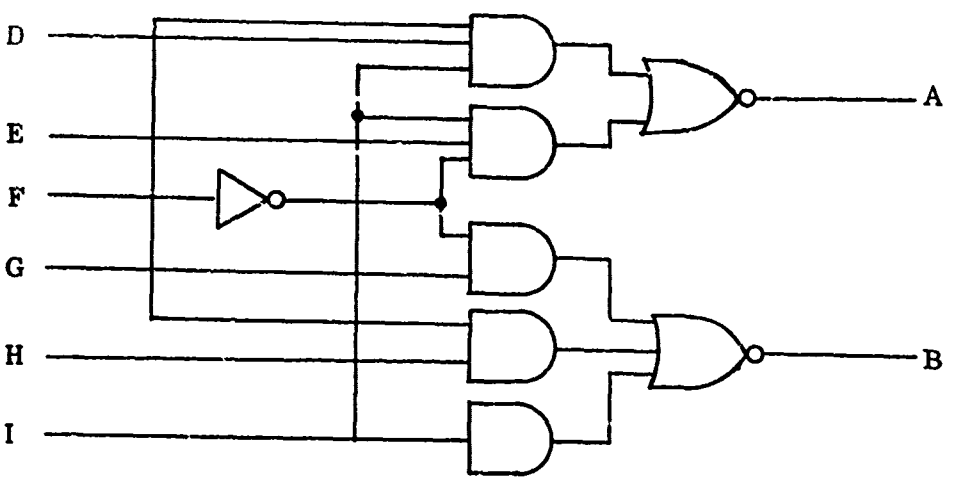
Vendor B

A	B	C
0	0	0
1	1	0
1	0	1
0	1	0

It should be noted that for condition 4, a different output is obtained.

For both G20's to be logically equivalent, condition 4 must be prohibited by the driving logic.

The driving logic for both G20's is



The Boolean equations for the last are:

Boolean Equations:

$$A = \overline{(D\,F\,I) + (E\,\overline{F}\,I)} = (\overline{D} + \overline{F} + \overline{I}) \quad (\overline{E} + F + \overline{I})$$

$$A = \overline{D}\,\overline{E} + \overline{D}\,F + \overline{E}\,\overline{F} + \overline{I}$$

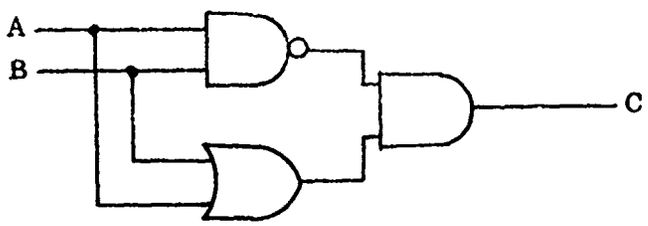
$$B = \overline{(\overline{F}\,G) + (F\,H) + (I)} = (F + \overline{G}) \quad (\overline{F} + \overline{H}) \quad (\overline{I})$$

$$B = F\,\overline{H}\,\overline{I} + \overline{F}\,\overline{G}\,\overline{I} + \overline{G}\,\overline{H}\,\overline{I}$$

It can be seen from the Boolean equations that condition 4 cannot be attained. When B is a logic 1, $\overline{I}$ must be a logic 1. However, if $\overline{I}$ is a logic 1, A is a logic 1. Therefore, as far as the function is concerned the Vendor B G20 is equivalent to the Vendor E G20.

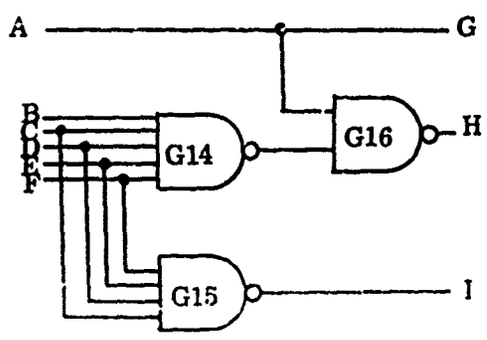
The same condition exists for gates G36, G54 and G55.

The "Exclusive OR" in the Vendor E device was modeled as:

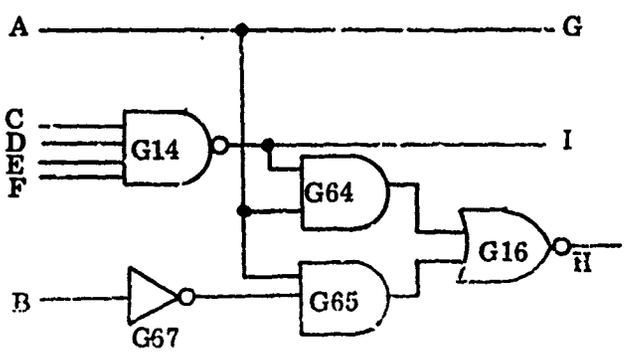


Since all possible input patterns cannot be applied to gates G20, G36, G54 and G55, input A of the NAND gate and input B of the OR gate cannot be tested and are irrelevent to the function.

The Vendor E and Vendor B devices also differ as follows:



Vendor E



Vendor B

The following two sets of Boolean equations are derived to show that both networks in the previous drawing perform the same function.

Vendor E

$$G = A$$

$$H = \overline{(A)\ (\overline{B\ C\ D\ E\ F})}$$

$$H = \bar{A} + (B\ C\ D\ E\ F)$$

$$I = \overline{C\ D\ E\ F}$$

Vendor B

$$G = A$$

$$H = \overline{((\overline{C\ D\ E\ F})A)\ +\ (\bar{B}\ A)}$$

$$H = (C\ D\ E\ F + \bar{A})(B + \bar{A}) = B\ C\ D\ E\ F + \bar{A}\ B\ C\ D\ E\ F + \bar{A}\ B + \bar{A}$$

$$H = B\ C\ D\ E\ G + \bar{A}\ (B\ C\ D\ E\ G + B + 1)$$

$$H = \bar{A} + (B\ C\ D\ E\ F)$$

$$I = \overline{C\ D\ E\ F}$$

Since the expressions for the respective outputs are identical both circuits perform the same function. As noted previously, vectors developed for the Vendor B device which has only a 4 input gate did not test the extra input of the Vendor E configuration which is a 5 input gate.

10.4 Functional Testing of the 2 and 4 bit Full Address

Test vector sets were generated for the 2 bit and 4 bit full address via our ATVG program. The generation of the vector sets were straight forward; however, when comparing the vectors for the two mechanizations of the 4 bit adder, a discrepancy was found. The copy of the Vendor D logic flow diagram had errors such that it did not function as an adder. The corrections were obtained from the vendor and a rerun was made on the ATVG program.

The final output was:

1) A set of test vectors that provide for a 100 percent TCL for the two different mechanizations of the 4 bit adder.

2) A set of test vectors that provide for a 100 percent TCL for the two different mechanizations of the 2 bit adder.

10.5 Logic Integrity Test (LIT)

The Logic Integrity Test is a test established to assure that a logic network is exercised to detect any Stuck "1" or Stuck "0" conditions on all logic element leads relevent to the network function. However, the logic realization of the function must be known. As previously demonstrated with the 9341-54181 ALU and the 2 bit and 4 bit Full Adders, one LIT can be generated for more than one logic realization of the same function.

Using the 9341-54181 ALU preliminary Slash Sheet as an example, the 700 or 800 test conditions in the procedure did not check the entire logic network. Approximately 16 percent of the logic could be defective or missing and the device would pass all tests in the procedure. The LIT would not only exercise the entire network, but would prevent exercising a lengthy test procedure before finding a static functional defect. It is therefore recommended that a Logic Integrity Test be added to each logic device specification.

Many of the d.c. parameter tests could be performed concurrently with the LIT and therefore reduce the number of test steps in the test procedure.

The Logic Integrity Tests for the 54181/9341 ALU's, 2 bit Full Adders, 4 bit Full Adders and the 934X 4 x 2 multiplier are given in tables 10.2, 10.3, 10.4 and 10.5 respectively.

VECTOR No.	$\overline{B_0}$	$\overline{A_0}$	S_3	S_2	S_1	S_0	C_n	M	$\overline{F_0}$	$\overline{F_1}$	$\overline{F_2}$	GND	$\overline{F_3}$	A=B	$\overline{P}$	C_{n+4}	$\overline{G}$	$\overline{B_3}$	$\overline{A_3}$	$\overline{B_2}$	$\overline{A_2}$	$\overline{B_1}$	$\overline{A_1}$	V_{CC}
1	L	L	L	L	L	L	L	L	H	L	L	GND	L	L	L	H	L	L	L	L	L	L	L	V_{CC}
2	L	L	L	H	L	H	H	H	H	H	H		H	H	L	H	L	L	L	L	L	L	L	
3	L	L	H	H	L	L	H	H	H	H	H		H	H	H	L	H	L	H	L	L	L	L	
4	H	H	H	L	L	H	L	L	H	L	L		L	L	H	L	H	H	L	H	L	L	H	
5	L	H	L	H	L	H	L	L	H	H	L		L	L	H	L	H	H	L	L	H	L	L	
6	L	L	H	H	H	H	L	L	L	L	L		L	L	L	L	H	H	L	H	L	H	L	
7	H	L	H	H	L	H	H	L	H	H	L		L	L	L	H	L	L	L	L	L	H	L	
8	L	L	H	L	L	L	H	H	H	H	H		L	L	L	H	L	L	H	L	L	L	L	
9	L	L	H	H	L	L	H	L	L	L	H		H	L	H	H	L	L	L	L	H	L	H	
10	L	H	H	H	H	L	L	L	H	H	H		H	H	H	H	L	L	L	H	L	L	H	
11	L	L	L	H	L	L	H	H	H	H	H		L	L	L	H	L	H	H	L	L	L	L	
12	L	L	H	L	L	H	L	L	H	H	L		H	L	L	H	L	H	L	L	L	H	L	
13	L	H	H	H	L	H	H	L	L	L	H		L	L	H	H	L	L	L	L	L	H	L	
14	L	L	H	H	L	L	H	L	L	L	H		L	L	H	H	L	H	L	L	L	L	H	
15	L	H	L	H	L	H	L	L	H	H	H		H	H	H	H	L	H	L	H	L	L	L	
16	L	L	L	H	L	H	H	L	L	H	H		H	L	L	H	L	H	H	H	H	L	H	
17	L	H	H	H	L	H	H	L	L	L	L		H	L	H	H	L	L	L	H	L	H	L	
18	L	H	L	H	H	L	L	L	H	H	H		H	H	H	H	L	L	L	L	H	H	L	
19	L	H	H	H	H	H	L	L	H	L	L		L	L	H	L	H	H	L	H	L	L	L	
20	L	L	L	H	L	L	H	L	L	L	L		H	L	H	H	L	L	L	L	H	L	L	
21	L	L	H	H	L	H	H	L	L	L	L		H	L	H	H	L	L	L	H	L	H	H	
22	L	L	H	L	L	H	H	L	L	L	H		H	L	L	H	L	H	L	L	H	L	L	
23	L	H	H	H	H	H	H	L	L	L	L		L	L	H	L	H	H	L	H	L	H	L	
24	H	L	H	L	L	H	H	L	H	H	H		H	H	L	H	H	H	L	H	L	H	L	
25	L	L	H	H	L	H	H	L	L	L	L		L	L	H	L	H	H	L	H	H	L	L	
26	H	H	L	H	L	L	H	L	H	H	H		H	H	L	H	H	H	H	H	H	H	H	
27	L	L	H	L	L	L	H	H	H	H	H		H	H	H	L	H	H	H	L	L	L	L	
28	L	H		L	L	H	H	L	H	H	H		H	H	L	H	H	H	L	H	L	H	L	
29	H	L	L		L	L	L	H	H	H	H		H	H	H	L	H	H	H	H	H	L	L	
30	L	H	H		H	H	H	H	L	H	L		H	L	H	L	H	H	H	H	L	H	H	
31	L	H	H	L	H	L	L	H	H	L	L		H	L	H	H	L	H	L	L	L	L	L	
32	H	L	H	H	L	H	L	L	L	L	L		L	L	H	L	H	L	L	L	L	H	H	
33	L	L	L	L	L	L	L	L	H	H	H		L	L	L	H	L	L	L	L	H	L	H	
34	L	H	H	H	H	H	L	H	H	L	H	GND	H	L	H	L	H	L	H	L	H	L	L	V_{CC}

LOGIC INTEGRITY TESTS FOR 54181/9341 ALU'S

TABLE 10.2

VECTOR	INPUTS					OUTPUTS		
	C_0	A_2	A_1	B_2	B_1	$*E_2$	E_1	C_2
1	L	L	L	L	L	L	L	L
2	L	H	H	L	H	L	L	H
3	H	H	H	H	H	H	H	H
4	H	H	L	H	L	L	H	H
5	L	H	H	L	L	H	H	L
6	H	L	H	L	L	H	L	L
7	L	L	H	H	H	L	L	H
8	L	L	L	H	H	H	H	L
9	H	L	L	L	H	H	L	L
10	H	H	H	L	L	L	L	H

* 'E' IS SUBSTITUTED FOR THE GREEK LETTER SIGMA

LOGIC INTEGRITY TESTS FOR 5482/155482
2 BIT BINARY FULL ADDERS

TABLE 10.3

TTL BINARY FULL ADDERS (4BIT)

VECTOR	INPUTS									OUTPUTS				
	C_0	A_4	A_3	A_2	A_1	B_4	B_3	B_2	B_1	$*E_4$	E_3	E_2	E_1	C_4
1	L	L	L	L	L	L	L	L	L	L	L	L	L	L
2	H	L	L	L	H	L	H	H	L	H	L	L	L	L
3	L	L	H	L	H	H	L	L	L	H	H	L	H	L
4	H	H	L	H	L	H	L	H	L	L	H	L	H	H
5	H	L	H	L	H	L	H	L	H	H	L	H	H	L
6	L	H	L	H	L	L	L	L	L	H	L	H	L	L
7	H	L	L	L	L	H	H	H	H	L	L	L	L	H
8	L	L	L	H	H	H	L	H	H	H	H	H	L	L
9	L	L	H	L	L	H	H	L	L	L	L	L	L	H
10	L	L	L	L	H	H	H	L	H	H	H	H	L	L
11	L	H	L	L	L	H	L	L	L	L	L	L	L	H
12	L	L	L	H	L	H	H	H	L	L	L	L	L	H
13	H	L	L	L	L	H	H	H	L	H	H	H	H	L
14	L	L	L	L	L	H	H	H	H	H	H	H	H	L
15	L	L	L	L	H	H	H	H	H	L	L	L	L	H
16	L	H	H	H	H	H	H	H	L	H	H	L	H	H
17	L	H	H	H	H	L	H	L	H	L	H	L	L	H
18	H	L	H	H	H	L	L	H	H	H	L	H	H	L

* 'E' IS SUBSCRIPT FOR THE GREEK LETTER SIGMA.

LOGIC INTEGRITY TESTS FOR SN5483/DM 5483
4 BIT BINARY FULL ADDERS
TABLE 10.4

	INPUTS														OUTPUTS					
VECTOR NO.	$\overline{Y_0}$	$\overline{Y_1}$	$\overline{X_0}$	$\overline{X_1}$	$\overline{X_{2A}}$	$\overline{X_{2B}}$	$\overline{X_{3B}}$	$\overline{X_{3A}}$	$\overline{M_1}$	$\overline{K_0}$	$\overline{M_0}$	$\overline{K_1}$	$\overline{K_2}$	$\overline{K_3}$	$\overline{S_0}$	$\overline{S_5}$	$\overline{S_4}$	$\overline{S_3}$	$\overline{S_2}$	$\overline{S_1}$
1	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
2	H	L	H	H	H	H	L	H	H	H	H	L	H	L	H	H	L	L	H	L
3	L	L	H	L	H	L	H	H	L	L	H	H	L	H	L	H	L	L	H	H
4	L	L	H	L	H	H	H	H	L	H	L	L	L	L	L	H	L	H	L	L
5	L	H	H	H	L	L	L	H	H	L	L	L	H	H	H	H	L	H	H	H
6	L	L	L	L	L	L	H	H	L	L	H	L	L	L	H	L	H	H	L	L
7	L	L	L	L	L	L	H	H	L	H	L	L	L	L	H	L	H	H	L	L
8	H	L	H	L	H	L	L	L	H	H	H	L	H	H	H	H	L	L	L	L
9	L	L	L	L	H	H	L	H	L	L	L	L	H	L	L	L	H	L	L	L
10	L	L	L	L	L	L	H	H	L	H	L	L	H	H	H	H	L	L	H	L
11	H	H	L	L	L	H	L	L	L	H	H	H	L	L	H	H	H	L	L	L
12	L	L	L	L	L	L	H	H	L	H	H	L	L	L	L	L	H	H	L	H
13	L	H	L	L	H	H	L	L	L	L	L	L	H	L	L	H	L	L	H	H
14	L	L	H	H	L	L	L	L	H	L	L	H	H	L	H	L	H	L	L	L
15	L	L	H	L	L	L	H	H	H	H	L	L	L	H	L	H	L	L	H	H
16	L	L	L	L	H	L	L	L	H	L	H	H	H	L	H	L	L	H	L	L
17	H	L	L	L	L	H	L	H	H	H	L	H	L	L	L	L	H	L	H	L
18	L	H	H	L	H	L	H	L	H	L	H	H	H	H	L	H	H	L	L	L
19	L	H	H	L	H	H	L	L	L	L	L	H	L	H	H	H	L	H	H	L
20	H	L	L	L	L	L	H	L	L	L	L	L	L	L	H	L	L	H	H	H
21	H	L	L	H	H	L	L	H	L	H	H	L	L	H	H	L	H	H	H	L
22	L	H	L	L	L	L	L	L	L	H	H	L	L	L	L	H	L	L	L	L
23	L	L	L	H	H	L	H	L	H	H	L	L	H	L	H	L	L	H	H	L
24	L	L	H	H	H	L	H	H	L	H	H	H	L	H	H	H	L	H	H	L
25	H	H	L	L	L	L	H	L	H	H	H	L	L	L	H	H	H	L	L	L
26	L	L	L	H	L	L	L	H	L	H	L	H	H	L	H	L	L	H	H	L
27	L	L	L	L	L	L	H	H	L	H	H	L	H	L	L	L	H	H	H	H
28	L	H	L	L	H	H	H	H	H	L	L	H	H	H	L	H	H	H	L	H

LOGIC INTEGRITY TESTS FOR TTL/MSI 9344, 4 x 2 MULTIPLIER

TABLE 10.5

SECTION XI

Rewrite of Section 3000 of MIL-STD-883

NOTE: To the index of sheet 9 - add 3000.....

.....General Instructions....

METHOD 3000

GENERAL INSTRUCTIONS

FOR TESTING DIGITAL MICROELECTRONIC DEVICES

1. Purpose. This method establishes the general instructions used in testing digital microelectronic devices.

2 Apparatus. The test instrument shall be capable of maintaining the test circuit at any temperature between -55°C and +125°C of applying worst case power supply voltages, and of applying worst case levels at all inputs when specified.

3. Procedure. The circuit under test shall be stabilized at the test temperature specified in the applicable procurement document. The worst case power supply voltage(s) shall be applied and the inputs and outputs shall be conditioned as stated in methods 3001 through 30X2 of this standard and the applicable procurement document.

4. Summary. The following test tolerances shall be observed unless otherwise stated herein or in the applicable procurement document:

(a) Ambient test temperature held to within 3°C.
(b) Power supply and bias voltages held to within 1%
(c) Input conditioning voltages held to within 1%
(d) Input pulse parameters, repetition rate, [illegible] to within 5%.
(e) Breakdown voltages held to within 1%.
(f) Output load currents. - Precaution shall be [illegible] that the maximum output load current flows under worst case output voltage conditions.
(g) Resistive loads shall be ±1%.
(h) Capacitive loads shall be ±5% or 1 pf whichever is greater.
(i) Inductor loads shall be ±5% or 5 μH whichever is greater.
(j) DC parameters shall be measured to within [illegible] meters shall be measured to within 5%

METHOD 3001
DRIVE SOURCE, DYNAMIC

1. Purpose. This method establishes a drive source to be used in measuring dynamic performance of logic gating and flip flop circuits.

2. Apparatus. Each driving source shall be capable of supplying flat top and bottom signals with rise transitions that are linear from 10% to 90% and fall transitions that are linear from 90% to 10%. Each source shall have controlled frequencies, duty factors, signal levels and transition times.

2.1 TTL, DTL. The impedance of the driving source shall be sufficiently low to maintain the signal levels and transition time linearities defined herein or in the applicable procurement document. The line used to transmit the driving signal shall be terminated in it's characteristic impedance at the test jig. Figure 3001-1 shows nominal signal parameters.

2.2 ECL. The driving source shall have the capability of swinging from and to the voltage levels defined herein or in the applicable procurement document. Particular care shall be taken with the source transmission line and line termination to prevent ringing. The line shall be terminated in its characteristic impedance at the test jig. Figure 3001-2 shows nominal signal parameters.

2.3 RTL. The driving source shall have the capability of having an up level of V_{OH} and a down level of V_{OL}, as specified herein or in the applicable procurement document. Figure 3001-3 shows nominal signal parameters.

2.4 C-MOS, MOS (N-Channel). The driving source shall have the capability of having an up level of V_{OH} and a down level of V_{OL}. The impedance of the driving source shall be sufficiently low to maintain signal levels and transition time linearities defined herein or in the applicable procurement document. The line used to transmit the driving signal shall be terminated in its characteristic impedance at the test jig. Figure 3001-4 shows typical nominal parameters.

2.5 MOS (P-Channel). The driving source shall have the capability of having an up level of V_{OH} and a down level of V_{OL}. The impedance of the driving source shall be sufficiently low to maintain signal levels and transition times as specified herein or in the applicable procurement document. The line used to transmit the driving signal shall be terminated in its characteristic impedance at the test jig. Figure 3001-5 shows nominal signal parameters.

3. Procedure. When using the driving sources of paragraphs 2.1 through 2.5, the parameters shall be adjusted according to Figures 3001-1 through 3001-5 respectively unless otherwise stated in the applicable procurement document.

3.1 TTL, DTL. The driving source of 2.1 shall be used. Level V_A shown in Figure 3001-1 is critical to delay measurements and shall be held to within ±20 mV. Level V_B shall be specified as a nominal V_{OH}. The driving signal shall be measured at the input terminal of the device under test.

3.2 ECL. The driving source of 2.2 shall be used. Voltage levels V_A and V_B shown in Figure 3001-2 shall be adjusted so that the threshold point of the device under test is always in the center of the transition region. The driving signal shall be measured at the input terminal of the device under test.

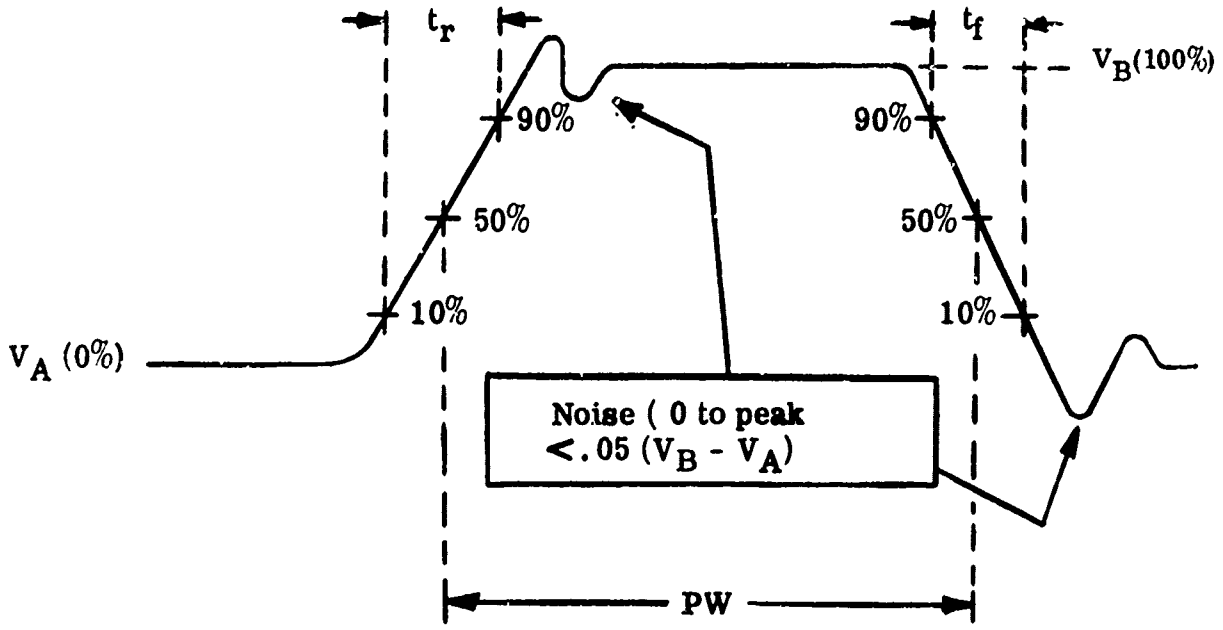
3.3 RTL. The driving source of 2.3 shall be used. Voltage levels V_A and V_B shown in Figure 3001-3 shall be specified as nominal V_{OL} and V_{OH} respectively. The driving signal shall be measured at the input terminal of the device under test with the device removed from the test jig.

3.4 C-MOS, MOS (N-Channel). The driving source of 2.4 shall be used. Voltage levels V_A and V_B shown in Figure 3001-4 shall be specified as nominal V_{OL} and V_{OH} respectively. The driving signal shall be measured at the input terminal of the device under test.

3.5 MOS(P-Channel). The driving source of 2.5 shall be used. Voltage levels V_A and V_B shown in Figure 3001-5 shall be specified as nominal V_{OL} and V_{OH} respectively. The driving signal shall be measured at the input terminal of the device under test.

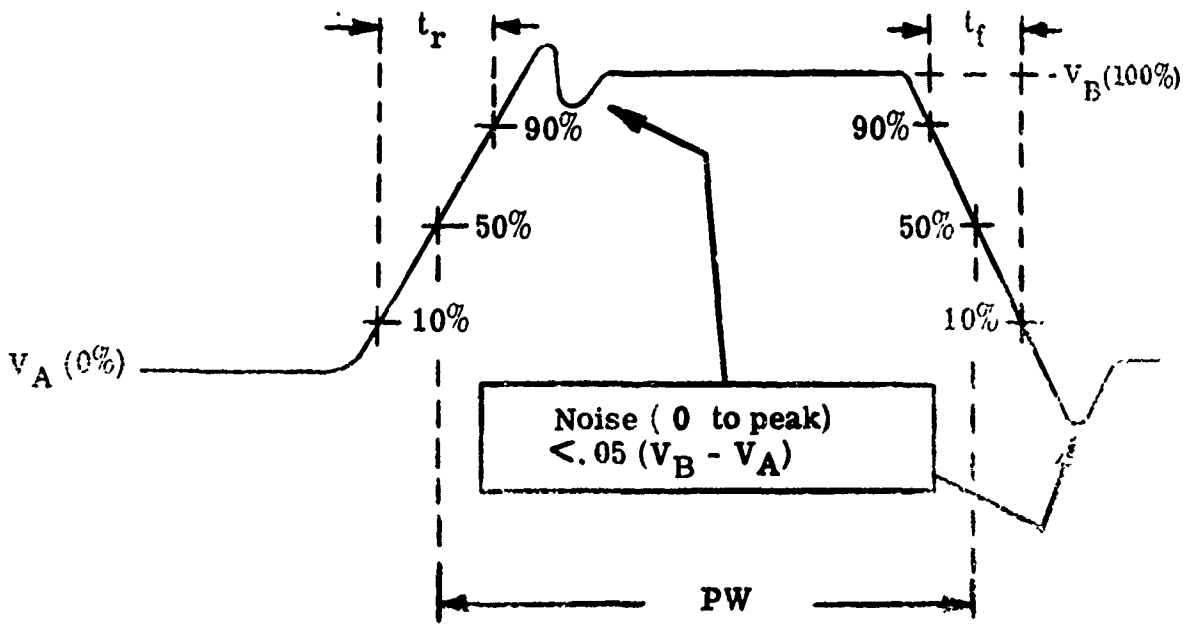
4. Summary. The following details, when applicable, shall be specified in the applicable procurement document:

(a) Levels V_A and V_B.
(b) Driving signal transition times.
(c) Repetition frequency.
(d) Duty factors.
(e) Specific pulse generator required.



Nominal Driving Signal Parameters		
Repetition Frequency	=	100 K Hz ±10%
Pulse Width	=	1 μ sec
V_A	=	OV
V_B	=	4V
$t_r = t_f$	=	10 n sec

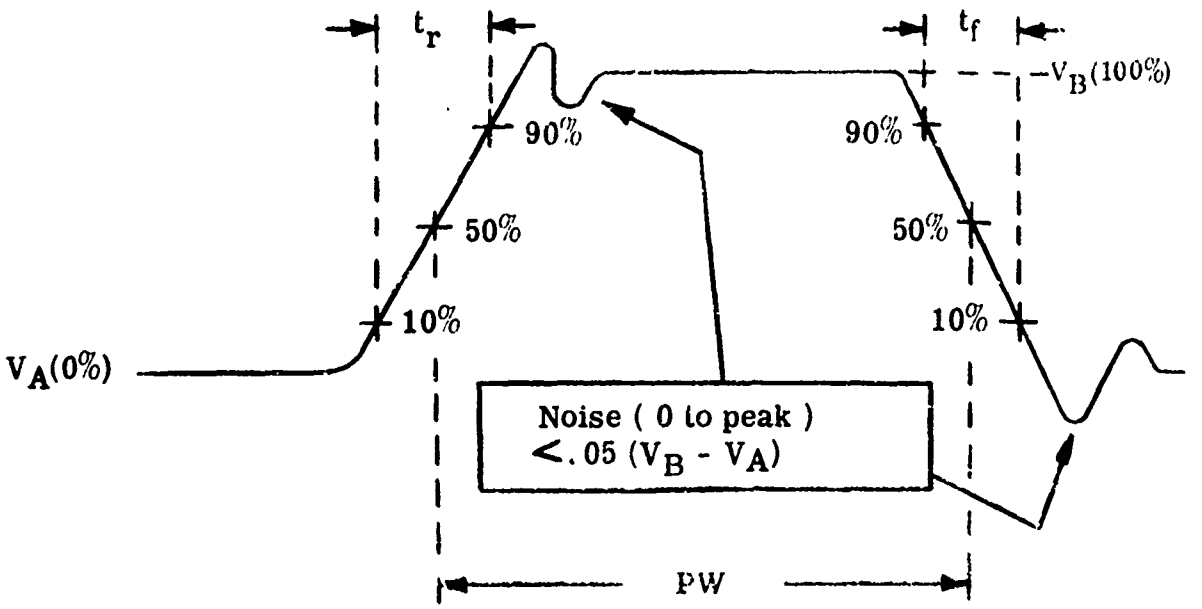
Figure 3001-1 Drive Signal for TTL, DTL



Nominal Driving Signal Parameters		
Repetition Frequency	=	1 M Hz ±10%
Pulse Width	=	100 n sec
V_A	=	-1.65 V*
V_B	=	-0.75 V*
$t_r = t_f$	=	2 n sec

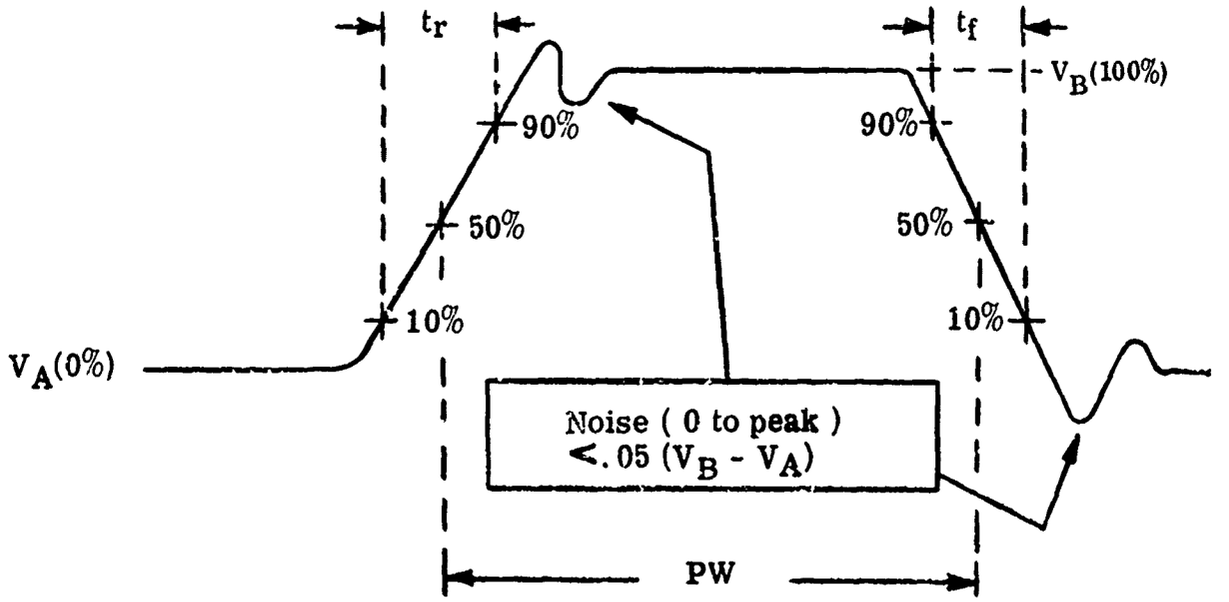
* These voltage level values are generally used with the V_{CC} terminal of the device under test connected to 0 V.

Figure 3001-2 Drive Signal for ECL



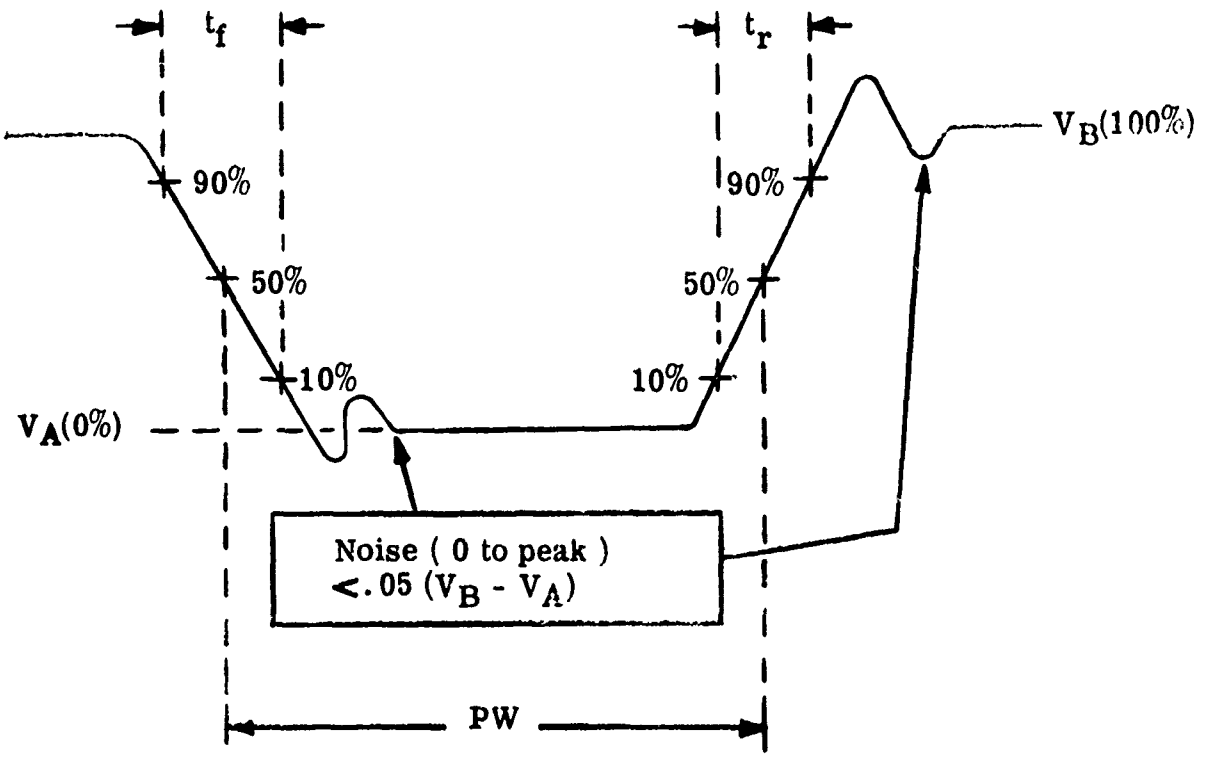
Nominal Driving Signal Parameters		
Repetition Frequency	=	100 K Hz : 10%
Pulse Width	=	1 μ sec
V_A	=	OV
V_B	=	1V
$t_r = t_f$	=	10 n sec

Figure 3001-3 Drive Signal for RTL



Nominal Driving Signal Parameters		
Repetition Frequency	=	10 K Hz ±10%
Pulse Width	=	10 μ sec
V_A	=	OV
V_B	=	10V
$t_r = t_f$	=	20 n sec

Figure 3001-4 Driving Signal for C-MOS, MOS (N-Channel)



Nominal Driving Signal Parameters		
Repetition Frequency	=	10 K Hz ±10%
Pulse Width	=	10 μ sec
V_A	=	-20 V
V_B	=	OV
$t_r = t_f$	=	20 n sec

Figure 3001-5 Driving Source for MOS (P-Channel)

METHOD 3002
LOAD CONDITIONS

1. Purpose. This method establishes the load conditions to be used in measuring dynamic performance of logic gating and flip flop circuits, such as TTL, DTL, RTL, ECTL and MOS.

2. Apparatus. The load for static tests shall simulate the worst case conditions for the circuit parameters being tested. The load for dynamic tests shall simulate nominal conditions for the parameters being tested. These loads shall be specified in the applicable procurement document.

2.1 Discrete component load. The load will consist of any combination of capacitive, inductive, resistive, or diode components.

2.1.1 Capacitive Load (C_L). The total load capacitance of the circuit under test shall include probe and test fixture capacitance and a compensating capacitor as required. The value of the capacitance, measured at 1 MHz ±10%, shall be specified in the applicable procurement document.

2.1.2 Inductive Load (L_L). The total load inductance of the circuit under test shall include probe and test fixture inductance and a compensating inductor as required. The value of the inductance, measured at 1 MHz ±10%, shall be specified in the applicable procurement document.

2.1.3 Resistive Load (R_L). The resistive load shall represent the worst case fan out conditions of the device under test for static tests and nominal fan out conditions for dynamic tests. For sink loads, the resistor shall be connected between the power supply (V_{CC} or V_{DD}) and the circuit output for TTL, DTL, RTL, ECL, C-MOS, and MOS (N-Channel) and between circuit output and ground for MOS (P-Channel). For source loads, the resistor shall be connected between circuit output and ground for TTL, DTL, RTL, ECL, C-MOS, and MOS (N-Channel) and between V_{DD} and circuit output for MOS (P-Channel).

2.1.4 Diode load (D_L). The diode load shall represent the input diode(s) of the circuit under test. The equivalent diode, as specified in the applicable procurement document, will also represent the base-emitter or base-collector diode of any transistor in the circuit path of the normal load.

2.2 Dynamic load change. The load shall automatically change its electrical parameters as the device under test changes logic state if this is the normal situation for the particular family of circuits being tested. One method of accomplishing this dynamic change is to simulate devices from the same logic family equal to the nominal fan out as the load.

3. Procedure. The load will normally be paralleled by a high impedance voltage detection indicator. The indicator may be either visual or memory storage.

4. Summary. The following must be defined in the applicable procurement document:

(a) C_L, L_L, R_L, D_L and equivalent circuit (see 2.1).

METHOD 3003

DELAY MEASUREMENTS

1. Purpose. This method establishes the means for measuring propagation delay of logic gating and flip flop circuits.

1.1 Definitions. The following definitions for the purpose of this test method shall apply.

1.1.1 Propagation delay (t_{pLH}). The time measured with the specified output changing from the defined high level to the defined low level with respect to the corresponding input transition.

1.1.2 Propagation delay (t_{pHL}). The time measured with the specified output changing from the defined low level to the defined high level with respect to the corresponding input transition.

2. Apparatus. Equipment capable of measuring elapsed time between the input signal and output signal at any percentage point or voltage point between the maximum low level and minimum high level shall be provided. The input shall be supplied by a driving source as described in method 3001 of this standard. It is desirable for this equipment to have data logging capability so that circuit dynamic performance distribution can be monitored.

3. Procedure. The test circuit shall be loaded according to method 3002 of this standard. The driving signal to the test circuit shall be provided according to method 3001 of this standard.

3.1 Measurements at a Voltage Point. t_{pLH} and t_{pHL} shall be measured from the threshold voltage point on the driving signal to the threshold voltage point on the test circuit output signal for both inverting and noninverting logic. These delays shall be measured at the input and output terminals of the device under test. The device under test shall be conditioned according to the applicable procurement document with nominal bias voltages applied. Figures 3003-1 and 3003-2 show typical delay measurements.

3.2 Measurements at Percentage Points. t_{pLH} and t_{pHL} shall be measured from a specified percentage point on the driving signal to a specified percentage point on the test circuit output signal for both inverting and noninverting logic. These delays shall be measured at the input and output terminals of the device under test. The device under test shall be conditioned according to the applicable procurement document with nominal bias voltages applied. Figures 3003-1 and 3003-2 show typical delay measurements.

4. Summary. The following details must be specified in the applicable procurement document:

(a) t_{PLH} and t_{PHL} limits.
(b) Parameters of the driving signal, when applicable.
(c) Load conditions.
(d) Conditioning voltages.
(e) Measurement points (see 3.1 and 3.2).
(f) Power supply voltages.

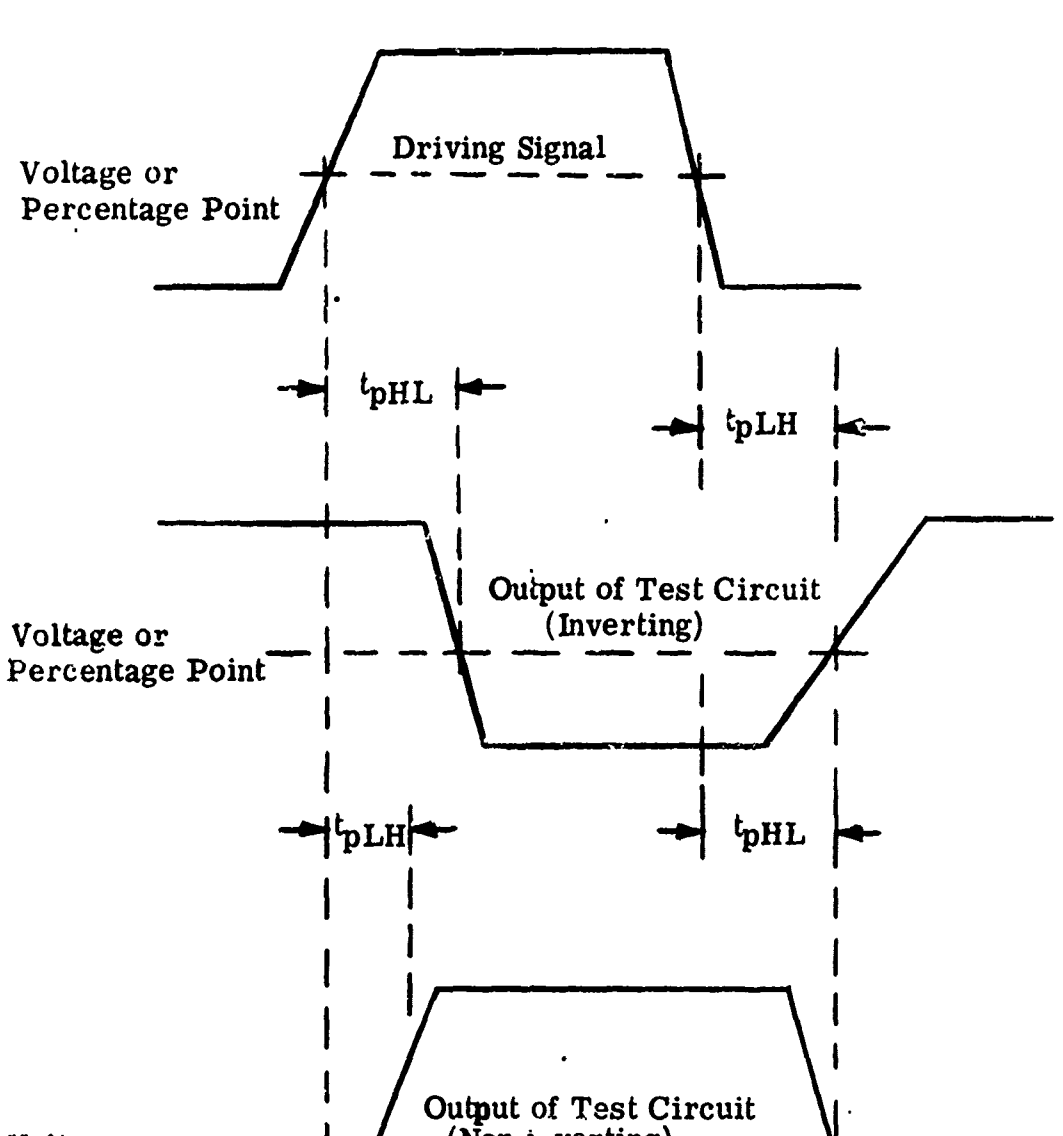


Figure 3003-1 Propagation Delay

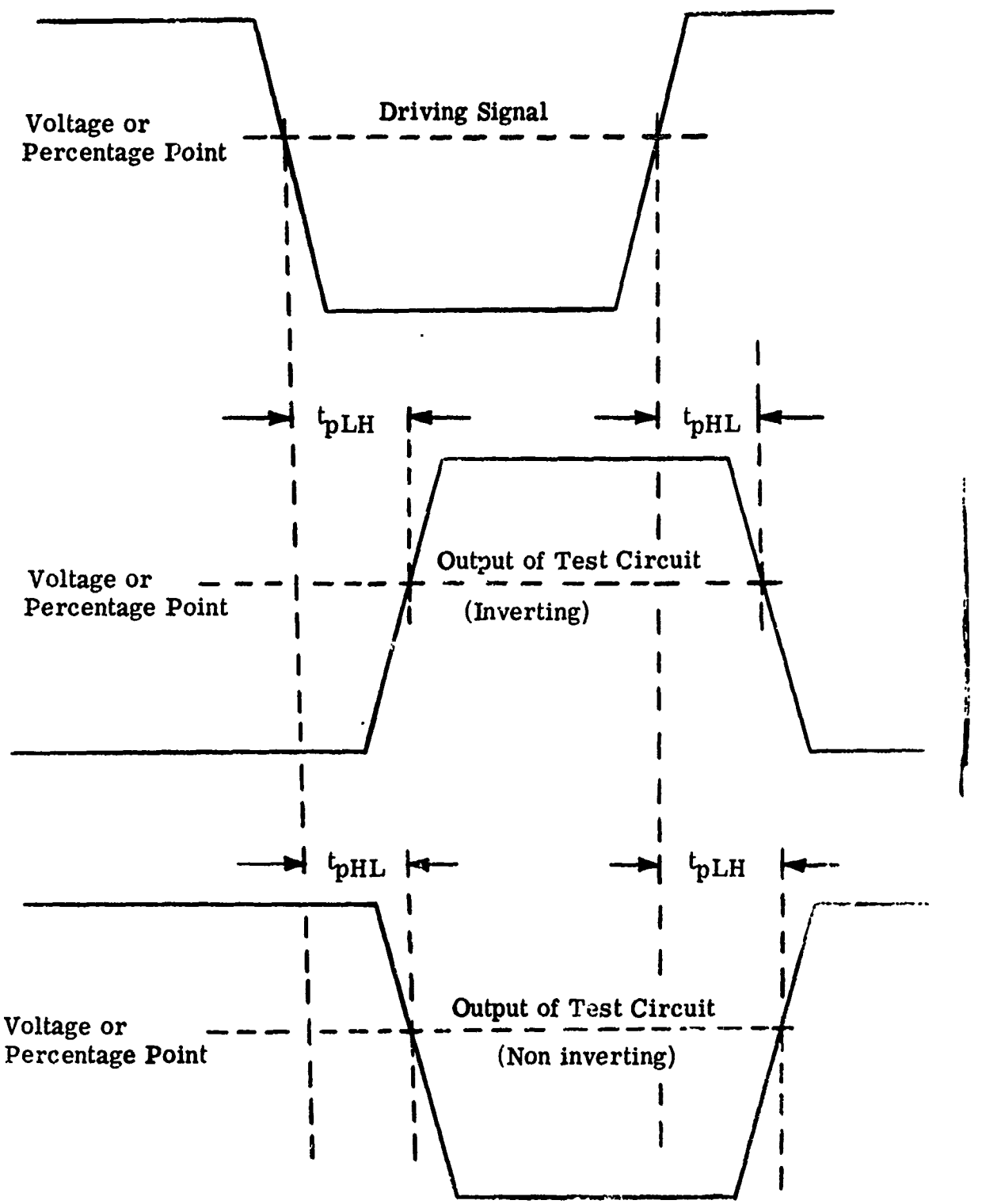


Figure 3003-2 Propagation Delay

METHOD 3004
TRANSITION TIME MEASUREMENTS

1. Purpose. This method establishes the means for measuring the output transition times of logic gating and flip flop circuits.

1.1 Definitions. The following definitions shall apply for the purpose of this method.

1.1.1 Rise time (t_r). The transition time of the output from 10% to 90% or 10% to a specified value of output voltage with the specified output changing from the defined low level to the defined high level.

1.1.2 Fall time (t_f). The transition time of the output from 90% to 10% or 90% to a specified value of output voltage with the specified output changing from the defined high level to the defined low level.

2. Apparatus. Equipment capable of measuring the elapsed time between the 10% to 90% or 10% to a specified voltage on the rise transition and the 90% to 10% or 90% to a specified voltage on the fall transition of the test circuit output shall be provided. It is desirable for this equipment to have data logging capability so that circuit dynamic performance distribution can be monitored.

3. Procedure. The test circuit shall be loaded according to method 3002 of this standard. The driving signal to the test circuit shall be provided according to method 3001 of this standard.

3.1 Measurement of t_r and t_f. The rise transition time (t_r) at the output of the test circuit shall be measured from the 10% points to the 90% points or from the 10% points to a specified voltage point. Fall transition time (t_f) at the outputs of the test circuit shall be measured from the 90% points to the 10% points or from the 90% points to a specified voltage point. These measurements shall be made at the test circuit terminals. The device under test shall be conditioned according to the applicable procurement document and nominal bias voltages applied. Figures 3004-1 and 3004-2 show typical transition time measurements.

4. Summary. The following details must be specified in the applicable procurement document:

(a) t_r limits
(b) t_f limits
(c) Transition time measurement points if other than 10% or 90%
(d) Parameters of the driving signal, when applicable.
(e) Conditioning voltages.
(f) Load condition.
(g) Power supply voltages.

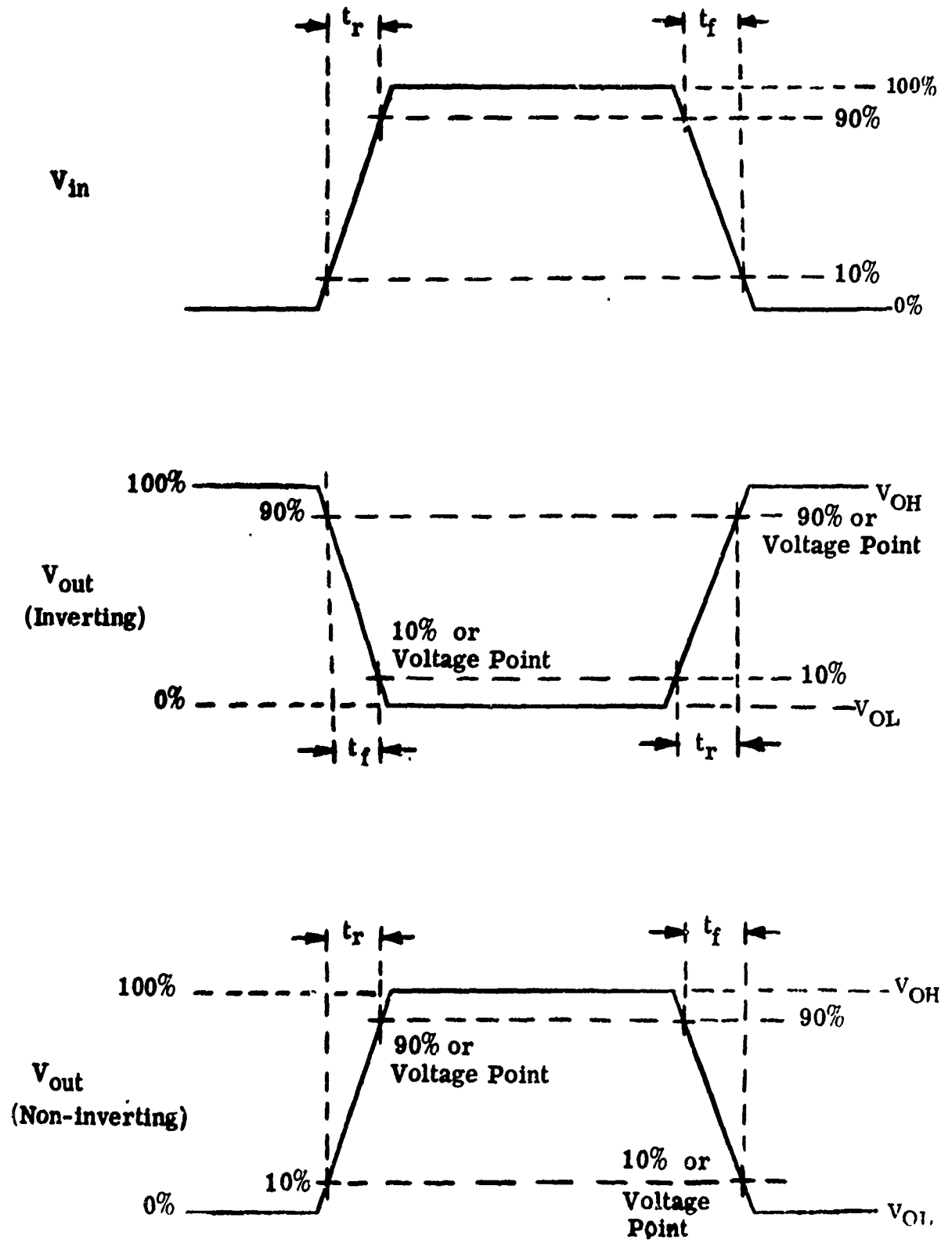


Figure 3004-1 Transition Time Measurements

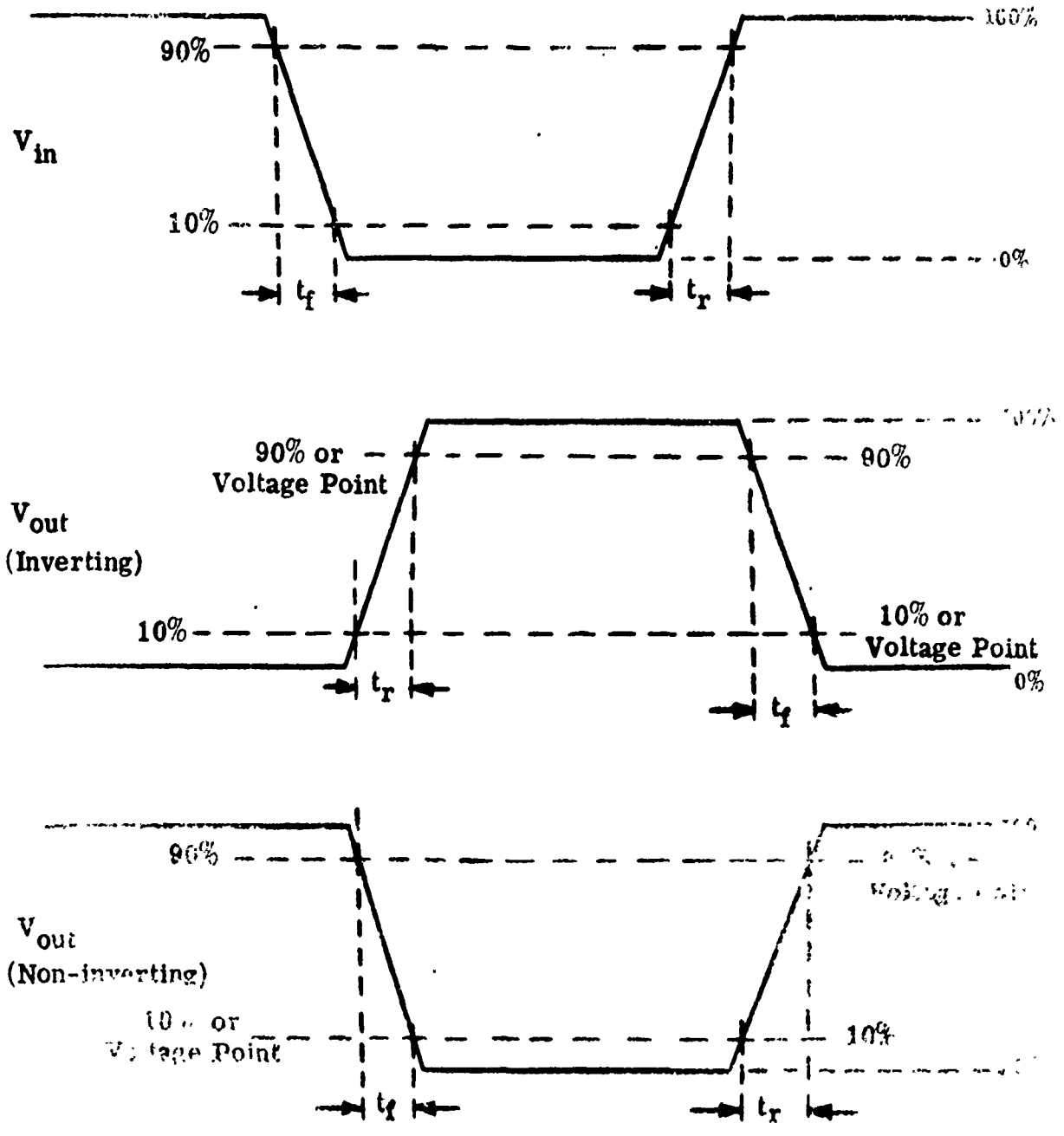


Figure 3004-2 Transition Time Measurements

METHOD 3005

POWER SUPPLY CURRENT

1. Purpose. This method establishes the means for measuring power supply currents of logic gating and flip flop circuits such as TTL, RTL, ECTL, DTL (I_{CC}), and MOS (I_{DD} and I_{GG}).

2. Apparatus. Equipment capable of applying prescribed voltage to the test circuit power supply terminals and measuring the resultant currents flowing in these terminals shall be provided.

3. Procedure.

3.1 I_{CCH} (Logic Gate). Inputs of the device under test shall be conditioned in such a way as to provide an up level at the output, the worst case supply voltage(s) shall be applied and the resultant current flow in the supply terminals measured.

3.2 I_{CCL} (Logic Gate). Inputs of the device under test shall be conditioned in such a way as to provide a down level at the output, the worst case supply voltage(s) shall be applied and the resultant current flow in the supply terminals measured.

3.3 I_{CCQH} (Flip Flop). Inputs of the device under test shall be conditioned in such a way as to provide an up level at the Q output; the worst case voltage(s) shall be applied and the resultant current flow in the supply terminals measured.

3.4 $I_{CC\overline{Q}H}$ (Flip Flop). Inputs of the device under test shall be conditioned in such a way as to provide an up level at the $\overline{Q}$ output; the worst case voltage(s) shall be applied and the resultant current flow in the supply terminals measured.

3.5 I_{DD} (MOS Logic Gate). Inputs of the device under test shall be conditioned in such a way as to provide an up level at the output of MOS (P-Channel and C-MOS) or a down level at the output of MOS (N-Channel and C-MOS), worst case voltage(s) shall be applied and the resultant current flow in the supply terminals measured.

3.6 I_{GG} (MOS P-Channel and N-Channel Logic Gates). Inputs of the device under test shall be conditioned in such a way as to provide an up level at the output of MOS (P-Channel) or a down level at the output of MOS (N-Channel); worst case voltage(s) shall be applied and the resultant current flow in the supply terminals measure.

3.7 I_{DDQL} (MOS Flip Flop). Inputs of the device under test shall be conditioned in such a way as to provide a down level at the Q output; worst case voltage(s) shall be applied and the resultant current flow in the supply terminals measured.

3.8 $I_{DD\bar{Q}L}$ (MOS Flip Flop). Inputs of the device under test shall be conditioned in such a way as to provide a down level at the $\bar{Q}$ output; worst case voltage(s) shall be applied and the resultant current flow in the supply terminals measured.

3.9 I_{GGQL} (MOS (N-Channel and P-Channel) Flip Flop). Inputs of the device under test shall be conditioned in such a way as to provide a down level at the Q output; worst case voltage(s) shall be applied and the resultant leakage current flow in the supply terminals measured.

3.10 $I_{GG\bar{Q}L}$ (MOS (P-Channel and N-Channel) Flip Flop). Inputs of the device under test shall be conditioned in such a way as to provide a down level at the $\bar{Q}$ output; worst case voltage(s) shall be applied and the resultant leakage current flow in the supply terminals measured.

3.11 I_{DD} Dynamic (C-MOS Logic Gating and Flip Flop Circuits). The driving signal to the test circuit shall be provided according to method 3001 of this standard; the worst case voltage(s) shall be applied and the resultant current flow in the supply terminals measure.

4. Summary. The following details must be specified in the applicable procurement document:

(a) Test temperature.
(b) Power supply voltages.
(c) I_{CCH}, I_{CCL}, I_{DD}, and I_{GG} limits.
(d) Conditioning of inputs.

METHOD 3006

HIGH LEVEL OUTPUT VOLTAGE

1. Purpose. This method establishes the means for assuring circuit performance to the limits specified in the applicable procurement document in regard to high level output drive, which may be specified as a minimum value V_{OH} min or as a maximum V_{OH} max. This method applies to TTL, DTL, RTL, ECTL, and MOS logic gating and flip flop circuits.

2. Apparatus. An instrument shall be provided that has the capability of forcing current from the output terminal for TTL, DTL, RTL, ECTL, MOS (N-Channel) and C-MOS and forcing current into the output terminal for MOS (P-Channel) of the test circuit and measuring the resultant output voltage. Magnitude and tolerance of this current shall be defined in the applicable procurement document.

3. Procedure. Worst case power supply voltages and worst case input levels including guaranteed noise margins shall be applied to the test circuit to provide an up level. Forcing current, equal to the circuit worst case high level fan out, shall then be applied to the test circuit output terminal and the resultant output voltage measured. For an inverting gate, every input shall have the maximum low level voltage applied individually with the output measurement being made after each input is conditioned.

4. Summary. The following details must be specified in the applicable procurement document:

(a) Test temperature.
(b) Current to be forced from or into output terminal.
(c) Power supply voltage.
(d) Input levels.
(e) V_{OH} min or V_{OH} max limits.

METHOD 3007

LOW LEVEL OUTPUT VOLTAGE

1. Purpose. This method establishes the means for assuring circuit performance to the limits specified in the applicable procurement document with regard to low level output drive which is specified as a maximum value ($V_{OL\ max}$) or a minimum value ($V_{OL\ min}$). This method applies to TTL, DTL, ECTL, RTL, and MOS logic gating and flip flop circuits.

2. Apparatus. An instrument shall be provided that has the capability of forcing current into the output terminals for TTL, DTL, MOS (N-Channel) and C-MOS and forcing current from the output for RTL, ECTL and MOS (P-Channel) of the test circuit and measuring the resultant output voltage. Magnitude and tolerance of this current shall be defined in the applicable procurement document.

3. Procedure. Worst case power supply voltages and worst case input levels including guaranteed noise margins shall be applied to the test circuit to provide a low level output. Forcing current, equal to the circuit worst case low level fan out, shall be applied to the test circuit output and the resultant output voltage measured. For a non-inverting gate, every input shall have the minimum high level voltage applied individually with the output measurement being made after each input is conditioned.

4. Summary. The following details must be specified in the applicable procurement document:

(a) Test temperature
(b) Current to be forced into or from the output terminal.
(c) Power supply voltages.
(d) Input levels and noise margins.
(e) $V_{OL\ max}$ or $V_{OL\ min}$ limits.

METHOD 3008

BREAKDOWN VOLTAGE, INPUT OR OUTPUT

1. Purpose. This method establishes the means for assuring device performance to the limits specified in the applicable procurement document in regard to input and output breakdown voltage symbolized as (BV_{IN}) and (BV_{OUT}), respectively. These tests shall be the first tests performed on any device.

2. Apparatus

2.1 Method A. This test is generally performed to assure that breakdown does not occur on a device. An instrument shall be provided that has the capability of forcing a specified voltage at the input or output terminal of the test circuit and measuring the resultant current flowing in that terminal. The test instrument shall also have the capability of applying voltage levels to all other terminals. Care should be taken to assure that the test equipment does not inadvertently apply voltage to the device under test that will exceed the maximum rating of each terminal and that the current from the test equipment is sufficiently limited so that the device is not destroyed. This method can also be used to test the ability of power supply terminals to withstand a voltage overload.

2.2 Method B. This test is generally performed to assure that breakdown does occur on a device as specified in the applicable procurement document. An instrument shall be provided that has the capability of forcing a specified voltage and source impedance at the input or output terminal of the test circuit and measuring the resultant voltage at that terminal. The test instrument shall also have the capability of applying voltage levels to all other terminals. Care should be taken to assure that the test equipment does not inadvertently apply voltage to the device under test that will exceed the maximum rating of each terminal so that the device is not destroyed.

3. Procedure

3.1 Method A. All terminals, with the exception of the test terminal, shall be conditioned according to the applicable procurement document. A prescribed voltage shall be applied to the designated input or output terminal and the resultant current measured. When testing for breakdown, all input and output terminals shall be tested individually. At the conclusion of the test, the device shall be functional.

3.2 Method B. All terminals, with the exception of the test terminal, shall be conditioned according to the applicable procurement document. A prescribed voltage with a prescribed series source impedance shall be applied to the designated input or output terminal and the voltage at that terminal measured. At the conclusion of the test, the device shall be functional.

4. Summary. The following details must be specified in the applicable procurement document:

(a) Test temperature.
(b) BV_{IN} and BV_{OUT}.
(c) Conditioning voltages for all other terminals.
(d) Source impedance (Method B).
(e) Maximum breakdown current limits or minimum breakdown terminal voltage.

METHOD 3009

INPUT CURRENT, LOW LEVEL

1. Purpose. This method establishes the means for assuring circuit performance to the limits specified in the applicable procurement document in regard to low level input load which may be specified as a minimum value ($I_{IL\ min}$) or as a maximum value ($I_{IL\ max}$).

2. Apparatus. An instrument shall be provided that has the capability of applying the worst case down voltage to the input terminal of the test circuit, (and worst case levels on the other inputs) and measuring the resultant current flowing in the input terminal. Magnitude and tolerances of these voltages shall be defined in the applicable procurement document.

3. Procedure. Worst case power supply voltages and worst case input voltages shall be applied to the test circuit and the resultant current flowing in the input terminal shall be measured. All inputs shall be tested individually.

4. Summary. The following details must be specified in the applicable procurement document:

(a) Test temperature.
(b) Power supply voltages.
(c) Input voltages.
(d) Worst case voltages at other input terminals.
(e) $I_{IL\ max}$ or $I_{IL\ min}$.

METHOD 3010

INPUT CURRENT, HIGH LEVEL

1. Purpose. This method establishes the means for assuring circuit performance to the limits specified in the applicable procurement document in regard to high level input load which may be specified as a maximum value ($I_{IH\ max}$) or a minimum value ($I_{IH\ min}$).

2. Apparatus. An instrument shall be provided that has the capability of applying the worst case up voltage to the input terminal of the test circuit, and worst case levels at the other inputs, and measuring the resultant current flowing in the input terminal. Magnitude and tolerance of these voltages shall be defined in the applicable procurement document.

3. Procedure. Worst case power supply voltages and worst case input voltages shall be applied to the test circuit and the resultant current flowing in the input terminal shall be measured. All inputs shall be tested individually.

4. Summary. The following details must be specified in the applicable procurement document:

(a) Test temperature.
(b) Power supply voltages.
(c) Input voltage.
(d) Worst case input voltages at other input terminals.
(e) I_{IH} max.

METHOD 3011

OUTPUT SHORT CIRCUIT CURRENT

1. Purpose. This method establishes the means for assuring circuit performance to the limits specified in the applicable procurement document in regard to output short circuit current (I_{OS}). This method applies to TTL, DTL, ECTL, RTL, and MOS logic gating and flip flop circuits.

2. Apparatus. An instrument will be provided that has the capability of forcing a voltage specified in the applicable procurement document at the output terminal of the device under test and measuring the resultant current flowing in that terminal. The test instrument shall also have the capability of applying specified voltage levels to all other inputs.

3. Procedure. Each output per package shall be tested individually.

3.1 TTL, DTL, ECTL, RTL, MOS (P-Channel and N-Channel). Inputs of the device under test shall be conditioned in such a way as to provide a high level at the output for TTL, DTL, ECTL, RTL, and MOS (N-Channel) and a low level at the output for MOS (P-Channel). The output terminal shall be forced to 0 volt potential and the resultant current flow measured.

3.2 C-MOS I_{OSH}. Inputs of the device under test shall be conditioned in such a way as to provide a high level at the output. The output terminal shall be forced to 0 volt potential and the resultant current flow measured.

3.3 C-MOS I_{OSL}. Inputs of the device under test shall be conditioned in such a way as to provide a low level at the output. The output terminal shall be forced to a voltage potential specified in the procurement document and the resultant current flow measured.

4. Summary. The following details must be specified in the applicable procurement document:

(a) Test temperature.
(b) Input conditioning voltages.
(c) Power supply voltages.
(d) $I_{OS\ max}$ and $I_{OS\ min}$ limits.

METHOD 3012

TERMINAL CAPACITANCE

1. Purpose. This method establishes the means for assuring circuit performance to the limits specified in the applicable procurement document in regard to terminal capacitance. This method applies to all logic gating and flip flop circuits.

2. Apparatus. An instrument will be provided that has the capability of applying a 1 MHz controllable amplitude signal superimposed on a variable plus or minus DC voltage. The instrument will also have the capability of measuring the capacitance of this terminal to within the limits and tolerance specified in the applicable procurement document.

3. Procedure. This test may be performed at room temperature. The capacitance measuring bridge shall be connected between the input or output terminal and the ground terminal of the test circuit. The bridge shall be adjusted for a signal of 1 MHz, 50 MV in amplitude riding a bias level specified in the applicable procurement document. With no device in the test socket the bridge shall then be zeroed. For capacitance values below 20 pf, the device shall be connected directly to the bridge with leads as short as possible to avoid the effects of lead inductance. After inserting the device under test and applying the specified bias conditions, the terminal capacitance shall be measured and compared to the limits listed in the applicable procurement document.

4. Summary. The following details must be specified in the applicable procurement document:

(a) Circuit bias conditions.
(b) Bias level at which measurements are to be made.
(c) Maximum capacitance limits.

METHOD 3013

NOISE MARGIN MEASUREMENTS FOR MICROELECTRONIC LOGIC GATING AND FLIP FLOP CIRCUITS

1. Purpose. This method establishes the means of measuring the DC (steady state) and AC (transient) noise margin of microelectronic logic gating and flip flop circuits or to determine compliance with specified noise margin requirements in the applicable procurement document. It is also intended to provide assurance of interchangeability of devices and to eliminate misunderstanding between manufacturers and users on noise margin test procedures and results. The standardization of particular combinations of test parameters (e.g., pulse width, pulse amplitude, etc.) does not preclude the characterization of devices under test with other variations in these parameters. However, such variations shall, where applicable, be provided as additional conditions of test and shall not serve as a substitute for the requirements established herein.

1.1 Definitions. The following definitions shall apply for the purposes of this test method:

(a) Noise margin. Noise margin is defined as the voltage amplitude of extraneous signal which can be algebraically added to the noise-free worst case "input" level before the output voltage deviates from the allowable logic voltage levels. The term "input" (in quotation marks) is used here to refer to logic input terminals or ground reference terminals.

(b) DC noise margin. DC noise margin is defined as the DC voltage amplitude which can be algebraically added to the noise-free worst case "input" level before the output exceeds the allowable logic voltage levels.

(c) AC noise margin. AC noise margin is defined as the transient or pulse voltage amplitude which can be algebraically added to the noise-free worst case "input" level before the output voltage exceeds the allowable logic voltage levels.

1.2 Symbols. The following symbols shall apply for the purposes of this test method and shall be used in accordance with the definitions provided (see 1.2.1, 1.2.2, and 1.2.3) and depicted in Figures 3013-1, 3013-2, and 3013-3.

1.2.1 Logic levels.

V_{IL} max: The maximum allowed input "low" level in a logic system.

V_{IL} min: The minimum allowed input "low" level in a logic system.

V_{IH} max: The maximum allowed input "high" level in a logic system.

V_{IH} min: The minimum allowed input "high" level in a logic system.

V_{OL} max: The maximum output "low" level specified for a logic gating or flip flop circuit.
V_{OL} max is also the noise-free worst case input "zero" level.

$$V_{OL} \text{ max} \leq V_{IL} \text{ max}$$

V_{OH} min: The minimum output "high" level specified for a logic gating or flip flop circuit.
V_{OH} min is also the noise-free worst case input "high" level.

$$V_{OH} \text{ min} \geq V_{IH} \text{ min}$$

1.2.2 Noise margin levels.

V_{NL}: The "low" level noise margin which can be algebraically added to V_{OL} max before the output level exceeds the allowed logic level.

V_{NH}: The "high" level noise margin which can be algebraically added to V_{OH} min before the output level exceeds the allowed logic level.

V_{NG+}: The positive voltage which can be algebraically added to the ground level before the output exceeds the allowed logic level determined by worst case logic input levels.

V_{NG-}: The negative voltage which can be algebraically added to the ground level before the output exceeds the allowed logic level determined by worst case logic input levels.

V_{NP+}: The positive voltage which can be algebraically added to the noise-free worst case upper power supply voltage before the output exceeds the allowed logic level determined by worst case logic input levels.

V_{NP-}: The negative voltage which can be algebraically added to the noise-free worst case lower power supply voltage before the output exceeds the allowed logic level determined by worst case logic input levels.

1.2.3 Noise pulse widths.

PW_L: The "low" level noise pulse width, measured at the V_{IL} max level.

PW_H: The "high" level noise pulse width, measured at the V_{IH} min level.

2. Apparatus. The apparatus used for noise margin measurements shall include a suitable source generator (see 2.1), load (see 2.2), and voltage detection devices for determining logic state.

2.1 Source generator. The source generator for this test shall be capable of supplying the required AC and DC noise inputs. In the case of pulsed inputs the rise and fall times of the injected noise pulse shall each be maintained to less than 20% of the pulse width measured at the 50% amplitude level. For the purpose of this criteria, the rise and fall times shall be defined as the transition times between the 10% and 90% amplitude levels. The pulse repetition rate shall be sufficiently low that the element under test is at steady-state conditions prior to the application of the noise pulse. For the purpose of this criteria, doubling the repetition rate or duty cycle shall not affect the outcome of the measurement.

2.2 Load. The load for this test shall simulate the circuit parameters of the normal load which would be applied in application of the device under worst-case conditions. The load shall automatically change its electrical parameters as the device under test changes logic state if this is the normal situation for the particular device load. The load shall be paralleled by a high impedance voltage detection device.

3. Procedure. The device shall be connected for operation using a source generator and load as specified (see 2), and measurements shall be made of V_{NL}, V_{NH}, V_{NG}, V_{NP}, PW_L and PW_H following the procedures for both AC noise margin and DC noise margin (see 3.2 through 3.3.3).

3.1 General considerations.

3.1.1 Non-propagation of injected noise. As defined in 1.1, noise margin is the amplitude of extraneous signal which may be added to a noise-free worst case "input" level before the output breaks the allowable logic levels. This definition of noise margin allows the measurement of both DC and AC noise immunity on logic inputs or power supply lines or ground reference lines by detection of either a maximum "low" level or a minimum "high" level at the output terminal. Since the output level never exceeds the allowable logic level under conditions of injected noise, the noise is not considered to propagate through the element under test.

3.1.2 Superposition of simultaneously injected noise. Because the logic levels are restored after one stage, and because the noise margin measurement is performed with all "inactive" inputs at the worst case logic levels, the proper system logic levels are guaranteed in the presence of simultaneous disturbances separated by at least one stage.

3.1.3 Characterization of AC noise margin. Although the purpose of this standard test procedure is to insure interchangeability of elements by a single-point measurement of AC noise margin, the test procedure is well suited to the measurement of AC noise margin as a function of noise pulse width. In particular, for very wide pulse widths, the AC noise margin asymptotes to a value identically equal to the DC noise margin.

3.2 Test procedure for DC noise margin.

3.2.1 Worse case configuration. The measurement of DC noise margin using a particular logic input terminal should correspond to the worst case test configuration in the applicable procurement document. For example, the measurement of "low" level noise margin for a positive-logic inverting NAND gate should be performed under the same worst case test conditions as the DC measurement of $V_{OH\ min}$. If the worst case DC test conditions for $V_{OH\ min}$ are high power supply voltage, all unused logic inputs connected to $V_{OH\ min}$ and output current equal to zero, these conditions should be applied to the corresponding DC noise margin measurement.

3.2.2 "Low" Level noise margin, V_{NL}. The "low" level noise margin test is normally performed during the V_{OH} test for inverting logic and during the V_{OL} test for non-inverting logic. The noise margin is calculated from the following expression:

$$V_{NL} = V_{IL(max)} - V_{OL(max)}$$

3.2.3 "High" Level noise margin, V_{NH}. The "high" level noise margin test is performed during the V_{OL} test for inverting logic and during the V_{OH} test for non-inverting logic. The noise margin is calculated from the following expression:

$$V_{NH} = V_{OH(min)} - V_{IH(min)}$$

3.2.4 Negative ground noise margin, V_{NG-}. With all power supply and output terminals connected to the appropriate worst case conditions, apply $V_{OL(max)}$ to the inputs specified in the applicable module document and decrease the voltage applied to the ground terminal until the output levels equal $V_{IH(min)}$ for inverting logic and $V_{IL(max)}$ for non-inverting logic. The DC ground noise margin is the voltage measured at the device ground terminal. The DC source resistance of the injected ground line voltage shall be negligible.

3.2.5 Positive ground noise margin, V_{NG+}. With all power supply and output terminals connected to the appropriate worst case conditions, apply $V_{OH(min)}$ to the inputs specified in the applicable module document and increase the voltage applied to the ground terminal until the output levels equal $V_{IL(max)}$ for inverting logic and $V_{IH(min)}$ for non-inverting logic. The DC ground noise margin is the voltage measured at the device ground terminal. The DC source resistance of the injected ground line voltage shall be negligible.

3.2.6 Power supply noise margin, V_{NP+} or V_{NP-}. With all input, power supply, and output terminals connected to the appropriate worst case conditions, increase (or decrease) the power supply voltage(s) until the output level equals the appropriate logic level limit. The power supply noise margin is the difference between the measured supply voltage(s) and the appropriate noise-free worst case supply voltage level(s). If more than one power supply is required, the noise margin of each supply should be measured separately.

3.3 Test procedure for AC noise margin.

3.3.1 AC noise margin test point. If, for any combination of noise pulse width or rise and fall times, the AC noise margin is less than the DC noise margin, the noise pulse amplitude, pulse width, and rise or fall time which produce the minimum noise margin shall be used as the conditions for test. If the AC noise margin exceeds the DC noise margin, the DC noise margin tests only shall be performed.

3.3.2 "Low" Level noise margin, PW_L. With all unused logic input, power supply, and output terminals connected to the appropriate worst case conditions, a positive-going noise pulse shall be applied to the input under test. The pulse amplitude shall be equal to V_{OH} min minus V_{OL} max; the pulse shall be superimposed on a DC level equal to V_{OL} max; and the rise and fall times shall be much less than the minimum transition times of the device under test. The test is performed by initially adjusting the input pulse width at the .9 amplitude level to one and one quarter times the rise time. The pulse width is increased until the output voltage is equal to V_{IH} max for inverting logic and equal to V_{IL} min for non-inverting logic. The noise margin pulse width is then measured at the input pulse V_{IL} max level.

3.3.3 "High" Level noise margin, PW_H. With all unused logic input, power supply, and output terminals connected to the appropriate worst case conditions, a negative-going noise pulse shall be applied to the input under test. The pulse amplitude shall be equal to V_{OH} min minus V_{OL} max; the pulse shall be superimposed on a DC level equal to V_{OH} min; and the rise fall times shall be much less than the minimum transition times of the device under test. The test is performed by initially adjusting the input pulse width at the .1 amplitude level to one and one quarter times the rise time. The pulse width is increased until the output voltage is equal to V_{IL} min for inverting logic and V_{IH} max for non-inverting logic. The noise margin pulse width is then measured at the input pulse V_{IH} min level.

4. Summary. The following details, when applicable, shall be specified in the applicable procurement document:

(a) V_{IL} max

(b) V_{IL} min

(c) V_{IH} min

(d) V_{IH} max

(e) V_{OL} max

(f) V_{OH} min

(g) V_{NL}

(h) V_{NH}

(i) V_{NG}

(j) V_{NP}

(k) PW_L

(l) PW_H

(m) Test temperature. Unless otherwise specified DC noise margin measurements shall be made at the rated operating temperature extremes in addition to any other nominal test temperatures.

(n) Specific noise margin measurements and conditions which are to be performed.

(o) Power supply voltages.

(p) Input conditioning voltages.

(q) Output loads

(r) Parameters of noise signal.

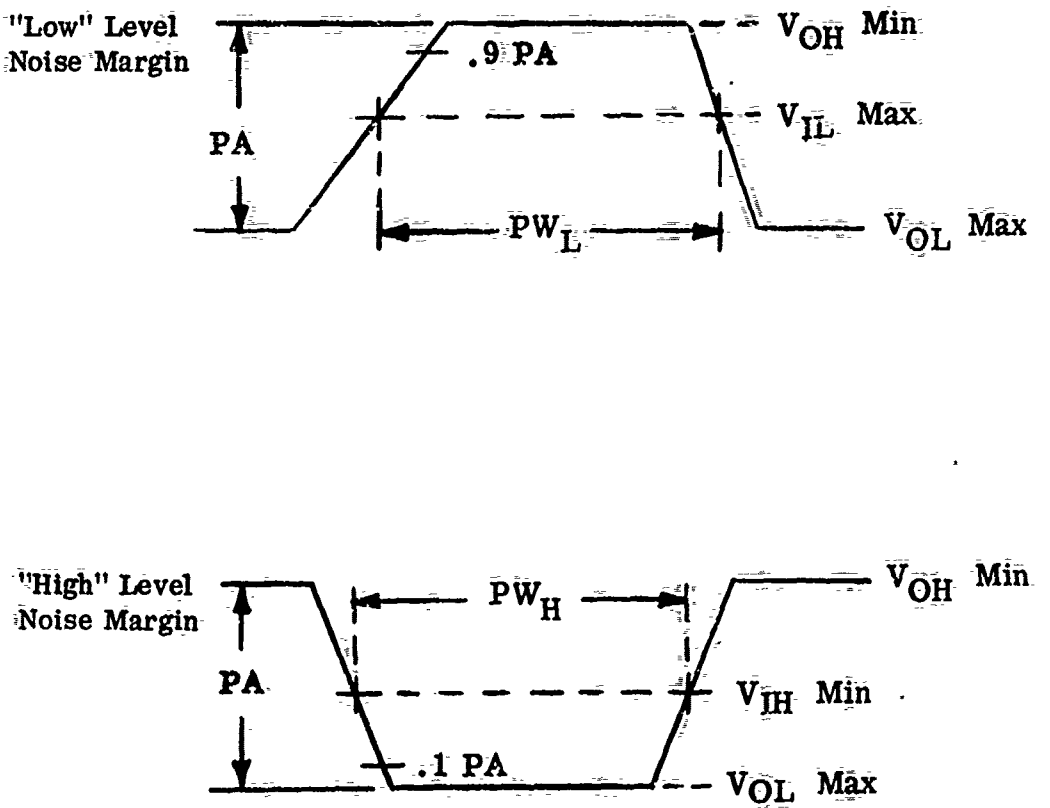


Figure 3013-1 Definitions of Noise Pulse Width

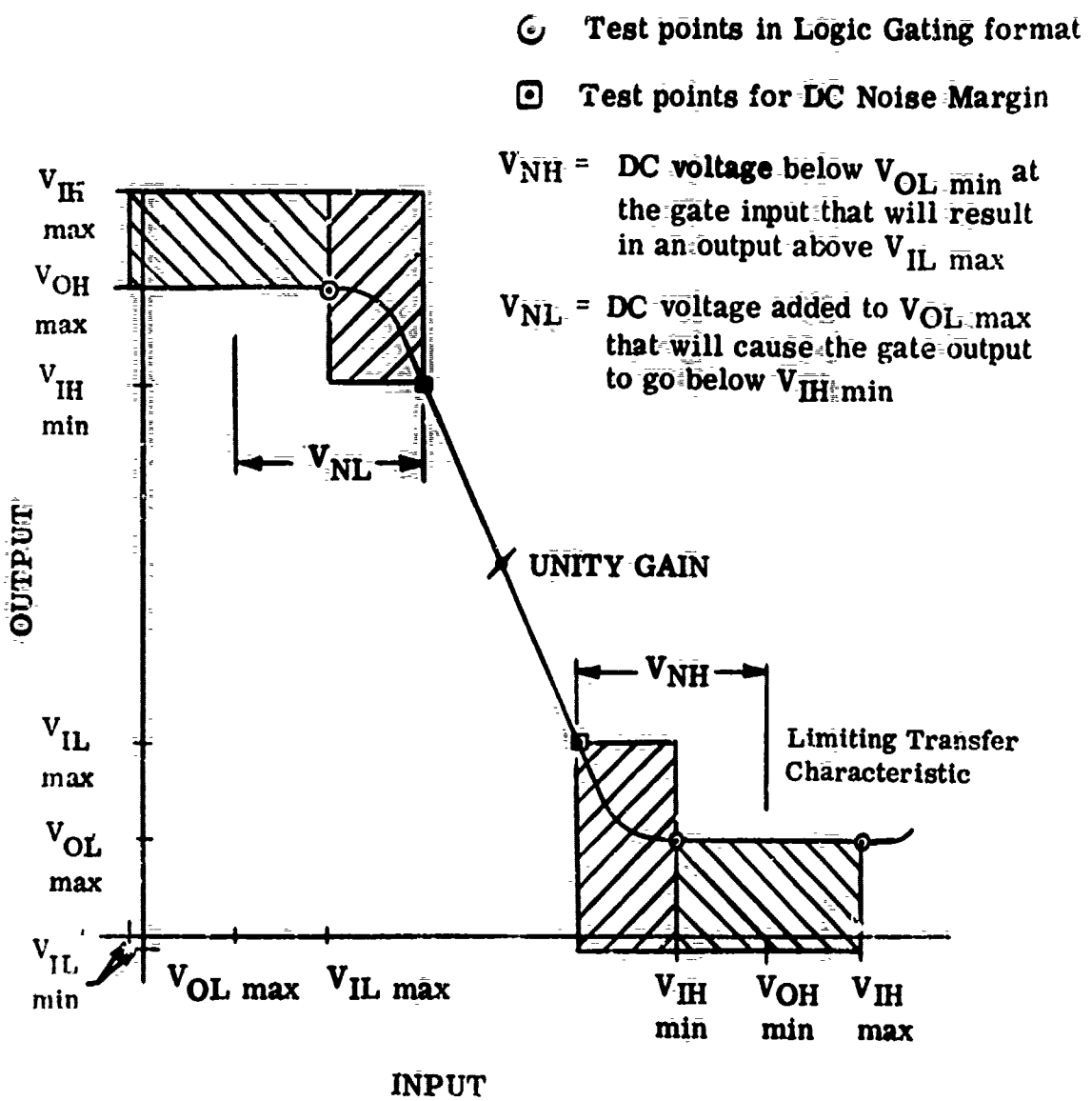


FIGURE 3013-2. Inverting logic gate transfer characteristic defining test points.

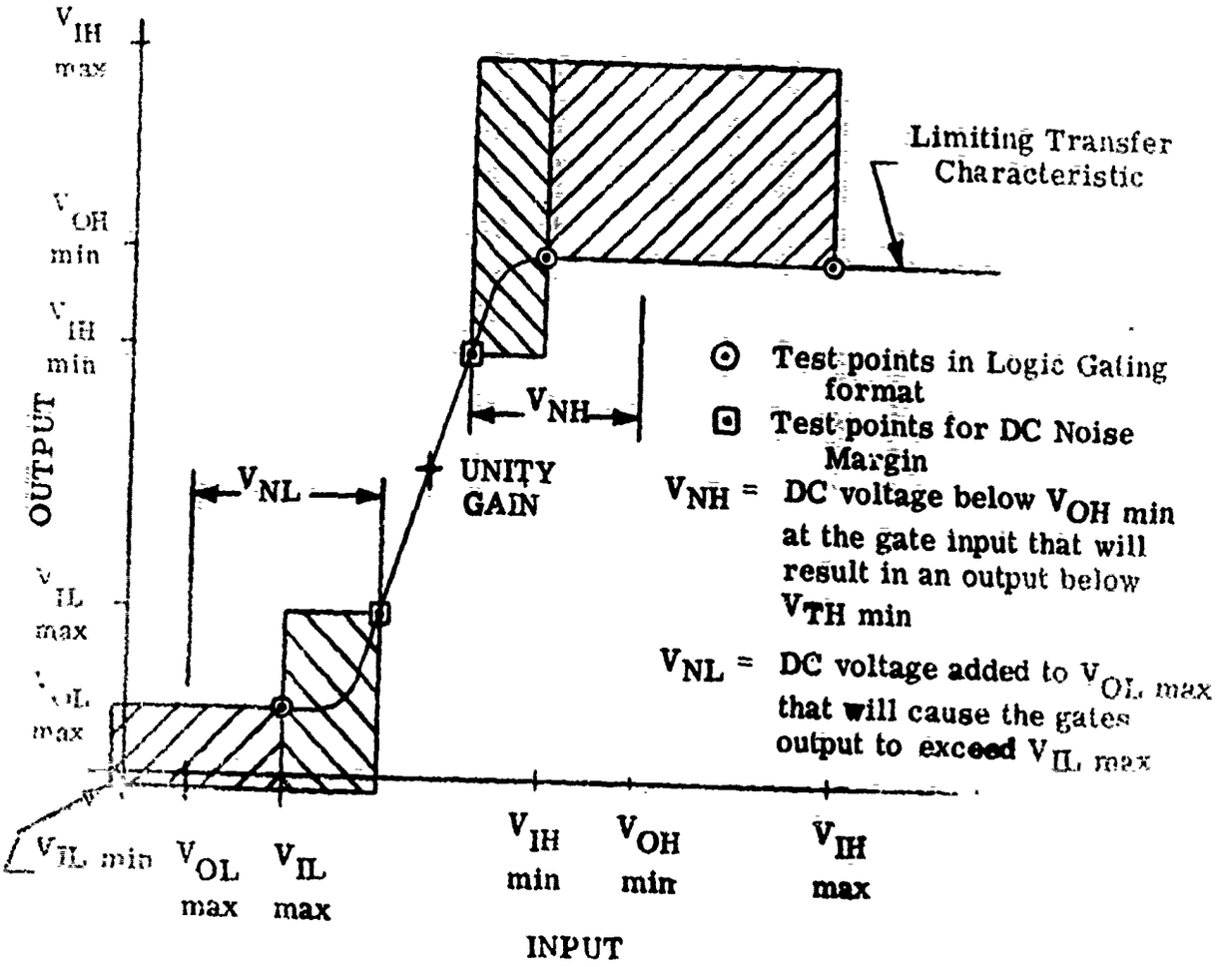


FIGURE 3013-3. Non-inverting logic gate transfer characteristic defining test points.

METHOD 30X1

LOGIC INTEGRITY TESTING

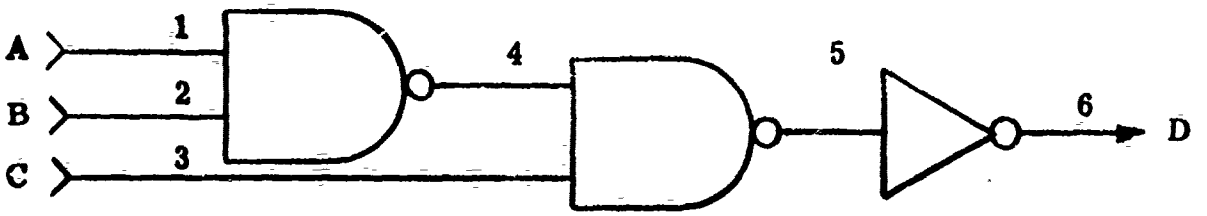
1. Purpose. This method establishes the means for assuring that a complex logic network is exercised to detect any open, stuck high level, or stuck low level conditions on all logic element leads relevant to the network function.

2. Apparatus. An instrument shall be provided that has the capability of applying a sequential logic pattern to the inputs as specified in the applicable procurement document. The test instrument shall also be capable of applying nominal power supply ;es and of monitoring the outputs for the resultant logic pattern.

3. Procedure. The circuit under test shall be stabilized to the test temperature specified in the applicable procurement document. Nominal power supply voltages and the input logic pattern shall then be applied to the test circuit and the output pattern monitored. Figures 30X1-1, 30X1-2 and 30X1-3 illustrate the objective of the logic integrity test. The test sequence may be performed concurrently when performing Method 3006, High Level Output Voltage, and Method 3007, Low Level Output Voltage, of this document.

4. Summary. The following details shall be specified in the applicable procurement document:

(a) Test temperature
(b) Power supply voltages
(c) Input conditioning voltage levels
(d) Input logic patterns (when applicable)
(e) Output logic patterns (when applicable)
(f) Output logic levels (when applicable)
(g) Input logic levels (when applicable)



LOGIC FLOW DIAGRAM

FIGURE 30X1-1

VECTOR	INPUTS			OUTPUTS	FAILURE RESPONSE
	A	B	C	D	D
1	L	H	H	H	L
2	H	L	H	H	L
3	H	H	H	L	H
4	L	H	L	L	H

INPUT VECTORS AND OUTPUT RESPONSE

FIGURE 30X1-2

Vector #	Element Lead	①	①	②	②	③	③	④	④	⑤	⑤	⑥	⑥
	Fault Detected	S1	S0	S1	S0	S1	S0	S1	S0	S1	S0	S1	S0
1		X					X		X	X			X
2				X			X		X	X			X
3			X		X			X			X	X	
4						X					X	X	

S1 - Stuck "1"

S0 - Stuck "0"

TEST VECTOR VS. DETECTED FAULT

FIGURE 30XI-3

METHOD 30X2

FLIP FLOP FUNCTION TESTING

1. Purpose. This method establishes the means for assuring circuit performance to the limits specified in the applicable procurement document in regards to functional operation, i.e. a J-K Flip Flop operates as a J-K Flip Flop.

2. Apparatus. An instrument shall be provided that has the capability of applying a sequential logic pattern to the inputs as specified in the applicable procurement document. The test instrument shall also be capable of applying nominal power supply voltages and of monitoring the outputs for the resultant logic pattern.

3. Procedure. The circuit under test shall be stabilized to the test temperature specified in the applicable procurement document. Nominal power supply voltages and the input logic pattern shall then be applied to the test circuit and the output pattern monitored. Typical input/output patterns are shown in Figure 30X2-1 through 30X2-3. This test sequence may be performed concurrently when performing Method 3006, High Level Output Voltage, and Method 3007, Low Level Output Voltage, of this document.

4. Summary. The following details shall be specified in the applicable procurement document:

(a) Test temperature
(b) Power supply voltages
(c) Input conditioning voltage levels
(d) Input logic pattern (when applicable)
(c) Output logic pattern (when applicable)
(f) Output logic levels (when applicable)

J.K. TRUTH TABLE

t_n		$t_n + 1$
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

Notes: 1. t_n = Bit time before clock pulse.
2. t_{n+1} = Bit time after clock pulse.

FIGURE 30X2-1

D TRUTH TABLE

t_n	$t_n + 1$	
D	Q	$\overline{Q}$
L	L	H
H	H	L

Notes: 1. t_n = Bit time before clock pulse.
2. t_{n+1} = Bit time after clock pulse.

FIGURE 30X2-2

R. S. TRUTH TABLE

t_n		$t_n + 1$
R	S	Q
L	L	Q_n
L	H	H
H	L	L
H	H	Ind.

Notes: 1. t_n = Bit time before clock pulse.
2. $t_n + 1$ = Bit time before clock pulse.
3. Ind. = Indeterminate

FIGURE 30X2-3

MILITARY SPECIFICATION

MICROCIRCUITS LINEAR, DIFFERENTIAL VOLTAGE COMPARATOR, MONOLITHIC SILICON

1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic, silicon voltage comparator. Three product assurance classes and a choice of case outline and lead finish are provided for each type and are reflected in the complete part number.

1.2 Part number. The complete part number shall be as shown in the following example:

M38510	/103	01	B	A	C
Military designator	Detail specification	Device type (1.2.1)	Device class (1.2.2)	Case outline (1.2.3)	Lead finish (3.3.2)

1.2.1 Device type. The device type shall be as shown in the following:

Device type	Circuit
01	Single Differential Voltage Comparator
02	Dual Channel Differential Voltage Comparator
03	Single Voltage Comparator, Buffer

1.2.2 Device class. The device class shall be the product assurance level as defined in MIL-M-38510.

1.2.3 Case outline. The case outline shall be designated as follows:

Case outline A - (1/4" X 1/4" 14 lead flat pack)
Case outline C - (Dual-in-line pack)
Case outline G - (8 lead can)
Case outline H - (1/4" X 1/4", 10 lead flat pack)
Case outline I - (10 lead can)

1.2.4 Absolute maximum ratings.

	Type 01	Type 02	Type 03
Positive Supply Voltage	+14.0V	+14.0V	+15.0V
Negative Supply Voltage	-7.0V	-7.0V	-15.0V
Output Voltage			+24.0V
Output to Negative Supply Voltage			30.0V
Input Voltage Range	±7.0V	±7.0V	±7.0V
Differential Input Voltage	±5.0V	±5.0V	±5.0V
Peak Output Current	10 ma	50 ma	
Sink Current			100 ma
Output Short Circuit Duration	10 sec	10 sec	10 sec
Strobe Voltage		6.0V	6.0V
Storage Temperature Range	-65°C to +150°C		
Junction Temperature	150°C	150°C	150°C
Lead Temperature(soldering, 60 sec)	300°C	300°C	300°C

1.2.5 Recommended operating conditions.

Supply voltage range ----------+Vcc = 12.0Vdc, -Vcc = -6.0Vdc(type 01+02)
Supply voltage range ----------+Vcc = 12.0Vdc, -Vcc = -3.0 to = 12.0Vdc
Operating temperature range----- -55 to +125°C (type 03)

1.2.6 Power and Thermal characteristics.

Case outline	Package	Maximum allowable power dissipation	Maximum θ J-C	Maximum θ J-A
A	14 lead FP	420 mw, Tc = 125°C	60°C/W	210°C/W
C	Dual-in-line	500 mw, Tc = 125°C	50°C/W	150°C/W
G	8 lead can	360 mw, Tc = 125°C	70°C/W	220°C/W
H	10 lead FP	420 mw, Tc = 125°C	60°C/W	220°C/W
I	10 lead can	360 mw, Tc = 125°C	70°C/W	185°C/W

2. APPLICABLE DOCUMENT

2.1 The following document, of the issue in effect on date of invitation for bids or request for proposal, forms a part of this specification to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

(Copies of specifications, standards, drawings, and publications required by suppliers in connection with specific procurement functions should be obtained from the procuring activity or as directed by the contracting officer.)

3. REQUIREMENTS

3.1 Detail specifications. The individual item requirements shall be in accordance with MIL-M-38510, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Circuit disgram and terminal connections. The circuit diagram and terminal connections shall be as specified on figure 5.

3.2.2 Schematic circuit. The schematic circuit shall be as specified on figure 6.

3.3 Lead material and finish.

3.3.1 Lead material. Lead material shall conform to one of the following chemical compositions:

(a) Kovar - MIL-STD-1276, Type K
(b) Alloy 42 -

Nickel - - - - - - - - - - -	41 to 43 percent.
Manganese - - - - - - - - -	0.50 percent, maximum.
Carbon - - - - - - - - - -	0.10 percent, maximum.
Silicon - - - - - - - - - -	0.25 percent, maximum.
Iron - - - - - - - - - - - -	Remainder.

3.3.2 Lead finish.

Finish letter	Lead frame material and coating
A	Kovar or Alloy 42 with hot solder dip
B	Kovar or Alloy 42 with bright tin plate
C	Kovar or Alloy 42 with gold plate

The lead finish shall conform to one of the following, as applicable:

(a) Hot solder dip - Minimum thickness of 300 microinches of solder (SN60 or SN 63) over primary finishes in accordance with (b) or (c) below.
(b) Bright acid tin plate - Thickness between 100 and 400 microinches. Nickel underplating is optional.
(c) Gold plate - In accordance with Type K requirements of MIL-STD-1276, except that the thickness of the nickel undercoating, if used, shall be 100 microinches, maximum.

3.4 Electrical performance characteristics. The following electrical performance characteristics apply over the full operating ambient temperature range of -55°C to 125°C and for supply voltages of +Vcc = 12.0Vdc and -Vcc = -6.0Vdc, unless otherwise specified (see table I).

3.5 Rebonding. Rebonding shall be in accordance with MIL-M-38510. The total number of rebond attempts shall be limited to a maximum of 10 percent of the total number of bonds in the microcircuit. The 10 percent limit on rebonds may be interpreted as the nearest whole number to the 10 percent value. A bond shall be defined as a wire to post or wire to pad bond (i.e., for a 14 lead wire bonded package there are 28 bonds). Bond-offs required to clear the bonder after an unsuccessful first bond attempt need not be considered as rebonds provided they can be identified as bond-offs by being physically off the plated post or if they contain a non-typical number of wedge marks. The initial bond attempt need not be visible. A replacement of one wire bonded at one end or an unsuccessful bond attempt at one end of the wire counts as one rebond; a replacement of a wire bonded at both ends counts as two rebonds. A ball bond on top of a ball bond is not permissible. No more than one rebond attempt shall be permitted at any pad or post and no rebonds shall be made where pad metallization has been lifted.

3.6 Electrical test requirements. Electrical test requirements shall be as specified in table III for the applicable device type and device class. The subgroups of table III and limits of table IV which constitute the minimum electrical test requirements for screening, qualification and quality conformance, by device class are specified in table II.

TABLE II. Electrical test requirements

MIL-STD-883 test requirement	Class A devices	Class B devices	Class C devices
Interim electrical parameters (Pre Burn-In) (Method 5004)	1	1	None
Final electrical test parameters (Method 5004)	1*,2,3,4	1*,2,3,4	1
Group A test requirements (Method 5005)	1,2,3,4, 5,6,7	1,2,3,4, 5,6,7	1,2,3,4,7
Groups B and C end point electrical parameters (Method 5005)	1,2,3 and table IV delta limits	Table IV delta limits and limits	Table IV delta limits and limits
Additional electrical subgroups for Group C periodic inspections	None	None	5,6

* PDA applies to subgroup 1 (see 4.3(h)).

Subgroups 4, 5 and 6 do not apply for Type 03.

3.7 Marking. Marking shall be in accordance with MIL-M-38510 and 1.2. At the option of the manufacturer, the following marking may be omitted from the body of the microcircuit, but shall be retained on the initial container.

(a) Country of origin.
(b) Manufacturer's identification.

4. PRODUCT ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-M-38510 and Method 5005 of MIL-STD-883, except as modified herein.

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified herein for groups A, B, and C inspections (see 4.4.1, 4.4.2, and 4.4.3). After qualification of one or more electrically and structurally similar types with a single lead finish, other lead finishes of the same case outline may be qualified by submitting a single type in the qualified case outline to the group B, subgroup 3 test and the group C, subgroups 1, 3, and 4 tests.

4.3 Screening. Screening shall be in accordance with Method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. The following additional criteria shall apply:

(a) Test samples for the group B bond strength test specified in Method 5005 of MIL-STD-883 may, at the manufacturer's option be randomly selected immediately following the internal visual (precap) inspection and prior to sealing (see 4.4.2(b)).

(b) Temperature cycling (Method 1010 of MIL-STD-883).
(1) Omit seal test as post-test measurement.

(c) Thermal shock (Method 1011 of MIL-STD-883), when substituted for temperature cycling.
(1) Omit seal test as post-test measurement.

(d) Burn-In Test (Method 1015 of MIL-STD-883).

(e) Reverse bias burn-in and interim electrical test in accordance with 3.1.10 of Method 5004 of MIL-STD-883 shall be omitted.

(f) Interim and final electrical test parameters shall be as specified in table II, except interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.

(g) External visual inspection shall not include measurement of case and lead dimensions.

(h) Percent defective allowable (PDA) - The PDA is specified as 5 percent for class A devices and 10 percent for class B devices based on failures from group A, subgroup 4 test after cool-down as final electrical test in accordance with Method 5004 of MIL-STD-883, and with no intervening electrical measurements. If interim electrical parameter tests are performed prior to burn-in, failures resulting from pre burn-in screening may be excluded from the PDA. If interim electrical parameter tests prior to burn-in are omitted, then all screening failures shall be included in the PDA. The verified failures of group A, subgroup 1 after burn-in in that lot shall be used to determine the percent defective for that lot, and the lot shall be accepted or rejected based on the PDA for the applicable device class.

4.4 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-M-38510.

4.4.1 Group A inspection. Group A inspection shall consist of the test subgroups and LTPD values shown in table I of Method 5005 of MIL-STD-883 and as follows:

(a) Subgroups 9, 10, and 11 shall be omitted.
(b) Tests shall be as specified in table II.

4.4.2 Group B inspection. Group B inspection shall consist of the test subgroups and LTPD values shown in table II of Method 5005 of MIL-STD-883 and as follows:

(a) End point electrical parameters shall be as specified in table II.
(b) Bond strength test may be conducted on samples collected prior to sealing (see 4.3(a)).
(c) Operating life test (Metnod 1005 of MIL-STD-883).

4.4.3 Group C inspection. Group C inspection shall consist of the test subgroups and LTPD values shown in table III of Method 5005 of MIL-STD-883 and as follows:

(a) End point electrical parameters shall be as specified in table II.
(b) Lead torsion initial conditioning prior to moisture resistance and salt atmosphere tests may be omitted.
(c) Omit steady-state reverse bias test.

4.5 Methods of examination and test. Methods of examination and test shall be as specified in the appropriate tables. Electrical test circuits as prescribed herein or in the referenced test methods of MIL-STD-883 shall be acceptable. Other test circuits shall require the approval of the qualifying activity.

4.5.1 Voltage and current. All voltages given are referenced to the microcircuit ground terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

4.5.2 Life test cool-down procedure. When devices are measured at 25°C following application of the operating life or burn-in test condition, they shall be cooled to room temperature prior to removal of the bias.

4.6 Inspection of preparation for delivery. Inspection of preparation for delivery shall be in accordance with MIL-M-38510, except that the rough handling test shall not apply.

5. PREPARATION FOR DELIVERY

5.1 Preservation-packaging and packing. Microcircuits shall be prepared for delivery in accordance with MIL-M-38510. Level C requirements shall be used unless otherwise stated in the ordering data.

6. NOTES

6.1 Notes. The notes specified in MIL-M-38510 are applicable to this specification.

6.2 Intended use. Microcircuits conforming to this specification are intended for use for Government microcircuit applications (original equipment) and logistic purposes.

6.3 Ordering data. The contract or order should specify the following:

(a) Complete part number (see 1.2).

(b) Requirements for delivery of one copy of the quality conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.

(c) Requirement for certificate of compliance, if applicable.

(d) Requirements for notification of change of product or process to procuring activity in addition to notification to the qualifying activity, if applicable.

(e) Requirements for packaging and packing, if other than level C of MIL-M-55565.

(f) Requirements for failure analysis (including required test condition of Method 5003), corrective action and reporting of results, if applicable.

(g) Requirements for product assurance options.

(h) Requirements for carriers, special lead lengths or lead forming, if applicable. These requirements shall not affect the part number. Unless otherwise specified, these requirements will not apply to direct purchase by or direct shipment to the Government.

6.4 Abbreviations, symbols, and definitions used herein are defined in MIL-STD-1313 and MIL-STD-1331.

6.6 Substitutability. Microcircuits covered by this specification are substitutable for the following commercial device types:

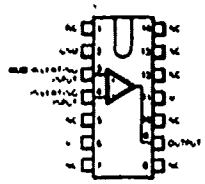
Device type	Commercial type
01	710
02	711
03	106

DEVICE TYPE 01

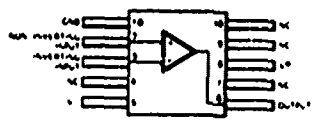
CASE G

NOTE: Pin 4 connected to case.

CASE C

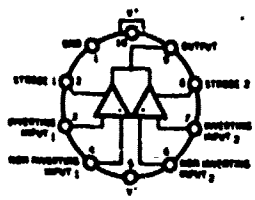


CASE H



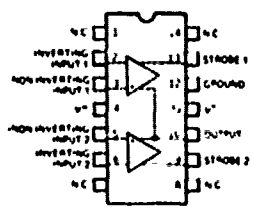
DEVICE TYPE 02

CASE I

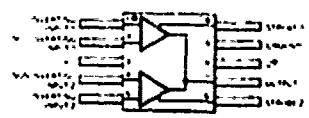


Note: Pin 5 connected to case.

CASE C

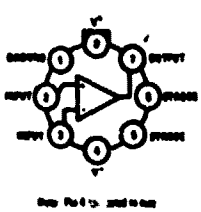


CASE H



DEVICE TYPE 03

CASE G



CASE A

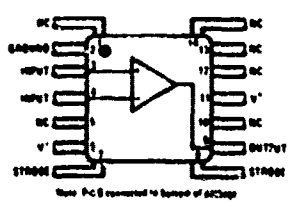
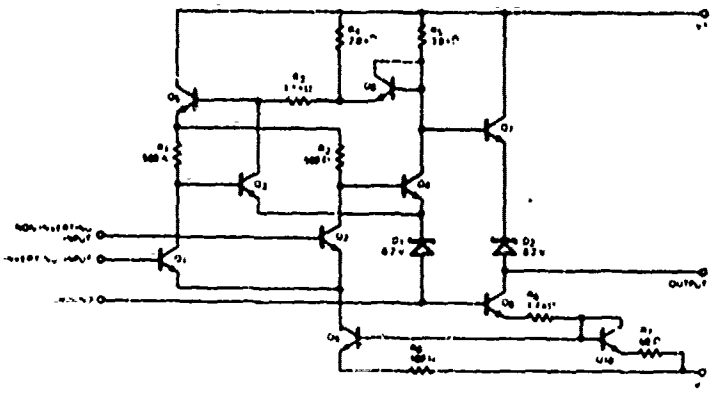
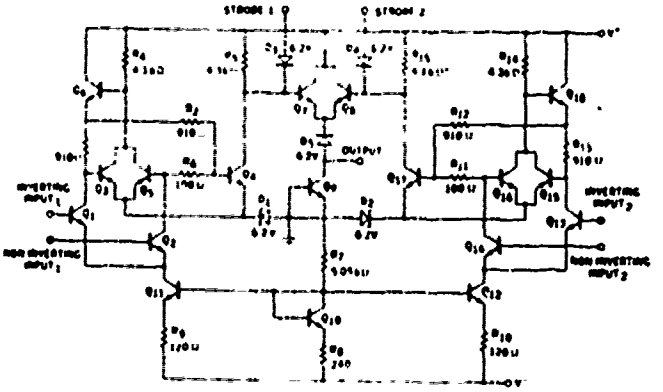


FIGURE 5 TERMINAL CONNECTIONS

DEVICE TYPE 01



DEVICE TYPE 02



DEVICE TYPE 03

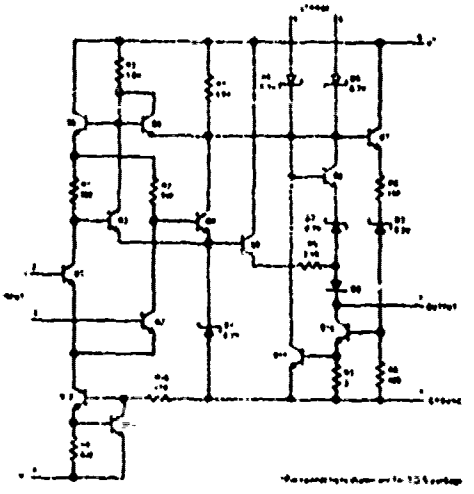
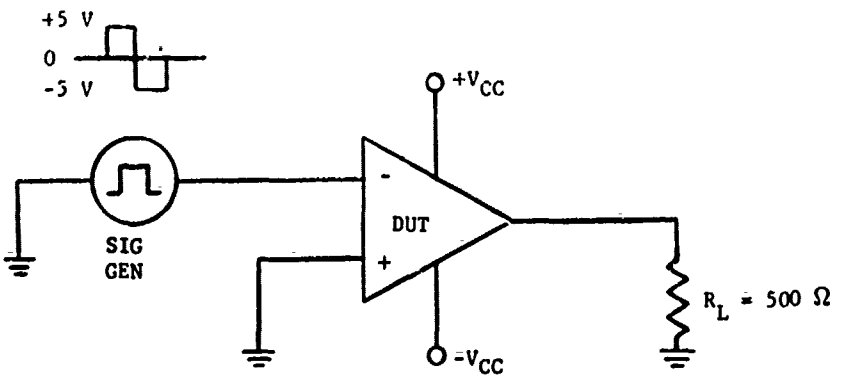
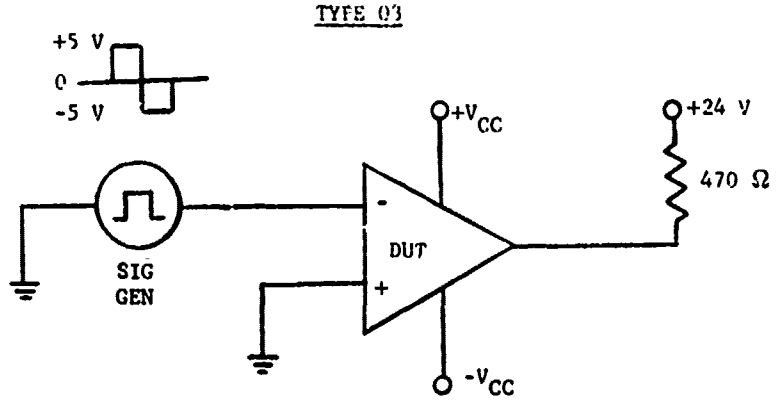


FIGURE 6 SCHEMATIC CIRCUITS

TYPE 01 AND 02



TYPE 03



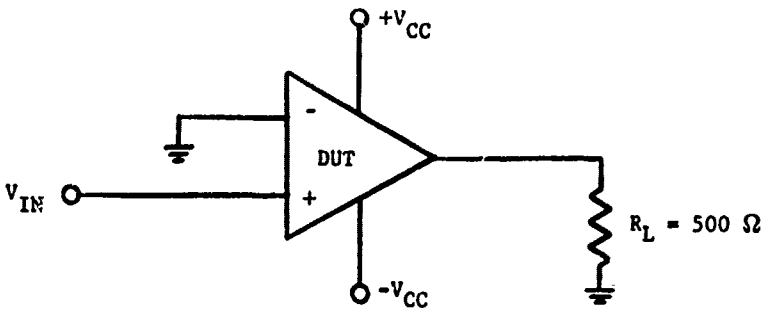
TEST CONDITIONS (T_A = +125°C) +V_{CC} = 12 V, -V_{CC} = -6 V

SIG GEN f = 5 Hz, OUTPUT = 10 V (P-P)

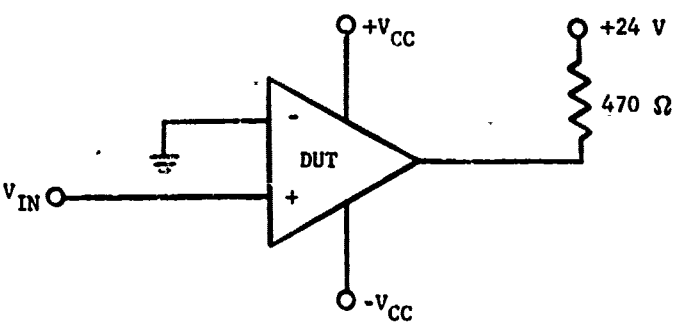
NOTES:
1. ALL RESISTORS ARE 5% TOLERANCE.
2. INPUT APPLIED TO BOTH CHANNELS OF DEVICE TYPE 02, STROBE INPUTS OPEN.
3. FOR DEVICE TYPE 03, STROBE INPUTS OPEN.

FIGURE 7. - TEST CIRCUIT, BURN-IN AND OPERATING LIFE TEST

TYPE 01 AND 02



TYPE 03



TEST CONDITIONS (T_A = +125°C) $+V_{CC}$ = 12 V, $-V_{CC}$ = -6 V

V_{IN} = 5 Vdc (SEE NOTE 1)

NOTES: 1. FOR DEVICE TYPE 02, V_{IN} SHALL BE POSITIVE INTO ONE CHANNEL AND NEGATIVE INTO THE OTHER CHANNEL, STROBE INPUTS OPEN.
2. FOR DEVICE TYPE 03, STROBE INPUTS OPEN. V_{IN} shall be negative.

FIGURE 8. - TEST CIRCUIT, BURN-IN (STEADY STATE POWER AND REVERSE BIAS) AND OPERATING LIFE TEST

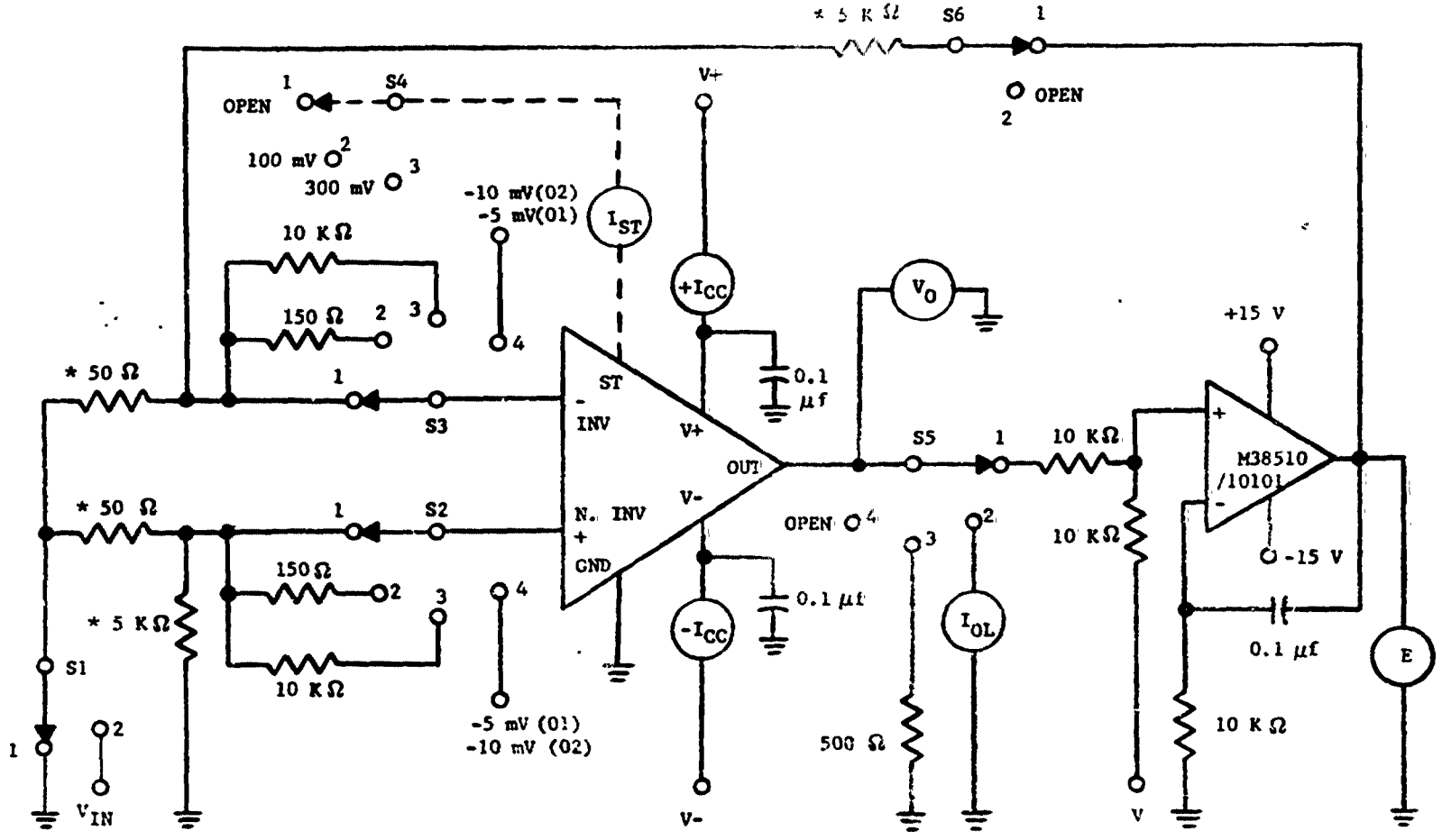


FIGURE 9 - TEST CIRCUIT FOR STATIC AND DYNAMIC TESTS. (Type 01 and 02)

* These are 0.1% resistors matched to 0.01%. All other resistors are 1%, capacitor tolerance is 10%.

Precautions must be taken to prevent damage to the device during insertion into socket and change of switch positions.

FIGURE 9. (Continued) TYPE 01 AND 02

PARAMETER	APPLY (IN VOLTS) $+V_{CC}$	$-V_{CC}$	V_{IN}	V	SWITCH POSITIONS S1	S2	S3	S4	S5	S6	MEASURE VALUE	UNITS	MEASURED PARAMETERS EQUATION	UNITS
V_{IO}(50 Ω)	12	-6	--	SEE TABULATION	1	1	1	1	1	1	E_1	mV	$V_{IO} = \frac{E1}{100}$	mV
V_{IO}(200 Ω)	12	-6	--		1	2	2	1	1	1	E_2	mV	$V_{IO} = \frac{E2}{100}$	mV
I_{IO}	12	-6	--		1	3	3	1	1	1	E_3	mV	$I_{IO} = \frac{E_1 - E_3}{1000}$	μA
$+I_{IB}$	12	-6	--		1	3	1	1	1	1	E_4	mV	$+I_{IB} = \frac{E_1 - E_4}{1000}$	μA
$-I_{IB}$	12	-6	--		1	1	3	1	1	1	E_5	mV	$-I_{IB} = \frac{E_5 - E_1}{1000}$	μA
I_{IB}	CALCULATION												$I_{IB} = \frac{E_5 - E_4}{2000}$	μA
CMRR	12	-7	+5	SEE TAB.	2	2	2	1	1	1	E_6	mV	$CMRR = 20 \log \frac{10 \times 10^5}{E_6 - E_7}$	dB
	12	-7	-5		2	2	2	1	1	1	E_7	mV		
$+I_{CC}$	12	-6	--	--	1	4	1	1	4	2	$+I_{CC}$	mA		
$-I_{CC}$	12	-6	--	--	1	4	1	1	4	2	$-I_{CC}$	mA		
V_{OH} (Loaded)	12	-6	--	--	1	1	4	1	3	2	V_O	V	$V_{OH} = V_O$	V
V_{OH} (Unloaded)	12	-6	--	--	1	1	4	1	4	2	V_O	V	$V_{OH} = V_O$	V
V_{OL}	12	-6	-	--	1	4	1	1	4	2	V_O	V	$V_{OL} = V_O$	V

FIGURE 9. (Continued) TYPE 01 AND 02

PARAMETERS	APPLY (IN VOLTS) $+V_{CC}$	$-V_{CC}$	V_{IN}	V	SWITCH POSITIONS S1	S2	S3	S4	S5	S6	MEASURE VALUE	UNITS	MEASURED PARAMETERS EQUATION	UNITS
V_O (STROBED)	12	-6	--	--	1	1	4	3	4	2	V_O	V	$V_O(\text{STROBED}) = V_O$	V
I_{OL}	12	-6	--	--	1	4	1	1	2	2	I_{OL}	mA		
I_{STROBE}	12	-6	--	--	1	1	4	2	4	2	I_{ST}	mA	$I_{STROBE} = I_{ST}$	mA
A_{V+}	12	-6	--	TABLE III	1	1	1	1	1	1	E_8	mV	$A_{V+} = \frac{500 \times 10^2}{E_1 - E_8}$	mV/mV
A_{V-}	12	-6	--	TABLE III	1	1	1	1	1	1	E_9	mV	$A_{V-} = \frac{500 \times 10^2}{E_1 - E_9}$	mV/mV

VALUES FOR V

T_A	V
+ 25°C	-1.4 VOLTS
- 55°C	-1.8 VOLTS
+ 125°C	-1.0 VOLTS

FIGURE 9 (Continued) CASE CONFIGURATION PIN ASSIGNMENT

	PINS													
CASE	1	2	3	4	5	6	7	8	9	10	11	12	13	14
						TYPE 01								
G	GND	N.INV	INV	V-	NC	NC	OUT	V+	-	-	-	-	-	-
H	GND	N.INV	INV	NC	V-	OUT	NC	V+	NC	NC	-	-	-	-
C	NC	GND	N.INV	INV	NC	V-	NC	NC	OUT	NC	V+	NC	NC	NC
						TYPE 02								
I	GND	ST1	INV1	N.INV1	V-	N.INV2	INV2	ST2	OUT	V+	-	-	-	-
H	INV1	N.INV1	V-	N.INV2	INV2	ST2	OUT	V+	GND	ST1	-	-	-	-
C	NC	INV1	N.INV1	V-	N.INV2	INV2	NC	NC	ST2	OUT	V+	GND	ST1	NC

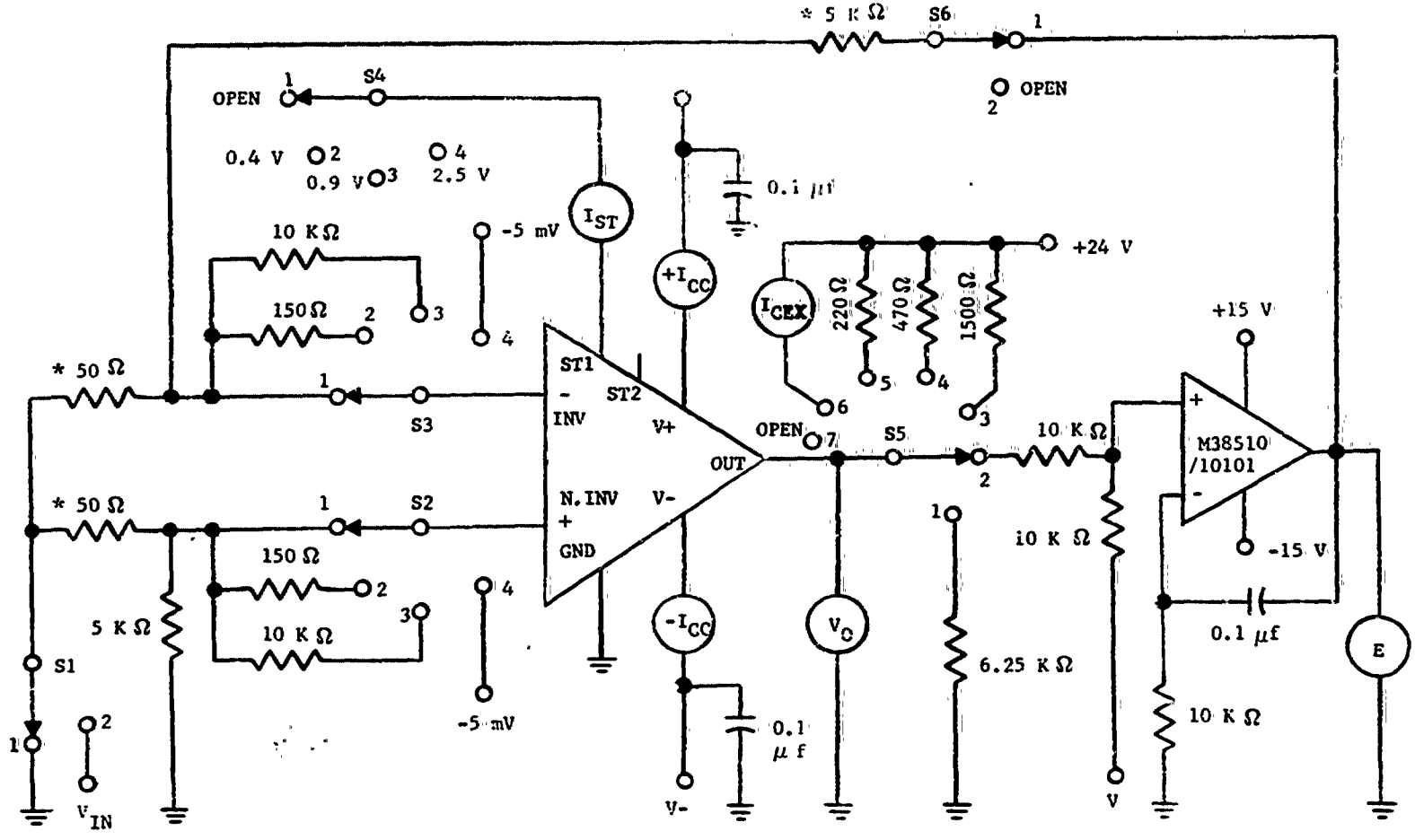


FIGURE 10 - TEST CIRCUIT FOR STATIC AND DYNAMIC TESTS. (Type 03)

* These are 0.1% resistors matched to 0.01%. All other resistors are 1%, capacitor tolerance is 10%.

Precautions must be taken to prevent damage to the device during insertion into socket and change of switch positions.

FIGURE 10. (Continued) TYPE 03

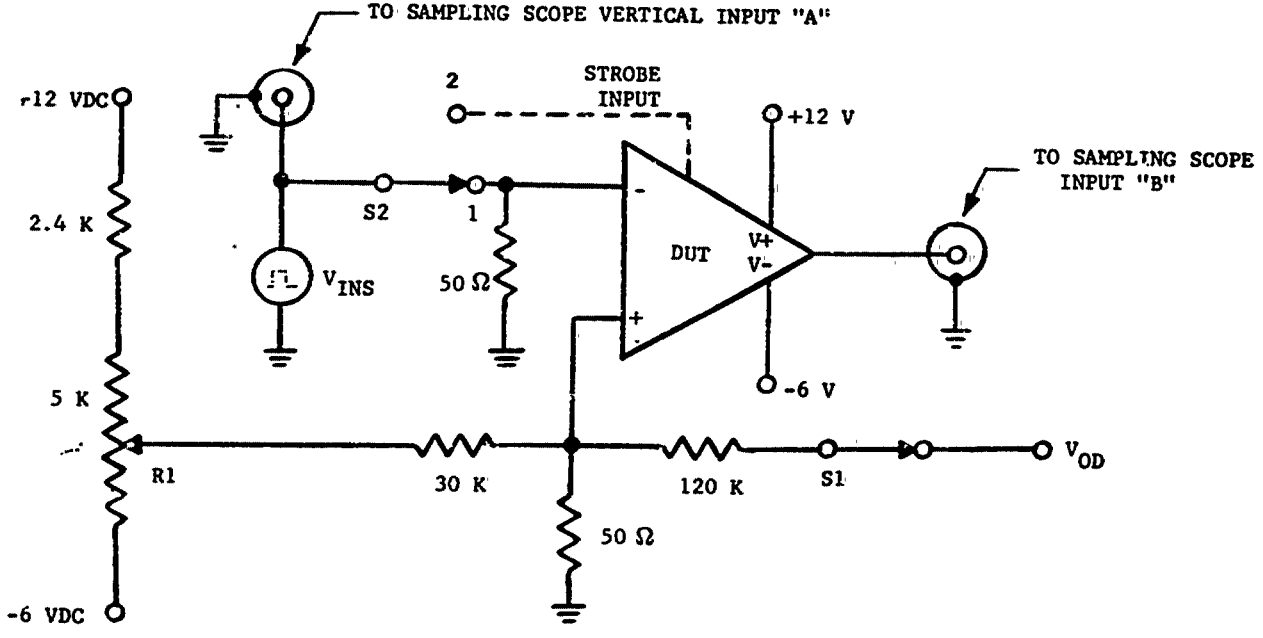
PARAMETER	APPLY (IN VOLTS) $+V_{CC}$	$-V_{CC}$	V_{IN}	V	SWITCH POSITIONS S1	S2	S3	S4	S5	S6	MEASURE VALUE	UNITS	MEASURED PARAMETERS EQUATION	UNITS
$V_{IO}(50\Omega)$	12	-6	--	-1.5	1	1	1	1	2	1	E_1	mV	$V_{IO} = \frac{E1}{100}$	mV
$V_{IO}(200\Omega)$	12	-6	--	-1.5	1	2	2	1	2	1	E_2	mV	$V_{IO} = \frac{E2}{100}$	mV
I_{IO}	12	-6	--	-1.5	1	3	3	1	2	1	E_3	mV	$I_{IO} = \frac{E_1 - E_3}{1000}$	μA
$+I_{IB}$	12	-6	--	-1.5	1	3	1	1	2	1	E_4	mV	$+I_{IB} = \frac{E_1 - E_4}{1000}$	μA
$-I_{IB}$	12	-6	--	-1.5	1	1	3	1	2	1	E_5	mV	$-I_{IB} = \frac{E_5 - E_1}{1000}$	μA
I_{IB}	CALCULATION												$I_{IB} = \frac{E_5 - E_4}{2000}$	μA
CMRR	12	-7	+5	-1.5	2	2	2	1	2	1	E_6	mV	$CMRR = 20 \log \frac{10 \times 10^5}{E_6 - E_7}$	dB
	12	-7	-5	-1.5	2	2	2	1	2	1	E_7	mV		
$+I_{CC}$	12	-6	--	--	1	4	1	1	7	2	$+I_{CC}$	mA		
$-I_{CC}$	12	-6	--	--	1	4	1	1	7	2	$-I_{CC}$	mA		
V_{OH}	12	-6	--	--	1	1	4	1	1	2	V_O	V	$V_{OH} = V_O$	V
$V_{OL}(100mA)$	12	-6	--	--	1	4	1	1	5	2	V_O	V	$V_{OL} = V_O$	V
$V_{OL}(50mA)$	12	-6	--	--	1	4	1	1	4	2	V_O	V	$V_{OL} = V_O$	V
$V_{OL}(16mA)$	12	-6	--	--	1	4	1	1	3	2	V_O	V	$V_{OL} = V_O$	V

FIGURE 10. (Continued) TYPE 03

PARAMETERS	APPLY (IN VOLTS) $+V_{CC}$	$-V_{CC}$	V_{IN}	V	SWITCH POSITIONS S1	S2	S3	S4	S5	S6	MEASURE VALUE	UNITS	MEASURED PARAMETERS EQUATION	UNITS
V_O STROBE LOW	12	-6	--	--	1	4	1	3	7	2	V_O	V		V
V_O STROBE HIGH	12	-6	--	--	1	4	1	4	3	2	V_O	V		V
I_{STROBE}	12	-6	--	--	1	4	1	2	7	2	V_O	V	$I_{ST} = I_{STROBE}$	mA
I_{CEX}	12	-6	--	--	1	1	4	1	6	2	I_{CEX}	μA		

FIGURE 10 (Continued) CASE CONFIGURATION PIN ASSIGNMENT

	PINS													
CASE	1	2	3	4	5	6	7	8	9	10	11	12	13	14
						TYPE 03								
G	GND	NINV	INV	V-	ST1	ST2	OUT	V+	-	-	-	-	-	-
A	NC	GND	N.INV	INV	NC	V-	ST1	ST2	OUT	NC	V+	NC	NC	NC



NOTES:

1. V_{INS} = 100 ns pulse width, 100 K Hz repetition rate, t_r and $t_f \leq 5$ ns.
2. Set up procedure : with S1 open and V_{INS} = 0 adjust R1 for V_{OUT} = 1.5 V. Apply V_{OD} and close S1. Apply V_{INS}.

FIGURE 11. - RESPONSE TIME TEST CIRCUIT AND WAVE FORMS

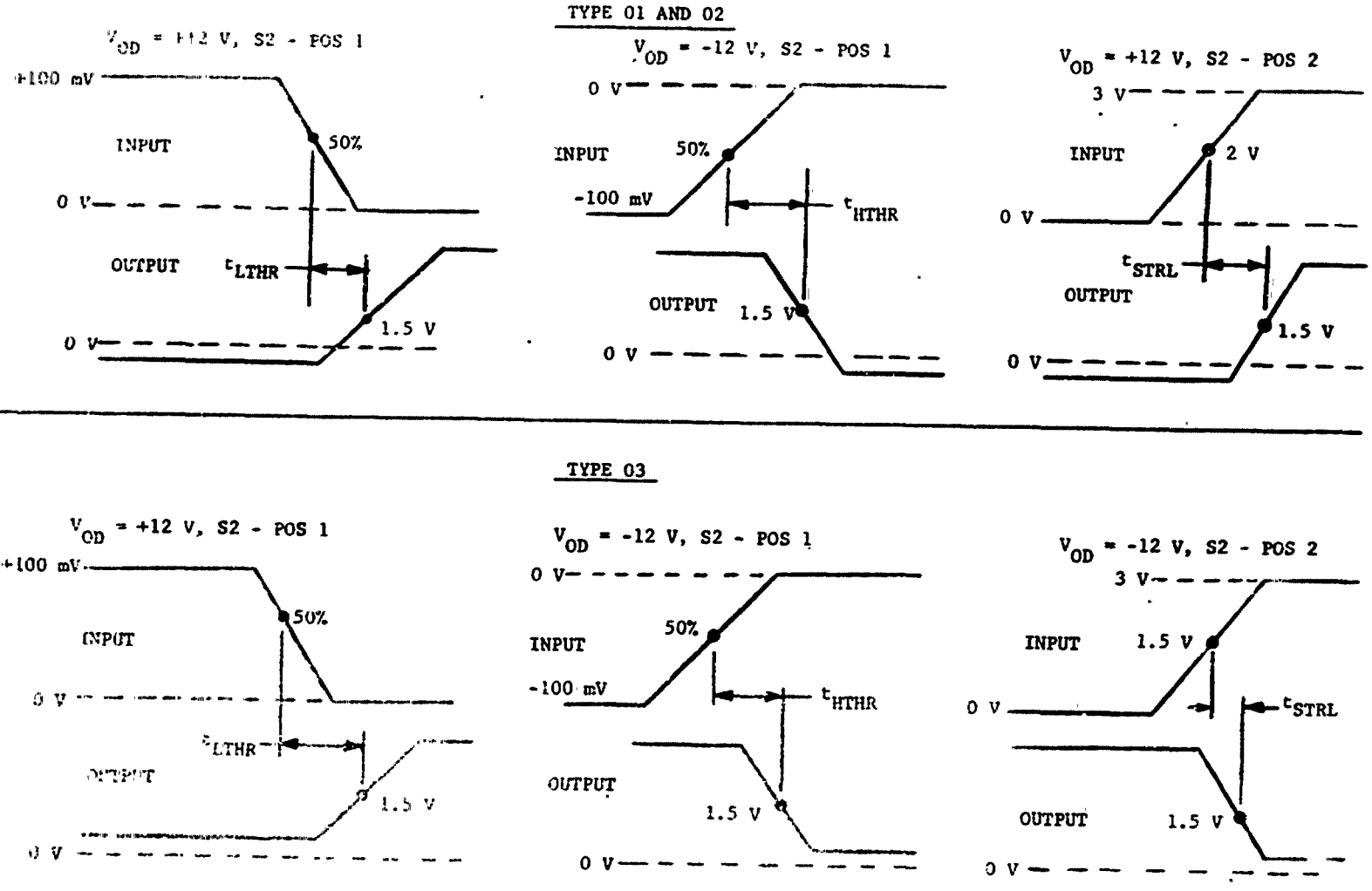


FIGURE 11. - RESPONSE TIME TEST CIRCUIT AND WAVE FORMS

Table I. Electrical Performance Characteristics Type 01 and 02

Characteristic	Symbol	Conditions			Limits Min	Limits Max	Unit
Input Offset Voltage	V_{IO}	$R_S = 200\ \Omega$	$V_{OUT} = 1.4V$, $T_A = +25°C$	TYPE 01		2	mv
				TYPE 02		3.5	mv
			$V_{OUT} = 1.8V$, $T_A = -55°C$	TYPE 01		3	mv
				TYPE 02		4.5	mv
			$V_{OUT} = 1.0V$, $T_A = +125°C$	TYPE 01		3	mv
				TYPE 02		4.5	mv
Input Offset Voltage Temperature Coefficient	$\frac{\Delta V_{IO}}{\Delta T}$	$R_S = 50\ \Omega$	$+25 \leq T_A \leq +125°C$			10	uV/°C
			$-55°C \leq T_A \leq -25°C$			10	uV/°C
Input Offset Current	I_{IO}		$V_{OUT} = 1.4V$, $T_A = +25°C$	TYPE 01		3	ua
				TYPE 02		10	ua
			$V_{OUT} = 1.8V$, $T_A = -55°C$	TYPE 01		7	ua
				TYPE 02		20	ua
			$V_{OUT} = 1.0V$, $T_A = +125°C$	TYPE 01		3	ua
				TYPE 02		10	ua
Input Offset Current Temperature Coefficient	$\frac{\Delta I_{IO}}{\Delta T}$		$+25°C \leq T_A \leq -125°C$			25	na/°C
			$-55°C \leq T_A \leq -25°C$			75	na/°C

For type 02 strobe on device not being tested is connected to ground strobe on device being tested left open unless otherwise specified.

Table I. Electrical Performance Characteristics Type 01 and 02

Characteristic	Symbol	Conditions		Limits Min	Limits Max	Unit
Input Bias Current	I_{IB}	T_A = -25°C	TYPE 01		20	ua
			TYPE 02		75	ua
		T_A = -55°C	TYPE 01		45	ua
			TYPE 02		150	ua
		T_A = -125°C	TYPE 01		10	ua
			TYPE 02		40	ua
Strobe Current	I_{STROBE}	Type 02 ONLY V_{STROBE} = 100 mv ΔV_{IN} = -10 mv			-2.5	ma
Input Voltage Common Mode Rejection Ratio	C_{MRR}	R_S = 200 Ω, -5V ≤ V_{IN} ≤ +5V V- = -7.0V		80		dB
Positive Output Level	V_{OH}	I_{OH} = 0 ma	ΔV_{IN} = -5 mv, TYPE 01 ΔV_{IN} = -10 mv, TYPE 02		5.0	
		I_{OH} = 5 ma	ΔV_{IN} = -5 mv, TYPE 01 ΔV_{IN} = -10 mv, TYPE 02	2.5	4.0	Volts
Negative Output Level	V_{OL}	I_{OL} = 0 ma	ΔV_{IN} = -5 mv, TYPE 01 ΔV_{IN} = -10 mv, TYPE 02	-1.0	0	Volts

For type 02 strobe on device not being tested is connected to ground strobe on device being tested left open unless otherwise specified.

Table I. Electrical Performance Characteristics Type 01 and 02

Characteristic	Symbol	Conditions			Limits Min	Limits Max	Unit
Strobed Output Level 2/	V_o (Strobed)	TYPE 02 ONLY $V_{STROBE} = 0.3V$, $\Delta V_{IN} = +10$ mv			-1.0	0	Volts
Output Sink Current	I_{OL}	$V_{OL} = 0V$	$T_A = +25°C$	$\Delta V_{IN} = -5$ mv, TYPE 01	2.0		ma
				$\Delta V_{IN} = -10$ mv, TYPE 02	0.5		ma
			$T_A = -55°C$	$\Delta V_{IN} = -5$ mv, TYPE 01	1.0		ma
				$\Delta V_{IN} = -10$ mv, TYPE 02			ma
			$T_A = +125°C$	$\Delta V_{IN} = -5$ mv, TYPE 01	0.5		ma
				$\Delta V_{IN} = -10$ mv, TYPE 02			ma
Positive Supply Current	$+I_{CC}$	$V_{OUT} = 0$		TYPE 01		9.0	ma
				TYPE 02		13.5	ma
Negative Supply Current	$-I_{CC}$			TYPE 01		7.0	ma
				TYPE 02		6.2	ma
Power Dissipation	P_D			TYPE 01		150	mw
				TYPE 02		200	mw
Voltage Gain	$A_V(\pm)$	$\Delta V_{OUT} = \pm 0.5V$ $V_{OUT} =$ 1/	$T_A = +25°C$	TYPE 01	1250		V/V
				TYPE 02	750		V/V
			$-55°C \leq T_A \leq +125°C$	TYPE 01	1000		V/V
				TYPE 02	500		V/V

For type 02 strobe on device not being tested is connected to ground strobe on device being tested left open unless otherwise specified.

1/ V_{OUT} = 1.4 V at +25°C, 1.8 at -55°C, 1.0V at +125°C

2/ The output voltage follows the strobe voltage staying one diode drop below.

Table I. Electrical Performance Characteristics Type 01 and 02

Characteristic	Symbol	Conditions	Limits		Unit
			Min	Max	
Response Time - Output Saturated High Level to Threshold Level	t_{HTHR}	Figure 11 T_A = +25°C 100 mv step, 5 mv overdrive		60	n sec
Response Time - Output Saturated Low Level to Threshold Level	t_{LTHR}	Figure 11 T_A = +25°C 100 mv step, 5 mv overdrive		60	n sec
Strobe Release Time	t_{STRL}	Figure 11 T_A = +25°C TYPE 02 ONLY ΔV_{IN} = +10 mv		15	n sec

For type 02 strobe on device not being tested is connected to ground strobe on device being tested left open unless otherwise specified.

Table 1. Electrical Performance Characteristics Type 03

Characteristic	Symbol	Conditions		Limits Min	Limits Max	Unit
Input Offset Voltage	V_{IO}	$R_S = 200\ \Omega$	$T_A = +25°C$		2	mv
		$V_{OUT} = 1.5V$	$T_A = -55°C$		3	mv
			$T_A = +125°C$		3	mv
Input Offset Voltage Temperature Coefficient	$\frac{\Delta V_{IO}}{\Delta T}$	$R_S = 50\ \Omega$	$+25°C \leq T_A \leq +125°C$		10	uV/°C
			$-55°C \leq T_A \leq +25°C$		10	uV/°C
Input Offset Current	I_{IO}	$V_{OUT} = 1.5V$	$T_A = +25°C$		3	ua
			$T_A = -55°C$		7	ua
			$T_A = +125°C$		3	ua
Input Offset Current Temperature Coefficient	$\frac{\Delta I_{IO}}{\Delta T}$		$+25°C \leq T_A \leq +125°C$		25	na/°C
			$-55°C \leq T_A \leq +25°C$		75	na/°C

For all tests strobes are high unless otherwise specified.

Table I. Electrical Performance Characteristics Type 03

Characteristic	Symbol	Conditions	Limits Min	Limits Max	Unit
Input Bias Current	I_{IB}	T_A = +25°C		20	ua
		T_A = -55°C		45	ua
		T_A = +125°C		10	ua
Strobe Current	I_{STROBE}	V_{STROBE} = 0.4V ΔV_{IN} = -5 mv		-3.3	ma
Input Voltage Common Mode Rejection Ratio	CMRR	V- = -7.0V -5V ≤ V_{IN} ≤ +5V	80		dB
High Output Level	V_{OH}	ΔV_{IN} = +5 mv, I_{OH} = 400 ua	2.5	5.5	Volts
Low Output Level	V_{OL}	ΔV_{IN} = -5 mv, I_{OL} = 100 ma T_A = +25°C		1.5	Volts
		ΔV_{IN} = -5 mv, I_{OL} = 50 ma		1.0	Volts
		ΔV_{IN} = -5 mv, I_{OL} = 16 ma		0.4	Volts

For all tests strobes are high unless otherwise specified.

Table 1. Electrical Performance Characteristics Type 03

Characteristic	Symbol	Conditions	Limits Min	Limits Max	Unit
Output Level Strobe Low	V_o STROBE LOW	V_{STROBE} = 0.9V ΔV_{IN} = -5 mv	2.5	5.5	Volts
Output Level Strobe High	V_o STROBE HIGH	V_{STROBE} = 2.5V I_{OL} = 16 ma ΔV_{IN} = -5 mv		0.4	Volts
Output Leakage Current	I_{CEX}	V_{OUT} = 24V ΔV_{IN} = + 5 mv T_A = + 25°C		1.0	ua
				100	ua
		T_A = + 125°C		100	ua
Positive Supply Current	$+I_{CC}$	ΔV_{IN} = -5 mv		10	ma
Negative Supply Current	$-I_{CC}$	ΔV_{IN} = -5 mv		3.6	ma
Power Dissipation	P_D	ΔV_{IN} = -5 mv		142	mw
Response Time - Output Saturated High Level to Threshold Level	t_{HTHR}	Figure 11 T_A = + 25°C 100 mv step, 5 mv overdrive		60	usec

For all tests strobes are high unless otherwise specified.

Table I. Electrical Performance Characteristics Type 03

Characteristic	Symbol	Conditions	Limits Min	Limits Max	Units
Response Time - Output Saturated Low Level to Threshold Level	t_{LTHR}	Figure 11 T_A = + 25°C 100 mv step, 5 mv overdrive		60	usec
Strobe Release Time	t_{STRL}	Figure 11 T_A = + 25°C ΔV_{IN} = -5 mv		15	nsec

For all tests strobes are high unless otherwise specified.

TABLE III. Group A Inspection Type 01 and 02

Subgroup	Symbol	MIL-STD-883 Method	Test	Conditions		Limits Min	Limits Max	Unit
1 T_A = 25°C	V_{IO}	4001	1	Figure 9 R_S = 50Ω, V_{OUT} = 1.4V	TYPE 01		2	mv
					TYPE 02		3.5	mv
	V_{IO}	4001	2	Figure 9 R_S = 200Ω, V_{OUT} = 1.4V	TYPE 01		2	mv
					TYPE 02		3.5	mv
	I_{IO}	4001	3	Figure 9 V_{OUT} = 1.4V	TYPE 01		3	ua
					TYPE 02		10	ua
	I_{IB}	4001	4	Figure 9	TYPE 01		20	ua
					TYPE 02		75	ua
	CMRR	4003	5	Figure 9 R_S = 200Ω, V_- = -7.0V, V_{IN} = ±5V		80		db
	$+I_{CC}$	3005	6	Figure 9 V_{OUT} = 0	TYPE 01		9.0	mA
					TYPE 02		13.5	mA
	$-I_{CC}$	3005	7	Figure 9	TYPE 01		7.0	mA
					TYPE 02		6.2	mA
	I_{STROBE}	3009	8	Figure 9 TYPE 02 ONLY V_{STROBE} = 100 mv, ΔV_{IN} = +10mv			-2.5	mA
	V_{OH}	3006	9	Figure 9 I_{OH} = 5 ma	ΔV_{IN} = +5 mv, TYPE 01 ΔV_{IN} = + 10 mv, TYPE 02	2.5	4.0	V
	V_{OH}	3006	10	Figure 9 I_{OH} = 0 ma	ΔV_{IN} = +5 mv, TYPE 01 ΔV_{IN} = +10 mv, TYPE 02		5.0	V

For type 02, strobe on device not being tested is connected to ground, strobe on device being tested is left open unless otherwise specified. Tests to be performed on both sections of this dual unit.

TABLE III. Group A Inspection Type 01 and 02

Subgroup	Symbol	MIL-STD-883 Method	Test	Conditions	Limits Min	Limits Max	Unit
	V_{OL}	3007	11	Figure 9 I_{OL} = 0 ma ΔV_{IN} = -5 mv, TYPE 01; ΔV_{IN} = -10 mv, TYPE 02	-1.0	0	V
	V_O (Strobed)	3007	12	Figure 9 TYPE 02 ONLY V_{STROBE} = 0.3V ΔV_{IN} = +10 mv	-1.0	0	V
	I_{OL}	3009	13	Figure 9 V_{OL} = 0V ΔV_{IN} = -5 mv, TYPE 01	2.0		mA
				ΔV_{IN} = -10 mv, TYPE 02	0.5		mA
2 T_A = 125°C	V_{IO}	4001	14	Figure 9 R_S = 50Ω V_{OUT} = 1.0V TYPE 01		3	mV
				TYPE 02		4.5	mV
	V_{IO}	4001	15	Figure 9 R_S = 200Ω V_{OUT} = 1.0V TYPE 01		3	mV
				TYPE 02		4.5	mV
	$\Delta V_{IO}/\Delta T$	4001	16	$\frac{\Delta V_{IO}}{\Delta T} = \frac{V_{IO}\text{ (test 14)} - V_{IO}\text{(test 1)} \times 10^3}{100°C}$		10	uV/°C
	I_{IO}	4001	17	Figure 9 V_{OUT} = 1.0V TYPE 01		3	uA
				TYPE 02		10	uA
	$\Delta I_{IO}/\Delta T$	4001	18	$\frac{\Delta I_{IO}}{\Delta T} = \frac{I_{IO}\text{ (test 17)} - I_{IO}\text{(test 3)} \times 10^3}{100°C}$		25	nA/°C

TABLE III. Group A Inspection Type 01 and 02

Subgroup	Symbol	MIL-STD-883 Method	Test	Conditions	Limits Min	Limits Max	Unit
	I_{IB}	4001	19	Figure 9 TYPE 01		10	uA
				Figure 9 TYPE 02		40	uA
	$+I_{CC}$	3005	20	Figure 9 V_{OUT} = 0V TYPE 01		9.0	mA
				Figure 9 V_{OUT} = 0V TYPE 02		13.5	mA
	$-I_{CC}$	3005	21	Figure 9 TYPE 01		7.0	mA
				Figure 9 TYPE 02		6.2	mA
	I_{STROBE}	3009	22	Figure 9 TYPE 02 ONLY V_{STROBE} = 100 mv, ΔV_{IN} = +10mv		-2.5	mA
	V_{OH}	3005	23	Figure 9 I_{OH} = 5 ma ΔV_{IN} = +5 mv, TYPE 01 ΔV_{IN} = +10 mv, TYPE 02	2.5	4.0	V
	V_{OH}	3006	24	Figure 9 I_{OH} = 0 ma ΔV_{IN} = +5 mv, TYPE 01 ΔV_{IN} = +10 mv, TYPE 02		5.0	V
	V_{OL}	3007	25	Figure 9 I_{OL} = 0 ma ΔV_{IN} = -5 mv, TYPE 01 ΔV_{IN} = -10 mv, TYPE 02	-1.0	0	V
	V_O (Strobed)	3007	26	Figure 9 TYPE 02 ONLY V_{STROBE} = 0.3V, ΔV_{IN} = +10 mv	-1.0	0	V
	I_{OL}	3009	27	Figure 9, V_{OL} = 0V ΔV_{IN} = -5 mv, TYPE 01 ΔV_{IN} = -10 mv, TYPE 02	0.5		mA

TABLE III. Group A Inspection Type 01 and 02

Subgroup	Symbol	MIL-STD-883 Method	Test	Conditions		Limits Min	Limits Max	Unit
3 T_A = -55°C	V_{IO}	4001	28	Figure 9 $R_S = 50\Omega$, $V_{OUT} = 1.8$ V	TYPE 01		3	mV
					TYPE 02		4.5	mV
	V_{IO}	4001	29	Figure 9 $R_S = 200\Omega$, $V_{OUT} = 1.8$ V	TYPE 01		3	mV
					TYPE 02		4.5	mV
	$\Delta V_{IO}/\Delta T$	4001	30	$\frac{\Delta V_{IO}}{\Delta T} = \frac{V_{IO}(\text{test 28}) - V_{IO}(\text{test 1}) \times 10^3}{80°C}$			10	uV/°C
	I_{IO}	4001	31	Figure 9 $V_{OUT} = 1.8$ V	TYPE 01		7	uA
					TYPE 02		20	uA
	$\Delta I_{IO}/\Delta T$	4001	32	$\frac{\Delta I_{IO}}{\Delta T} = \frac{I_{IO}(\text{test 31}) - I_{IO}(\text{test 3}) \times 10^3}{80°C}$			75	nA/°C
	I_{IB}	4001	33	Figure 9	TYPE 01		45	uA
					TYPE 02		150	uA
	$+I_{CC}$	3005	34	Figure 9 $V_{OUT} = 0$V	TYPE 01		9.0	mA
					TYPE 02		13.5	
	$-I_{CC}$	3005	35	Figure 9	TYPE 01		7.0	mA
					TYPE 02		6.2	
	I_{STROBE}	3009	36	Figure 9 TYPE 02 ONLY $V_{STROBE} = -100$ mv, $\Delta V_{IN} = +10$mv			-2.5	mA

TABLE III. Group A Inspection Type 01 and 02

Subgroup	Symbol	MIL-STD-883 Method	Test	Conditions			Limits Min	Limits Max	Unit
	V_{OH}	3006	37	Figure 9, I_{OH} = 5 ma	ΔV_{IN} = +5 mv,	TYPE 01	2.5	4.0	V
					ΔV_{IN} = +10 mv,	TYPE 02			
	V_{OH}	3006	38	Figure 9, I_{OH} = 0 ma	ΔV_{IN} = +5 mv,	TYPE 01		5.0	V
					ΔV_{IN} = +10 mv,	TYPE 02			
	V_{OL}	3007	39	Figure 9, I_{OL} = 0 ma	ΔV_{IN} = -5 mv,	TYPE 01	-1.0	0	V
					ΔV_{IN} = -10 mv,	TYPE 02			
	V_O (Strobed)	3007	40	Figure 9	TYPE 02 ONLY V_{STROBE} = 0.3V	ΔV_{IN} = +10 mv	-1.0	0	V
	I_{OL}	3009	41	Figure 9, V_{OL} = 0V	ΔV_{IN} = -5 mv,	TYPE 01	1.0		mA
					ΔV_{IN} = -10 mv,	TYPE 02			
4 T_A = 25°C	A_{V+}	4004	42	Figure 9, V = -1.9 V		TYPE 01	1250		V/V
						TYPE 02	750		V/V
	A_{V-}	4004	43	Figure 9, V = -0.9 V		TYPE 01	1250		V/V
						TYPE 02	750		V/V
5 T_A = -55°C	A_{V+}	4004	44	Figure 9, V = -2.3 V		TYPE 01	1000		V/V
						TYPE 02	500		V/V
	A_{V-}	4004	45	Figure 9, V = -1.3 V		TYPE 01	1000		V/V
						TYPE 02	500		V/V

TABLE III: Group A inspection Type 01 and 02

Subgroup	Symbol	MIL-STD-883 Method	Test	Conditions		Limits Min	Limits Max	Unit
6 T_A = 125°C	A_{V+}	4004	46	Figure 9, V = - 1.5 V	TYPE 01	1000		V/V
					TYPE 02	500		V/V
	A_{V-}	4004	47	Figure 9, V = - 0.5 V	TYPE 01	1000		V/V
					TYPE 02	500		V/V
7 T_A = 25°C	*t_{LTHR}		48	Figure 11, V_{OD} = +12V, S2-Position 1			60	ns
	*t_{HTHR}		49	Figure 11, V_{OD} = -12V, S2-Position 1			60	ns
	*t_{STRL}		50	Figure 11, V_{OD} = +12V, S2-Position 2			15	ns

TABLE III. Group A Inspection Type 03

Subgroup	Symbol	MIL-STD-883 Method	Test	Conditions	Limits Min	Limits Max	Unit
1 $T_A = 25°C$	V_{IO}	4001	1	Figure 10 $R_S = 50\Omega$, $V_{OUT} = 1.5V$		2.0	mV
	V_{IO}	4001	2	Figure 10 $R_S = 200\Omega$, $V_{OUT} = 1.5V$		2.0	mV
	I_{IO}	4001	3	Figure 10 $V_{OUT} = 1.5V$		3.0	uA
	I_{IB}	4001	4	Figure 10		20	uA
	CMRR	4003	5	Figure 10, $R_S = 200\Omega$, $V- = -7.0V$, $V_{IN} = \pm 5V$	80		db
	$+I_{CC}$	4005	6	Figure 10, $\Delta V_{IN} = -5$ mv		10	mA
	$-I_{CC}$	4005	7	Figure 10, $\Delta V_{IN} = -5$ mv		3.6	mA
	I_{STROBE} (1)	3009	8	Figure 10, $V_{STROBE} = 0.4V$, $\Delta V_{IN} = -5$ mv		-3.3	mA
	I_{STROBE} (2)	3009	9	Figure 10, $V_{STROBE} = 0.4V$, $\Delta V_{IN} = -5$ mv		-3.3	mA
	V_{OH}	3006	10	Figure 10, $\Delta V_{IN} = +5$ mv $I_{OH} = 400$ ua	2.5	5.5	V

For all tests strobes are open unless otherwise specified.

TABLE III. Group A Inspection Type 03

Subgroup	Symbol	MIL-STD-883 Method	Test	Conditions	Limits Min	Limits Max	Unit
	V_{OL}	3007	11	Figure 10, ΔV_{IN} = -5 mv I_{OL} = 100 ma		1.5	V
	V_{OL}	3007	12	Figure 10, ΔV_{IN} = -5 mv I_{OL} = 50 ma		1.0	V
	V_{OL}	3007	13	Figure 10, ΔV_{IN} = -5 mv I_{OL} = 16 ma		0.4	V
	V_o STROBE LOW (1)		14	Figure 10, ΔV_{IN} = -5 mv V_{STROBE} = 0.9 V	2.5	5.5	V
	V_o STROBE LOW (2)		15	Figure 10, ΔV_{IN} = -5 mv V_{STROBE} = 0.9 V	2.5	5.5	V
	V_o STROBE HIGH (1)		16	Figure 10, ΔV_{IN} = -5 mv V_{STROBE} = 2.5 V I_{OL} = 16 ma		0.4	V
	V_o STROBE HIGH (2)		17	Figure 10, ΔV_{IN} = -5 mv V_{STROBE} = 2.5 V I_{OL} = 16 ma		0.4	V
	I_{CEX}		18	Figure 10 V_{OUT} = 24 V ΔV_{IN} = +5 mv		1.0	ua
2 T_A = 125°C	V_{IO}	4001	19	Figure 10 R_S = 50Ω V_{OUT} = 1.5 V		3.0	mV

TABLE III. Group A Inspection Type 03

Subgroup	Symbol	MIL-STD-883 Method	Test	Conditions	Limits Min	Limits Max	Unit
	V_{IO}	4001	20	Figure 10, $R_S = 200\Omega$ $V_{OUT} = 1.5V$		3.0	mV
	$\Delta V_{IO}/\Delta T$	4001	21	$\frac{\Delta V_{IO}}{\Delta T} = \frac{V_{IO}(\text{test 19}) - V_{IO}(\text{test 1}) \times 10^3}{100°C}$		10	uV/°C
	I_{IO}	4001	22	Figure 10, $V_{OUT} = 1.5V$		3.0	uA
	$\Delta I_{IO}/\Delta T$	4001	23	$\frac{\Delta I_{IO}}{\Delta T} = \frac{I_{IO}(\text{test 22}) - I_{IO}(\text{test 3}) \times 10^3}{100°C}$		25	nA/°C
	I_{IB}	4001	24	Figure 10		10	uA
	$+I_{CC}$	4005	25	Figure 10 $\Delta V_{IN} = -5$ mv		10	mA
	$-I_{CC}$	4005	26	Figure 10 $\Delta V_{IN} = -5$ mv		3.6	mA
	I_{STROBE} (1)	3009	27	Figure 10, $V_{STROBE} = 0.4V$, $\Delta V_{IN} = -5$ mv		-3.3	mA
	I_{STROBE} (2)	3009	28	Figure 10, $V_{STROBE} = 0.4V$, $\Delta V_{IN} = -5$ mv		-3.3	mA

TABLE III. Group A Inspection Type 03

Subgroup	Symbol	MIL-STD-883 Method	Test	Conditions	Limits Min.	Limits Max	Unit
	V_{OH}	3006	29	Figure 10 ΔV_{IN} = +5 mv, I_{OH} = 400 ua	2.5	5.5	V
	V_{OL}	3007	30	Figure 10 ΔV_{IN} = -5 mv, I_{OL} = 50 ma		1.0	V
	V_{OL}	3007	31	Figure 10 ΔV_{IN} = -5 mv, I_{OL} = 16 ma		0.4	V
	V_o STROBE LOW (1)		32	Figure 10 ΔV_{IN} = -5 mv V_{STROBE} = 0.9V	2.5	5.5	V
	V_o STROBE LOW (2)		33	Figure 10 ΔV_{IN} = -5 mv V_{STROBE} = 0.9V	2.5	5.5	V
	V_o STROBE HIGH (1)		34	Figure 10 ΔV_{IN} = -5 mv, V_{STROBE} = 2.5V I_{OL} = 16 ma		0.4	V
	V_o STROBE HIGH (2)		35	Figure 10 ΔV_{IN} = -5 mv, V_{STROBE} = 2.5V I_{OL} = 16 ma		0.4	V
	I_{CEX}		36	Figure 10, V_{OUT} = 24V ΔV_{IN} = +5 mv		100	uA

TABLE III. Group A Inspection Type 03

Subgroup	Symbol	MIL-STD-883 Method	Test	Conditions	Limits Min	Limits Max	Unit
3 $T_A = -55°C$	V_{IO}	4001	37	Figure 10, $R_S = 50\,\Omega$ $V_{OUT} = 1.5V$		3.0	mV
	V_{IO}	4001	38	Figure 10, $R_S = 200\,\Omega$ $V_{OUT} = 1.5V$		3.0	mV
	$\Delta V_{IO}/\Delta T$	4001	39	$\frac{\Delta V_{IO}}{\Delta T} = \frac{V_{IO}(\text{test 37}) - V_{IO}(\text{test 1}) \times 10^3}{80°C}$		10	uV/°C
	I_{IO}	4001	40	Figure 10, $V_{OUT} = 1.5V$		7.0	uA
	$\Delta I_{IO}/\Delta T$	4001	41	$\frac{\Delta I_{IO}}{\Delta T} = \frac{I_{IO}(\text{test 40}) - I_{IO}(\text{test 3}) \times 10^3}{80°C}$		75	nA/°C
	I_{IB}	4001	42	Figure 10		45	uA
	$+I_{CC}$	4005	43	Figure 10, $\Delta V_{IN} = -5$ mv		10	mA
	$-I_{CC}$	4005	44	Figure 10, $\Delta V_{IN} = -5$ mv		3.6	mA
	I_{STROBE} (1)	3009	45	Figure 10, $V_{STROBE} = 0.4V$, $\Delta V_{IN} = -5$ mv		-3.3	mA
	I_{STROBE} (2)	3009	46	Figure 10, $V_{STROBE} = 0.4V$, $\Delta V_{IN} = -5$ mv		-3.3	mA

TABLE III. Group A Inspection Type 03

Subgroup	Symbol	MIL-STD-883 Method	Test	Conditions	Limits. Min	Limits. Max	Unit
	V_{OH}	3006	47	Figure 10 ΔV_{IN} = +5 mv I_{OH} = 400 ua	2.5	5.5	V
	V_{OL}	3007	48	Figure 10 ΔV_{IN} = -5 mv I_{OL} = 50 ma		1.0	V
	V_{OL}	3007	49	Figure 10 ΔV_{IN} = -5 mv I_{OL} = 16 ma	..	0.4	V
	V_o STROBE LOW (1)		50	Figure 10 ΔV_{IN} = -5 mv V_{STROBE} = 0.9V	2.5	5.5	V
	V_o STROBE LOW (2)		51	Figure 10 ΔV_{IN} = -5 mv V_{STROBE} = 0.9V	2.5	5.5	V
	V_o STROBE HIGH (1)		52	Figure 10 ΔV_{IN} = -5 mv I_{OL} = 16 ma V_{STROBE} = 2.5V		0.4	V
	V_o STROBE HIGH (2)		53	Figure 10 ΔV_{IN} = -5 mv I_{OL} = 16 ma V_{STROBE} = 2.5V		0.4	V
	I_{CEX}		54	Figure 10 V_{OUT} = 24V ΔV_{IN} = +5 mv		100	uA
T_A = 25°C	t_{LTHR}		55	Figure 11, V_{OD} = -12V, S2-Position 1		60	ns

TABLE III. Group A Inspection Type 03

Subgroup	Symbol	MIL-STD-883 Method	Test	Conditions	Limits		Unit
					Min	Max	
	t_{HTHR}		56	Figure 11, V_{OD} =-12V, S2-Position 1		60	ns
	t_{STRL-1}		57	Figure 11, V_{OD} =-12V, S2-Position 2		15	ns
	t_{STRL-2}		58	Figure 11, V_{OD} =-12V, S2-Position 2		15	ns

TABLE IV

GROUP B AND C, END POINT ELECTRICAL PARAMETERS
(T_A = 25°C, V_+ = +12 Vdc, V_- = -6 Vdc)

TEST	TYPE 01		TYPE 02		TYPE 03	
	LIMIT	DELTA	LIMIT	DELTA	LIMIT	DELTA
V_{IO}	2.5 mV	±0.5 mV	4.0 mV	±0.5 mV	2.5 mV	±0.5 mV
I_{IB}	20 μA	±2 μA	75 μA	±7.5 μA	20 μA	±2 μA
I_{IO}	3 μA	±0.3 μA	10 μA	±1.0 μA	3 μA	±0.3 μA

DEFINITIONS

LOGIC THRESHOLD VOLTAGE - The approximate voltage at the output of the comparator at which the loading logic circuitry changes its digital state.

INPUT OFFSET VOLTAGE - The voltage between the input terminals when the output is at the logic threshold voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT - The difference in the currents into the two input terminals with the output at the logic threshold voltage.

INPUT BIAS CURRENT - The average of the two input currents.

INPUT VOLTAGE RANGE - The range of voltage on the input terminals for which the comparator will operate within specifications.

INPUT COMMON MODE REJECTION RATIO - The ratio of the input voltage range to the maximum change in input offset voltage over this range.

DIFFERENTIAL INPUT VOLTAGE RANGE - The range of voltage between the input terminals for which operation within specifications is assured.

VOLTAGE GAIN - The ratio of the change in output voltage to the change in voltage between the input terminals producing it with the DC output level in the vicinity of the logic threshold voltage.

RESPONSE TIME - The interval between the application of an input step function and the time when the output crosses the logic threshold voltage. The input step drives the comparator from some initial, saturated input voltage to an input level just barely in excess of that required to bring the output from saturation to the logic threshold voltage. This excess is referred to as the voltage overdrive.

POSITIVE OUTPUT LEVEL - The DC output voltage in the positive direction with the input voltage equal to or greater than a minimum specified amount.

NEGATIVE OUTPUT LEVEL - The DC output voltage in the negative direction with the input voltage equal to or greater than a minimum specified amount.

OUTPUT SINK CURRENT - The maximum negative current than can be delivered by the comparator.

PEAK OUTPUT CURRENT - The maximum current that may flow into the output load without causing damage to the comparator.

OUTPUT RESISTANCE - The resistance seen looking into the output terminal with the DC output level at the logic threshold voltage.

POWER CONSUMPTION - The DC power into the amplifier with no output load. The DC power will vary with signal level, but is specified as a maximum for the entire range of input-signal conditions.

TABLE 1. Electrical Performance Characteristics

Characteristic	Symbol	Conditions		Limits Min	Limits Max	Units
Line Regulation	V_{RLINE}	Vin = 12 to 15 V Vout = 5 V, I_L = 1ma	T_A = + 25°C		0.1	% Vout
			T_A = - 55°C		0.3	% Vout
			T_A = + 125°C		0.2	% Vout
	V_{RLINE}	Vin = 9.5 to 40 V Vout = 5 V, I_L = 1ma	T_A = + 25°C		0.3	% Vout
	V_{RLINE}	Vin = 12 to 40 V Vout = 2 V, I_L = 1ma	T_A = + 25°C		2.0	% Vout
Load Regulation	V_{RLOAD}	I_L = 1 to 50 ma Vout = 5 V, Vin = 12 V	T_A = + 25°C		0.15	% Vout
			T_A = - 55°C		0.6	% Vout
			T_A = + 125°C		0.4	% Vout
	V_{RLOAD}	I_L = 1 to 10ma Vout = 37 V, Vin = 40 V	T_A = + 25°C		0.5	% Vout
	V_{RLOAD}	I_L = 6 to 12ma Vout = 7.5, Vin = 10 V	T_A = + 25°C		0.2	% Vout
Reference Voltage	V_{REF}	I_{REF} = 1 ma Vin = 12 V	T_A = + 25°C	6.95	7.35	V_{DC}
			- 55°C ≤ T_A ≤ 125°C	6.90	7.40	V_{DC}
Output Short Circuit Current	I_{OS}	R_{SC} = 10Ω, R_L = 0 Vout = 5 V, Vin = 12 V	T_A = + 25°C	45	85	ma
Standby Current Drain	I_{SCD}	I_L = I_{REF} = 0, Vin = 30 V Vout = V_{REF}	T_A = + 25°C		3.0	ma
			T_A = - 55°C		3.5	ma
			T_A = + 125°C		2.4	ma

All regulation requirements are based on a constant junction temperature.
All Vout values are nominal.

TABLE 1. Electrical Performance Characteristics (Continued)

Page 2

Characteristic	Symbol	Conditions	Limits Min	Limits Max	Units
Average Temp. Coefficient of Output Voltage	TC Vout	V_{out} = 5 V, V_{in} = 12 V, I_L = 1 ma; $+25°C \leq T_A \leq +125°C$		0.010	%/°C
		$-55°C \leq T_A \leq +25°C$		0.015	%/°C
Long Term Stability				0.3	% Vout
Zener Voltage	V_Z	Available in packages A, B, C and D only; T_A = +25°C, I_Z = 1 ma	5.58	6.82	V_{DC}
Ripple Rejection	$\frac{\Delta vout}{\Delta vin}$	f = 50 Hz to 10KHz, See figure 13, Vout = 5 V; C_{REF} = 0, T_A = +25°C	64		db
	$\frac{\Delta vout}{\Delta vin}$	C_{REF} = 5 uf, T_A = +25°C	76		db
Output Noise	No	BW = 100Hz to 10KHz, See figure 13, Vout = 5 V; C_{REF} = 0, T_A = +25°C		30	u Vrms
	No	C_{REF} = 5 uf, T_A = +25°C		3.5	u Vrms
Line Transient Response	$\frac{\Delta Vout}{\Delta Vin}$	V_{in} = 12 V, V_{out} = 5 V, I_L = 1 ma, T_A = +25°C, R_{SC} = 0Ω, ΔV_{in} = 3 V, See figure 14		3	mv
Load Transient Response	$\frac{\Delta Vout}{\Delta IL}$	V_{in} = 12 V, V_{out} = 5 V, I_L = 40ma, T_A = +25°C, R_{SC} = 0Ω, ΔI_L = 10 ma, See figure 14		15	mv

All Vout values are nominal.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirement	Class A devices	Class B devices	Class C devices
Interim electrical parameters (Pre Burn-In) (Method 5004)	1	1	None
Final electrical test parameters (Method 5004)	1*, 2, 3	1*, 2, 3	1
Group A test requirements (Method 5005)	1, 2, 3, 4	1, 2, 3	1, 2, 3
Group B and C end point electrical parameters (Method 5005)	1, 2, 3 and Table IV delta limits	Table IV delta limits	Table IV delta limits
Additional electrical subgroups for Group C periodic inspections	None	4	4

* PDA applied to subgroup 1 (see 4.3 (h)).

TABLE III. GROUP A INSPECTION

Subgroup	Symbol	Test	Conditions	Limits Min	Limits Max	Units
1 T_A = +25°C	V_{RLINE}	1	V_{out} = 5 V I_L = 1 ma V_{in} = 12 to 15 V		0.10	% V_{out}
	V_{RLINE}	2	V_{out} = 5 V I_L = 1 ma (See Note 1) V_{in} = 9.5 to 40 V		0.3	% V_{out}
	V_{RLINE}	3	V_{out} = 2 V I_L = 1 ma V_{in} = 12 to 15 V		2.0	% V_{out}
	V_{RLOAD}	4	V_{out} = 5 V V_{in} = 12 V (See Note 1) I_L = 1 to 50 ma		0.15	% V_{out}
	V_{RLOAD}	5	V_{out} = 37 V V_{in} = 40 V I_L = 1 to 10 ma		0.5	% V_{out}
	V_{RLOAD}	6	V_{out} = 7.5V V_{in} = 10 V I_L = 6 to 12 ma		0.2	% V_{out}
	V_{REF}	7	V_{in} = 12 V I_{REF} = 1 ma	6.95	7.35	V_{DC}
	I_{OS}	8	R_{SC} = 10 Ω R_L = 0 (See Note 1) V_{out} = 5 V, V_{in} = 12 V	45	85	ma
	I_{SCD}	9	I_L = I_{REF} = 0, V_{in} = 30 V, Vout = V_{REF}		3.0	ma
	V_Z	10	I_Z = 1 ma Available in packages A, B, C and D only	5.58	6.82	V_{DC}

1. To eliminate heating, test must be made in less than 10 m sec, duty cycle of less than 5%.
2. All Vout values are nominal.
3. Use figure 12 unless otherwise specified.

TABLE III. GROUP A INSPECTION

Page 2

Subgroup	Symbol	Test	Conditions	Limits Min	Limits Max	Units
2 T_A = +125°C	V_{RLINE}	11	V_{out} = 5 V, I_L = 1 ma V_{in} = 12 to 15 V		0.2	% V_{out}
	V_{RLOAD}	12	V_{out} = 5 V, V_{in} = 12 V (See Note 1) I_L = 1 to 50 ma		0.4	% V_{out}
	V_{REF}	13	I_{REF} = 1 ma V_{in} = 12 V	6.90	7.40	V_{DC}
	TC_{Vout}	14	V_{out} = 5 V, V_{in} = 12 V I_L = 1 ma		0.010	%/°C
	I_{SCD}	15	I_L = I_{REF} = 0, V_{in} = 30 V, Vout = V_{REF}		2.4	ma
3 T_A = -55°C	V_{RLINE}	16	V_{out} = 5 V, I_L = 1 ma V_{in} = 12 to 15 V		0.3	% V_{out}
	V_{RLOAD}	17	V_{out} = 5 V, V_{in} = 12 V (See Note 1) I_L = 1 to 50 ma		0.6	% V_{out}
	V_{REF}	18	I_{REF} = 1 ma V_{in} = 12 V	6.90	7.40	V_{DC}
	TC_{Vout}	19	V_{out} = 5 V, V_{in} = 12 V I_L = 1 ma		0.015	%/°C
	I_{SCD}	20	I_L = I_{REF} = 0, V_{in} = 30 V, Vout = V_{REF}		3.5	ma
4 T_A = 25°C	Ripple Rej	21	f = 10KHz, C_{REF} = 0, see figure 13	64		dB
	Ripple Rej	22	f = 10KHz, C_{REF} = 5 uf, see figure 13	76		dB
	Output Noise	23	BW = 100 Hz to 10KHz, C_{REF} = 0 See figure 13		30	μ Vrms

All Vout values are nominal.
Use figure 12 unless otherwise specified.

TABLE III. GROUP A INSPECTION

Page 3

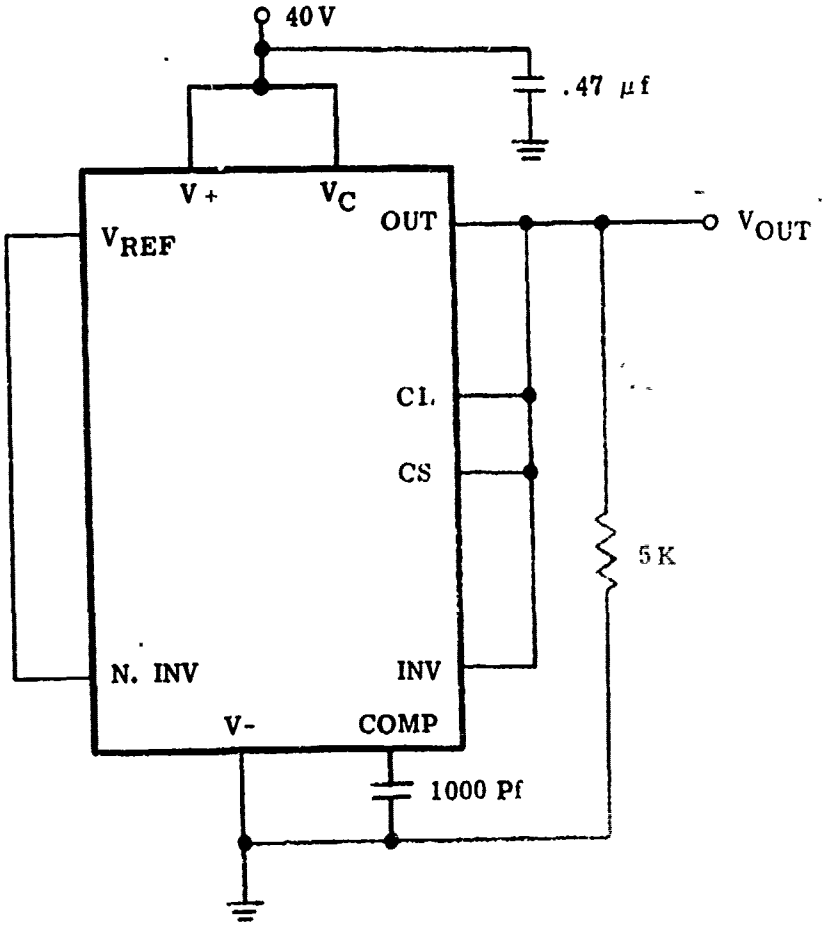
Subgroup	Symbol	Test	Conditions	Limits Min	Limits Max	Units
4	Output Noise	24	BW = 100 Hz to 10KHz, C_{REF} = 5 µf See figure 13		3.5	µ Vrms
T_A = 25°C	Line Transient Response	25	V_{in} = 12 V, V_{out} = 5 V, I_L = 1ma, R_{SC} = 0Ω, ΔV_{in} = 3 V, see figure 14		3	mv
	Load Transient Response	26	V_{in} = 12 V, V_{out} = 5 V, I_L = 40 ma, R_{SC} = 0Ω, ΔI_L = 10ma, see figure 14		15	mv

All Vout values are nominal.

TABLE IV. Groups B and C, end point electrical parameters (T_A = 25°C)

Characteristic	Symbol	Delta limits	Limits		Unit
			min	max	
Line regulation	V_{RLine}	± 15% or 1 mv*		0.10	% V_{out}
Load regulation	V_{RLoad}	± 20% or 1 mv*		0.15	% V_{out}
Reference voltage	V_{REF}	± 21mV	6.95	7.35	Vdc
Standby current drain	I_{SCD}	± 10%		3.0	mAdc

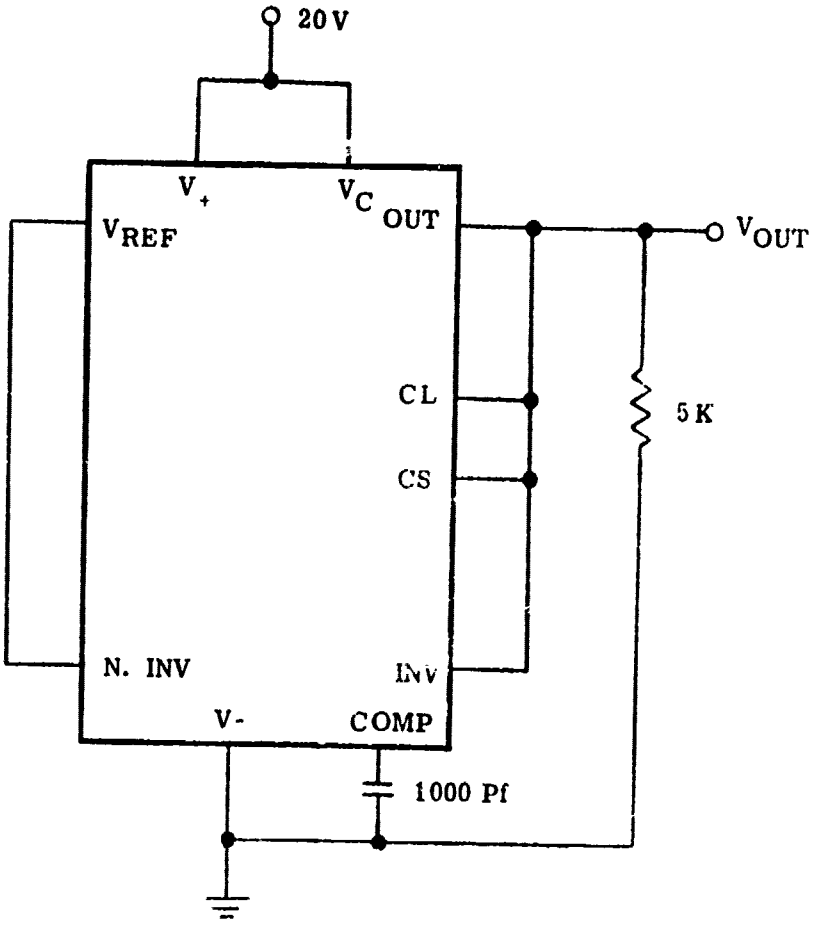
* whichever is greater



Pin Number Designations

Case	CS	INV	N. INV	V_{REF}	V-	OUT	V_C	V+	COMP	CL
H & I	1	2	3	4	5	6	7	8	9	10
A, B, C & D	3	4	5	6	7	10	11	12	13	2

FIGURE 10 - BURN-IN AND OPERATING LIFE TEST, TEST CIRCUIT



Pin Number Designations

Case	CS	INV	N. INV	V_{REF}	V-	OUT	V_C	V+	COMP	CL
H & I	1	2	3	4	5	6	7	8	9	10
A, P, C & D	3	4	5	6	7	10	11	12	13	2

FIGURE 11 - ACCELERATED BURN-IN AND LIFE TEST CIRCUIT

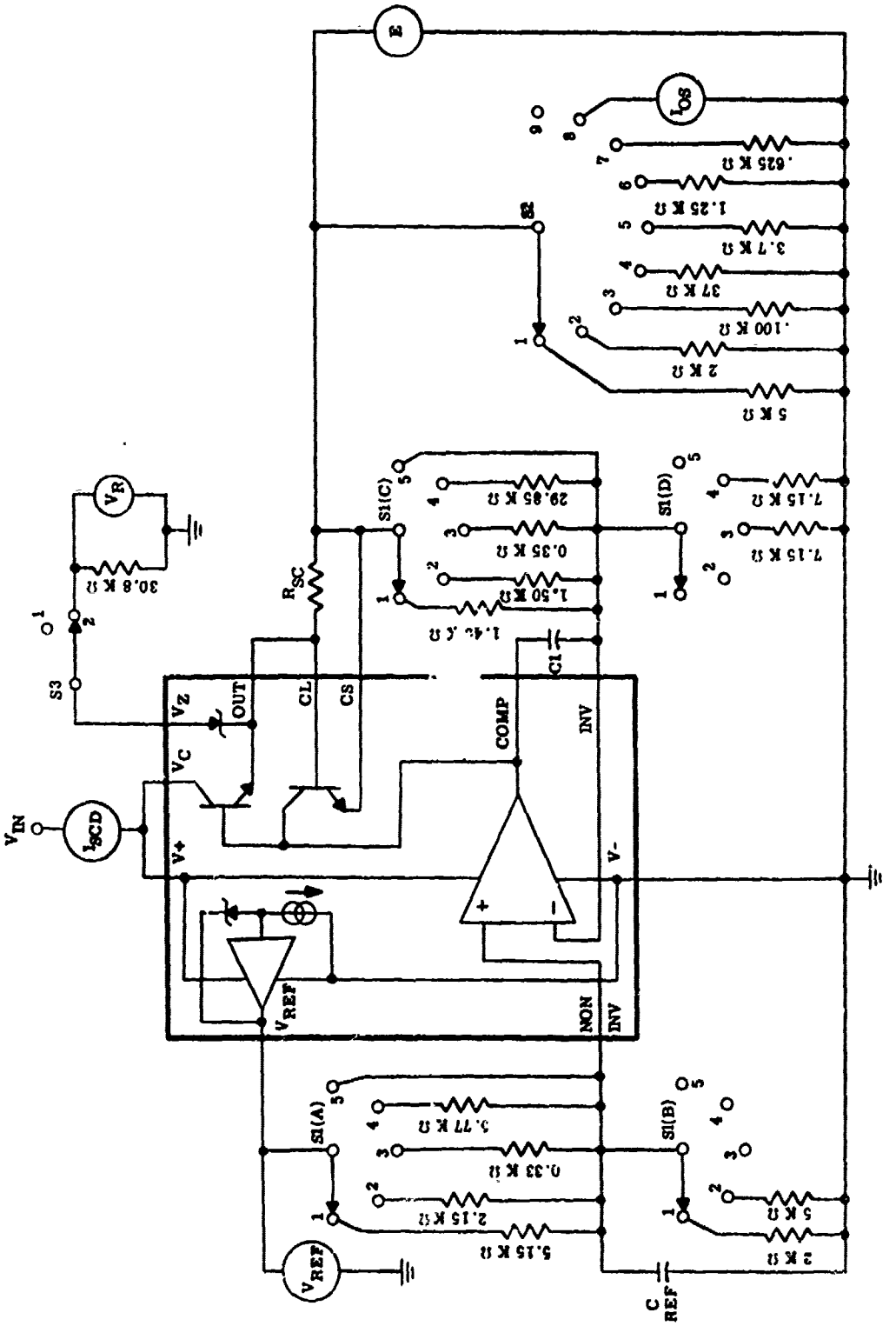


FIGURE 12

TEST CIRCUIT FOR STATIC AND DYNAMIC TESTS

FIGURE 12 (Continued)

Parameter	Test	V_{IN} (Volts)	Switch Positions S1	S2	S3	Measure Value	Units	Measured Parameters Equation	Units
V_{RLINE}	1, 11, 16	12 15	2 2	1 1	1 1	E1 E2	Volts Volts	$V_{RLINE} = \frac{E1 - E2}{E1} \times 100$	% V_{out}
V_{RLINE}	2	9.5 40	2 2	1 1	1 1	E3 E4	Volts Volts	$V_{RLINE} = \frac{E3 - E4}{E3} \times 100$	% V_{out}
V_{RLINE}	3	12 15	1 1	2 2	1 1	E5 E6	Volts Volts	$V_{RLINE} = \frac{E5 - E6}{E5} \times 100$	% V_{out}
V_{RLOAD}	4, 12, 17	12 12	2 2	1 3	1 1	E7 E8	Volts Volts	$V_{RLOAD} = \frac{E7 - E8}{E7} \times 100$	% V_{out}
V_{RLOAD}	5	40 40	4 4	4 5	1 1	E9 E10	Volts Volts	$V_{RLOAD} = \frac{E9 - E10}{E9} \times 100$	% V_{out}
V_{RLOAD}	6	10 10	3 3	6 7	1 1	E11 E12	Volts Volts	$V_{RLOAD} = \frac{E11 - E12}{E11} \times 100$	% V_{out}
V_{REF}	7, 13, 18	12	2	1	1	V_{REF}	Volts		
I_{OS}	8	12	2	8	1	I_{OS}	mA		
I_{SCD}	9, 15, 20	30	5	9	1	I_{SCD}	mA		
V_Z	10	40	4	4	2	V_R	Volts	$V_Z = E9 - V_R$	Volts
TC_{VOUT}	14, 19	12	2	1	1	E1	Volts	See notes 4 and 5	%/°C

NOTES:

1. Unless otherwise specified:

   V_{IN} = V+ = V_C = 12 V, V- = 0V, I_L = 1 mA, R_{SC} = 0 Ω, C1 = 100 pF and CREF = 0.

2. Resistor values required to set output voltage.

   a) For V_{OUT} = 2 to 7 V dc, R1, R2, R3, and R4 are determined as follows:

   $V_{OUT} = V_{REF} \times \frac{R2}{R1 + R2}$ $\qquad$ $\frac{V_{REF}}{R1 + R2} = 1$ mA

   $\frac{R1\ R2}{R1 + R2} = R3 \leq 10$ K Ω $\qquad$ R4 = Open Circuit

   b) For V_{OUT} = 7 to 37 Vdc, R1, R2, R3, and R4 are determined as follows:

   $V_{OUT} = V_{REF} \times \frac{R3 + R4}{R4}$ $\qquad$ $\frac{V_{OUT}}{R3 + R4} = 1$ mA

   $\frac{R3\ R4}{R3 + R4} = R1 \leq 10$ K $\qquad$ R2 = Open Circuit

   c) For the purpose of this specification, the following table shall be used to determine the resistor value required to obtain a given nominal output voltage.

	R1	R2	R3	R4
V_{OUT}	S1(A)	S1(B)	S1(C)	S1(D)
2V	5.15 K	2 K	1.45 K	∞
5V	2.15 K	5 K	1.50 K	∞
7.5V	0.33 K	∞	0.35 K	7.15 K
37V	5.77 K	∞	29.85 K	7.15 K

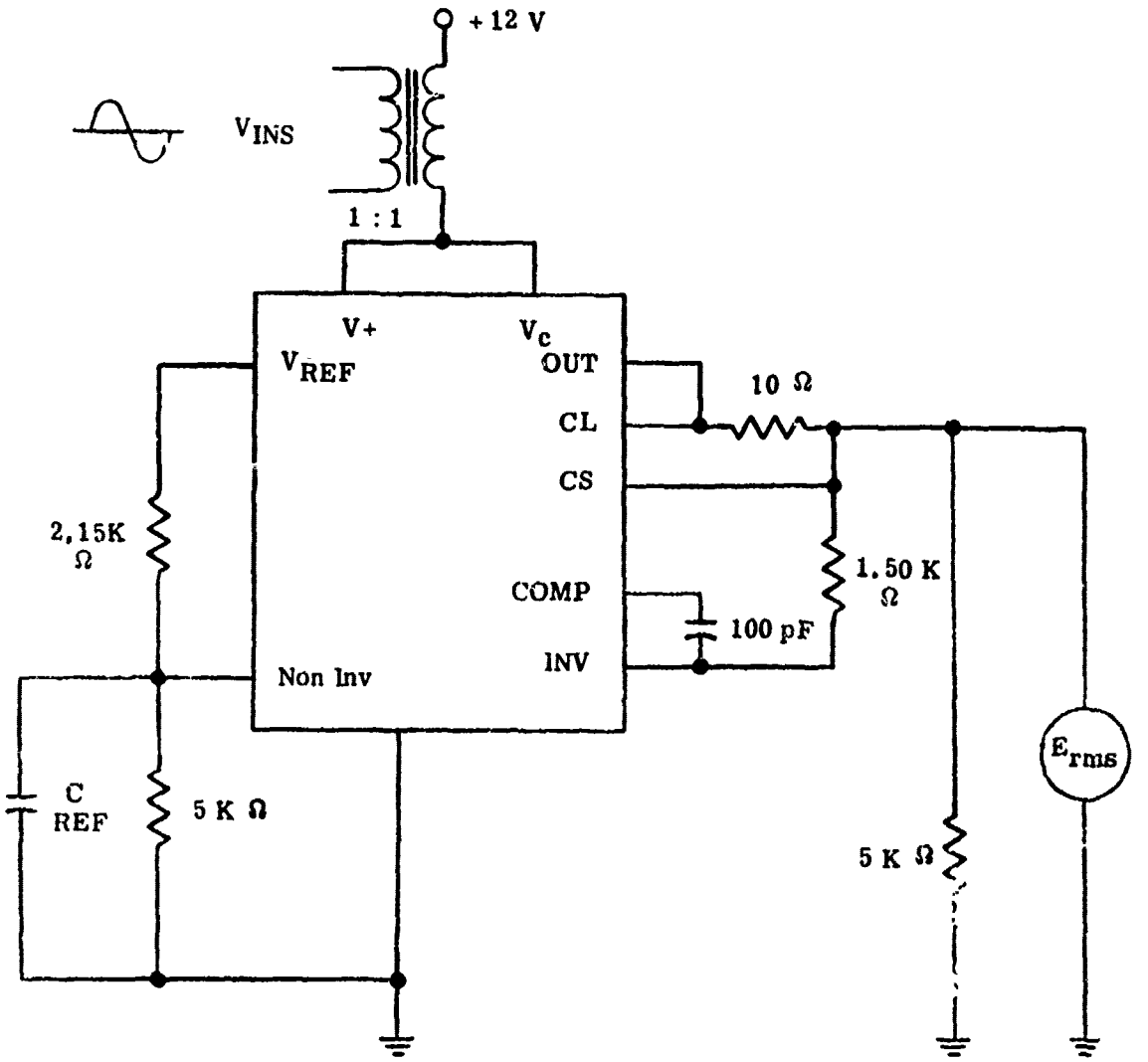
   If 1% resistors are used nominal V_{OUT} will be achieved within ±5%.

3. R_L chosen to obtain required I_L for given nominal output voltage.

4. TC V_{OUT} 25°C to 125°C = $\left| \frac{V_{OUT}\ @\ 25^{\circ}C - V_{OUT}\ @\ 125^{\circ}C}{V_{OUT}\ @\ 25^{\circ}C} \right| \div 100^{\circ}C$ = %/°C

5. T_C V_{OUT} -55°C to 25°C = $\left| \frac{V_{OUT}\ @\ -55^{\circ}C - V_{OUT}\ @\ 25^{\circ}C}{V_{OUT}\ @\ 25^{\circ}C} \right| \div 80^{\circ}C$ = %/°C

FIGURE 12 - Test Circuit for Static and Dynamic Tests (Continued)

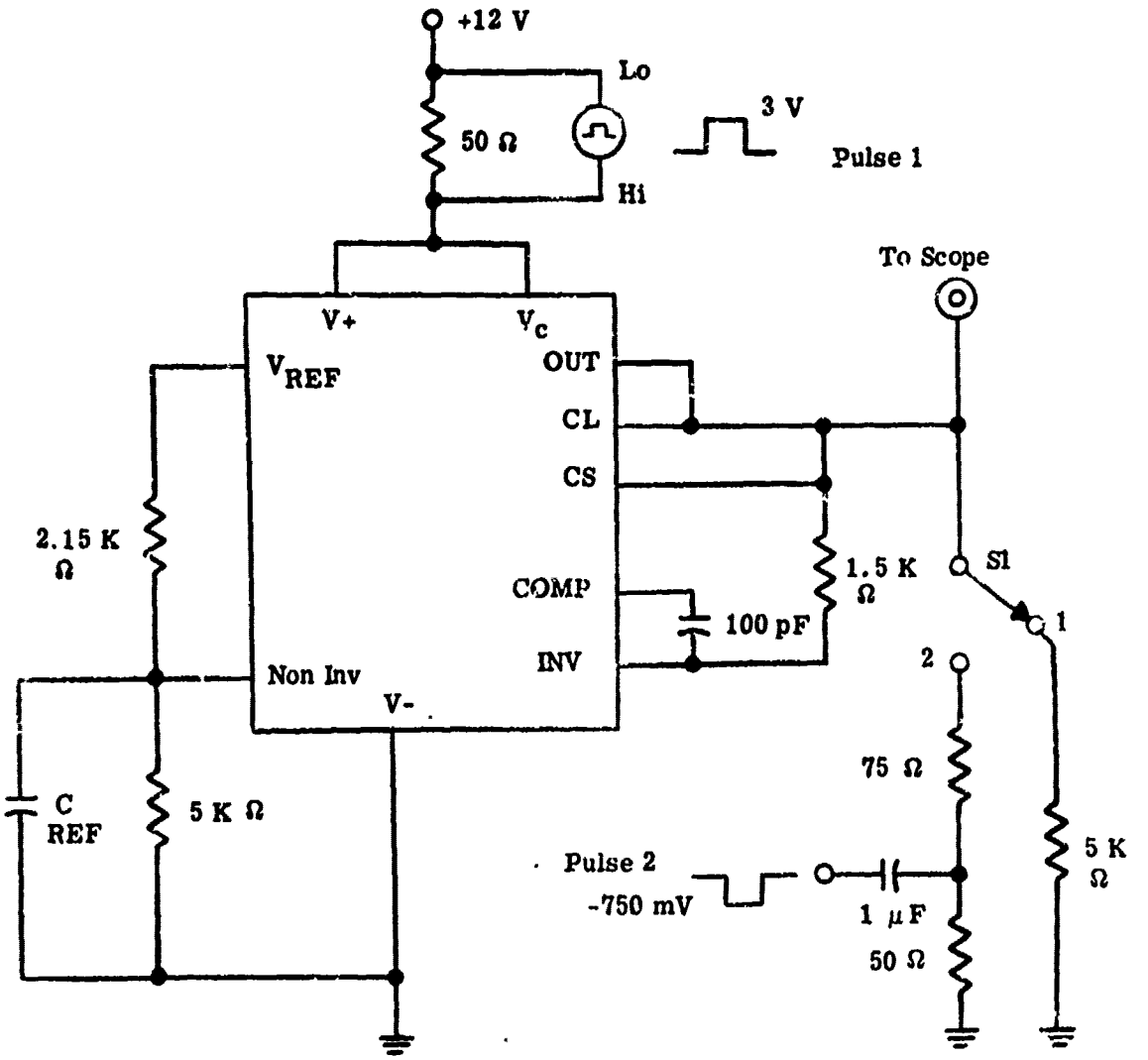


1. For ripple rejection
   V_{INS} = 2 V rms, 10 K Hz

$$\text{RIPPLE REJECTION (db)} = 20 \log \frac{E_{rms}}{V_{INS}}$$

2. For noise
   V_{INS} = 0 V rms
   E_{rms} (filtered to 100 Hz to 10 K Hz) = noise μ V rms

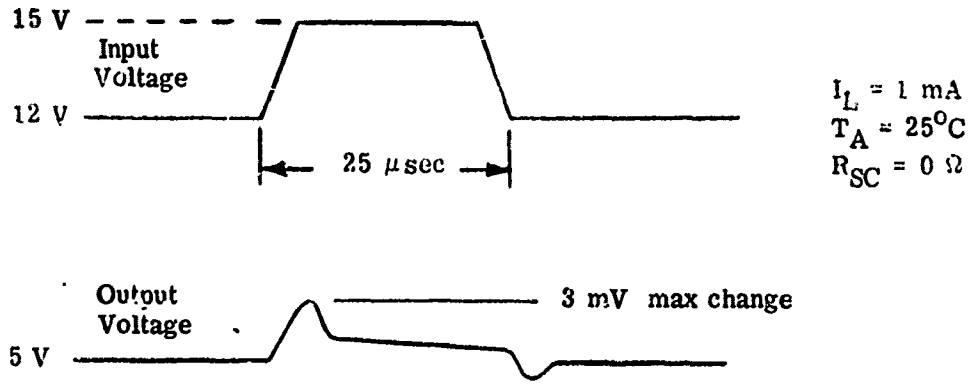
FIGURE 13 - RIPPLE REJECTION AND NOISE TEST CIRCUIT



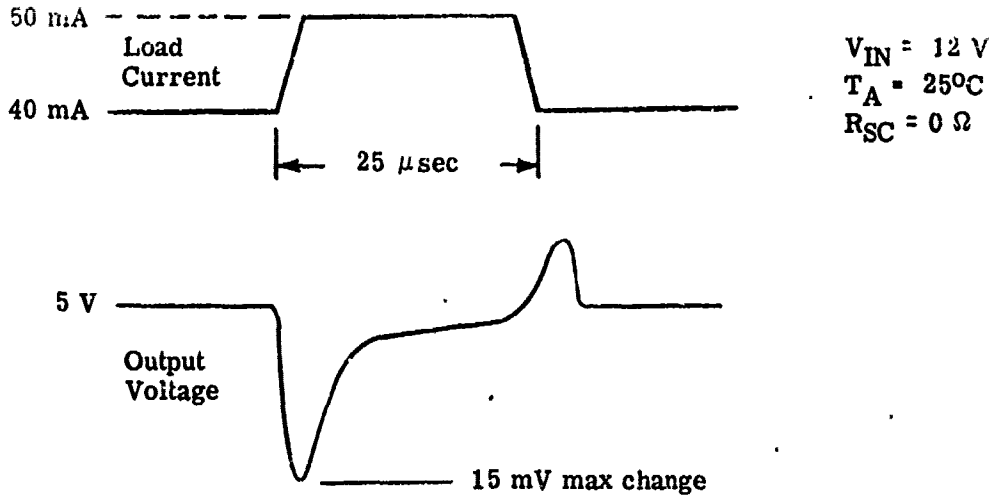
1. For line transient response, S1 in position 1
   Pulse 1 equals 3 V high, 25 μ sec wide, 3% duty cycle

2. For load transient response, S1 in position 2
   Pulse 1 = 0
   Pulse 2 equals -750 mV, 25 μsec wide, 3% duty cycle

FIGURE 14 - TRANSIENT RESPONSE TEST CIRCUIT



LINE TRANSIENT RESPONSE



LOAD TRANSIENT RESPONSE

Figure 14 (Continued)

DTL 930

TABLE I ELECTRICAL PERFORMANCE CHARACTERISTICS

TEST	SYMBOL	CONDITIONS	TEMP	LIMITS MIN	LIMITS MAX	UNITS
HIGH-LEVEL OUTPUT VOLTAGE	V_{OH}	V_{CC} = 4.5V, I_{OH} = -120μa 1/	V_{IN} = 1.1V, +25°C	3.4		VOLTS
			V_{IN} = 1.4V, -55°C	3.3		
			V_{IN} = 0.8V, +125°C	3.3		
LOW-LEVEL OUTPUT VOLTAGE	V_{OL}	V_{CC} = 4.5V, I_{OL} = 12.0ma 2/	V_{IN} = 1.8V, +25°C		0.40	VOLTS
			V_{IN} = 2.1V, -55°C		0.40	
			V_{IN} = 1.7V, +125°C		0.45	
HIGH-LEVEL INPUT CURRENT	I_{IH}	V_{CC} = 5.5V, V_{IN} = 4.0V 3/	+25°C		2.0	μa
			-55°C		2.0	
			+125°C		5.0	
LOW-LEVEL INPUT CURRENT	I_{IL}	V_{CC} = 5.5V, V_{IN} = 0.0V 1/	+25°C		-1.60	ma
			-55°C		-1.60	
			+125°C		-1.50	
OUTPUT TRANSISTOR LEAKAGE CURRENT	I_{CEX}	V_{CC} = 4.5V V_{IN} = 0.0V V_{OUT} = 4.5V	+25°C		50	μa
SHORT-CIRCUIT OUTPUT CURRENT	I_{OS}	V_{CC} = 5.5V, V_{IN} = 0.0V	+25°C	-.700	-1.34	ma
			-55°C	-.700	-1.34	
			+125°C	-.615	-1.30	
HIGH-LEVEL SUPPLY CURRENT PER GATE	I_{CCH}	V_{CC} = 5.0V V_{IN} = 0.0V	-55°C TO +125°C		1.47	ma
LOW-LEVEL SUPPLY CURRENT PER GATE	I_{CCL}	V_{CC} = 5.0V V_{IN} = OPEN	-55°C TO +125°C		3.25	ma
MAXIMUM HIGH-LEVEL SUPPLY CURRENT PER GATE	I_{CCH} (MAX)	V_{CC} = 5.5V V_{IN} = 0.0V	+25°C		2.75	ma
PROPAGATION DELAY TIME HIGH-TO-LOW-LEVEL	t_{PHL}	C_L = 50 Pf R_L = 400Ω SEE FIG	-25°C	10	30	ns
			-55°C	15	40	
			+125°C	6	35	
PROPAGATION DELAY TIME LOW-TO-HIGH-LEVEL	t_{PLH}	C_L = 30 Pf R_L = 3.9KΩ SEE FIG	+25°C	25	70	ns
			-55°C	35	80	
			+125°C	35	112	

1/ All but driven input shall be open.
2/ Vin applied to all inputs of gate at same time.
3/ All but driven input shall be grounded.

TABLE III. GROUP A INSPECTION FOR DEVICE TYPE 01

TERMINAL CONDITIONS (PINS NOT DESIGNATED ARE OPEN)

Subgroup	Symbol	MIL-STD-883 method	CASE A+B	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Meas. terminal	TEST LIMITS		
			CASE C	4	2	NC	3	NC	4	5	6	NC	NC	7	8	9	10				
			TEST NO	1A	1B	1X	1C	1D	1E	GND	F	G	H	Y	I	J	V_{CC}		Min	Max	Unit
1	V_{OL}	3007	1	1.9V	1.9V		1.9V	1.9V	12ma	GND							4.5V	E		.4	V
T_A=25°C	V_{OL}	↓	2								12ma	1.9V	1.9V		1.9V	1.9V		F		.4	V
	V_{OH}	3006	3	1.1V					-120ua									E	3.4		V
	V_{OH}		4		1.1V				-120ua									E	3.4		V
	V_{OH}		5				1.1V		-120ua									E	3.4		V
	V_{OH}		6					1.1V	-120ua									E	3.4		V
	V_{OH}		7			1.8V			-120ua									E	3.4		V
	V_{OH}		8								-120ua	1.1V						F	3.4		V
	V_{OH}		9								-120ua		1.1V					F	3.4		V
	V_{OH}		10								-120ua				1.1V			F	3.4		V
	V_{OH}		11								-120ua					1.1V		F	3.4		V
	V_{OH}		12								-120ua			1.8V				E	3.4		V
	I_{OS}	3011	13	GND					GND								5.5V	E	-.700	-1.34	ma
	I_{OS}	↓	14								GND				GND			F	-.700	-1.34	ma
	I_{IH}	3010	15	4.0V	GND		GND	GND										A		2.0	ua
	I_{IH}		16	GND	4.0V		GND	GND										B		2.0	ua
	I_{IH}		17	GND	GND		4.0V	GND										C		2.0	ua
	I_{IH}		18	GND	GND		GND	4.0V										D		2.0	ua
	I_{IH}		19									4.0V	GND		GND	GND		G		2.0	ua
	I_{IH}		20									GND	4.0V		GND	GND		H		2.0	ua
	I_{IH}		21									GND	GND		4.0V	GND		I		2.0	ua
	I_{IH}		22									GND	GND		GND	4.0V		J		2.0	ua

C2

Subgroup	Symbol	Mil-STD-883 method	CASE A+B CASE C TEST NO.	1 A	2 B	3 X	4 C	5 D	6 E	7 GND	8 F	9 G	10 H	11 Y	12 I	13 J	14 V_{CC}	MEAS TERMINAL	TEST LIMITS MIN	MAX	UNIT
1 T_A = 25°C	I_{IL}	3009	23	GND						GND							5.5V	A		-1.60	ma
	I_{IL}		24		GND													B		-1.60	ma
	I_{IL}		25				GND											C		-1.60	ma
	I_{IL}		26					GND										D		-1.60	ma
	I_{IL}		27									GND						G		-1.60	ma
	I_{IL}		28										GND					H		-1.60	ma
	I_{IL}		29												GND			I		-1.60	ma
	I_{IL}		30													GND		J		-1.60	ma
	I_{CCL}	3005	31														5.0V	V_{CC}		6.50	ma
	I_{CCH}	3005	32	GND											GND		5.0V	V_{CC}		2.94	ma
	$I_{CC,V(MAX)}$	3005	33	GND											GND		8.0V	V_{CC}		5.50	ma
	I_{CEX}		34	GND					4.5V								4.5V	E		50	μa
	I_{CEX}		35								4.5V				GND		4.5V	F		50	μa
2 T_A = 125°C	V_{OL}	3007	36	1.7V	1.7V		1.7V	1.7V	12ma								4.5V	E		.45	V
	V_{OL}		37								12ma	1.7V	1.7V		1.7V	1.7V		F		.45	V
	V_{OH}	3006	38	0.8V					-120μa									E	3.3		V
	V_{OH}		39		0.8V				-120μa									E	3.3		V
	V_{OH}		40				0.8V		-120ma									E	3.3		V
	V_{OH}		41					0.8V	-120ma									E	3.3		V
	V_{OH}		42								-120μa	0.8V						F	3.3		V
	V_{OH}		43								-120μa		0.8V					F	3.3		V
	V_{OH}		44								-120ma				0.8V			F	3.3		V
	V_{OH}		45								-120mA					0.8V		E	3.3		V

Subgroup	Symbol	Mil-STD-883 method	CASE A+B / CASE C / TEST No	1 / 1 / A	2 / 2 / B	3 / NC / X	4 / 3 / C	5 / NC / D	6 / 4 / E	7 / 5 / GND	8 / 6 / F	9 / NC / G	10 / NC / H	11 / 7 / Y	12 / 8 / I	13 / 9 / J	14 / 10 / Vcc	MEAS TERMINAL	TEST LIMITS Min	Max	UNIT
2	I_{OS}	3011	46	GND					GND	GND							5.5V	E	-.615	-1.30	mA
$T_A = 125°C$	I_{OS}	↓	47								GND				GND			F	-.615	-1.30	mA
	I_{IN}	3010	48	4.0V	GND		GND	GND										A		5.0	μA
	I_{IL}		49	GND	4.0V		GND	GND										B		5.0	μA
	I_{IN}		50	GND	GND		4.0V	GND										C		5.0	μA
	I_{IL}		51	GND	GND		GND	4.0V										D		5.0	μA
	I_{IN}		52									4.0V	4.0		GND	GND		G		5.0	μA
	I_{IN}		53									GND	4.0V		GND	GND		H		5.0	μA
	I_{IN}		54									GND	GND		4.0V	GND		I		5.0	μA
	I_{IN}	↓	55									GND	GND		GND	4.0V		J		5.0	μA
	I_{IL}	3009	56	GND														A		-1.50	mA
	I_{IL}		57		GND													B		-1.50	mA
	I_{IL}		58				GND											C		-1.50	mA
	I_{IL}		59					GND										D		-1.50	mA
	I_{IL}		60									GND						G		-1.50	mA
	I_{IL}		61										GND					H		-1.50	mA
	I_{IL}		62												GND			I		-1.50	mA
	I_{IL}	↓	63													GND	↓	J		-1.50	mA
	I_{CCL}	3005	64														5.0V	Vcc		6.60	mA
7	I_{CCN}	3005	65	GND						GND					GND		5.0V	Vcc		2.34	mA

			CASE A&B	1	2	3	4	5	6	7	8	9	10	11	12	13	14		TEST LIMITS		
			CASE C	1	2	NC	3	NC	4	5	6	NC	7	8	9	10	V_{CC}	MEAS			
			TEST #	A	B	X	C	D	E	GND	F	G	H	Y	I	J	V_{CC}	TERMINAL	Min	Max	Unit
3	V_{OL}	3007	66	2.1V	2.1V		2.1V	2.1V	12ma	GND							4.5V	E		.4	V
T_A = -55°C	V_{OL}	↓	67								12ma	2.1V	2.1V		2.1V	2.1V	↓	F		.4	V
	V_{OH}	3006	68	1.4V					120ua									E	3.3		V
	V_{OH}	↓	69		1.4V				120ua									E	3.3		V
	V_{OH}		70				1.4V		120ua									E	3.3		V
	V_{OH}		71					1.4V	120ua									E	3.3		V
	V_{OH}		72								120ua	1.4V						F	3.3		V
	V_{OH}		73								120ua		1.4V					F	3.3		V
	V_{OH}		74								120ua				1.4V			F	3.3		V
	V_{OH}	↓	75								120ua					1.4V	↓	F	3.3		V
	I_{OS}	3011	76	GND					GND								5.5V	E	-.700	-1.34	ma
	I_{OS}	↓	77								GND				GND		↓	F	-.700	-1.34	ma
	I_{IN}	3010	78	4.0V	GND		GND	GND										A		2.0	ua
	I_{IN}		79	GND	4.0V		GND	GND										B		2.0	ua
	I_{IN}		80	GND	GND		4.0V	GND										C		2.0	ua
	I_{IN}		81	GND	GND		GND	4.0V										D		2.0	ua
	I_{IN}		82									4.0V	GND		GND	GND		G		2.0	ua
	I_{IN}		83									GND	4.0V		GND	GND		H		2.0	ua
	I_{IN}		84									GND	GND		4.0V	GND		I		2.0	ua
	I_{IN}	↓	85									GND	GND		GND	4.0V		J		2.0	ua
	I_{IL}	3009	26	GND														A		-1.60	ma
	I_{IL}		27		GND													B		-1.60	ma
	I_{IL}	↓	28				GND			↓							↓	C		-1.60	ma

Subgroup	Symbol	MIL-STD-883 METHOD	CASE A & B	1	2	3	4	5	6	7	8	9	10	11	12	13	14	MEAS TERMINAL	TEST LIMITS Min	Max	Unit
			CASE C	1	2	NC	3	NC	4	5	6	NC	NC	7	8	9	10				
			TEST No	A	B	X	C	D	E	GND	F	G	H	Y	I	J	V_{CC}				
3	I_{IL}	3009	89					GND		GND							5.5V	D		-1.60	mA
T_A = -55°C	I_{IL}		90									GND						G		-1.60	mA
	I_{IL}		91										GND					H		-1.60	mA
	I_{IL}		92												GND			I		-1.60	mA
	I_{IL}		93													GND		J		-1.60	mA
	I_{CCL}	3005	94														5.0V	V_{CC}		6.50	mA
	I_{CCH}	3005	95	GND											GND		5.0V	V_{CC}		2.94	mA
9	t_{PHL}	3003 FIG HEREIN	96	IN					OUT	GND							5.0V	A TO E	10	30	nsec
T_A = 25°C	t_{PHL}		97								OUT				IN			G TO F	10	30	nsec
	t_{PLH}	3003 FIG HEREIN	98	IN					OUT									A TO E	25	80	nsec
	t_{PLH}		99								OUT				IN			G TO F	25	80	nsec
10	t_{PHL}	3003 FIG HEREIN	100	IN					OUT									A TO E	15	40	nsec
T_A = +125°C	t_{PHL}		101								OUT				IN			G TO F	15	40	nsec
	t_{PLH}	3003 FIG HEREIN	102	IN					OUT									A TO E	35	112	nsec
	t_{PLH}		103								OUT				IN			G TO F	35	112	nsec
11	t_{PHL}	3003 FIG HEREIN	104	IN					OUT									A TO E	15	40	nsec
T_A = 55°C	t_{PHL}		105								OUT				IN			G TO F	15	40	nsec
	t_{PLH}	3003 FIG HEREIN	106	IN					OUT									A TO E	25	80	nsec
	t_{PLH}		107								OUT				IN			G TO F	25	80	nsec

DTL 932

TABLE I ELECTRICAL PERFORMANCE CHARACTERISTICS

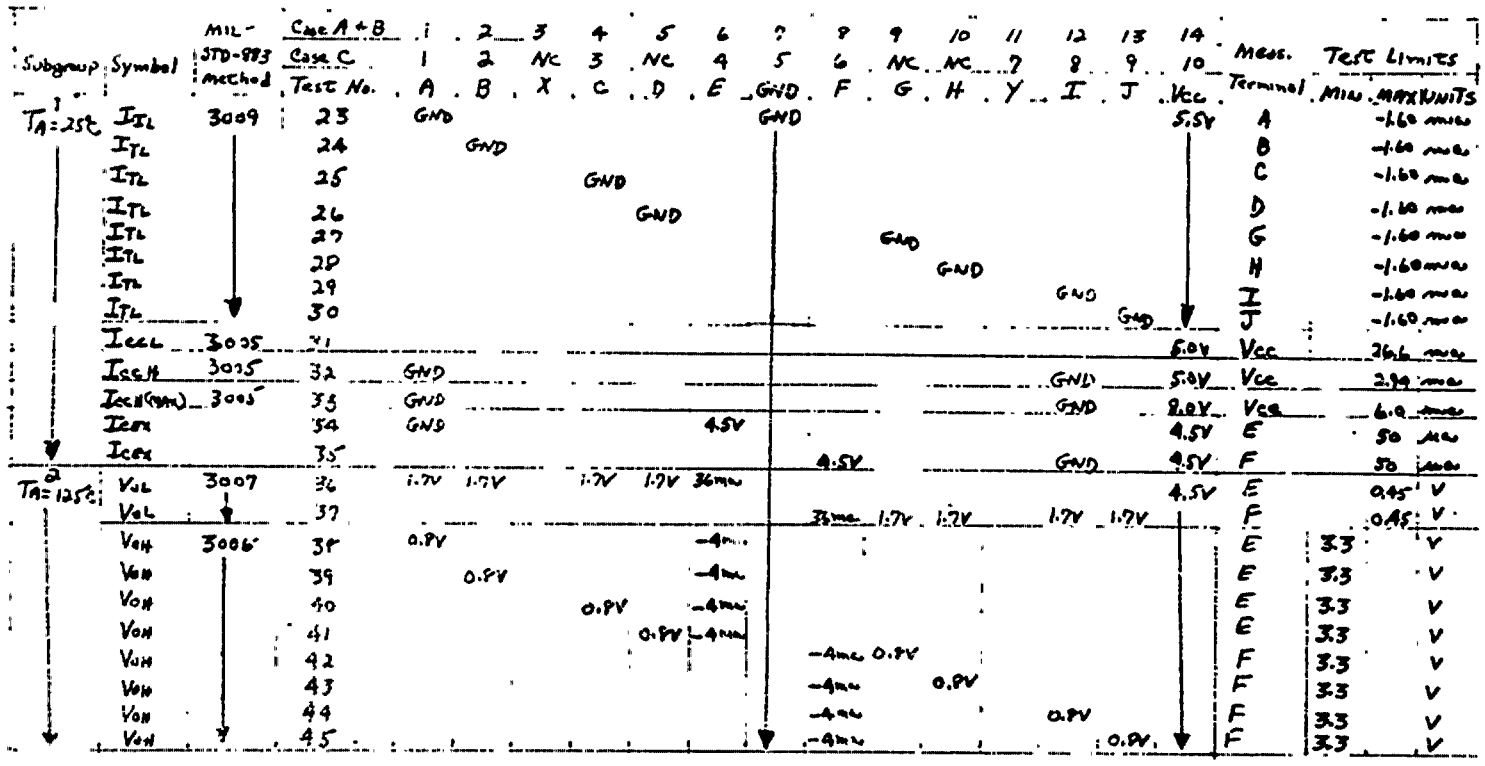
TEST	SYMBOL	CONDITIONS			TEMP	LIMITS MIN	LIMITS MAX	UNITS
HIGH-LEVEL OUTPUT VOLTAGE	V_{OH}	V_{CC} = 4.5V [1]	I_{OH} = -2.5ma	V_{IN} = 1.1V	+25°C	3.4		
			I_{OH} = -2.0ma	V_{IN} = 1.4V	-55°C	3.3		
			I_{OH} = -4.0 ma	V_{IN} = 0.8V	+125°C	3.3		
LOW-LEVEL OUTPUT VOLTAGE	V_{OL}	V_{CC} = 4.5V		V_{IN} = 1.9V	+25°C		0.40	VOLT
		I_{OL} = 3 ma		V_{IN} = 2.1V	-55°C		0.40	
		[2]		V_{IN} = 1.7V	+125°C		0.45	
HIGH-LEVEL INPUT CURRENT	I_{IH}	V_{CC} = 5.5V			+25°C		2.0	
		V_{IN} = 4.0V			-55°C		2.0	ma
		[3]			+125°C		5.0	
LOW-LEVEL INPUT CURRENT	I_{IL}	V_{CC} = 5.5V			+25°C		-1.6	
		V_{IN} = 0.0V			-55°C		-1.6	ma
		[1]			+125°C		-1.5	
OUTPUT TRANSISTOR LEAKAGE CURRENT	I_{CEX}	V_{CC} = 4.5V	V_{IN} = 0.0V	V_{OUT} = 4.5V	+25°C		50	μa
SHORT-CIRCUIT OUTPUT CURRENT	I_{OS}	V_{CC} = 5.5V			+25°C	18		
		V_{IN} = 0.0V			-55°C	16		ma
					+125°C	16		
HIGH-LEVEL SUPPLY CURRENT PER GATE	I_{CCH}	V_{CC} = 5.0V	V_{IN} = 0.0V		-55°C to +125°C		1.47	ma
LOW-LEVEL SUPPLY CURRENT PER GATE	I_{CCL}	V_{CC} = 5.0V	V_{IN} = OPEN		-55°C to +125°C		13.3	ma
MAXIMUM HIGH-LEVEL SUPPLY CURRENT PER GATE	$I_{CCH(MAX)}$	V_{CC} = 5.0V	V_{IN} = 0.0V		+25°C		3.0	ma
PROPAGATION DELAY TIME HIGH-TO-LOW-LEVEL	t_{PHL}	C_L = 500pf	R_L = 150Ω	SEE FIG	+25°C	5	40	n.s.
					-55°C	15	60	
					+125°C	15	60	
PROPAGATION DELAY TIME LOW-TO-HIGH-LEVEL	t_{PLH}	C_L = 500pf	R_L = 510Ω	SEE FIG	+25°C	25	80	n.s.
					-55°C	25	120	
					+125°C	45	120	

[1] ALL BUT DRIVEN INPUT SHALL BE OPEN.
[2] V_{IN} APPLIED TO ALL INPUTS OF GATE AT SAME TIME.
[3] ALL BUT DRIVEN INPUT SHALL BE GROUNDED.

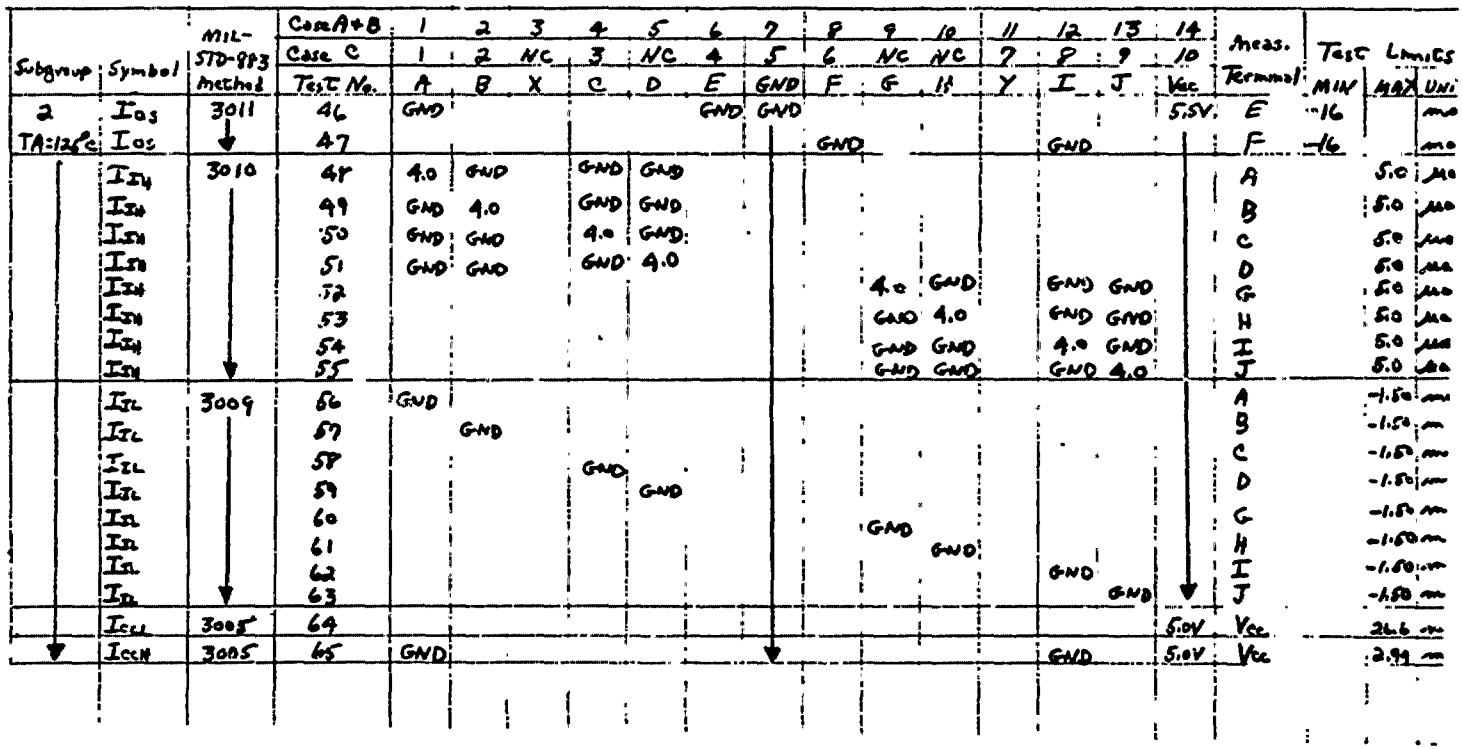
TABLE III GROUP A INSPECTION FOR DEVICE TYPE 01

TERMINAL CONDITIONS (PINS NOT DESIGNATED ARE OPEN)

Subgroup	Symbol	MIL-STD-883 method	Case A+B: Case C Test No.	1 1 A	2 2 B	3 NC X	4 3 C	5 NC D	6 4 E	7 GND GND	8 5 F	9 6 G	10 NC NC H	11 7 Y	12 8 I	13 9 J	14 10 Vcc	Meas. Terminal	Test Limits Min	Max	Units
																	4.5V	E		0.4	V
T_A=25°C	V_{OL}	3007	1	1.1V	1.9V		1.9V	1.9V													
	V_{OL}	↓	2									1.9V	1.9V		1.9V	1.9V		F		0.4	V
	V_{OH}	3006	3	1.1V					-2.5mA									E	3.4		V
	V_{OH}		4		1.1V				-2.5mA									E	3.4		V
	V_{OH}		5				1.1V		-2.5mA									E	3.4		V
	V_{OH}		6					1.1V	-2.5mA									E	3.4		V
	V_{OH}		7			1.8V			-2.5mA									E	3.4		V
	V_{OH}		8								-2.5mA	1.1V						F	3.4		V
	V_{OH}		9								-2.5mA		1.1V					F	3.4		V
	V_{OH}		10								-2.5mA				1.1V			F	3.4		V
	V_{OH}		11								-2.5mA					1.1V		F	3.4		V
	V_{OH}		12								-2.5mA			1.9V				F	3.4		V
	I_{OS}	3011	13	GND					GND								6.5V	E	-18		mA
	I_{OS}	↓	14								GND				GND			F	-18		mA
	I_{CC}	3010	15	4.0	GND		GND	GND										A		2.0	mA
	I_{CC}		16	GND	4.0		GND	GND										B		2.0	mA
	I_{CC}		17	GND	GND		4.0	GND										C		2.0	mA
	I_{CC}		18	GND	GND		GND	4.0										D		2.0	mA
	I_{CC}		19									4.0	GND		GND	GND		G		2.0	mA
	I_{CC}		20									GND	4.0		GND	GND		H		2.0	mA
	I_{CC}		21									GND	GND		4.0	GND		I		2.0	mA
	I_{CC}	↓	22									GND	GND		GND	4.0		J		2.0	mA

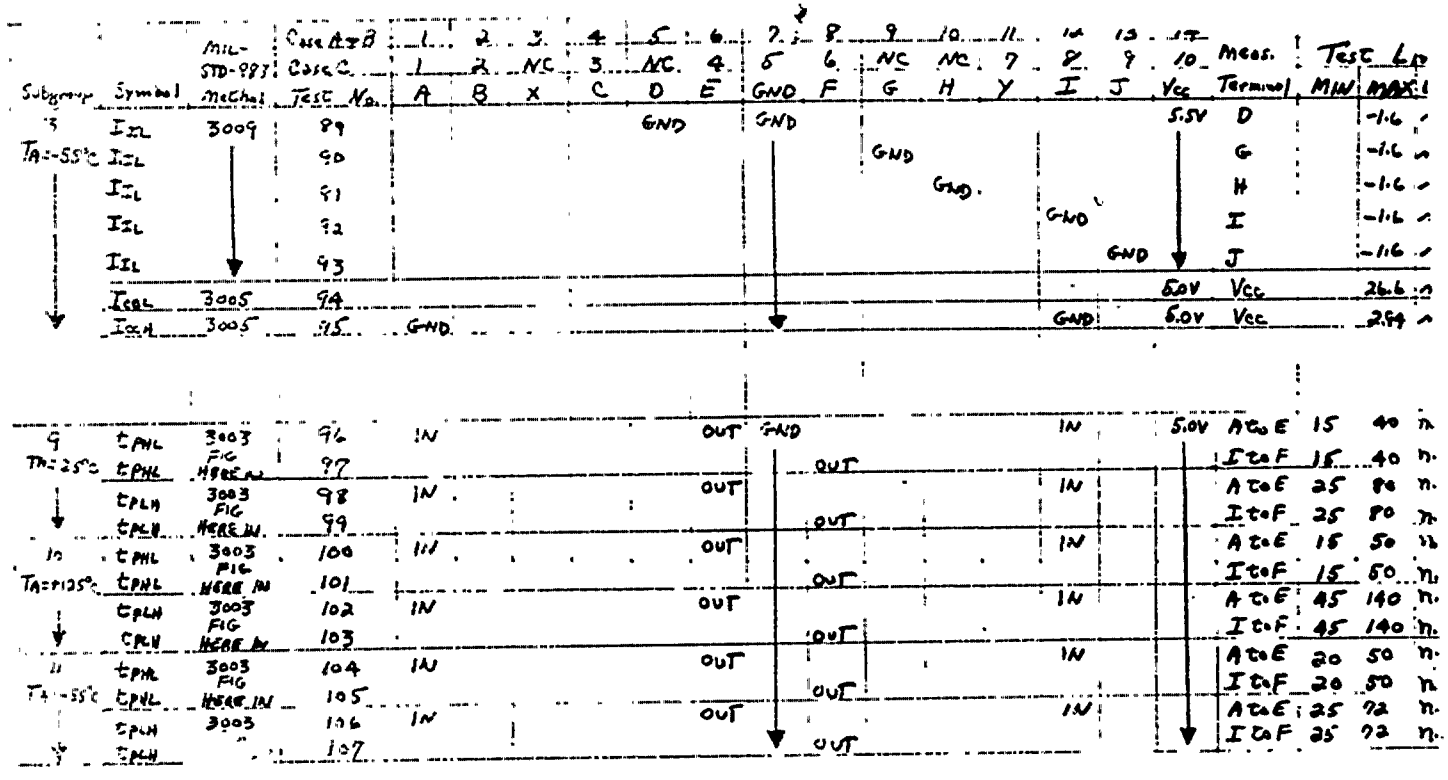


Subgroup	Symbol	MIL-STD-883 method	Case A+B / Case C Test No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Meas. Terminal	Test Limits Min	Max	Units
				A	B	X	C	D	E	GND	F	G	H	Y	I	J	Vcc				
T_A=25°C	I_{IL}	3009	23	GND						GND							5.5V	A		-1.60	mA
	I_{IL}		24		GND													B		-1.60	mA
	I_{IL}		25				GND											C		-1.60	mA
	I_{IL}		26					GND										D		-1.60	mA
	I_{IL}		27									GND						G		-1.60	mA
	I_{IL}		28										GND					H		-1.60	mA
	I_{IL}		29												GND			I		-1.60	mA
	I_{IL}		30													GND		J		-1.60	mA
	I_{CCL}	3005	31														5.0V	Vcc		26.6	mA
	I_{CCH}	3005	32	GND											GND		5.0V	Vcc		2.94	mA
	$I_{CC(SM)}$	3005	33	GND											GND		2.8V	Vcc		6.0	mA
	I_{CEX}		34	GND					4.5V								4.5V	E		50	μA
	I_{CEX}		35								4.5V				GND		4.5V	F		50	μA
T_A=125°C	V_{OL}	3007	36	1.7V	1.7V		1.7V	1.7V	36mA								4.5V	E		0.45	V
	V_{OL}		37								36mA	1.7V	1.7V		1.7V	1.7V		F		0.45	V
	V_{OH}	3006	38	0.8V					-4mA									E	3.3		V
	V_{OH}		39		0.8V				-4mA									E	3.3		V
	V_{OH}		40				0.8V		-4mA									E	3.3		V
	V_{OH}		41					0.8V	-4mA									E	3.3		V
	V_{OH}		42								-4mA	0.8V						F	3.3		V
	V_{OH}		43								-4mA		0.8V					F	3.3		V
	V_{OH}		44								-4mA				0.8V			F	3.3		V
	V_{OH}		45								-4mA					0.8V		F	3.3		V

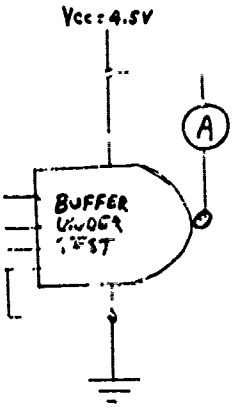


Subgroup	Symbol	MIL-STD-883 Method	Case A+B	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Meas. Terminal	Test Limits MIN	MAX	UNI
			Case C	1	2	NC	3	NC	4	5	6	NC	NC	7	8	9	10				
			Test No.	A	B	X	C	D	E	GND	F	G	H	Y	I	J	Vcc				
2	I_{OS}	3011	46	GND					GND	GND							5.5V	E	-16		mA
TA:125°C	I_{OZ}	↓	47								GND				GND			F	-16		mA
	I_{IH}	3010	48	4.0	GND		GND	GND										A		5.0	μA
	I_{IH}		49	GND	4.0		GND	GND										B		5.0	μA
	I_{IH}		50	GND	GND		4.0	GND										C		5.0	μA
	I_{IH}		51	GND	GND		GND	4.0										D		5.0	μA
	I_{IH}		52									4.0	GND		GND	GND		G		5.0	μA
	I_{IH}		53									GND	4.0		GND	GND		H		5.0	μA
	I_{IH}		54									GND	GND		4.0	GND		I		5.0	μA
	I_{IH}		55									GND	GND		GND	4.0		J		5.0	μA
	I_{IL}	3009	56	GND														A		-1.5	mA
	I_{IL}		57		GND													B		-1.5	mA
	I_{IL}		58				GND											C		-1.5	mA
	I_{IL}		59					GND										D		-1.5	mA
	I_{IL}		60									GND						G		-1.5	mA
	I_{IL}		61										GND					H		-1.5	mA
	I_{IL}		62												GND			I		-1.5	mA
	I_{IL}		63													GND		J		-1.5	mA
	I_{CCL}	3005	64														5.0V	V_{CC}		26.6	mA
	I_{CCH}	3005	65	GND											GND		5.0V	V_{CC}		2.94	mA

Subgroup	Symbol	MIL-STD-883 method	Case A+B	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Meas. Terminal	Test Limits		
			Case C	1	2	NC	3	NC	4	5	6	NC	NC	9	R	9	10				
			Test No.	A	B	X	C	D	E	GND	F	G	H	Y	I	J	V_{CC}		MIN	MAX	Units
3	V_{OL}	3007	66	2.1	2.1		2.1	2.1	36ma.	GND							4.5V	E		0.4	V
T_A:-55°C	V_{OL}	↓	67								36ma.	2.1	2.1		2.	2.1		F		0.4	V
	V_{OH}	3006	68	1.4					-2.0ma.									E	3.3		V
	V_{OH}		69		1.4				-2.0ma.									E	3.3		V
	V_{OH}		70				1.4		-2.0ma.									E	3.3		V
	V_{OH}		71					1.4	-2.0ma.									E	3.3		V
	V_{OH}		72								-2.0ma.	1.4						F	3.3		V
	V_{OH}		73								-2.0ma.		1.4					F	3.3		V
	V_{OH}		74								-2.0ma.				1.4			F	3.3		V
	V_{OH}	↓	75								-2.0ma.					1.4	↓	F	3.3		V
	I_{OS}	3011	76	GND					GND								5.5V	E	16		ma.
	I_{OS}	↓	77								GND				GND			F	16		ma.
	I_{IH}	3010	78	4.0	GND		GND	GND										A		2.0	ma.
	I_{IH}		79	GND	4.0		GND	GND										B		2.0	ma.
	I_{IH}		80	GND	GND		4.0	GND										C		2.0	ma.
	I_{IH}		81	GND	GND		GND	4.0										D		2.0	ma.
	I_{IH}		82									4.0	GND		GND	GND		G		2.0	ma.
	I_{IH}		83									GND	4.0		GND	GND		H		2.0	ma.
	I_{IH}		84									GND	GND		4.0	GND		I		2.0	ma.
	I_{IH}	↓	85									GND	GND		GND	4.0		J		2.0	ma.
	I_{IL}	3009	86	GND														A		-1.6	ma.
	I_{IL}		87		GND													B		-1.6	ma.
	I_{IL}	↓	88				GND											C		-1.6	ma.



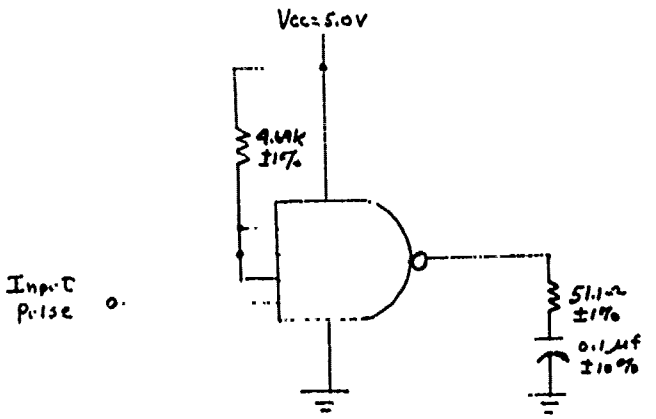
Subgroup	Symbol	MIL-STD-883 Method	Test No.	Case A/B 1	2	3	4	5	6	7	8	9	10	11	12	13	14	Meas. Terminal	Test Limits MIN	MAX
				Case C 1	2	NC	3	NC	4	5	6	NC	NC	7	8	9	10			
				A	B	X	C	D	E	GND	F	G	H	Y	I	J	V_{CC}			
3	I_{IL}	3009	89					GND		GND							5.5V	D		-1.6 mA
T_A=-55°C	I_{IL}		90									GND						G		-1.6 mA
	I_{IL}		91										GND					H		-1.6 mA
	I_{IL}		92												GND			I		-1.6 mA
	I_{IL}		93													GND		J		-1.6 mA
	I_{CCL}	3005	94														5.0V	V_{CC}		26.6 mA
	I_{CCH}	3005	95			GND									GND		5.0V	V_{CC}		2.64 mA
9	t_{PHL}	3003 FIG HERE IN	96	IN						OUT	GND				IN		5.0V	A to E	15	40 ns
T_A=25°C	t_{PHL}		97								OUT							I to F	15	40 ns
	t_{PLH}	3003 FIG HERE IN	98	IN						OUT					IN			A to E	25	80 ns
	t_{PLH}		99								OUT							I to F	25	80 ns
10	t_{PHL}	3003 FIG HERE IN	100	IN						OUT					IN			A to E	15	50 ns
T_A=+125°C	t_{PHL}		101								OUT							I to F	15	50 ns
	t_{PLH}	3003 FIG HERE IN	102	IN						OUT					IN			A to E	45	140 ns
	t_{PLH}		103								OUT							I to F	45	140 ns
11	t_{PHL}	3003 FIG HERE IN	104	IN						OUT					IN			A to E	20	50 ns
T_A=-55°C	t_{PHL}		105								OUT							I to F	20	50 ns
	t_{PLH}	3003	106	IN						OUT					IN			A to E	25	92 ns
	t_{PLH}		107								OUT							I to F	25	92 ns



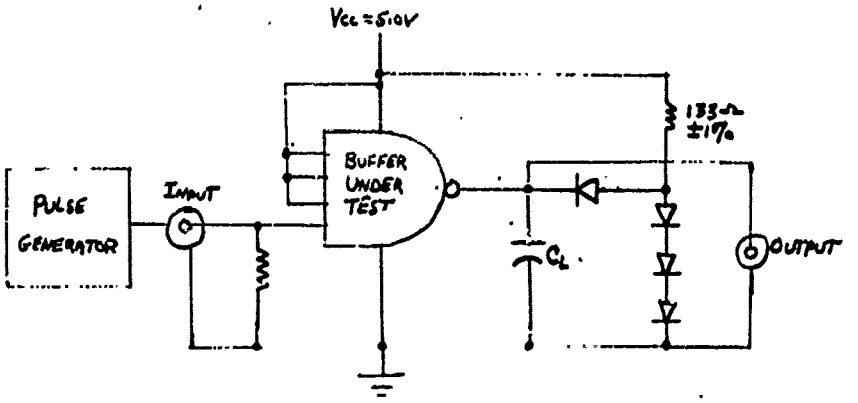
TEST CIRCUIT

CAUTION: Do not connect Ammeter (A) until the Input to the Buffer Under Test is grounded

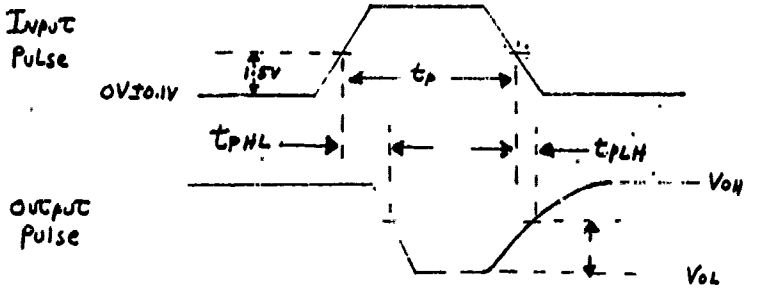
Figure ICEX Test Circuit



NOTES:
1. The Input Pulse Characteristics, are: V_{osu} = 4.0V; PRR = 100 kHz Duty cycle = 50%; t_r (10% to 90%) = 100 n.sec; t_f (90% to 10%) = 100 n.sec
2. All input adjustments are ±5%.



TEST CIRCUIT



NOTES:

1. Input Pulse Characteristics: $V_{GEN} = 4.0V$; PRR = 100KHz; t_p = 1μsec; t_r (10% to 90%) = 20n.sec; t_f (90% to 10%) = 20n.sec
2. Unless otherwise stated, all input adjustments are ±5%.
3. C_L = 50pf. This capacitance includes probe and stray capacitance and shall be measured at 1MHz. The measured capacitance shall be within ±2pf of nominal.
4. All diodes are IN4150 or equivalent.

DTL 945

TABLE I ELECTRICAL PERFORMACE CHARACTERISTICS

TEST	SYMBOL	CONDITIONS	TEMP	LIMITS MIN	LIMITS MAX	UNITS
HIGH-LEVEL OUTPUT VOLTAGE	V_{OH}	V_{CC}=4.5V I_{OH}=-120μa	+25°C -55°C +125°C	3.4 3.3 3.3		VOLTS
LOW-LEVEL OUTPUT VOLTAGE	V_{OL}	V_{CC}=4.5V I_{OL}=16.0ma	+25°C -55°C +125°C		0.40 0.40 0.45	VOLTS
HIGH-LEVEL INPUT VOLTAGE	V_{IH}		+25°C -55°C +125°C	1.9 2.1 1.7		VOLTS
LOW-LEVEL INPUT VOLTAGE	V_{IL}		+25°C -55°C +125°C		1.1 1.4 0.8	VOLTS
HIGH-LEVEL INPUT CURRENT	I_{IH1}	V_{CC}=5.5V V_{IN}=4.0V	+25°C -55°C +125°C		2.0 2.0 5.0	μa
HIGH-LEVEL INPUT CURRENT	I_{IH2}	V_{CC}=5.5V V_{IN}=4.4V	+25°C -55°C +125°C		4.0 4.0 10.0	μa
HIGH-LEVEL INPUT CURRENT	I_{IH3}	V_{CC}=4.0V V_{IN}=4.0V	+25°C -55°C +125°C		10.0 10.0 200	μa
LOW-LEVEL INPUT CURRENT	I_{IL1}	V_{CC}=5.5V V_{IN}=0.0V	+25°C -55°C +125°C		-1.07 -1.07 -1.00	ma

TABLE I CONTINUED

TEST	SYMBOL	CONDITIONS			LIMITS TEMP	LIMITS MIN	LIMITS MAX	UNITS
LOW-LEVEL INPUT CURRENT	I_{IL2}	V_{CC} = 5.5V, V_{IN} = 0.0V			+25°C -55°C +125°C		-3.2 -3.2 -2.8	ma
OUTPUT TRANSISTOR LEAKAGE CURRENT	I_{CEX}	V_{CC} = 5.5V	V_{IN} = 0.0V	V_{OUT} = 5.5V	+25°C		50	μa
SHORT-CIRCUIT OUTPUT CURRENT	I_{OS}	V_{CC} = 5.5V V_{IN} = 0.0V			+25°C -55°C +125°C	-0.700 -0.700 -0.615	-1.34 -1.34 -1.30	ma.
POWER SUPPLY CURRENT	I_{CC}	V_{CC} = 5.0V	V_{IN} = OPEN		+25°C		14	ma.
MAXIMUM POWER SUPPLY CURRENT FLAT PACK	$I_{CC(MAX)}$	V_{CC} = 5.0V	V_{IN} = OPEN		+25°C		16	ma.
MAXIMUM POWER SUPPLY CURRENT TO-5	$I_{CC(MAX)}$	V_{CC} = 5.0V	V_{IN} = OPEN		+25°C		20	ma
CLOCK TO OUTPUT PROPAGATION DELAY TIME HIGH-TO-LOW-LEVEL	t_{PHL1}	C_L = 50 pf	R_L = 332Ω	SEE FIG.	+25°C -55°C +125°C	30 25 30	75 65 90	n.sec
CLOCK TO OUTPUT PROPAGATION DELAY TIME LOW-TO-HIGH LEVEL	t_{PLH1}	C_L = 30 pf	R_L = 2.0KΩ	SEE FIG.	+25°C -55°C +125°C	35 35 40	75 85 100	n.sec
SET-UP TIME	t_{SET-UP}	C_L = 50 pf	R_L = 332Ω	SEE FIG.	+25°C -55°C +125°C	35 45 30		n.sec
RELEASE TIME	$t_{RELEASE}$	C_L = 50 pf	R_L = 332Ω	SEE FIG.	+25°C -55°C +125°C		10 15 8	n.sec

TABLE I CONTINUED

TEST	SYMBOL	CONDITIONS	TEMP	LIMITS MIN	LIMITS MAX	UNITS
R/S TO OUTPUT PROPAGATION DELAY TIME HIGH-TO-LOW LEVEL	t_{PHL2}	C_L = 50pf R_L = 332Ω SEE FIG	+25°C -55°C +125°C	15 15 20	60 60 100	n.sec
R/S TO OUTPUT PROPAGATION DELAY TIME LOW-TO-HIGH LEVEL	t_{PLH2}	C_L = 30pf R_L = 2.05K SEE FIG	+25°C -55°C +125°C	15 15 20	80 80 125	n.sec
CLOCK HIGH-LEVEL INPUT THRESHOLD VOLTAGE	V_{ICH}	C_L = 50pf R_L = 332Ω SEE FIG	+25°C -55°C +125°C	1.9 2.1 1.7		VOLTS
CLOCK LOW-LEVEL INPUT THRESHOLD VOLTAGE	V_{ICL}	C_L = 50pf R_L = 332Ω SEE FIG	+25°C -55°C +125°C		1.1 1.4 0.8	VOLTS
MAXIMUM CLOCK FREQUENCY	f_{max}	C_L = 50pf R_L = 332Ω SEE FIG	+25°C		3.0	MHZ

TABLE III GROUP A INSPECTION FOR DEVICE TYPE 01

TERMINAL CONDITIONS (PINS NOT DESIGNATED ARE OPEN)

Subgroup	Symbol	MIL-STD-883 Method	Case A&B Case C Test No.	1 NC	2 Clock	3 S_1	4 S_2	5 C_D	6 $\overline{Q}$	7 GND	8 NC	9 $\overline{Q}$	10 S_D	11 C_2	12 C_1	13 NC	14 V_{CC}	Meas. Terminal	Test Limits MIN	Test Limits MAX	Units
1	V_{OH} ③	3006	1		A	1.9V	1.9V	B	-12mA	GND				GND	GND		4.5V	$\overline{Q}_1$	3.4		V
T_A=25°C	V_{OH}		2		A	GND	GND					-12mA	B	1.9V	1.9V			$\overline{Q}_D$	3.4		V
	V_{OH}		3		A	GND			-12mA				1.1V					$\overline{Q}_2$	3.4		V
	V_{OH} ③		4		A			1.1V				-12mA			GND			$\overline{Q}_1$	3.4		V
	V_{OH}		5		A	GND	GND		-12mA				B	1.1V	1.1V			GND	3.4		V
	V_{OL} ③		6		A	1.1V	1.1V	B				-12mA		GND	GND			Q_1	3.4		V
	V_{OL} ③	3007	7					B	16mA				1.9V					Q_D		0.40	V
	V_{OL} ③		8					1.9V				16mA	B					Q_2		0.40	V
	I_{IH1}	3010	9		GND	4.0V	GND										5.5V	S_1		2.0	μA
	I_{IH1}		10		GND	GND	4.0V											S_2		2.0	μA
	I_{IH1}		11		GND									4.0V	GND			C_2		2.0	μA
	I_{IH1}		12		GND									GND	4.0V			C_1		2.0	μA
	I_{IH2} ③	3010	13		A	GND		4.0V										C_D		4.0	μA
	I_{IH2}		14		A								4.0V		GND			S_D		4.0	μA
	I_{IH3}	3010	15		4.0V	GND									GND		4.0V	Clock		10.0	μA
	I_{IL1}	3009	16		5.5V	GND	5.5V										5.5V	S_1		-1.07	mA
	I_{IL1}		17		5.5V	5.5V	GND											S_2		-1.07	mA
	I_{IL1}		18		5.5V									GND	5.5V			C_2		-1.07	mA
	I_{IL1}		19		5.5V									5.5V	GND			C_1		-1.07	mA
	I_{IL2} ③	3009	20					GND							GND			C_D		-3.20	mA
	I_{IL2}		21			GND							GND					S_D		-3.20	mA
	I_{IL2} ③		22		GND			B										Clock		-3.20	mA
	I_{IL2}		23		GND								B					Clock		-3.20	mA

Subgroup	Symbol	MIL-STD-883 Method	Case A or B	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Meas. Terminal	Test Limits MIN	Test Limits MAX	Test Limits UNITS
			Case C	NC	1	2	3	NC	4	5	NC	6	7	8	9	NC	10				
			Test No.	NC	CLOCK	S1	S2	C0	Q	GND	NC	$\overline{Q}$	S0	C2	C1	NC	Vcc				
1 T_A=25°C	I_{CEX}		24						5.5V	GND			GND				5.5V	Q		50	μa
	I_{CEX} 3]		25					GND		↓		5.5V					↓	$\overline{Q}$		50	μa
	I_{OS}	3011	26						GND				GND					Q	-0.70	-1.34	ma
	I_{OS} 3]	↓	27					GND				GND					↓	$\overline{Q}$	-0.70	-1.34	ma
	I_{CC}	3005	29														5.0	Vcc		14.0	ma
	$I_{CC(MIN)}$	3005	29A														8.0	Vcc		11.0	ma
	$I_{CC(MIN)}$	↓	29B														↓	Vcc		20.0	ma
2 T_A=125°C	V_{OH} 3]	3006	30		A	1.7V	1.7V	B	-12μa						GND		4.5V	Q	3.3		V
	V_{OH}		31		A	GND						-10μa	B	1.7V	1.7V			$\overline{Q}$	3.3		V
	V_{OH}		32		A	GND			-12μa				0.8V					Q	3.3		V
	V_{OH} 4]		33		A			0.8V				-12μa			GND			$\overline{Q}$	3.3		V
	V_{OH}		34		A	GND	GND		-12μa				B	0.8V	0.8V			Q	3.3		V
	V_{OH} 3]	↓	35		A	0.8V	0.8V	B				-12μa		GND	GND			$\overline{Q}$	3.3		V
	V_{OL} 3]	3007	36					B	16ma				1.7V					Q		0.45	V
	V_{OL} 5]	↓	37					1.7V				16ma	B				↓	$\overline{Q}$		0.45	V
	I_{IH1}	3010	38		GND	4.0V	GND										5.5V	S1		6.0	μa
	I_{IH1}		39		GND	GND	4.0V											S2		5.0	μa
	I_{IH1}		40		GND									4.0V	GND			C2		5.0	μa
	I_{IH1}	↓	41		GND									GND	4.0V			C1		5.0	μa
	I_{IH2} 4]	3010	42		A	GND		4.0V										C0		10.0	μa
	I_{IH2}	↓	43		A					↓			4.0V		GND		↓	S0		10.0	μa

Subgroup	Symbol	MIL-STD-883 Method	Case A+B / Case C / Test No.	1 / NC / NC	2 / 1 / Clock	3 / 2 / S1	4 / 3 / S2	5 / NC / CD	6 / 4 / Φ	7 / 5 / GND	8 / NC / NC	9 / 6 / $\overline{\Phi}$	10 / 7 / SD	11 / 8 / C2	12 / 9 / C1	13 / NC / NC	14 / 10 / Vcc	Meas. Terminal	Test Limits MIN	MAX	Units
2 T_A=125°C	I_{IO3}	3010	44		4.0V	GND				GND					GND		4.5V	Clock		20.0	μA
	I_{IL1}	3009	45		5.5V	GND	5.5V	GND									5.5V	S1		-1.00	mA
	I_{IL1}		46		5.5V	5.5V	GND	GND										S2		-1.00	mA
	I_{IL1}		47		5.5V								GND	GND	5.5V			C2		-1.00	mA
	I_{IL1}		48		5.5V								GND	5.5V	GND			C1		-1.00	mA
	I_{IL2} 4]	3009	49					GND					GND		GND			CD		-2.00	mA
	I_{IL2}		50			GND		GND					GND					SD		-2.50	mA
	I_{IL2} 3]		51		GND			B										Clock		-2.00	mA
	I_{IL2}		52		GND								B					Clock		-2.50	mA
	I_{OS}	3011	53						GND				GND					Φ	-0.415	-1.30	mA
	I_{OS} 3]		54					GND				GND						$\overline{\Phi}$	-0.615	-1.20	mA
3 T_A=-55°C	V_{OL} 3]	3006	55		A	2.1V	2.1V	B	-120μA						GND		4.5V	Φ	3.3		V
	V_{OB}		56		A	GND						-120μA	B	2.1V	2.1V			Φ/$\overline{\Phi}$	3.3		V
	V_{OB}		57		A	GND			-120μA				1.4V					Φ	3.3		V
	V_{OB} 4]		58		A			1.4V				-120μA			GND			$\overline{\Phi}$	3.3		V
	V_{OS}		59		A	GND	GND		-120μA				B	1.4V	1.4V			Φ/$\overline{\Phi}$	3.3		V
	V_{OH} 3]		60		A	1.4V	1.4V	B				-120μA		GND	GND			Φ/$\overline{\Phi}$	3.3		V
	V_{OL} 3]	3007	61					B	16mA				2.1V					Φ/$\overline{\Phi}$		0.40	V
	V_{OL} 5]		62					2.1V				16mA	B					$\overline{\Phi}$		0.40	V

Subgroup	Symbol	MIL-STD-883 Method	Case A & B / Case C / Test No.	1 / NC / NC	2 / 1 / Clock	3 / 2 / S1	4 / 3 / S2	5 / NC / CD	6 / 4 / Q	7 / 5 / GND	8 / NC / NC	9 / 6 / $\overline{Q}$	10 / 7 / SD	11 / 8 / C2	12 / 9 / C1	13 / NC / NC	14 / 10 / V_{CC}	Meas. Terminal	Test Limits MIN	MAX	UNITS
3 T_A=-55°C	I_{IN1}	3010	63		GND	4.0V	GND			GND							5.5V	S_1		2.0	μa
	I_{IN1}		64		GND	GND	4.0V											S_2		2.0	μa
	I_{IN1}		65		GND									4.0V	GND			C_2		2.0	μa
	I_{IN1}		66		GND									GND	4.0V			C_1		2.0	μa
	I_{IN2} 4]	3010	67		A	GND		4.0V										C_D		4.0	μa
	I_{IN2}		68		A								4.0V		GND			S_D		4.0	μa
	I_{IN3}	3010	69		4.0V	GND									GND		4.0V	Clock		10.0	μa
	I_{I1}	3009	70		5.5V	GND	5.5V	GND									5.5V	S_1		-1.07	ma
	I_{I1}		71		5.5V	5.5V	GND	GND										S_2		-1.11	ma
	I_{I1}		72		5.5V								GND	GND	5.5V			C_2		1.07	ma
	I_{I1}		73		5.5V								GND	5.5V	GND			C_1		-1.07	ma
	I_{I2a} 4]	3009	74					GND					GND	GND				C_D		-3.20	ma
	I_{I2a}		75			GND		GND					GND					S_D		-3.20	ma
	I_{I2a} 3]		76		GND			B										Clock		-3.20	ma
	I_{I2a}		77		GND								B					Clock		-3.20	ma
	I_{OS}	3011	78						GND				GND					Q	-0.70	-1.34	ma
	I_{OS} 3]		79					GND				GND						$\overline{Q}$	-0.70	-1.34	ma
9 T_A=25°C	t_{PHL1}	3003 FIG MEAS IN	80		IN	IN-B	$\overline{Q}$	5.0V	OUT			OUT	5.0V	Q	IN-B		5.0V		30	75	n.sec.
	t_{PLH1}		81		IN	IN-B	Q	5.0V	OUT			OUT	5.0V	Q	IN-B				35	75	n.sec.
	t_{SET-UP}	FIG MEAS IN	82		IN-A	IN-B	$\overline{Q}$	5.0V	OUT				5.0V	Q	IN-B			Q	48	2.2	μ.sec.
	$t_{RECOVERY}$		83		IN-A	IN-B	$\overline{Q}$	GND				OUT	B	Q	IN-B			$\overline{Q}$		0.4	V

Subgroup	Symbol	MIL-STD-883 Method	Case A+B / Case C Test No.	1 / NC	2 / 1	3 / 2	4 / 3	5 / NC	6 / 4	7 / 5	8 / NC	9 / 6	10 / 7	11 / 8	12 / 9	13 / NC	14 / 10	Meas. Terminal	Test Limits MIN	MAX	UNITS
9 T_A=25°C	t_{PHL2}	3003 FIG HERE IN	84		IN-A	IN-A	Q	IN-B	OUT	GND				Q			5.0V	Q	15	60	n.sec
	t_{PLH2}		85		IN-A		Q					OUT	IN-B	Q	IN-A			Q	15	60	n.sec
	t_{PHL2}		86		IN-A	IN-A	Q	IN-B				OUT		Q				Q	15	80	n.sec
	t_{PLH2}		87		IN-A		Q		OUT				IN-B	Q	IN-A			Q	15	80	n.sec
	V_{IOH}	FIG HERE IN	88		B=1.4V		Q					OUT		Q				Q	4	6	m.sec
	V_{IOL}		89		B=1.1V		Q					OUT	B	Q				Q		0.40	V
	F_{MAX}	FIG	90		IN		Q		OUT					Q				Q	1.5		MHZ
10 T_A=125°C	t_{PHL}	3003 FIG HERE IN	91		IN	IN-B	Q	5.0V	OUT			OUT	5.0V	Q	IN-B				30	90	n.sec
	t_{PLH}		92		IN	IN-B	Q	5.0V	OUT			OUT	5.0V	Q	IN-B				40	100	n.sec
	t_{SET-UP}	FIG HERE IN	93		IN-A	IN-B	Q	5.0V	OUT				5.0V	Q	IN-B				1.8	2.2	μsec
	t_{PULSE}		94		IN-A	IN-B	Q	5.0V				OUT	B	Q	IN-B					0.45	V
	t_{PHL2}	3003 FIG HERE IN	95		IN-A	IN-A	Q	IN-B	OUT					Q					20	100	n.sec
	t_{PLH2}		96		IN-A		Q					OUT	IN-B	Q	IN-A				20	100	n.sec
	t_{PHL2}		97		IN-A	IN-A	Q	IN-B				OUT		Q					20	125	n.sec
	t_{PLH2}		98		IN-A		Q		OUT				IN-B	Q	IN-A				20	125	n.sec
	V_{IOH}	FIG HERE IN	99		B=1.7V		Q					OUT		Q					4	6	m.sec
	V_{IOL}		100		B=0.9V		Q					OUT	B	Q						0.45	V
11 T_A=-55°C	t_{PHL1}	3003 FIG HERE IN	101		IN	IN-B	Q	5.0V	OUT			OUT	5.0V	Q	IN-B				25	65	n.sec
	t_{PLH1}		102		IN	IN-B	Q	5.0V	OUT			OUT	5.0V	Q	IN-B				35	85	n.sec
	t_{SET-UP}	FIG HERE IN	103		IN-A	IN-B	Q	5.0V	OUT				5.0V	Q	IN-B				1.8	2.2	μsec
	t_{PULSE}		104		IN-A	IN-B	Q	5.0V				OUT	B	Q	IN-B					0.40	V

Subgroup	Symbol	MIL-STD-883 Method	Case A+B / Case C / Test No.	1 / NC / NC	2 / I / Clock	3 / 2 / S_1	4 / 3 / S_2	5 / NC / C_0	6 / 4 / Q	7 / 5 / GND	8 / NC / NC	9 / 6 / $\overline{Q}$	10 / 7 / S_0	11 / 8 / C_2	12 / 9 / C_1	13 / NC / NC	14 / 10 / V_{CC}	Meas. Terminal	Test Limits MIN	MAX	UNITS
11 T_A=-55°C	t_{PHL2} [4]	3003 Fig Here in	105		IN-A	IN-A	Q	IN-B	OUT	GND				Q			5.0V	Q	15	60	n.sec
	t_{PLH2}		106		IN-A		Q					OUT	IN-B	Q	IN-A			Q	15	60	n.sec
	t_{PLH2} [4]		107		IN-A	IN-A	Q	IN-B				OUT		Q				Q	15	80	n.sec
	t_{PHL2}		108		IN-A		Q		OUT				IN-B	Q	IN-A			Q	15	80	n.sec
	V_{IEH}	Fig Here in	109		H=2.0V		Q					OUT		Q				Q	1.8	2.2	Asec
	V_{IEL}		110		A=1.0V		Q					OUT	B	Q				Q		0.40	V

NOTES FOR TABLE III

A = INITIALLY GROUND; THEN 4.0V. FOR 100 n.sec. MINIMUM; THEN GROUND (SWITCHING SHOULD BE BUFFERED SO NO BOUNCE OCCURS)

B = INITIALLY Vcc; THEN GROUND FOR 100 n.sec. MINIMUM; THEN Vcc

1] Test Sequence:

a. Make all circuit connections
b. Always perform "B" switching first if applicable
c. Perform "A" switching next if applicable
d. Make measurement

2] When Q & $\overline{Q}$ show out, both outputs shall be tested

3] See Table IIIA when performing this test on Case C

4] Do not perform this test on Case C

5] The C_D connection is not needed when testing case C

TABLE III.A INSPECTION FOR DEVICE TYPE 01

TERMINAL CONDITIONS (PINS NOT DESIGNATED ARE OPEN)

Subgroup	Symbol	MIL-STD-883 Test No.	Case C Test No.	NC	1	2	3	NC	4	5	NC	6	7	8	9	NC	10	Meas. Terminal	Test Limits Min	Max	Units
				Nc	clock	S1	S2	Nc	Q	GND	Nc	$\overline{Q}$	S_D	C_2	C_1	Nc	V_{CC}				
1	V_{OH}	3006	1-A		A	C	C			GND				D	D		4.5V	$\overline{Q}$	3.4		V
T_A=25°C	V_{OH}	↓	6-A		A	1.1V	1.1V							D	D			$\overline{Q}$	3.4		V
	V_{OL}	3007	7-A		A	GND							1.9V					Q		0.40	V
	I_{IL2}	3009	22-A		E	GND	GND										5.5V	Clock		-3.20	mA
	I_{IEX}		25-A		A	GND	GND						5.5V					$\overline{Q}$		50	μA
	I_{OS}	3011	27-A		A	GND	GND						GND					$\overline{Q}$	-0.300	-1.34	mA
2	V_{OH}	3006	30-A		A	C	C							D	D		4.5V	Q	3.3		V
T_A=125°C	V_{OH}	↓	35-A		A	0.9V	0.9V							D	D			$\overline{Q}$	3.3		V
	V_{OL}	3007	36-A		A	GND							1.7V					Q		0.45	V
	I_{IL2}	3009	51-A		E	GND	GND										5.5V	Clock		-2.90	mA
	I_{OS}	3011	54-A		A	GND	GND						GND					$\overline{Q}$	-0.345	-1.30	mA
3	V_{OH}	3006	55-A		A	C	C							D	D		4.5V	Q	3.3		V
T_A=-55°C	V_{OH}	↓	60-A		A	1.4	1.4							D	D			$\overline{Q}$	3.3		V
	V_{OL}	3007	61-A		A	GND							2.1V					Q		0.40	V
	I_{IL2}	3009	76-A		E	GND	GND										5.5V	Clock		-3.20	mA
	I_{OS}	3011	79-A		A	GND	GND						GND					$\overline{Q}$	-0.300	-1.34	mA

NOTES FOR TABLE III A

A = INITIALLY GROUND; THEN 40V FOR 100 n.sec MINIMUM; THEN GROUND (SWITCHING SHOULD BE BUFFERED SO NO BOUNCE OCCURS)

C = INITIALLY GROUND; THEN HIGH LEVEL INPUT VOLTAGE (25°C = 1.9V; -55°C = 2.1V; +125°C = 1.7V)

D = INITIALLY OPEN; THEN GROUND

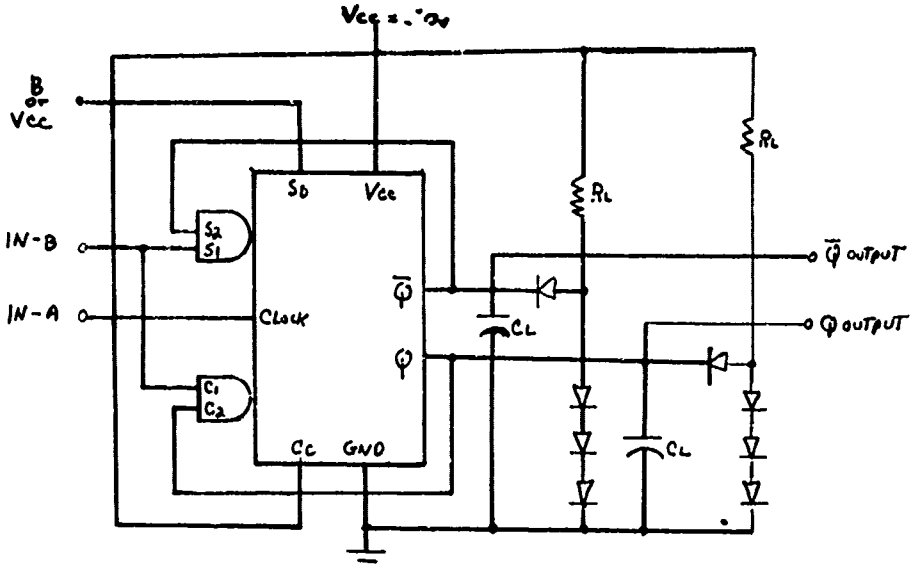
E = MAKE ALL CIRCUIT CONNECTIONS ... THEN CONNECT AMMETER BETWEEN THE CLOCK INPUT AND GROUND AND MAKE MEASUREMENT

1) TEST SEQUENCE

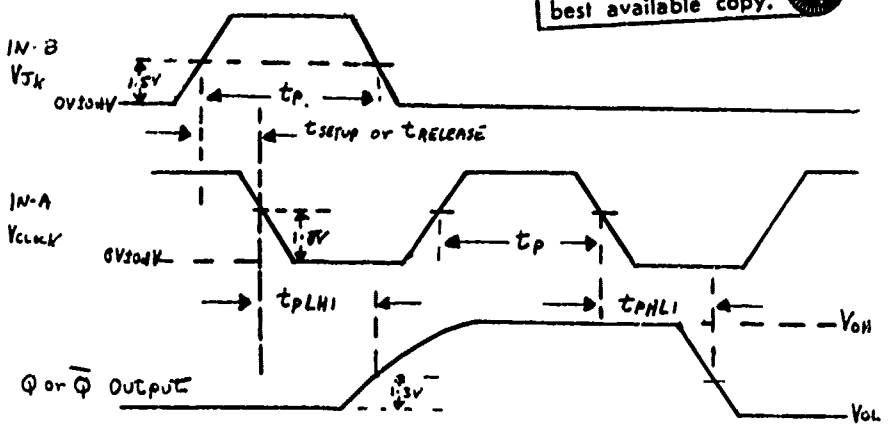
a. MAKE ALL CIRCUIT CONNECTIONS
b. PERFORM A SWITCHING
c. PERFORM C AND D SWITCHING
d. PERFORM A SWITCHING AGAIN AND MAKE MEASUREMENT

2) MAKE ALL CONNECTIONS AND PERFORM A SWITCHING BEFORE CONNECTING AMMETER TO $\overline{\Phi}$.

Figure for Clock Delay – t_{set-up} & $t_{release}$



TEST CIRCUIT



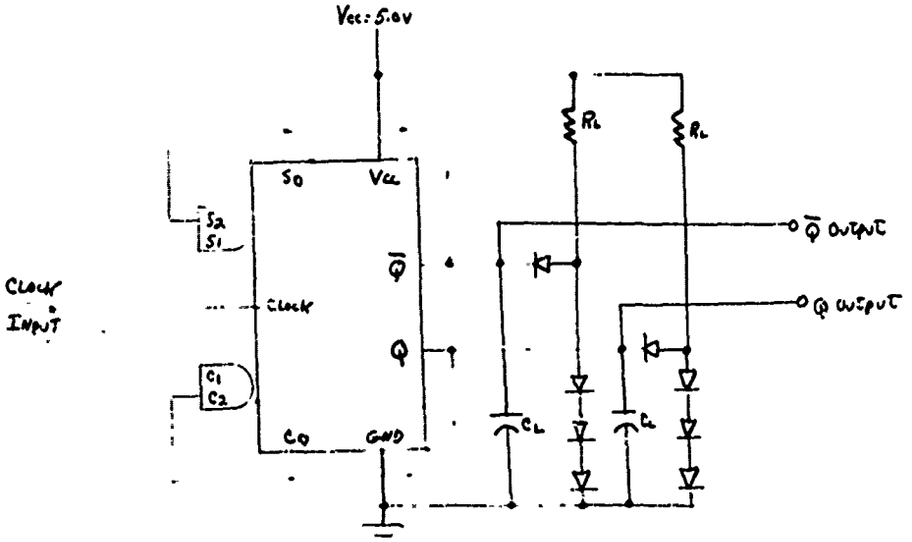
VOLTAGE WAVEFORMS

NOTES:

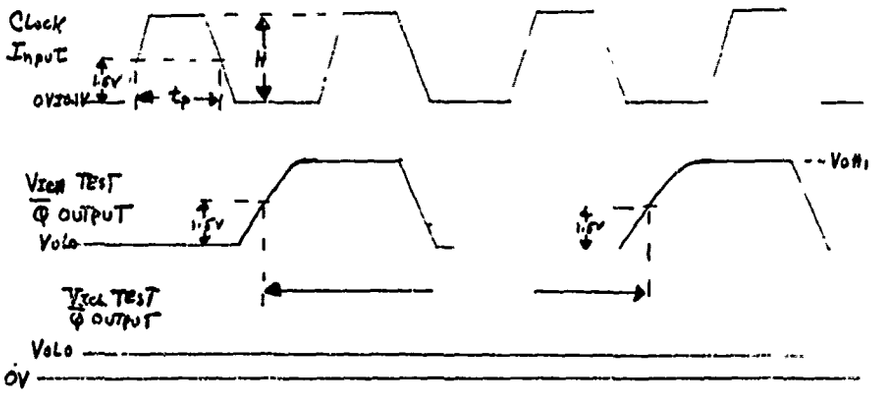
1. IN-A (CLOCK PULSE) CHARACTERISTICS: V_{GEN} = 3.0V; PRR = 1 MHz; t_p = 60 n.sec; t_r (10% to 90%) = 20 n.sec; t_f (90% to 10%) = 20 n.sec
2. IN-B (JK PULSE) CHARACTERISTICS: V_{GEN} = 3.0V; PRR = 1 MHz; t_p = 60 n.sec; t_r (10% to 90%) = 20 n.sec; t_f (90% to 10%) = 20 n.sec.
3. All diodes are IN4150 or equivalent.
4. C_L = 50pf for t_{PHL} measurements and C_L = 30pf for t_{PLH} measurements. This capacitance shall include probe and stray and is measured at 1 MHz. The capacitance should be within ±2 pf of nominal.
5. R_L = 332Ω ±1% for t_{PHL} measurements and R_L = 2.05KΩ ±1% for t_{PLH} measurements.
6. All input adjustments are ±5%
7. The t_{PHL1} and t_{PLH1} measurements are made after the t_{SET-up} measurement.

8. When testing f_{max}, adjust the clock input pulse frequency to 8.0 MC. An output pulse shall be present and the frequency of the output shall meet the requirements of Table III when measured at the 1.5V level.

Figure for V_{ICH} & V_{ICL}



TEST CIRCUIT

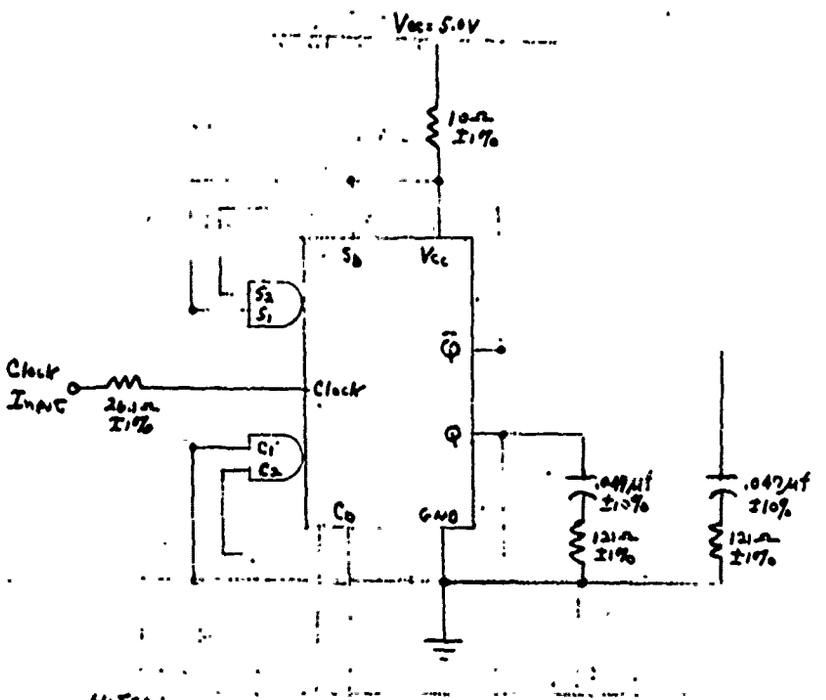


VOLTAGE WAVEFORMS

NOTES:

1. Clock Input pulse CHARACTERISTICS: V_{GEN} = See Note 2; PRR = 400 Hz; t_p = 1.25 m.s.; t_r (10% to 90%) = 0.5ms; t_f (90% to 10%) = 0.5ms
2. The amplitude of the Clock Input Pulse (V_{GEN}) shall be adjusted to the requirements of Table III; Clock column.
3. For the V_{ICH} test, an output pulse shall be present and the period of the output pulse shall meet the requirements of Table III
4. For the V_{ICL} test, make all circuit connections, perform the B switching and make the output measurement. There shall be no output pulse present and the output voltage level shall meet the requirements of Table III.

5. All diodes are IN9150. or equivalent.
6. C_L: 50pf ± 2pf. This capacitance includes probe and stray capacitance and is measured at 1 mHz.
7. R_L: 332Ω ± 1%
8. Unless otherwise stated, all input adjustments are ±5%.

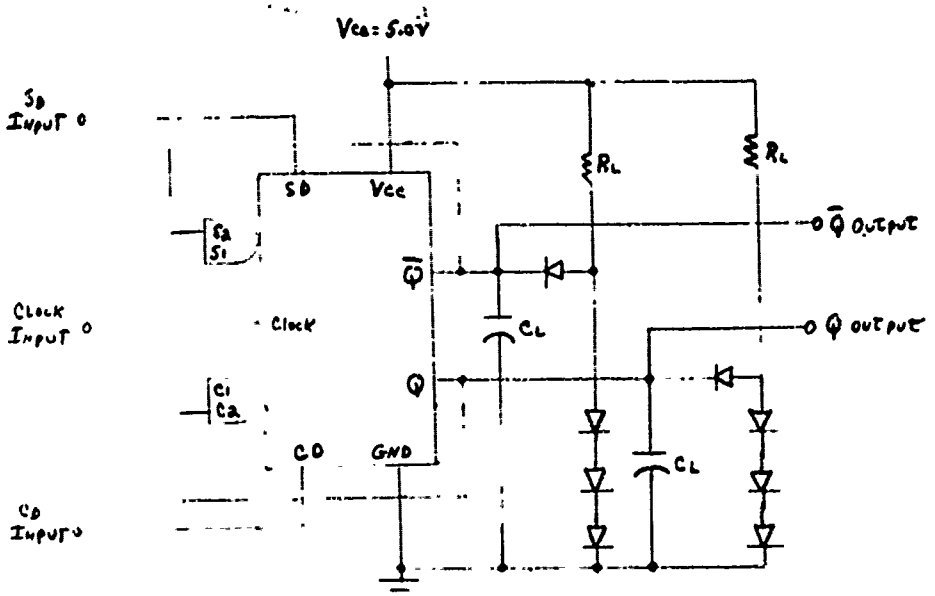


NOTES:

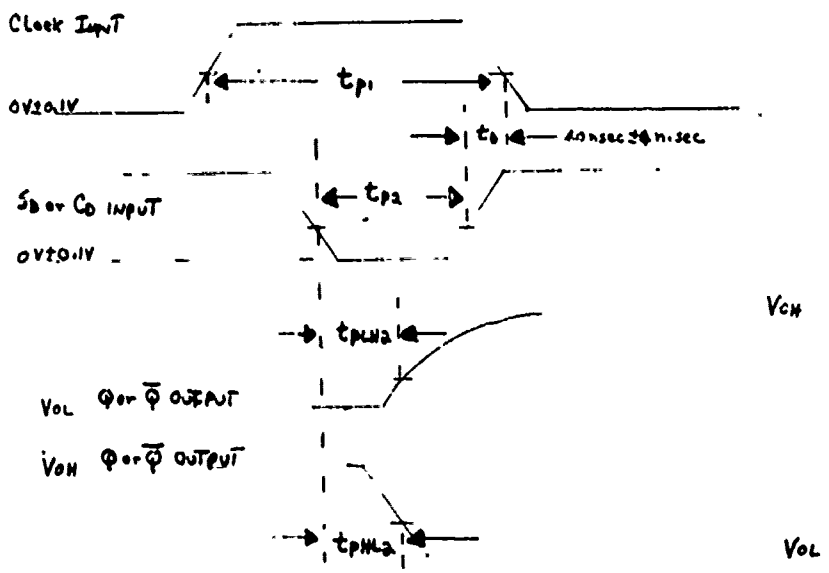
1. Clock Input Pulse Characteristics: V_{GEN} = 4.0V; PRR = 100KHZ; Duty Cycle = 50%; t_r (10% to 90%) = 20n.sec; t_f (90% to 10%) = 20 n.sec
2. All input adjustments are ±5%.

BURN IN AND LIFE TEST CIRCUIT

Figure for R/S Delay



TEST CIRCUIT



VOLTAGE WAVEFORMS

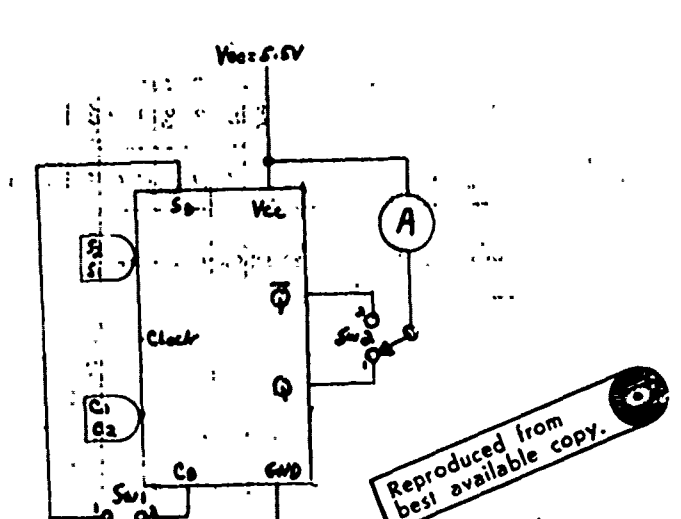
NOTES:

1. Clock Input pulse CHARACTERISTICS: V_{GEN} = 3.0V; PRR = 250KHz; t_{p1} = 600 n.sec; t_r (10% to 90%) = 20 n.sec; t_f (90% to 10%) = 20 n.sec.
2. SD or CD Input pulse characteristics: V_{GEN} = 3.0V; PRR = 250KHz; t_{p2} = 200 n.sec t_r (10% to 90%) = 20 n.sec; t_f (90% to 10%) = 20 n.sec
3. Unless otherwise stated, all input adjustments are ±5%

4. All diodes are 1N4150 or equivalent

5. C_L = 50pf for t_{PHL} measurements and C_L = 30pf for t_{PLH} measurements. This capacitance shall include probe and stray capacitance and is measured at 1 MHz. The capacitance shall be within ±2pf of nominal.

6. R_L = 833Ω ±1% for t_{PHL} measurements and R_L = 2.05K ±1% for t_{PLH} measurements.

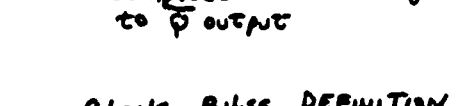


TEST CIRCUIT

NOTES:

1. Place Sw1 in position 1; Sw2 in position 1 and make measurement using Ammeter (A).
2. Place Sw1 in position 2; Sw2 in position 2 and make measurement using Ammeter (A).
3. CAUTION: When performing test 26-A of Table III-A, complete all switching before connecting Ammeter (A) to $\overline{Q}$ output

CLOCK PULSE DEFINITION



Description

These JK flip-flops are based on the master-slave principle and each has AND gate inputs for entry into the master section which are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operations is as follows:

1. Isolate slave from master
2. Enter Information from AND gate inputs to master.
3. Disable AND gate inputs
4. Transfer information from master and slave.

Appendix D

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